LTC4267-3

Power over Ethernet IEEE 802.3af PD Interface with Integrated Switching Regulator

FEATURES

- **Complete Power Interface Port for IEEE 802®.3af Powered Device (PD)**
- **Onboard 100V, UVLO Switch**
- **Constant-Frequency 300kHz Operation**
- **Precision Dual Level Inrush Current Limit**
- **Integrated Current Mode Switching Regulator**
- Onboard 25k Signature Resistor with Disable
- Programmable Classification Current (Class 0-4)
- Thermal Overload Protection
- Power Good Signal
- Integrated Error Amplifier and Voltage Reference
- Low Profile 16-Pin SSOP or DFN Packages

APPLICATIONS

- IP Phone Power Management
- Wireless Access Points
- Security Cameras
- Power over Ethernet

DESCRIPTION

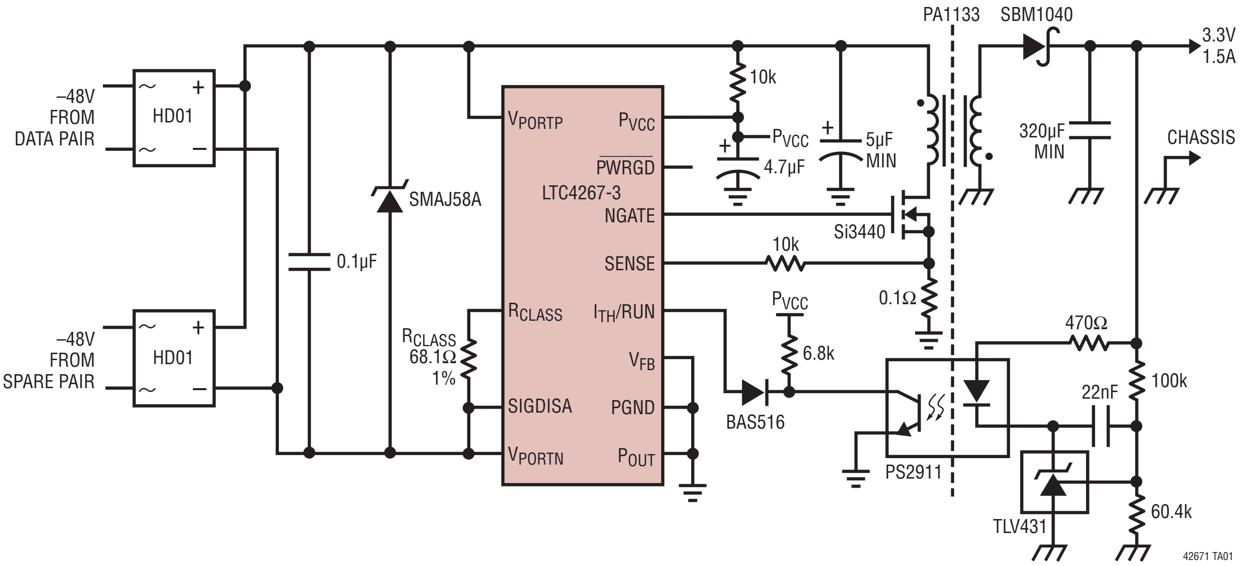
The LTC®4267-3 combines an IEEE 802.3af compliant Powered Device (PD) interface with a 300kHz current mode switching regulator, providing a complete power solution for PD applications. The LTC4267-3 integrates the 25k signature resistor, classification current source, thermal overload protection, signature disable and power good signal along with an undervoltage lockout optimized for use with the IEEE-required diode bridge. The LTC4267-3 provides an increased operational current limit, maximizing power available for class 3 applications.

The 300kHz current mode switching regulator provides higher output power or smaller external size compared to its lower frequency counterparts. The LTC4267-3 is designed for driving a 6V rated N-channel MOSFET and features programmable slope compensation, soft-start, and constant-frequency operation, minimizing noise even with light loads. The LTC4267-3 includes an onboard error amplifier and voltage reference allowing use in both isolated and nonisolated configurations.

The LTC4267-3 is available in a space saving, low profile 16-pin SSOP or DFN packages.

TYPICAL APPLICATION

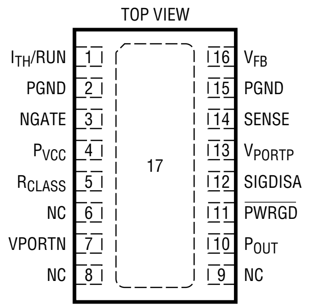
Class 2 PD with 3.3V Isolated Power Supply



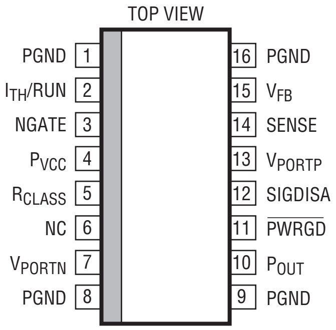
ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{PORTN} with Respect to V_{PORTP} Voltage ... 0.3V to –100V
P_{OUT}, SIGDISA, $\overline{PWRGD}$
  Voltage .... V_{PORTN} + 100V to V_{PORTN} –0.3V
P_{VCC} to PGND Voltage (Note 2)
  Low Impedance Source .... –0.3V to 8V
  Current Fed .... 5mA into P_{VCC}
$\overline{R_{CLASS}}$ Voltage .... V_{PORTN} + 7V to V_{PORTN} – 0.3V
$\overline{PWRGD}$ Current 10mA
R_{CLASS} Current 100mA
NGATE to PGND Voltage .... –0.3V to P_{VCC}
V_{FB}, I_{TH}/RUN to PGND Voltages .... –0.3V to 3.5V
SENSE to PGND Voltage .... –0.3V to 1V
NGATE Peak Output Current (<10μs) 1A
Operating Ambient Temperature Range
  LTC4267C-3 .... 0°C to 70°C
  LTC4267I-3 .... –40°C to 85°C
Junction Temperature .... 150°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PIN CONFIGURATION



DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43.5°C/W
EXPOSED PAD (PIN 17) MUST BE SOLDERED
TO ELECTRICALLY ISOLATED PCB HEAT SINK



GN PACKAGE
16-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 90°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4267CDHC-3#PBF	LTC4267CDHC-3#TRPBF	4267-3	16-Lead (5mm × 3mm) Plastic DFN	0°C to 70°C
LTC4267IDHC-3#PBF	LTC4267IDHC-3#TRPBF	4267-3	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4267CGN-3#PBF	LTC4267CGN-3#TRPBF	4267-3	16-Lead Narrow Plastic SSOP	0°C to 70°C
LTC4267IGN-3#PBF	LTC4267IGN-3#TRPBF	4267I-3	16-Lead Narrow Plastic SSOP	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC4267CDHC-3	LTC4267CDHC-3#TR	4267-3	16-Lead (5mm × 3mm) Plastic DFN	0°C to 70°C
LTC4267IDHC-3	LTC4267IDHC-3#TR	4267-3	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4267CGN-3	LTC4267CGN-3#TR	4267-3	16-Lead Narrow Plastic SSOP	0°C to 70°C
LTC4267IGN-3	LTC4267IGN-3#TR	4267-3	16-Lead Narrow Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{PORTN}	Supply Voltage	Voltage with Respect to V_{PORTP} Pin					
	Maximum Operating Voltage	(Notes 4, 5, 6)	●			–57	V
	Signature Range		●	–1.5		–9.5	V
	Classification Range		●	–12.5		–21	V
	UVLO Turn-On Voltage		●	–34.8	–36	–37.2	V
	UVLO Turn-Off Voltage		●	–29.3	–30.5	–31.5	V
V_{TURNON}	P_{VCC} Turn-On Voltage	Voltage with Respect to PGND	●	7.6	8.7	9.2	V
$V_{TURNOFF}$	P_{VCC} Turn-Off Voltage	Voltage with Respect to PGND	●	4.6	5.7	7	V
V_{HYST}	P_{VCC} Hysteresis	V_{TURNON} – $V_{TURNOFF}$	●	1	3		V
$V_{CLAMP1mA}$	P_{VCC} Shunt Regulator Voltage	I_{PVCC} = 1mA, V_{ITH}/RUN = 0V, Voltage with Respect to PGND	●	8.3	9.4	10.3	V
V_{MARGIN}	$V_{CLAMP1mA}$ – V_{TURNON} Margin		●	0.05	0.6		V
I_{VPORTN_ON}	V_{PORTN} Supply Current when ON	V_{PORTN} = –48V, P_{OUT}, $\overline{PWRGD}$, SIGDISA Floating	●			3	mA
I_{PVCC_ON}	P_{VCC} Supply Current	(Note 7)					
	Normal Operation	V_{ITH}/RUN – PGND = 1.3V	●		240	350	µA
	Start-Up	P_{VCC} – PGND = V_{TURNON} – 100mV	●		40	90	µA
I_{VPORTN_CLASS}	V_{PORTN} Supply Current During Classification	V_{PORTN} = –17.5V, P_{OUT} Tied to V_{PORTP}, R_{CLASS}, SIGDISA Floating (Note 8)	●	0.35	0.5	0.65	mA
ΔI_{CLASS}	Current Accuracy During Classification	10mA < I_{CLASS} < 40mA, –12.5V ≤ V_{PORTN} ≤ –21V (Note 9)	●			±3.5	%
$R_{SIGNATURE}$	Signature Resistance	–1.5V ≤ V_{PORTN} ≤ –9.5V, P_{OUT} Tied to V_{PORTP}, IEEE 802.3af 2-Point Measurement (Notes 4, 5)	●	23.25		26.00	kΩ
$R_{INVALID}$	Invalid Signature Resistance	–1.5V ≤ V_{PORTN} ≤ –9.5V, SIGDISA and P_{OUT} Tied to V_{PORTP}, IEEE 802.3af 2-Point Measurement (Notes 4, 5)	●		9	11.8	kΩ
V_{IH}	Signature Disable High Level Input Voltage	With Respect to V_{PORTN} High Level Invalidates Signature (Note 10)	●	3		57	V
V_{IL}	Signature Disable Low Level Input Voltage	With Respect to V_{PORTN} Low Level Enables Signature	●			0.45	V
R_{INPUT}	Signature Disable, Input Resistance	With Respect to V_{PORTN}	●	100			kΩ
V_{PG_OUT}	Power Good Output Low Voltage	I = 1mA V_{PORTN} = –48V, $\overline{PWRGD}$ Referenced to V_{PORTN}	●			0.5	V
	Power Good Trip Point	V_{PORTN} = –48V, Voltage between V_{PORTN} and P_{OUT} (Note 11)					
V_{PG_FALL}		P_{OUT} Falling	●	1.3	1.5	1.7	V
V_{PG_RISE}		P_{OUT} Rising	●	2.7	3	3.3	V
I_{PG_LEAK}	Power Good Leakage Current	V_{PORTN} = 0V, $\overline{PWRGD}$ FET Off, $V_{\overline{PWRGD}}$ = 57V	●			1	µA
R_{ON}	On-Resistance	I = 300mA, V_{PORTN} = –48V, Measured from V_{PORTN} to P_{OUT} (Note 11)			1	1.6	Ω
			●			2	Ω
$V_{ITHSHDN}$	Shutdown Threshold (at I_{TH}/RUN)	P_{VCC} – PGND = V_{TURNON} + 100mV	●	0.15	0.28	0.45	V
$I_{THSTART}$	Start-Up Current Source at I_{TH}/RUN	V_{ITH}/RUN – PGND = 0V, P_{VCC} – P_{GND} = 8V		0.2	0.3	0.4	µA
V_{FB}	Regulated Feedback Voltage	Referenced to PGND, P_{VCC} – P_{GND} = 8V (Note 12)	●	0.780	0.800	0.812	V
I_{FB}	V_{FB} Input Current	P_{VCC} – P_{GND} = 8V (Note 12)			10	50	nA
g_m	Error Amplifier Transconductance	I_{TH}/RUN Pin Load = ±5µA (Note 12)		200	333	500	µA/V
$\Delta V_{O(LINE)}$	Output Voltage Line Regulation	$V_{TURNOFF}$ < P_{VCC} < V_{CLAMP} (Note 12)			0.05		mV/V
$\Delta V_{O(LOAD)}$	Output Voltage Load Regulation	I_{TH}/RUN Sinking 5µA, P_{VCC} – P_{GND} = 8V (Note 12)			3		mV/µA
		I_{TH}/RUN Sourcing 5µA, P_{VCC} – P_{GND} = 8V (Note 12)			3		mV/µA
I_{POUT_LEAK}	P_{OUT} Leakage	V_{PORTN} = 0V, Power MOSFET Off, P_{OUT} = 57V (Note 13)	●			150	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{LIM_HI}	Input Current Limit, High Level	V_{PORTN} = –48V, P_{OUT} = –43V (Note 14, 15)	●	350		450	mA
I_{LIM_LO}	Input Current Limit, Low Level	V_{PORTN} = –48V, P_{OUT} = –43V (Note 14, 15)	●	90		205	mA
f_{OSC}	Oscillator Frequency	V_{ITH}/RUN – PGND = 1.3V, P_{VCC} – P_{GND} = 8V		270	300	330	kHz
$DC_{ON(MIN)}$	Minimum Switch On Duty Cycle	V_{ITH}/RUN – PGND = 1.3V, V_{FB} – PGND = 0.8V, P_{VCC} – P_{GND} = 8V			8	9.6	%
$DC_{ON(MAX)}$	Maximum Switch On Duty Cycle	V_{ITH}/RUN – PGND = 1.3V, V_{FB} – PGND = 0.8V, P_{VCC} – P_{GND} = 8V		70	80	90	%
t_{RISE}	NGATE Drive Rise Time	C_{LOAD} = 3000pF, P_{VCC} – P_{GND} = 8V			40		ns
t_{FALL}	NGATE Drive Fall Time	C_{LOAD} = 3000pF, P_{VCC} – P_{GND} = 8V			40		ns
V_{IMAX}	Peak Current Sense Voltage	R_{SL} = 0, P_{VCC} – P_{GND} = 8V (Note 16)	●	90	100	115	mV
I_{SLMAX}	Peak Slope Compensation Output Current	P_{VCC} – P_{GND} = 8V (Note 17)			5		A
t_{SFST}	Soft-Start Time	P_{VCC} – P_{GND} = 8V			1.4		ms
$T_{SHUTDOWN}$	Thermal Shutdown Trip Temperature	(Notes 14, 18)			140		°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: P_{VCC} internal clamp circuit self regulates to 9.4V with respect to PGND.

Note 3: The LTC4267-3 operates with a negative supply voltage in the range of – 1.5V to – 57V. To avoid confusion, voltages for the PD interface are always referred to in terms of absolute magnitude. Terms such as "maximum negative voltage" refer to the largest negative voltage and a "rising negative voltage" refers to a voltage that is becoming more negative.

Note 4: The LTC4267-3 is designed to work with two polarity protection diode drops between the PSE and PD. Parameter ranges specified in the Electrical Characteristics section are with respect to this product pins and are designed to meet IEEE 802.3af specifications when these diode drops are included. See the Application Information section.

Note 5: Signature resistance is measured via the two-point $\Delta V/\Delta I$ method as defined by IEEE 802.3af. The PD signature resistance is offset from the 25k to account for diode resistance. With two series diodes, the total PD resistance will be between 23.75k and 26.25k and meet IEEE 802.3af specifications. The minimum probe voltages measured at the LTC4267-3 pins are –1.5V and –2.5V. The maximum probe voltages are –8.5V and –9.5V.

Note 6: The PD interface includes hysteresis in the UVLO voltages to preclude any start-up oscillation. Per IEEE 802.3af requirements, the PD will power up from a voltage source with 20Ω series resistance on the first trial.

Note 7: Dynamic Supply current is higher due to the gate charge being delivered at the switching frequency.

Note 8: I_{VPORTN_CLASS} does not include classification current programmed at the R_{CLASS} pin. Total current in classification mode will be I_{VPORTN_CLASS} + I_{CLASS} (See note 9).

Note 9: I_{CLASS} is the measured current flowing through R_{CLASS}. ΔI_{CLASS} accuracy is with respect to the ideal current defined as I_{CLASS} = 1.237/R_{CLASS}. The current accuracy does not include variations in R_{CLASS} resistance. The total classification current for a PD also includes the IC quiescent current (I_{VPORTN_CLASS}). See the Applications Information section.

Note 10: To disable the 25k signature, tie SIGDISA to V_{PORTP} or hold SIGDISA high with respect to V_{PORTN}. See the Applications Information section.

Note 11: For the DHC package, this parameter is assured by design and wafer level testing.

Note 12: The switching regulator is tested in a feedback loop that servos V_{FB} to the output of the error amplifier while maintaining I_{TH}/RUN at the midpoint of the current limit range.

Note 13: I_{POUT_LEAK} includes current drawn through P_{OUT} by the power good status circuit. This current is compensated for in the 25k signature resistance and does not affect PD operation.

Note 14: The LTC4267-3 PD Interface includes thermal protection. In the event of an overtemperature condition, the PD interface will turn off the switching regulator until the part cools below the overtemperature limit. The LTC4267-3 is also protected against thermal damage from incorrect classification probing by the PSE. If the LTC4267-3 exceeds the overtemperature threshold, the classification load current is disabled.

Note 15: The PD interface includes dual level input current limit. At turn-on, before the P_{OUT} load capacitor is charged, the PD current level is set to a low level. After the load capacitor is charged and the P_{OUT} – V_{PORTN} voltage difference is below the power good threshold, the PD switches to high level current limit. The PD stays in high level current limit until the input voltage drops below the UVLO turn-off threshold.

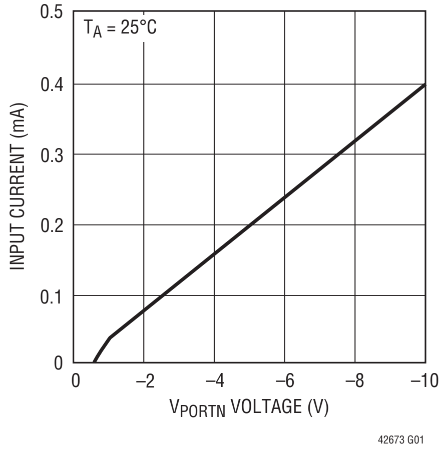
Note 16: Peak current sense voltage is reduced dependent on duty cycle and an optional external resistor in series with the SENSE pin (R_{SL}). For details, refer to the programmable slope compensation feature in the Applications Information section.

Note 17: Guaranteed by design.

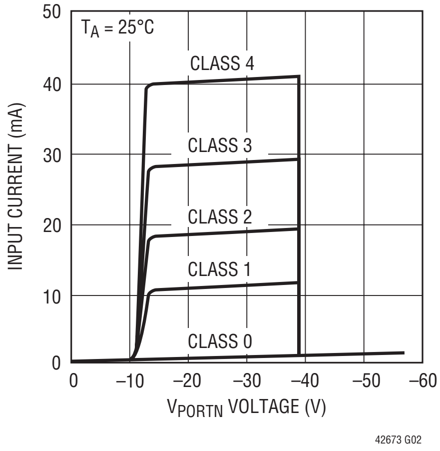
Note 18: The LTC4267-3 features thermal overload protection. Thermal overload protection is intended to protect the device during momentary fault conditions and continuous operation in thermal overload should be avoided as it may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

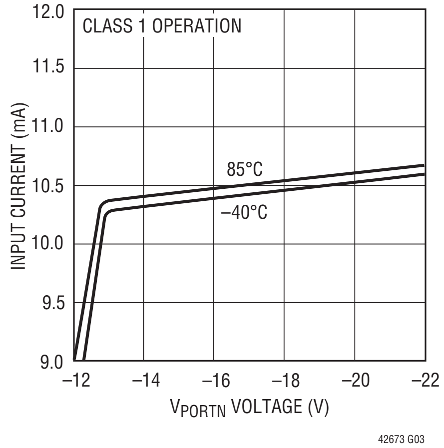
Input Current vs Input Voltage 25k Detection Range



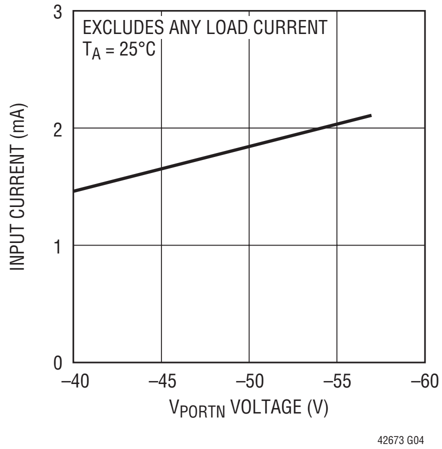
Input Current vs Input Voltage Classification Range



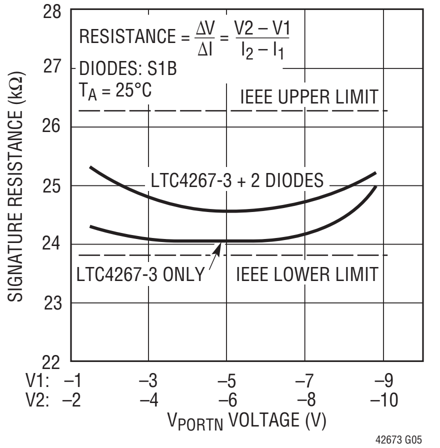
Input Current vs Input Voltage



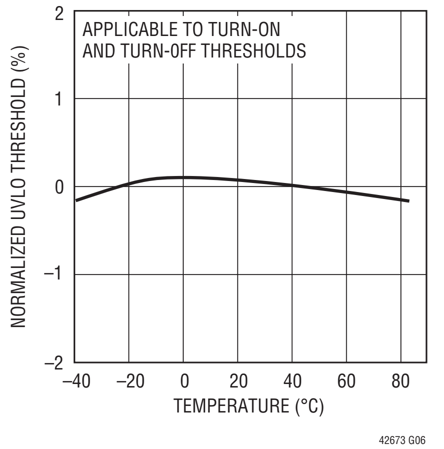
Input Current vs Input Voltage



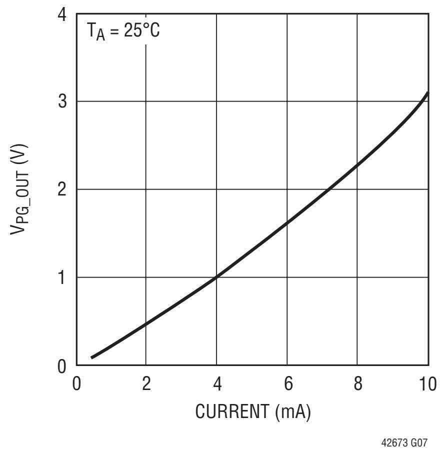
Signature Resistance vs Input Voltage



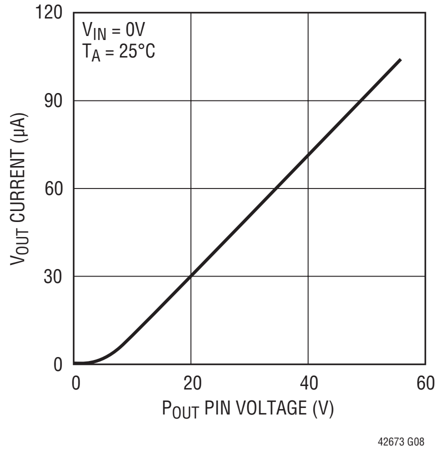
Normalized UVLO Threshold vs Temperature



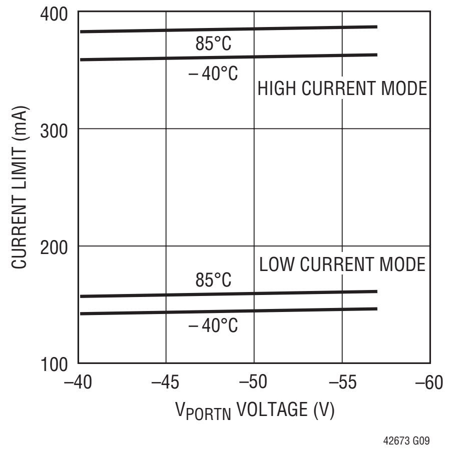
Power Good Output Low Voltage vs Current



P_{OUT} Leakage Current

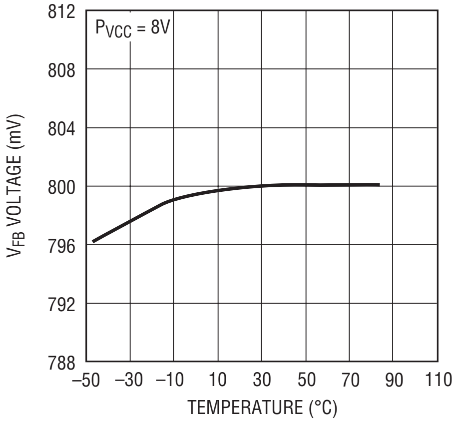


Current Limit vs Input Voltage



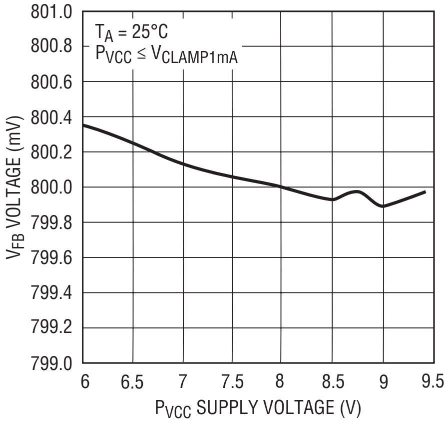
TYPICAL PERFORMANCE CHARACTERISTICS

Reference Voltage vs Temperature



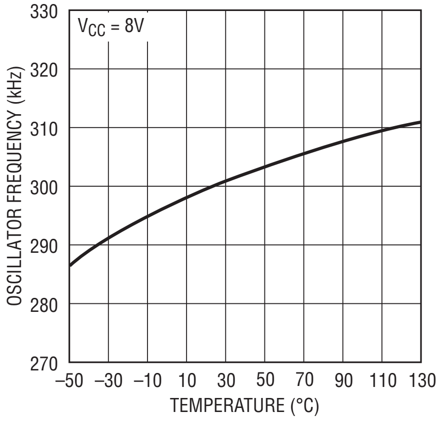
42673 G10

Reference Voltage vs Supply Voltage



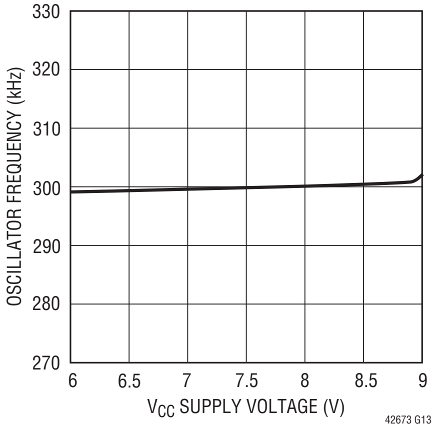
42673 G11

Oscillator Frequency vs Temperature



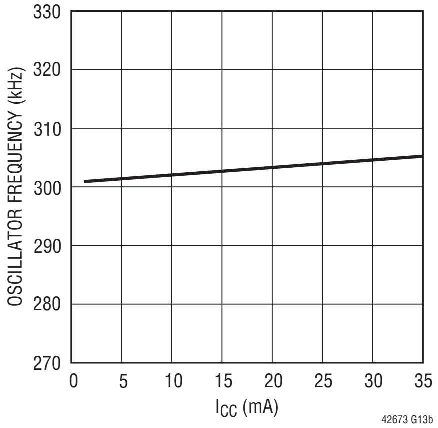
42673 G12

Oscillator Frequency vs Supply Voltage



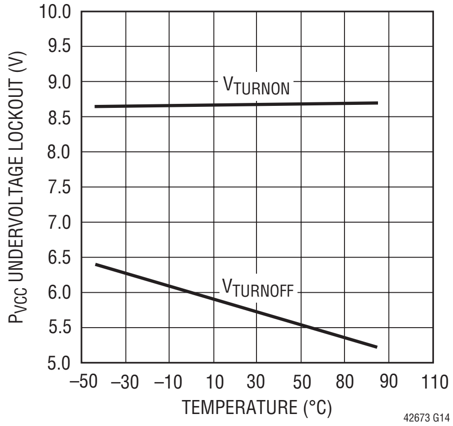
42673 G13

Oscillator Frequency vs V_{CC} Shunt Regulator Current



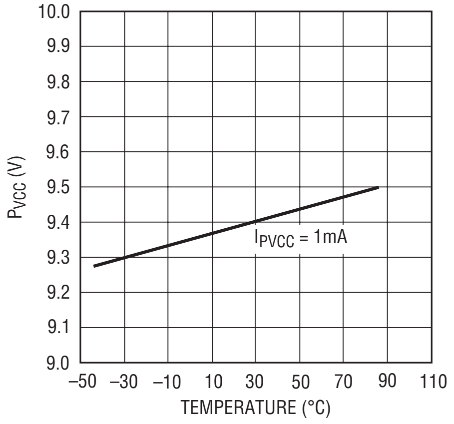
42673 G13b

P_{VCC} Undervoltage Lockout Thresholds vs Temperature



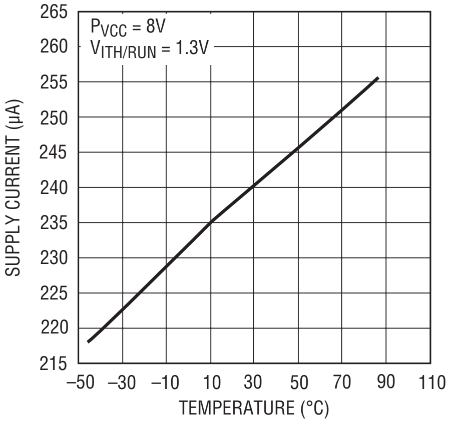
42673 G14

P_{VCC} Shunt Regulator Voltage vs Temperature



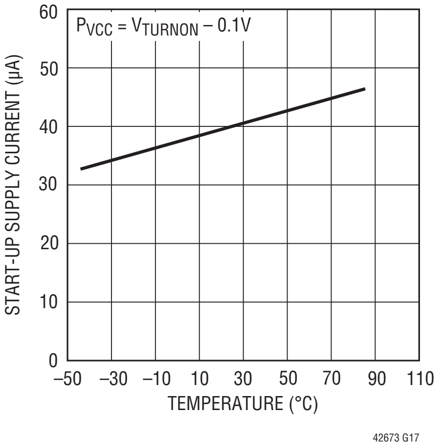
42673 G15

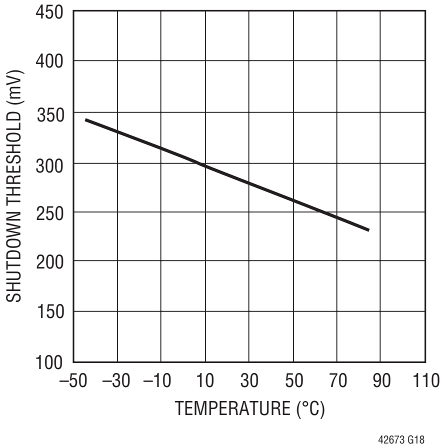
I_{PVCC} Supply Current vs Temperature

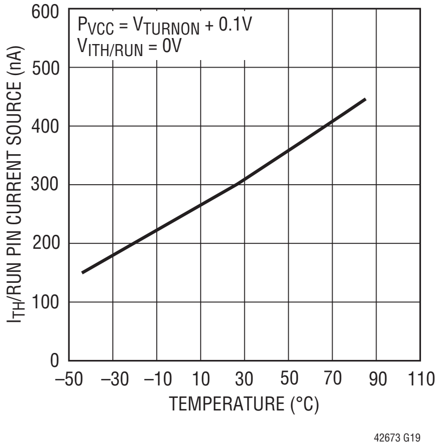


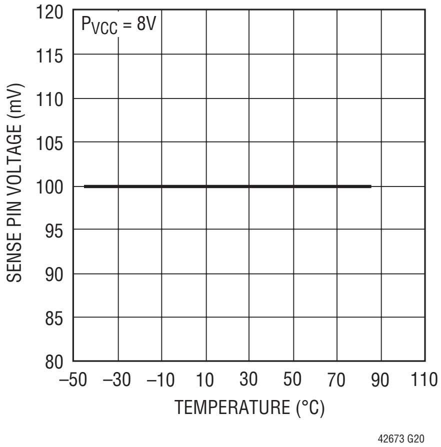
42673 G16

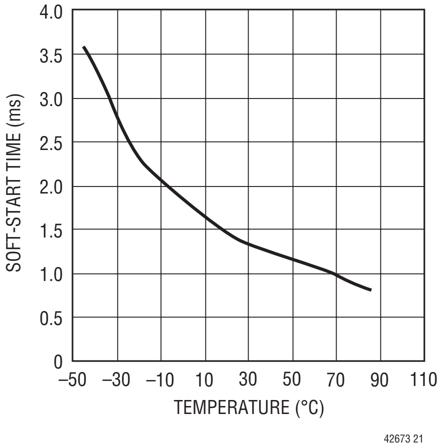
TYPICAL PERFORMANCE CHARACTERISTICS


Start-Up I_{PVCC} Supply Current vs Temperature


I_{TH}/RUN Shutdown Threshold vs Temperature


I_{TH}/RUN Start-Up Current Source vs Temperature


Peak Current Sense Voltage vs Temperature


Soft-Start Time vs Temperature

PIN FUNCTIONS (DFN/SSOP)

PGND (Pins 2, 15/Pins 1, 8, 9, 16): Switching Regulator Negative Supply. This pin is the negative supply rail for the switching regulator controller and must be tied to P_{OUT}.

I_{TH}/RUN (Pin 1/Pin 2): Current Threshold/Run Input. This pin performs two functions. It serves as the switching regulator error amplifier compensation point as well as the run/shutdown control input. Nominal voltage range is 0.7V to 1.9V. Forcing the pin below 0.28V with respect to PGND causes the controller to shut down.

NGATE (Pin 3): Gate Driver Output. This pin drives the regulator's external N-Channel MOSFET and swings from PGND to P_{VCC}.

P_{VCC} (Pin 4): Switching Regulator Positive Supply. This pin is the positive supply rail for the switching regulator and must be closely decoupled to PGND.

R_{CLASS} (Pin 5): Class Select Input. Used to set the current value the PD maintains during classification. Connect a resistor between R_{CLASS} and V_{PORTN} (see Table 2).

NC (Pins 6, 8, 9/Pin 6): No Internal Connection.

V_{PORTN} (Pin 7): Negative Power Input. Tie to the –48V input port through the input diodes.

P_{OUT} (Pin 10): Power Output. Supplies –48V to the switching regulator PGND pin and any additional PD loads through an internal power MOSFET that limits input current. P_{OUT} is high impedance until the voltage reaches the turn-on UVLO threshold. The output is then current limited. See the Application Information section.

$\overline{\text{PWRGD}}$ (Pin 11): Power Good Output, Open-Drain. Indicates that the PD MOSFET is on and the switching regulator can start operation. Low impedance indicates power is good. $\overline{\text{PWRGD}}$ is high impedance during detection, classification and in the event of a thermal overload. $\overline{\text{PWRGD}}$ is referenced to V_{PORTN}.

SIGDISA (Pin 12): Signature Disable Input. SIGDISA allows the PD to present an invalid signature resistance and remain inactive. Connecting SIGDISA to V_{PORTP} lowers the signature resistance to an invalid value and disables all functions of the LTC4267-3. If unused, tie SIGDISA to V_{PORTN}.

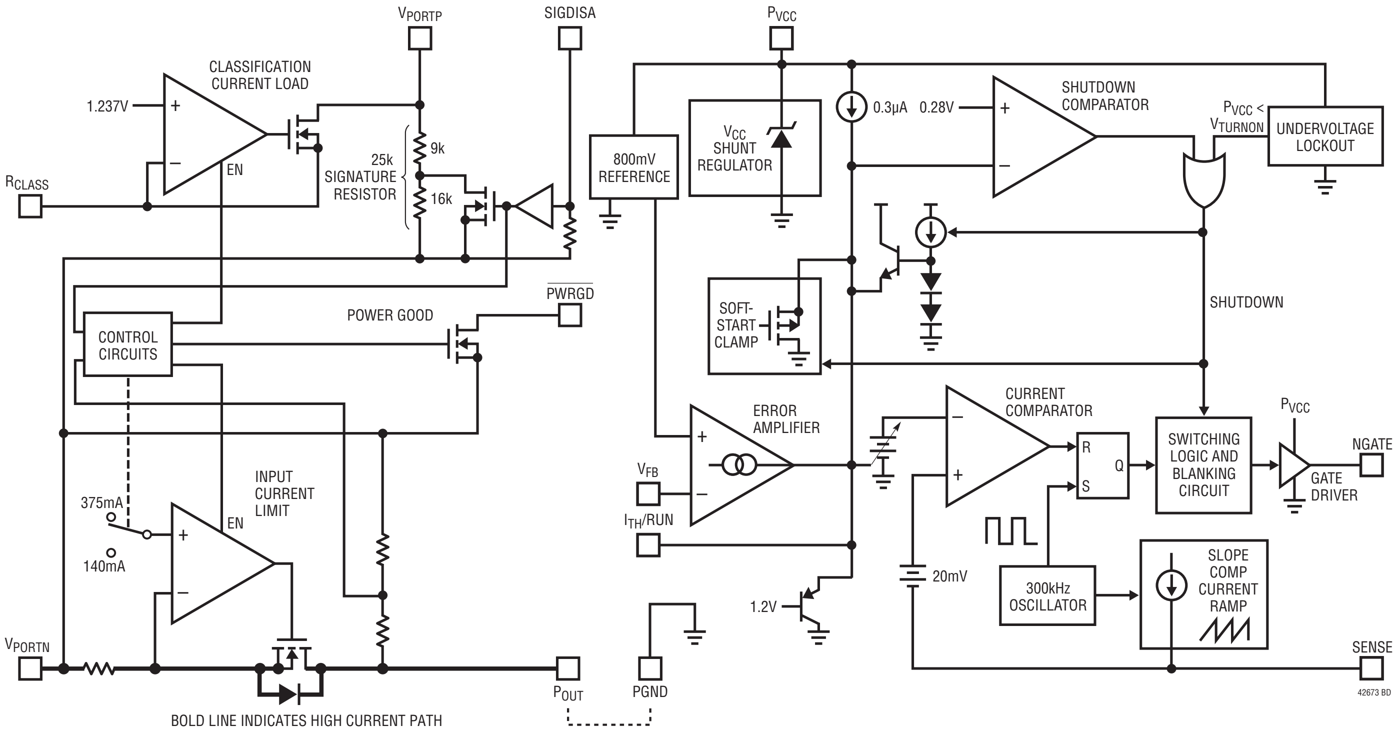
V_{PORTP} (Pin 13): Positive Power Input. Tie to the input port power return through the input diodes.

SENSE (Pin 14): Current Sense. This pin performs two functions. It monitors the regulator switch current by reading the voltage across an external sense resistor. It also injects a current ramp that develops a slope compensation voltage across an optional external programming resistor. See the Applications Information section.

V_{FB} (Pin 16/Pin 15): Feedback Input. Receives the feedback voltage from the external resistor divider across the output.

Exposed Pad (Pin 17, DFN Only): Ground. The Exposed Pad must be soldered to an electrically isolated PCB heat sink.

BLOCK DIAGRAM



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OVERVIEW

The LTC4267-3 is partitioned into two major blocks: a Powered Device (PD) interface controller and a current mode flyback switching regulator. The Powered Device (PD) interface is intended for use as the front end of a PD adhering to the IEEE 802.3af standard, and includes a trimmed 25k signature resistor, classification current source, and an input current limit circuit. With these functions integrated into the LTC4267-3, the signature and power interface for a PD can be built that meets all the requirements of the IEEE 802.3af specification with a minimum of external components.

The switching regulator portion of the LTC4267-3 is a constant-frequency current mode controller that is optimized for Power over Ethernet applications. The regulator is designed to drive a 6V N-channel MOSFET and features soft-start and programmable slope compensation. The integrated error amplifier and precision reference give the PD designer the option of using a nonisolated topology without the need for an external amplifier or reference. The LTC4267-3 has been specifically designed to interface with both IEEE compliant Power Sourcing Equipment (PSE) and legacy PSEs which do not meet the inrush current requirement of the IEEE 802.3af specification. By setting the initial inrush current limit to a low level, a PD using the LTC4267-3 minimizes the current drawn from the PSE during start-up. After powering up, the LTC4267-3 switches to the high level current limit, thereby allowing the PD to consume up to 12.95W if an IEEE 802.3af PSE is present. This low level current limit also allows the LTC4267-3 to charge arbitrarily large load capacitors without exceeding the inrush limits of the IEEE 802.3af specification. This dual level current limit provides the system designer with flexibility to design PDs which are compatible with legacy PSEs while also being able to take advantage of the higher power available in an IEEE 802.3af system.

Using an LTC4267-3 for the power and signature interface functions of a PD provides several advantages. The LTC4267-3 current limit circuit includes an onboard 100V power MOSFET. This low leakage MOSFET is specified to

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avoid corrupting the 25k signature resistor while also saving board space and cost. In addition, the inrush current limit requirement of the IEEE 802.3af standard can cause large transient power dissipation in the PD. The LTC4267-3 is designed to allow multiple turn-on sequences without overheating the miniature 16-lead package. In the event of excessive power cycling, the LTC4267-3 provides thermal overload protection to keep the onboard power MOSFET within its safe operating area.

OPERATION

The LTC4267-3 PD interface has several modes of operation depending on the applied input voltage as shown in Figure 1 and summarized in Table 1. These modes satisfy the requirements defined in the IEEE 802.3af specification. The input voltage is applied to the V_{PORTN} pin and must be negative relative to the V_{PORTP} pin. Voltages in the data sheet for the PD interface portion of the LTC4267-3 are with respect to V_{PORTP} while the voltages for the switching regulator are referenced to PGND. It is assumed that PGND is tied to P_{OUT}. Note the use of different ground symbols throughout the data sheet.

Table 1. LTC4267-3 Operational Mode as a Function of Input Voltage

INPUT VOLTAGE (V_{PORTN} with RESPECT to V_{PORTP})	LTC4267-3 MODE OF OPERATION
0V to –1.4V	Inactive
–1.5V to –9.5V**	25k Signature Resistor Detection
–9.8V to –12.4V	Classification Load Current Ramps up from 0% to 100%
–12.5V to UVLO*	Classification Load Current Active
UVLO* to –57V	Power Applied to Switching Regulator

*V_{PORTN} UVLO includes hysteresis.
Rising input threshold ≅ –36.0V
Falling input threshold ≅ –30.5V

**Measured at LTC4267-3 pin. The LTC4267-3 meets the IEEE 802.3af 10V minimum when operating with the required diode bridges.

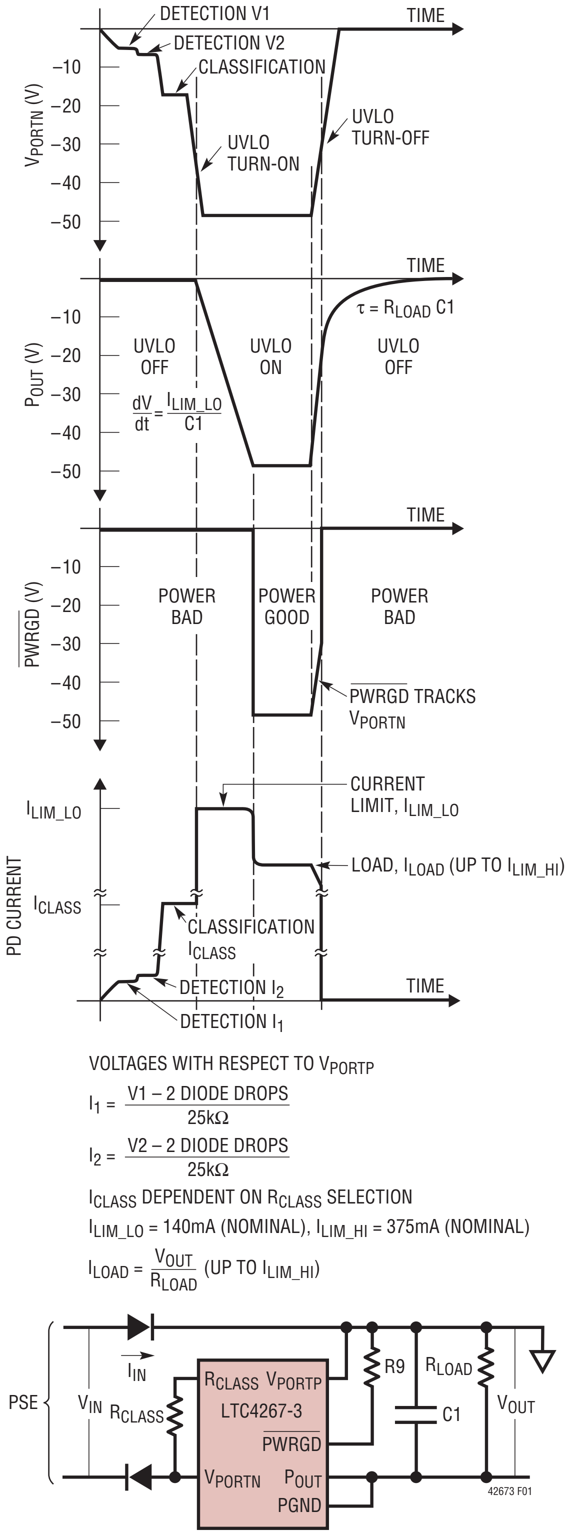

Figure 1. Output Voltage, $\overline{PWRGD}$ and PD Current as a Function of Input Voltage

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Series Diodes

The IEEE 802.3af-defined operating modes for a PD reference the input voltage at the RJ45 connector on the PD. The PD must be able to accept power of either polarity at each of its inputs, so it is common to install diode bridges (Figure 2). The LTC4267-3 takes this into account by compensating for these diode drops in the threshold points for each range of operation. A similar adjustment is made for the UVLO voltages.

Detection

During detection, the PSE will apply a voltage in the range of –2.8V to –10V on the cable and look for a 25k signature resistor. This identifies the device at the end of the cable as a PD. With the terminal voltage in this range, the LTC4267-3 connects an internal 25k resistor between the V_{PORTP} and V_{PORTN} pins. This precision, temperature compensated resistor presents the proper signature to alert the PSE that a PD is present and desires power to be applied. The internal low-leakage UVLO switch prevents the switching regulator circuitry from affecting the detection signature.

The LTC4267-3 is designed to compensate for the voltage and resistance effects of the IEEE required diode bridge. The signature range extends below the IEEE range to accommodate the voltage drop of the two diodes. The IEEE specification requires the PSE to use a $\Delta V/\Delta I$ measurement technique to keep the DC offset of these diodes from affecting the signature resistance measurement. However, the diode resistance appears in series with the signature resistor and must be included in the overall signature resistance of the PD. The LTC4267-3 compensates for the two series diodes in the signature path by offsetting the resistance so that a PD built using the LTC4267-3 will meet the IEEE specification.

In some applications it is necessary to control whether or not the PD is detected. In this case, the 25k signature resistor can be enabled and disabled with the use of the SIGDISA pin (Figure 3). Disabling the signature via the SIGDISA pin will change the signature resistor to 9k (typical) which is an invalid signature per the IEEE 802.3af specification. This invalid signature is present for PD input voltages from –2.8V to –10V. If the input rises above –10V, the signature resistor reverts to 25k to minimize power dissipation in the LTC4267-3. To disable the signature, tie SIGDISA to V_{PORTP}. Alternately, the SIGDISA pin can be driven high with respect to V_{PORTN}. When SIGDISA is high, all functions of the PD interface are disabled.

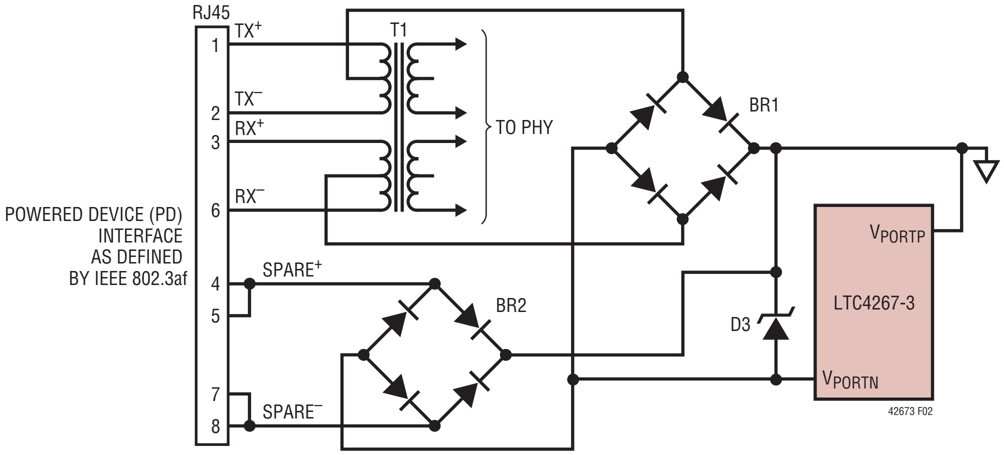


Figure 2. LTC4267-3 PD Front End Using Diode Bridges on Main and Spare Inputs

APPLICATIONS INFORMATION

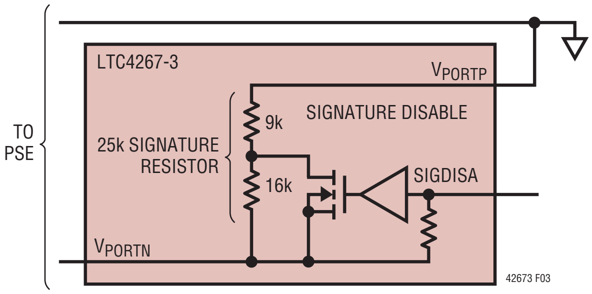


Figure 3. 25k Signature Resistor with Disable

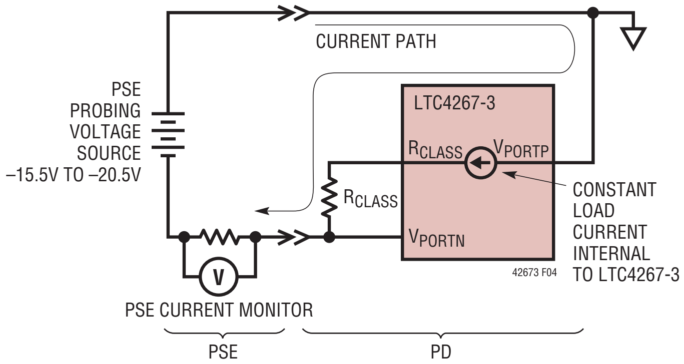


Figure 4. IEEE 802.3af Classification Probing

Classification

Once the PSE has detected a PD, the PSE may optionally classify the PD. Classification provides a method for more efficient allocation of power by allowing the PSE to identify lower power PDs and allocate less power for these devices. The IEEE 802.3af specification defines five classes (Table 2) with varying power levels. The designer selects the appropriate classification based on the power consumption of the PD. For each class, there is an associated load current that the PD asserts onto the line during classification probing. The PSE measures the PD load current to determine the proper classification and PD power requirements.

During classification (Figure 4), the PSE presents a fixed voltage between –15.5V and –20.5V to the PD. With the input voltage in this range, the LTC4267-3 asserts a load current from the V_{PORTP} pin through the R_{CLASS} resistor. The magnitude of the load current is set by the R_{CLASS} resistor. The resistor values associated with each class are shown in Table 2. Note that the switching regulator will not interfere with the classification measurement since the LTC4267-3 has not passed power to the regulator.

Table 2. Summary of IEEE 802.3af Power Classifications and LTC4267-3 R_{CLASS} Resistor Selection

Class	Usage	Maximum Power Levels at Input of PD (W)	Nominal Classification Load Current (mA)	LTC4267-3 R_{CLASS} Resistor (Ω, 1%)
0	Default	0.44 to 12.95	<5	Open
1	Optional	0.44 to 3.84	10.5	124
2	Optional	3.84 to 6.49	18.5	68.1
3	Optional	6.49 to 12.95	28	45.3
4	Reserved	Reserved*	40	30.9

*Class 4 is currently reserved and should not be used.

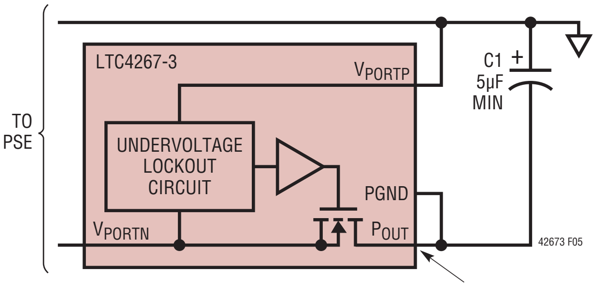
The IEEE 802.3af specification limits the classification time to 75ms because a significant amount of power is dissipated in the PD. The LTC4267-3 is designed to handle the power dissipation for this time period. If the PSE probing exceeds 75ms, the LTC4267-3 may overheat. In this situation, the thermal protection circuit will engage and disable the classification current source in order to protect the part. The LTC4267-3 stays in classification mode until the input voltage rises above the UVLO turn-on voltage.

V_{PORTN} Undervoltage Lockout

The IEEE specification dictates a maximum turn-on voltage of 42V and a minimum turn-off voltage of 30V for the PD. In addition, the PD must maintain large on-off hysteresis to prevent resistive losses in the wiring between the PSE and the PD from causing start-up oscillation. The LTC4267-3 incorporates an undervoltage lockout (UVLO) circuit that monitors the line voltage at V_{PORTN} to determine when to apply power to the integrated switching regulator (Figure 5). Before the power is applied to the switching regulator, the P_{OUT} pin is high impedance and sitting at the ground potential since there is no charge on capacitor C1. When the input voltage rises above the UVLO turn-on threshold, the LTC4267-3 removes the detection and classification loads and turns on the internal power MOSFET. C1 charges up under the LTC4267-3 current limit control and the P_{OUT} pin transitions from 0V to V_{PORTN}. This sequence is shown in Figure 1. The LTC4267-3 includes a hysteretic UVLO circuit on V_{PORTN} that keeps power applied to the load until the input voltage falls below the UVLO turn-off threshold. Once the input voltage drops below –30V, the internal power MOSFET is turned off and

APPLICATIONS INFORMATION

the classification current is reenabled. C1 will discharge through the PD circuitry and the P_{OUT} pin will go to a high impedance state.



INPUT VOLTAGE	LTC4267-3 POWER MOSFET
0V TO UVLO*	OFF
>UVLO*	ON

*UVLO INCLUDES HYSTERESIS
RISING INPUT THRESHOLD ≅ –36V
FALLING INPUT THRESHOLD ≅ –30.5V

Figure 5. LTC4267-3 V_{PORTN} Undervoltage Lockout

Input Current Limit

IEEE 802.3af specifies a maximum inrush current and also specifies a minimum load capacitor between the V_{PORTP} and P_{OUT} pins. To control turn-on surge current in the system, the LTC4267-3 integrates a dual level current limit circuit with an onboard power MOSFET and sense resistor to provide a complete inrush control circuit without additional external components. At turn-on, the LTC4267-3 will limit the input current to the low level, allowing the load capacitor to ramp up to the line voltage in a controlled manner.

The LTC4267-3 has been specifically designed to interface with legacy PSEs which do not meet the inrush current requirement of the IEEE 802.3af specification. At turn-on the LTC4267-3 current limit is set to the lower level. After C1 is charged up and the $P_{OUT} – V_{PORTN}$ voltage difference is below the power good threshold, the LTC4267-3 switches to the high level current limit. The dual level current limit allows legacy PSEs with limited current sourcing capability to power up the PD while also allowing the PD to draw full power from an IEEE 802.3af PSE. The dual level current limit also allows use of arbitrarily large load capacitors. The IEEE 802.3af specification mandates that at turn-on the PD not exceed the inrush current limit for more than 50ms. The LTC4267-3 is not restricted to the 50ms time limit because the load capacitor is charged with a current below the IEEE inrush current limit specification.

As the LTC4267-3 switches from the low to high level current limit, the current will increase momentarily. This current spike is a result of the LTC4267-3 charging the last 1.5V at the high level current limit. When charging a 10µF capacitor, the current spike is typically 100µs wide and 125% of the nominal low level current limit.

The LTC4267-3 stays in the high level current limit mode until the input voltage drops below the UVLO turn-off threshold. This dual level current limit provides the system designer with the flexibility to design PDs which are compatible with legacy PSEs while also being able to take advantage of the higher power allocation available in an IEEE 802.3af system.

During the current limited turn on, a large amount of power is dissipated in the power MOSFET. The LTC4267-3 PD interface is designed to accept this thermal load and is thermally protected to avoid damage to the onboard power MOSFET. Note that in order to adhere to the IEEE 802.3af standard, it is necessary for the PD designer to ensure the PD steady state power consumption falls within the limits shown in Table 2. In addition, the steady state current must be less than I_{LIM_HI}.

Power Good

The LTC4267-3 PD Interface includes a power good circuit (Figure 6) that is used to indicate that load capacitor C1 is fully charged and that the switching regulator can start operation. The power good circuit monitors the voltage across the internal UVLO power MOSFET and $\overline{PWRGD}$ is asserted when the voltage falls below 1.5V. The power good circuit includes hysteresis to allow the LTC4267-3 to operate near the current limit point without inadvertently disabling $\overline{PWRGD}$. The MOSFET voltage must increase to 3V before $\overline{PWRGD}$ is disabled.

If a sudden increase in voltage appears on the input line, this voltage step will be transferred through capacitor C1 and appear across the power MOSFET. The response of the LTC4267-3 will depend on the magnitude of the voltage step, the rise time of the step, the value of capacitor C1 and the switching regulator load. For fast rising inputs,

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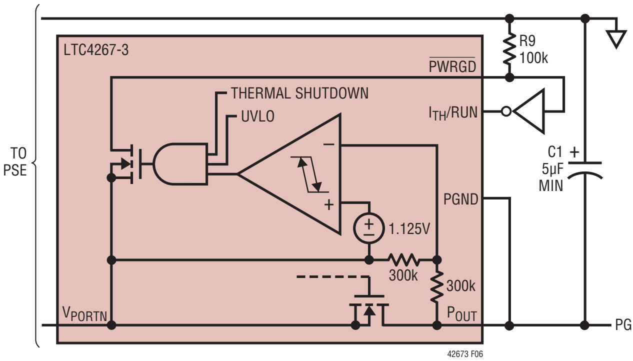
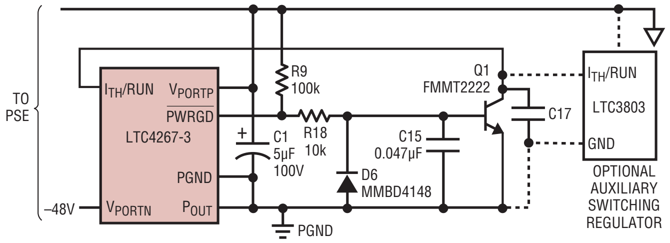


Figure 6. LTC4267-3 Power Good

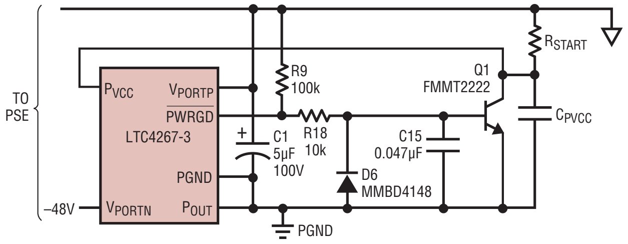
the LTC4267-3 will attempt to quickly charge capacitor C1 using an internal secondary current limit circuit. In this scenario, the PSE current limit should provide the overall limit for the circuit. For slower rising inputs, the 375mA current limit in the LTC4267-3 will set the charge rate of the capacitor C1. In either case, the $\overline{\text{PWRGD}}$ signal may go inactive briefly while the capacitor is charged up to the new line voltage. In the design of a PD, it is necessary to determine if a step in the input voltage will cause the $\overline{\text{PWRGD}}$ signal to go inactive and how to respond to this event. In some designs, it may be desirable to filter the $\overline{\text{PWRGD}}$ signal so that intermittent power bad conditions are ignored. Figure 7 demonstrates a method to insert a lowpass filter on the power good interface.

For PD designs that use a large load capacitor and also consume a lot of power, it is important to delay activation of the switching regulator with the $\overline{\text{PWRGD}}$ signal. If the regulator is not disabled during the current-limited turn-on sequence, the PD circuitry will rob current intended for charging up the load capacitor and create a slow rising input, possibly causing the LTC4267-3 to go into thermal shutdown.

The $\overline{\text{PWRGD}}$ pin connects to an internal open drain, 100V transistor capable of sinking 1mA. Low impedance to V_{PORTN} indicates power is good. $\overline{\text{PWRGD}}$ is high impedance during signature and classification probing and in the event of a thermal overload. During turn-off, $\overline{\text{PWRGD}}$ is deactivated when the input voltage drops below 30V. In addition, $\overline{\text{PWRGD}}$ may go active briefly at turn-on for fast rising input waveforms. $\overline{\text{PWRGD}}$ is referenced to the V_{PORTN} pin and when active, will be near the V_{PORTN} potential. Connect the $\overline{\text{PWRGD}}$ pin to the switching regulator circuitry as shown in Figure 7.



ACTIVE-HIGH ENABLE FOR RUN PIN WITH INTERNAL PULL-UP



ALTERNATE ACTIVE-HIGH ENABLE FOR P_{VCC} PIN
C15 AND C17 OPTIONAL
SEE APPLICATIONS INFORMATION SECTION

42673 F07

Figure 7. Power Good Interface Examples

PD Interface Thermal Protection

The LTC4267-3 PD Interface includes thermal overload protection in order to provide full device functionality in a miniature package while maintaining safe operating temperatures. Several factors create the possibility of significant power dissipation within the LTC4267-3. At turn-on, before the load capacitor has charged up, the instantaneous power dissipated by the LTC4267-3 can be as much as 10W. As the load capacitor charges up, the power dissipation in the LTC4267-3 will decrease until it reaches a steady-state value dependent on the DC load current. The size of the load capacitor determines how fast the power dissipation in the LTC4267-3 will subside. At room temperature, the LTC4267-3 can typically handle load capacitors as large as 800µF without going into thermal shutdown. With large load capacitors, the LTC4267-3 die temperature will increase by as much as 50°C during a single turn-on sequence. If for some reason power were removed from the part and then quickly reapplied so that the LTC4267-3 had to charge up the load capacitor again, the temperature rise would be excessive if safety precautions were not implemented.

The LTC4267-3 PD interface protects itself from thermal damage by monitoring the die temperature. If the die

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temperature exceeds the overtemperature trip point, the current is reduced to zero and very little power is dissipated in the part until it cools below the overtemperature set point. Once the LTC4267-3 has charged up the load capacitor and the PD is powered and running, there will be minor residual heating due to the DC load current of the PD flowing through the internal MOSFET.

During classification, excessive heating of the LTC4267-3 can occur if the PSE violates the 75ms probing time limit. To protect the LTC4267-3, thermal overload circuitry will disable classification current if the die temperature exceeds the overtemperature trip point. When the die cools down below the trip point, classification current is reenabled.

The PD is designed to operate at a high ambient temperature and with the maximum allowable supply (57V). However, there is a limit to the size of the load capacitor that can be charged up before the LTC4267-3 reaches the overtemperature trip point. Hitting the overtemperature trip point intermittently does not harm the LTC4267-3, but it will delay the completion of capacitor charging. Capacitors up to 200µF can be charged without a problem over the full operating temperature range.

Switching Regulator Main Control Loop

Due to space limitations, the basics of current mode DC/DC conversion will not be discussed here. The reader is referred to the detail treatment in Application Note 19 or in texts such as Abraham Pressman's *Switching Power Supply Design.*

In a Power over Ethernet System, the majority of applications involve an isolated power supply design. This means that the output power supply does not have any DC electrical path to the PD interface or the switching regulator primary. The DC isolation is achieved typically through a transformer in the forward path and an optoisolator in the feedback path or a third winding in the transformer. The typical application circuit shown on the front page of the datasheet represents an isolated design using an optoisolator. In applications where a nonisolated topology is desired, the LTC4267-3 features a feedback port and an internal error amplifier that can be enabled for this specific application.

In the typical application circuit (Figure 11), the isolated topology employs an external resistive voltage divider to present a fraction of the output voltage to an external error amplifier. The error amplifier responds by pulling an analog current through the input LED on an optoisolator. The collector of the optoisolator output presents a corresponding current into the I_{TH}/RUN pin via a series diode. This method generates a feedback voltage on the I_{TH}/RUN pin while maintaining isolation.

The voltage on the I_{TH}/RUN pin controls the pulse-width modulator formed by the oscillator, current comparator, and RS latch. Specifically, the voltage at the I_{TH}/RUN pin sets the current comparator's trip threshold. The current comparator monitors the voltage across a sense resistor in series with the source terminal of the external N-Channel MOSFET. The LTC4267-3 turns on the external power MOSFET when the internal free-running 300kHz oscillator sets the RS latch. It turns off the MOSFET when the current comparator resets the latch or when 80% duty cycle is reached, whichever happens first. In this way, the peak current levels through the flyback transformer's primary and secondary are controlled by the I_{TH}/RUN voltage.

In applications where a nonisolated topology is desirable (Figure 11), an external resistive voltage divider can present a fraction of the output voltage directly to the V_{FB} pin of the LTC4267-3. The divider must be designed so when the output is at its desired voltage, the V_{FB} pin voltage will equal the 800mV onboard internal reference. The internal error amplifier responds by driving the I_{TH}/RUN pin. The LTC4267-3 switching regulator performs in a similar manner as described previously.

Regulator Start-Up/Shutdown

The LTC4267-3 switching regulator has two shutdown mechanisms to enable and disable operation: an undervoltage lockout on the P_{VCC} supply pin and a forced shutdown whenever external circuitry drives the I_{TH}/RUN pin low. The LTC4267-3 switcher transitions into and out of shutdown according to the state diagram (Figure 8). It is important not to confuse the undervoltage lockout of the PD interface at V_{PORTN} with that of the switching regulator at P_{VCC}. They are independent functions.

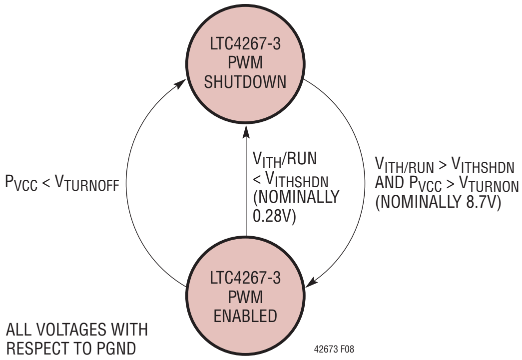

Figure 8. LTC4267-3 Switching Regulator Start-Up/Shutdown State Diagram

The undervoltage lockout mechanism on P_{VCC} prevents the LTC4267-3 switching regulator from trying to drive the external N-Channel MOSFET with insufficient gate-to-source voltage. The voltage at the P_{VCC} pin must exceed V_{TURNON} (nominally 8.7V with respect to PGND) at least momentarily to enable operation. The P_{VCC} voltage must fall to $V_{TURNOFF}$ (nominally 5.7V with respect to PGND) before the undervoltage lockout disables the switching regulator. This wide UVLO hysteresis range supports applications where a bias winding on the flyback transformer is used to increase the efficiency of the LTC4267-3 switching regulator.

The I_{TH}/RUN can be driven below $V_{ITHSHDN}$ (nominally 0.28V with respect to PGND) to force the LTC4267-3 switching regulator into shutdown. An internal 0.3µA current source always tries to pull the I_{TH}/RUN pin towards P_{VCC}. When the I_{TH}/RUN pin voltage is allowed to exceed $V_{ITHSHDN}$ and P_{VCC} exceeds V_{TURNON}, the LTC4267-3 switching regulator begins to operate and an internal clamp immediately pulls the I_{TH}/RUN pin to about 0.7V. In operation, the I_{TH}/RUN pin voltage will vary from roughly 0.7V to 1.9V to represent current comparator thresholds from zero to maximum.

Internal Soft-Start

An internal soft-start feature is enabled whenever the LTC4267-3 switching regulator comes out of shutdown. Specifically, the I_{TH}/RUN voltage is clamped and is prevented from reaching maximum until 1.4ms have passed. This allows the input current of the PD to rise in a smooth and controlled manner on start-up and stay within the current limit requirement of the LTC4267-3 interface.

Adjustable Slope Compensation

The LTC4267-3 switching regulator injects a 5µA peak current ramp out through its SENSE pin which can be used for slope compensation in designs that require it. This current ramp is approximately linear and begins at zero current at 6% duty cycle, reaching peak current at 80% duty cycle. Programming the slope compensation via a series resistor is discussed in the External Interface and Component Selection section.

EXTERNAL INTERFACE AND COMPONENT SELECTION

Input Interface Transformer

Nodes on an Ethernet network commonly interface to the outside world via an isolation transformer (Figure 9). For PoE devices, the isolation transformer must include a center tap on the media (cable) side. Proper termination is required around the transformer to provide correct impedance matching and to avoid radiated and conducted emissions. Transformer vendors such as Bel Fuse, Coilcraft, Pulse and Tyco (Table 3) can provide assistance with selection of an appropriate isolation transformer and proper termination methods. These vendors have transformers specifically designed for use in PD applications.

Table 3. Power over Ethernet Transformer Vendors

VENDOR	CONTACT INFORMATION
Bel Fuse Inc.	206 Van Vorst Street Jersey City, NJ 07302 Tel: 201-432-0463 FAX: 201-432-9542 http://www.belfuse.com
Coilcraft, Inc.	1102 Silver Lake Road Cary, IL 60013 Tel: 847-639-6400 FAX: 847-639-1469 http://www.coilcraft.com
Pulse Engineering	12220 World Trade Drive San Diego, CA 92128 Tel: 858-674-8100 FAX: 858-674-8262 http://www.pulseeng.com
Tyco Electronics	308 Constitution Drive Menlo Park, CA 94025-1164 Tel: 800-227-7040 FAX: 650-361-2508 http://www.circuitprotection.com

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Diode Bridge

IEEE 802.3af allows power wiring in either of two configurations: on the TX/RX wires or via the spare wire pairs in the RJ45 connector. The PD is required to accept power in either polarity on either the main or spare inputs; therefore it is common to install diode bridges on both inputs in order to accommodate the different wiring configurations. Figure 9 demonstrates an implementation of these diode bridges. The IEEE 802.3af specification also mandates that the leakage back through the unused bridge be less than 28µA when the PD is powered with 57V.

The IEEE standard includes an AC impedance requirement in order to implement the AC disconnect function. Capacitor C14 in Figure 9 is used to meet this AC impedance requirement. A 0.1µF capacitor is recommended for this application.

The LTC4267-3 has several different modes of operation based on the voltage present between V_{PORTN} and V_{PORTP} pins. The forward voltage drop of the input diodes in a PD design subtracts from the input voltage and will affect the transition point between modes. When using the LTC4267-3, it is necessary to pay close attention to this forward voltage drop. Selection of oversized diodes will help keep the PD thresholds from exceeding IEEE specifications.

The input diode bridge of a PD can consume over 4% of the available power in some applications. It may be desirable to use Schottky diodes in order to reduce power loss. However, if the standard diode bridge is replaced with a Schottky bridge, the transition points between the modes will be affected. Figure 10 shows a technique for using Schottky diodes while maintaining proper threshold points to meet IEEE 802.3af compliance. D13 is added to compensate for the change in UVLO turn-on voltage caused by the Schottky diodes and consumes little power.

Classification Resistor Selection (R_{CLASS})

The IEEE specification allows classifying PDs into four distinct classes with class 4 being reserved for future use (Table 2). An external resistor connected from R_{CLASS} to V_{PORTN} (Figure 4) sets the value of the load current. The

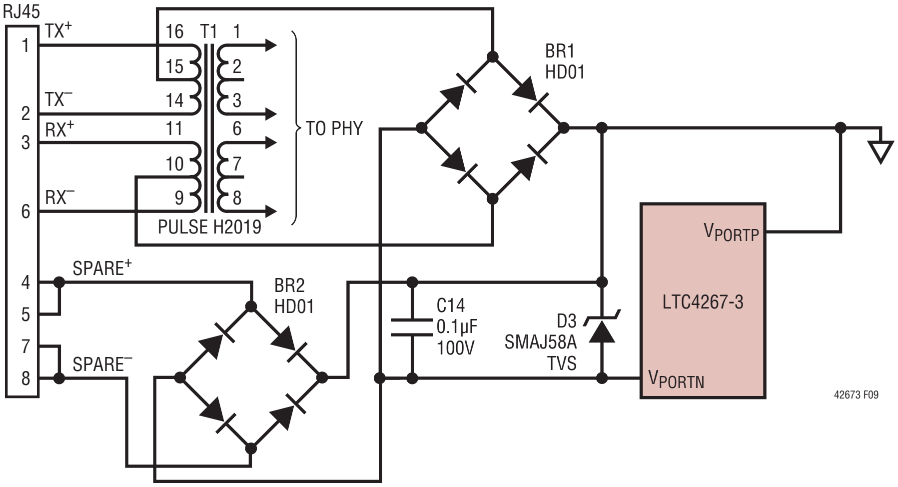
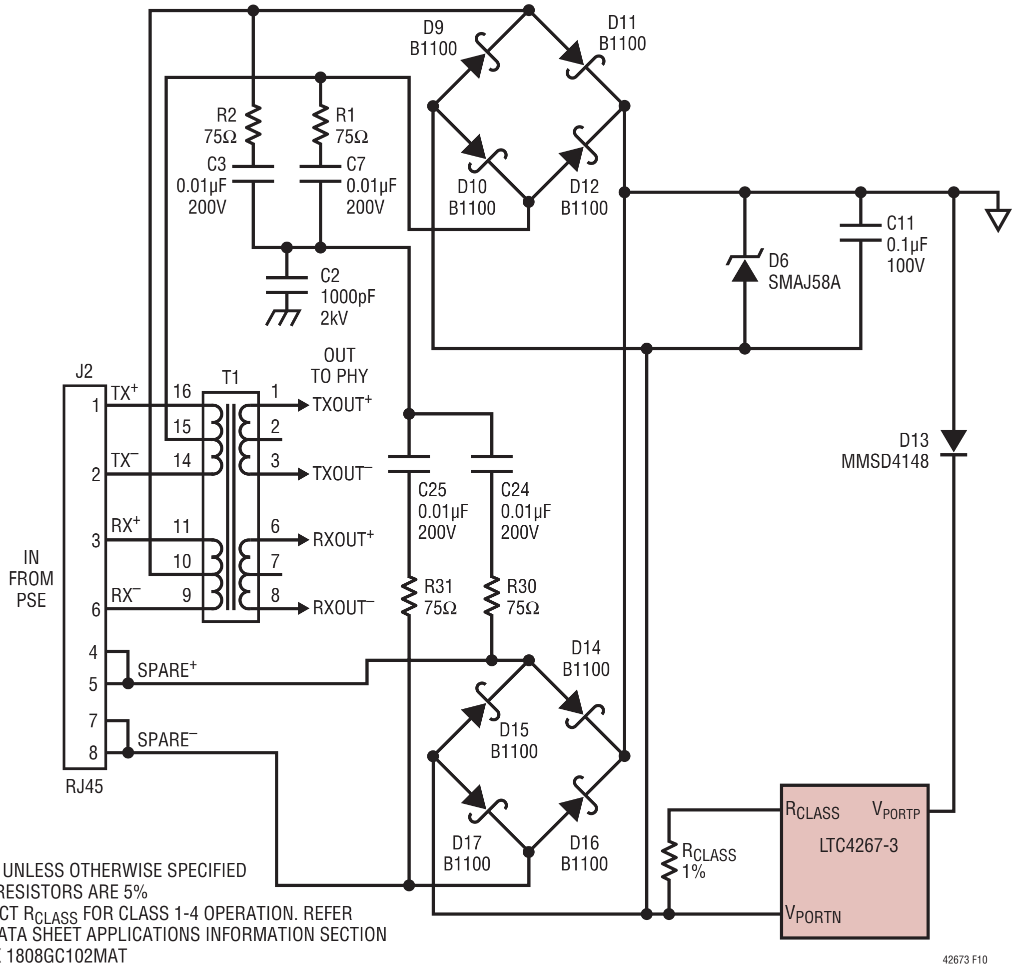


Figure 9. PD Front End with Isolation Transformer, Diode Bridges and Capacitor

APPLICATIONS INFORMATION



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 5%
2. SELECT R_{CLASS} FOR CLASS 1-4 OPERATION. REFER
TO DATA SHEET APPLICATIONS INFORMATION SECTION
C2: AVX 1808GC102MAT
D9 TO D12, D14 TO D17: DIODES INC., B1100
T1: PULSE H2019

Figure 10. PD Front End with Isolation Transformer, 2nd Schottky Diode Bridge

designer should determine which power category the PD falls into and then select the appropriate value of R_{CLASS} from Table 2. If a unique load current is required, the value of R_{CLASS} can be calculated as:

$$R_{CLASS} = 1.237V/(I_{DESIRED} - I_{IN\_CLASS})$$

where I_{IN_CLASS} is the LTC4267-3 IC supply current during classification and is given in the electrical specifications. The R_{CLASS} resistor must be 1% or better to avoid degrading the overall accuracy of the classification circuit. Resistor power dissipation will be 50mW maximum and is transient so heating is typically not a concern. In order to maintain loop stability, the layout should minimize capacitance at the R_{CLASS} node. The classification circuit can be disabled by floating the R_{CLASS} pin. The R_{CLASS} pin should not be shorted to V_{PORTN} as this would force the LTC4267-3 classification circuit to attempt to source very large currents and quickly go into thermal shutdown.

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Power Good Interface

The $\overline{\text{PWRGD}}$ signal is controlled by a high voltage, open-drain transistor. The designer has the option of using this signal to enable the onboard switching regulator through the I_{TH}/RUN or the P_{VCC} pins. Examples of active-high interface circuits for controlling the switching regulator are shown in Figure 7.

In some applications, it is desirable to ignore intermittent power bad conditions. This can be accomplished by including capacitor C15 in Figure 7 to form a lowpass filter. With the components shown, power bad conditions less than about 200µs will be ignored. Conversely, in other applications it may be desirable to delay assertion of $\overline{\text{PWRGD}}$ to the switching regulator using C_{PVCC} or C17 as shown in Figure 7.

It is recommended that the designer use the power good signal to enable the switching regulator. Using $\overline{\text{PWRGD}}$ ensures the capacitor C1 has reached within 1.5V of the final value and is ready to accept a load. The LTC4267-3 is designed with wide power good hysteresis to handle sudden fluctuations in the load voltage and current without prematurely shutting off the switching regulator. Please refer to the Power-Up Sequencing of the Application Information section.

Signature Disable Interface

To disable the 25k signature resistor, connect SIGDISA pin to the V_{PORTP} pin. Alternately, SIGDISA pin can be driven high with respect to V_{PORTN}. An example of a signature disable interface is shown in Figure 16, option 2. Note that the SIGDISA input resistance is relatively large and the threshold voltage is fairly low. Because of high voltages present on the printed circuit board, leakage currents from the V_{PORTP} pin could inadvertently pull SIGDISA high. To ensure trouble-free operation, use high voltage layout techniques in the vicinity of SIGDISA. If unused, connect SIGDISA to V_{PORTN}.

Load Capacitor

The IEEE 802.3af specification requires that the PD maintain a minimum load capacitance of 5µF (provided by C1 in Figure 11). It is permissible to have a much larger load capacitor and the LTC4267-3 can charge very large load capacitors before thermal issues become a problem. The load capacitor must be large enough to provide sufficient energy for proper operation of the switching regulator. However, the capacitor must not be too large or the PD design may violate IEEE 802.3af requirements.

If the load capacitor is too large, there can be a problem with inadvertent power shutdown by the PSE. Consider the following scenario. If the PSE is running at –57V (maximum allowed) and the PD has detected and powered up, the load capacitor will be charged to nearly –57V. If for some reason the PSE voltage is suddenly reduced to –44V (minimum allowed), the input bridge will reverse bias and the PD power will be supplied by the load capacitor. Depending on the size of the load capacitor and the DC load of the PD, the PD will not draw any power for a period of time. If this period of time exceeds the IEEE 802.3af 300ms disconnect delay, the PSE will remove power from the PD. For this reason, it is necessary to ensure that inadvertent shutdown cannot occur.

Very small output capacitors (≤10µF) will charge very quickly in current limit. The rapidly changing voltage at the output may reduce the current limit temporarily, causing the capacitor to charge at a somewhat reduced rate. Conversely, charging a very large capacitor may cause the current limit to increase slightly. In either case, once the output voltage reaches its final value, the input current limit will be restored to its nominal value.

The load capacitor can store significant energy when fully charged. The design of a PD must ensure that this energy is not inadvertently dissipated in the LTC4267-3. The polarity-protection diode(s) prevent an accidental short

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on the cable from causing damage. However, if the V_{PORTN} pin is shorted to V_{PORTP} inside the PD while the capacitor is charged, current will flow through the parasitic body diode of the internal MOSFET and may cause permanent damage to the LTC4267-3.

Maintain Power Signature

In an IEEE 802.3af system, the PSE uses the Maintain Power Signature (MPS) to determine if a PD continues to require power. The MPS requires the PD to periodically draw at least 10mA and also have an AC impedance less than 26.25k in parallel with 0.05µF. If either the DC current is less than 10mA or the AC impedance is above 26.25k, the PSE may disconnect power. The DC current must be less than 5mA and the AC impedance must be above 2M to guarantee power will be removed.

Selecting Feedback Resistor Values

The regulated output voltage of the switching regulator is determined by the resistor divider across V_{OUT} (R1 and R2 in Figure 11) and the error amplifier reference voltage V_{REF}. The ratio of R2 to R1 needed to produce the desired voltage can be calculated as:

$$R2 = R1 \bullet (V_{OUT} - V_{REF})/V_{REF}$$

In an isolated power supply application, V_{REF} is determined by the designer's choice of an external error amplifier. Commercially available error amplifiers or programmable shunt regulators may include an internal reference of 1.25V or 2.5V. Since the LTC4267-3 internal reference and error amplifier are not used in an isolated design, tie the V_{FB} pin to PGND.

In a nonisolated power supply application, the LTC4267-3 onboard internal reference and error amplifier can be used. The resistor divider output can be tied directly to the V_{FB} pin. The internal reference of the LTC4267-3 is 0.8V nominal.

Choose resistance values for R1 and R2 to be as large as possible to minimize any efficiency loss due to the static current drawn from V_{OUT}, but just small enough so that when V_{OUT} is in regulation, the error caused by the nonzero input current from the output of the resistor divider to the error amplifier pin is less than 1%.

Error Amplifier and Optoisolator Considerations

In an isolated topology, the selection of the external error amplifier depends on the output voltage of the switching regulator. Typical error amplifiers include a voltage reference of either 1.25V or 2.5V. The output of the amplifier and the amplifier upper supply rail are often tied together internally. The supply rail is usually specified with a wide upper voltage range, but it is not allowed to fall below the reference voltage. This can be a problem in an isolated switcher design if the amplifier supply voltage is not properly managed. When the switcher load current decreases and the output voltage rises, the error amplifier responds by pulling more current through the LED. The LED voltage can be as large as 1.5V, and along with R_{LIM}, reduces the supply voltage to the error amplifier. If the error amp does not have enough headroom, the voltage drop across the LED and R_{LIM} may shut the amplifier off momentarily, causing a lock-up condition in the main loop. The switcher will undershoot and not recover until the error amplifier releases its sink current. Care must be taken to select the reference voltage and R_{LIM} value so that the error amplifier always has enough headroom. An alternate solution that avoids these problems is to utilize the LT1431 or LT4430 where the output of the error amplifier and amplifier supply rail are brought out to separate pins.

The PD designer must also select an optoisolator such that its bandwidth is sufficiently wider than the bandwidth of the main control loop. If this step is overlooked, the main control loop may be difficult to stabilize. The output

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collector resistor of the optoisolator can be selected for an increase in bandwidth at the cost of a reduction in gain of this stage.

Output Transformer Design Considerations

Since the external feedback resistor divider sets the output voltage, the PD designer has relative freedom in selecting the transformer turns ratio. The PD designer can use simple ratios of small integers (i.e. 1:1, 2:1, 3:2) which yields more freedom in setting the total turns and mutual inductance and may allow the use of an off the shelf transformer.

Transformer leakage inductance on either the primary or secondary causes a voltage spike to occur after the output switch (Q1 in Figure 11) turns off. The input supply voltage plus the secondary-to-primary referred voltage of the flyback pulse (including leakage spike) must not exceed the allowed external MOSFET breakdown rating. This spike is increasingly prominent at higher load currents, where more stored energy must be dissipated. In some cases, a "snubber" circuit will be required to avoid overvoltage breakdown at the MOSFET's drain node. Application Note 19 is a good reference for snubber design.

Current Sense Resistor Consideration

The external current sense resistor (R_{SENSE} in Figure 11) allows the designer to optimize the current limit behavior for a particular application. As the current sense resistor is varied from several ohms down to tens of milliohms, peak swing current goes from a fraction of an ampere to several amperes. Care must be taken to ensure proper circuit operation, especially for small current sense resistor values.

Choose R_{SENSE} such that the switching current exercises the entire range of the I_{TH}/RUN voltage. The nominal voltage range is 0.7V to 1.9V and R_{SENSE} can be determined by experiment. The main loop can be temporarily stabilized by connecting a large capacitor on the power supply. Apply the maximum load current allowable at the power supply output based on the class of the PD. Choose R_{SENSE} such that I_{TH}/RUN approaches 1.9V. Finally, exercise the output load current over the entire operating range and ensure that I_{TH}/RUN voltage remains within the 0.7V to 1.9V range. Layout is critical around the R_{SENSE} resistor. For example, a 0.020Ω sense resistor, with one milliohm (0.001Ω) of parasitic resistance will cause a 5% reduction in peak switch current. The resistance of printed circuit copper traces cannot necessarily be ignored and good layout techniques are mandatory.

Programmable Slope Compensation

The LTC4267-3 switching regulator injects a ramping current through its SENSE pin into an external slope compensation resistor (R_{SL} in Figure 11). This current ramp starts at zero after the NGATE pin has been high for the LTC4267-3's minimum duty cycle of 6%. The current rises linearly towards a peak of 5µA at the maximum duty cycle of 80%, shutting off once the NGATE pin goes low. A series resistor (R_{SL}) connecting the SENSE pin to the current sense resistor (R_{SENSE}) develops a ramping voltage drop. From the perspective of the LTC4267-3 SENSE pin, this ramping voltage adds to the voltage across the sense resistor, effectively reducing the current comparator threshold in proportion to duty cycle. This stabilizes the control loop against subharmonic oscillation. The amount of reduction in the current comparator threshold (ΔV_{SENSE}) can be calculated using the following equation:

$$\Delta V_{SENSE} = 5\mu A \bullet R_{SL} \bullet [(\text{Duty Cycle} - 6\%)/74\%]$$

Note: The LTC4267-3 enforces 6% < Duty Cycle < 80%.

Designs not needing slope compensation may replace R_{SL} with a short-circuit.

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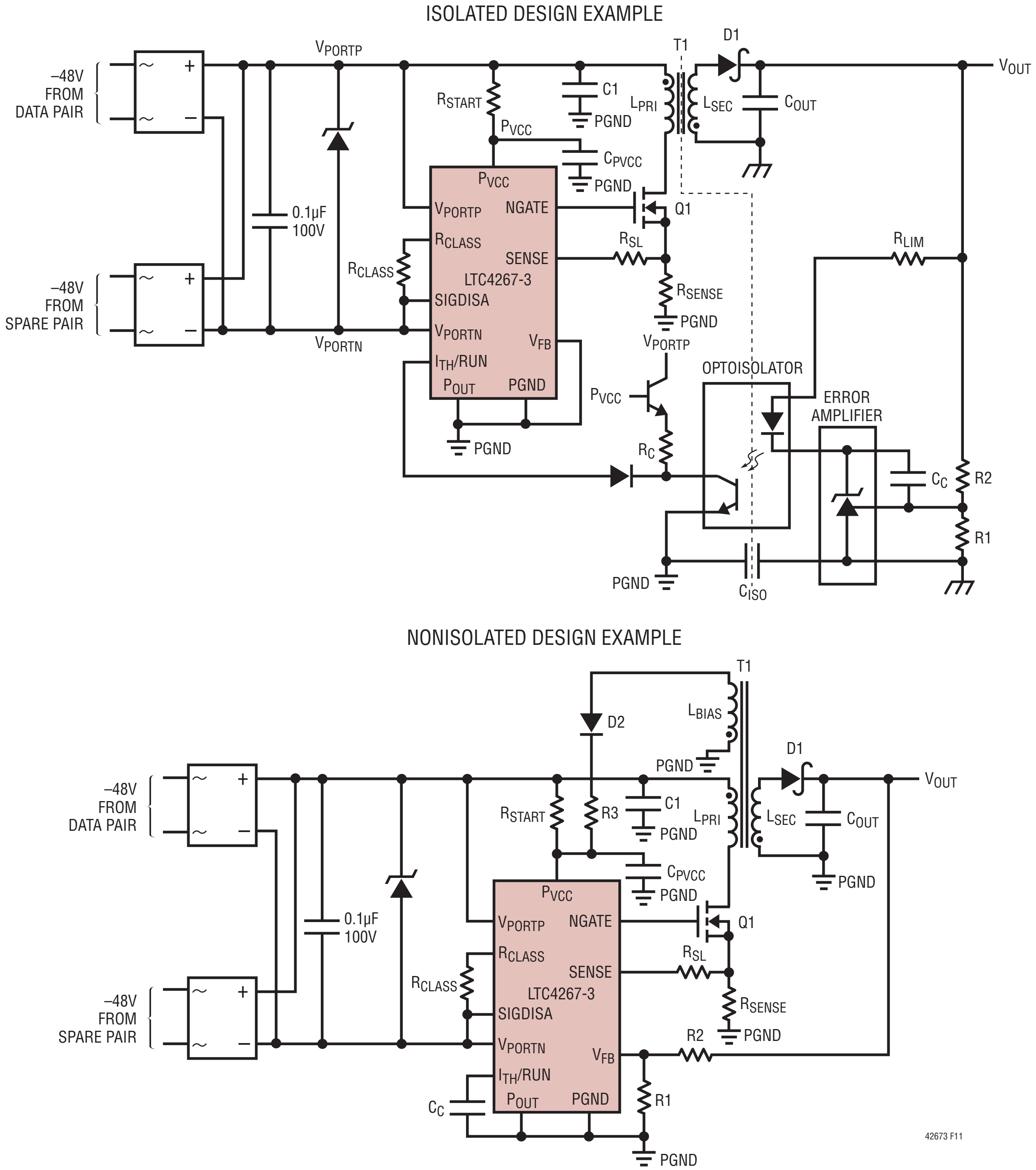

Figure 11. Typical LTC4267-3 Application Circuits

APPLICATIONS INFORMATION

Applications Employing a Third Transformer Winding

A standard operating topology may employ a third winding on the transformer's primary side that provides power to the LTC4267-3 switching regulator via its P_{VCC} pin (Figure 11). However, this arrangement is not inherently self-starting. Start-up is usually implemented by the use of an external "trickle-charge" resistor (R_{START}) in conjunction with the internal wide hysteresis undervoltage lockout circuit that monitors the P_{VCC} pin voltage.

R_{START} is connected to V_{PORTP} and supplies a current, typically 100µA, to charge C_{PVCC}. After some time, the voltage on C_{PVCC} reaches the P_{VCC} turn-on threshold. The LTC4267-3 switching regulator then turns on abruptly and draws its normal supply current. The NGATE pin begins switching and the external MOSFET (Q1) begins to deliver power. The voltage on C_{PVCC} begins to decline as the switching regulator draws its normal supply current, which exceeds the delivery from R_{START}. After some time, typically tens of milliseconds, the output voltage approaches the desired value. By this time, the third transformer winding is providing virtually all the supply current required by the LTC4267-3 switching regulator.

One potential design pitfall is under-sizing the value of capacitor C_{PVCC}. In this case, the normal supply current drawn through P_{VCC} will discharge C_{PVCC} rapidly before the third winding drive becomes effective. Depending on the particular situation, this may result in either several off-on cycles before proper operation is reached or permanent relaxation oscillation at the P_{VCC} node.

Resistor R_{START} should be selected to yield a worst-case minimum charging current greater that the maximum rated LTC4267-3 start-up current to ensure there is enough current to charge C_{PVCC} to the P_{VCC} turn-on threshold. R_{START} should also be selected large enough to yield a worst-case maximum charging current less than the minimum-rated P_{VCC} supply current, so that in operation, most of the P_{VCC} current is delivered through the third winding. This results in the highest possible efficiency.

Capacitor C_{PVCC} should then be made large enough to avoid the relaxation oscillation behavior described previously. This is difficult to determine theoretically as it depends on the particulars of the secondary circuit and load behavior. Empirical testing is recommended.

The third transformer winding should be designed so that its output voltage, after accounting for the forward diode voltage drop, exceeds the maximum P_{VCC} turn-off threshold. Also, the third winding's nominal output voltage should be at least 0.5V below the minimum rated P_{VCC} clamp voltage to avoid running up against the LTC4267-3 shunt regulator, needlessly wasting power.

P_{VCC} Shunt Regulator

In applications including a third transformer winding, the internal P_{VCC} shunt regulator serves to protect the LTC4267-3 switching regulator from overvoltage transients as the third winding is powering up.

If a third transformer winding is undesirable or unavailable, the shunt regulator allows the LTC4267-3 switching regulator to be powered through a single dropping resistor from V_{PORTP} as shown in Figure 12. This simplicity comes at the expense of reduced efficiency due to static power dissipation in the R_{START} dropping resistor.

The shunt regulator can sink up to 5mA through the P_{VCC} pin to PGND. The values of R_{START} and C_{PVCC} must be selected for the application to withstand the worst-case load conditions and drop on P_{VCC}, ensuring that the P_{VCC} turn-off threshold is not reached. C_{PVCC} should be sized sufficiently to handle the switching current needed to drive NGATE while maintaining minimum switching voltage.

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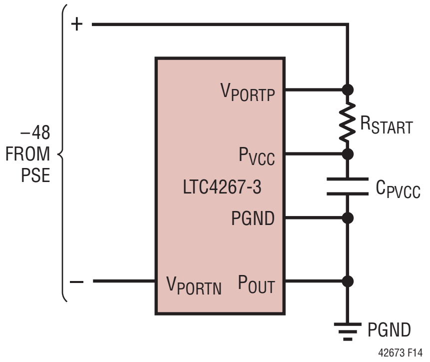

Figure 12. Powering the LTC4267-3 Switching Regulator via the Shunt Regulator

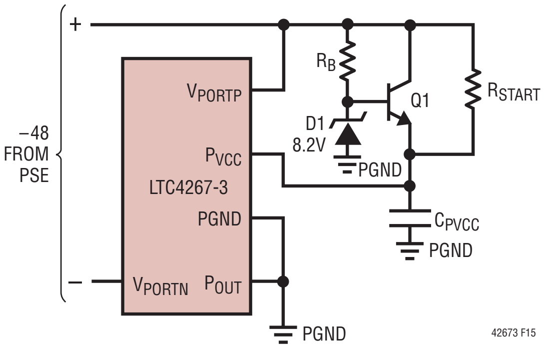

Figure 13. Powering the LTC4267-3 Switching Regulator with an External Preregulator

External Preregulator

The circuit in Figure 13 shows a third way to power the LTC4267-3 switching regulator circuit. An external series preregulator consists of a series pass transistor Q1, zener diode D1, and a bias resistor R_B. The preregulator holds P_{VCC} at 7.6V nominal, well above the maximum rated P_{VCC} turn-off threshold of 6.8V. Resistor R_{START} momentarily charges the P_{VCC} node up to the P_{VCC} turn-on threshold, enabling the switching regulator. The voltage on C_{PVCC} begins to decline as the switching regulator draws its normal supply current, which exceeds the delivery of R_{START}. After some time, the output voltage approaches the desired value. By this time, the pass transistor Q1 catches the declining voltage on the P_{VCC} pin, and provides virtually all the supply current required by the LTC4267-3 switching regulator. C_{PVCC} should be sized sufficiently to handle the switching current needed to drive NGATE while maintaining minimum switching voltage.

The external preregulator has improved efficiency over the simple resistor-shunt regulator method mentioned previously. R_B can be selected so that it provides a small current necessary to maintain the zener diode voltage and the maximum possible base current Q1 will encounter. The actual current needed to power the LTC4267-3 switching regulator goes through Q1 and P_{VCC} sources current on an “as-needed” basis. The static current is then limited only to the current through R_B and D1.

Compensating the Main Loop

In an isolated topology, the compensation point is typically chosen by the components configured around the external error amplifier. Shown in Figure 14, a series RC network is connected from the compare voltage of the error amplifier to the error amplifier output. In PD designs where transient load response is not critical, replace R_Z with a short. The product of R2 and C_C should be sufficiently large to ensure stability. When fast settling transient response is critical, introduce a zero set by R_ZC_C. The PD designer must ensure that the faster settling response of the output voltage does not compromise loop stability.

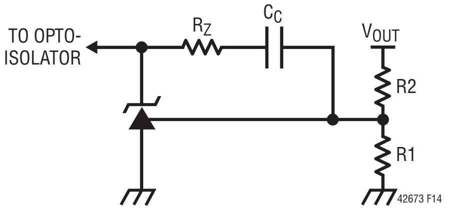

Figure 14. Main Loop Compensation for an Isolated Design

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In a nonisolated design, the LTC4267-3 incorporates an internal error amplifier where the I_{TH}/RUN pin serves as a compensation point. In a similar manner, a series RC network can be connected from I_{TH}/RUN to PGND as shown in Figure 15. C_C and R_Z are chosen for optimum load and line transient response.

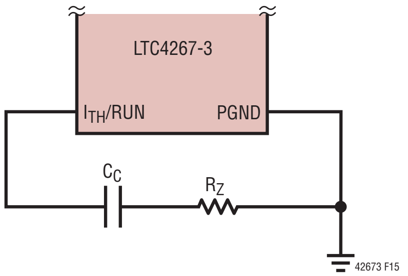

Figure 15. Main Loop Compensation for a Nonisolated Design

Selecting the Switching Transistor

With the N-channel power MOSFET driving the primary of the transformer, the inductance will cause the drain of the MOSFET to traverse twice the voltage across V_{PORTP} and PGND. The LTC4267-3 operates with a maximum supply of – 57V; thus the MOSFET must be rated to handle 114V or more with sufficient design margin. Typical transistors have 150V ratings while some manufacturers have developed 120V rated MOSFETs specifically for Power-over-Ethernet applications.

The NGATE pin of the LTC4267-3 drives the gate of the N-channel MOSFET. NGATE will traverse a rail-to-rail voltage from PGND to P_{VCC}. The designer must ensure the MOSFET provides a low "ON" resistance when switched to P_{VCC} as well as ensure the gate of the MOSFET can handle the P_{VCC} supply voltage.

For high efficiency applications, select an N-channel MOSFET with low total gate charge. The lower total gate charge improves the efficiency of the NGATE drive circuit and minimizes the switching current needed to charge and discharge the gate.

Auxiliary Power Source

In some applications, it may be desirable to power the PD from an auxiliary power source such as a wall transformer. The auxiliary power can be injected into the PD at several locations and various trade-offs exist. Power can be injected at the 3.3V or 5V output of the isolated power supply with the use of a diode ORing circuit. This method accesses the internal circuits of the PD after the isolation barrier and therefore meets the 802.3af isolation safety requirements for the wall transformer jack on the PD. Power can also be injected into the PD interface portion of the LTC4267-3. In this case, it is necessary to ensure the user cannot access the terminals of the wall transformer jack on the PD since this would compromise the 802.3af isolation safety requirements.

Figure 16 demonstrates three methods of diode ORing external power into a PD. Option 1 inserts power before the LTC4267-3 interface controller while options 2 and 3 bypass the LTC4267-3 interface controller section and power the switching regulator directly.

If power is inserted before the LTC4267-3 interface controller, it is necessary for the wall transformer to exceed the LTC4267-3 UVLO turn-on requirement and include a transient voltage suppressor (TVS) to limit the maximum voltage to 57V. This option provides input current limit for the transformer, provides a valid power good signal, and simplifies power priority issues. As long as the wall transformer applies power to the PD before the PSE, it will take priority and the PSE will not power up the PD because the wall power will corrupt the 25k signature. If the PSE is already powering the PD, the wall transformer power will be in parallel with the PSE. In this case, priority will be given to the higher supply voltage. If the wall transformer voltage is higher, the PSE should remove the line voltage since no current will be drawn from the PSE. On the other hand, if the wall transformer voltage is lower, the PSE will continue to supply power to the PD and the wall transformer will not be used. Proper operation should occur in either scenario.

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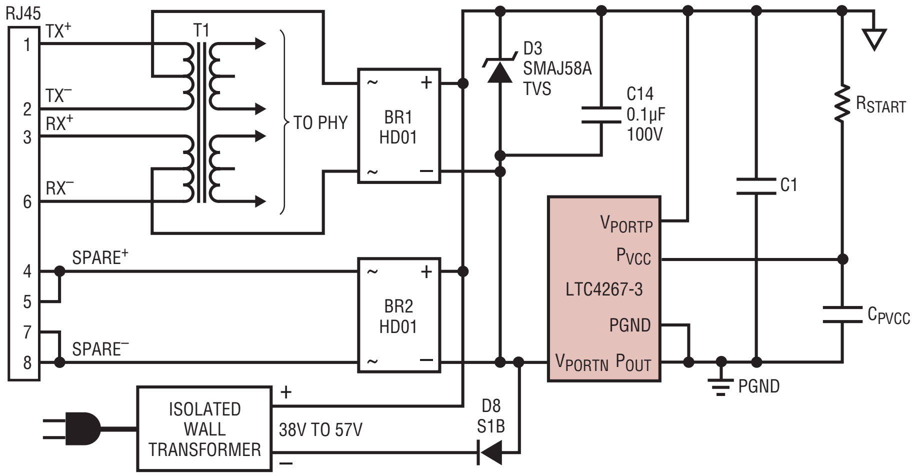
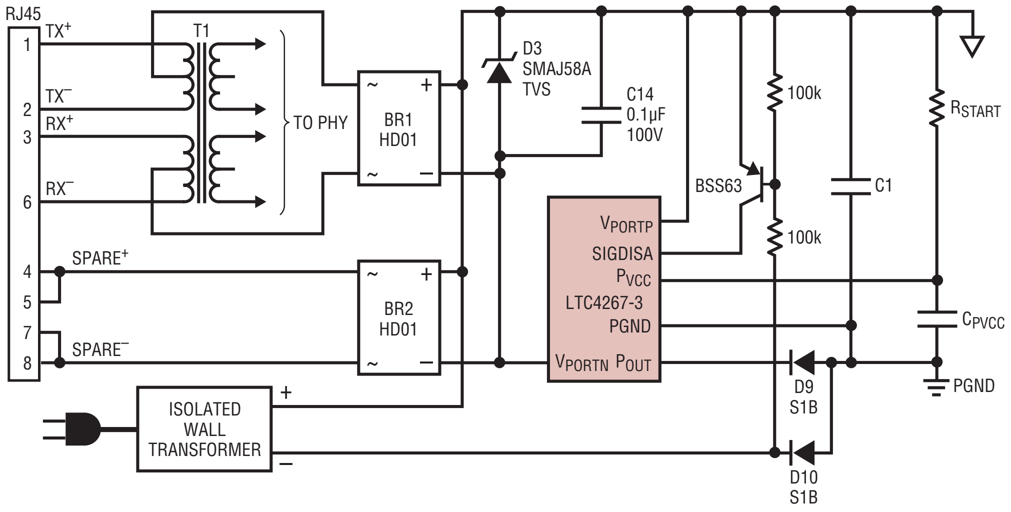
OPTION 1: AUXILIARY POWER INSERTED BEFORE LTC4267-3 PD



OPTION 2: AUXILIARY POWER INSERTED AFTER LTC4267-3 PD WITH SIGNATURE DISABLED



OPTION 3: AUXILIARY POWER APPLIED TO LTC4267-3 PD AND SWITCHING REGULATOR

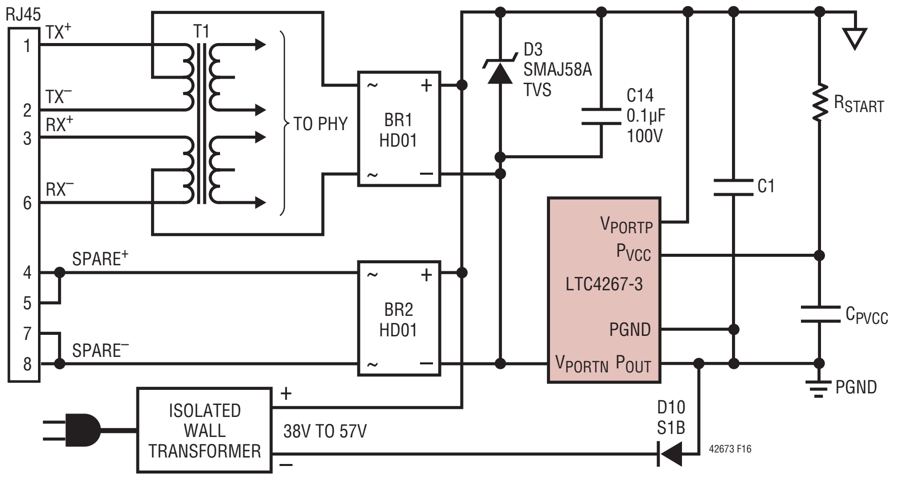


Figure 16. Auxiliary Power Source for PD

APPLICATIONS INFORMATION

If auxiliary power is applied directly to the LTC4267-3 switching regulator (bypassing the LTC4267-3 PD interface), a different set of tradeoffs arise. In the configuration shown in option 2, the wall transformer does not need to exceed the LTC4267-3 turn-on UVLO requirement; however, it is necessary to include diode D9 to prevent the transformer from applying power to the LTC4267-3 interface controller. The transformer voltage requirement will be governed by the needs of the onboard switching regulator. However, power priority issues require more intervention. If the wall transformer voltage is below the PSE voltage, then priority will be given to the PSE power. The LTC4267-3 interface controller will draw power from the PSE while the transformer will sit unused. This configuration is not a problem in a PoE system. On the other hand, if the wall transformer voltage is higher than the PSE voltage, the LTC4267-3 switching regulator will draw power from the transformer. In this situation, it is necessary to address the issue of power cycling that may occur if a PSE is present. The PSE will detect the PD and apply power. If the switcher is being powered by the wall transformer, then the PD will not meet the minimum load requirement and the PSE will subsequently remove power. The PSE will again detect the PD and power cycling will start. With a transformer voltage above the PSE voltage, it is necessary to either disable the signature, as shown in option 2, or install a minimum load on the output of the LTC4267-3 interface to prevent power cycling.

The third option also applies power directly to the LTC4267-3 switching regulator, bypassing the LTC4267-3 interface controller and omitting diode D9. With the diode omitted, the transformer voltage is applied to the LTC4267-3 interface controller in addition to the switching regulator. For this reason, it is necessary to ensure that the transformer maintain the voltage between 38V and 57V to keep the LTC4267-3 interface controller in its normal operating range. The third option has the advantage of automatically disabling the 25k signature resistor when the external voltage exceeds the PSE voltage.

Power-Up Sequencing the LTC4267-3

The LTC4267-3 consists of two functional cells, the PD interface and the switching regulator, and the power up sequencing of these two cells must be carefully considered. The PD designer should ensure that the switching regulator does not begin operation until the interface has completed charging up the load capacitor. This will ensure that the switcher load current does not compete with the load capacitor charging current provided by the PD interface current limit circuit. Overlooking this consideration may result in slow power supply ramp up, power-up oscillation, and possibly thermal shutdown.

The LTC4267-3 includes a power good signal in the PD interface that can be used to indicate to the switching regulator that the load capacitor is fully charged and ready to handle the switcher load. Figure 7 shows two examples of ways the $\overline{\text{PWRGD}}$ signal can be used to control the switching regulator. The first example employs an N-channel MOSFET to drive the I_{TH}/RUN port below the shutdown threshold (typically 0.28V). The second example drives P_{VCC} below the P_{VCC} turn-off threshold. Employing the second example has the added advantage of adding delay to the switching regulator start-up beyond the time the power good signal becomes active. The second example ensures additional timing margin at start-up without the need for added delay components. In applications where it is not desirable to utilize the power good signal, sufficient timing margin can be achieved with R_{START} and C_{PVCC}. R_{START} and C_{PVCC} should be set to a delay of two to three times longer than the duration needed to charge up C1.

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Layout Considerations for the LTC4267-3

The most critical layout considerations for the LTC4267-3 are the placement of the supporting external components associated with the switching regulator. Efficiency, stability, and load transient response can deteriorate without good layout practices around critical components.

For the LTC4267-3 switching regulator, the current loop through C1, T1 primary, Q1, and R_{SENSE} must be given careful layout attention. (Refer to Figure 11.) Because of the high switching current circulating in this loop, these components should be placed in close proximity to each other. In addition, wide copper traces or copper planes should be used between these components. If vias are necessary to complete the connectivity of this loop, placing multiple vias lined perpendicular to the flow of current is essential for minimizing parasitic resistance and reducing current density. Since the switching frequency and the power levels are substantial, shielding and high frequency layout techniques should be employed. A low current, low impedance alternate connection should be employed between the PGND pins of the LTC4267-3 and the PGND side of R_{SENSE}, away from the high current loop. This Kelvin sensing will ensure an accurate representation of the sense voltage is measured by the LTC4267-3.

The placement of the feedback resistors R1 and R2 as well as the compensation capacitor C_C is very important in the accuracy of the output voltage, the stability of the main control loop, and the load transient response. In an isolated design application, R1, R2, and C_C should be placed as close as possible to the error amplifier’s input with minimum trace lengths and minimum capacitance. In a nonisolated application, R1, and R2 should be placed as close as possible to the V_{FB} pin of the LTC4267-3 and C_C should be placed close to the I_{TH}/RUN pin of the LTC4267-3.

In essence, a tight overall layout of the high current loop and careful attention to current density will ensure successful operation of the LTC4267-3 in a PD.

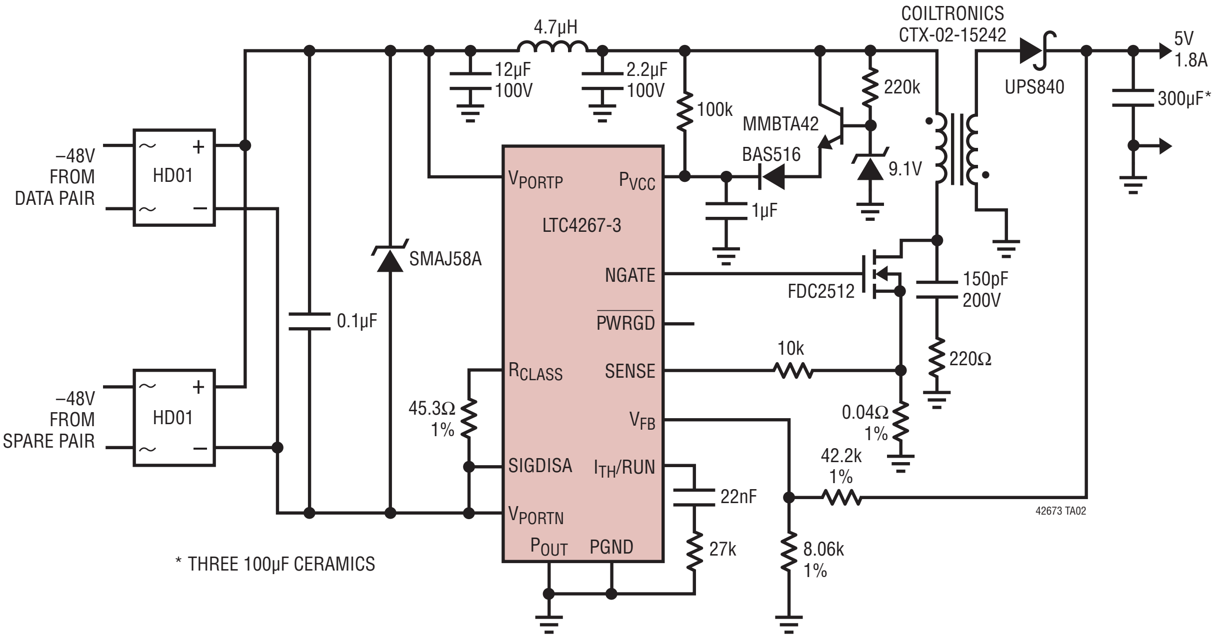
The PD interface section of the LTC4267-3 is relatively immune to layout problems. Excessive parasitic capacitance on the R_{CLASS} pin should be avoided. The SIGDISA pin is adjacent to the V_{PORTP} pin and any coupling, whether resistive or capacitive may inadvertently disable the signature resistance. To ensure consistent behavior, the SIGDISA pin should be electrically connected and not left floating. Voltages in a PD can be as large as –57V, so high voltage layout techniques should be employed.

Electro Static Discharge and Surge Protection

The LTC4267-3 is specified to operate with an absolute maximum voltage of –100V and is designed to tolerate brief overvoltage events. However, the pins that interface to the outside world (primarily V_{PORTN} and V_{PORTP}) can routinely see peak voltages in excess of 10kV. To protect the LTC4267-3, it is highly recommended that a transient voltage suppressor be installed between the diode bridge and the LTC4267-3 (D3 in Figure 2).

TYPICAL APPLICATIONS

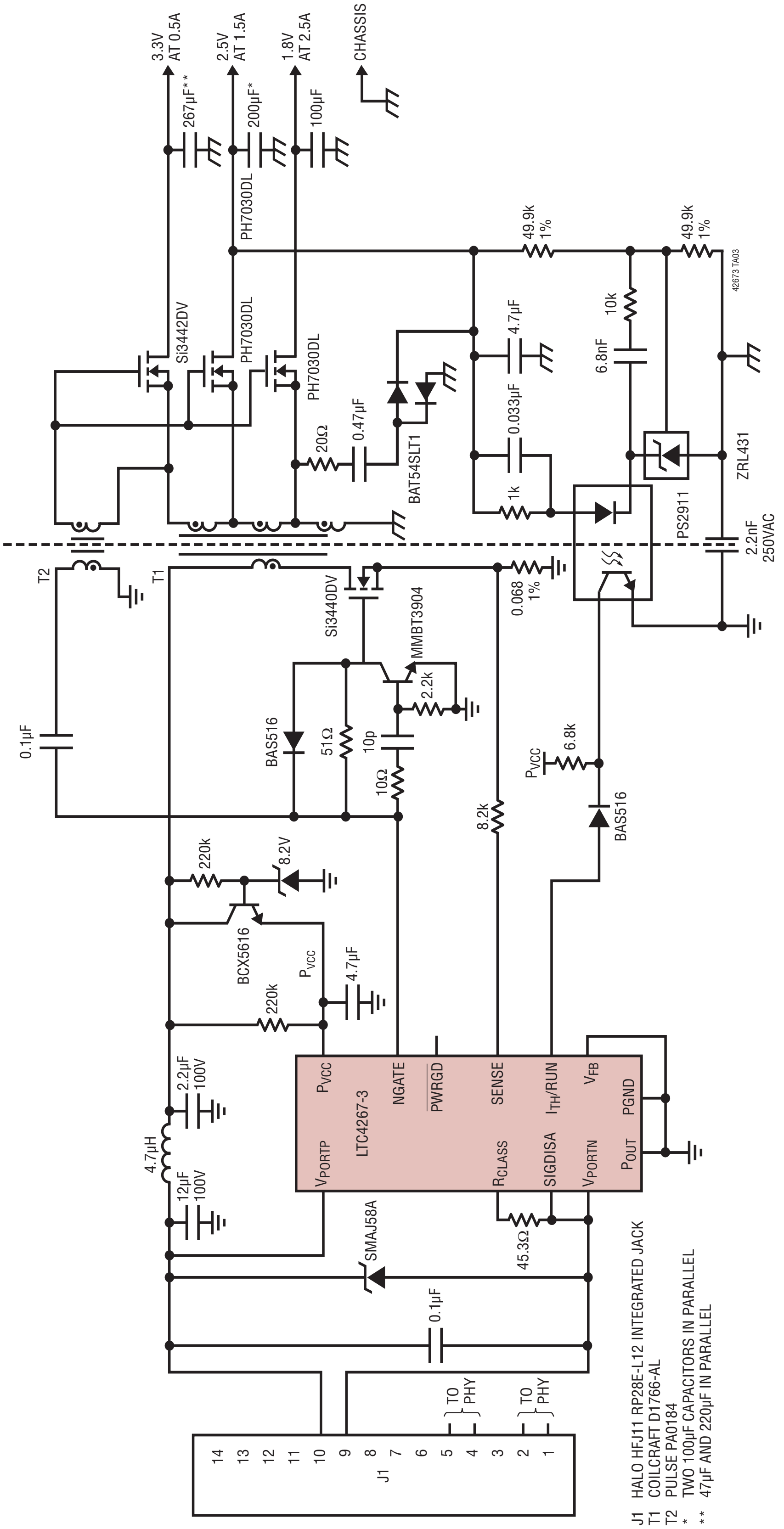
Class 3 PD with 5V Nonisolated Power Supply



* THREE 100μF CERAMICS

TYPICAL APPLICATIONS

Synchronous Class 3 PD with Triple Output Isolated Power Supplies

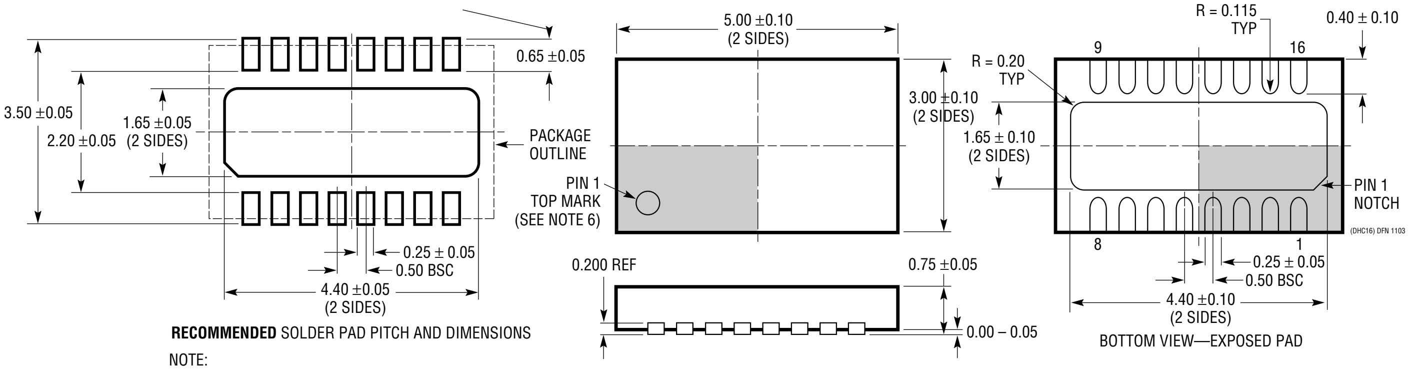


J1 HALO HFJ11 RP28E-L12 INTEGRATED JACK
T1 COILCRAFT D1766-AL
T2 PULSE PA0184
* TWO 100µF CAPACITORS IN PARALLEL
** 47µF AND 220µF IN PARALLEL

PACKAGE DESCRIPTION

DHC Package
16-Lead Plastic DFN (5mm × 3mm)

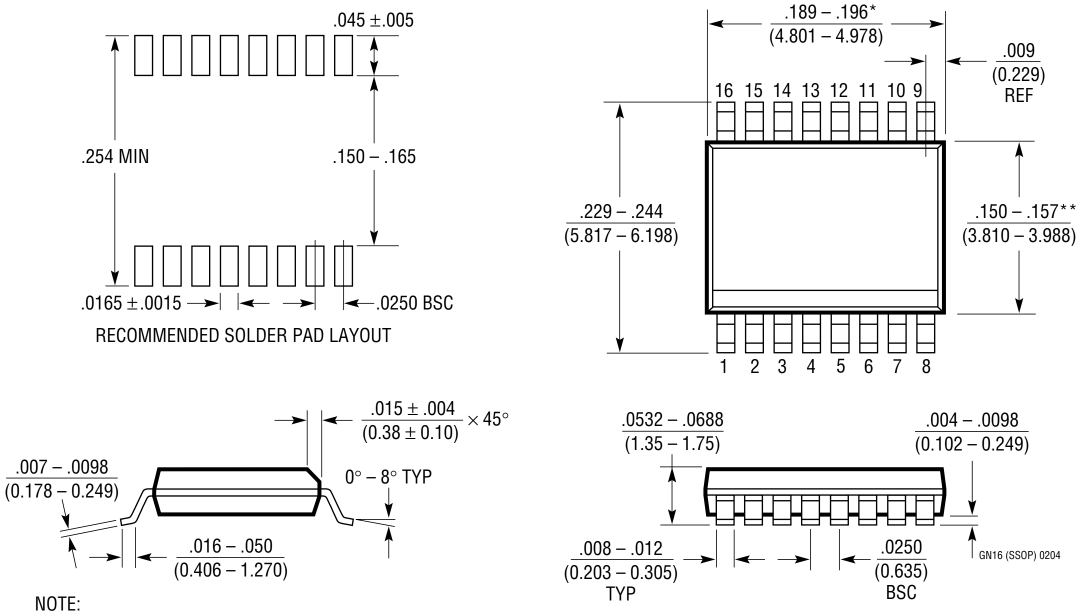
(Reference LTC DWG # 05-08-1706)



NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)

(Reference LTC DWG # 05-08-1641)



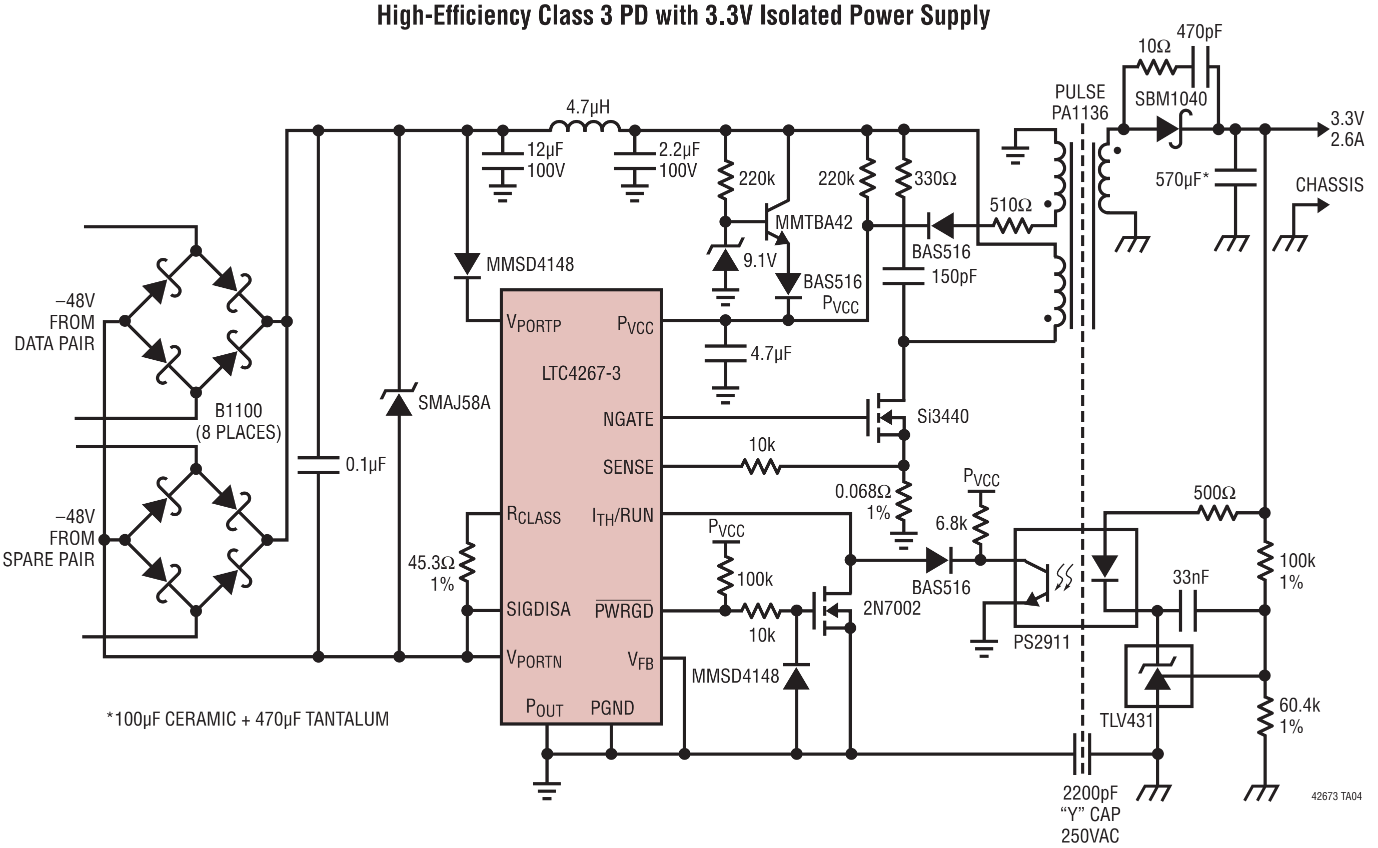
NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

High-Efficiency Class 3 PD with 3.3V Isolated Power Supply



*100µF CERAMIC + 470µF TANTALUM

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3803-3	Current Mode Flyback DC/DC Controller in ThinSOT™	300kHz Constant-Frequency, Adjustable Slope Compensation, Optimized for High Input Voltage Applications
LTC3825	Isolate No-Opto Synchronous Flyback Controller with Wide Input Supply Range	Adjustable Switching Frequency, Programmable Undervoltage Lockout, Accurate Regulation without Trim, Synchronous for High Efficiency
LTC4257	IEEE 802.3af PD Interface Controller	100V 400mA Internal Switch, Programmable Classification
LTC4257-1	IEEE 802.3af PD Interface Controller	100V 400mA Internal Switch, Programmable Classification Dual Current Limit
LTC4258	Quad IEEE 802.3af Power over Ethernet Controller	DC Disconnect Only, IEEE-Compliant PD Detection and Classification, Autonomous Operation or I^2C Control
LTC4259A-1	Quad IEEE 802.3af Power over Ethernet Controller	AC or DC Disconnect IEEE-Compliant PD Detection and Classification, Autonomous Operation or I^2C Control
LTC4263	Single IEEE 802.3af Power over Ethernet Controller	AC or DC Disconnect IEEE-Compliant PD Detection and Classification, Autonomous Operation or I^2C Control
LTC4263-1	High Power Single PSE Controller with Internal Switch	30W PSE Output Power, Internal MOSFET with Thermal Protection
LTC4264	High Power PD Interface Controller	750mA Internal Switch, Programmable Classification, Complementary Power Good Outputs
LTC4267-1	IEEE 802.3af PD Interface with an Integrated Switching Regulator	100V 400mA Internal Switch, Programmable Classification, 200kHz Constant-Frequency PWM, Interface and Switcher Optimized for IEEE-Compliant PD System

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