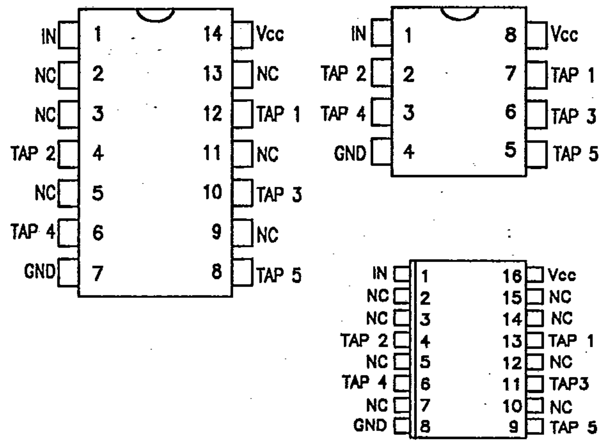
Dallas Semiconductor 5 TAP SILICON DELAY LINE

DS1005 14-Pin DIP
DS1005M 8-Pin DIP
DS1005S 16-Pin SOIC

FEATURES

- All silicon time delay
- 5 TAPS equally spaced. Delay tolerance ± 2 ns or ± 2% whichever is greater
- Stable and precise over temperature and voltage range
- Leading and trailing edge accuracy
- Standard 14-pin DIP, 8-pin DIP, or 16-pin SOIC
- Auto-insertable
- Low power CMOS
- TTL compatible
- Custom delays available

PIN CONNECTIONS



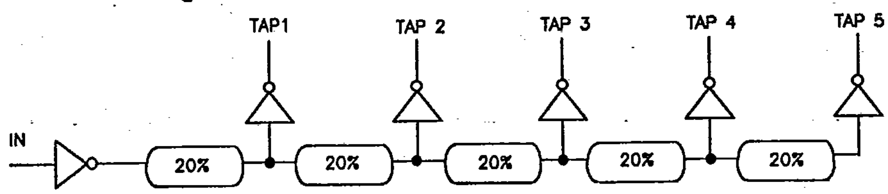
PIN NAMES

TAP 1-TAP 5	- TAP Output Number
Vcc	- +5 Volts
GND	- Ground
NC	- No Connection
IN	- Input

DESCRIPTION

The DS1005 Delay Line Product Family provides five equally spaced TAPS with delays ranging from 10 ns to 500 ns, with an accuracy of ± 2 ns or 2%. These devices are offered in a standard 14 pin DIP, compatible with existing delay line products. A space saving 8 pin -DIP is also available. The 14 pin DIP, the 8 pin -DIP, and SOIC packaging are available in a surface mountable "gullwing" construction. Since the DS1005 is an all silicon solution, better economy and reliability are achieved when compared to older methods using hybrid technology. The DS1005 Delay Line reproduces the input logic level at each TAP after the fixed delay specified by the "dash number" in Table 1. The device is designed to produce both the leading and trailing edge delays with equal precision. Each TAP is capable of driving up to ten 74LS loads.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

PART NO.	TAP 1	TAP2	TAP3	TAP4	TAP5
DS1005-75*	15ns	30ns	45ns	60ns	75ns
DS1005-100	20ns	40ns	60ns	80ns	100ns
DS1005-125	25ns	50ns	75ns	100ns	125ns
DS1005-150	30ns	60ns	90ns	120ns	150ns
DS1005-175	35ns	70ns	105ns	140ns	175ns
DS1005-200	40ns	80ns	120ns	160ns	200ns
DS1005-250*	50ns	100ns	150ns	200ns	250ns
DS1005-500*	100ns	200ns	300ns	400ns	500ns

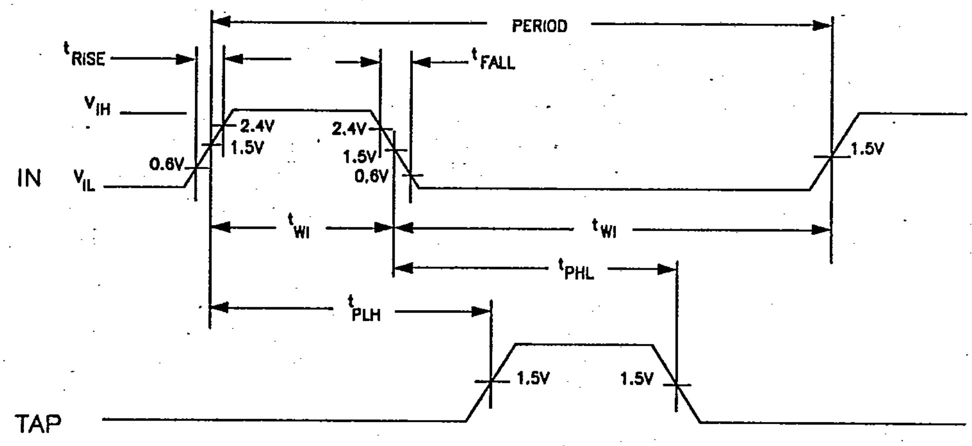
*Consult Dallas Semiconductor for availability

ABSOLUTE MAXIMUM RATINGS*

Voltage on a pin to ground: -1.0Vto + 7.0V
Operating temperature: 0°C to 70°C
Storage temperature: -55°C to + 125°C
Soldering temperature: 260°C for 10 seconds
Short circuit output current: 50mA for 1 second

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

TIMING DIAGRAM- SILICON DELAY LINE Figure 2



TERMINOLOGY

Period The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width) The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time) The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time) The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

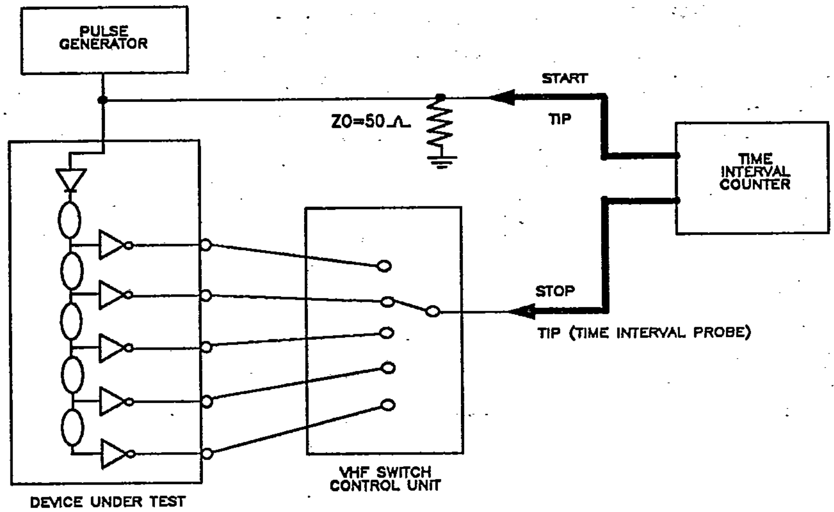
t_{PLH} (Time Delay, Rising) The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any TAP output pulse.

t_{PHL} (Time Delay, Falling) The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any TAP output pulse.

NOTES

1. All voltages are referenced to ground.
2. Measured with outputs open, minimum period.
3. Vcc=5V @25°C Delays accurate on both rising and falling edges within +/- 2 ns.
4. See Test Conditions (following page).
5. The combination of temperature vari ations between 0°C and 70°C and voltage variations between 4.75 volts and 5.25 volts produce a worst case delay shift of +/- 5%.

DALLAS SEMICONDUCTOR TEST CIRCUIT Figure 3



TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1005. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each TAP. Each TAP is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS-INPUT:

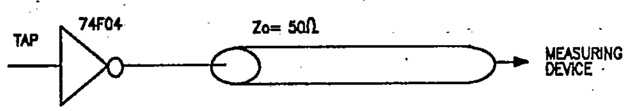
Ambient Temperature: 25°C+/-3°C
Supply Voltage (Vcc): 5.0V+/-0.1V
Input Pulse: High = 3.0V+/-0.1V
Low = 0.0V+/-0.1V
Source Impedance: 50 ohm Max.
Rise and Fall Time: 3.0 ns Max.
(measured between 0.6V and 2.4V)
Pulse Width = 500 ns
Period= 1us

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

OUTPUT:

Each output is loaded with a 74F04. Delay is measured at the 1.5V level on the rising and falling edge.



T-47-13

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, Vcc = 5.0V +/- 5%)

PARAMETER	SYMBOL	TEST COND.	MIN.	TYP.	MAX.	UNITS	NOTES
Supply Voltage	Vcc		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		5.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	0.0V≤VI≤Vcc	-1.0		1.0	uA	
Active Current	I_{CC}	Vcc= Max; Period= Min.		40.0	70.0	mA	2
High Level Output Current	I_{OH}	Vcc= Min. V_{OH}= 2.4V			-1.0	mA	
Low Level Output Current	I_{OL}	Vcc=Min V_{OL}=0.5V	12.0			mA	

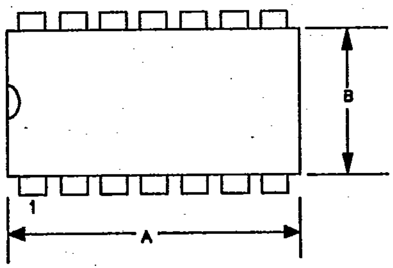
A.C. ELECTRICAL CHARACTERISTICS (T_A= 25°C, Vcc=5V+/- 5%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Pulse Width	t_{WI}	40%ofTAP5			ns	
Input to TAP delay (leading edge)	t_{PLH}	note 3	Table 1	note 3	ns	4,5
Input to TAP Delay (trailing edge)	t_{PHL}	note 3	Table 1	note 3	ns	4,5
	Period	4 (tWI)			ns	

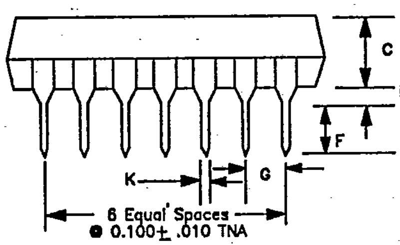
CAPACITANCE (T_A=25°C)

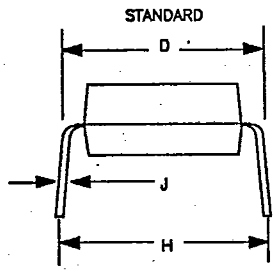
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Output Capacitance	C_{OUT}		5	10	pF	

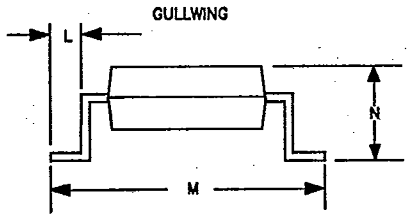
Silicon Delay Line
DS1005
14-Pin DIP



DIM.	INCHES	
	MIN.	MAX.
A	0.740	0.780
B	0.240	0.260
C	0.120	0.140
D	0.290	0.310
E	0.020	0.040
F	0.110	0.130
G	0.090	0.110
H	.320	.370
J	0.008	0.012
K	0.015	0.021
L	0.040	0.060
M	0.370	0.420
N	0.160	0.180

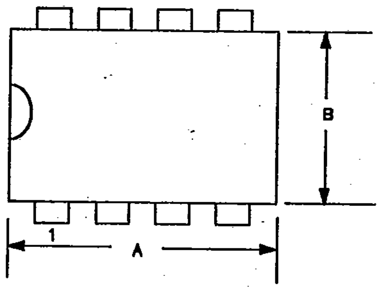




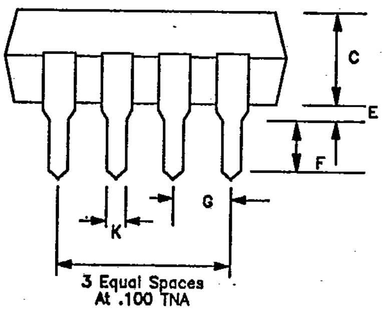


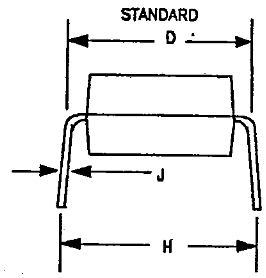
T-47-13

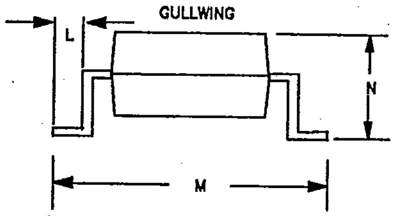
Silicon Delay Line
DS1005M
8-Pin DIP



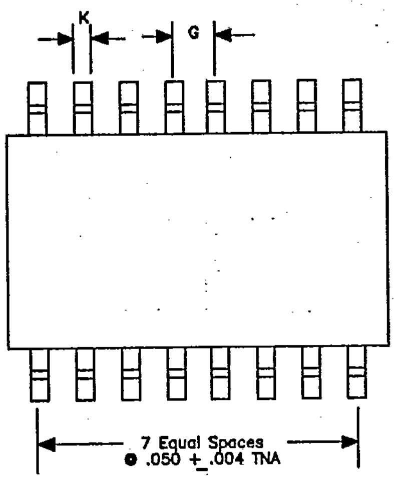
DIM.	INCHES	
	MIN.	MAX.
A	0.345	0.400
B	0.240	0.260
C	0.120	0.140
D	0.290	0.310
E	0.020	0.040
F	0.110	0.130
G	0.090	0.110
H	.320	.370
J	0.008	0.012
K	0.015	0.021
L	0.040	0.060
M	0.370	0.420
N	0.160	0.180







Silicon Delay Line DS1005S 16-Pin SOIC



DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019