Agilent Technologies

Very High CMR, Wide V_{CC} Logic Gate Optocouplers

Technical Data

HCPL-2201 HCPL-2202
HCPL-2211 HCPL-2212
HCPL-2231 HCPL-2232
HCPL-0201 HCPL-0211
HCNW2201 HCNW2211

Features

- **10 kV/µs Minimum Common Mode Rejection (CMR) at V_{CM} = 1000 V (HCPL-2211/2212/0211/ 2232, HCNW2211)**
- **Wide Operating V_{CC} Range: 4.5 to 20 Volts**
- **300 ns Propagation Delay Guaranteed over the Full Temperature Range**
- **5 Mbd Typical Signal Rate**
- **Low Input Current (1.6 mA to 1.8 mA)**
- **Hysteresis**
- **Totem Pole Output (No Pullup Resistor Required)**
- **Available in 8-Pin DIP, SOIC-8, Widebody Packages**
- **Guaranteed Performance from -40°C to 85°C**
- **Safety Approval**
  UL Recognized -3750 V rms for 1 minute (5000 V rms for 1 minute for HCNW22XX) per UL1577
  CSA Approved
  IEC/EN/DIN EN 60747-5-2 Approved with V_{IORM} = 630 V peak (HCPL-2211/2212 Option 060 only) and V_{IORM} = 1414 V peak (HCNW22XX only)
- **MIL-PRF-38534 Hermetic Version Available (HCPL-52XX/62XX)**

Applications

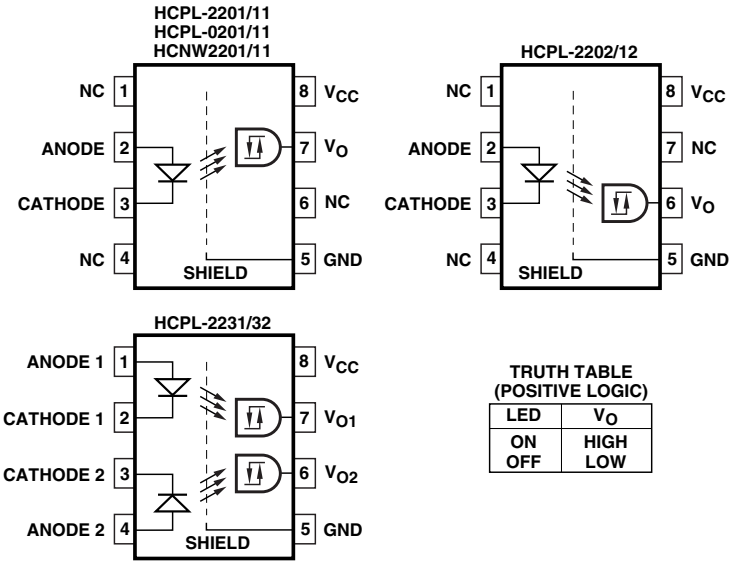
- **Isolation of High Speed Logic Systems**
- **Computer-Peripheral Interfaces**
- **Microprocessor System Interfaces**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**
- **High Speed Line Receiver**
- **Power Control Systems**

Description

The HCPL-22XX, HCPL-02XX, and HCNW22XX are optically-coupled logic gates. The HCPL-22XX, and HCPL-02XX contain a GaAsP LED while the HCNW22XX contains an AlGaAs LED. The detectors have totem pole output stages and optical receiver input stages with built-in Schmitt triggers to provide logic-compatible waveforms, eliminating the need for additional waveshaping.

A superior internal shield on the HCPL-2211/12, HCPL-0211,

Functional Diagram



TRUTH TABLE (POSITIVE LOGIC)

LED	V_O
ON	HIGH
OFF	LOW

A 0.1 µF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

HCPL-2232 and HCNW2211 guarantees common mode transient immunity of 10 kV/µs at a common mode voltage of 1000 volts.

The electrical and switching characteristics of the HCPL-22XX, HCPL-02XX and HCNW22XX are guaranteed from -40°C to +85°C and a V_{CC} from 4.5 volts to 20 volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic and result in lower power consumption compared to other high speed couplers. Logic signals are transmitted with a typical propagation delay of 150 ns.

Selection Guide

Minimum CMR		Input On-Current (mA)	8-Pin DIP (300 Mil)		Small-Outline SO-8	Widebody (400 Mil)	Hermetic
dV/dt (V/µs)	V_{CM} (V)		Single Channel Package	Dual Channel Package	Single Channel Package	Single Channel Package	Single and Dual Channel Packages
1,000	50	1.6	HCPL-2200[1,2] HCPL-2201 HCPL-2202		HCPL-0201	HCNW2201	
		1.8		HCPL-2231			
2,500	400	1.6	HCPL-2219[1,2]				
5,000[3]	300[3]	1.6	HCPL-2211 HCPL-2212		HCPL-0211	HCNW2211	
		1.8		HCPL-2232			
1,000	50	2.0					HCPL-52XX[2] HCPL-62XX[2]

Notes:
1. HCPL-2200/2219 devices include output enable/disable function.
2. Technical data for the HCPL-2200/2219, HCPL-52XX and HCPL-62XX are on separate Agilent publications.
3. Minimum CMR of 10 kV/µs with V_{CM} = 1000 V can be achieved with input current, I_F, of 5 mA.

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

HCPL-2211#XXXX

- 060 = IEC/EN/DIN EN 60747-5-2 V_{IORM} = 630 V peak Option*
- 300 = Gull Wing Surface Mount Option**
- 500 = Tape and Reel Packaging Option
- XXXE = Lead Free Option

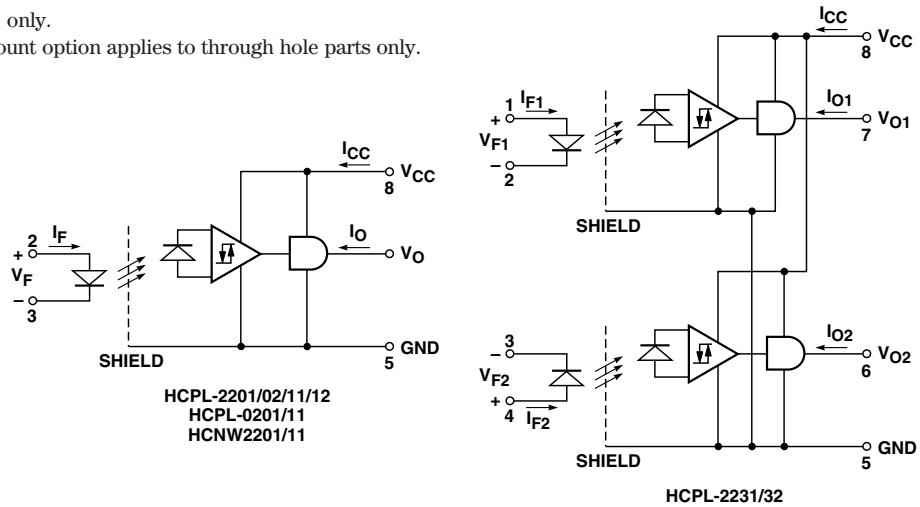
Option data sheets available. Contact your Agilent sales representative or authorized distributor for information.

Remarks: The notation "#" is used for existing products, while (new) products launched since 15th July 2001 and lead free option will use "-"

*For HCPL-2211/2212 only.

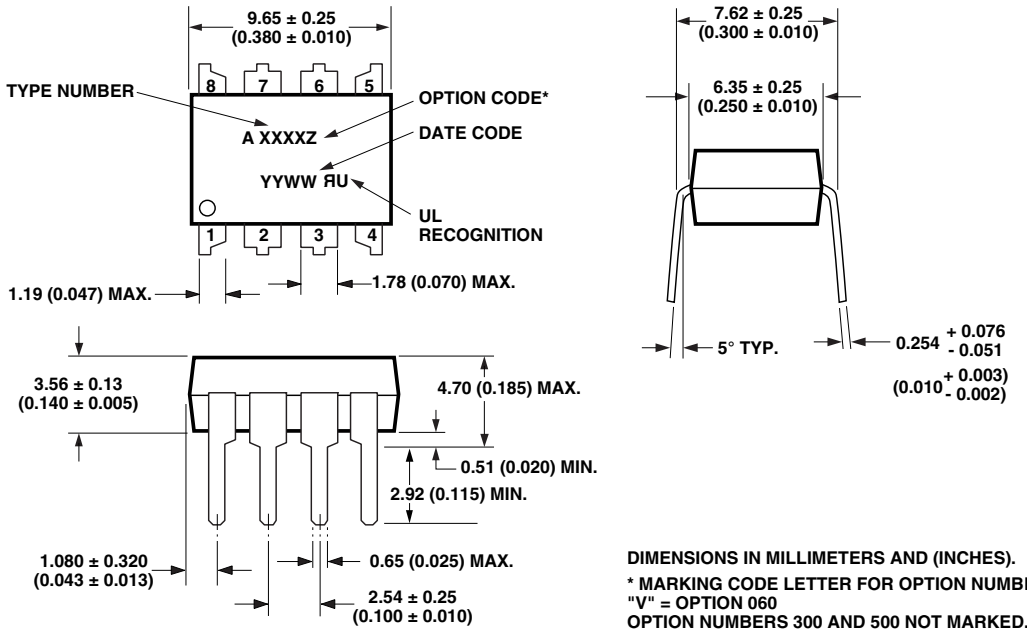
**Gull wing surface mount option applies to through hole parts only.

Schematic



Package Outline Drawings

8-Pin DIP Package (HCPL-2201/02/11/12/31/32)

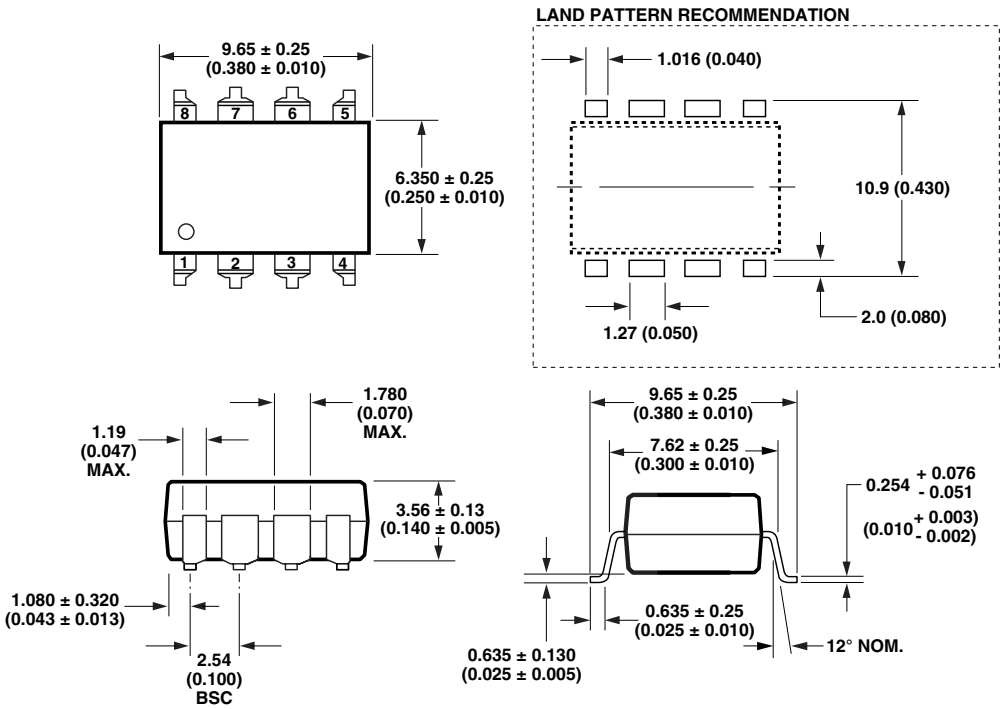


DIMENSIONS IN MILLIMETERS AND (INCHES).

* MARKING CODE LETTER FOR OPTION NUMBERS
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

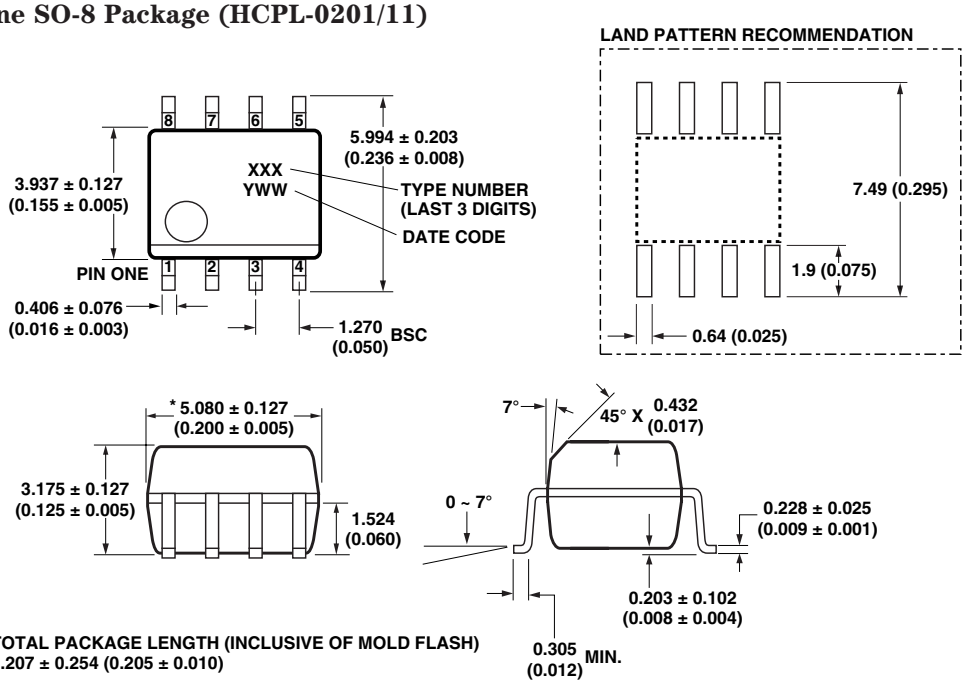
8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-2201/02/11/12/31/32)



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Small-Outline SO-8 Package (HCPL-0201/11)

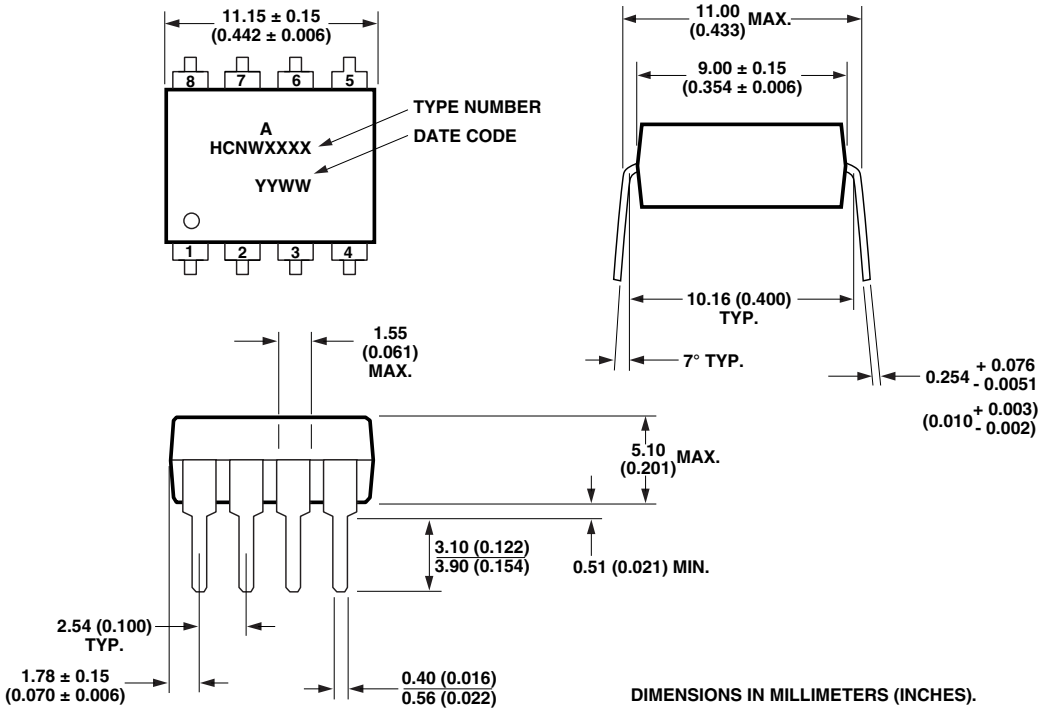


* TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

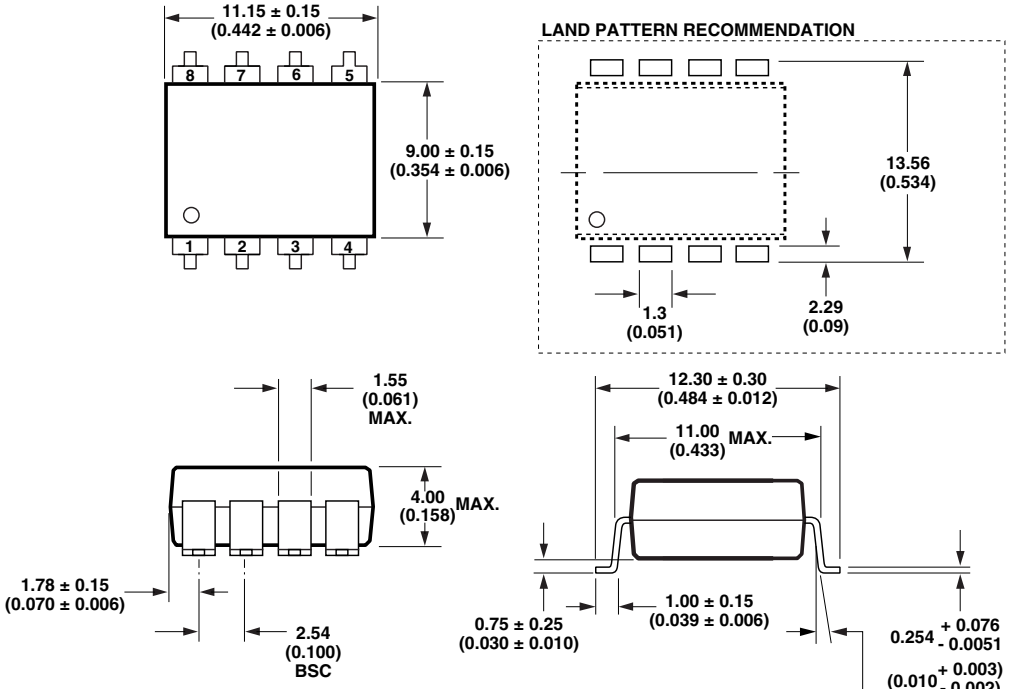
8-Pin Widebody DIP Package (HCNW2201/11)



DIMENSIONS IN MILLIMETERS (INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

8-Pin Widebody DIP Package with Gull Wing Surface Mount Option 300 (HCNW2201/11)

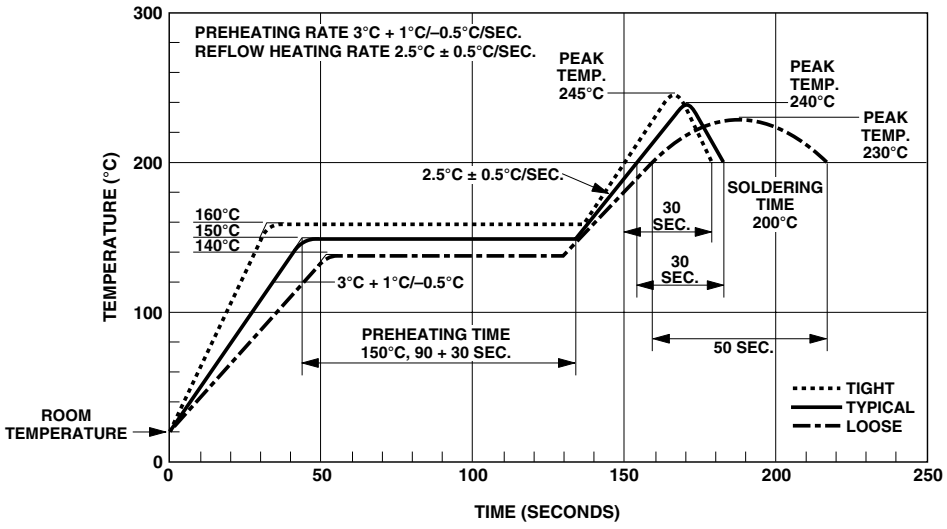


DIMENSIONS IN MILLIMETERS (INCHES).

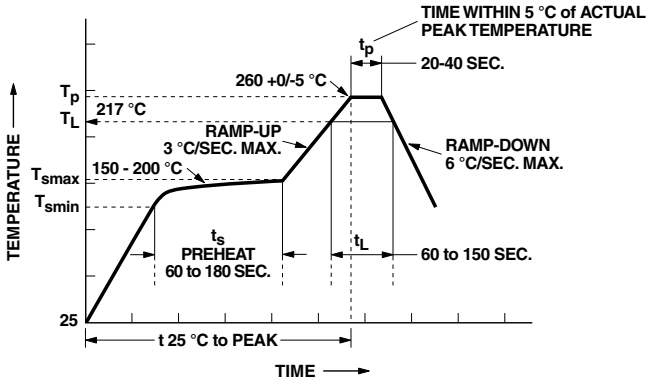
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Solder Reflow Temperature Profile



Recommended Pb-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

Regulatory Information

The HCPL-22XX/02XX and HCNW22XX have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-2

Approved under:
IEC 60747-5-2:1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01
(Option 060 and HCNW only)

Insulation and Safety Related Specifications

8-pin DIP Package

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Widebody (400 Mil) Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics (HCPL-2211/2212 Option 060 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 300 V rms		I-IV	
for rated mains voltage ≤ 450 V rms		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 12, Thermal Derating curve.) Case Temperature Input Current Output Power	 T_S $I_{S,OUTPUT}$ $P_{S,OUTPUT}$	 175 230 600	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-2, for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics (HCNW22XX ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 600 V rms		I-IV	
for rated mains voltage ≤ 1000 V rms		I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2652	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	2121	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	8000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 12, Thermal Derating curve.)			
Case Temperature	T_S	150	℃
Current (Input Current I_F, P_S = 0)	$I_{S,INPUT}$	400	mA
Output Power	$P_{S,OUTPUT}$	700	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-2, for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Note
Storage Temperature		T_S	-55	125	℃	
Operating Temperature		T_A	-40	85	℃	
Average Forward Input Current		$I_{F(AVG)}$		10	mA	1
Peak Transient Input Current (≤ 1 µs Pulse Width, 300 pps)		$I_{F(TRAN)}$		1.0	A	1
(≤ 200 µs Pulse Width, < 1% Duty Cycle)	HCNW22XX			40	mA	
Reverse Input Voltage		V_R		5	V	1
	HCNW22XX			3		
Average Output Current		I_O		25	mA	1
Supply Voltage		V_{CC}	0	20	V	
Output Voltage		V_O	-0.5	20	V	1
Total Package Power Dissipation		P_T		210	mW	2
	HCPL-223X			294		
Output Power Dissipation		P_O	See Figure 7			1
Lead Solder Temperature (Through Hole Parts Only)		260℃ for 10 sec., 1.6 mm below seating plane				
	HCNW22XX	260℃ for 10 sec., up to seating plane				
Solder Reflow Temperature Profile (Surface Mount Parts Only)		See Package Outline Drawings section				

Recommended Operating Conditions

Parameter		Symbol	Min.	Max.	Units
Power Supply Voltage		V_{CC}	4.5	20	V
Forward Input Current (ON)		$I_{F(ON)}$	1.6*	5	mA
	HCPL-223X		1.8†		
Forward Input Voltage (OFF)		$V_{F(OFF)}$	-	0.8	V
Operating Temperature		T_A	-40	85	℃
Junction Temperature		T_J	-40	125	℃
Fan Out		N		4	TTL Loads

*The initial switching threshold is 1.6 mA or less. It is recommended that 2.2 mA be used to permit at least a 20% LED degradation guardband.
†The initial switching threshold is 1.8 mA or less. It is recommended that 2.5 mA be used to permit at least a 20% LED degradation guardband.

Electrical Specifications

-40℃ ≤ T_A ≤ 85℃, 4.5 V ≤ V_{CC} ≤ 20 V, 1.6 mA ≤ $I_{F(ON)}$* ≤ 5 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V, unless otherwise specified. All Typicals at T_A = 25℃. See Note 7.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Logic Low Output Voltage	V_{OL}			0.5	V	I_{OL} = 6.4 mA (4 TTL Loads)		1, 3	1
Logic High Output Voltage	V_{OH}	2.4	**		V	I_{OH} = -2.6 mA		2, 3, 8	1
		2.7				I_{OH} = -0.4 mA			
Output Leakage Current (V_{OUT} > V_{CC})	I_{OHH}			100	µA	V_O = 5.5 V	I_F = 5 mA		1
				500		V_O = 20 V			
Logic Low Supply Current	I_{CCL}		3.7	6.0	mA	V_{CC} = 5.5 V	V_F = 0 V I_O = Open		
			4.3	7.0		V_{CC} = 20 V			
HCPL-223X			7.4	12.0		V_{CC} = 5.5 V			
			8.6	14.0		V_{CC} = 20 V			
Logic High Supply Current	I_{CCH}		2.4	4.0	mA	V_{CC} = 5.5 V	I_F = 5 mA I_O = Open		
			2.7	5.0		V_{CC} = 20 V			
HCPL-223X			4.8	8.0		V_{CC} = 5.5 V			
			5.4	10.0		V_{CC} = 20 V			
Logic Low Short Circuit Output Current	I_{OSL}	15			mA	V_O = V_{CC} = 5.5 V	V_F = 0 V		1, 3
		20				V_O = V_{CC} = 20 V			
Logic High Short Circuit Output Current	I_{OSH}			-10	mA	V_{CC} = 5.5 V	I_F = 5 mA V_O = GND		1, 3
				-20		V_{CC} = 20 V			
Input Forward Voltage	V_F		1.5	1.7	V	T_A = 25℃	I_F = 5 mA	4	1
				1.85					
HCNW22XX			1.5	1.82		T_A = 25℃			
				1.95					
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA			1
HCNW22XX		3				I_R = 100 µA			
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.7		mV/°C	I_F = 5 mA			
HCNW22XX			-1.4						
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V			1, 4
HCNW22XX			70						

*For HCPL-223X, 1.8 mA ≤ $I_{F(ON)}$ ≤ 5 mA.
**Typical V_{OH} = V_{CC} - 2.1 V.

Switching Specifications (AC)

-40°C ≤ T_A ≤ 85°C, 4.5 V ≤ V_{CC} ≤ 20 V, 1.6 mA ≤ $I_{F(ON)}$* ≤ 5 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V.
All Typicals at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 3 mA unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		150		ns	Without Peaking Capacitor	5, 6	1, 6
			160			HCNW22XX		
			150	300		With Peaking Capacitor		
Propagation Delay Time to Logic High Output Level	t_{PLH}		110		ns	Without Peaking Capacitor	5, 6	1, 6
			180			HCNW22XX		
			90	300		With Peaking Capacitor		
Output Rise Time (10-90%)	t_r		30		ns		5, 9	1
Output Fall Time (90-10%)	t_f		7		ns		5, 9	1

Parameter	Sym.	Device	Min.	Units	Test Conditions		Fig.	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	HCPL-2201/02 HCPL-0201 HCPL-2231 HCNW2201	1,000	V/µs	$\|V_{CM}\|$ = 50 V I_F = 1.6 mA†	V_{CC} = 5 V T_A = 25°C	10	1, 7
		HCPL-2211/12 HCPL-0211 HCPL-2232 HCNW2211	5,000	V/µs	$\|V_{CM}\|$ = 300 V I_F = 1.6 mA‡			
			10,000	V/µs	$\|V_{CM}\|$ = 1 kV I_F = 5.0 mA			
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	HCPL-2201/02 HCPL-0201 HCPL-2231 HCNW2201	1,000	V/µs	$\|V_{CM}\|$ = 50 V	V_F = 0 V V_{CC} = 5 V T_A = 25°C	10	1, 7
		HCPL-2211/12 HCPL-0211 HCPL-2232 HCNW2211	10,000	V/µs	$\|V_{CM}\|$ = 1 kV			

*For HCPL-223X, 1.8 mA ≤ $I_{F(ON)}$ ≤ 5 mA.
†I_F = 1.8 mA for HCPL-2231.
‡I_F = 1.8 mA for HCPL-2232.

Package Characteristics

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	3750			V rms	RH < 50%, t = 1 min.		5, 10
HCNW22XX		5000				T_A = 25°C		5, 11
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc		5
HCNW22XX		10^{12}	10^{13}			T_A = 25°C		
		10^{11}				T_A = 100°C		
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz,		5
HCNW22XX			0.5	0.6		T_A = 25°C, V_{I-O} = 0 Vdc		
Input-Input Insulation Leakage Current	I_{I-I}		0.005		µA	Relative Humidity = 45%, t = 5 s, V_{I-I} = 500 V		12
Resistance (Input-Input)	R_{I-I}		10^{11}		Ω	V_{I-I} = 500 V		12
Capacitance (Input-Input)	C_{I-I}		0.25		pF	f = 1 MHz		12

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table (if applicable), your equipment level safety specification or Agilent Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage," publication number 5963-2203E.

Notes:

1. Each channel.
2. Derate total package power dissipation, P_T, linearly above 70°C free-air temperature at a rate of 4.5 mW/°C.
3. Duration of output short circuit time should not exceed 10 ms.
4. For single devices, input capacitance is measured between pin 2 and pin 3.
5. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
6. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
7. CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state, V_O > 2.0 V. CM_L is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state, V_O < 0.8 V.
8. For HCPL-2202/12, V_O is on pin 6.
9. Use of a 0.1 µF bypass capacitor connected between pins 5 and 8 is recommended.
10. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V rms for one second (leakage detection current limit, $I_{I-O} \leq 5$ µA). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table, if applicable.
11. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V rms for one second (leakage detection current limit, $I_{I-O} \leq 5$ µA). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table.
12. For HCPL-2231/32 only. Measured between pins 1 and 2, shorted together, and pins 3 and 4, shorted together.

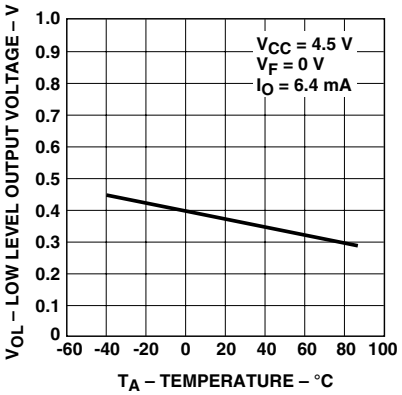


Figure 1. Typical Logic Low Output Voltage vs. Temperature.

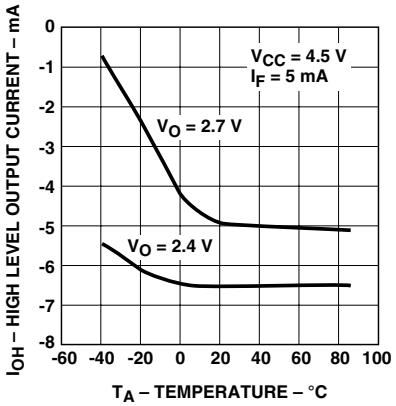


Figure 2. Typical Logic High Output Current vs. Temperature.

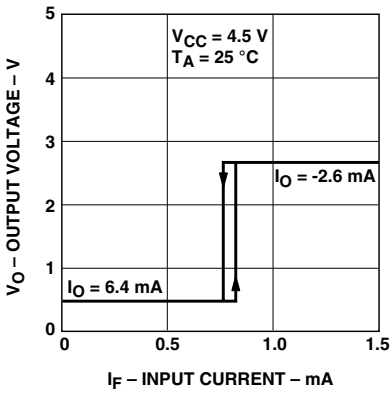


Figure 3. Typical Output Voltage vs. Forward Input Current.

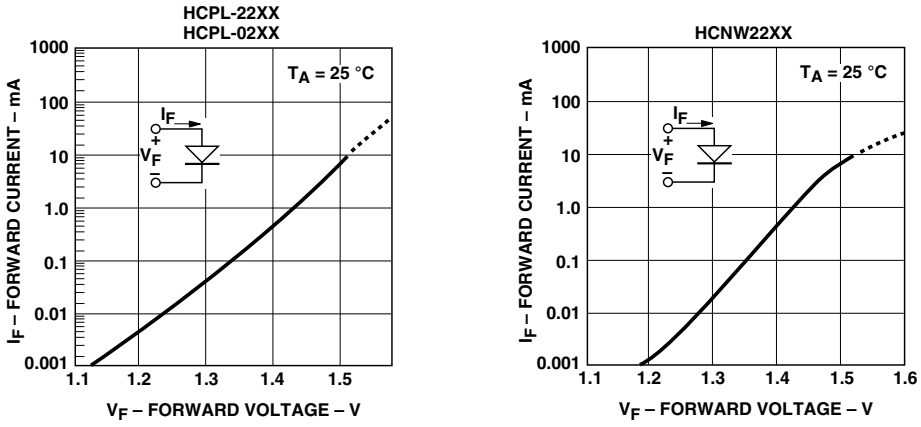
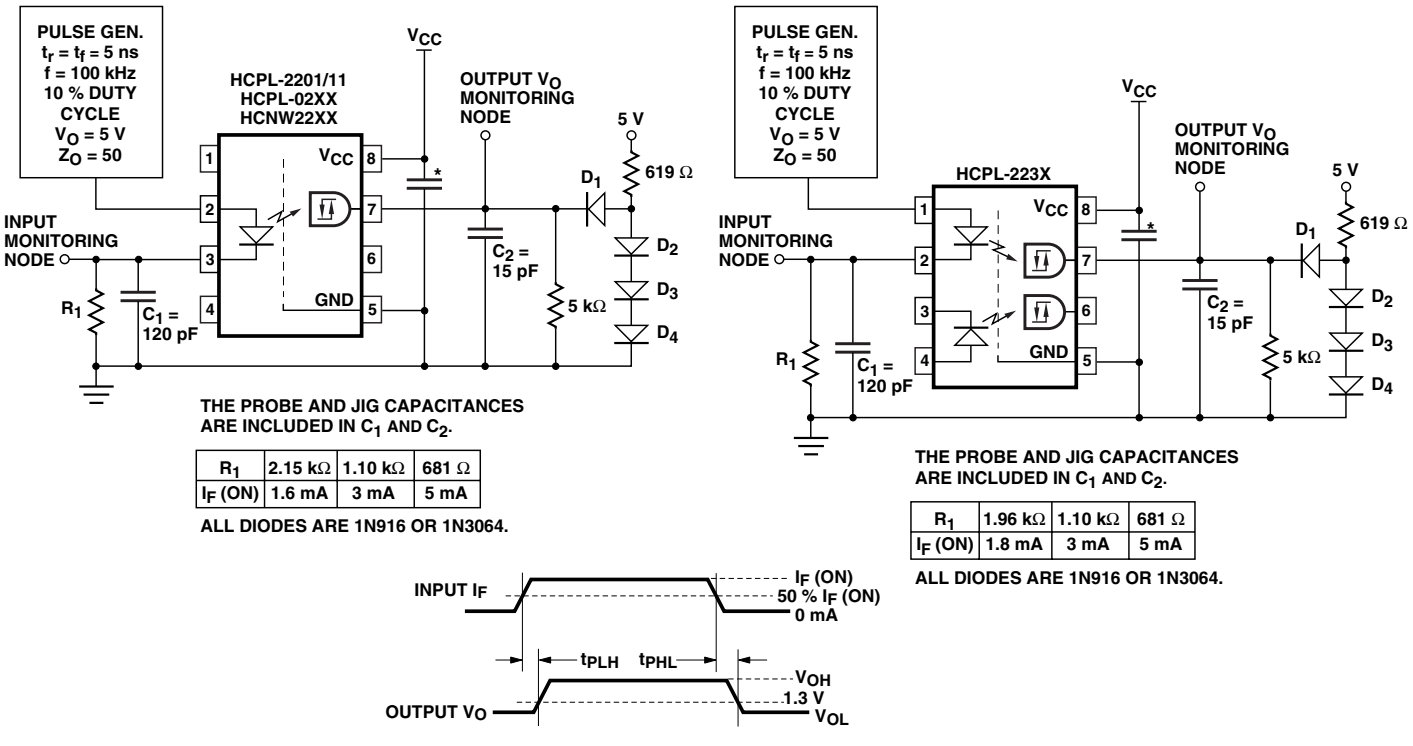


Figure 4. Typical Input Diode Forward Characteristic.

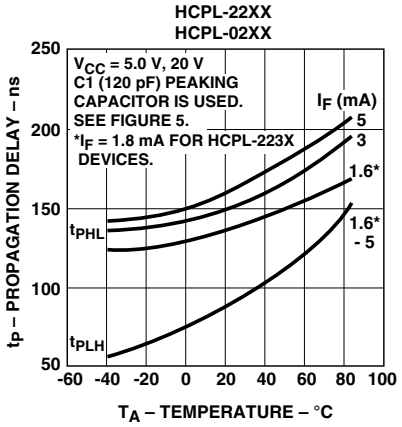


R_1	2.15 kΩ	1.10 kΩ	681 Ω
I_F (ON)	1.6 mA	3 mA	5 mA

R_1	1.96 kΩ	1.10 kΩ	681 Ω
I_F (ON)	1.8 mA	3 mA	5 mA

Figure 5. Circuit for t_{PLH}, t_{PHL}, t_r, t_f.

* 0.1 µF BYPASS — SEE NOTE 9.



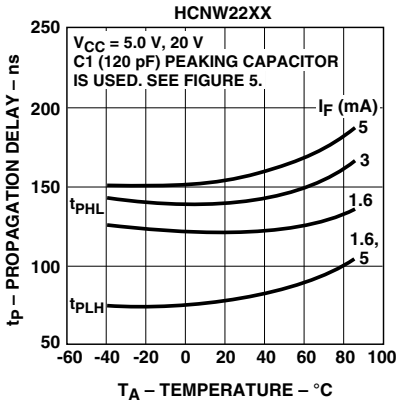


Figure 6. Typical Propagation Delays vs. Temperature.

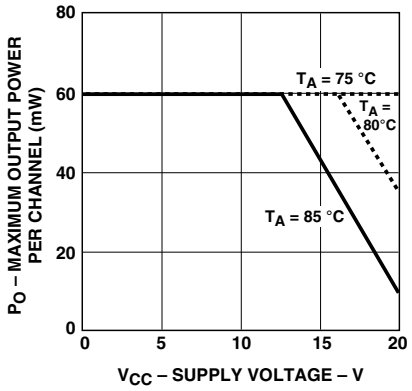


Figure 7. Maximum Output Power per Channel vs. Supply Voltage.

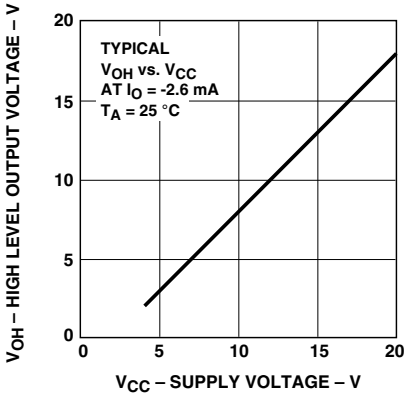


Figure 8. Typical Logic High Output Voltage vs. Supply Voltage.

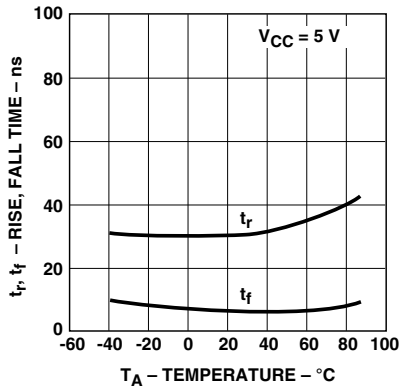


Figure 9. Typical Rise, Fall Time vs. Temperature.

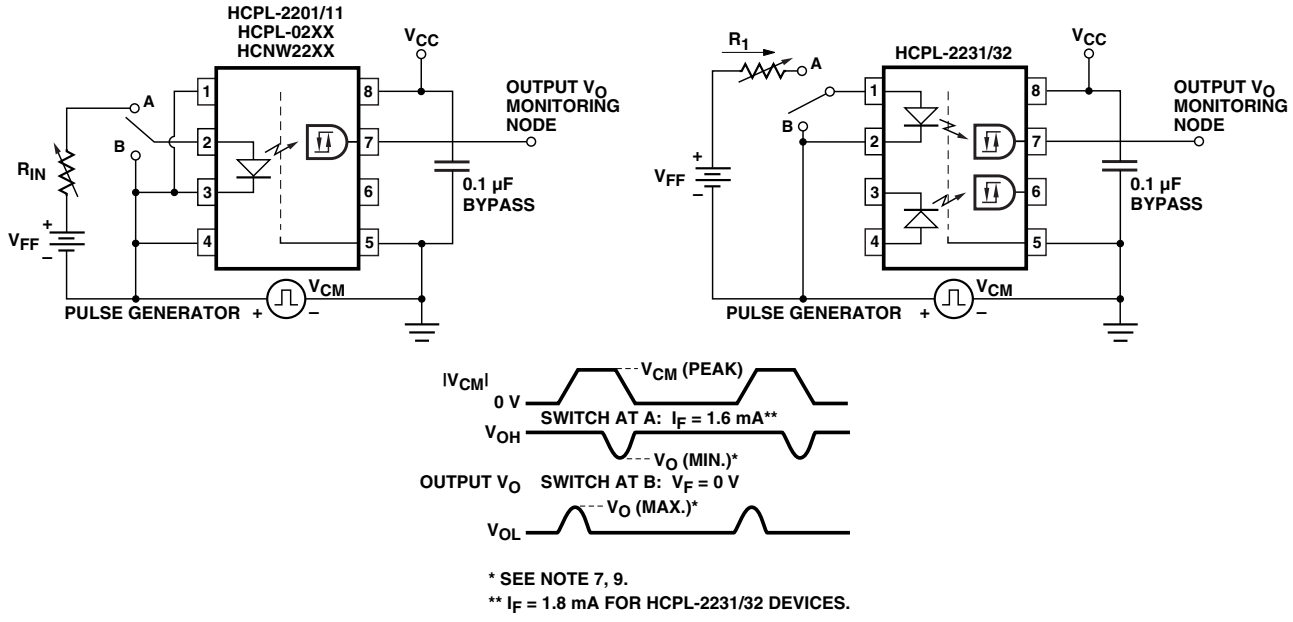


Figure 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

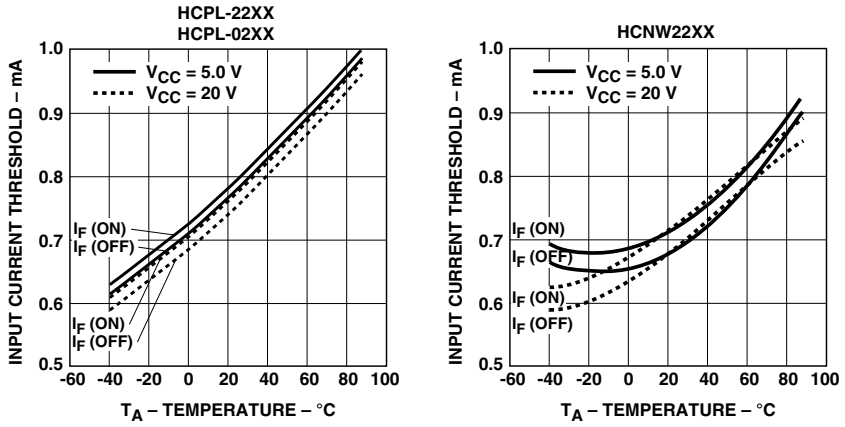


Figure 11. Typical Input Threshold Current vs. Temperature.

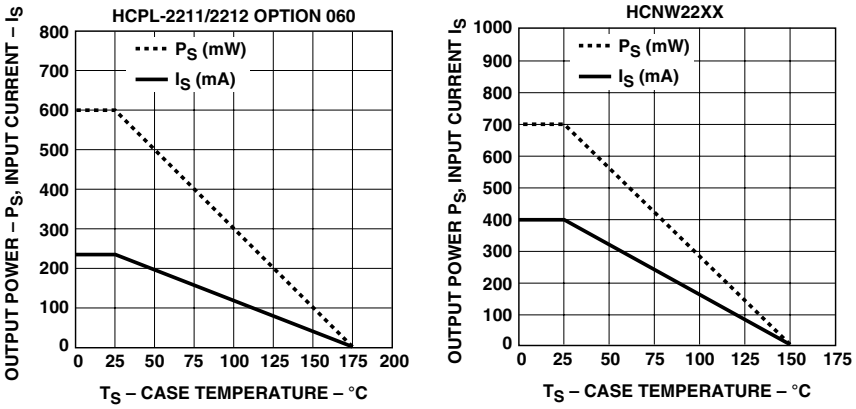


Figure 12. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per IEC/EN/DIN EN 60747-5-2.

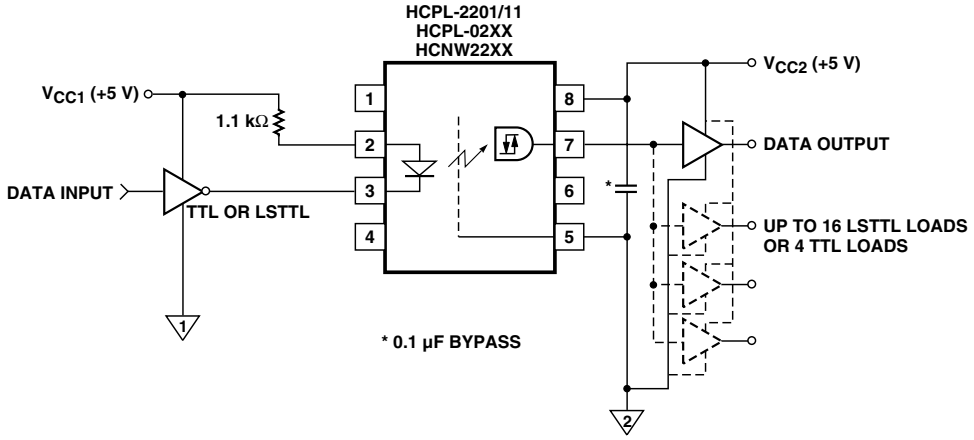


Figure 13a. Recommended LSTTL to LSTTL Circuit where 500 ns Propagation Delay is Sufficient.

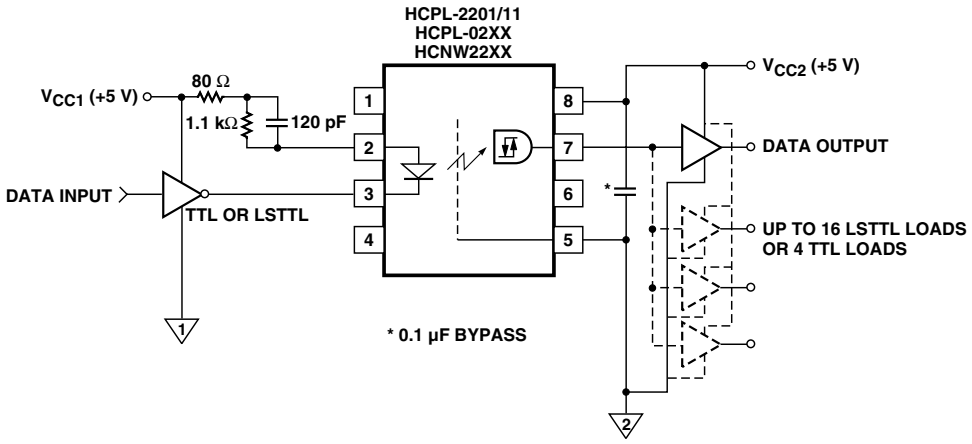


Figure 13b. Recommended LSTTL to LSTTL Circuit for Applications Requiring a Maximum Allowable Propagation Delay of 300 ns.

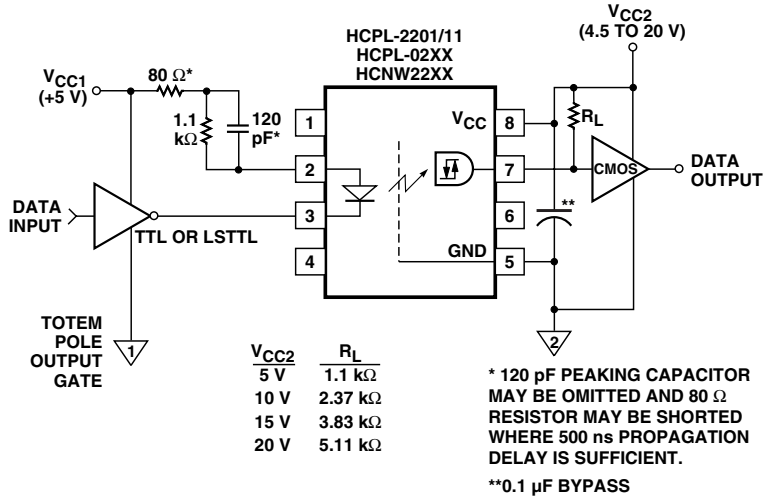


Figure 14. LSTTL to CMOS Interface Circuit.

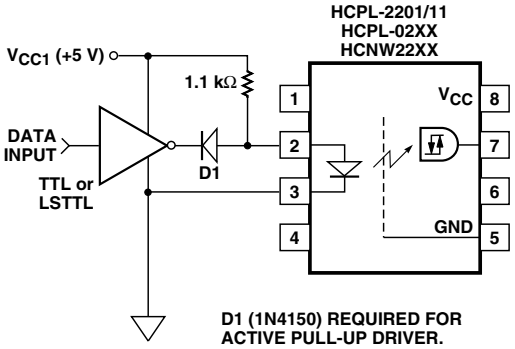


Figure 15. Alternative LED Drive Circuit.

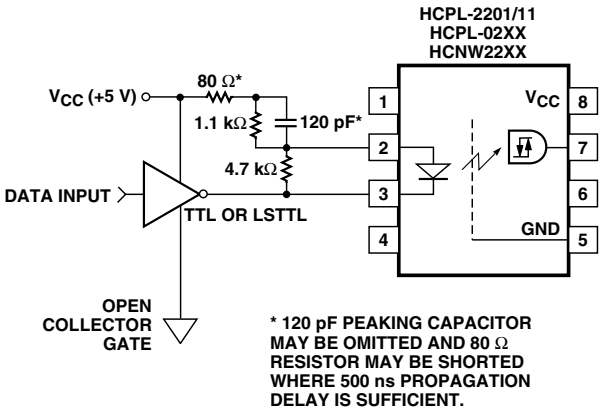


Figure 16. Series LED Drive with Open Collector Gate (4.7 k Resistor Shunts I_{OH} from the LED).

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Data subject to change.

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