CY7C1353G

4-Mbit (256K x 18) Flow-through SRAM with NoBL™ Architecture

Features

- Supports up to 133-MHz bus operations with zero wait states
  - Data is transferred on every clock
- Pin compatible and functionally equivalent to ZBT™ devices
- Internally self timed output buffer control to eliminate the need to use $\overline{OE}$
- Registered inputs for flow-through operation
- Byte Write capability
- 256K x 18 common IO architecture
- 2.5V/3.3V IO power supply (V_{DDQ})
- Fast clock-to-output times
  - 6.5 ns (for 133-MHz device)
- Clock Enable ($\overline{CEN}$) pin to suspend operation
- Synchronous self timed writes
- Asynchronous Output Enable
- Available in Pb-free 100-Pin TQFP package
- Burst Capability — linear or interleaved burst order
- Low standby power

Functional Description[1]

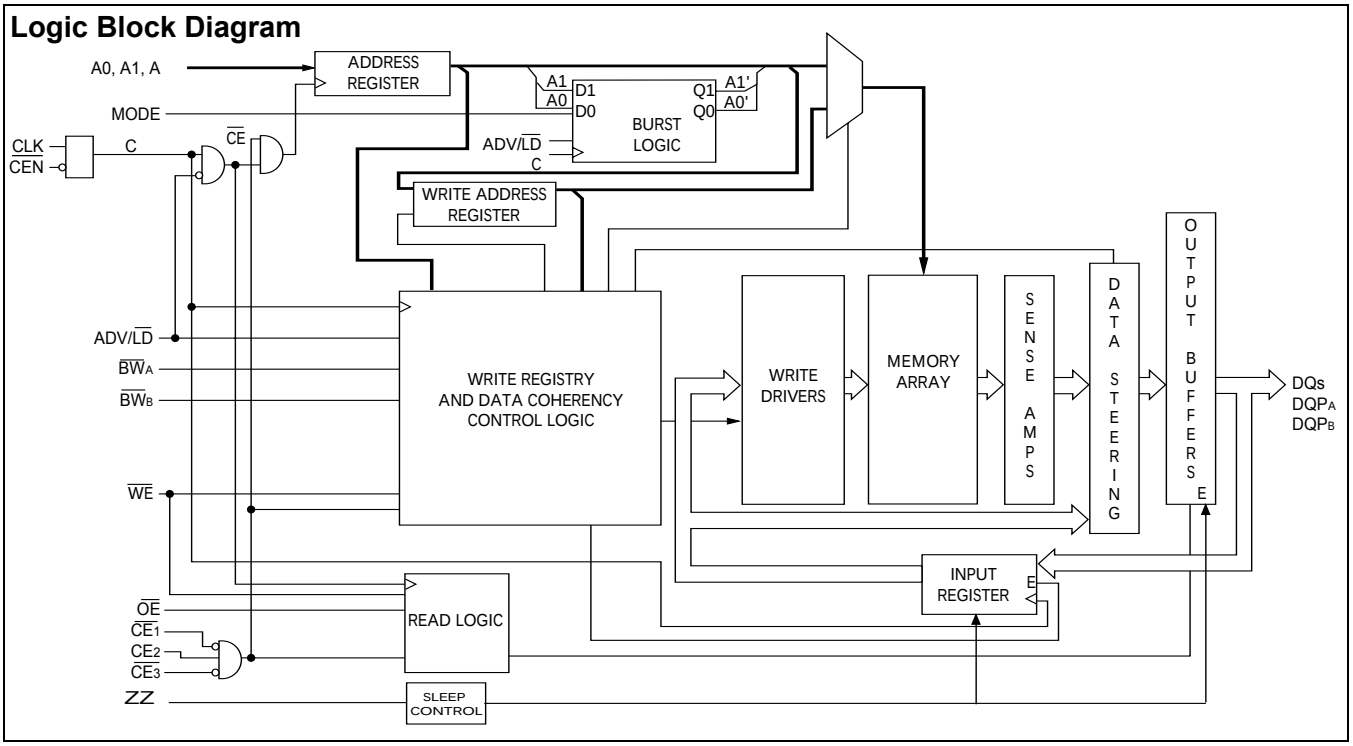
The CY7C1353G is a 3.3V, 256K x 18 Synchronous Flow-through Burst SRAM designed specifically to support unlimited true back-to-back Read/Write operations without the insertion of wait states. The CY7C1353G is equipped with the advanced No Bus Latency™ (NoBL™) logic required to enable consecutive Read/Write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent Write-Read transitions.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 6.5 ns (133-MHz device).

Write operations are controlled by the two Byte Write Select ($\overline{BW}_{[A:B]}$) and a Write Enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self timed write circuitry.

Three synchronous Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. To avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence.

Logic Block Diagram



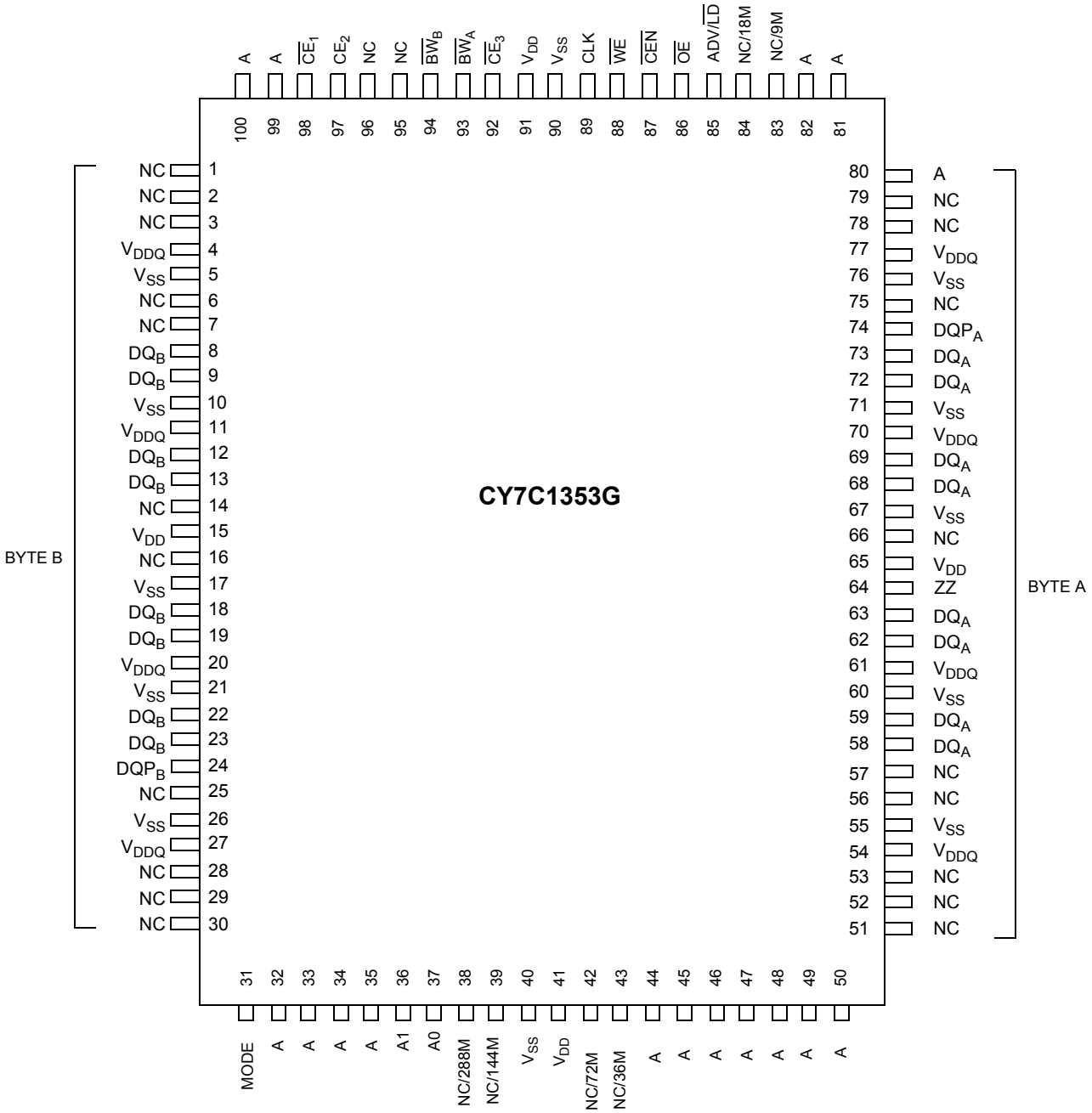
Note:
1.For best-practices recommendations, please refer to the Cypress application note *System Design Guidelines* on www.cypress.com.

Selection Guide

	133 MHz	100 MHz	Unit
Maximum Access Time	6.5	8.0	ns
Maximum Operating Current	225	205	mA
Maximum CMOS Standby Current	40	40	mA

Pin Configuration

100-Pin TQFP Pinout



Pin Definitions

Name	IO	Description
A_0, A_1, A	Input-Synchronous	**Address Inputs used to select one of the 256K address locations**. Sampled at the rising edge of the CLK. $A_{[1:0]}$ are fed to the two-bit burst counter.
$\overline{BW}_{[A:B]}$	Input-Synchronous	**Byte Write Inputs, Active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{WE}$	Input-Synchronous	**Write Enable Input, Active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input-Synchronous	**Advance/Load Input**. Used to advance the on-chip address counter or load a new address. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ must be driven LOW to load a new address.
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2, and $\overline{CE}_3$ to select/deselect the device.
CE_2	Input-Synchronous	**Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
$\overline{OE}$	Input-Asynchronous	**Output Enable, asynchronous input, Active LOW**. Combined with the synchronous logic block inside the device to control the direction of the IO pins. When LOW, the IO pins are allowed to behave as outputs. When deasserted HIGH, IO pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, when the device has been deselected.
$\overline{CEN}$	Input-Synchronous	**Clock Enable Input, Active LOW**. When asserted LOW the Clock signal is recognized by the SRAM. When deasserted HIGH the Clock signal is masked. While deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
ZZ	Input-Asynchronous	**ZZ "sleep" Input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. During normal operation, this pin has to be low or left floating. ZZ pin has an internal pull down.
DQ_s	IO-Synchronous	**Bidirectional Data IO Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by address during the clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, DQ_s and $DQP_{[A:B]}$ are placed in a tri-state condition. The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
$DQP_{[A:B]}$	IO-Synchronous	**Bidirectional Data Parity IO Lines**. Functionally, these signals are identical to DQ_s. During write sequences, $DQP_{[A:B]}$ is controlled by BW_x correspondingly.
MODE	Input Strap Pin	**MODE Input. Selects the burst order of the device.** When tied to Gnd selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{DDQ}	IO Power Supply	**Power supply for the IO circuitry**.
V_{SS}	Ground	**Ground for the device**.
NC,NC/9M, NC/18M, NC/36M NC/72M, NC/144M, NC/288M,	–	**No Connects**. Not internally connected to the die. NC/9M, NC/18M, NC/72M, NC/144M, NC/288M, are address expansion pins are not internally connected to the die.

Functional Overview

The CY7C1353G is a synchronous flow-through burst SRAM designed specifically to eliminate wait states during Write-Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133-MHz device).

Accesses can be initiated by asserting all three Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) active at the rising edge of the clock. If Clock Enable ($\overline{CEN}$) is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the Write Enable ($\overline{WE}$). $BW_{[A:B]}$ can be used to conduct byte write operations.

Write operations are qualified by the Write Enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) simplify depth expansion. All operations (Reads, Writes, and Deselects) are pipe lined. ADV/$\overline{LD}$ must be driven LOW after the device has been deselected to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are ALL asserted active, (3) the Write Enable input signal $\overline{WE}$ is deasserted HIGH, and 4) ADV/$\overline{LD}$ is asserted LOW. The address presented to the address inputs is latched into the Address Register and presented to the memory array and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the output buffers. The data is available within 6.5 ns (133-MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access, the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW in order for the device to drive out the requested data. On the subsequent clock, another operation (Read/Write/Deselect) can be initiated. When the SRAM is deselected at clock rise by one of the chip enable signals, its output is tri-stated immediately.

Burst Read Accesses

The CY7C1353G has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW to load a new address into the SRAM, as described in the Single Read Access section. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ increments the internal burst counter regardless of the state of chip enable inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (Read or Write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when these conditions are satisfied at clock rise:

- $\overline{CEN}$ is asserted LOW
- $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are ALL asserted active
- The write signal $\overline{WE}$ is asserted LOW.

The address presented to the address bus is loaded into the Address Register. The write signals are latched into the Control Logic block. The data lines are automatically tri-stated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQs and $DQP_{[A:B]}$.

On the next clock rise the data presented to DQs and $DQP_{[A:B]}$ (or a subset for byte write operations, see truth table for details) inputs is latched into the device and the write is complete. Additional accesses (Read/Write/Deselect) can be initiated on this cycle.

The data written during the Write operation is controlled by $BW_{[A:B]}$ signals. The CY7C1353G provides byte write capability that is described in the truth table. Asserting the Write Enable input ($\overline{WE}$) with the selected Byte Write Select input selectively writes to only the desired bytes. Bytes not selected during a byte write operation remains unaltered. A synchronous self timed write mechanism has been provided to simplify the write operations. Byte write capability has been included to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte write operations.

Because the CY7C1353G is a common IO device, data must not be driven into the device while the outputs are active. The Output Enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the DQs and $DQP_{[A:B]}$ inputs. Doing so tri-states the output drivers. As a safety precaution, DQs and $DQP_{[A:B]}$ are automatically tri-stated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

Burst Write Accesses

The CY7C1353G has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Write operations without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW to load the initial address, as described in the Single Write Access section. When ADV/$\overline{LD}$ is driven HIGH on the subsequent clock rise, the Chip Enables ($\overline{CE}_1$, CE_2, and $\overline{CE}_3$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The correct $BW_{[A:B]}$ inputs must be driven in each cycle of the burst write, to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE}_1$, CE_2, and $\overline{CE}_3$, must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Linear Burst Address Table (MODE = GND)

First Address A1, A0	Second Address A1, A0	Third Address A1, A0	Fourth Address A1, A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address A1, A0	Second Address A1, A0	Third Address A1, A0	Fourth Address A1, A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ ≥ V_{DD} – 0.2V		40	mA
t_{ZZS}	Device operation to ZZ	ZZ ≥ V_{DD} – 0.2V		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ ≤ 0.2V	$2t_{CYC}$		ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled		$2t_{CYC}$	ns
t_{RZZI}	ZZ inactive to exit sleep current	This parameter is sampled	0		ns

Truth Table [2, 3, 4, 5, 6, 7, 8]

Operation	Address Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	ADV/$\overline{LD}$	$\overline{WE}$	$\overline{BW_X}$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect Cycle	None	H	X	X	L	L	X	X	X	L	L->H	Tri-State
Deselect Cycle	None	X	X	H	L	L	X	X	X	L	L->H	Tri-State
Deselect Cycle	None	X	L	X	L	L	X	X	X	L	L->H	Tri-State
Continue Deselect Cycle	None	X	X	X	L	H	X	X	X	L	L->H	Tri-State
READ Cycle (Begin Burst)	External	L	H	L	L	L	H	X	L	L	L->H	Data Out (Q)
READ Cycle (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L->H	Data Out (Q)
NOP/DUMMY READ (Begin Burst)	External	L	H	L	L	L	H	X	H	L	L->H	Tri-State
DUMMY READ (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L->H	Tri-State
WRITE Cycle (Begin Burst)	External	L	H	L	L	L	L	L	X	L	L->H	Data In (D)
WRITE Cycle (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L->H	Data In (D)
NOP/WRITE ABORT (Begin Burst)	None	L	H	L	L	L	L	H	X	L	L->H	Tri-State
WRITE ABORT (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L->H	Tri-State
IGNORE CLOCK EDGE (Stall)	Current	X	X	X	L	X	X	X	X	H	L->H	–
SLEEP MODE	None	X	X	X	H	X	X	X	X	X	X	Tri-State

Notes:
2. X ="Don't Care." H = Logic HIGH, L = Logic LOW. $\overline{BW}$x = L signifies at least one Byte Write Select is active, $\overline{BW}$x = Valid signifies that the desired byte write selects are asserted, see truth table for details.
3. Write is defined by $\overline{BW_X}$, and $\overline{WE}$. See truth table for Read/Write.
4. When a write cycle is detected, all IOs are tri-stated, even during byte writes.
5. The DQs and $DQP_{[A:B]}$ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
6. $\overline{CEN}$ = H, inserts wait states.
7. Device powers up deselected and the IOs in a tri-state condition, regardless of $\overline{OE}$.
8. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and $DQP_{[A:B]}$ = tri-state when $\overline{OE}$ is inactive or when the device is deselected, and DQs and $DQP_{[A:B]}$ = data when $\overline{OE}$ is active.

Partial Truth Table for Read/Write[2, 3, 9]

Function	$\overline{WE}$	$\overline{BW_A}$	$\overline{BW_B}$
Read	H	X	X
Write – No bytes written	L	H	H
Write Byte A – (DQ_A and DQP_A)	L	L	H
Write Byte B – (DQ_B and DQP_B)	L	H	L
Write All Bytes	L	L	L

Note:
9. Table only lists a partial listing of the byte write combinations. Any combination of BW[A:D] is valid. Appropriate write is based on which byte write is active.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND..... –0.5V to +4.6V

Supply Voltage on V_{DDQ} Relative to GND ..... –0.5V to +V_{DD}

DC Voltage Applied to Outputs in tri-state ..... –0.5V to V_{DDQ} + 0.5V

DC Input Voltage ..... –0.5V to V_{DD} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (MIL-STD-883, Method 3015)

Latch up Current..... > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V – 5%/+10%	2.5V – 5% to V_{DD}
Industrial	–40°C to +85°C		

Electrical Characteristics Over the Operating Range [10,11]

Parameter	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	IO Supply Voltage			2.375	V_{DD}	V
V_{OH}	Output HIGH Voltage	for 3.3V IO, I_{OH} = –4.0 mA		2.4		V
		for 2.5V IO, I_{OH} = –1.0 mA		2.0		V
V_{OL}	Output LOW Voltage	for 3.3V IO, I_{OH} = 8.0 mA			0.4	V
		for 2.5V IO, I_{OH} = 1.0 mA			0.4	V
V_{IH}	Input HIGH Voltage	for 3.3V IO		2.0	V_{DD} + 0.3V	V
	Input HIGH Voltage	for 2.5V IO		1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[10]	for 3.3V IO		–0.3	0.8	V
	Input LOW Voltage[10]	for 2.5V IO		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30		µA
		Input = V_{DD}			5	µA
	Input Current of ZZ	Input = V_{SS}		–5		µA
		Input = V_{DD}			30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	7.5-ns cycle, 133 MHz		225	mA
			10-ns cycle, 100 MHz		205	mA
I_{SB1}	Automatic CE Power down Current—TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}, inputs switching	7.5-ns cycle, 133 MHz		90	mA
			10-ns cycle, 100 MHz		80	mA
I_{SB2}	Automatic CE Power down Current—CMOS Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{DD} – 0.3V or V_{IN} ≤ 0.3V, f = 0, inputs static	All speeds		40	mA
I_{SB3}	Automatic CE Power down Current—CMOS Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{DDQ} – 0.3V or V_{IN} ≤ 0.3V, f = f_{MAX}, inputs switching	7.5-ns cycle, 133 MHz		75	mA
			10-ns cycle, 100 MHz		65	mA
I_{SB4}	Automatic CE Power down Current—TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{DD} – 0.3V or V_{IN} ≤ 0.3V, f = 0, inputs static	All speeds		45	mA

Notes:
10. Overshoot: $V_{IH}(AC) < V_{DD} + 1.5V$ (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL}(AC) > -2V$ (Pulse width less than $t_{CYC}/2$).
11. $T_{Power\text{-}up}$: Assumes a linear ramp from 0V to V_{DD} (min.) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.

Capacitance[12]

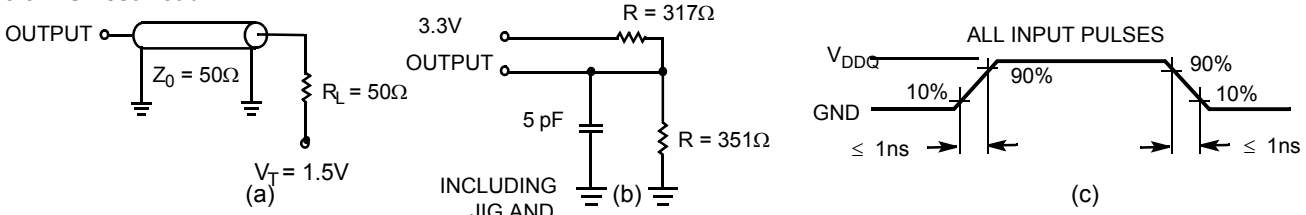
Parameter	Description	Test Conditions	100 TQFP Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V V_{DDQ}=3.3V	5	pF
C_{CLOCK}	Clock Input Capacitance		5	pF
C_{IO}	IO Capacitance		5	pF

Thermal Resistance[12]

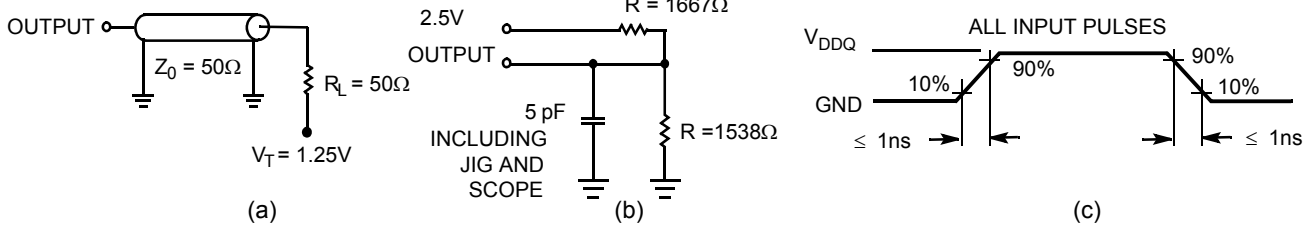
Parameters	Description	Test Conditions	100 TQFP Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51.	30.32	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		6.85	°C/W

AC Test Loads and Waveforms

3.3V IO Test Load



2.5V IO Test Load



Note:
12.Tested initially and after any design or process changes that may affect these parameters.

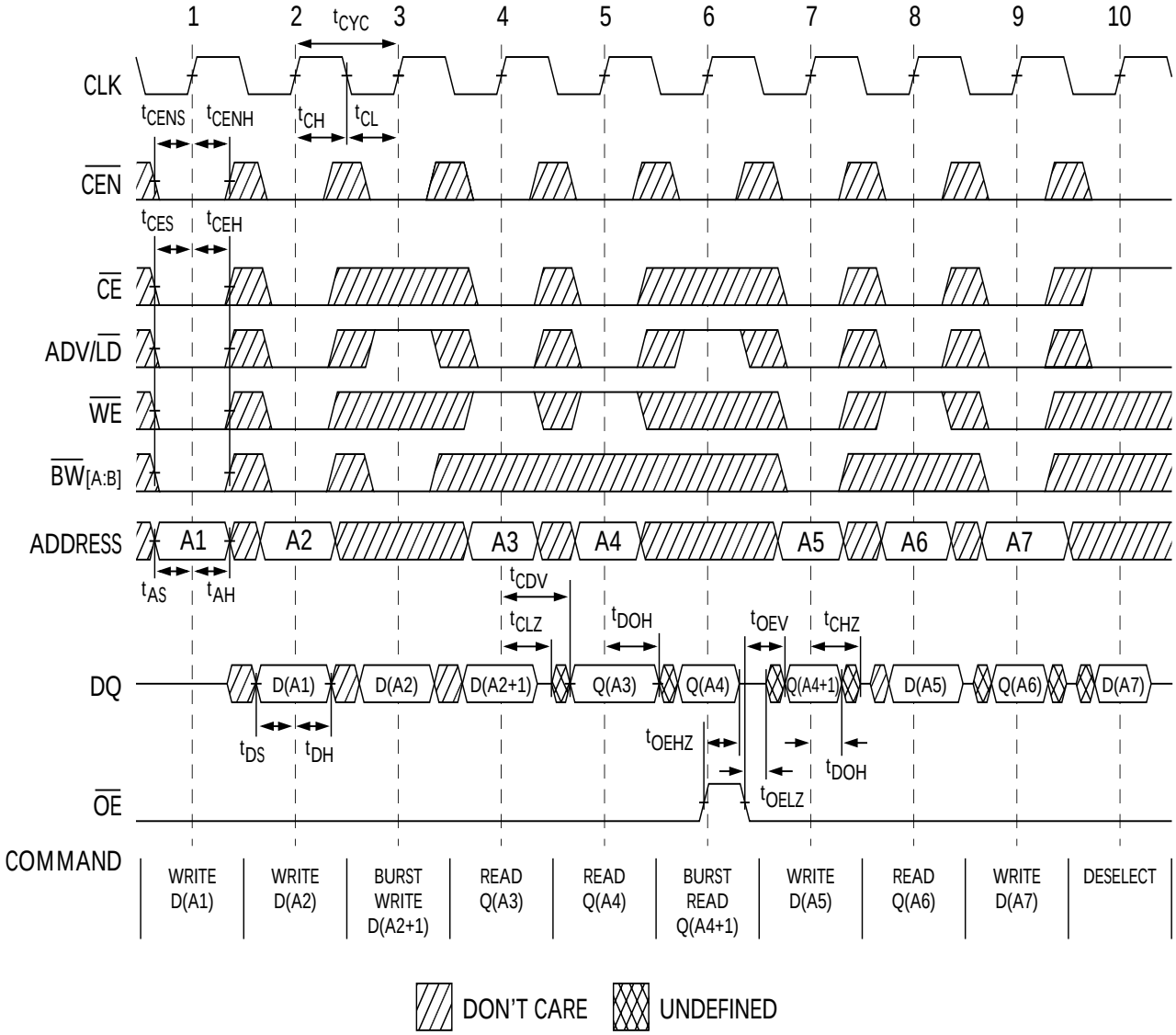
Switching Characteristics Over the Operating Range [17, 18]

Parameter	Description	–133		–100		Unit
		Min	Max	Min	Max	
t_{POWER}	V_{DD}(Typical) to the first Access[13]	1		1		ms
Clock						
t_{CYC}	Clock Cycle Time	7.5		10		ns
t_{CH}	Clock HIGH	2.5		4.0		ns
t_{CL}	Clock LOW	2.5		4.0		ns
Output Times						
t_{CDV}	Data Output Valid After CLK Rise		6.5		8.0	ns
t_{DOH}	Data Output Hold After CLK Rise	2.0		2.0		ns
t_{CLZ}	Clock to Low-Z[14, 15, 16]	0		0		ns
t_{CHZ}	Clock to High-Z[14, 15, 16]		3.5		3.5	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid		3.5		3.5	ns
t_{OELZ}	$\overline{OE}$ LOW to Output Low-Z[14, 15, 16]	0		0		ns
t_{OEHZ}	$\overline{OE}$ HIGH to Output High-Z[14, 15, 16]		3.5		3.5	ns
Setup Times						
t_{AS}	Address Setup Before CLK Rise	1.5		2.0		ns
t_{ALS}	ADV/$\overline{LD}$ Setup Before CLK Rise	1.5		2.0		ns
t_{WES}	$\overline{WE}$, $\overline{BW}_X$ Setup Before CLK Rise	1.5		2.0		ns
t_{CENS}	$\overline{CEN}$ Setup Before CLK Rise	1.5		2.0		ns
t_{DS}	Data Input Setup Before CLK Rise	1.5		2.0		ns
t_{CES}	Chip Enable Setup Before CLK Rise	1.5		2.0		ns
Hold Times						
t_{AH}	Address Hold After CLK Rise	0.5		0.5		ns
t_{ALH}	ADV/$\overline{LD}$ Hold after CLK Rise	0.5		0.5		ns
t_{WEH}	$\overline{WE}$, $\overline{BW}_X$ Hold After CLK Rise	0.5		0.5		ns
t_{CENH}	$\overline{CEN}$ Hold After CLK Rise	0.5		0.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5		0.5		ns

Notes:
13. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above V_{DD} minimum initially before a read or write operation can be initiated.
14. t_{CHZ}, t_{CLZ},t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
15. At any voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve tri-state prior to Low-Z under the same system conditions.
16. This parameter is sampled and not 100% tested.
17. Timing reference level is 1.5V when V_{DDQ}=3.3V and is 1.25V when V_{DDQ}=2.5V.
18. Test conditions shown in (a) of AC Test Loads, unless otherwise noted.

Switching Waveforms

Read/Write Waveforms[19, 20, 21]

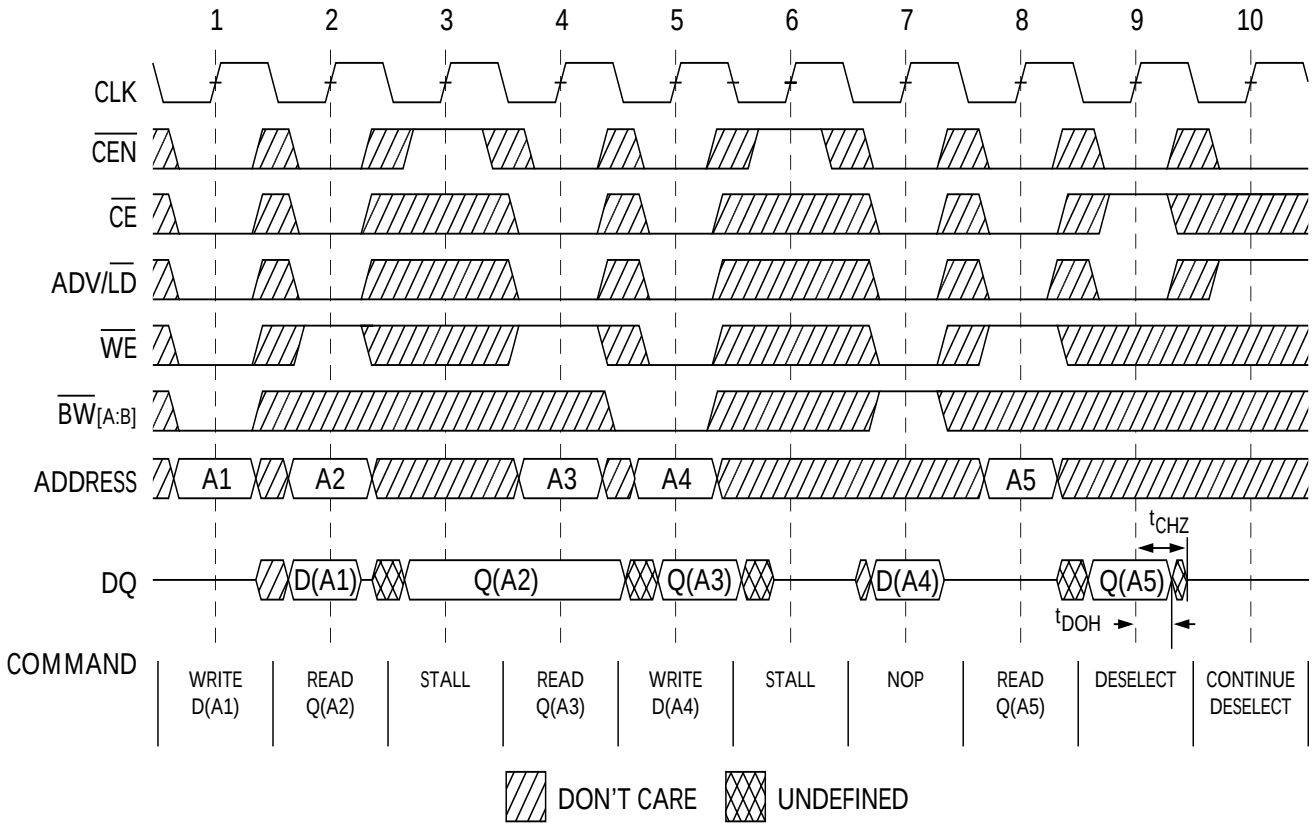


Notes:

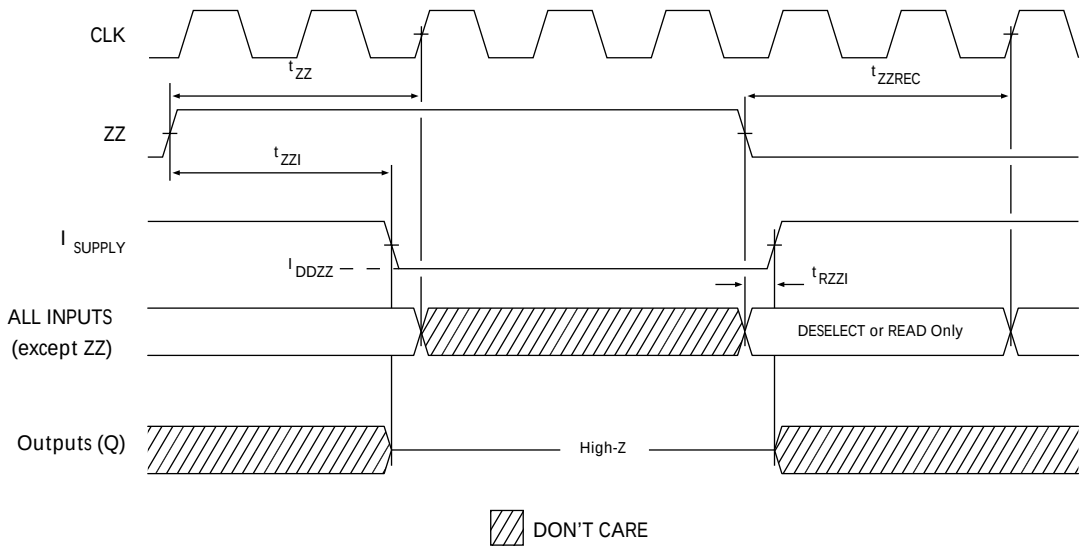
19. For this waveform ZZ is tied low.
20. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
21. Order of the Burst sequence is determined by the status of the MODE (0= Linear, 1= Interleaved). Burst operations are optional.

Switching Waveforms

NOP, STALL and DESELECT Cycles[19, 20, 22]



ZZ Mode Timing[23,24]



Notes:
22.The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrates $\overline{CEN}$ being used to create a pause. A write is not performed during this cycle.
23.Device must be deselected when entering ZZ mode. See truth table for all possible signal conditions to deselect the device.
24.DQs are in high-Z when exiting ZZ sleep mode

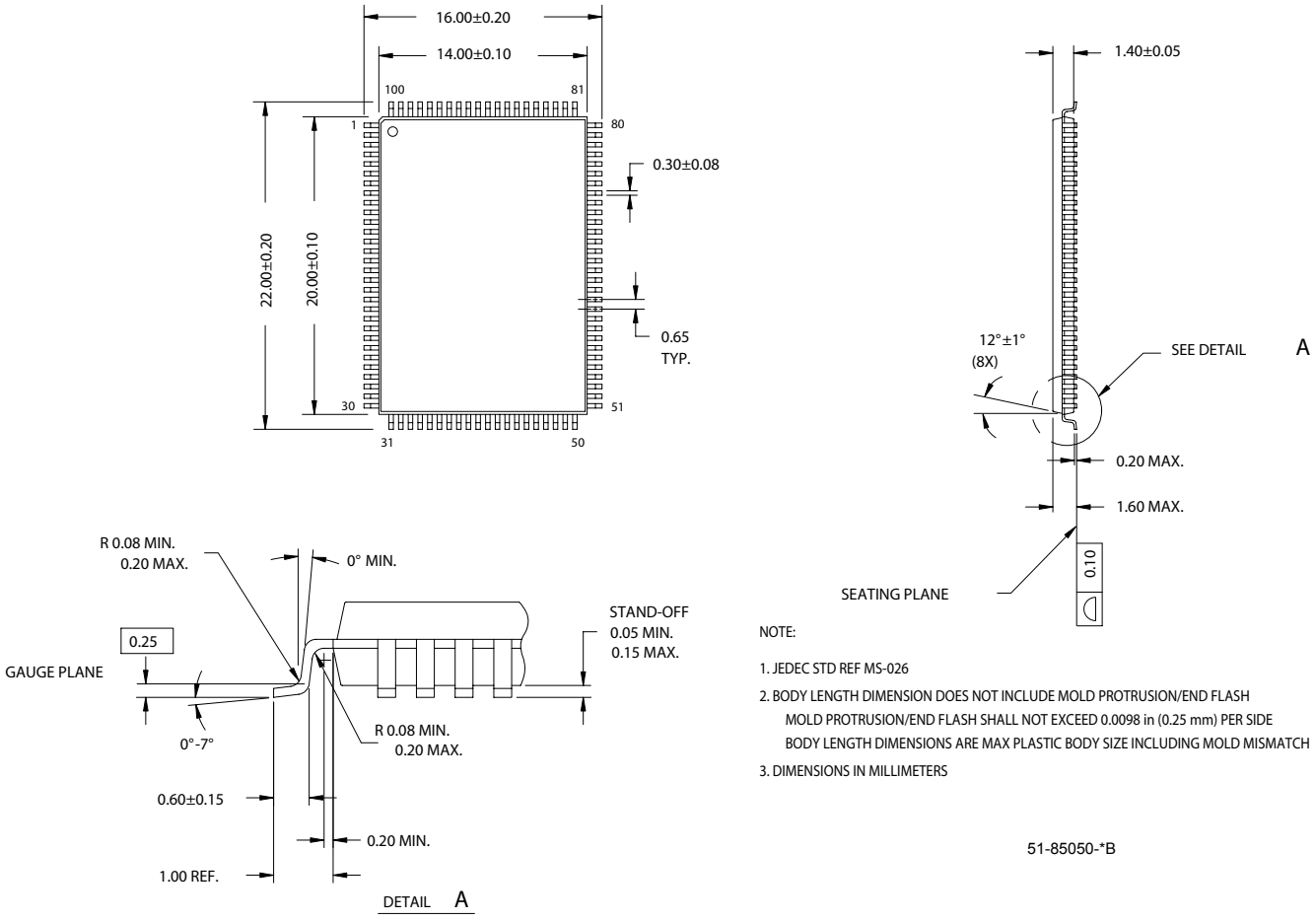
Ordering Information

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1353G-133AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
	CY7C1353G-133AXI			Industrial
100	CY7C1353G-100AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
	CY7C1353G-100AXI			Industrial

Package Diagrams

100-Pin TQFP (14 x 20 x 1.4 mm) (51-85050)



NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050-*B

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Document History Page

Document Title: CY7C1353G 4-Mbit (256K x 18) Flow-through SRAM with NoBL™ Architecture Document Number: 38-05515				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	224363	See ECN	RKF	New data sheet
*A	288431	See ECN	VBL	Deleted 66 MHz Changed TQFP package in Ordering Information section to Pb-free TQFP
*B	333626	See ECN	SYT	Removed 117-MHz speed bin Modified Address Expansion balls in the pinouts for 100 TQFP Packages according to JEDEC standards and updated the Pin Definitions accordingly Modified V_{OL}, V_{OH} test conditions Replaced 'Snooze' with 'Sleep' Replaced TBD's for Θ_{JA} and Θ_{JC} to their respective values on the Thermal Resistance table Updated the Ordering Information by shading and unshading MPNs according to availability
*C	418633	See ECN	RXU	Converted from Preliminary to Final Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Modified test condition from $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$ Modified test condition from $V_{DDQ} < V_{DD}$ to $V_{DDQ} \leq V_{DD}$ Modified "Input Load" to "Input Leakage Current except ZZ and MODE" in the Electrical Characteristics Table Replaced Package Name column with Package Diagram in the Ordering Information table Replaced Package Diagram of 51-85050 from *A to *B Updated the Ordering Information
*D	480124	See ECN	VKN	Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND. Updated the Ordering Information table.
*E	1274724	See ECN	VKN/AESA	Corrected typo in the Ordering Information table