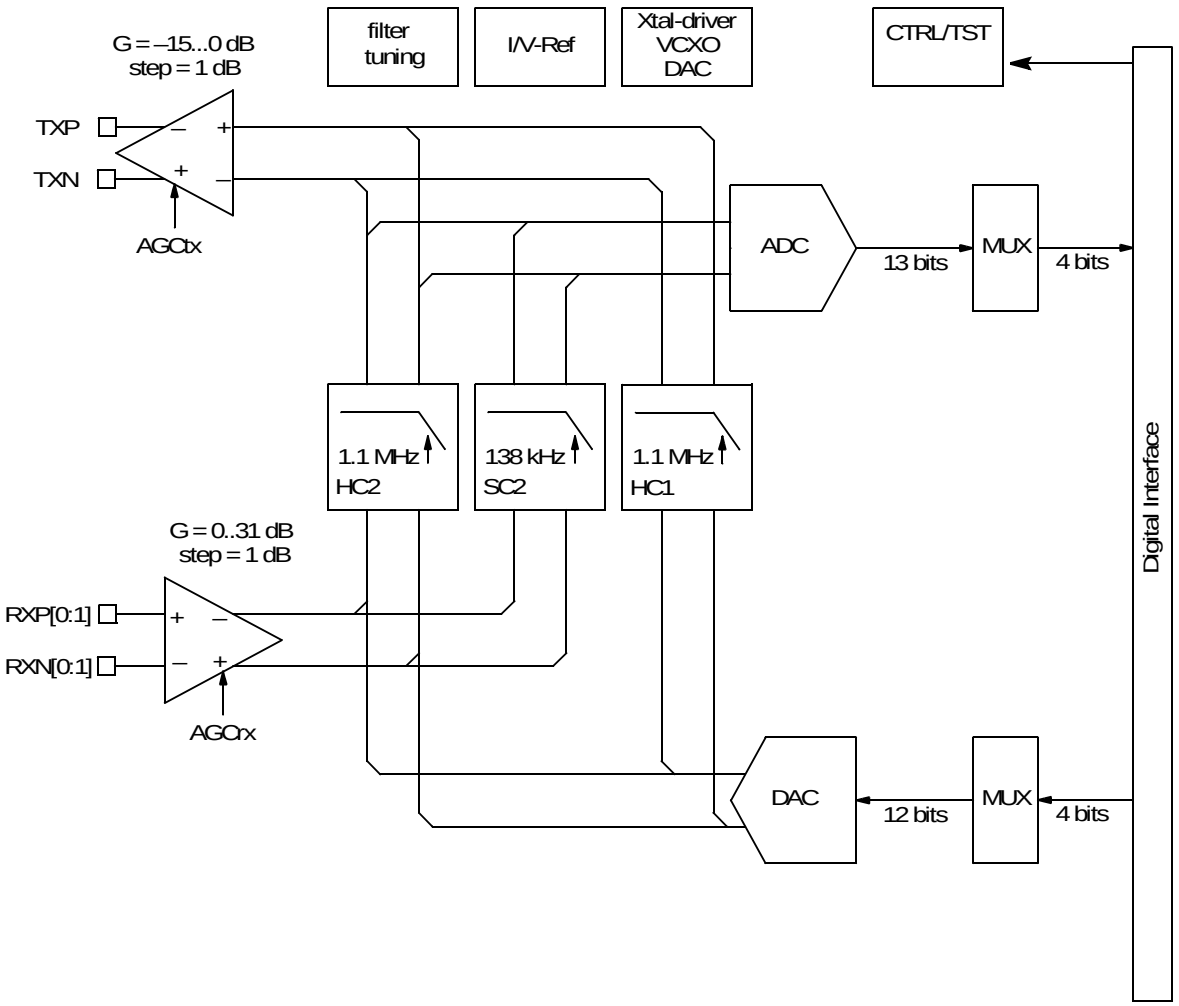
AmDSL134

Integrated ADSL CMOS Analog Front-End Circuit

DISTINCTIVE CHARACTERISTICS

- **Fully-integrated AFE for DMT-ADSL**
- **Proven full rate and lite ADSL solution when used in conjunction with the AmDSL135 device. Complies with ANSI T1.413 Issue 2, ITU G.992.1 (G.dmt), G.992.1 Annex B (ADSL over ISDN), and G.992.2 (G.Lite).**
- **1.1 MHz signal bandwidth**
- **8.8 MS/s 13-bit ADC**
- **8.8 MS/s 12-bit DAC**
- **4-bit digital data interface**
- **1.1 V full-scale input**
- **1.5 V full-scale output**
- **Differential analog I/O**
- **Accurate continuous-time channel filtering**
- **64-pin TQFP package**
- **0.32 Watt (typical) at 3.3 V**
- **3rd and 4th order tunable continuous time LP filters**

BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AmDSL134 device is a third generation Analog Front End (AFE) designed for DMT-based ADSL (Asymmetric Digital Subscriber Line) modems. It includes a 12-bit DAC and a 13-bit ADC. When used with the AmDSL135 DMT/ATM processor, the product supports ANSI T1.413 Issue 2, ITU G.992.1 (G.dmt), G.992.1 Annex B (ADSL over ISDN), and G.992.2 (G.Lite) specification.

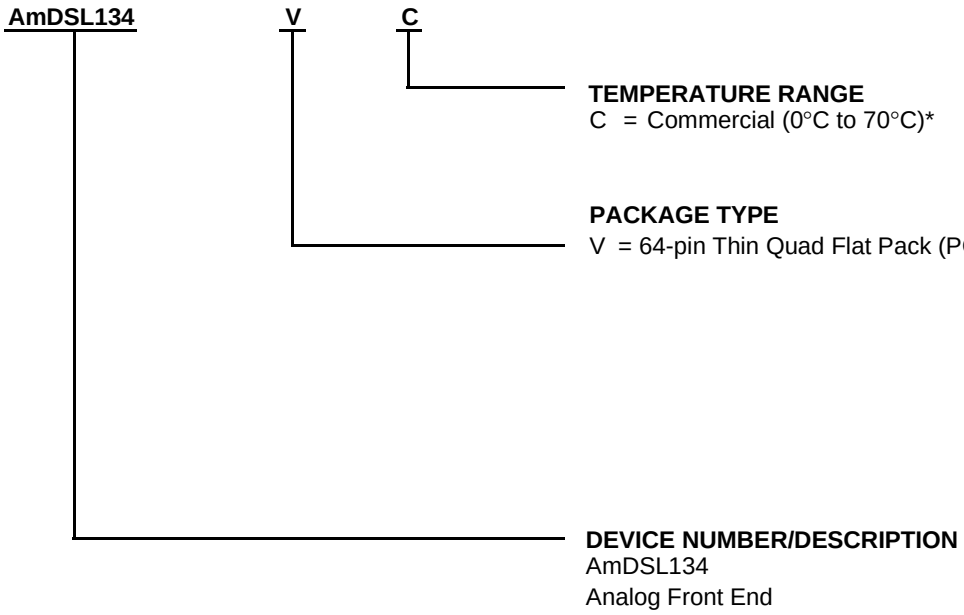
The AmDSL134 device provides programmable low-pass filters for each of the channels and support for automatic gain control. A configuration pin allows the filters to be switched from ATU-R mode to ATU-C mode. The pipeline ADC architecture provides 13-bits of resolution and a signal bandwidth of 1.1 MHz. The device consumes only 0.32 Watt (typical) in full operation and has a Power Down mode for standby. It is housed in a compact 64-pin Thin Plastic Quad Flat Pack.

The AmDSL134 device is electrically and pin-for-pin compatible with the MTC-20134 and the STLC60134.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AmDSL134	VC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

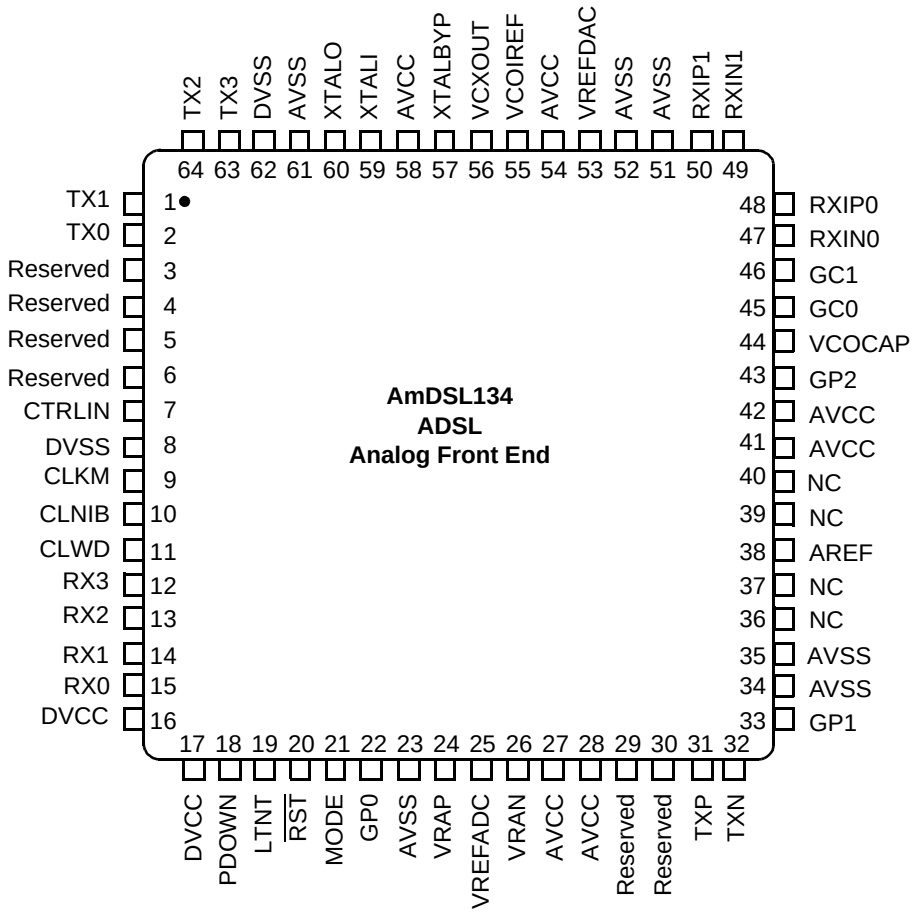
Note:

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

CONNECTION DIAGRAM

Top View

64-Pin TQFP



Notes:

1. *Pin 1 is marked for orientation.*
2. *NC = No Connect. Do not connect anything to this pin.*

Pin Descriptions

Table 1. Pin Description AmDSL134

Pin No.	Pin	Type	Function
Analog Interface			
38	AREF	I	Analog mid supply reference (AVCC/2)
45	GC0	O	External gain control output LSB
46	GC1	O	External gain control output MSB
29	Reserved		Do not connect to anything.
30	Reserved		Do not connect to anything.
47	RXIN0	I	Analog receive negative input Gain 0
49	RXIN1	I	Analog receive negative input Gain 1 (most sensitive input)
48	RXIP0	I	Analog receive positive input Gain 0
50	RXIP1	I	Analog receive positive input Gain 1 (most sensitive input)
32	TXN	O	Pre-driver output
31	TXP	O	Pre-driver output
44	VCOCAP		VCODAC time constant capacitor
55	VCOIREF		Current reference VCO DAC
56	VCXOUT		VXCO control current OUTPUT
26	VRAN		Negative voltage reference ADC
24	VRAP		Positive voltage reference ADC
25	VREFADC		ADC mid supply voltage reference
53	VREFDAC		Current reference TX DAC/DACE
59	XTALI	I	XTAL oscillator input pin
60	XTALO	O	XTAL oscillator output pin. Clock input if crystal is not used.
Digital Interface			
9	CLKM	O	Master clock output, f = 35.328 MHz
10	CLNIB	O	Nibble clock output, f = 17.664 MHz (OSR = 2) or “0” (OSR = 4)
11	CLWD	O	Word clock output, f = 8.832/4.416 MHz
3	Reserved	I	Connect this pin to DVCC.
4	Reserved	I	Connect this pin to DVCC.
5	Reserved	I	Connect this pin to DVCC.
6	Reserved	I	Connect this pin to DVCC.
7	CTRLIN	I	Serial data input (settings)
22	GP0	O	General purpose output 0
33	GP1	O	General purpose output 1
43	GP2	O	General purpose output 2
19	LTNT	I	NT/LT select pin, NT = 0/LT = 1
21	MODE	I	selects between: Normal functional mode: “0” Advanced functional mode: “1”

Table 1. Pin Description AmDSL134 (continued)

Pin No.	Pin	Type	Function
18	PDOWN	I	Power down select, “1” = power down
20	$\overline{\text{RST}}$	I	Reset pin (active Low)
15	RX0	O	Digital receive output, parallel data
14	RX1	O	Digital receive output, parallel data
13	RX2	O	Digital receive output, parallel data
12	RX3	O	Digital receive output, parallel data
2	TX0	I	Digital transmit input, parallel data
1	TX1	I	Digital transmit input, parallel data
64	TX2	I	Digital transmit input, parallel data
63	TX3	I	Digital transmit input, parallel data
57	XTALBYP	I	control to use external oscillator, “1” = bypass
Supply Voltages			
27	AVCC		Analog positive supply voltage
28	AVCC		
41	AVCC		
42	AVCC		
54	AVCC		
58	AVCC		
23	AVSS		Analog VSS
34	AVSS		
35	AVSS		
51	AVSS		
52	AVSS		
61	AVSS		
16	DVCC		Digital positive supply voltage
17	DVCC		
8	DVSS		Digital VSS
62	DVSS		
Test			
36	Reserved		Do not connect to anything.
37	Reserved		Do not connect to anything.
39	Reserved		Do not connect to anything.
40	Reserved		Do not connect to anything.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

Symbol	Parameter Description	Min	Typ	Max	Unit
VCC – VSS	Any AVCC or DVCC supply voltage, related to any AVSS or DVSS	–0.5		4.0	V
VCC – VCC	Any AVCC to DVCC at any time	–0.5		+0.5	V
Vin	Voltage at any input pin	–0.5		VCC + 0.5	V
Tstg	Storage temperature	–60		150	°C
TL	Lead temperature (10 second soldering)			300	°C
Pd	Power dissipation			600	mW
Tj	Junction temperature			150	°C

Operating Ranges

Operating ranges define those limits between which device functionality is guaranteed. Functionality of the device from 0°C to 70°C is guaranteed by production testing. Performance from –40°C to 85°C is guaranteed by characterization and periodic sampling of production units. It is extremely important to note that the voltage difference between AVCC and DVCC must never exceed 0.5 V, even during power supply rampup.

Symbol	Parameter Description	Min	Typ	Max	Unit
AVCC	AVCC supply voltages, related to AVSS	3.0		3.6	V
DVCC	DVCC supply voltages, related to DVSS	3.0		3.6	V
Vin, Vout	Voltage at any input and output pin	0		VCC	V
Ta	Ambient temperature	–40		85	°C

Static Characteristics

Digital Inputs

Schmitt-trigger inputs: TX[3:0], CTRLIN, PDOWN, LTNT, RESETN, MODE

Symbol	Parameter Description	Min	Typ	Max	Unit
VIL	Low level input voltage			0.2 ∗ DVCC	V
VIH	High level input voltage	0.8 ∗ DVCC			V
VH	Hysteresis	1.0		1.3	V
Cinp	Input capacitance			15	pF

Digital Outputs

Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
VOL	Low level output voltage RX[3:0] Clock Driver output: CLKM GP[2:0], GC[1:0]	Iout = 4 mA Iout = 2 mA			0.15 * DVCC	V
VOH	High level output voltage RX[3:0] Clock Driver output: CLKM GP[2:0], GC[1:0]	Iout = –4 mA Iout = –2 mA	0.85 * DVCC			V
Cload	Load capacitance RX[3:0] Clock Driver output: CLKM GP[2:0], GC[1:0]				30	pF
Dcycle	Duty cycle		45		55	%

Power Consumption

Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
PDDPD	Supply power	Power Down mode		100		mW
PDD	Supply power	Running		320		mW

FUNCTIONAL DESCRIPTION

The AmDSL134 chip can be used on the ATU-C side (LT) and on the ATU-R (NT) side (defined by LTNT pin). The selection consists mainly of a filter interchange between the RX and TX path. The filters (with a programmable cutoff frequency) use automatic continuous time tuning. The AmDSL134 device requires few external components, uses a 3.3 V supply, and is packaged in a 64-pin TQFP in order to reduce PCB area. On the digital interface, an alternative mode with lower sampling rate (OSR = 2; 4.4 MS/s) is provided. This allows support of xDSL digital components operating at different frequencies.

The Receiver (RX)

The DMT signal coming from the line to the AmDSL134 is first filtered by the following two external filters:

- POTS HP filter: Attenuation of speech and POTS signaling
- Channel filter: Attenuation of echo signal to improve RX dynamic range

An analog multiplexer allows the selection between two input ports, which can be used to select an attenuated (0, 10 dB for example) version of the signal in case of short loop or large echo. The signal is amplified by a low-noise gain stage (0–31 dB) then low-pass filtered to avoid aliasing and to ease further digital processing by removing unwanted high frequency out-of-band noise. A 13-bit A/D converter samples the data at 8.832 MS/s (a 4.416 MS/s mode is also possible), transforms the signal into a digital representation, and sends it to the DMT signal processor via the digital interface.

The Transmitter (TX/TXE)

The 12 bits of data at 8.832 MS/s (or 4.416 Ms/s) coming from the DMT signal processor through the digital interface are transformed by a D/A converter into an analog signal. This signal is then filtered to decrease the DMT sidelobes and to meet the ANSI transmitter spectral response, but also to reduce the out-of-band noise, which can be echoed to the RX path, to an acceptable level. The pre-driver buffers the signal for the external line driver, and in case of short loop, provide attenuation (–15..0 dB).

The VCXO

The VCXO is divided into two parts: an XTAL driver and an auxiliary 8-bit DAC for timing recovery. The XTAL driver is able to operate at 35.328 MHz. The DAC, which is driven by the CTRLIN pin, provides a current output with 8-bit resolution and can be used to tune the XTAL frequency with the help of external components. A time constant between DAC input and VCXOUT output can be introduced (via the CTRLIN interface) and programmed with the help of an external capacitor (on VCOCAP pin). If a crystal is not used, XTALI should be used as the clock input.

The Digital Interface

The digital interface of the AmDSL134 can be divided into two parts:

1. The data interface converts the multiplexed data from/to the DMT signal processor into valid representation for the TX DAC and RX ADC.
2. The control interface allows the board processor to configure the AmDSL134 paths (RX/TX gains, filter band, ...) or settings (OSR, VCODAC enable, digital/analog loopback, …).

Package

The AmDSL134 device is available in a 64-pin TQFP package.

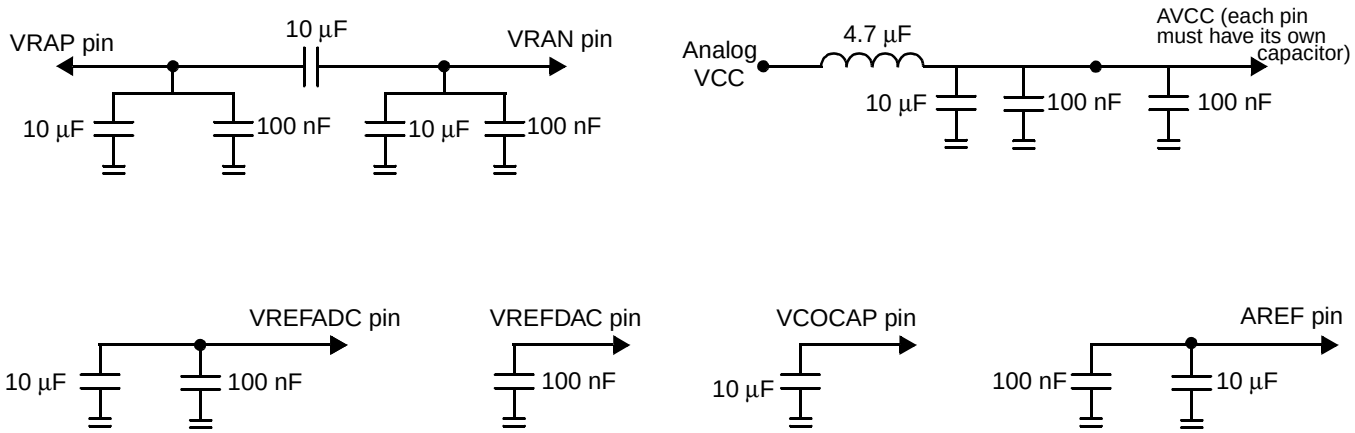


Figure 1. AmDSL134 Grounding and Decoupling Networks

Analog TX/RX Signals

The reference impedance for all power calculations is 100 Ω.

DMT Signal

A DMT signal is basically the sum of N independently QAM modulated signals, each carried over a distinct carrier. The frequency separation of each carrier is 4.3125 kHz, with a total number of 256 carriers (ANSI). For N large, the signal can be modeled by a Gaussian process with a certain amplitude probability density function. Because the maximum amplitude is expected to arise very rarely, the signal is clipped to trade off the resulting SNR loss against ADC/DAC dynamic range. A clipping factor (Vpeak/Vrms = "crest factor") of 5 is used, resulting in a maximum SNR of 75 dB. ADSL DMT signals are nominally sent at –40 dBm/Hz ±3 dB (–3.65 dBm/carrier) with a maximum power of 100 mW for downstream transmitter and 4.5 mW for upstream transmitter.

The minimum SNR+D needed for DMT carrier demodulation is about (3 • N + 20) dB with a minimum of 38 dB, where N is the constellation size of a carrier (in bits).

Table 2. Signal Levels (on the line)

	LT Side		NT Side	
Description	**RX**	**TX**	**RX**	**TX**
Max level	839 mVpdif	15.8 Vpdif	3.95 Vpdif	3.4 Vpdif
Max RMS level	168 Vrms	3.16 Vrms	791 mVrms	671 mVrms
Min level	54 mVpdif	3.95 Vpdif	42 mVpdif	839 mVpdif
Min RMS level	11 mVrms	791 mVrms	8 mVrms	168 mVrms

Table 3. Total Signal Level (on the line)

	LT Side	NT Side
Description	**RX**	**RX**
Max level for receiver	4 Vpdif (long line)	4.2 Vpdif (short line)

ATU_C Side Block Diagram

The transformer at ATU_C-side has a 1:2 ratio. The termination resistors are 12.5 Ω in case of 100 Ω lines. The hybrid bridge resistors should be < 2.5 kΩ for low noise. An HP filter must be used on the TX path to reduce DMT sidelobes and out-of-band noise influence on the receiver. On the RX path, a LP filter must be used in order to reduce the echo signal level and to avoid saturation of the input stage of the receiver. The POTS filter is used in both directions to reduce crosstalk between ADSL signals and POTS speech and signaling.

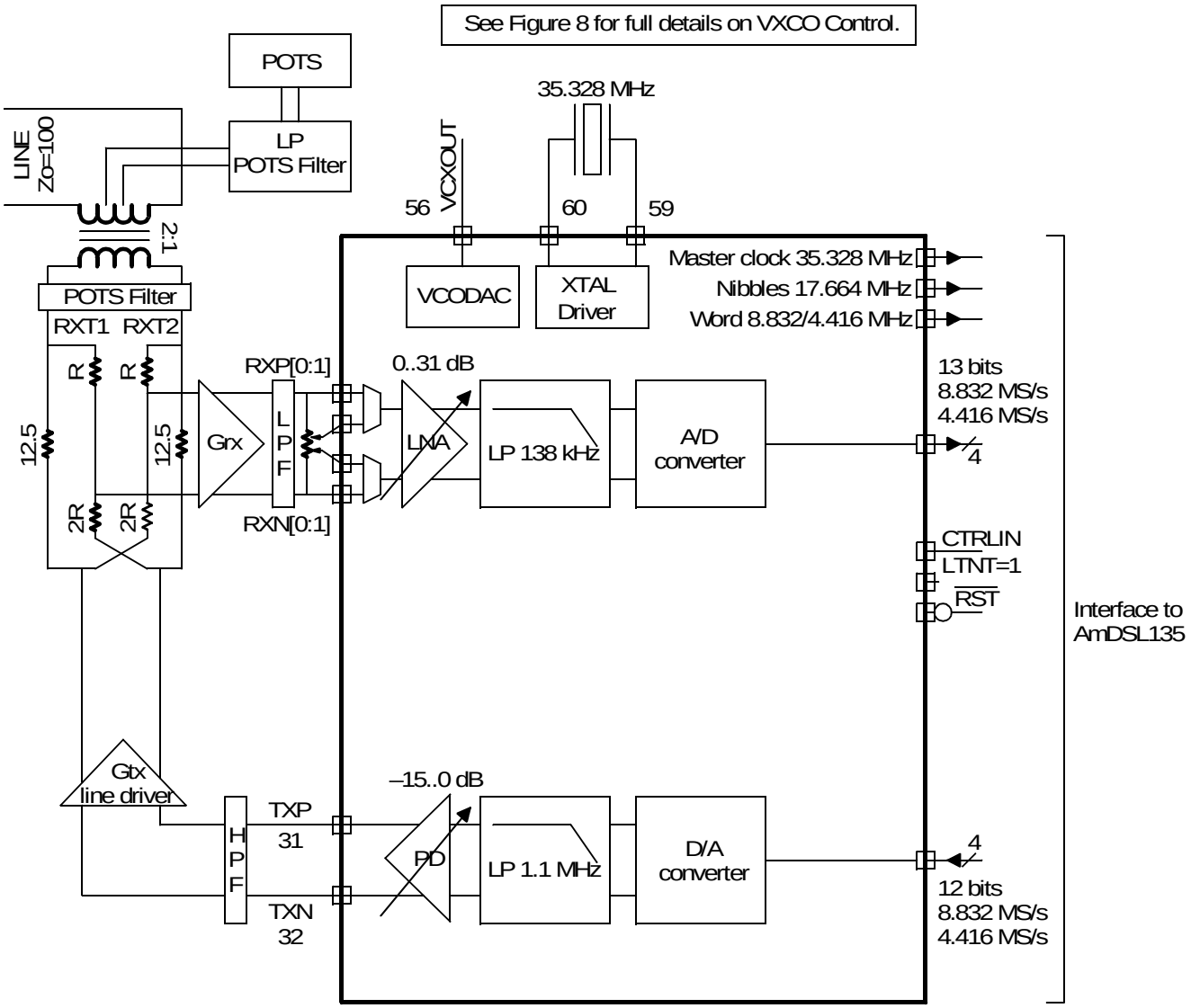


Figure 2. ATU-C AFE Schematic

ATU_R Side Block Diagram

The ATU_R-side block diagram is equal to the ATU_C-side block diagram with the following differences:

- The transformer ratio is 1:1
- Termination resistors are 50 Ω for 100 Ω lines

An LP filter may be used on the TX path to reduce DMT sidelobes and out-of-band noise influence on the receiver. On the RX path, an HP filter must be used in order to reduce the echo signal level and to avoid saturation of the input stage of the receiver. The POTS filter is used in both directions to reduce crosstalk between ADSL signals and POTS speech and signaling.

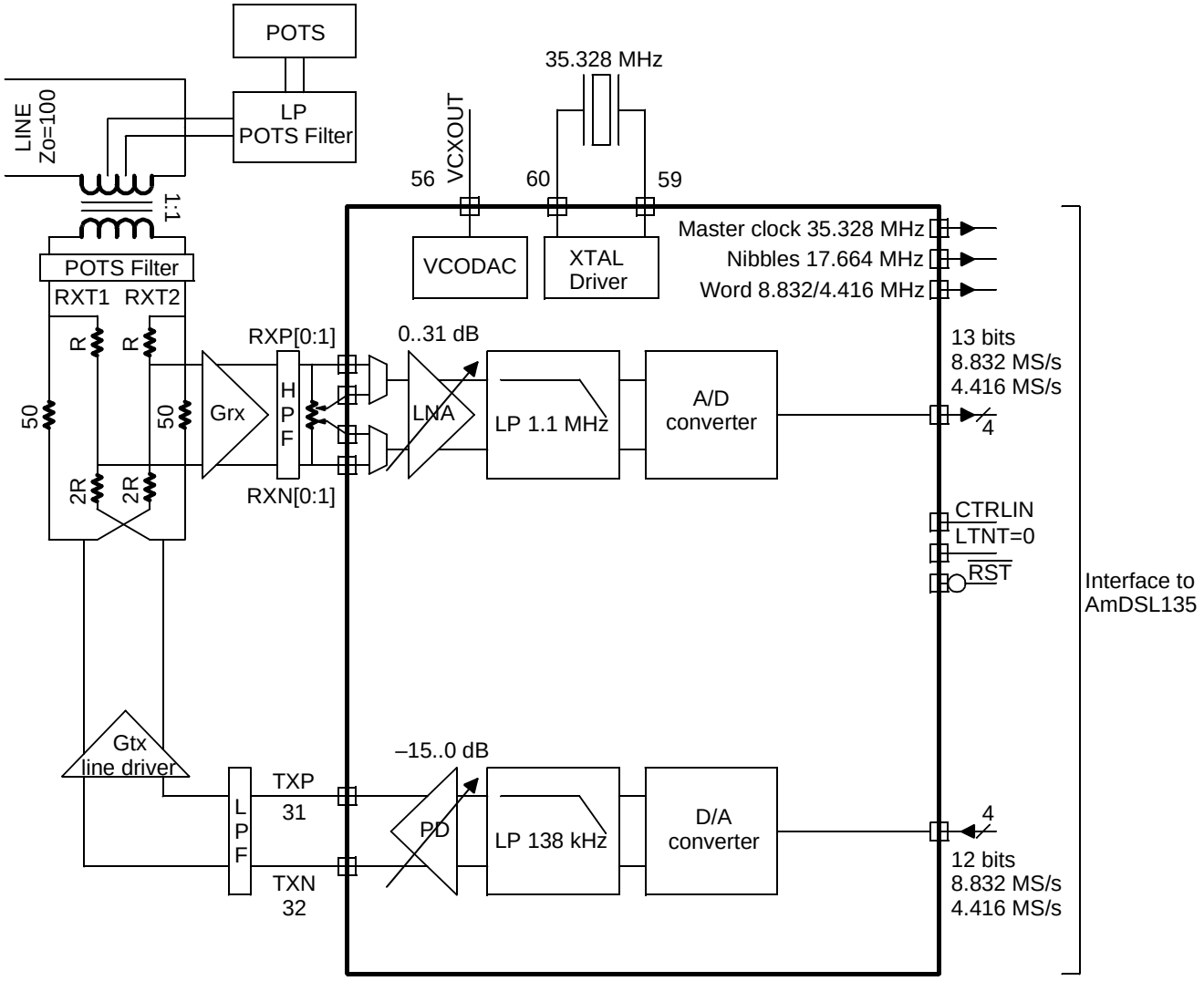


Figure 3. ATU-R AFE Schematics

AmDSL134 Device RX Path

Speech Filter

An external bidirectional LC filter for upstream and downstream POTS service splits out the speech signal to the analog telephone circuit on both the NT and LT sides of the line. The ADSL analog front end integrated circuit does not contain any circuitry for the POTS service, but guarantees that the POTS bandwidth is not disturbed by spurious signals from the ADSL spectrum.

Channel Filters

The purpose of these external analog circuits is to provide partial echo cancellation by an analog filtering of the receive signal for both ATU_R (reception of downstream channel) and ATU_C (reception of upstream channel). This is feasible because the upstream and the downstream data can be modulated on separate carriers (FDM).

RX Common-mode Voltage

Description	Value/Units
Common mode signal VCM at RXIN1 and RXIN2	AVCC/2

Automatic Gain Control of RX Path

The AGC gain in the RX path is controlled through a 5-bits digital code. Four inputs are provided for RX input and the selection is made with the RXMUX bits of the CTRLIN interface. This can be used to make lower gain paths in case of a high input signal. The AGC characteristics are:

Description	Typical Value/Units
Input referred noise (max. gain)	$\frac{20\ \mathrm{nV}}{\sqrt{\mathrm{Hz}}}$
Max. input level	1.1 Vpd
Gain range	0 dB … 31 dB with step = 1 dB
Gain and step accuracy	±0.3 dB

RX Filters

The combination of the external filter with the integrated low-pass filter provides:

- Echo reduction to improve dynamic range
- DMT sidelobe and out-of-band (anti-aliasing) attenuation
- Anti-alias filter (60 dB rejection @ image freq.)

ATU_R-RX Filters

The integrated filter has the following characteristics:

Description	Value/Units
Type	3rd order Butterworth
Frequency band	1.104 MHz (f0)
Frequency tuning	f0/1.4375 -> f0
Max. in-band ripple	2 dB

Phase characteristics:

Description	Value/Units
Total RX filter group delay	< 50 µs @ 138 kHz < f < 1.104 MHz
Total RX filter group delay distortion	< 50 µs @ 138 kHz < f < 1.104 MHz

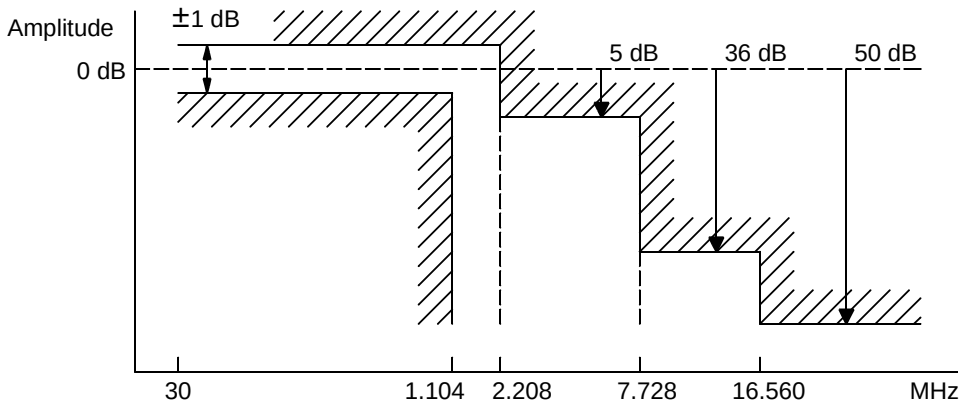


Figure 4. ATU_R-RX Filter Mask

ATU_C-RX Filter

This filter is the same as the one used for ATU_R_TX.

Linearity of RX

Linearity of the RX analog path is defined by the IM3 product of two sinusoidal signals with frequencies f1 and f2 and each with 0.5 Vpd amplitude (i.e., total ≤ 1 Vpd) at the output of the RX-AGC amplifier (i.e., before the ADC) for the case of minimal AGC setting.

Linearity of ATU_R-RX

f1 (0.5 Vpd) f2 (0.5 Vpd)	300 kHz 200 kHz	500 kHz 400 kHz	700 kHz 600 kHz
S/IM3 (AGC = 0 dB)	59.5 dB @ 100 kHz 53.5 dB @ 400 kHz 43.5 dB @ 700 kHz 42.5 dB @ 800 kHz	59.5 dB @ 300 kHz 48.0 dB @ 600 kHz	48.0 dB @ 500 kHz 42.5 dB @ 800 kHz

Linearity of ATU_C-RX

f1 (0.5 Vpd)	80 kHz
f2 (0.5 Vpd)	70 kHz
S/IM3	56.5 dB @ 60 kHz
(AGC = 20 dB)	56.5 dB @ 90 kHz

A/D Converters

A pipeline architecture is used for the A/D converter.

Number of bits:	13 bits
Full scale input range:	1.1 Vpdif ±5% @ 3.3 V
Sampling rate:	8.832 MHz (or 4.416 MHz in alternative mode)
Maximum attenuation at 1.1 MHz:	< 0.5 dB without in-band ripple
Latency:	5 sampling clock periods

AmDSL134 Device TX Path

Transmitter Spectral Response

Figure 5 and Figure 6 show the ANSI spectral response mask for ATU_C and ATU_R transmitters.

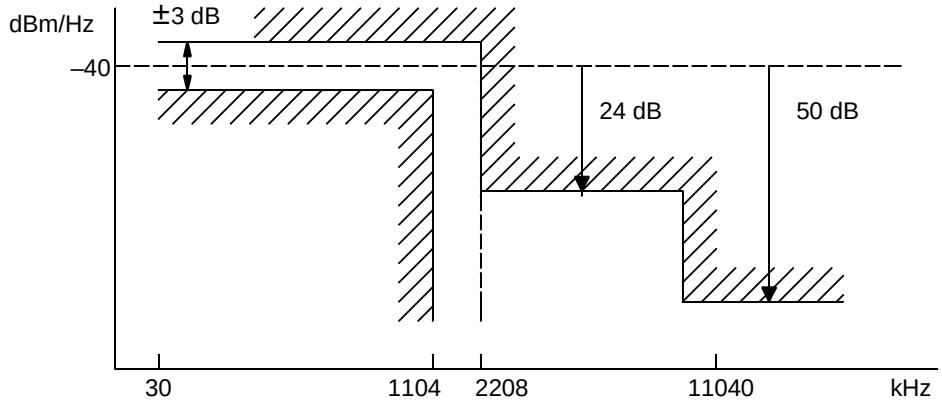


Figure 5. ATU_C PSD Mask

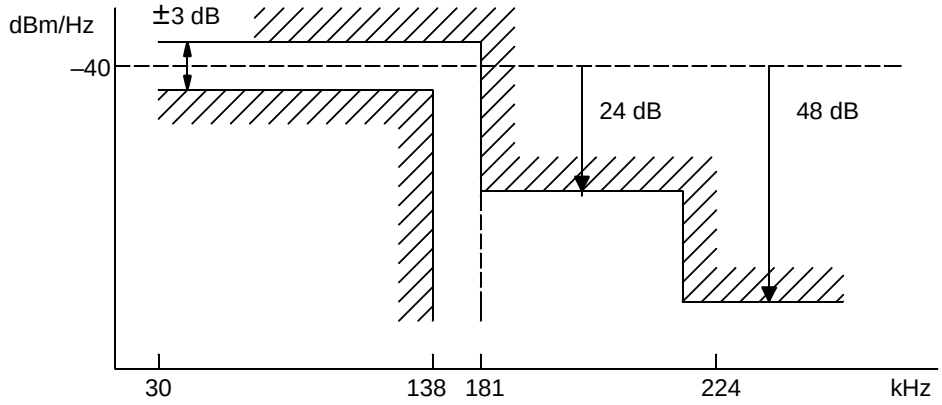


Figure 6. ATU_R PSD Mask

AGC of TX Path (from Filter Output to TXP and TXN)

Description	Value/Units
Input level (nominal)	1.0 Vpd
Output level (nominal)	1.5 Vpd
AGC range (nominal)	–14.5 dB … 0 dB
AGC step (nominal)	1.0 dB
Gain and step accuracy	±0.03 dB
Minimal code (0000) stands for AGC = –14.5 dB and maximal (1111) for AGC = 0 dB.	

TX Pre-driver Capability

The pre-driver drives an external line power amplifier that transmits the required power to the line.

Description	Value/Units	
TX drive level to the external line driver for max AGC setting		1.5 Vpdif
External line driver input impedance	resistive	> 500 Ω
	capacitive	< 30 pF
Pre-driver characteristics		
Closed loop gain	–14.5 dB … 0 dB with step = 1 dB < TBD	
Output offset voltage (0 dB) Input noise voltage (0 dB)	$< \frac{20\ \mathrm{nV}}{\sqrt{\mathrm{Hz}}}$ @ f > 250K	
Output common mode voltage	$< \frac{50\ \mathrm{nV}}{\sqrt{\mathrm{Hz}}}$ @ 34.5K < f < 138K 1.6 V < Vcm < 1.7 V	

TX Filter

The TX filters act not only to suppress the DMT sidebands, but also as smoothing filters on the D/A convertor's output to suppress the image spectrum. For this reason, they are realized in a time-continuous approach.

ATU_C-TX Filter

This is the same filter as ATU_R-RX. Its purpose now is to remove image frequency of the transmitted signal according to the ANSI definition.

ATU_R-TX Filter

The purpose of this filter is to remove out-of-band noise of the ATU_R-TX path echoed to the ATU_R-RX path. In order to meet the transmitter spectral response, any additional filtering is performed digitally. The integrated filter has the following characteristics:

Description	Value/Units
Input referred noise	$\frac{100\ \mathrm{nV}}{\sqrt{\mathrm{Hz}}}$
Max. input level	1 Vpd
Max. output level	1 Vpd
Type	4^{th} order Chebychef
Frequency band	138 kHz (f0)
Frequency tuning	f0/1.25 -> 1.25 • f0
Max. in-band ripple	±1 dB

Phase characteristic:

Description	Value/Units
Total RX filter group delay	< 50 µs @ 34.5 kHz < f < 138 kHz
Total RX filter group delay distortion	< 8 µs @ 34.5 kHz < f < 138 kHz

Note: *The total TX path (including DAC) group delay distortion is 8 µs.*

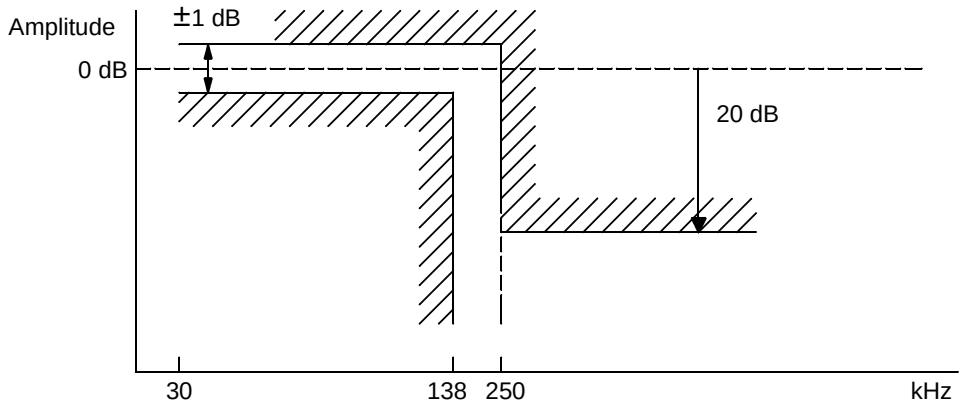


Figure 7. Filter Mask

D/A Convertor

Description	Value/Units
Number of bits	12 bits
Full scale output range	1 Vpdif ±5%
Sampling rate	8.832 MHz (or 4.416 in alternative mode)
Latency	1 sampling clock period

Linearity of ATU_C-TX

Linearity of the TX is defined by the IM3 product of two sinusoidal signals with frequencies f1 and f2 and each with 0.25 Vpd amplitude (–6 dB FS) at the output of the pre-driver for the case of a total AGC = 0 dB.

Linearity of ATU_C-TX

f1 (0.5 Vpd) f2 (0.5 Vpd)	300 kHz 200 kHz	500 kHz 400 kHz	700 kHz 600 kHz
S/IM3 (AGC = 0 dB)	59.5 dB @ 100 kHz 53.5 dB @ 400 kHz 43.5 dB @ 700 kHz 42.5 dB @ 800 kHz	59.5 dB @ 300 kHz 48.0 dB @ 600 kHz	48.0 dB @ 500 kHz 42.5 dB @ 800 kHz

Linearity of ATU_R-TX

f1 (0.5 Vpd) f2 (0.5 Vpd)	80 kHz 70 kHz
S/IM3 (AGC = 0 dB)	59.5 dB (60 kHz/90 kHz)

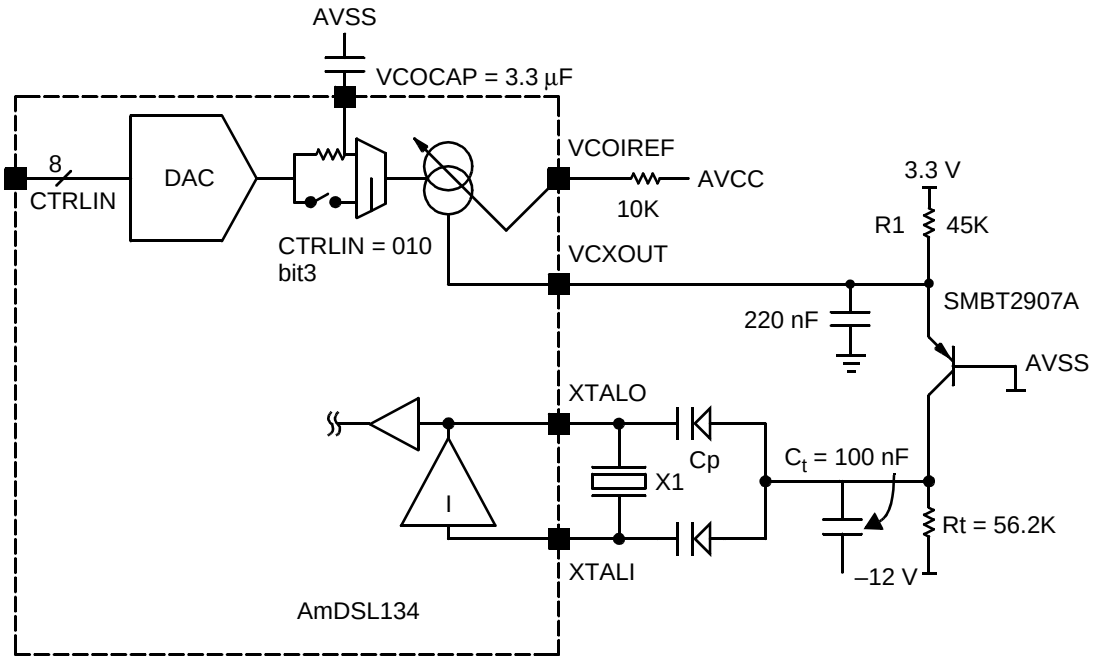
VCXO

A voltage-controlled crystal oscillator driver is integrated in the AmDSL134 device. Its nominal frequency is 35.328 MHz. The quartz crystal is connected between the pins XTAL1 and XTAL2. The principle of the VCXO control is shown in Figure 8. The information coming from the digital processor, via the CTRLIN path, is used to drive an 8-bit I-DAC, which generates a control current. This current is externally converted and filtered to generate the required control voltage for the varicap. The VCXO characteristics are given in Table 4. The tuning is monotonic with 8-bit resolution, with the worst-case tuning step of < 2 ppm/LSB (8-bit). The time constant of the tuning can be selected through an external capacitor Ct.

Table 4. VCXO Characteristics

Parameters	Min	Nominal	Max	Note
Required frequency accuracy	–50 ppm	35.328 MHz	+50 ppm	
Frequency tuning range		±100 ppm		Rref = 16.5 kΩ
VCXO output current		100 µA		AVCC = 3.3 V

N.B.: Frequency tuning range is proportional to the crystal dynamic capacitance Cm.



Note:

R1 and Rt values will depend on crystal and varactors (Cp) used. Values shown apply to BB644 varactors and ECLIPTEX ECX-5171-35.328 MHz crystal.

Figure 8. Principle of VCXO Control

Digital Interface

Mode Interface

The Normal mode is enabled with a low level on the MODE pin and the Advanced mode with a high level. In the Advanced mode, the values of the LTNT and PDOWN pins determine one of the following four available modes:

LTNT	PDOWN	Mode
0	0	Functional control mode
0	1	Reserved
1	0	NandTree test mode
1	1	Reserved

Functional control mode: see control interface

NandTree test mode: In this mode a NandTree for all digital inputs is enabled.

Mode Interface Timing

The value of LTNT and PDOWN pins is sampled with the second master clock edge after a rising edge on MODE pin. These registers are not in the scan chain.

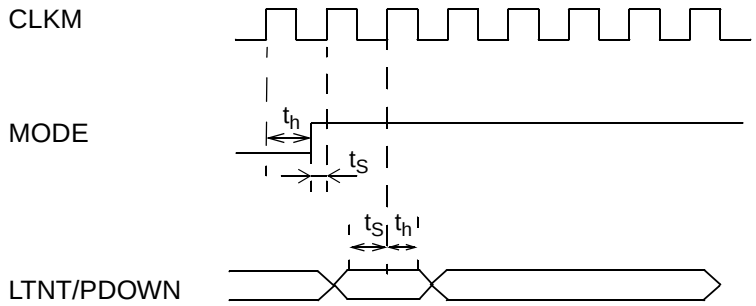


Figure 9. Advanced Mode Timing

Symbol	Parameter	Min	Typ	Max
t_s	Setup time	7 ns		
t_h	Hold time	0 ns		

Control Interface

The digital code setting for the AmDSL134 device configuration is sent over a serial line (CTRLIN) using the word clock (CLWD). The data burst is composed of 16 bits from which the first bit is used as start bit (“0”), the three LSBs (i.e., CTRLIN[2:0]) being used to identify the data contained in the 12 remaining bits.

Normal Mode

In the Normal mode (MODE = “0”), only the settings with data id “0xx” are available. Settings with the data id “1xx” are latched, but they are overruled by the default settings determined by the LTNT and PDOWN pins.

Table 5. Control Interface Bit Mapping

CTRLIN[2:0]	Description	Bit Mapping
“000”	**RX settings**	
	2 bit for external attenuation control (GC1, GC0) reset value = 00b	b[14:13]
	1 bit for RX input selection (“0” = RXIP0/RXIN0 .. “1” = RXIP1/RXIN1) reset value = 0b	b[12]
	5 bits for AGC RX – MSB first (“00000” = 0 dB, “11111” = 31 dB) reset value = 00000b	b[11:7]
	2 bits to force an HC filter selection for RX path used in LT configuration to use an HC filter as RX filter overloaded when test is active (direct selection) “00” & “11” Normal mode “01” HC2 -> RX, AREF -> TX, “10” HC1 -> RX reset value = “00”	b[6:5]
“001”	**TX settings**	
	4 bits for AGC TX – MSB first (“0000” = –15 dB, “1111” = 0 dB) reset value = 0000b	b[14:11]
	reserved reset value = 0000b	b[10:7]
	3 general purpose pins (GP2, GP1, GP0) reset value = 000b	b[6:4]
“010”	**AmDSL134 configuration**	
	1 bit for digital loopback (‘1’ enabled) reset value = 0b	b[14]
	1 bit for analog loopback (‘1’ enabled) reset value = 0b	b[13]
	1 bit for VCO DAC enable (‘1’ enabled) reset value = 1b	b[12]
	Reserved	b[11]
	1 bit for OSR (‘0’ = 4, ‘1’ = 2) reset value = 0b	b[10]
	3 bit for SC1 LPF frequency selection (“111” = 138 kHz = f0, “011” = f0/1.25, “100” = 1.23 ∗ f0) reset value = 111b	b[9:7]
	3 bit for HC1 and HC2 frequency selection (“100” = 1.104 MHz = f0, “011” = f0/1.4375) reset value = 100b	b[6:4]
	1 bit for filtered VCXO output (‘1’ = filtered, ‘0’ = not filtered) reset value = 0b	b[3]
“011”	**VCO DAC value settings**	
	8 bits for VCO DAC current (“0..0” = Min, “1..1” = Max current) reset value = 1000_000b	b[14:7]

Functional Control Mode

In the functional control mode (MODE = “1”, LTNT = “0”, PDWON = “0”), the default settings are overruled by the following registers via the CTRLIN path. After reset, these registers are initialized with values used for the default configuration.

CTRLIN[2:0]	Description	Bit Mapping
“100”	**Power Down States**	
	12 bits for analog power down, each bit controls one block: TXD (b14), ADC(b12), HC2(b11), HC1(b10), SC2(b9), LNA(b7), DAC(b6), VCODAC(b4), XTAL (b3) reset value = 0000_0000_0000b	b[14:3]
“101”	Filter control “A”	
	reserved - always write “0000” reset value = 0000b	b[14:11]
	reserved - always write “0” reset value = 0b	b[10]
	reserved - always write “0” reset value = 0b	b[9]
	2 bits for SC2 input selection: DAC (“00”), LNA (“10”), AREF (“11”) reset value = 00b	b[8:7]
“110”	Filter control “B”	
	2 bits for HC1 input selection: LNA (“01”), AREF (“11”) reset value = 00b	b[14:13]
	2 bits for HC2 input selection: DAC (“00”), LNA (“01”), AREF (“11”) reset value = 00b	b[12:11]
	2 bits for ADC input selection: SC2 (“00”), HC2 (“01”), HC1 (“10”) reset value = 00b	b[10:9]
	2 bits for reserved - always write “00” reset value = 00b	b[8:7]
	2 bits for TX input selection: HC2 (“00”), SC2 (“01”), AREF (“11”) reset value = 00b	b[6:5]
	reserved - always write “0”	b[4]
“111”	Not used. Reserved for future functionality.	b[14:0]

Control Interface Timing

A burst of data is defined by a low bit (b[15]) followed by at least 16 high bits and followed by 15 bits, split up into 12 data (b[14:3]) and 3 control (b[2:0]) bits. The 3 control bits are known as the 'data id' and determine the target for which the data is intended. The incoming stream is sampled on the rising edge of the master clock CLKM while the word clock CLWD is high.

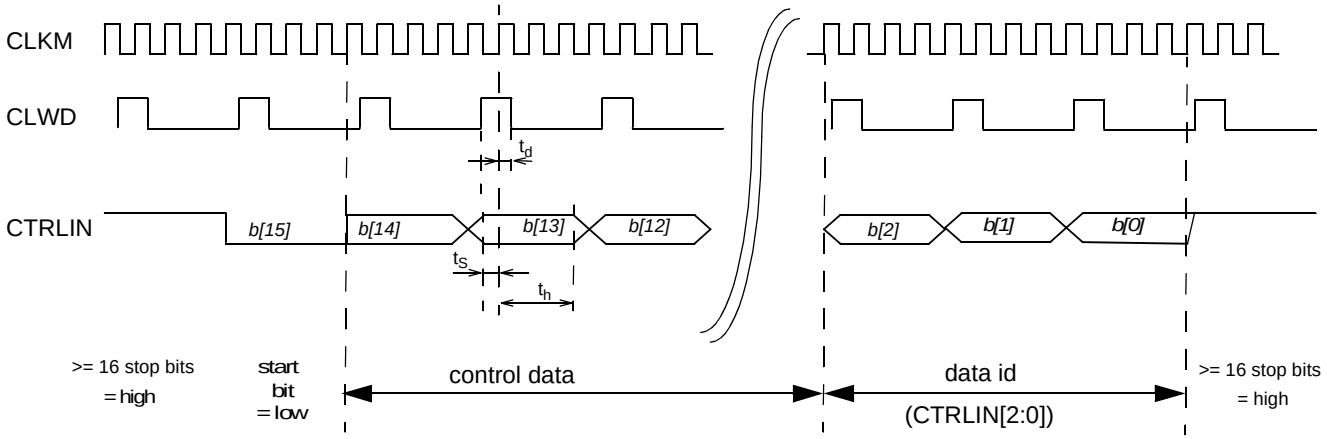


Figure 10. Control Interface Timing

Symbol	Parameter	Min	Typ	Max
t_s	Setup time	8 ns		
t_h	Hold time	0 ns		
t_d	Delay time	2 ns		8 ns

Receive/Transmit Interface

Receive/Transmit Protocol

The digital interface is based on a 4 ∗ 8.832 MHz (35.328 MHz) clock. The 8.832 MHz 13 bits ADC output signal or DAC input signal are SIPO multiplexed over 4 parallel 35.328 MHz data lines in the following table. If OSR = 2 bit is selected, CLNIB is used as nibble clock (17.664 MHz, disabled in Normal speed mode), and all the RX[3:0], TX[3:0], CLWD periods are twice as long as in Normal speed mode. This ensures a backward compatibility with lower frequency digital chips.

	N0	N1	N2	N3
RX0/TX0 will contain	b0	b4	b8	b12
RX1/TX1 will contain	b1	b5	b9	b13
RX2/TX2 will contain	b2	b6	b10	b14
RX3/TX3 will contain	b3	b7	b11	b15

TX Signal Format

The format of the signal for both DACs is 12 bits extracted from the available signed 16-bit two's complement representation coming from the digital processor. The maximum positive number is $2^{14} – 1$, the most negative number is $–2^{14}$, and the 3 LSBs are ignored. Any signal exceeding these limits is clamped to the maximum or minimum value depending on the two sign bits b[15:14].

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
sign	sign	tx_b10	tx_b9	tx_b8	tx_b7	tx_b6	tx_b5	tx_b4	tx_b3	tx_b2	tx_b1	tx_b0	n.u.	n.u.	n.u.

Figure 11. TX Bit Map

RX Signal Format

The resolution of the signal from the ADC is limited to 13 bits. Those bits are converted to a two's complement representation with a maximal positive number of $2^{14} – 1$ and a most negative number of $–2^{14}$. The 2 LSBs are filled with '0'.

Receive/Transmit Interface Timing

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
sign	sign	rx_b11	rx_b10	rx_b9	rx_b8	rx_b7	rx_b6	rx_b5	rx_b4	rx_b3	rx_b2	rx_b1	rx_b0	0	0

Figure 12. RX Bit Map

The data on interface RX[3:0], TX[3:0] are represented in 16 bit format, and transferred in groups of 4 bits (nibbles). The LSBs are transferred first. The AmDSL134 generates a nibble clock (CLKM in OSR = 4 mode {Normal speed mode}, CLNIB in OSR = 2 mode) and a word clock (CLWD) shared by the two directions of the interface. Data are transmitted (RX[3:0]) and sampled (TX[3:0]) on the rising edge of the master clock CLKM (when CLNIB is low for OSR = 2 mode).

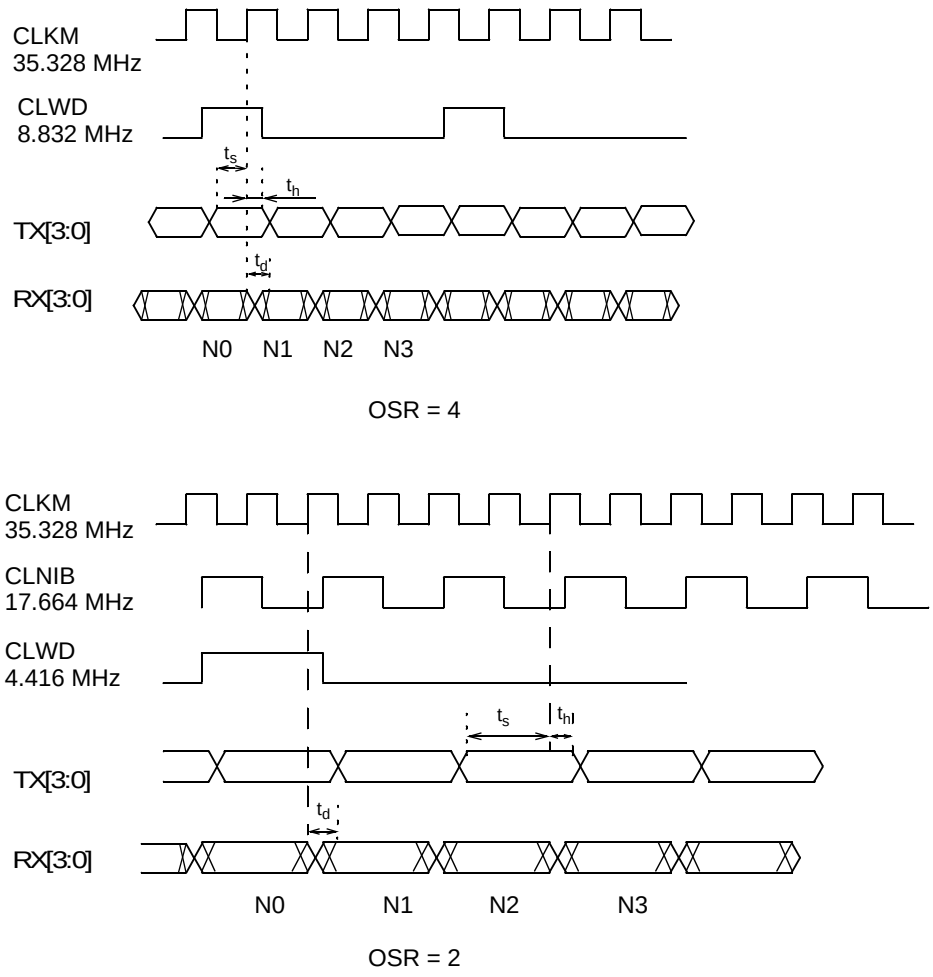


Figure 13. TX/RX Digital Interface Timing

Symbol	Parameter	Min	Typ	Max
t_s	Setup time	8 ns		
t_h	Hold time	0 ns		
t_d	Delay time	2 ns		8 ns

Power Down

When pin PDOWN = “1”, the chip is set in Power Down mode. In this mode, all analog functional blocks are deactivated, except preamplifier (TX), clock circuits for output clock CLKM. PDOWN does not affect the digital part of the chip. The chip is activated when PDOWN = “0”.

Power Down Conditions

In Power Down mode, the following conditions hold:

- Output voltages at TX01/TX02 = AREF.
- The XTAL output clock on pin CLKM keeps running.
- All digital settings are retained.
- Digital output on pins RX[3:0] are don’t care (not floating).

The following external conditions are added:

- Clock pin CLWD is running.
- CTRLIN signals can still be allowed.
- AREF remains at AVCC/2 (circuit is powered up).
- Input signals at TX[3:0] inputs are not strobed.

Reset Function

The reset function is implied when the $\overline{RST}$ pin is at a low voltage input level. In this condition, the reset function can be easily used for power-up reset conditions.

Detailed Description

During reset:

- All clock outputs are deactivated and set to logical “1” (except for the XTALO and masterclock CLKM).

After reset:

- OSR = 4
- All analog gains (RX, TX) are set to minimum value.
- Nominal filter frequency bands (138 kHz, 1.104 MHz)
- LNA input = “11” (max attenuation)
- VCODAC disabled
- Depending on the LTNT pin value, the following configuration is chosen:

Digital outputs are placed in don’t care condition (non-floating).

‘0’ (NT)
RX: LNA -> HC2 -> ADC TX: DAC -> SC2 -> TX
‘1’ (LT)
RX: LNA -> SC2 -> ADC TX: DAC -> HC2 -> TX

PHYSICAL DIMENSION

PQT 064