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Errata (Date Codes Before 9836)

- High Current Consumption at High V_{CC}
- Leakage Current on Tri-stated I/O Pins
- 32 kHz Oscillator

16. Releasing Reset Condition without Clock

If an external reset or a watchdog reset occurs while the clock is stopped and reset is released before the clock is restarted, the internal reset will time-out after the start-up delay which is independent of the external clock. If no external clock pulses are present in the period when internal reset is active, the reset does correctly cause tri-stating of the I/O while the reset is held. However, if the internal reset is released before the clock starts running, the part does not clear I/O registers, nor set PC to 0x00. Here, stopping the clock refers to gating the external clock input. Power-down or Power-save modes do not have this issue.

Problem Fix/Workaround

Make sure the clock is running whenever an external reset can be expected. If the Watchdog is used, never stop an external clock.

15. Incorrect Channel Changes in Free Running Mode

If the ADC operates in Free Running Mode and channels are changed by writing to ADMUX shortly after the ADC Interrupt Flag (ADIF in ADCSR) is set, the new setting in ADMUX may affect the ongoing conversion.

Problem Fix/Workaround

Use Single Conversion Mode when scanning channels, or avoid changing ADMUX until at least 0.5 ADC clock cycles after ADIF goes high.

14. 32 kHz Oscillator May Fail at Higher Voltages

When using an external 32 kHz crystal as asynchronous clock source for Timer2, the timer may fail at voltages above 4.0V.

Problem Fix/Workaround

Keep the supply voltage below 4.0V when clocking Timer2 from an external crystal.

8-bit AVR® Microcontroller with 8K Bytes In-System Programmable Flash

AT90S/LS8535 Rev. D Errata Sheet

Rev. 1196E–09/01

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13. Incorrect Start-up Time

When the FSTRT fuse is programmed, the start-up time from reset may still be 16 ms instead of 1 ms.

Problem Fix/Workaround

Leave the FSTRT fuse unprogrammed and design the system to allow a start-up time of 16 ms.

Use rev. E or later.

12. Lock Bits at High V_{CC} and Temperature

On some devices, the lock bits will not erase at high V_{CC} and temperature. In this situation, it will not be possible to reprogram the devices when the lock bits are set.

Problem Fix/Workaround

Lower V_{CC} below 4.0V at room temperature before performing a chip-erase. Then the device will unlock, and it will be possible to reprogram the device at any V_{CC}.

11. Error in Half Carry Flag

The half carry flag is undefined after executing the commands “ror”, “asr” and “lsr”.

Problem Fix/Workaround

Do not use the half carry flag value after executing the above instructions.

10. Error in Writing Reset Status Bits

The EXTRF flag in MCUSR will be cleared when clearing the PORF flag. The flag does not get cleared by writing a “0” to it.

Problem Fix/Workaround

Finish the test of both flags before clearing any of them. Clear both flags simultaneously by writing “0” to both PORF and EXTRF in MCUCR.

9. Wake-up from Sleep Executes Instructions before the Interrupt is Serviced

When waking up from Power-save, some instructions are executed before the interrupt is called. If the device is woken up by an external interrupt, 2 instruction cycles are executed. If it is woken up by the asynchronous timer, 3 instructions are executed before the interrupt.

Problem Fix/Workaround

Make sure that the first 2 or 3 instructions following sleep are not dependent on the executed interrupt.

8. The SPI Can Send Wrong Byte

If the SPI is in Master mode, it will restart the old transfer if new data is written on the same clock edge as the previous transfer is finished.

Problem Fix/Workaround

When writing to the SPI, first wait until it is ready, then write the byte to transmit.

7. Output Compare Output Value Corrupted by Writing to Port

When writing to the PORTD I/O location, the OC1A and OC1B output compare values will assume the values written to bits 5 and 4, respectively. This means that even when writing to another bit in the same port register (such as a read-modify-write to another pin in the same port), the output compare values will be affected. Effectively, if the output compare function is used, the other pins in the same port cannot be changed, unless the intention is to write the output compare values simultaneously.

Problem Fix/Workaround

Avoid updating the other port bits when using the output compare function.

Use rev. E or later.

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6. Serial Programming at Voltages below 3.0V

At voltages below 3.0V, serial programming might fail.

Problem Fix/Workaround

Keep V_{CC} at 3.0V or higher during In-System Programming.

5. Wake-up from Power-save without Global Interrupt Enabled

When an asynchronous timer interrupt is used to wake up the part from Power-save, the part will wake up even if global interrupts are disabled.

Problem Fix/Workaround

No workaround necessary.

4. UART Loses Synchronization if RXD Line is Low when UART Receive is Disabled

The UART will detect a UART start bit and start reception even if the UART is not enabled. If this occurs, the first byte after reenabling the UART will be corrupted.

Problem Fix/Workaround

Make sure that the RX line is high at start-up and when the UART is disabled. An external RS232-level converter keeps the line high during start-up.

In Addition to the Above, this Errata Applies for Devices with Date Code Marking before 9836.

3. High Current Consumption at High V_{CC}

Some of the early samples have higher current consumption than specified. The current consumption in Power-down/Power-save mode is 100 to 500 µA at 6V, rather than the specified 50 µA. The current consumption increases exponentially with supply voltage, and is strongly varying from sample to sample.

Problem Fix/Workaround

Use devices with date codes later than 9836.

2. Leakage Current on Tri-stated I/O Pins

On some of the early samples tri-stated I/O pins may source up to 20 µA and sink up to 6 µA at 6V supply voltage. This means that input pins will effectively have an input impedance of down to 300 kΩ. This may cause an unfortunate input offset voltage, particularly noticeable for the ADC and analog comparator pins.

Problem Fix/Workaround

Drivers for the analog and digital input signals to the MCU must be designed to drive a load of 300 kΩ per pin or use devices with date codes later than 9836.

1. 32 kHz Oscillator

On some of the early samples, the 32 kHz oscillator does not start at high voltages. This is dependent on the leakage current on the PC6 (TOSC1) pin, which can be up to 20 µA.

The higher the leakage current, the lower the failure voltage for the oscillator. A failing oscillator may in some cases be kickstarted with an external capacitance.

Problem Fix/Workaround

Lower the operating voltage below 4.0V or use devices with a date codes later than 9836.

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