

**ADSP-21161N**
**SUMMARY**

**High Performance 32-Bit DSP—Applications in Audio, Medical, Military, Wireless Communications, Graphics, Imaging, Motor-Control, and Telephony**  
**Super Harvard Architecture—Four Independent Buses for Dual Data Fetch, Instruction Fetch, and Nonintrusive, Zero-Overhead I/O**

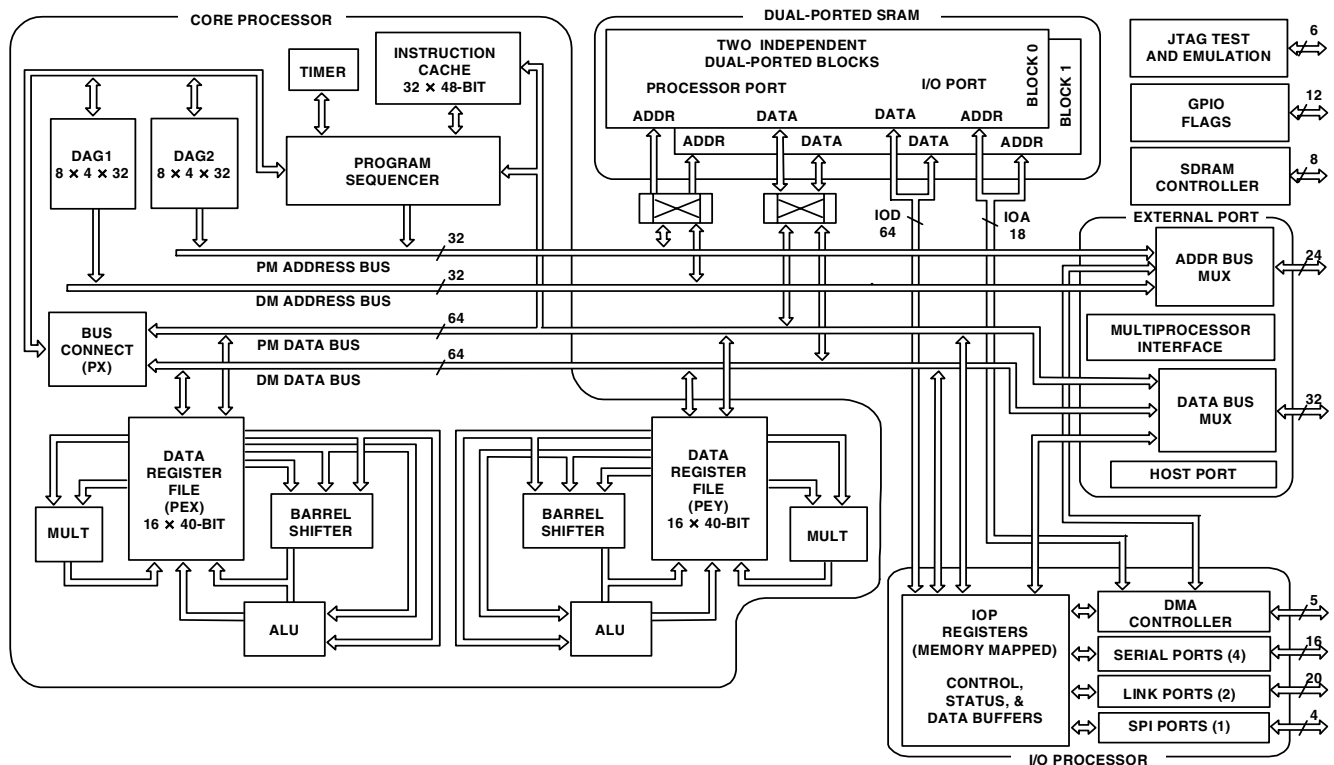
**Code Compatible with All Other SHARC Family DSPs**  
**Single-Instruction-Multiple-Data (SIMD) Computational Architecture—Two 32-Bit IEEE Floating-Point Computation Units, Each with a Multiplier, ALU, Shifter, and Register File**

**Serial Ports Offer I<sup>2</sup>S Support Via 8 Programmable and Simultaneous Receive or Transmit Pins, which Support up to 16 Transmit or 16 Receive Channels of Audio**

**Integrated Peripherals—Integrated I/O Processor, 1M Bit On-Chip Dual-Ported SRAM, SDRAM Controller, Glueless Multiprocessing Features, and I/O Ports (Serial, Link, External Bus, SPI, and JTAG)**  
**ADSP-21161N Supports 32-Bit Fixed, 32-Bit Float, and 40-Bit Floating-Point Formats**

**KEY FEATURES**

**100 MHz (10 ns) Core Instruction Rate**  
**Single-Cycle Instruction Execution, Including SIMD Operations in Both Computational Units**  
**600 MFLOPs Peak and 400 MFLOPs Sustained Performance**  
**225-Ball 17 mm × 17 mm MBGA Package**

**FUNCTIONAL BLOCK DIAGRAM**


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# ADSP-21161N

## KEY FEATURES (continued)

- 1 M Bit On-Chip Dual-Ported SRAM (0.5 M Bit Block 0, 0.5 M Bit Block 1) for Independent Access by Core Processor and DMA
- 200 Million Fixed-Point MACs Sustained Performance
- Dual Data Address Generators (DAGs) with Modulo and Bit-Reverse Addressing
- Zero-Overhead Looping with Single-Cycle Loop Setup, Providing Efficient Program Sequencing
- IEEE 1149.1 JTAG Standard Test Access Port and On-Chip Emulation
- Single Instruction Multiple Data (SIMD) Architecture Provides:
  - Two Computational Processing Elements
  - Concurrent Execution—Each Processing Element Executes the Same Instruction, but Operates on Different Data
  - Code Compatibility—At Assembly Level, Uses the Same Instruction Set as Other SHARC DSPs
- Parallelism in Buses and Computational Units Enables:
  - Single-Cycle Execution (with or without SIMD) of: a Multiply Operation, an ALU Operation, a Dual Memory Read or Write, and an Instruction Fetch
  - Transfers Between Memory and Core at Up to Four 32-Bit Floating- or Fixed-Point Words Per Cycle, Sustained 1.6 Gbytes/s Bandwidth
  - Accelerated FFT Butterfly Computation through a Multiply with Add and Subtract
- DMA Controller Supports:
  - 14 Zero-Overhead DMA Channels for Transfers between ADSP-21161N Internal Memory and External Memory, External Peripherals, Host Processor, Serial Ports, Link Ports, or Serial Peripheral Interface (SPI- Compatible)
  - 64-Bit Background DMA Transfers at Core Clock Speed, in Parallel with Full-Speed Processor Execution
  - 800 M Bytes/s Transfer Rate over IOP Bus
  - Host Processor Interface to 8-, 16-, and 32-Bit Microprocessors; the Host Can Directly Read/Write ADSP-21161N IOP Registers
- 32-Bit (or up to 48-Bit) Wide Synchronous External Port Provides:
  - Glueless Connection to Asynchronous, SBSRAM and SDRAM External Memories
  - Memory Interface Supports Programmable Wait State Generation and Wait Mode for Off-Chip Memory
  - Up to 50 MHz Operation for Non-SDRAM Accesses
  - 1:2, 1:3, 1:4, 1:6, 1:8 Clock into Core Clock Frequency Multiply Ratios
  - 24-Bit Address, 32-Bit Data Bus. 16 Additional Data Lines via Multiplexed Link Port Data Pins Allow Complete 48-Bit Wide Data Bus for Single-Cycle External Instruction Execution
  - Direct Reads and Writes of IOP Registers from Host or Other 21161N DSPs
  - 62.7 Mega-Word Address Range for Off-Chip SRAM and SBSRAM Memories

- 32-48, 16-48, 8-48 Execution Packing for Executing Instruction Directly from 32-Bit, 16-Bit, or 8-Bit Wide External Memories
- 32-48, 16-48, 8-48, 32-32/64, 16-32/64, 8-32/64, Data Packing for DMA Transfers Directly from 32-Bit, 16-Bit, or 8-Bit Wide External Memories to and from Internal 32-, 48-, or 64-Bit Internal Memory
- Can be Configured to have 48-Bit Wide External Data Bus, if Link Ports are not Used. The Link Port Data Lines are Multiplexed with the Data Lines D0 to D15 and are Enabled through Control Bits in SYSCON
- SDRAM Controller for Glueless Interface to Low Cost External Memory
  - Zero Wait State, 100 MHz Operation for Most Accesses
  - Extended External Memory Banks (64 M Words) for SDRAM Accesses
  - Page Sizes up to 2048 Words
  - An SDRAM Controller Supports SDRAM in Any and All Memory Banks
  - Support for Interface to Run at Core Clock and Half the Core Clock Frequency
  - Support for 16 M Bits, 64 M Bits, 128 M Bits, and 256 M Bits with SDRAM Data Bus Configurations of  $\times 4$ ,  $\times 8$ ,  $\times 16$ , and  $\times 32$
  - 254 Mega-Word Address Range for Off-Chip SDRAM Memory
- Multiprocessing Support Provides:
  - Glueless Connection for Scalable DSP Multiprocessing Architecture
  - Distributed On-Chip Bus Arbitration for Parallel Bus Connect of Up to Six ADSP-21161Ns, Global Memory, and a Host
  - Two 8-Bit Wide Link Ports for Point-to-Point Connectivity Between ADSP-21161Ns
  - 400 M Bytes/s Transfer Rate over Parallel Bus
  - 200 M Bytes/s Transfer Rate Over Link Ports
- Serial Ports Provide:
  - Four 50 M Bit/s Synchronous Serial Ports with Companding Hardware
  - 8 Bidirectional Serial Data Pins, Configurable as Either a Transmitter or Receiver
  - I<sup>2</sup>S Support, Programmable Direction for 8 Simultaneous Receive and Transmit Channels, or Up to Either 16 Transmit Channels or 16 Receive Channels
  - 128 Channel TDM Support for T1 and E1 Interfaces
  - Companding Selection on a Per Channel Basis in TDM Mode
- Serial Peripheral Interface (SPI)
  - Slave Serial Boot through SPI from a Master SPI Device
  - Full-Duplex Operation
  - Master-Slave Mode Multimaster Support
  - Open-Drain Outputs
  - Programmable Baud Rates, Clock Polarities and Phases
- 12 Programmable I/O Pins
- 1 Programmable Timer

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## GENERAL DESCRIPTION

The ADSP-21161N SHARC DSP is the first low cost derivative of the ADSP-21160 featuring Analog Devices Super Harvard Architecture. Easing portability, the ADSP-21161N is source code compatible with the ADSP-21160 and with first generation ADSP-2106x SHARCs in SISD (Single Instruction, Single Data) mode. Like other SHARC DSPs, the ADSP-21161N is a 32-bit processor that is optimized for high performance DSP applications. The ADSP-21161N includes a 100 MHz core, a dual-ported on-chip SRAM, an integrated I/O processor with multiprocessing support, and multiple internal buses to eliminate I/O bottlenecks.

As was first offered in the ADSP-21160, the ADSP-21161N offers a Single-Instruction-Multiple-Data (SIMD) architecture. Using two computational units (ADSP-2106x SHARCs have one), the ADSP-21161N can double cycle performance versus the ADSP-2106x on a range of DSP algorithms.

Fabricated in a state of the art, high speed, low power CMOS process, the ADSP-21161N has a 10 ns instruction cycle time. With its SIMD computational hardware running at 100 MHz, the ADSP-21161N can perform 600 million math operations per second. Table 1 shows performance benchmarks for the ADSP-21161N.

**Table 1. Benchmarks (at 100 MHz)**

Benchmark Algorithm	Speed (at 100 MHz)
1024 Point Complex FFT (Radix 4, with reversal)	171 μs
FIR Filter (per tap) <sup>1</sup>	5 ns
IIR Filter (per biquad) <sup>1</sup>	40 ns <sup>1</sup>
Matrix Multiply (pipelined)	
[3 × 3] × [3 × 1]	30 ns
[4 × 4] × [4 × 1]	37 ns
Divide (y/x)	60 ns <sup>1</sup>
Inverse Square Root	40 ns <sup>1</sup>
DMA Transfers	800 M bytes/s

<sup>1</sup>Specified in SISD mode. Using SIMD, the same benchmark applies for two sets of computations. For example, two sets of biquad operations can be performed in the same amount of time as the SISD mode benchmark.

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The ADSP-21161N continues SHARC's industry-leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features. These features include a 1 M bit dual ported SRAM memory, host processor interface, I/O processor that supports 14 DMA channels, four serial ports, two link ports, SDRAM controller, SPI interface, external parallel bus, and glueless multiprocessing.

The block diagram of the ADSP-21161N on Page 1 illustrates the following architectural features:

- Two processing elements, each made up of an ALU, Multiplier, Shifter, and Data Register File
- Data Address Generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core every core processor cycle
- Interval timer

- On-Chip SRAM (1 M bit)
- SDRAM Controller for glueless interface to SDRAMs
- External port that supports:
  - Interfacing to off-chip memory peripherals
  - Glueless multiprocessing support for six ADSP-21161N SHARCs
  - Host port read/write of IOP registers
- DMA controller
- Four serial ports
- Two link ports
- SPI compatible interface
- JTAG test access port
- 12 General-Purpose I/O Pins

Figure 1 shows a typical single-processor system. A multiprocessing system appears in Figure 4 on Page 8.

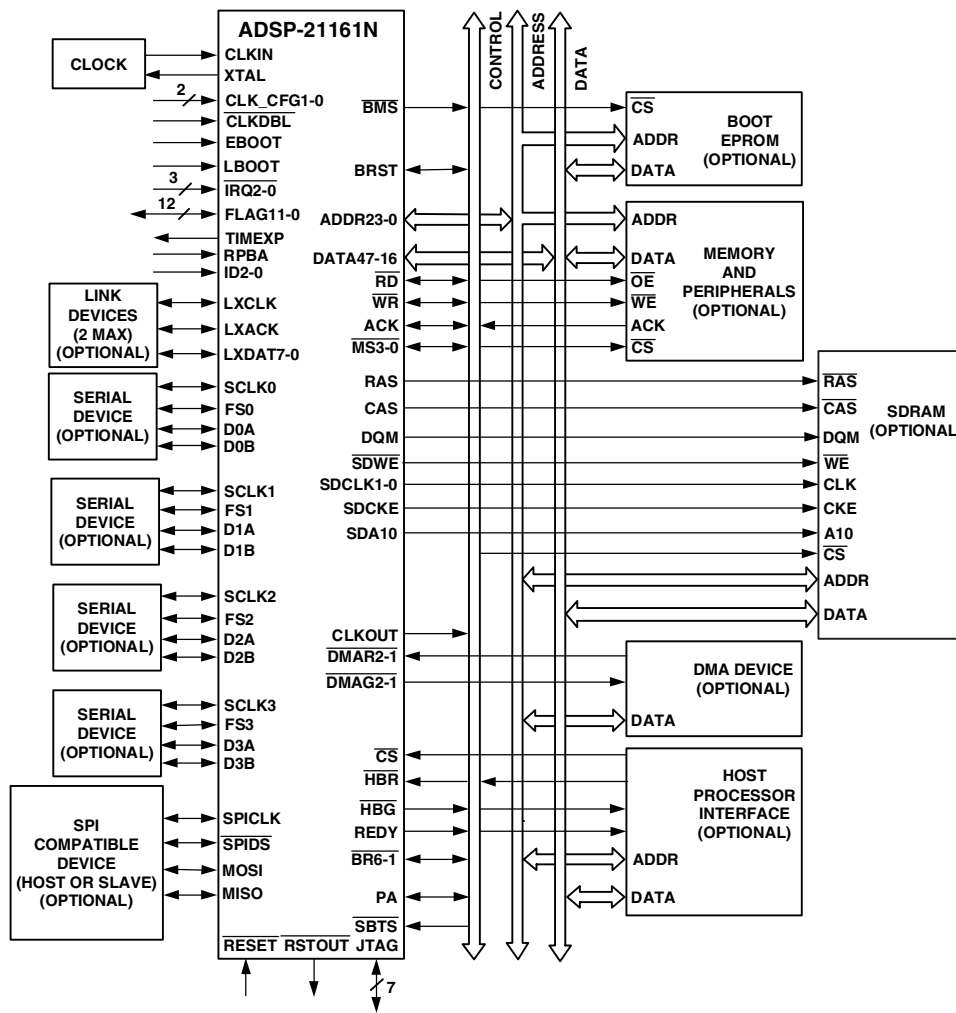


Figure 1. System Diagram

### ADSP-21161N Family Core Architecture

The ADSP-21161N includes the following architectural features of the ADSP-2116x family core. The ADSP-21161N is code compatible at the assembly level with the ADSP-21160, ADSP-21060, ADSP-21061, ADSP-21062, and ADSP-21065L.

#### *SIMD Computational Engine*

The ADSP-21161N contains two computational processing elements that operate as a Single Instruction Multiple Data (SIMD) engine. The processing elements are referred to as PEX and PEY, and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

SIMD is supported only for internal memory accesses and is not supported for off-chip accesses.

#### *Independent, Parallel Computation Units*

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform single-cycle instructions. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

#### *Data Register File*

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the ADSP-2116x enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

#### *Single-Cycle Fetch of Instruction and Four Operands*

The ADSP-21161N features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see [Figure 1 on Page 4](#)). With the ADSP-21161N's separate program and data memory buses and on-chip instruction cache,

the processor can simultaneously fetch four operands (two over each data bus) and an instruction (from the cache), all in a single cycle.

#### *Instruction Cache*

The ADSP-21161N includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache enables full-speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

#### *Data Address Generators With Hardware Circular Buffers*

The ADSP-21161N's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-21161N contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wrap-around, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

#### *Flexible Instruction Set*

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21161N can conditionally execute a multiply, an add, and a subtract in both processing elements, while branching, all in a single instruction.

#### *ADSP-21161N Memory and I/O Interface Features*

The ADSP-21161N adds the following architectural features to the ADSP-2116x family core:

#### *Dual-Ported On-Chip Memory*

The ADSP-21161N contains one megabit of on-chip SRAM, organized as two blocks of 0.5 M bits. Each block can be configured for different combinations of code and data storage. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor. The dual-ported memory in combination with three separate on-chip buses allow two data transfers from the core and one from the I/O processor, in a single cycle. On the ADSP-21161N, the memory can be configured as a maximum of 32K words of 32-bit data, 64K words of 16-bit data, 21K words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to one megabit. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers. Using the DM bus and



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PM bus, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

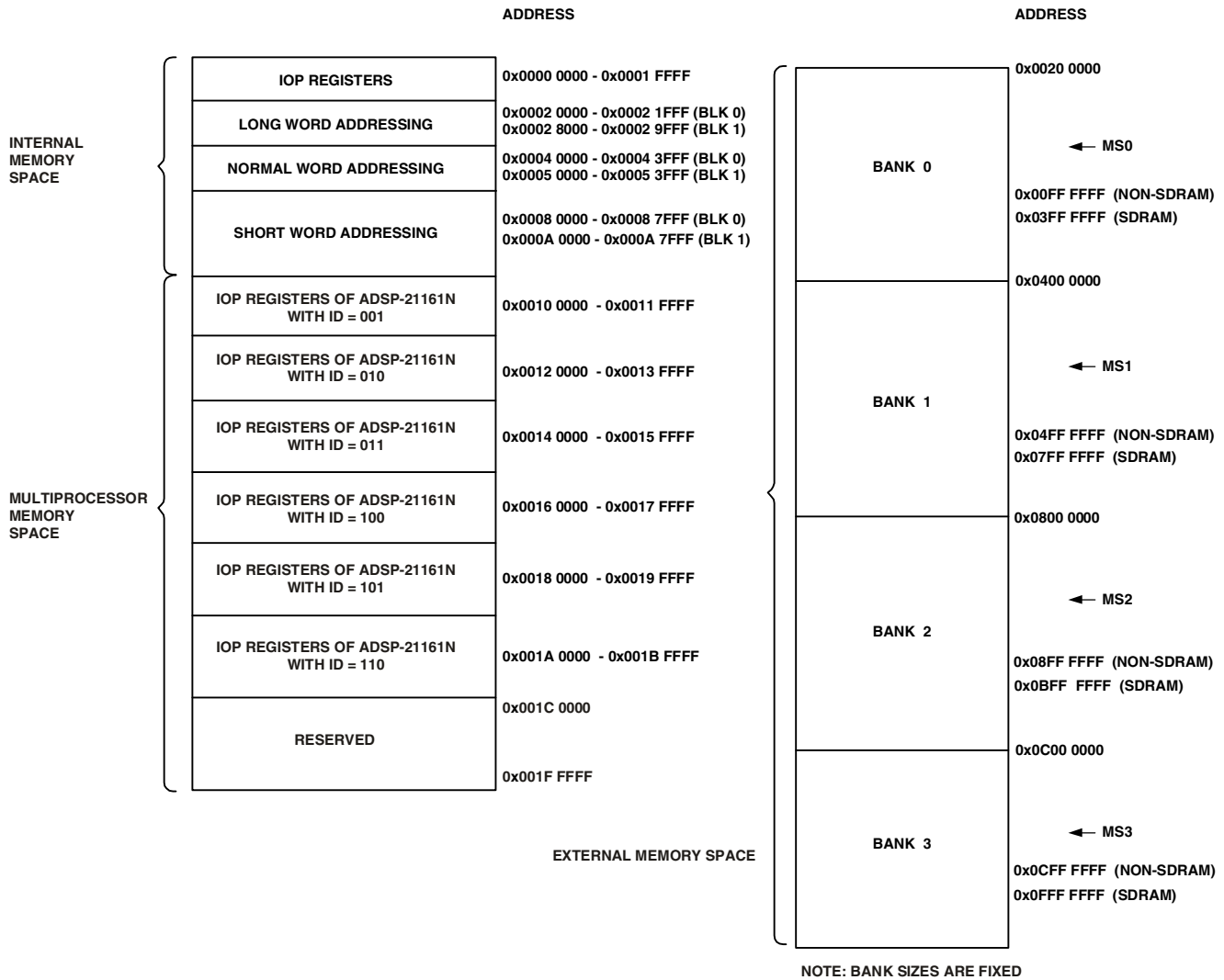


Figure 2. Memory Map

## Off-Chip Memory and Peripherals Interface

The ADSP-21161N's external port provides the processor's interface to off-chip memory and peripherals. The 62.7-M word off-chip address space (254.7-M word if all SDRAM) is included in the ADSP-21161N's unified address space. The separate on-chip buses—for PM addresses, PM data, DM addresses, DM data, I/O addresses, and I/O data—are multiplexed at the external port to create an external system bus with a single 24-bit address bus and a single 32-bit data bus. Every access to external memory is based on an address that fetches a 32-bit word. When fetching an instruction from external memory, two 32-bit data locations are being accessed for packed instructions. Unused link port lines can also be used as additional data lines DATA15–DATA0, allowing single-cycle execution of instructions from external memory, at up to 100 MHz. Figure 3 on Page 7 shows the alignment of various accesses to external memory.

The external port supports asynchronous, synchronous, and synchronous burst accesses. Synchronous burst SRAM can be interfaced gluelessly. The ADSP-21161N also can interface gluelessly to SDRAM. Addressing of external memory devices is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals. The ADSP-21161N provides programmable memory wait states and external memory acknowledge controls to allow interfacing to memory and peripherals with variable access, hold, and disable time requirements.

## SDRAM Interface

The SDRAM interface enables the ADSP-21161N to transfer data to and from synchronous DRAM (SDRAM) at the core clock frequency or at one-half the core clock frequency. The

synchronous approach, coupled with the core clock frequency, supports data transfer at a high throughput—up to 400 M bytes/s for 32-bit transfers and 600 M bytes/s for 48-bit transfers.

The SDRAM interface provides a glueless interface with standard SDRAMs—16 Mb, 64 Mb, 128 Mb, and 256 Mb—and includes options to support additional buffers between the ADSP-21161N and SDRAM. The SDRAM interface is extremely flexible and provides capability for connecting SDRAMs to any one of the ADSP-21161N's four external memory banks, with up to all four banks mapped to SDRAM.

Systems with several SDRAM devices connected in parallel may require buffering to meet overall system timing requirements. The ADSP-21161N supports pipelining of the address and control signals to enable such buffering between itself and multiple SDRAM devices.

### Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-21161N processor to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

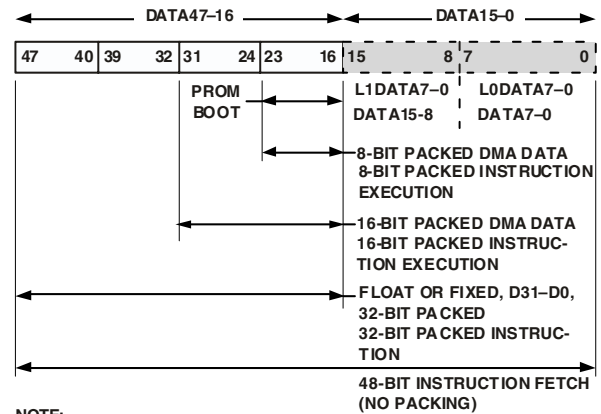
For complete information on SHARC Analog Devices DSP Tools product line of JTAG emulator operation, see the appropriate Emulator Hardware User's Guide. For detailed information on the interfacing of Analog Devices JTAG emulators with Analog Devices DSP products with JTAG emulation ports, please refer to Engineer to Engineer Note *EE-68: Analog Devices JTAG Emulation Technical Reference*. Both of these documents can be found on the Analog Devices website:

[http://www.analog.com/dsp/tech\\_docs.html](http://www.analog.com/dsp/tech_docs.html)

### DMA Controller

The ADSP-21161N's on-chip DMA controller enables zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the ADSP-21161N's internal memory and external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-21161N's internal memory and its serial ports, link ports, or the SPI-compatible (Serial Peripheral Interface) port. External bus packing and unpacking of 32-, 48-, or 64-bit words in internal memory is performed during DMA transfers from either 8-, 16-, or 32-bit wide external memory. Fourteen channels of DMA are available on the ADSP-21161N—two are shared between the SPI interface and the link ports, eight via the serial ports, and four via the processor's external port (for host processor, other ADSP-21161Ns, memory, or I/O transfers). Programs can be downloaded to the ADSP-21161N using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA Request/Grant lines ( $\overline{\text{DMAR2-I}}$ ,  $\overline{\text{DMAG2-I}}$ ).

Other DMA features include interrupt generation upon completion of DMA transfers, and DMA chaining for automatic linked DMA transfers.



NOTE:  
EXTRA DATA LINES DATA15-0 ARE ONLY ACCESSIBLE IF LINK PORTS ARE DISABLED. ENABLE THESE ADDITIONAL DATA LINKS BY SELECTING IPACK1-0 = 01 IN SYSCON.

Figure 3. External Data Alignment Options

### Multiprocessing

The ADSP-21161N offers powerful features tailored to multiprocessing DSP systems. The external port and link ports provide integrated glueless multiprocessing support.

The external port supports a unified address space (see Figure 2 on Page 6) that enables direct interprocessor accesses of each ADSP-21161N's internal memory-mapped (I/O processor) registers. All other internal memory can be indirectly accessed via DMA transfers initiated via the programming of the IOP DMA parameter and control registers. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-21161Ns and a host processor. Master processor change over incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock enables indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 400 M bytes/s over the external port.

Two link ports provide a second method of multiprocessing communications. Each link port can support communications to another ADSP-21161N. The ADSP-21161N, running at 100 MHz, has a maximum throughput for interprocessor communications over the links of 200 M bytes/s. The link ports and cluster multiprocessing can be used concurrently or independently.

### Link Ports

The ADSP-21161N features two 8-bit link ports that provide additional I/O capabilities. With the capability of running at 100 MHz, each link port can support 100 M bytes/s. Link port I/O is especially useful for point-to-point interprocessor communication in multiprocessing systems. The link ports can operate independently and simultaneously, with a maximum data throughput of 200 M bytes/s. Link port data is packed into 48- or 32-bit words and can be directly read by the core processor

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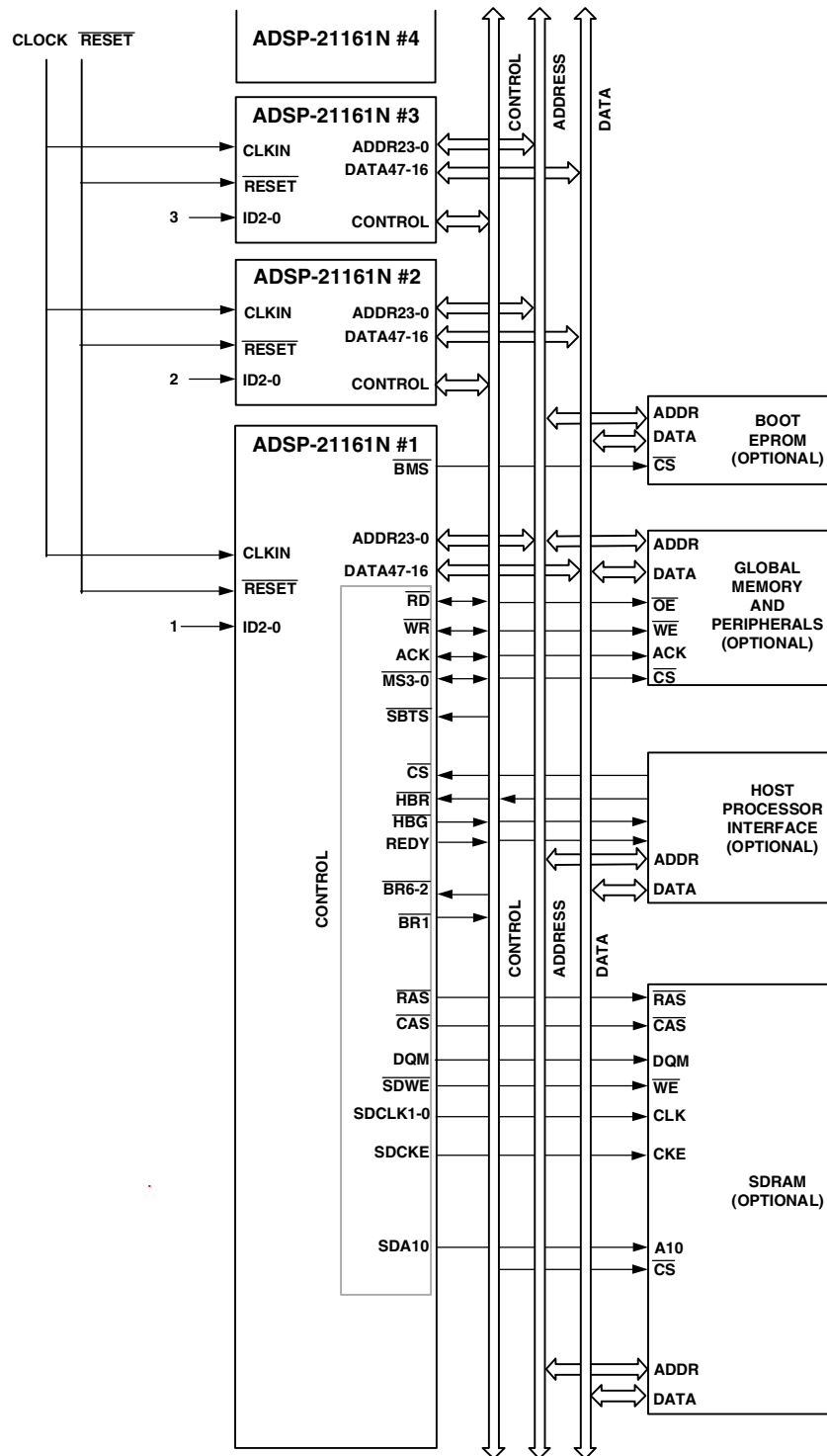


Figure 4. Shared Memory Multiprocessing System

or DMA-transferred to on-chip memory. Each link port has its own double-buffered input and output registers. Clock/acknowledge handshaking controls link port transfers. Transfers are programmable as either transmit or receive.

### Serial Ports

The ADSP-21161N features four synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. Each serial port is made up of two data lines, a clock and frame sync. The data lines can be programmed to either transmit or receive.



The serial ports operate at up to half the clock rate of the core, providing each with a maximum data rate of 50 M bit/s. The serial data pins are programmable as either a transmitter or receiver, providing greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via a dedicated DMA. Each of the serial ports features a Time Division Multiplex (TDM) multichannel mode, where two serial ports are TDM transmitters and two serial ports are TDM receivers (SPORT0 Rx paired with SPORT2 Tx, SPORT1 Rx paired with SPORT3 Tx). Each of the serial ports also support the I<sup>2</sup>S protocol (an industry standard interface commonly used by audio codecs, ADCs and DACs), with two data pins, allowing four I<sup>2</sup>S channels (using two I<sup>2</sup>S stereo devices) per serial port, with a maximum of up to 16 I<sup>2</sup>S channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For I<sup>2</sup>S mode, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional  $\mu$ -law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated.

### Serial Peripheral (Compatible) Interface

Serial Peripheral Interface (SPI) is an industry standard synchronous serial link, enabling the ADSP-21161N SPI-compatible port to communicate with other SPI-compatible devices. SPI is a 4-wire interface consisting of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The ADSP-21161N SPI-compatible peripheral implementation also features programmable baud rate and clock phase/polarities. The ADSP-21161N SPI-compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

### Host Processor Interface

The ADSP-21161N host interface enables easy connection to standard 8-bit, 16-bit, or 32-bit microprocessor buses with little additional hardware required. The host interface is accessed through the ADSP-21161N's external port. Four channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead. The host processor requests the ADSP-21161N's external bus with the host bus request ( $\overline{\text{HBR}}$ ), host bus grant ( $\overline{\text{HBG}}$ ), and chip select (CS) signals. The host can directly read and write the internal IOP registers of the ADSP-21161N, and can access the DMA channel setup and message registers. DMA setup via a host would allow it to access any internal memory address via DMA transfers. Vector interrupt support provides efficient execution of host commands.

### General-Purpose I/O Ports

The ADSP-21161N also contains 12 programmable, general purpose I/O pins that can function as either input or output. As output, these pins can signal peripheral devices; as input, these pins can provide the test for conditional branching.

### Program Booting

The internal memory of the ADSP-21161N can be booted at system power-up from either an 8-bit EPROM, a host processor, the SPI interface, or through one of the link ports. Selection of the boot source is controlled by the Boot Memory Select (BMS), EBOOT (EPROM Boot), and Link/Host Boot (LBOOT) pins. 8-, 16-, or 32-bit host processors can also be used for booting.

### Phase-Locked Loop and Crystal Double Enable

The ADSP-21161N uses an on-chip Phase-Locked Loop (PLL) to generate the internal clock for the core. The CLK\_CFG1–0 pins are used to select ratios of 2:1, 3:1, and 4:1. In addition to the PLL ratios, the  $\overline{\text{CLKDBL}}$  pin can be used for more clock ratio options. The  $(1 \times / 2 \times \text{CLKIN})$  rate set by the  $\overline{\text{CLKDBL}}$  pin determines the rate of the PLL input clock and the rate at which the external port operates. With the combination of CLK\_CFG1–0 and  $\overline{\text{CLKDBL}}$ , ratios of 2:1, 3:1, 4:1, 6:1, and 8:1 between the core and CLKIN are supported. See also [Figure 10 on Page 20](#).

### Power Supplies

The ADSP-21161N has separate power supply connections for the analog ( $\text{AV}_{\text{DD}}/\text{AGND}$ ), internal ( $\text{V}_{\text{DDINT}}$ ), and external ( $\text{V}_{\text{DDEXT}}$ ) power supplies. The internal and analog supplies must meet the 1.8 V requirement. The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same supply.

Note that the analog supply ( $\text{AV}_{\text{DD}}$ ) powers the ADSP-21161N's clock generator PLL. To produce a stable clock, provide an external circuit to filter the power input to the  $\text{AV}_{\text{DD}}$  pin. Place the filter as close as possible to the pin. For an example circuit, see [Figure 5](#). To prevent noise coupling, use a wide trace for the analog ground (AGND) signal and install a decoupling capacitor as close as possible to the pin.

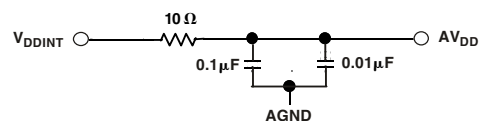


Figure 5. Analog Power ( $\text{AV}_{\text{DD}}$ ) Filter Circuit

### Development Tools

The ADSP-21161N is supported with a complete set of software and hardware development tools, including Analog Devices emulators and VisualDSP++<sup>1</sup> development environment. The same emulator hardware that supports other ADSP-21xxx DSPs, also fully emulates the ADSP-21161N.

The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy-to-use assembler that is based on an algebraic syntax; an archiver (librarian/library builder), a linker, a loader,

<sup>1</sup>VisualDSP++ is a registered trademark of Analog Devices, Inc.

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a cycle-accurate instruction-level simulator, a C/C++ compiler, and a C/C++ run-time library that includes DSP and mathematical functions. Two key points for these tools are:

- Compiled ADSP-21161N C/C++ code efficiency—The compiler has been developed for efficient translation of C/C++ code to ADSP-21161N assembly. The DSP has architectural features that improve the efficiency of compiled C/C++ code.
- ADSP-2106x family code compatibility—The assembler has legacy features to ease the conversion of existing ADSP-2106x applications to the ADSP-21161N.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information)
- Insert break points
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution
- Perform linear or statistical profiling of program execution
- Fill, dump, and graphically plot the contents of memory
- Source level debugging
- Create custom debugger windows

The VisualDSP++ IDE lets programmers define and manage DSP software development. Its dialog boxes and property pages let programmers configure and manage all of the ADSP-21xxx development tools, including the syntax highlighting in the VisualDSP++ editor. This capability permits:

- Controlling how the development tools process inputs and generate outputs.
- Maintaining a one-to-one correspondence with the tool's command line switches.

Analog Devices DSP emulators use the IEEE 1149.1 JTAG test access port of the ADSP-21161N processor to monitor and control the target board processor during emulation. The emulator provides full-speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the ADSP-21xxx processor family. Hardware tools include ADSP-21xxx PC plug-in cards. Third Party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

## Designing an Emulator-Compatible DSP Board (Target)

The Analog Devices DSP Tools family of emulators are tools that every DSP developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG Test Access Port (TAP) on each JTAG DSP. The emulator

uses the TAP to access the internal features of the DSP, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The DSP must be halted to send data and commands, but once an operation has been completed by the emulator, the DSP system is set running at full speed with no impact on system timing.

To use these emulators, the target's design must include the interface between an Analog Devices JTAG DSP and the emulation header on a custom DSP target board.

### Target Board Header

The emulator interface to an Analog Devices JTAG DSP is a 14-pin header, as shown in Figure 6. The customer must supply this header on the target board in order to communicate with the emulator. The interface consists of a standard dual row 0.025" square post header, set on 0.1" × 0.1" spacing, with a minimum post length of 0.235". Pin 3 is the key position used to prevent the pod from being inserted backwards. This pin must be clipped on the target board.

Also, the clearance (length, width, and height) around the header must be considered. Leave a clearance of at least 0.15" and 0.10" around the length and width of the header, and reserve a height clearance to attach and detach the pod connector.

As can be seen in Figure 6, there are two sets of signals on the header. There are the standard JTAG signals TMS, TCK, TDI, TDO,  $\overline{\text{TRST}}$ , and  $\overline{\text{EMU}}$  used for emulation purposes (via an emulator). There are also secondary JTAG signals BTMS, BTCK, BTDI, and  $\overline{\text{BTRST}}$  that are optionally used for board-level (boundary scan) testing.

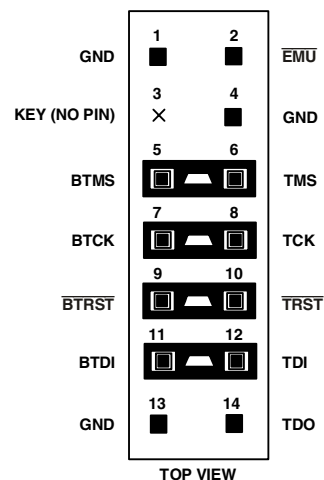


Figure 6. JTAG Target Board Connector for JTAG Equipped Analog Devices DSP (Jumpers in Place)

When the emulator is not connected to this header, place jumpers across BTMS, BTCK,  $\overline{\text{BTRST}}$ , and BTDI as shown in Figure 7. This holds the JTAG signals in the correct state to allow the DSP to run free. Remove all the jumpers when connecting the emulator to the JTAG header.

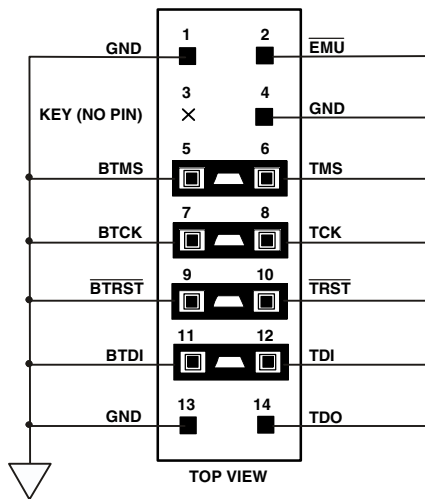


Figure 7. JTAG Target Board Connector with No Local Boundary Scan

**JTAG Emulator Pod Connector**

Figure 8 details the dimensions of the JTAG pod connector at the 14-pin target end. Figure 9 displays the keep-out area for a target board header. The keep-out area enables the pod connector to properly seat onto the target board header. This board area should contain no components (chips, resistors, capacitors, etc.). The dimensions are referenced to the center of the 0.025" square post pin.

**Design-for-Emulation Circuit Information**

For details on target board design issues including mechanical layout, single processor connections, multiprocessor scan chains, signal buffering, signal termination, and emulator pod logic, see

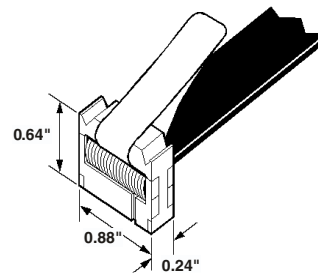


Figure 8. JTAG Pod Connector Dimensions

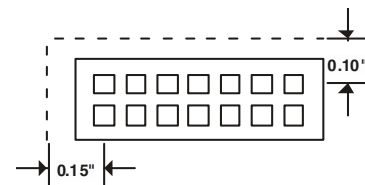


Figure 9. JTAG Pod Connector Keep-Out Area

the EE-68: *Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website ([www.analog.com](http://www.analog.com))—use site search on “EE-68”. This document is updated regularly to keep pace with improvements to emulator support.

**Additional Information**

This data sheet provides a general overview of the ADSP-21161N architecture and functionality. For detailed information on the ADSP-2116x Family core architecture and instruction set, refer to the *ADSP-21161 SHARC DSP Hardware Reference* and the *ADSP-21160 SHARC DSP Instruction Set Reference*.

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## PIN FUNCTION DESCRIPTIONS

ADSP-21161N pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for  $\overline{\text{TRST}}$ ). Tie or pull unused inputs to  $V_{\text{DDEXT}}$  or GND, except for the following:

- ADDR23–0, DATA47–0, BRST, CLKOUT (Note: These pins have a logic-level hold circuit enabled on the ADSP-21161N DSP with ID2–0 = 00x.)
- $\overline{\text{PA}}$ , ACK,  $\overline{\text{RD}}$ ,  $\overline{\text{WR}}$ ,  $\overline{\text{DMARx}}$ ,  $\overline{\text{DMAGx}}$ , (ID2–0 = 00x) (Note: These pins have a pull-up enabled on the ADSP-21161N DSP with ID2–0 = 00x.)
- LxCLK, LxACK, LxDAT7–0 (LxPDRDE = 0) (Note: See Link Port Buffer Control Register Bit definitions in the ADSP-21161N SHARC DSP Hardware Reference.)
- DxA, DxB, SCLKx, SPICLK, MISO, MOSI,  $\overline{\text{EMU}}$ , TMS,  $\overline{\text{TRST}}$ , TDI (Note: These pins have a pull-up.)

The following symbols appear in the Type column of Table 2: A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, and T = Three-State (when  $\overline{\text{SBTS}}$  is asserted or when the ADSP-21161N is a bus slave).

Unlike previous SHARC processors, the ADSP-21161N contains internal series resistance equivalent to 50  $\Omega$  on all input/output drivers except the CLKIN and XTAL pins. Therefore, for traces longer than six inches, external series resistors on control, data, clock, or frame sync pins are not required to dampen reflections from transmission line effects for point-to-point connections. However, for more complex networks such as a star configuration, series termination is still recommended.

Table 2. Pin Function Descriptions

Pin	Type	Function
ADDR23–0	I/O/T	<b>External Bus Address.</b> The ADSP-21161N outputs addresses for external memory and peripherals on these pins. In a multiprocessor system the bus master outputs addresses for read/writes of the IOP registers of other ADSP-21161Ns while all other internal memory resources can be accessed indirectly via DMA control (that is, accessing IOP DMA parameter registers). The ADSP-21161N inputs addresses when a host processor or multiprocessing bus master is reading or writing its IOP registers. A keeper latch on the DSP's ADDR23–0 pins maintains the input at the level it was last driven. This latch is only enabled on the ADSP-21161N with ID2–0=00x.
DATA47–16	I/O/T	<b>External Bus Data.</b> The ADSP-21161N inputs and outputs data and instructions on these pins. Pull-up resistors on unused data pins are not necessary. A keeper latch on the DSP's DATA47–16 pins maintains the input at the level it was last driven. This latch is only enabled on the ADSP-21161N with ID2–0=00x. <b>Note:</b> DATA15–8 pins (multiplexed with L1DAT7–0) can also be used to extend the data bus if the link ports are disabled and will not be used. In addition, DATA7–0 pins (multiplexed with L0DAT7–0) can also be used to extend the data bus if the link ports are not used. This enables execution of 48-bit instructions from external SBSRAM (system clock speed-external port), SRAM (system clock speed-external port) and SDRAM (core clock or one-half the core clock speed). The IPACKx Instruction Packing Mode Bits in SYSCON should be set correctly (IPACK1–0=0x1) to enable this full instruction Width/No-packing Mode of operation.
$\overline{\text{MS3}}\text{--}0$	I/O/T	<b>Memory Select Lines.</b> These outputs are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank sizes are fixed to 16 M words for non-SDRAM and 64 M words for SDRAM. The $\overline{\text{MS3}}\text{--}0$ outputs are decoded memory address lines. In asynchronous access mode, the $\overline{\text{MS3}}\text{--}0$ outputs transition with the other address outputs. In synchronous access modes, the $\overline{\text{MS3}}\text{--}0$ outputs assert with the other address lines; however, they deassert after the first CLKIN cycle in which ACK is sampled asserted. In a multiprocessor system, the $\overline{\text{MSx}}$ signals are tracked by slave SHARCs. The internal addresses 24 and 25 are zeros and 26 and 27 are decoded into $\overline{\text{MS3}}\text{--}0$ .
$\overline{\text{RD}}$	I/O/T	<b>Memory Read Strobe.</b> $\overline{\text{RD}}$ is asserted whenever ADSP-21161N reads a word from external memory or from the IOP registers of other ADSP-21161Ns. External devices, including other ADSP-21161Ns, must assert $\overline{\text{RD}}$ for reading from a word of the ADSP-21161N IOP register memory. In a multiprocessing system, $\overline{\text{RD}}$ is driven by the bus master. $\overline{\text{RD}}$ has a 20 k $\Omega$ internal pull-up resistor that is enabled for DSPs with ID2–0=00x.

**Table 2. Pin Function Descriptions (continued)**

Pin	Type	Function
$\overline{WR}$	I/O/T	<b>Memory Write Low Strobe.</b> $\overline{WR}$ is asserted when ADSP-21161N writes a word to external memory or IOP registers of other ADSP-21161Ns. External devices must assert $\overline{WR}$ for writing to ADSP-21161N IOP registers. In a multiprocessing system, the bus master drives $\overline{WR}$ . $\overline{WR}$ has a 20 k $\Omega$ internal pull-up resistor that is enabled for DSPs with ID2=0=00x.
BRST	I/O/T	<b>Sequential Burst Access.</b> BRST is asserted by ADSP-21161N to indicate that data associated with consecutive addresses is being read or written. A slave device samples the initial address and increments an internal address counter after each transfer. The incremented address is not pipelined on the bus. A master ADSP-21161N in a multiprocessing environment can read slave external port buffers (EPBx) using the burst protocol. BRST is asserted after the initial access of a burst transfer. It is asserted for every cycle after that, except for the last data request cycle (denoted by $\overline{RD}$ or $\overline{WR}$ asserted and BRST negated). A keeper latch on the DSP's BRST pin maintains the input at the level it was last driven. This latch is only enabled on the ADSP-21161N with ID2=0=00x.
ACK	I/O/S	<b>Memory Acknowledge.</b> External devices can de-assert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-21161N deasserts ACK as an output to add wait states to a synchronous access of its IOP registers. ACK has a 20 k $\Omega$ internal pull-up resistor that is enabled during reset or on DSPs with ID2=0=00x.
$\overline{SBTS}$	I/S	<b>Suspend Bus and Three-State.</b> External devices can assert $\overline{SBTS}$ (low) to place the external bus address, data, selects, and strobes in a high impedance state for the following cycle. If the ADSP-21161N attempts to access external memory while $\overline{SBTS}$ is asserted, the processor will halt and the memory access will not be completed until $\overline{SBTS}$ is deasserted. $\overline{SBTS}$ should only be used to recover from host processor/ADSP-21161N deadlock.
$\overline{CAS}$	I/O/T	<b>SDRAM Column Access Strobe.</b> In conjunction with $\overline{RAS}$ , $\overline{MSx}$ , $\overline{SDWE}$ , SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
$\overline{RAS}$	I/O/T	<b>SDRAM Row Access Strobe.</b> In conjunction with $\overline{CAS}$ , $\overline{MSx}$ , $\overline{SDWE}$ , SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
$\overline{SDWE}$	I/O/T	<b>SDRAM Write Enable.</b> In conjunction with $\overline{CAS}$ , $\overline{RAS}$ , $\overline{MSx}$ , SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
DQM	O/T	<b>SDRAM Data Mask.</b> In write mode, DQM has a latency of zero and is used during a precharge command and during SDRAM power-up initialization.
SDCLK0	I/O/S/T	<b>SDRAM Clock Output 0.</b> Clock for SDRAM devices.
SDCLK1	O/S/T	<b>SDRAM Clock Output 1.</b> Additional clock for SDRAM devices. For systems with multiple SDRAM devices, handles the increased clock load requirements, eliminating need of off-chip clock buffers. Either SDCLK1 or both SDCLKx pins can be three-stated.
SDCKE	I/O/T	<b>SDRAM Clock Enable.</b> Enables and disables the CLK signal. For details, see the data sheet supplied with the SDRAM device.
SDA10	O/T	<b>SDRAM A10 Pin.</b> Enables applications to refresh an SDRAM in parallel with a non-SDRAM accesses or host accesses. This pin replaces the DSP's A10 pin only during SDRAM accesses.
$\overline{IRQ2-0}$	I/A	<b>Interrupt Request Lines.</b> These are sampled on the rising edge of CLKIN and may be either edge-triggered or level-sensitive.
FLAG11-0	I/O/A	<b>Flag Pins.</b> Each is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
TIMEXP	O	<b>Timer Expired.</b> Asserted for four core clock cycles when the timer is enabled and TCOUNT decrements to zero.
$\overline{HBR}$	I/A	<b>Host Bus Request.</b> Must be asserted by a host processor to request control of the ADSP-21161N's external bus. When $\overline{HBR}$ is asserted in a multiprocessing system, the ADSP-21161N that is bus master will relinquish the bus and assert $\overline{HBG}$ . To relinquish the bus, the ADSP-21161N places the address, data, select, and strobe lines in a high impedance state. $\overline{HBR}$ has priority over all ADSP-21161N bus requests ( $\overline{BR6-1}$ ) in a multiprocessing system.



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Table 2. Pin Function Descriptions (continued)

Pin	Type	Function
$\overline{\text{HBG}}$	I/O	<b>Host Bus Grant.</b> Acknowledges an $\overline{\text{HBR}}$ bus request, indicating that the host processor may take control of the external bus. $\overline{\text{HBG}}$ is asserted (held low) by the ADSP-21161N until $\overline{\text{HBR}}$ is released. In a multiprocessing system, $\overline{\text{HBG}}$ is output by the ADSP-21161N bus master and is monitored by all others. After $\overline{\text{HBR}}$ is asserted, and before $\overline{\text{HBG}}$ is given, $\overline{\text{HBG}}$ will float for 1 $t_{\text{CK}}$ (1 CLKIN cycle). To avoid erroneous grants, $\overline{\text{HBG}}$ should be pulled up with a 20k $\Omega$ to 50k $\Omega$ external resistor.
$\overline{\text{CS}}$	I/A	<b>Chip Select.</b> Asserted by host processor to select the ADSP-21161N.
REDY	O (O/D)	<b>Host Bus Acknowledge.</b> The ADSP-21161N deasserts REDY (low) to add wait states to a host access of its IOP registers when $\overline{\text{CS}}$ and $\overline{\text{HBR}}$ inputs are asserted.
$\overline{\text{DMAR1}}$	I/A	<b>DMA Request 1</b> (DMA Channel 11). Asserted by external port devices to request DMA services. $\overline{\text{DMAR1}}$ has a 20 k $\Omega$ internal pull-up resistor that is enabled for DSPs with ID2=0=00x.
$\overline{\text{DMAR2}}$	I/A	<b>DMA Request 2</b> (DMA Channel 12). Asserted by external port devices to request DMA services. $\overline{\text{DMAR2}}$ has a 20 k $\Omega$ internal pull-up resistor that is enabled for DSPs with ID2=0=00x.
$\overline{\text{DMAG1}}$	O/T	<b>DMA Grant 1</b> (DMA Channel 11). Asserted by ADSP-21161N to indicate that the requested DMA starts on the next cycle. Driven by bus master only. $\overline{\text{DMAG1}}$ has a 20 k $\Omega$ internal pull-up resistor that is enabled for DSPs with ID2=0=00x.
$\overline{\text{DMAG2}}$	O/T	<b>DMA Grant 2</b> (DMA Channel 12). Asserted by ADSP-21161N to indicate that the requested DMA starts on the next cycle. Driven by bus master only. $\overline{\text{DMAG2}}$ has a 20 k $\Omega$ internal pull-up resistor that is enabled for DSPs with ID2=0=00x.
$\overline{\text{BR6-1}}$	I/O/S	<b>Multiprocessing Bus Requests.</b> Used by multiprocessing ADSP-21161Ns to arbitrate for bus mastership. An ADSP-21161N only drives its own $\overline{\text{BRx}}$ line (corresponding to the value of its ID2=0 inputs) and monitors all others. In a multiprocessor system with less than six ADSP-21161Ns, the unused $\overline{\text{BRx}}$ pins should be pulled high; the processor's own $\overline{\text{BRx}}$ line must not be pulled high or low because it is an output.
BMSTR	O	<b>Bus Master Output.</b> In a multiprocessor system, indicates whether the ADSP-21161N is current bus master of the shared external bus. The ADSP-21161N drives BMSTR high only while it is the bus master. In a single-processor system (ID=000), the processor drives this pin high. This pin is used for debugging purposes.
ID2=0	I	<b>Multiprocessing ID.</b> Determines which multiprocessing bus request ( $\overline{\text{BR6-1}}$ ) is used by ADSP-21161N. ID=001 corresponds to $\overline{\text{BR1}}$ , ID=010 corresponds to $\overline{\text{BR2}}$ , and so on. Use ID=000 or ID=001 in single-processor systems. These lines are a system configuration selection that should be hardwired or only changed at reset.
RPBA	I/S	<b>Rotating Priority Bus Arbitration Select.</b> When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection that must be set to the same value on every ADSP-21161N. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every ADSP-21161N.
$\overline{\text{PA}}$	I/O/T	<b>Priority Access.</b> Asserting its $\overline{\text{PA}}$ pin enables an ADSP-21161N bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{\text{PA}}$ is connected to all ADSP-21161Ns in the system. If access priority is not required in a system, the $\overline{\text{PA}}$ pin should be left unconnected. $\overline{\text{PA}}$ has a 20 k $\Omega$ internal pull-up resistor that is enabled for DSPs with ID2=0=00x.
DxA	I/O	<b>Data Transmit or Receive Channel A</b> (Serial Ports 0, 1, 2, 3). Each DxA pin has an internal pull-up resistor. Bidirectional data pin. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
DxB	I/O	<b>Data Transmit or Receive Channel B</b> (Serial Ports 0, 1, 2, 3). Each DxB pin has an internal pull-up resistor. Bidirectional data pin. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SCLKx	I/O	<b>Transmit/Receive Serial Clock</b> (Serial Ports 0, 1, 2, 3). Each SCLK pin has an internal pull-up resistor. This signal can be either internally or externally generated.

**Table 2. Pin Function Descriptions (continued)**

Pin	Type	Function
FSx	I/O	<b>Transmit or Receive Frame Sync</b> (Serial Ports 0, 1, 2, 3). The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally. It can be active high or low or an early or a late frame sync, in reference to the shifting of serial data.
SPICLK	I/O	<b>Serial Peripheral Interface Clock Signal.</b> Driven by the master, this signal controls the rate at which data is transferred. The master may transmit data at a variety of baud rates. SPICLK cycles once for each bit transmitted. SPICLK is a gated clock that is active during data transfers, only for the length of the transferred word. Slave devices ignore the serial clock if the slave select input is driven inactive (HIGH). SPICLK is used to shift out and shift in the data driven on the MISO and MOSI lines. The data is always shifted out on one clock edge of the clock and sampled on the opposite edge of the clock. Clock polarity and clock phase relative to data are programmable into the SPICTL control register and define the transfer format. SPICLK has a 50 kΩ internal pull-up resistor.
$\overline{\text{SPIDS}}$	I	<b>Serial Peripheral Interface Slave Device Select.</b> An active low signal used to enable slave devices. This input signal behaves like a chip select, and is provided by the master device for the slave devices. In multimaster mode $\overline{\text{SPIDS}}$ signal can be asserted to a master device to signal that an error has occurred, as some other device is also trying to be the master device. If asserted low when the device is in master mode, it is considered a multimaster error. For a single-master, multiple-slave configuration where FLAG3–0 are used, this pin must be tied or pulled high to $V_{\text{DDEXT}}$ on the master device. For ADSP-21161N to ADSP-21161N SPI interaction, any of the master ADSP-21161N's FLAG3–0 pins can be used to drive the $\overline{\text{SPIDS}}$ signal on the ADSP-21161N SPI slave device.
MOSI	I/O (o/d)	<b>SPI Master Out Slave.</b> If the ADSP-21161N is configured as a master, the MOSI pin becomes a data transmit (output) pin, transmitting output data. If the ADSP-21161N is configured as a slave, the MOSI pin becomes a data receive (input) pin, receiving input data. In an ADSP-21161N SPI interconnection, the data is shifted out from the MOSI output pin of the master and shifted into the MOSI input(s) of the slave(s). MOSI has an internal pull-up resistor.
MISO	I/O (o/d)	<b>SPI Master In Slave Out.</b> If the ADSP-21161N is configured as a master, the MISO pin becomes a data receive (input) pin, receiving input data. If the ADSP-21161N is configured as a slave, the MISO pin becomes a data transmit (output) pin, transmitting output data. In an ADSP-21161N SPI interconnection, the data is shifted out from the MISO output pin of the slave and shifted into the MISO input pin of the master. MISO has an internal pull-up resistor. MISO can be configured as o/d by setting the OPD bit in the SPICTL register. <b>Note:</b> <i>Only one slave is allowed to transmit data at any given time.</i>
LxDAT7–0 [DATA15–0]	I/O [I/O/T]	Link Port Data (Link Ports 0–1). For silicon revisions 1.2 and higher, each LxDAT pin has a keeper latch that is enabled when used as a data pin; or a 20 kΩ internal pull-down resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register. For silicon revisions 0.3, 1.0, and 1.1 each LxDAT pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register. <b>Note:</b> <i>L1DAT7–0 are multiplexed with the DATA15–8 pins L0DAT7–0 are multiplexed with the DATA7–0 pins. If link ports are disabled and are not used, these pins can be used as additional data lines for executing instructions at up to the full clock rate from external memory. See DATA47–16 for more information.</i>
LxCLK	I/O	<b>Link Port Clock</b> (Link Ports 0–1). Each LxCLK pin has an internal pull-down 50 kΩ resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register.
LxACK	I/O	<b>Link Port Acknowledge</b> (Link Ports 0–1). Each LxACK pin has an internal pull-down 50 kΩ resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register.
EBOOT	I	<b>EPROM Boot Select.</b> For a description of how this pin operates, see the table in the $\overline{\text{BMS}}$ pin description. This signal is a system configuration selection that should be hardwired.
LBOOT	I	<b>Link Boot.</b> For a description of how this pin operates, see the table in the $\overline{\text{BMS}}$ pin description. This signal is a system configuration selection that should be hardwired.

# ADSP-21161N

Table 2. Pin Function Descriptions (continued)

Pin	Type	Function
$\overline{\text{BMS}}$	I/O/T	<b>Boot Memory Select.</b> Serves as an output or input as selected with the EBOOT and LBOOT pins (see Table 4). This input is a system configuration selection that should be hardwired. For Host and PROM boot, DMA channel 10 (EPB0) is used. For Link boot and SPI boot, DMA channel 8 is used. Three-state only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output).
CLKIN	I	<b>Local Clock In.</b> Used in conjunction with XTAL. CLKIN is the ADSP-21161N clock input. It configures the ADSP-21161N to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the ADSP-21161N to use the external clock source such as an external clock oscillator. The ADSP-21161N external port cycles at the frequency of CLKIN. The instruction cycle rate is a multiple of the CLKIN frequency; it is programmable at power-up via the CLK_CFG1–0 pins. CLKIN may not be halted, changed, or operated below the specified frequency.
XTAL	O	<b>Crystal Oscillator Terminal 2.</b> Used in conjunction with CLKIN to enable the ADSP-21161N's internal clock oscillator or to disable it to use an external clock source. See CLKIN.
CLK_CFG1-0	I	<b>Core/CLKIN Ratio Control.</b> ADSP-21161N core clock (instruction cycle) rate is equal to $n \times \text{PLLCLK}$ where $n$ is user selectable to 2, 3, or 4, using the CLK_CFG1–0 inputs. These pins can also be used in combination with the $\overline{\text{CLKDBL}}$ pin to generate additional core clock rates of $6 \times \text{CLKIN}$ and $8 \times \text{CLKIN}$ (see the Clock Rate Ratios table in the $\overline{\text{CLKDBL}}$ description).
$\overline{\text{CLKDBL}}$	I	<b>Crystal Double Mode Enable.</b> This pin is used to enable the $2\times$ clock double circuitry, where CLKOUT can be configured as either $1\times$ or $2\times$ the rate of CLKIN. This CLKIN double circuit is primarily intended to be used for an external crystal in conjunction with the internal clock generator and the XTAL pin. The internal clock generator when used in conjunction with the XTAL pin and an external crystal is designed to support up to a maximum of 25 MHz external crystal frequency. $\overline{\text{CLKDBL}}$ can be used in XTAL mode to generate a 50 MHz input into the PLL. The $2\times$ clock mode is enabled (during $\overline{\text{RESET}}$ low) by tying $\overline{\text{CLKDBL}}$ to GND, otherwise it is connected to $V_{\text{DDEXT}}$ for $1\times$ clock mode. For example, this enables the use of a 25 MHz crystal to enable 100 MHz core clock rates and a 50 MHz CLKOUT operation when CLK_CFG0=0, CLK_CFG1=0 and $\overline{\text{CLKDBL}}=0$ . This pin can also be used to generate different clock rate ratios for external clock oscillators as well. The possible clock rate ratio options (up to 100 MHz) for either CLKIN (external clock oscillator) or XTAL (crystal input) are shown in Table 3 on Page 17. An 8:1 ratio enables the use of a 12.5 MHz crystal to generate a 100 MHz core (instruction clock) rate and a 25 MHz CLKOUT (external port) clock rate. See also Figure 10 on Page 20. <b>Note:</b> When using an external crystal, the maximum crystal frequency cannot exceed 25 MHz. For all other external clock sources, the maximum CLKIN frequency is 50 MHz.
CLKOUT	O/T	<b>Local Clock Out.</b> CLKOUT is $1\times$ or $2\times$ and is driven at either $1\times$ or $2\times$ the frequency of CLKIN frequency by the current bus master. The frequency is determined by the $\overline{\text{CLKDBL}}$ pin. This output is three-stated when the ADSP-21161N is not the bus master or when the host controls the bus ( $\overline{\text{HBG}}$ asserted). A keeper latch on the DSP's CLKOUT pin maintains the output at the level it was last driven. This latch is only enabled on the ADSP-21161N with ID2–0=00x. If $\overline{\text{CLKDBL}}$ enabled, $\text{CLKOUT}=2 \times \text{CLKIN}$ If $\overline{\text{CLKDBL}}$ disabled, $\text{CLKOUT}=1 \times \text{CLKIN}$ <b>Note:</b> CLKOUT is only controlled by the $\overline{\text{CLKDBL}}$ pin and operates at either $1 \times \text{CLKIN}$ or $2 \times \text{CLKIN}$ . Do not use CLKOUT in multiprocessing systems. Use CLKIN instead.
$\overline{\text{RESET}}$	I/A	<b>Processor Reset.</b> Resets the ADSP-21161N to a known state and begins execution at the program memory location specified by the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.

**Table 2. Pin Function Descriptions (continued)**

Pin	Type	Function
$\overline{\text{RSTOUT}}^1$	O	<b>Reset Out.</b> When $\overline{\text{RSTOUT}}$ is asserted (low), this pin indicates that the core blocks are in reset. It is deasserted 4080 cycles after $\overline{\text{RESET}}$ is deasserted indicating that the PLL is stable and locked.
TCK	I	<b>Test Clock (JTAG).</b> Provides a clock for JTAG boundary scan.
TMS	I/S	<b>Test Mode Select (JTAG).</b> Used to control the test state machine. TMS has a 20 k $\Omega$ internal pull-up resistor.
TDI	I/S	<b>Test Data Input (JTAG).</b> Provides serial data for the boundary scan logic. TDI has a 20 k $\Omega$ internal pull-up resistor.
TDO	O	<b>Test Data Output (JTAG).</b> Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	<b>Test Reset (JTAG).</b> Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21161N. $\overline{\text{TRST}}$ has a 20 k $\Omega$ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D)	<b>Emulation Status.</b> Must be connected to the ADSP-21161N Analog Devices DSP Tools product line of JTAG emulators target board connector only. $\overline{\text{EMU}}$ has a 50 k $\Omega$ internal pull-up resistor.
$V_{\text{DDINT}}$	P	<b>Core Power Supply.</b> Nominally +1.8 V dc and supplies the DSP's core processor (14 pins).
$V_{\text{DDEXT}}$	P	<b>I/O Power Supply.</b> Nominally +3.3 V dc. (13 pins).
AVDD	P	<b>Analog Power Supply.</b> Nominally +1.8 V dc and supplies the DSP's internal PLL (clock generator). This pin has the same specifications as $V_{\text{DDINT}}$ , except that added filtering circuitry is required. <a href="#">See Power Supplies on Page 9.</a>
AGND	G	<b>Analog Power Supply Return.</b>
GND	G	<b>Power Supply Return.</b> (26 pins).
NC		<b>Do Not Connect.</b> Reserved pins that must be left open and unconnected. (5 pins <sup>2</sup> ).

<sup>1</sup> $\overline{\text{RSTOUT}}$  exists only for silicon revision 1.2.

<sup>2</sup>Four NC pins for silicon revision 1.2, because  $\overline{\text{RSTOUT}}$  has been added.

**Table 3. Clock Rate Ratios**

CLKDBL	CLK_CFG1	CLK_CFG0	Core:CLKIN	CLKIN:CLKOUT
1	0	0	2:1	1:1
1	0	1	3:1	1:1
1	1	0	4:1	1:1
0	0	0	4:1	1:2
0	0	1	6:1	1:2
0	1	0	8:1	1:2

## BOOT MODES

**Table 4. Boot Mode Selection**

EBOOT	LBOOT	$\overline{\text{BMS}}$	Booting Mode
1	0	Output	EPROM (Connect $\overline{\text{BMS}}$ to EPROM chip select.)
0	0	1 (Input)	Host Processor
0	1	0 (Input)	Serial Boot via SPI
0	1	1 (Input)	Link Port
0	0	0 (Input)	No Booting. Processor executes from external memory.
1	1	x (Input)	Reserved

# ADSP-21161N

## SPECIFICATIONS

### RECOMMENDED OPERATING CONDITIONS

Parameter	Test Conditions	C Grade		K Grade		Unit
		Min	Max	Min	Max	
V <sub>DDINT</sub>	Internal (Core) Supply Voltage	1.71	1.89	1.71	1.89	V
A <sub>VDD</sub>	Analog (PLL) Supply Voltage	1.71	1.89	1.71	1.89	V
V <sub>DDEXT</sub>	External (I/O) Supply Voltage	3.13	3.47	3.13	3.47	V
V <sub>IH</sub>	High Level Input Voltage <sup>1</sup>	@ V <sub>DDEXT</sub> = max	2.0 V <sub>DDEXT</sub> + 0.5	2.0	V <sub>DDEXT</sub> + 0.5	V
V <sub>IL</sub>	Low Level Input Voltage <sup>1</sup>	@ V <sub>DDEXT</sub> = min	-0.5 + 0.8	-0.5	+ 0.8	V
T <sub>CASE</sub>	Case Operating Temperature <sup>2</sup>	-40	+105	0	+ 85	°C

Specifications subject to change without notice.

<sup>1</sup> Applies to input and bidirectional pins: DATA47-16, ADDR23-0, MS3-0, RD, WR, ACK, SBTS, IRQ2-0, FLAG11-0, HBG, HBR, CS, DMAR1, DMAR2, BR6-1, ID2-0, RPBA, PA, BRST, FSx, DxA, DxB, SCLKx, RAS, CAS, SDWE, SDCLK0, LxDAT7-0, LxCLK, LxACK, SPICLK, MOSI, MISO, SPIDS, EBOOT, LBOOT, BMS, SDCKE, CLK\_CFGx, CLKDBL, CLKIN, RESET, TRST, TCK, TMS, TDI.

<sup>2</sup> See Thermal Characteristics on Page 52 for information on thermal specifications.

### ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions	Min	Max	Unit	
V <sub>OH</sub>	High Level Output Voltage <sup>1</sup>	@ V <sub>DDEXT</sub> = min, I <sub>OH</sub> = -2.0 mA <sup>2</sup>	2.4	V	
V <sub>OL</sub>	Low Level Output Voltage <sup>1</sup>	@ V <sub>DDEXT</sub> = min, I <sub>OL</sub> = 4.0 mA <sup>2</sup>	0.4	V	
I <sub>IH</sub>	High Level Input Current <sup>3, 4</sup>	@ V <sub>DDEXT</sub> = max, V <sub>IN</sub> = V <sub>DDEXT</sub> max	10	μA	
I <sub>IL</sub>	Low Level Input Current <sup>3</sup>	@ V <sub>DDEXT</sub> = max, V <sub>IN</sub> = 0 V	10	μA	
I <sub>IHC</sub>	CLKIN High Level Input Current <sup>5</sup>	@ V <sub>DDEXT</sub> = max, V <sub>IN</sub> = V <sub>DDEXT</sub> max	35	μA	
I <sub>ILC</sub>	CLKIN Low Level Input Current <sup>5</sup>	@ V <sub>DDEXT</sub> = max, V <sub>IN</sub> = 0 V	35	μA	
I <sub>IKH</sub>	Keeper High Load Current <sup>6</sup>	@ V <sub>DDEXT</sub> = max, V <sub>IN</sub> = 2.0 V	-250	-100	μA
I <sub>IKL</sub>	Keeper Low Load Current <sup>6</sup>	@ V <sub>DDEXT</sub> = max, V <sub>IN</sub> = 0.8 V	50	200	μA
I <sub>IKH-OD</sub>	Keeper High Overdrive Current <sup>6, 7, 8</sup>	@ V <sub>DDEXT</sub> = max	-300		μA
I <sub>IKL-OD</sub>	Keeper Low Overdrive Current <sup>6, 7, 8</sup>	@ V <sub>DDEXT</sub> = max	300		μA
I <sub>ILPU</sub>	Low Level Input Current Pull-Up <sup>4</sup>	@ V <sub>DDEXT</sub> = max, V <sub>IN</sub> = 0 V	350		μA
I <sub>OZH</sub>	Three-State Leakage Current <sup>9, 10, 11</sup>	@ V <sub>DDEXT</sub> = max, V <sub>IN</sub> = V <sub>DDEXT</sub> max	10		μA
I <sub>OZL</sub>	Three-State Leakage Current <sup>9, 12, 13</sup>	@ V <sub>DDEXT</sub> = max, V <sub>IN</sub> = 0 V	10		μA
I <sub>OZLPU1</sub>	Three-State Leakage Current Pull-Up <sup>10</sup>	@ V <sub>DDEXT</sub> = max, V <sub>IN</sub> = 0 V	500		μA
I <sub>OZLPU2</sub>	Three-State Leakage Current Pull-Up <sup>11</sup>	@ V <sub>DDEXT</sub> = max, V <sub>IN</sub> = 0 V	350		μA
I <sub>OZHDP1</sub>	Three-State Leakage Current Pull-Down <sup>12</sup>	@ V <sub>DDEXT</sub> = max, V <sub>IN</sub> = V <sub>DDEXT</sub> max	350		μA
I <sub>OZHDP2</sub>	Three-State Leakage Current Pull-Down <sup>13</sup>	@ V <sub>DDEXT</sub> = max, V <sub>IN</sub> = V <sub>DDEXT</sub> max	500		μA
I <sub>DD-INPEAK</sub>	Supply Current (Internal) <sup>14, 15</sup>	t <sub>CCLK</sub> = 10.0 ns, V <sub>DDINT</sub> = max	900		mA
I <sub>DD-INHIGH</sub>	Supply Current (Internal) <sup>15, 16</sup>	t <sub>CCLK</sub> = 10.0 ns, V <sub>DDINT</sub> = max	650		mA
I <sub>DD-INLOW</sub>	Supply Current (Internal) <sup>15, 17</sup>	t <sub>CCLK</sub> = 10.0 ns, V <sub>DDINT</sub> = max	500		mA
I <sub>DD-IDLE</sub>	Supply Current (Idle) <sup>15, 18</sup>	t <sub>CCLK</sub> = 10.0 ns, V <sub>DDINT</sub> = max	400		mA
A <sub>IDD</sub>	Supply Current (Analog) <sup>19</sup>	@ A <sub>VDD</sub> = max	10		mA
C <sub>IN</sub>	Input Capacitance <sup>20, 21</sup>	f <sub>IN</sub> = 1 MHz, T <sub>CASE</sub> = 25°C, V <sub>IN</sub> = 1.8 V	4.7		pF

Specifications subject to change without notice.

<sup>1</sup> Applies to output and bidirectional pins: DATA47-16, ADDR23-0, MS3-0, RD, WR, ACK, DQM, FLAG11-0, HBG, REDY, DMAG1, DMAG2, BR6-1, BMSTR, PA, BRST, FSx, DxA, DxB, SCLKx, RAS, CAS, SDWE, SDA10, LxDAT7-0, LxCLK, LxACK, SPICLK, MOSI, MISO, BMS, SDCLKx, SDCKE, EMU, XTAL, TDO, CLKOUT, TIMEXP, RSTOUT.

<sup>2</sup> See Output Drive Currents on Page 51 for typical drive current capabilities.

<sup>3</sup> Applies to input pins: DATA47-16, ADDR23-0, MS3-0, SBTS, IRQ2-0, FLAG11-0, HBG, HBR, CS, BR6-1, ID2-0, RPBA, BRST, FSx, DxA, DxB, SCLKx, RAS, CAS, SDWE, SDCLK0, LxDAT7-0, LxCLK, LxACK, SPICLK, MOSI, MISO, SPIDS, EBOOT, LBOOT, BMS, SDCKE, CLK\_CFGx, CLKDBL, TCK, RESET, CLKIN.

<sup>4</sup> Applies to input pins with 20 kΩ internal pull-ups: RD, WR, ACK, DMAR1, DMAR2, PA, TRST, TMS, TDI.

<sup>5</sup> Applies to CLKIN only.

<sup>6</sup> Applies to all pins with keeper latches: ADDR23-0, DATA47-0, MS3-0, BRST, CLKOUT.

<sup>7</sup> Current required to switch from kept high to low or from kept low to high.

<sup>8</sup> Characterized, but not tested.



<sup>9</sup>Applies to three-statable pins: DATA47–16, ADDR23–0,  $\overline{MS3-0}$ , CLKOUT, FLAG11–0, REDY,  $\overline{HBG}$ ,  $\overline{BMS}$ ,  $\overline{BR6-1}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{SDWE}$ , DQM,  $\overline{SDCLKx}$ ,  $\overline{SDCKE}$ , SDA10, BRST.

<sup>10</sup>Applies to three-statable pins with 20 k $\Omega$  pull-ups:  $\overline{RD}$ ,  $\overline{WR}$ ,  $\overline{DMAG1}$ ,  $\overline{DMAG2}$ ,  $\overline{PA}$ .

<sup>11</sup>Applies to three-statable pins with 50 k $\Omega$  internal pull-ups: DxA, DxB, SCLKx, SPICLK.,  $\overline{EMU}$ , MISO, MOSI

<sup>12</sup>Applies to three-statable pins with 50 k $\Omega$  internal pull-downs: LxDAT7–0 (below Revision 1.2), LxCLK, LxACK. Use IOZHPD2 for Rev. 1.2 and higher.

<sup>13</sup>Applies to three-statable pins with 20 k $\Omega$  internal pull-downs: LxDAT7-0 (Revision 1.2 and higher).

<sup>14</sup>The test program used to measure  $I_{DDINPEAK}$  represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified. For more information, see “Power Dissipation” on Page 21.

<sup>15</sup>Current numbers are for V<sub>DDINT</sub> and AVDD supplies combined.

<sup>16</sup> $I_{DDINHIG}$  is a composite average based on a range of high activity code. See Power Dissipation on Page 21.

<sup>17</sup> $I_{DDINLOW}$  is a composite average based on a range of low activity code. See Power Dissipation on Page 21.

<sup>18</sup>Idle denotes ADSP-21161N state during execution of IDLE instruction. See Power Dissipation on Page 21.

<sup>19</sup>Characterized, but not tested.

<sup>20</sup>Applies to all signal pins.

<sup>21</sup>Guaranteed, but not tested.

## ABSOLUTE MAXIMUM RATINGS

Internal (Core) Supply Voltage (V <sub>DDINT</sub> ) <sup>1</sup> . . .	–0.3 V to +2.2 V
Analog (PLL) Supply Voltage (AV <sub>DD</sub> ) <sup>1</sup> . . . .	–0.3 V to +2.2 V
External (I/O) Supply Voltage (V <sub>DDEXT</sub> ) <sup>1</sup> . . .	–0.3 V to +4.6 V
Input Voltage <sup>1</sup> . . . . .	–0.5 V to V <sub>DDEXT</sub> + 0.5 V
Output Voltage Swing <sup>1</sup> . . . . .	–0.5 V to V <sub>DDEXT</sub> + 0.5 V
Load Capacitance <sup>1</sup> . . . . .	.200 pF
Storage Temperature Range <sup>1</sup> . . . . .	–65°C to +150°C

<sup>1</sup>Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD SENSITIVITY

### CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-21161N features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# ADSP-21161N

## TIMING SPECIFICATIONS

The ADSP-21161N's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the DSP uses an internal phase-locked loop (PLL). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the DSP's internal clock (the clock source for the external port logic and I/O pads).

The ADSP-21161N's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, link ports, serial ports, and external port (as required for read/write strobes in asynchronous access mode). During reset, program the ratio between the DSP's internal clock frequency and external (CLKIN) clock frequency with the CLK\_CFG1-0

and CLKDBL pins. Even though the internal clock is the clock source for the external port, it behaves as described in the Clock Rate Ratio chart in Table 3 on Page 17. To determine switching frequencies for the serial and link ports, divide down the internal clock, using the programmable divider control of each port (DIVx for the serial ports and LxCLKD for the link ports).

Note the following definitions of various clock periods that are a function of CLKIN and the appropriate ratio control.

Figure 10 enables Core-to-CLKIN ratios of 2:1, 3:1, 4:1, 6:1, and 8:1 with external oscillator or crystal. It also shows support for CLKOUT-to-CLKIN ratios of 1:1 and 2:1.

**Table 5. CLKOUT and CCLK Clock Generation Operation**

Timing Requirements	Description <sup>1</sup>	Calculation
CLKIN	Input Clock	$1/t_{CK}$
CLKOUT	External Port System Clock	$1/t_{CKOP}$
PLLICK	PLL Input Clock	$1/t_{PLLIN}$
CCLK	Core Clock	$1/t_{CCLK}$
$t_{CK}$	CLKIN Clock Period	$1/CLKIN$
$t_{CCLK}$	(Processor) Core Clock Period	$1/CCLK$
$t_{LCLK}$	Link Port Clock Period	$(t_{CCLK}) \times LR$
$t_{SCLK}$	Serial Port Clock Period	$(t_{CCLK}) \times SR$
$t_{SDK}$	SDRAM Clock Period	$(t_{CCLK}) \times SDCKR$
$t_{SPICLK}$	SPI Clock Period	$(t_{CCLK}) \times SPIR$

<sup>1</sup>where:

- LR = link port-to-core clock ratio (1, 2, 3, or 1:4, determined by LxCLKD)
- SR = serial port-to-core clock ratio (wide range, determined by CLKDIV)
- SDCKR = SDRAM-to-Core Clock Ratio (1:1 or 1:2, determined by SDCTL register)
- SPIR = SPI-to-Core Clock Ratio (wide range, determined by SPICL register)
- LCLK = Link Port Clock
- SCLK = Serial Port Clock
- SDK = SDRAM Clock
- SPICLK = SPI Clock

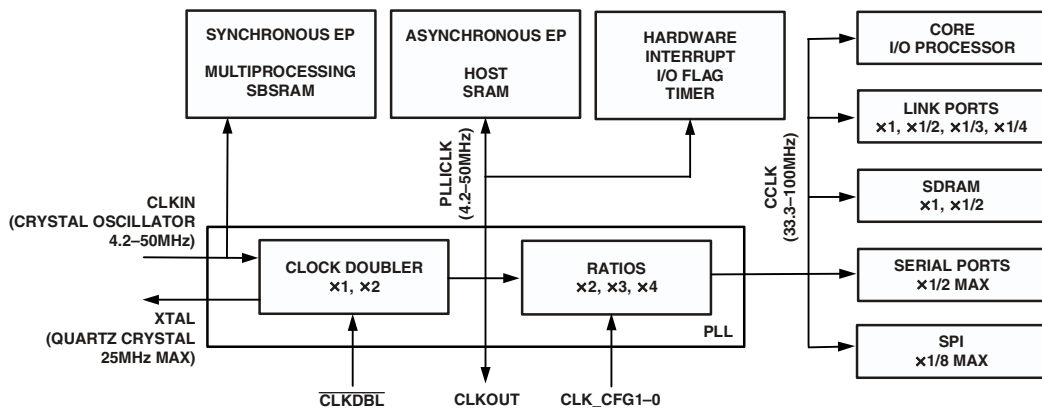


Figure 10. Core Clock and System Clock Relationship to CLKIN

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times.

See [Figure 40 on Page 51](#) under Test Conditions for voltage reference levels.

Switching characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

### Power Dissipation

Total power dissipation has two components: one due to internal circuitry and one due to the switching of external output drivers.

Internal power dissipation depends on the instruction execution sequence and the data operands involved. Using the current specifications ( $I_{DDINPEAK}$ ,  $I_{DDINHIG}$ ,  $I_{DDINLOW}$ ,  $I_{DDIDLE}$ ) from the Electrical Characteristics [on Page 18](#) and the current-versus-operation information in [Table 6](#), the programmer can estimate the ADSP-21161N's internal power supply ( $V_{DDINT}$ ) input current for a specific application, according to the following formula:

$$\frac{\% Peak \times I_{DDINPEAK} + \% High \times I_{DDINHIG} + \% Low \times I_{DDINLOW} + \% Idle \times I_{DDIDLE}}{I_{DDINT}}$$

**Table 6. Operation Types Versus Input Current**

Operation	Peak Activity <sup>1</sup> ( $I_{DDINPEAK}$ )	High Activity <sup>1</sup> ( $I_{DDINHIG}$ )	Low Activity <sup>1</sup> ( $I_{DDINLOW}$ )
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core Memory Access <sup>2</sup>	2 per $t_{CK}$ cycle (DM×64 and PM×64)	1 per $t_{CK}$ cycle (DM×64)	None
Internal Memory DMA	1 per 2 $t_{CCLK}$ cycles	1 per 2 $t_{CCLK}$ cycles	N/A
External Memory DMA	1 per external port cycle (×32)	1 per external port cycle (×32)	N/A
Data bit pattern for core memory access and DMA	Worst case	Random	N/A

<sup>1</sup>The state of the PEYEN bit (SIMD versus SISD mode) does not influence these calculations.

<sup>2</sup>These assume a 2:1 core clock ratio. For more information on ratios and clocks ( $t_{CK}$  and  $t_{CCLK}$ ), see the timing ratio definitions [on Page 20](#).

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- The number of output pins that switch during each cycle ( $O$ )
- The maximum frequency at which they can switch ( $f$ )
- Their load capacitance ( $C$ )
- Their voltage swing ( $V_{DD}$ )

and is calculated by:

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor package capacitance ( $C_{IN}$ ). The switching frequency includes driving the load high and then back low. At a maximum rate of  $1/t_{CK}$ , address and data pins can drive high and low, while writing to a SDRAM memory.

Example: Estimate  $P_{EXT}$  with the following assumptions:

- A system with one bank of external memory (32 bit)
- Two 1M × 16 SDRAM chips are used, each with a load of 10 pF (ignoring trace capacitance)

- External Data Memory writes can occur every cycle at a rate of  $1/t_{CK}$  with 50% of the pins switching
- The bus cycle time is 50 MHz
- The external SDRAM clock rate is 100 MHz
- Ignoring SDRAM refresh cycles
- Addresses are incremental and on the same page

The  $P_{EXT}$  equation is calculated for each class of pins that can drive, as shown in [Table 7](#).

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + P_{INT} + P_{PLL}$$

Where:

$P_{EXT}$  is from [Table 7](#).

$P_{INT}$  is  $I_{DDINT} \times 1.8$  V, using the calculation  $I_{DDINT}$  listed in [Power Dissipation on Page 21](#).

$P_{PLL}$  is  $AI_{DD} \times 1.8$  V, using the value for  $AI_{DD}$  listed in the Electrical Characteristics [on Page 18](#).

# ADSP-21161N

**Table 7. External Power Calculations (3.3 V Device)**

Pin Type	Number of Pins	% Switching	$\times C$	$\times f$	$\times V_{DD}^2$	$= P_{EXT}$
Address	11	20	24.7 pF	50 MHz	10.9 V	= 0.030 W
$\overline{MSx}$	4	0	24.7 pF	N/A	10.9 V	= 0.000 W
$\overline{SDWE}$	1	0	24.7 pF	N/A	10.9 V	= 0.000 W
Data	32	50	14.7 pF	50 MHz	10.9 V	= 0.128 W
SDCLK0	1	100	24.7 pF	100 MHz	10.9 V	= 0.027 W
						$P_{EXT} = 0.185 \text{ W}$

Note that the conditions causing a worst-case  $P_{EXT}$  are different from those causing a worst-case  $P_{INT}$ . Maximum  $P_{INT}$  cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

**Power-Up Sequencing – Silicon Revision 0.3, 1.0, 1.1**  
The timing requirements for DSP startup for silicon revision 0.3, 1.0, or 1.1 are given in Table 8.

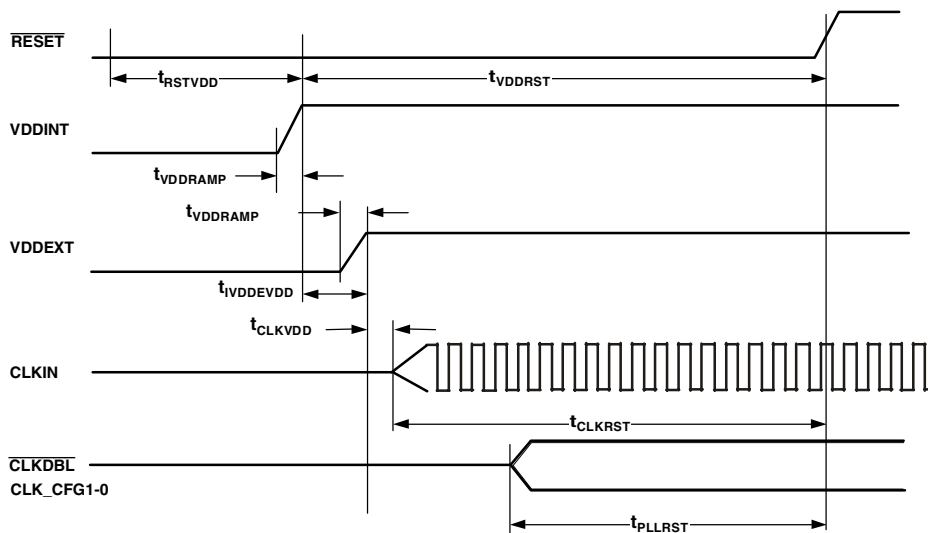
**Table 8. Power-Up Sequencing for Revisions 0.3, 1.0, and 1.1 (DSP Startup)**

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
$t_{RSTVDD}$	$\overline{RESET}$ Low Before $V_{DDINT}/V_{DDEXT}$ on	0		ns
$t_{VDDRAMP}$	$V_{DDINT}/V_{DDEXT}$ Voltage Ramp Rate <sup>1</sup>	0.0009	9	V/ $\mu$ s
$t_{IVDDEVD}$	$V_{DDINT}$ on Before $V_{DDEXT}$	-50	+200	ms
$t_{CLKVDD}$	CLKIN Valid After $V_{DDINT}/V_{DDEXT}$ Valid	0	200	ms
$t_{VDDRST}$	$V_{DDINT}/V_{DDEXT}$ Valid Before $\overline{RESET}$ Deasserted <sup>2</sup>	100		$\mu$ s
$t_{CLKRST}$	CLKIN Valid Before $\overline{RESET}$ Deasserted <sup>3</sup>	100		$\mu$ s
$t_{PLLRST}$	PLL Control Setup Before $\overline{RESET}$ Deasserted	20		$\mu$ s

<sup>1</sup>The minimum 0.9 V/ms is based on the slowest allowable ramp-up time (2 ms) for  $V_{DDINT}$  to ramp from 0 volts to 1.8 volts and (3.6 ms) for  $V_{DDEXT}$  to ramp from 0 volts to 3.3 volts.

<sup>2</sup>The minimum time of 0 ns assumes that  $V_{DDINT}$  and  $V_{DDEXT}$  power supplies are valid. The  $V_{DDINT}$  and  $V_{DDEXT}$  supplies must be fully ramped to their 1.8 and 3.3 volt rails before  $\overline{RESET}$  can be deasserted.

<sup>3</sup>The 100  $\mu$ s minimum assumes a stable CLKIN signal after meeting worst-case start-up timing of crystal oscillator circuits. Refer to the crystal oscillator manufacturer's data sheet for start-up time. A 25 ms maximum oscillator start-up time can be assumed if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal. 100  $\mu$ s is the minimum time required for the PLL to reliably lock to a valid (stable) CLKIN frequency.



**Figure 11. Power-Up Sequencing for Revisions 0.3, 1.0, and 1.1 (DSP Startup)**

## Power-Up Sequencing – Silicon Revision 1.2

The timing requirements for DSP startup for silicon with revision 1.2 are given in Table 9.

**Table 9. Power-Up Sequencing for Revision 1.2 (DSP Startup)**

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
$t_{RSTVDD}$	$\overline{RESET}$ Low Before $V_{DDINT}/V_{DDEXT}$ on		ns
$t_{IVDDEVDD}$	$V_{DDINT}$ on Before $V_{DDEXT}$		ms
$t_{CLKVDD}$	CLKIN Valid After $V_{DDINT}/V_{DDEXT}$ Valid <sup>1</sup>		ms
$t_{CLKRST}$	CLKIN Valid Before $\overline{RESET}$ Deasserted <sup>2</sup>		$\mu$ s
$t_{PLLST}$	PLL Control Setup Before $\overline{RESET}$ Deasserted <sup>3</sup>		$\mu$ s
$t_{WRST}$	Subsequent $\overline{RESET}$ Low Pulsewidth <sup>4</sup>		ns
<i>Switching Requirements</i>			
$t_{CORERST}$	DSP core reset deasserted after $\overline{RESET}$ deasserted		$4080t_{CK}$ <sup>3,5</sup>

<sup>1</sup> Valid  $V_{DDINT}/V_{DDEXT}$  assumes that the supplies are fully ramped to their 1.8 and 3.3 volt rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

<sup>2</sup> Assumes a stable CLKIN signal, after meeting worst-case start-up timing of crystal oscillators. Refer to the crystal oscillator manufacturer's data sheet for start-up time. Assume a 25 ms maximum oscillator start-up time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

<sup>3</sup> Based on CLKIN cycles

<sup>4</sup> Applies after the power-up sequence is complete. Subsequent resets require a minimum of 4 CLKIN cycles for  $\overline{RESET}$  to be held low in order to properly initialize and propagate default states at all I/O pins.

<sup>5</sup> The 4080 cycle count depends on  $t_{SRST}$  specification in Table 11. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4081 cycles maximum.

$\overline{RSTOUT}$  does not currently exist for ADSP-21161N revisions 0.3, 1.0, and 1.1. This new signal will be placed on one of the current no-connect pins: ball B15.

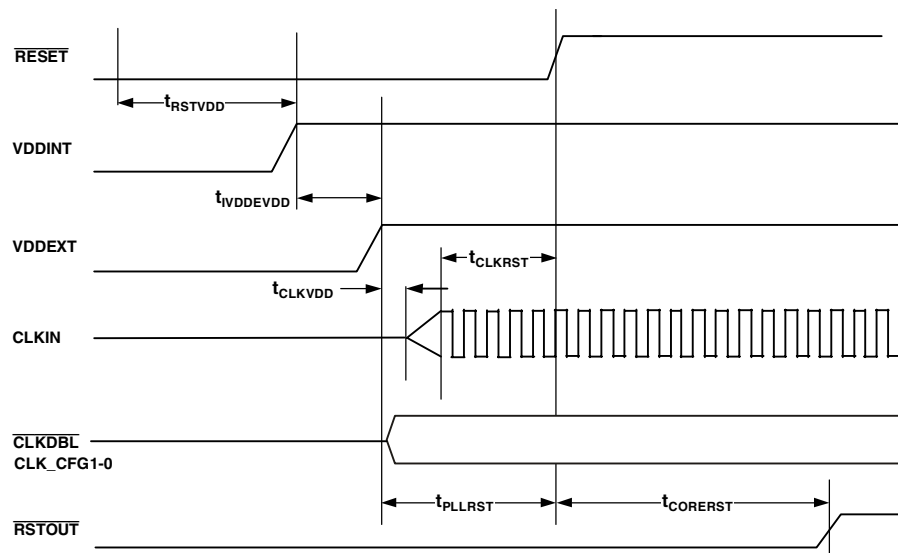


Figure 12. Power-Up Sequencing for Revision 1.2 (DSP Startup)

During the power-up sequence of the DSP, differences in the ramp-up rates and activation time between the two supplies can cause current to flow in the I/O ESD protection circuitry. To prevent damage to the ESD diode protection circuitry, Analog Devices recommends including a bootstrap Schottky diode.

The bootstrap Schottky diode is connected between the 1.8 V and 3.3 V power supplies as shown in Figure 13. It protects the ADSP-21161N from partially powering the 3.3 V supply. Including a Schottky diode will shorten the delay between the supply ramps and thus prevent damage to the ESD diode



# ADSP-21161N

protection circuitry. With this technique, if the 1.8 V rail rises ahead of the 3.3 V rail, the Schottky diode pulls the 3.3 V rail along with the 1.8 V rail.

## Clock Input

In systems that use multiprocessing or SBSRAM,  $\overline{\text{CLKDBL}}$  cannot be enabled nor can the systems use an external crystal as the CLKIN source.

Do not use CLKOUT as the clock source for the SBSRAM device. Using an external crystal in conjunction with  $\overline{\text{CLKDBL}}$  to generate a CLKOUT frequency is not supported. Negative hold times can result from the potential skew between CLKIN and CLKOUT.

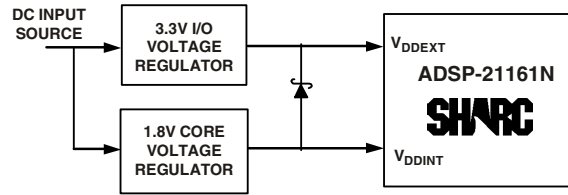
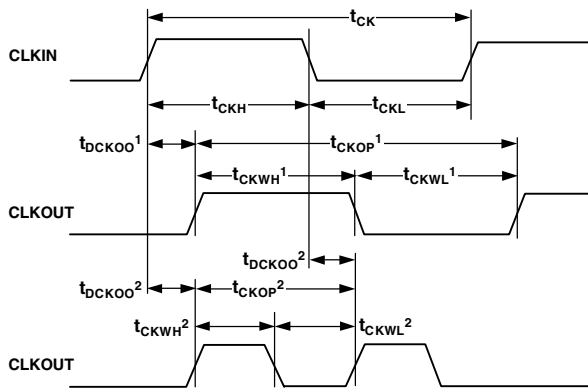


Figure 13. Dual Voltage Schottky Diode

Table 10. Clock Input

Parameter	100 MHz		Unit
	Min	Max	
<i>Timing Requirements</i>			
$t_{\text{CK}}$	CLKIN Period <sup>1</sup>		ns
$t_{\text{CKL}}$	CLKIN Width Low <sup>1</sup>		ns
$t_{\text{CKH}}$	CLKIN Width High <sup>1</sup>		ns
$t_{\text{CKRF}}$	CLKIN Rise/Fall (0.4 V–2.0 V)		ns
$t_{\text{CCLK}}$	CCLK Period		ns
<i>Switching Characteristics</i>			
$t_{\text{DCKOO}}$	CLKOUT Delay After CLKIN		ns
$t_{\text{CKOP}}$	CLKOUT Period		ns
$t_{\text{CKWH}}$	CLKOUT Width High		ns
$t_{\text{CKWL}}$	CLKOUT Width Low		ns

<sup>1</sup> CLKIN is dependent on the configuration of the CLKCFGx and  $\overline{\text{CLKDBL}}$  pins to achieve desired  $t_{\text{CCLK}}$ .



### NOTES:

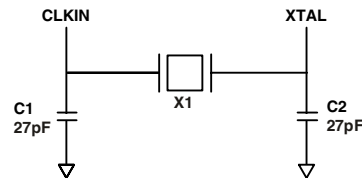
1. WHEN  $\overline{\text{CLKDBL}}$  IS DISABLED, ANY SPECIFICATION TO CLKIN APPLIES TO THE RISING EDGE, ONLY.
2. WHEN  $\overline{\text{CLKDBL}}$  IS ENABLED, ANY SPECIFICATION TO CLKIN APPLIES TO THE RISING OR FALLING EDGE.

Figure 14. Clock Input

## Clock Signals

The ADSP-21161N can use an external clock or a crystal. See CLKIN pin description. The programmer can configure the ADSP-21161N to use its internal clock generator by connecting

the necessary components to CLKIN and XTAL. Figure 15 shows the component connections used for a crystal operating in fundamental mode.



SUGGESTED COMPONENTS FOR 100MHz OPERATION:  
 ECLIPTEK EC2SM-25.000M (SURFACE MOUNT PACKAGE)  
 ECLIPTEK EC-25.000M (THROUGH-HOLE PACKAGE)  
 C1 = 27pF  
 C2 = 27pF

NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. THIS 25MHz CRYSTAL GENERATES A 100MHz CCLK AND A 50MHz EP CLOCK WITH  $\overline{\text{CLKDBL}}$  ENABLED AND A 2:1 PLL MULTIPLY RATIO.

Figure 15. 100 MHz Operation (Fundamental Mode Crystal)

## Reset

**Table 11. Reset**

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
$t_{WRST}$	$\overline{\text{RESET}}$ Pulsewidth Low <sup>1</sup>	$4t_{CK}$	ns
$t_{SRST}$	$\overline{\text{RESET}}$ Setup Before CLKIN High <sup>2</sup>	8.5	ns

<sup>1</sup>Applies after the power-up sequence is complete.

<sup>2</sup>Only required if multiple ADSP-21161Ns must come out of reset synchronous to CLKIN with program counters (PC) equal. Not required for multiple ADSP-21161Ns communicating over the shared bus (through the external port), because the bus arbitration logic synchronizes itself automatically after reset.

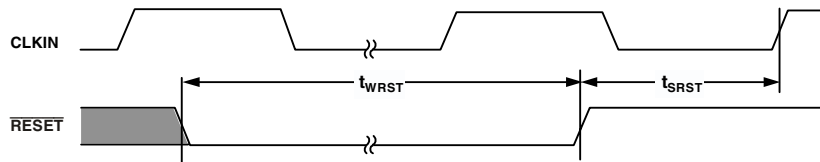


Figure 16. Reset

## Interrupts

**Table 12. Interrupts**

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
$t_{SIR}$	$\overline{\text{IRQ2-0}}$ Setup Before CLKIN <sup>1</sup>	6	ns
$t_{HIR}$	$\overline{\text{IRQ2-0}}$ Hold After CLKIN <sup>1</sup>	0	ns
$t_{IPW}$	$\overline{\text{IRQ2-0}}$ Pulsewidth <sup>2</sup>	$2 + t_{CKOP}$	ns

<sup>1</sup>Only required for  $\overline{\text{IRQx}}$  recognition in the following cycle.

<sup>2</sup>Applies only if  $t_{SIR}$  and  $t_{HIR}$  requirements are not met.

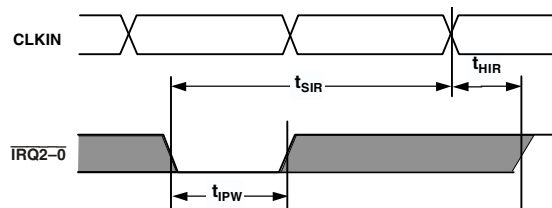


Figure 17. Interrupts

# ADSP-21161N

## Timer

Table 13. Timer

Parameter	Min	Max	Unit
<i>Switching Characteristic</i>			
$t_{DTEX}$ CLKIN to TIMEXP	1	7	ns

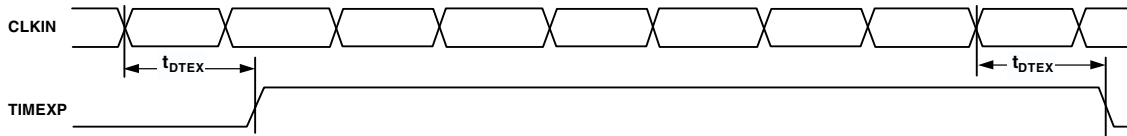


Figure 18. Timer

## Flags

Table 14. Flags

Parameter	Min	Max	Unit
<i>Timing Requirement</i>			
$t_{SFI}$ FLAG11-0 <sub>IN</sub> Setup Before CLKIN <sup>1</sup>	4		ns
$t_{HFI}$ FLAG11-0 <sub>IN</sub> Hold After CLKIN <sup>1</sup>	1		ns
$t_{DWRFI}$ FLAG11-0 <sub>IN</sub> Delay After $\overline{RD}/\overline{WR}$ Low <sup>1</sup>		12	ns
$t_{HFIWR}$ FLAG11-0 <sub>IN</sub> Hold After $\overline{RD}/\overline{WR}$ Deasserted <sup>1</sup>	0		ns
<i>Switching Characteristics</i>			
$t_{DFO}$ FLAG11-0 <sub>OUT</sub> Delay After CLKIN		9	ns
$t_{HFO}$ FLAG11-0 <sub>OUT</sub> Hold After CLKIN	1		ns
$t_{DFOE}$ CLKIN to FLAG11-0 <sub>OUT</sub> Enable	1		ns
$t_{DFOD}$ CLKIN to FLAG11-0 <sub>OUT</sub> Disable		5	ns

<sup>1</sup> Flag inputs meeting these setup and hold times for instruction cycle N will affect conditional instructions in instruction cycle N+2.

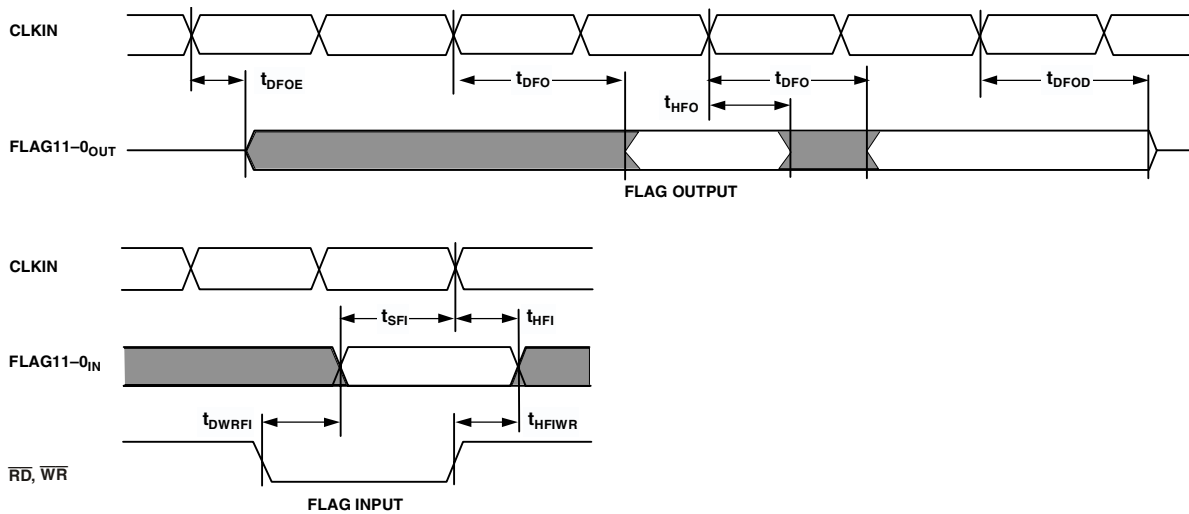


Figure 19. Flags

**Memory Read – Bus Master**

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21161N is the bus master accessing external memory space in asynchronous access mode.

**Table 15. Memory Read – Bus Master**

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
$t_{DAD}$ Address, Selects Delay to Data Valid <sup>1, 2</sup>		$t_{CKOP} - 0.25t_{CCLK} - 11 + W$	ns
$t_{DRLD}$ $\overline{RD}$ Low to Data Valid <sup>1</sup>		$0.75t_{CKOP} - 11 + W$	ns
$t_{HDA}$ Data Hold from Address, Selects <sup>3</sup>	0		ns
$t_{SDS}$ Data Setup to $\overline{RD}$ High	8		ns
$t_{HDRH}$ Data Hold from $\overline{RD}$ High <sup>3</sup>	1		ns
$t_{DAAK}$ ACK Delay from Address, Selects <sup>2, 4</sup>		$t_{CKOP} - 0.5t_{CCLK} - 12 + W$	ns
$t_{DSAK}$ ACK Delay from $\overline{RD}$ Low <sup>4</sup>		$t_{CKOP} - 0.75t_{CCLK} - 11 + W$	ns
$t_{SAKC}$ ACK Setup to CLKIN <sup>4</sup>	$0.5t_{CCLK} + 3$		ns
$t_{HAKC}$ ACK Hold After CLKIN	1		ns
<i>Switching Characteristics</i>			
$t_{DRHA}$ Address Selects Hold After $\overline{RD}$ High	$0.25t_{CCLK} - 1 + H$		ns
$t_{DARL}$ Address Selects to $\overline{RD}$ Low <sup>2</sup>	$0.25t_{CCLK} - 3$		ns
$t_{RW}$ $\overline{RD}$ Pulsewidth	$t_{CKOP} - 0.5t_{CCLK} - 1 + W$		ns
$t_{RWR}$ $\overline{RD}$ High to $\overline{WR}$ , $\overline{RD}$ , $\overline{DMAGx}$ Low	$0.5t_{CCLK} - 1 + HI$		ns

$W = (\text{number of wait states specified in WAIT register}) \times t_{CKOP}$ .

$HI = t_{CKOP}$  (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise  $HI = 0$ ).

$H = t_{CKOP}$  (if an address hold cycle occurs as specified in WAIT register; otherwise  $H = 0$ ).

<sup>1</sup>Data Delay/Setup: User must meet  $t_{DAD}$ ,  $t_{DRLD}$ , or  $t_{SDS}$ .

<sup>2</sup>The falling edge of  $\overline{MSx}$ ,  $\overline{BMS}$  is referenced.

<sup>3</sup>Data Hold: User must meet  $t_{HDA}$  or  $t_{HDRH}$  in asynchronous access mode. See [Example System Hold Time Calculation on Page 51](#) for the calculation of hold times given capacitive and dc loads.

<sup>4</sup>ACK Delay/Setup: User must meet  $t_{DAAK}$ ,  $t_{DSAK}$ , or  $t_{SAKC}$  for deassertion of ACK (Low); all three specifications must be met for assertion of ACK (High).

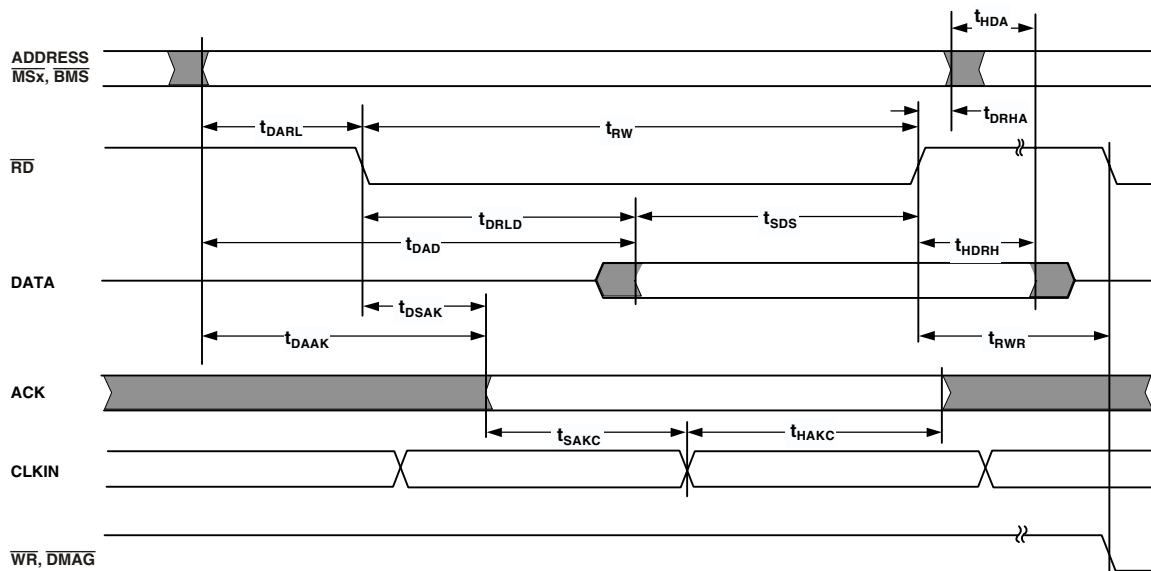


Figure 20. Memory Read – Bus Master

# ADSP-21161N

## Memory Write – Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21161N is the bus master accessing external memory space in asynchronous access mode.

**Table 16. Memory Write – Bus Master**

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
$t_{DAAK}$ ACK Delay from Address, Selects <sup>1,2</sup>		$t_{CKOP}-0.5t_{CCLK}-12+W$	ns
$t_{DSAK}$ ACK Delay from $\overline{WR}$ Low <sup>1</sup>		$t_{CKOP}-0.75t_{CCLK}-11+W$	ns
$t_{SAKC}$ ACK Setup to CLKIN <sup>1</sup>	$0.5t_{CCLK}+3$		ns
$t_{HAKC}$ ACK Hold After CLKIN <sup>1</sup>	1		ns
<i>Switching Characteristics</i>			
$t_{DAWH}$ Address, Selects to $\overline{WR}$ Deasserted <sup>2</sup>	$t_{CKOP}-0.25t_{CCLK}-3+W$		ns
$t_{DAWL}$ Address, Selects to $\overline{WR}$ Low <sup>2</sup>	$0.25t_{CCLK}-3$		ns
$t_{WW}$ $\overline{WR}$ Pulsewidth	$t_{CKOP}-0.5t_{CCLK}-1+W$		ns
$t_{DDWH}$ Data Setup Before $\overline{WR}$ High	$t_{CKOP}-0.25t_{CCLK}-13.5+W$		ns
$t_{DWHa}$ Address Hold After $\overline{WR}$ Deasserted	$0.25t_{CCLK}-1+H$		ns
$t_{DWHd}$ Data Hold After $\overline{WR}$ Deasserted	$0.25t_{CCLK}-1+H$		ns
$t_{DATRWH}$ Data Disable After $\overline{WR}$ Deasserted <sup>3</sup>	$0.25t_{CCLK}-2+H$	$0.25t_{CCLK}+2.5+H$	ns
$t_{WWR}$ $\overline{WR}$ High to $\overline{WR}$ , $\overline{RD}$ , $\overline{DMAGx}$ Low	$0.5t_{CCLK}-1.25+HI$		ns
$t_{DDWR}$ Data Disable Before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CCLK}-3+I$		ns
$t_{WDE}$ $\overline{WR}$ Low to Data Enabled	$-0.25t_{CCLK}-1$		ns

$W$  = (number of wait states specified in WAIT register)  $\times t_{CKOP}$ .

$H$  =  $t_{CKOP}$  (if an address hold cycle occurs, as specified in WAIT register; otherwise  $H = 0$ ).

$HI$  =  $t_{CKOP}$  (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise  $HI = 0$ ).

$I$  =  $t_{CKOP}$  (if a bus idle cycle occurs, as specified in WAIT register; otherwise  $I = 0$ ).

<sup>1</sup> ACK Delay/Setup: User must meet  $t_{DAAK}$  or  $t_{DSAK}$  or  $t_{SAKC}$  for deassertion of ACK (Low); all three specifications must be met for assertion of ACK (High).

<sup>2</sup> The falling edge of MSx, BMS is referenced.

<sup>3</sup> See [Example System Hold Time Calculation on Page 51](#) for calculation of hold times given capacitive and dc loads.

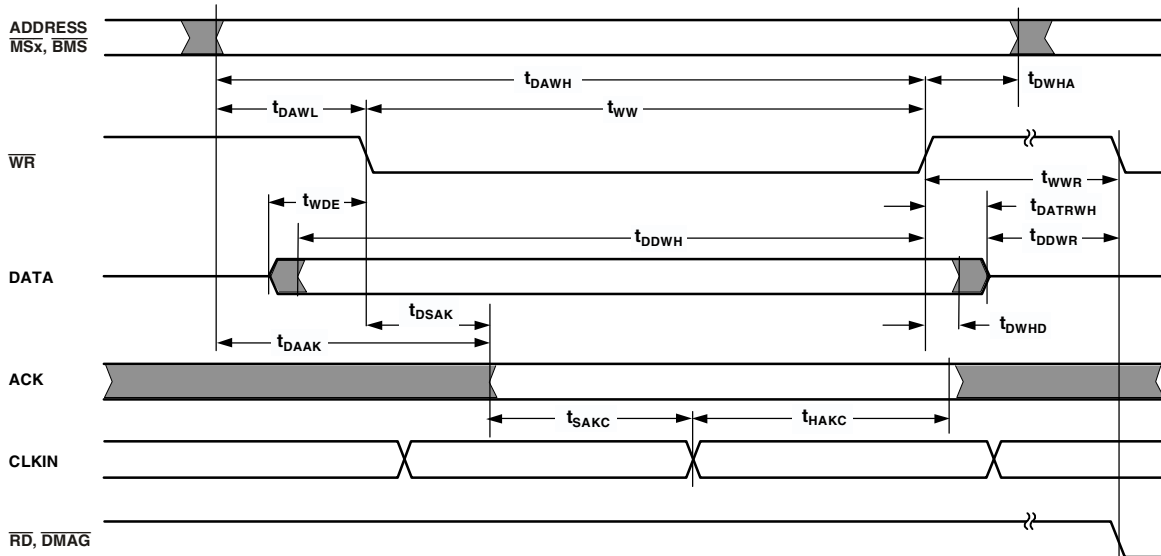


Figure 21. Memory Write – Bus Master



### Synchronous Read/Write – Bus Master

Use these specifications for interfacing to external memory systems that require CLKIN, relative to timing or for accessing a slave ADSP-21161N (in multiprocessor memory space). When accessing a slave ADSP-21161N, these switching characteristics

must meet the slave's timing requirements for synchronous read/writes (see [Synchronous Read/Write – Bus Slave on Page 30](#)). The slave ADSP-21161N must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

**Table 17. Synchronous Read/Write – Bus Master**

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
$t_{SSDATI}$	Data Setup Before CLKIN	5.5		ns
$t_{HSDATI}$	Data Hold After CLKIN	1		ns
$t_{SACKC}$	ACK Setup Before CLKIN	$0.5t_{CCLK}+3$		ns
$t_{HACKC}$	ACK Hold After CLKIN	1		ns
<i>Switching Characteristics</i>				
$t_{DADD0}$	Address, $\overline{MSx}$ , $\overline{BMS}$ , BRST, Delay After CLKIN		10	ns
$t_{HADD0}$	Address, $\overline{MSx}$ , $\overline{BMS}$ , BRST, Hold After CLKIN	1.5		ns
$t_{DRDO}$	$\overline{RD}$ High Delay After CLKIN	$0.25t_{CCLK}-1$	$0.25t_{CCLK}+9$	ns
$t_{DWRO}$	$\overline{WR}$ High Delay After CLKIN	$0.25t_{CCLK}-1$	$0.25t_{CCLK}+9$	ns
$t_{DRWL}$	$\overline{RD}/\overline{WR}$ Low Delay After CLKIN	$0.25t_{CCLK}-1$	$0.25t_{CCLK}+9$	ns
$t_{DDATO}$	Data Delay After CLKIN		12.5	ns
$t_{HDATA}$	Data Hold After CLKIN	1.5		ns

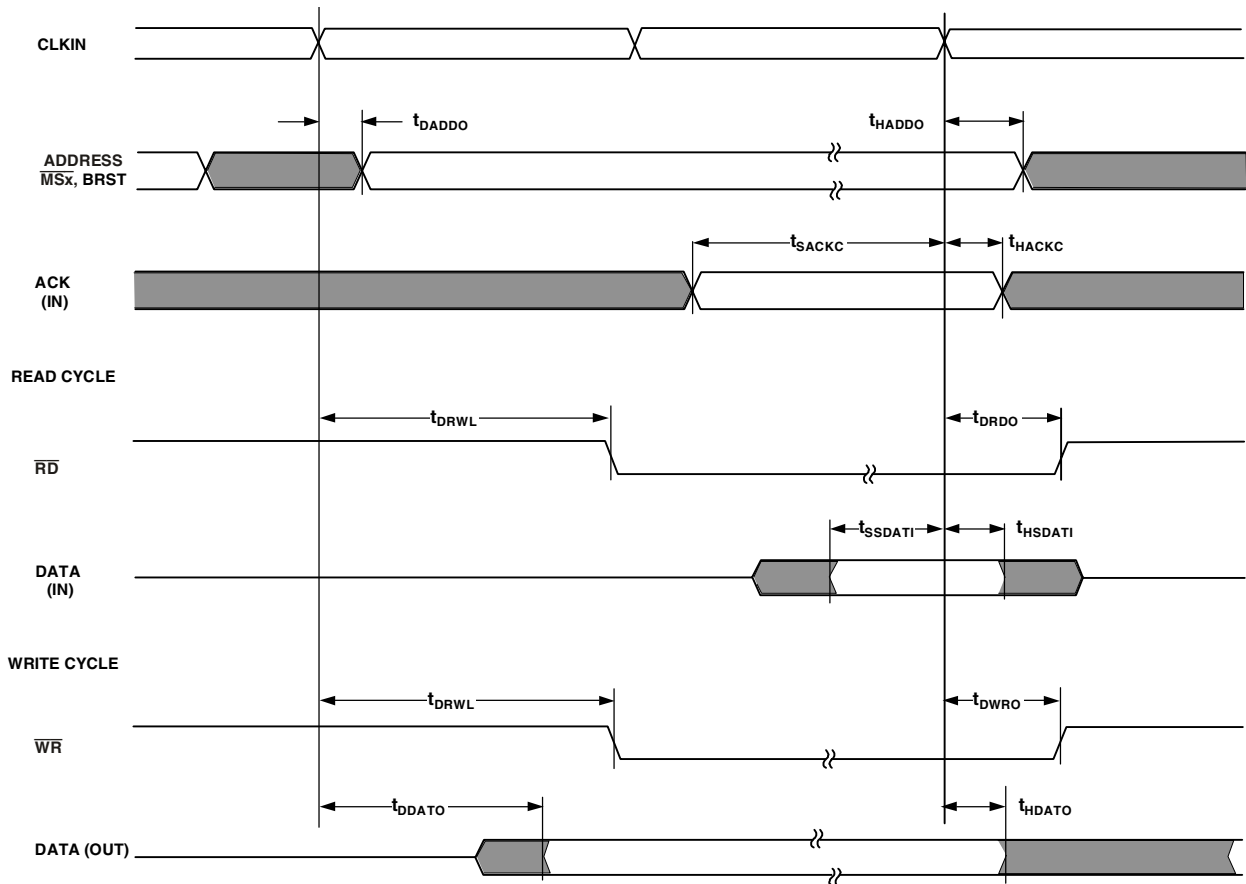


Figure 22. Synchronous Read/Write – Bus Master

# ADSP-21161N

## Synchronous Read/Write – Bus Slave

Use these specifications for ADSP-21161N bus master accesses of a slave's IOP registers in multiprocessor memory space. The bus master must meet these (bus slave) timing requirements.

**Table 18. Synchronous Read/Write – Bus Slave**

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
$t_{SADDI}$	Address, BRST Setup Before CLKIN	5		ns
$t_{HADDI}$	Address, BRST Hold After CLKIN	1		ns
$t_{SRWI}$	$\overline{RD}/\overline{WR}$ Setup Before CLKIN	5		ns
$t_{HRWI}$	$\overline{RD}/\overline{WR}$ Hold After CLKIN	1		ns
$t_{SSDATI}$	Data Setup Before CLKIN	5.5		ns
$t_{HSDATI}$	Data Hold After CLKIN	1		ns
<i>Switching Characteristics</i>				
$t_{DDATO}$	Data Delay After CLKIN		12.5	ns
$t_{HDATO}$	Data Hold After CLKIN	1.5		ns
$t_{DACKC}$	ACK Delay After CLKIN		10	ns
$t_{HACKO}$	ACK Hold After CLKIN	1.5		ns

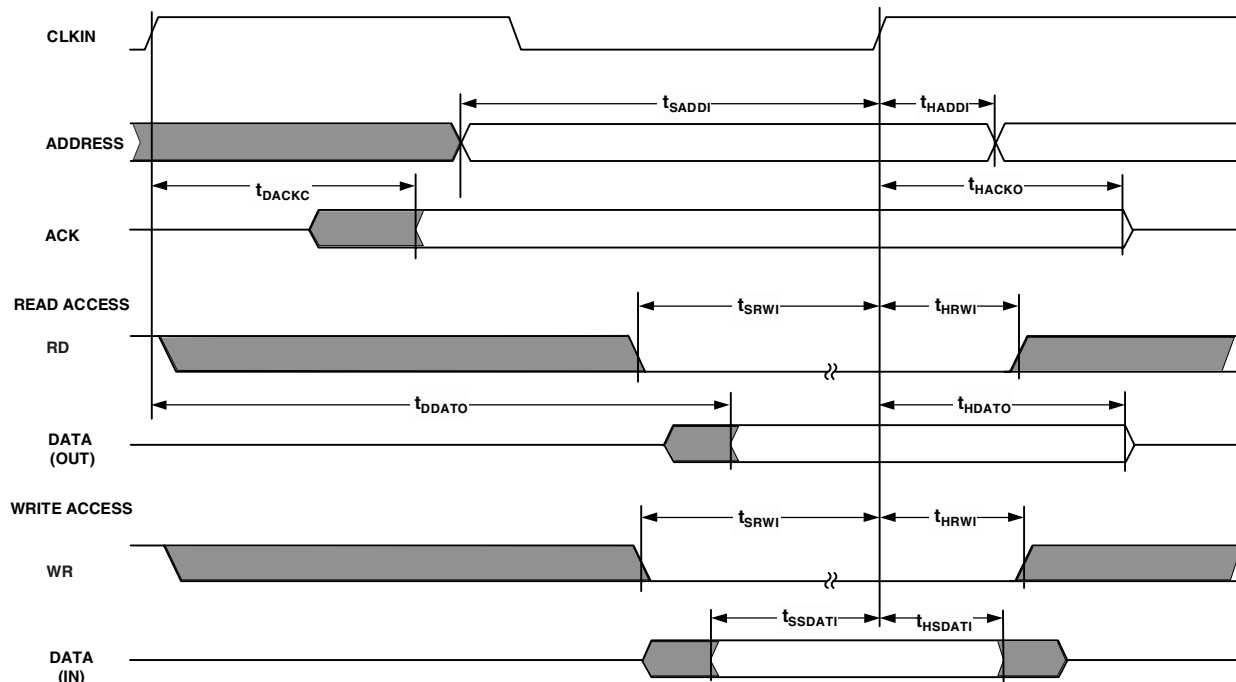


Figure 23. Synchronous Read/Write – Bus Slave

**Host Bus Request**

Use these specifications for asynchronous host bus requests of an ADSP-21161N ( $\overline{\text{HBR}}$ ,  $\overline{\text{HBG}}$ ).

**Table 19. Host Bus Request**

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
$t_{\text{HBGRCSV}}$	$\overline{\text{HBG}}$ Low to $\overline{\text{RD}}/\overline{\text{WR}}/\overline{\text{CS}}$ Valid		19	ns
$t_{\text{SHBRI}}$	$\overline{\text{HBR}}$ Setup Before CLKIN <sup>1</sup>	6		ns
$t_{\text{HHBRI}}$	$\overline{\text{HBR}}$ Hold After CLKIN <sup>1</sup>	1		ns
$t_{\text{SHBGI}}$	$\overline{\text{HBG}}$ Setup Before CLKIN	6		ns
$t_{\text{HHBGI}}$	$\overline{\text{HBG}}$ Hold After CLKIN	1		ns
<i>Switching Characteristics</i>				
$t_{\text{DHBGO}}$	$\overline{\text{HBG}}$ Delay After CLKIN		7	ns
$t_{\text{HHBGO}}$	$\overline{\text{HBG}}$ Hold After CLKIN	1.5		ns
$t_{\text{DRDYCS}}$	REDY (O/D) or (A/D) Low from $\overline{\text{CS}}$ and $\overline{\text{HBR}}$ Low <sup>2</sup>		10	ns
$t_{\text{TRDYHG}}$	REDY (O/D) Disable or REDY (A/D) High from $\overline{\text{HBG}}$ <sup>2</sup>	$t_{\text{CKOP}}+14$		ns
$t_{\text{ARDYTR}}$	REDY (A/D) Disable from $\overline{\text{CS}}$ or $\overline{\text{HBR}}$ High <sup>2</sup>		11	ns

<sup>1</sup>Only required for recognition in the current cycle.

<sup>2</sup>(O/D) = open drain, (A/D) = active drive.

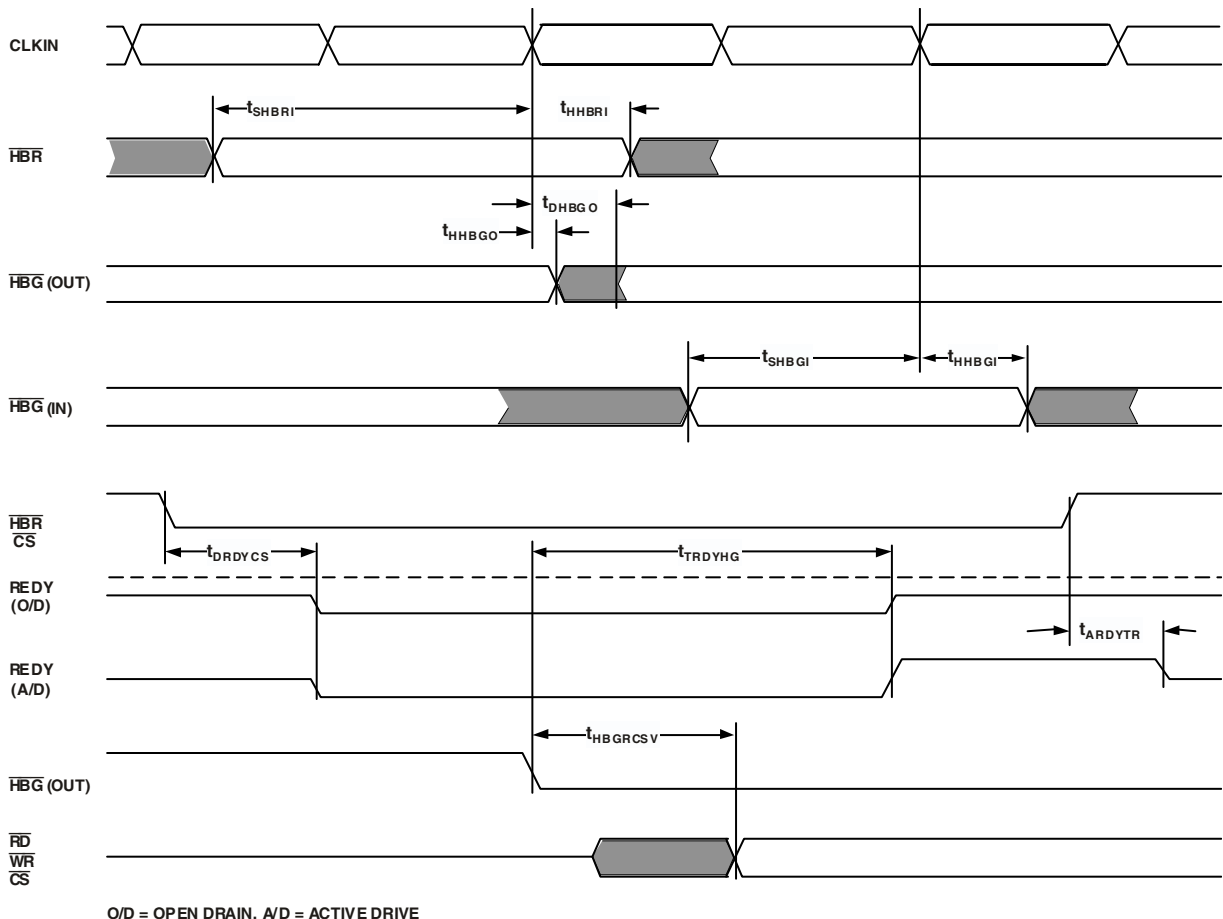


Figure 24. Host Bus Request

# ADSP-21161N

## Multiprocessor Bus Request

Use these specifications for passing of bus mastership between multiprocessor ADSP-21161Ns ( $\overline{\text{BRx}}$ ).

**Table 20. Multiprocessor Bus Request**

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
$t_{\text{SBRI}}$	$\overline{\text{BRx}}$ , Setup Before CLKIN High	9		ns
$t_{\text{HBRI}}$	$\overline{\text{BRx}}$ , Hold After CLKIN High	0.5		ns
$t_{\text{SPAI}}$	$\overline{\text{PA}}$ Setup Before CLKIN High	9		ns
$t_{\text{HPAI}}$	$\overline{\text{PA}}$ Hold After CLKIN High	1		ns
$t_{\text{SRPBAI}}$	RPBA Setup Before CLKIN High	6		ns
$t_{\text{HRPBAI}}$	RPBA Hold After CLKIN High	2		ns
<i>Switching Characteristics</i>				
$t_{\text{DBRO}}$	$\overline{\text{BRx}}$ Delay After CLKIN High		8	ns
$t_{\text{HBRO}}$	$\overline{\text{BRx}}$ Hold After CLKIN High	1.0		ns
$t_{\text{DPASO}}$	$\overline{\text{PA}}$ Delay After CLKIN High, Slave		8	ns
$t_{\text{TRPAS}}$	$\overline{\text{PA}}$ Disable After CLKIN High, Slave	1.5		ns
$t_{\text{DPAMO}}$	$\overline{\text{PA}}$ Delay After CLKIN High, Master		$0.25t_{\text{CLK}}+9$	ns
$t_{\text{PATR}}$	$\overline{\text{PA}}$ Disable Before CLKIN High, Master	$0.25t_{\text{CLK}}-5$		ns

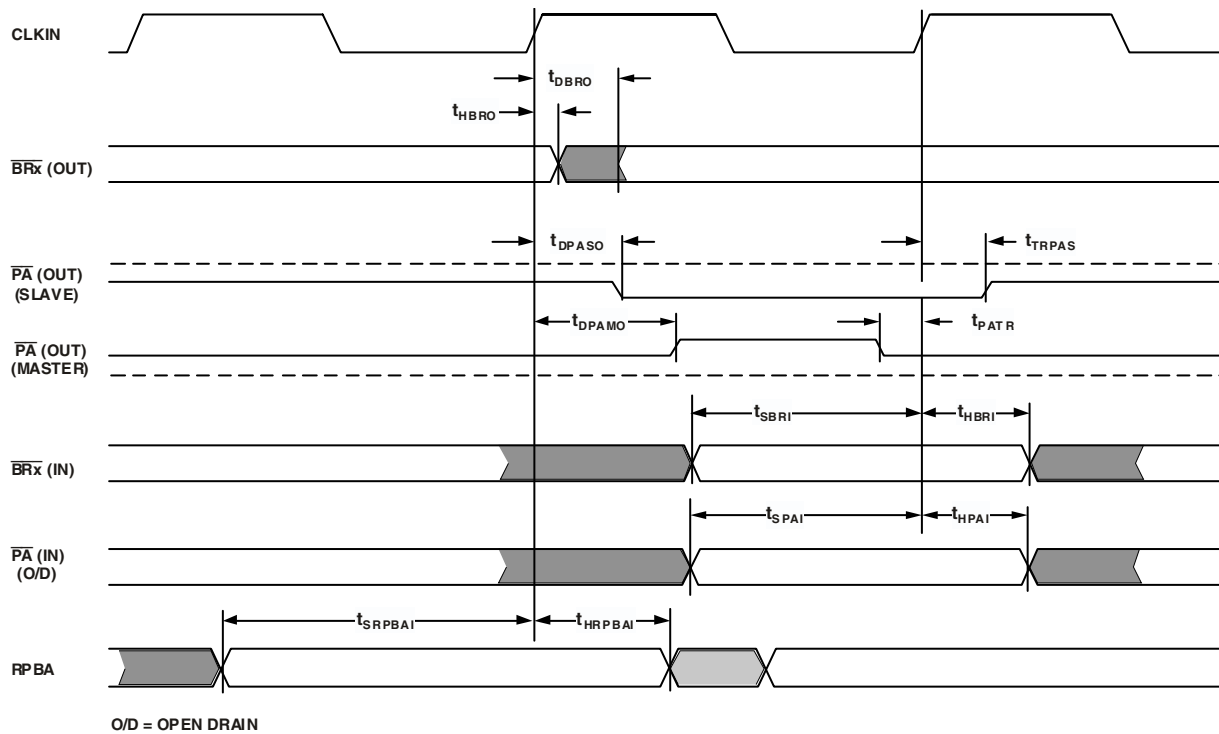


Figure 25. Multiprocessor Bus Request

### Asynchronous Read/Write – Host to ADSP-21161N

Use these specifications for asynchronous host processor accesses of an ADSP-21161N, after the host has asserted  $\overline{CS}$  and  $\overline{HBR}$  (low). After  $\overline{HBG}$  is returned by the ADSP-21161N, the host can drive the  $\overline{RD}$  and  $\overline{WR}$  pins to access the ADSP-21161N's IOP registers.  $\overline{HBR}$  and  $\overline{HBG}$  are assumed low for this timing.

Although the DSP will recognize  $\overline{HBR}$  asserted before reset, a  $\overline{HBG}$  will not be returned by the DSP until after reset is deasserted and the DSP completes bus synchronization.

**Note:** Host internal memory access is not supported.

**Table 21. Read Cycle**

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
$t_{SADRDL}$ Address Setup and $\overline{CS}$ Low Before $\overline{RD}$ Low	0		ns
$t_{HADRDH}$ Address Hold and $\overline{CS}$ Hold Low After $\overline{RD}$	2		ns
$t_{WRWH}$ $\overline{RD}/\overline{WR}$ High Width	3.5		ns
$t_{DRDHRDY}$ $\overline{RD}$ High Delay After REDY (O/D) Disable	0		ns
$t_{DRDHRDY}$ $\overline{RD}$ High Delay After REDY (A/D) Disable	0		ns
<i>Switching Characteristics</i>			
$t_{SDATRDY}$ Data Valid Before REDY Disable from Low	2		ns
$t_{DRDYRDL}$ REDY (O/D) or (A/D) Low Delay After $\overline{RD}$ Low		10	ns
$t_{RDYPRD}$ REDY (O/D) or (A/D) Low Pulsewidth for Read	$1.5t_{CCLK}$		ns
$t_{HDARWH}$ Data Disable After $\overline{RD}$ High	2	6	ns

**Table 22. Write Cycle**

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
$t_{SCSWRL}$ $\overline{CS}$ Low Setup Before $\overline{WR}$ Low	0		ns
$t_{HCSWRH}$ $\overline{CS}$ Low Hold After $\overline{WR}$ High	0		ns
$t_{SADWRH}$ Address Setup Before $\overline{WR}$ High	6		ns
$t_{HADWRH}$ Address Hold After $\overline{WR}$ High	2		ns
$t_{WWRL}$ $\overline{WR}$ Low Width	$t_{CCLK}+1$		ns
$t_{WRWH}$ $\overline{RD}/\overline{WR}$ High Width	3.5		ns
$t_{DWRHRDY}$ $\overline{WR}$ High Delay After REDY (O/D) or (A/D) Disable	0		ns
$t_{SDATWH}$ Data Setup Before $\overline{WR}$ High	5		ns
$t_{HDATWH}$ Data Hold After $\overline{WR}$ High	4		ns
<i>Switching Characteristics</i>			
$t_{DRDYWRL}$ REDY (O/D) or (A/D) Low Delay After $\overline{WR}/\overline{CS}$ Low <sup>1</sup>		11	ns
$t_{RDYPWR}$ REDY (O/D) or (A/D) Low Pulsewidth for Write <sup>1</sup>	12		ns

<sup>1</sup> Only when slave write FIFO is full.



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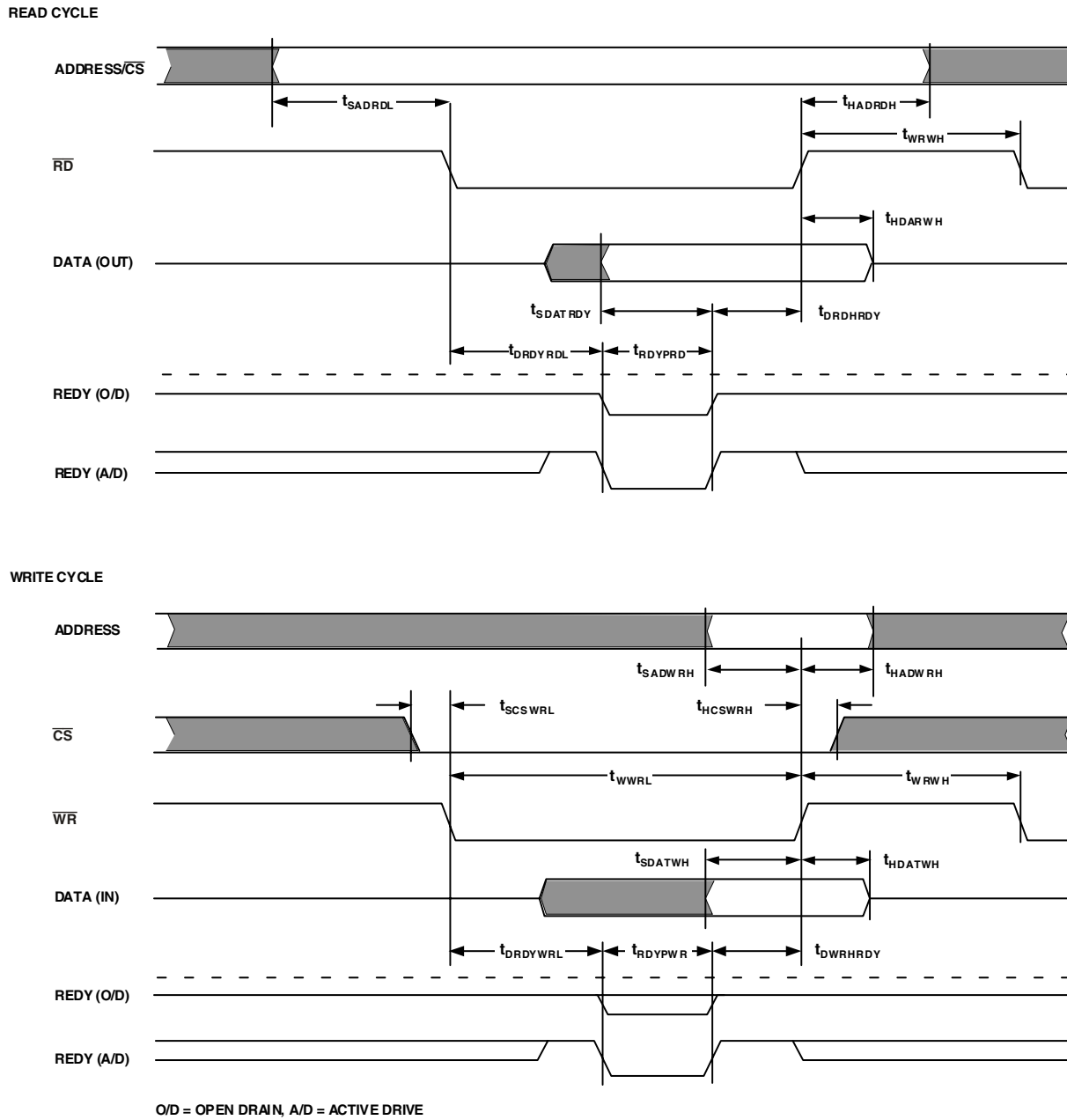


Figure 26. Asynchronous Read/Write – Host to ADSP-21161N

### Three-State Timing – Bus Master, Bus Slave

These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the SBT $\overline{S}$  pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the SBT $\overline{S}$  pin.

During reset, the DSP will not respond to  $\overline{SBTS}$ ,  $\overline{HBR}$ , and MMS accesses. Although the DSP will recognize  $\overline{HBR}$  asserted before reset, a  $\overline{HBG}$  will not be returned by the DSP until after reset is deasserted and the DSP completes bus synchronization.

**Table 23. Three-State Timing – Bus Master, Bus Slave**

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
t $\overline{S}$ TSCK	$\overline{SBTS}$ Setup Before CLKIN	6		ns
t $\overline{H}$ TSCK	$\overline{SBTS}$ Hold After CLKIN	2		ns
<i>Switching Characteristics</i>				
t $\overline{M}$ IENA	Address/Select Enable After CLKIN High	1.5	9	ns
t $\overline{M}$ IENS	Strobes Enable After CLKIN High <sup>1</sup>	-1.5	+9	ns
t $\overline{M}$ IENHG	$\overline{HBG}$ Enable After CLKIN	1.5	9	ns
t $\overline{M}$ ITRA	Address/Select Disable After CLKIN High	-0.5t $\overline{C}$ KOP-20	-0.5t $\overline{C}$ KOP-15	ns
t $\overline{M}$ ITRS	Strobes Disable After CLKIN High	t $\overline{C}$ KOP-0.25t $\overline{C}$ CLK-17	t $\overline{C}$ KOP-0.25t $\overline{C}$ CLK-12.5	ns
t $\overline{M}$ ITRHG	$\overline{HBG}$ Disable After CLKIN <sup>2</sup>	0.5t $\overline{C}$ KOP+N×t $\overline{C}$ CLK-20	0.5t $\overline{C}$ KOP+N×t $\overline{C}$ CLK-15	ns
t $\overline{D}$ ATEN	Data Enable After CLKIN <sup>3</sup>	1.5	10	ns
t $\overline{D}$ ATTR	Data Disable After CLKIN <sup>3</sup>	1.5	6	ns
t $\overline{A}$ CKEN	ACK Enable After CLKIN High	1.5	9	ns
t $\overline{A}$ CKTR	ACK Disable After CLKIN High	0.2	5	ns
t $\overline{C}$ DCEN	CLKOUT Enable After CLKIN <sup>2</sup>	0.5t $\overline{C}$ KOP+N×t $\overline{C}$ CLK	0.5t $\overline{C}$ KOP+N×t $\overline{C}$ CLK+5	ns
t $\overline{C}$ DCTR	CLKOUT Disable After CLKIN	t $\overline{C}$ KOP-5	t $\overline{C}$ KOP	ns
t $\overline{A}$ TRHBG	Address/Select Disable Before $\overline{HBG}$ Low <sup>4</sup>	1.5t $\overline{C}$ KOP-6	1.5t $\overline{C}$ KOP+2	ns
t $\overline{S}$ TRHBG	$\overline{RD}/\overline{WR}/\overline{DMAGx}$ Disable Before $\overline{HBG}$ Low <sup>4</sup>	t $\overline{C}$ KOP+0.25t $\overline{C}$ CLK-4	t $\overline{C}$ KOP+0.25t $\overline{C}$ CLK+3	ns
t $\overline{B}$ TRHBG	$\overline{BMS}$ Disable Before $\overline{HBG}$ Low <sup>4</sup>	0.5t $\overline{C}$ KOP-4	0.5t $\overline{C}$ KOP+2	ns
t $\overline{M}$ ENHBG	Memory Interface Enable After $\overline{HBG}$ High <sup>4</sup>	t $\overline{C}$ KOP-5	t $\overline{C}$ KOP+5	ns

<sup>1</sup>Strobes =  $\overline{RD}$ ,  $\overline{WR}$ ,  $\overline{DMAGx}$ .

<sup>2</sup>Where N = 0.5, 1.0, 1.5 for 1:2, 1:3, and 1:4, respectively.

<sup>3</sup>In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.

<sup>4</sup>Memory Interface = Address,  $\overline{RD}$ ,  $\overline{WR}$ ,  $\overline{MSx}$ ,  $\overline{DMAGx}$ , and  $\overline{BMS}$  (in EPROM boot mode).  $\overline{BMS}$  is only an output in EPROM boot mode.

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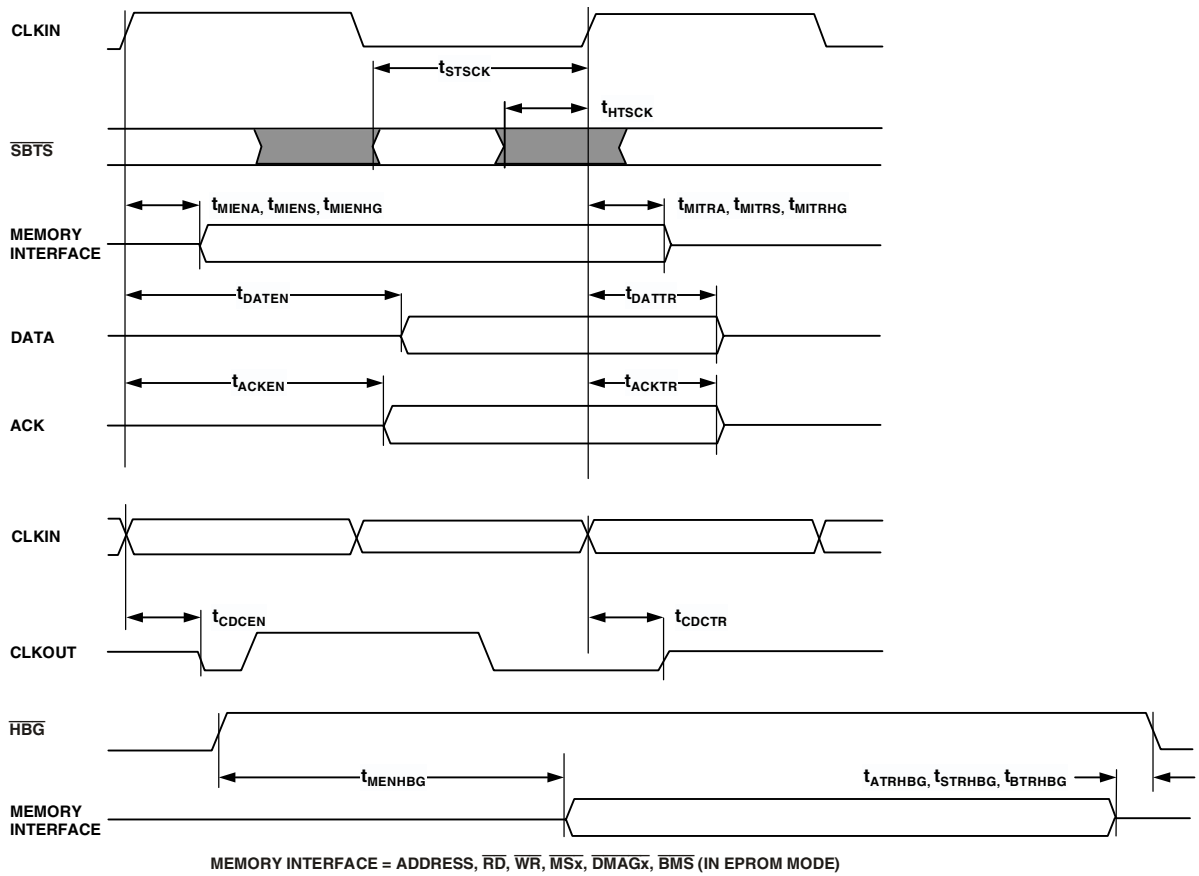


Figure 27. Three-State Timing – Bus Master, Bus Slave

## DMA Handshake

These specifications describe the three DMA handshake modes. In all three modes  $\overline{\text{DMAR}}$  is used to initiate transfers. For handshake mode,  $\overline{\text{DMAG}}$  controls the latching or enabling of data externally. For external handshake mode, the data transfer is controlled by the  $\overline{\text{ADDR23-0}}$ ,  $\overline{\text{RD}}$ ,  $\overline{\text{WR}}$ ,  $\overline{\text{MS3-0}}$ ,  $\overline{\text{ACK}}$ , and

$\overline{\text{DMAG}}$  signals. For Paced Master mode, the data transfer is controlled by  $\overline{\text{ADDR23-0}}$ ,  $\overline{\text{RD}}$ ,  $\overline{\text{WR}}$ ,  $\overline{\text{MS3-0}}$ , and  $\overline{\text{ACK}}$  (not  $\overline{\text{DMAG}}$ ). For Paced Master mode, the Memory Read-Bus Master, Memory Write-Bus Master, and Synchronous Read/Write-Bus Master timing specifications for  $\overline{\text{ADDR23-0}}$ ,  $\overline{\text{RD}}$ ,  $\overline{\text{WR}}$ ,  $\overline{\text{MS3-0}}$ ,  $\overline{\text{DATA47-16}}$ , and  $\overline{\text{ACK}}$  also apply.

**Table 24. DMA Handshake**

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
$t_{\text{SDRC}}$	$\overline{\text{DMARx}}$ Setup Before $\text{CLKIN}^1$	3.5	ns
$t_{\text{WDR}}$	$\overline{\text{DMARx}}$ Width Low (Nonsynchronous) <sup>2</sup>	$t_{\text{CCLK}} + 4.5$	ns
$t_{\text{SDATDGL}}$	Data Setup After $\overline{\text{DMAGx}}$ Low <sup>3</sup>	$t_{\text{CKOP}} - 0.5t_{\text{CCLK}} - 7$	ns
$t_{\text{HDATIDG}}$	Data Hold After $\overline{\text{DMAGx}}$ High	2	ns
$t_{\text{DATDRH}}$	Data Valid After $\overline{\text{DMARx}}$ High <sup>3</sup>	$t_{\text{CKOP}} + 3$	ns
$t_{\text{DMARLL}}$	$\overline{\text{DMARx}}$ Low Edge to Low Edge <sup>4</sup>	$t_{\text{CKOP}}$	ns
$t_{\text{DMARH}}$	$\overline{\text{DMARx}}$ Width High <sup>2</sup>	$t_{\text{CCLK}} + 4.5$	ns
<i>Switching Characteristics</i>			
$t_{\text{DDGL}}$	$\overline{\text{DMAGx}}$ Low Delay After $\text{CLKIN}$	$0.25t_{\text{CCLK}} + 1$	ns
$t_{\text{WDGH}}$	$\overline{\text{DMAGx}}$ High Width	$0.5t_{\text{CCLK}} - 1 + \text{HI}$	ns
$t_{\text{WDGL}}$	$\overline{\text{DMAGx}}$ Low Width	$t_{\text{CKOP}} - 0.5t_{\text{CCLK}} - 1$	ns
$t_{\text{HDGC}}$	$\overline{\text{DMAGx}}$ High Delay After $\text{CLKIN}$	$t_{\text{CKOP}} - 0.25t_{\text{CCLK}} + 1.0$	ns
$t_{\text{VDATDGH}}$	Data Valid Before $\overline{\text{DMAGx}}$ High <sup>5</sup>	$t_{\text{CKOP}} - 0.25t_{\text{CCLK}} - 8$	ns
$t_{\text{DATRDGH}}$	Data Disable After $\overline{\text{DMAGx}}$ High <sup>6</sup>	$t_{\text{CKOP}} - 0.25t_{\text{CCLK}} + 5$	ns
$t_{\text{DGWRL}}$	$\overline{\text{WRx}}$ Low Before $\overline{\text{DMAGx}}$ Low	-1.5	ns
$t_{\text{DGWRH}}$	$\overline{\text{DMAGx}}$ Low Before $\overline{\text{WRx}}$ High	$t_{\text{CKOP}} - 0.5t_{\text{CCLK}} - 2 + \text{W}$	ns
$t_{\text{DGWRR}}$	$\overline{\text{WRx}}$ High Before $\overline{\text{DMAGx}}$ High <sup>7</sup>	-1.5	ns
$t_{\text{DGRDL}}$	$\overline{\text{RDx}}$ Low Before $\overline{\text{DMAGx}}$ Low	-1.5	ns
$t_{\text{DRDGH}}$	$\overline{\text{RDx}}$ Low Before $\overline{\text{DMAGx}}$ High	$t_{\text{CKOP}} - 0.5t_{\text{CCLK}} - 2 + \text{W}$	ns
$t_{\text{DGRDR}}$	$\overline{\text{RDx}}$ High Before $\overline{\text{DMAGx}}$ High <sup>7</sup>	-1.5	ns
$t_{\text{DGWR}}$	$\overline{\text{DMAGx}}$ High to $\overline{\text{WRx}}$ , $\overline{\text{RDx}}$ Low	$0.5t_{\text{CCLK}} - 2 + \text{HI}$	ns
$t_{\text{DADGH}}$	Address/Select Valid to $\overline{\text{DMAGx}}$ High	15	ns
$t_{\text{DDGHA}}$	Address/Select Hold After $\overline{\text{DMAGx}}$ High	1	ns

$\text{W} = (\text{number of wait states specified in WAIT register}) \times t_{\text{CKOP}}$ .

$\text{HI} = t_{\text{CKOP}}$  (if data bus idle cycle occurs, as specified in WAIT register; otherwise  $\text{HI} = 0$ ).

<sup>1</sup> Only required for recognition in the current cycle.

<sup>2</sup> Maximum throughput using  $\overline{\text{DMARx}}$ / $\overline{\text{DMAGx}}$  handshaking equals  $t_{\text{WDR}} + t_{\text{DMARH}} = (t_{\text{CCLK}} + 4.5) + (t_{\text{CCLK}} + 4.5) = 29$  ns (34.5 MHz). This throughput limit applies to non-synchronous access mode only.

<sup>3</sup>  $t_{\text{SDATDGL}}$  is the data setup requirement if  $\overline{\text{DMARx}}$  is not being used to hold off completion of a write. Otherwise, if  $\overline{\text{DMARx}}$  low holds off completion of the write, the data can be driven  $t_{\text{DATDRH}}$  after  $\overline{\text{DMARx}}$  is brought high.

<sup>4</sup> Use  $t_{\text{DMARLL}}$  if  $\overline{\text{DMARx}}$  transitions synchronous with  $\text{CLKIN}$ . Otherwise, use  $t_{\text{WDR}}$  and  $t_{\text{DMARH}}$ .

<sup>5</sup>  $t_{\text{VDATDGH}}$  is valid if  $\overline{\text{DMARx}}$  is not being used to hold off completion of a read. If  $\overline{\text{DMARx}}$  is used to prolong the read, then

$t_{\text{VDATDGH}} = t_{\text{CKOP}} - 0.25t_{\text{CCLK}} - 8 + (n \times t_{\text{CKOP}})$  where  $n$  equals the number of extra cycles that the access is prolonged.

<sup>6</sup> See [Example System Hold Time Calculation on Page 51](#) for calculation of hold times given capacitive and dc loads.

<sup>7</sup> This parameter applies for synchronous access mode only.

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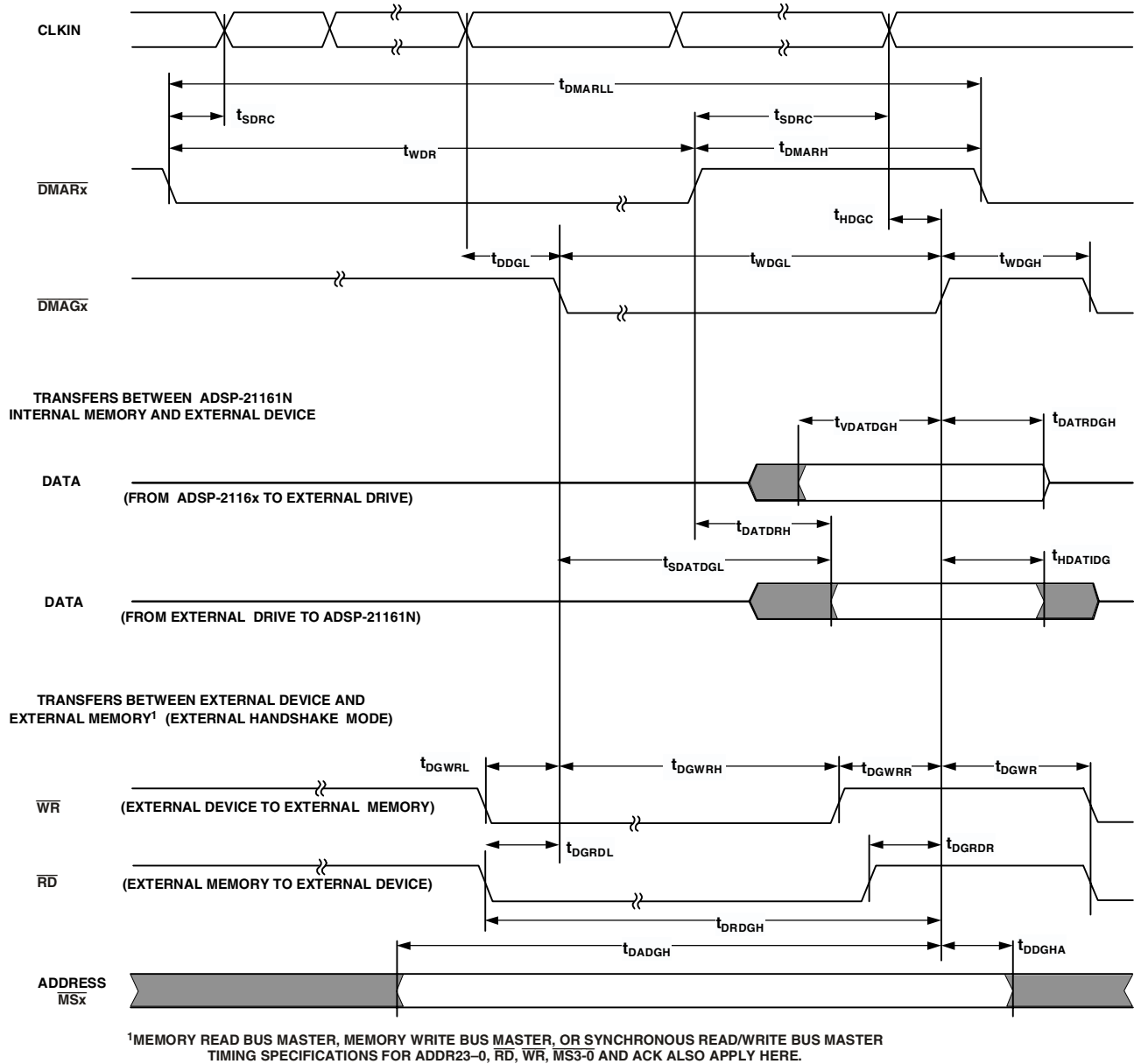


Figure 28. DMA Handshake



**SDRAM Interface – Bus Master**

Use these specifications for ADSP-21161N bus master accesses of SDRAM:

**Table 25. SDRAM Interface – Bus Master**

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
t <sub>SDSDK</sub>	Data Setup Before SDCLK	2.0		ns
t <sub>HDSDK</sub>	Data Hold After SDCLK	2.3		ns
<i>Switching Characteristics</i>				
t <sub>SDSK1</sub>	First SDCLK Rise Delay After CLKIN <sup>1, 2</sup>	0.75t <sub>CCLK</sub> + 1.5	0.75t <sub>CCLK</sub> + 8.0	ns
t <sub>SDK</sub>	SDCLK Period	t <sub>CCLK</sub>	2 × t <sub>CCLK</sub>	ns
t <sub>SDKH</sub>	SDCLK Width High	4		ns
t <sub>SDKL</sub>	SDCLK Width Low	4		ns
t <sub>DCADSDK</sub>	Command, Address, Data, Delay After SDCLK <sup>3</sup>		0.25t <sub>CCLK</sub> + 2.5	ns
t <sub>HCADSDK</sub>	Command, Address, Data, Hold After SDCLK <sup>3</sup>	2.0		ns
t <sub>SDTRS</sub>	Data Three-State After SDCLK <sup>4</sup>		0.5t <sub>CCLK</sub> + 2.0	ns
t <sub>SDENS</sub>	Data Enable After SDCLK <sup>5</sup>	0.75t <sub>CCLK</sub>		ns
t <sub>SDCTR</sub>	Command Three-State After CLKIN	0.5t <sub>CCLK</sub> - 1.5	0.5t <sub>CCLK</sub> + 6.0	ns
t <sub>SDCEN</sub>	Command Enable After CLKIN	2	5	ns
t <sub>SDSKTR</sub>	SDCLK Three-State After CLKIN	0	3	ns
t <sub>SDSKEN</sub>	SDCLK Enable After CLKIN	1	4	ns
t <sub>SDATR</sub>	Address Three-State After CLKIN	-0.25 t <sub>CCLK</sub> - 5	-0.25t <sub>CCLK</sub>	ns
t <sub>SDAEN</sub>	Address Enable After CLKIN	-0.4	+7.2	ns

<sup>1</sup> For the second, third, and fourth rising edges of SDCLK delay from CLKIN, add appropriate number of SDCLK period to the t<sub>SDSK1</sub> and t<sub>SSDKC1</sub> values, depending upon the SDCKR value and the core clock to CLKIN ratio.

<sup>2</sup> Subtract t<sub>CCLK</sub> from result if value is greater than or equal to t<sub>CCLK</sub>.

<sup>3</sup> Command = SDCKE, MSx, DQM, RAS, CAS, SDA10, and SDWE

<sup>4</sup> SDRAM Controller adds one SDRAM CLK three-stated cycle delay on a read, followed by a write.

<sup>5</sup> Valid when DSP transitions to SDRAM master from SDRAM slave.

**SDRAM Interface – Bus Slave**

These timing requirements allow a bus slave to sample the bus master’s SDRAM command and detect when a refresh occurs:

**Table 26. SDRAM Interface – Bus Slave**

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
t <sub>SSDKC1</sub>	First SDCLK Rise after CLKOUT <sup>1, 2, 3</sup>	SDCK × t <sub>CCLK</sub> - 0.5t <sub>CCLK</sub> - 0.5	SDCKR × t <sub>CCLK</sub> - 0.25t <sub>CCLK</sub> + 2.0	ns
t <sub>SCSDK</sub>	Command Setup before SDCLK <sup>4</sup>	2		ns
t <sub>HCSDK</sub>	Command Hold after SDCLK <sup>4</sup>	1		ns

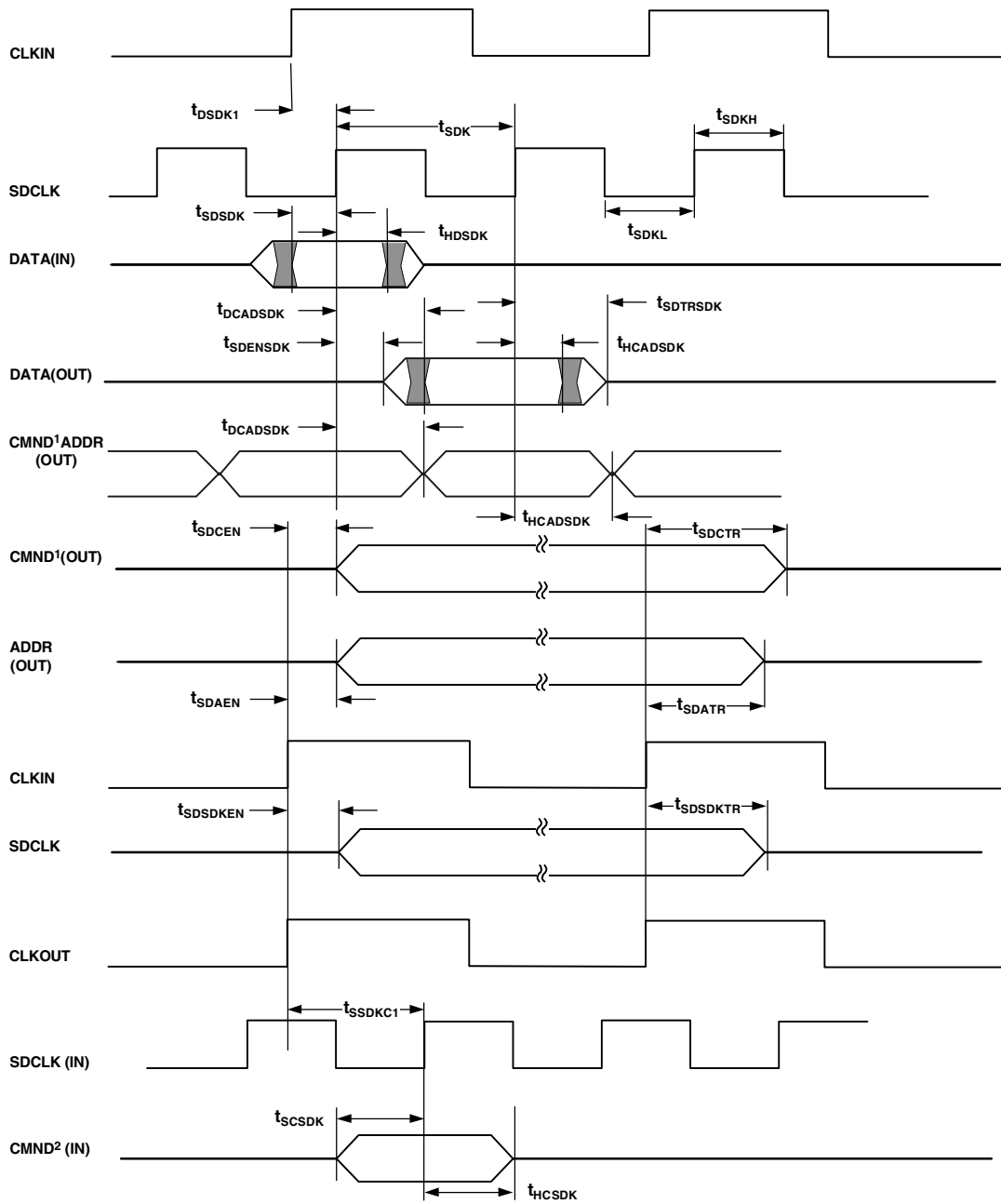
<sup>1</sup> For the second, third, and fourth rising edges of SDCLK delay from CLKOUT, add appropriate number of SDCLK period to the t<sub>SDSK1</sub> and t<sub>SSDKC1</sub> values, depending upon the SDCKR value and the Core clock to CLKOUT ratio.

<sup>2</sup> SDCKR = 1 for SDCLK equal to core clock frequency and SDCKR = 2 for SDCLK equal to half core clock frequency.

<sup>3</sup> Subtract t<sub>CCLK</sub> from result if value is greater than or equal to t<sub>CCLK</sub>.

<sup>4</sup> Command = SDCKE, RAS, CAS, and SDWE.

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<sup>1</sup>COMMAND = SDCKE,  $\overline{MSx}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{SDWE}$ , DQM, AND SDA10.

<sup>2</sup>COMMAND = SDCKE,  $\overline{RAS}$ ,  $\overline{CAS}$ , AND  $\overline{SDWE}$ .

Figure 29. SDRAM Interface

### Link Ports

Calculation of link receiver data setup and hold relative to link clock is required to determine the maximum allowable skew that can be introduced in the transmission path between LDATA and LCLK. Setup skew is the maximum delay that can be introduced in LDATA relative to LCLK, (setup skew =  $t_{LCLKTWH} \text{ min} - t_{DLDC} - t_{SLDCL}$ ). Hold skew is the maximum delay that can be introduced in LCLK relative to LDATA, (hold skew =  $t_{LCLKTWL} \text{ min} - t_{HLDCH} - t_{HLDCL}$ ). Calculations made directly from speed specifications

will result in unrealistically small skew times because they include multiple tester guardbands. The setup and hold skew times shown below are calculated to include only one tester guardband.

ADSP-21161N Setup Skew = 1.5 ns max

ADSP-21161N Hold Skew = 1.5 ns max

Note that there is a two-cycle effect latency between the link port enable instruction and the DSP enabling the link port.

**Table 27. Link Ports – Receive**

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
$t_{SLDCL}$ Data Setup Before LCLK Low	1		ns
$t_{HLDCL}$ Data Hold After LCLK Low	3.5		ns
$t_{LCLKIW}$ LCLK Period	$t_{LCLK}$		ns
$t_{LCLKRWL}$ LCLK Width Low	4.0		ns
$t_{LCLKRWH}$ LCLK Width High	4.0		ns
<i>Switching Characteristics</i>			
$t_{DLALC}$ LACK Low Delay After LCLK High <sup>1</sup>	8	12	ns

<sup>1</sup>LACK goes low with  $t_{DLALC}$  relative to rise of LCLK after first nibble, but does not go low if the receiver's link buffer is not about to fill.

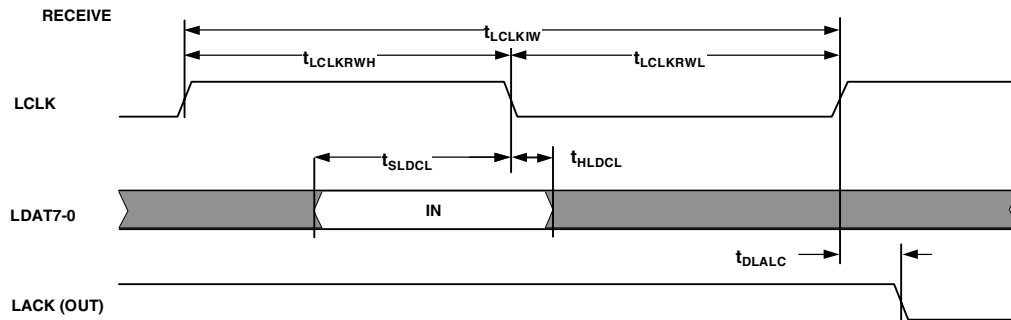


Figure 30. Link Ports—Receive

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**Table 28. Link Ports – Transmit**

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
$t_{SLACH}$ LACK Setup Before LCLK High	8		ns
$t_{HLACH}$ LACK Hold After LCLK High	-2		ns
<i>Switching Characteristics</i>			
$t_{DLDC}$ Data Delay After LCLK High		3	ns
$t_{HLDCH}$ Data Hold After LCLK High	0		ns
$t_{LCLKTWL}$ LCLK Width Low	$0.5t_{LCLK}-1.0$	$0.5t_{LCLK}+1.0$	ns
$t_{LCLKTWH}$ LCLK Width High	$0.5t_{LCLK}-1.0$	$0.5t_{LCLK}+1.0$	ns
$t_{DLACK}$ LCLK Low Delay After LACK High	$0.5t_{LCLK}+3$	$3t_{LCLK}+11$	ns

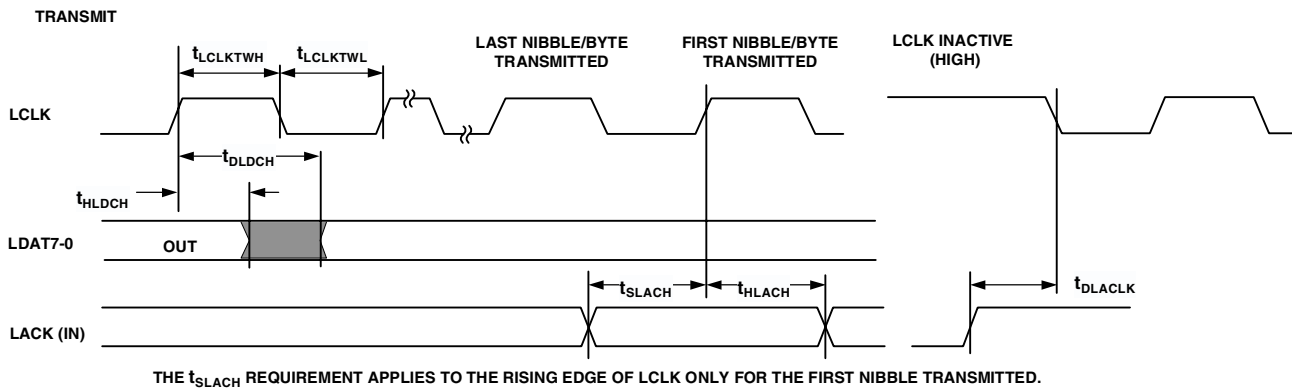


Figure 31. Link Ports – Transmit

**Serial Ports**

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

**Table 29. Serial Ports – External Clock**

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t <sub>SFSE</sub> Transmit/Receive FS Setup Before Transmit/Receive SCLK <sup>1</sup>	3.5		ns
t <sub>HFSE</sub> Transmit/Receive FS Hold After Transmit/Receive SCLK <sup>1</sup>	4		ns
t <sub>SDRE</sub> Receive Data Setup Before Receive SCLK <sup>1</sup>	1.5		ns
t <sub>HDRE</sub> Receive Data Hold After Receive SCLK <sup>1</sup>	4		ns
t <sub>SCLKW</sub> SCLKx Width	7		ns
t <sub>SCLK</sub> SCLKx Period	2t <sub>CCLK</sub>		ns

<sup>1</sup>Referenced to sample edge.

**Table 30. Serial Ports – Internal Clock**

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t <sub>SFSI</sub> FS Setup Time Before SCLK (Transmit/Receive Mode) <sup>1</sup>	8		ns
t <sub>HFSI</sub> FS Hold After SCLK (Transmit/Receive Mode) <sup>1</sup>	0.5t <sub>CCLK</sub> +1		ns
t <sub>SDRI</sub> Receive Data Setup Before SCLK <sup>1</sup>	4		ns
t <sub>HDRI</sub> Receive Data Hold After SCLK <sup>1</sup>	3		ns

<sup>1</sup>Referenced to sample edge.

**Table 31. Serial Ports – External Clock**

Parameter	Min	Max	Unit
<i>Switching Characteristics</i>			
t <sub>DFSE</sub> FS Delay After SCLK (Internally Generated FS) <sup>1,2,3</sup>		13	ns
t <sub>HOFSE</sub> FS Hold After SCLK (Internally Generated FS) <sup>1,2,3</sup>	3		ns
t <sub>DDTE</sub> Transmit Data Delay After SCLK <sup>1,2</sup>		16	ns
t <sub>HDTTE</sub> Transmit Data Hold After SCLK <sup>1,2</sup>	0		ns

<sup>1</sup>Referenced to drive edge.

<sup>2</sup>SCLK/FS Configured as a transmit clock/frame sync with the DDIR bit = 1 in SPCTLx register.

<sup>3</sup>SCLK/FS Configured as a receive clock/frame sync with the DDIR bit = 0 in SPCTLx register.

**Table 32. Serial Ports – Internal Clock**

Parameter	Min	Max	Unit
<i>Switching Characteristics</i>			
t <sub>DFSI</sub> FS Delay After SCLK (Internally Generated FS) <sup>1,2,3</sup>		4.5	ns
t <sub>HOFSI</sub> FS Hold After SCLK (Internally Generated FS) <sup>1,2,3</sup>	-1.5		ns
t <sub>DDTI</sub> Transmit Data Delay After SCLK <sup>1,2</sup>		7.5	ns
t <sub>HDTI</sub> Transmit Data Hold After SCLK <sup>1,2</sup>	0		ns
t <sub>SCLKIW</sub> SCLK Width <sup>2</sup>	0.5t <sub>SCLK</sub> -2.5	0.5t <sub>SCLK</sub> +2	ns

<sup>1</sup>Referenced to drive edge.

<sup>2</sup>SCLK/FS Configured as a transmit clock/frame sync with the DDIR bit = 1 in SPCTLx register.

<sup>3</sup>SCLK/FS Configured as a receive clock/frame sync with the DDIR bit = 0 in SPCTLx register.

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**Table 33. Serial Ports – Enable and Three-State**

Parameter	Min	Max	Unit
<i>Switching Characteristics</i>			
t <sub>DDTEN</sub> Data Enable from External Transmit SCLK <sup>1,2</sup>	4		ns
t <sub>DDTTE</sub> Data Disable from External Transmit SCLK <sup>1</sup>		10	ns
t <sub>DDTIN</sub> Data Enable from Internal Transmit SCLK <sup>1</sup>	0		ns
t <sub>DDTTI</sub> Data Disable from Internal Transmit SCLK <sup>1</sup>		3	ns

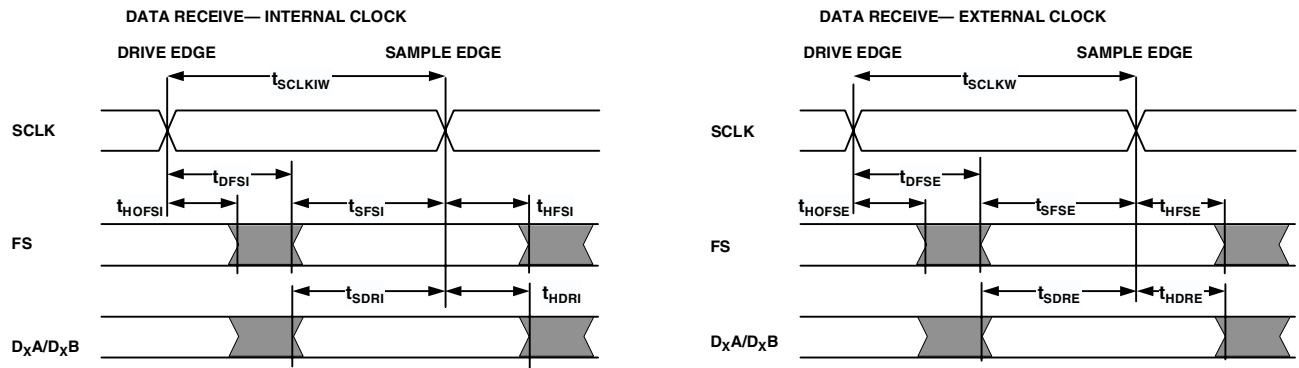
<sup>1</sup>Referenced to drive edge.

<sup>2</sup>SCLK/FS Configured as a transmit clock/frame sync with the DDIR bit = 1 in SPCTLx register.

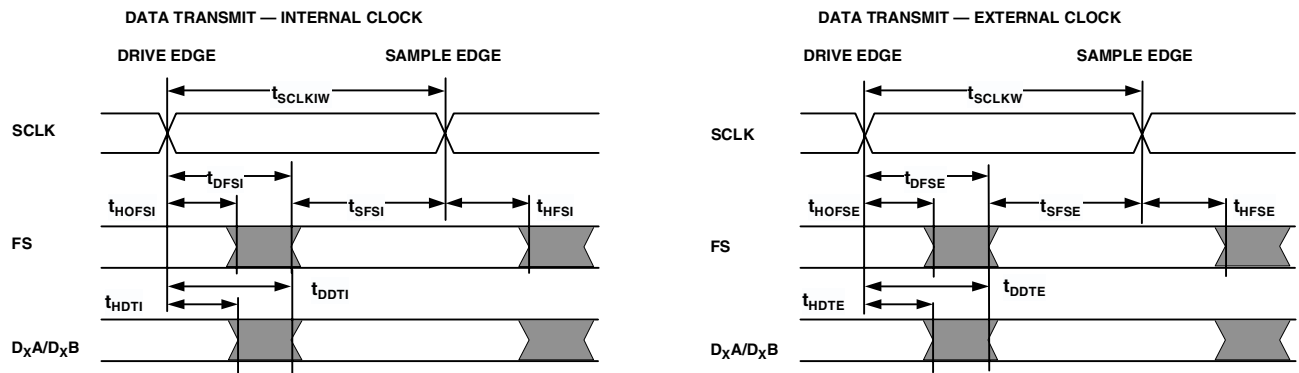
**Table 34. Serial Ports – External Late Frame Sync**

Parameter	Min	Max	Unit
<i>Switching Characteristics</i>			
t <sub>DDTLFSE</sub> Data Delay from Late External Transmit FS or External Receive FS with MCE = 1, MFD = 0 <sup>1</sup>		13	ns
t <sub>DDTENFS</sub> Data Enable from Late FS or MCE = 1, MFD = 0 <sup>1</sup>	0.5		ns

<sup>1</sup>MCE = 1, Transmit FS enable and Transmit FS valid follow t<sub>DDTLFSE</sub> and t<sub>DDTENFS</sub>.



NOTE: EITHER THE RISING EDGE OR FALLING EDGE OF SCLK (EXTERNAL), SCLK (INTERNAL) CAN BE USED AS THE ACTIVE SAMPLING EDGE.



NOTE: EITHER THE RISING EDGE OR FALLING EDGE OF SCLK (EXTERNAL), SCLK (INTERNAL) CAN BE USED AS THE ACTIVE SAMPLING EDGE.

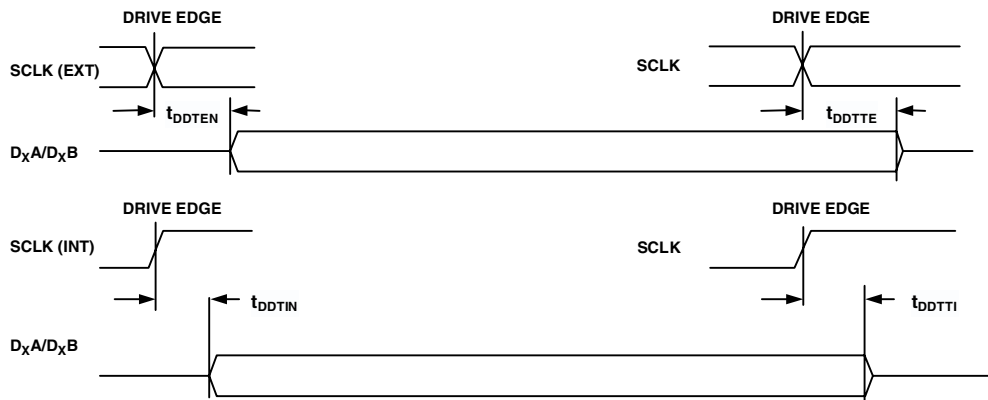


Figure 32. Serial Ports



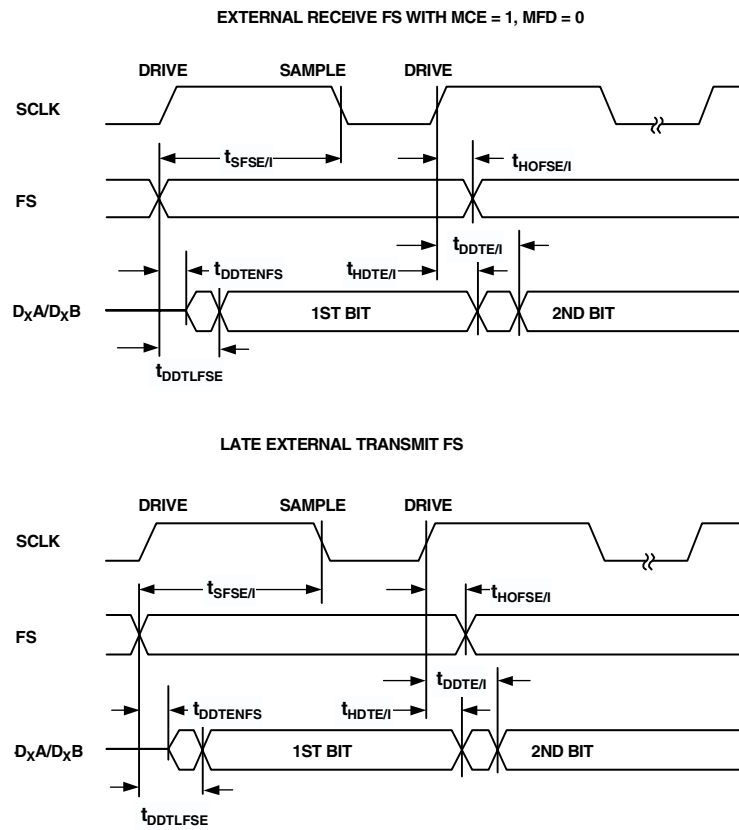


Figure 33. Serial Ports – External Late Frame Sync

## SPI Interface Specifications

**Table 35. SPI Interface Protocol – Master Switching and Timing**

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
$t_{SSPIDM}$ Data Input Valid to SPICLK Edge (Data Input Set-up Time)	$0.5t_{CCLK}+10$		ns
$t_{HSPIDM}$ SPICLK Last Sampling Edge to Data Input Not Valid	$0.5t_{CCLK}+1$		ns
$t_{SPITDM}$ Sequential Transfer Delay	$2t_{CCLK}$		ns
<i>Switching Characteristics</i>			
$t_{SPICLKM}$ Serial Clock Cycle	$8 t_{CCLK}$		ns
$t_{SPICHM}$ Serial Clock High Period	$4t_{CCLK}-4$		ns
$t_{SPICLM}$ Serial Clock Low Period	$4t_{CCLK}-4$		ns
$t_{DDSPIDM}$ SPICLK Edge to Data Out Valid (Data Out Delay Time)		3	ns
$t_{HDSPIDM}$ SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	0		ns
$t_{SDSCIM_0}$ FLAG3-0 (SPI Device Select) Low to First SPICLK Edge for CPHASE = 0	$5t_{CCLK}$		ns
$t_{SDSCIM_1}$ FLAG3-0 (SPI Device Select) Low to First SPICLK Edge for CPHASE = 1	$3t_{CCLK}$		ns
$t_{HDSM}$ Last SPICLK Edge to FLAG3-0 High	$t_{CCLK}-3$		ns

**Table 36. SPI Interface Protocol – Slave Switching and Timing**

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
$t_{SPICLKS}$ Serial Clock Cycle	$8t_{CCLK}$		ns
$t_{SPICHS}$ Serial Clock High Period	$4t_{CCLK}-4$		ns
$t_{SPICLS}$ Serial Clock Low Period	$4t_{CCLK}-4$		ns
$t_{SDSCO}$ $\overline{SPIDS}$ Assertion to First SPICLK Edge			
CPHASE = 0	$3.5t_{CCLK}+8$		ns
CPHASE = 1	$1.5t_{CCLK}+8$		ns
$t_{HDS}$ Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted			
CPHASE = 0	0		ns
$t_{SSPIDS}$ Data Input Valid to SPICLK Edge (Data Input Set-up Time)	0		ns
$t_{HSPIDS}$ SPICLK Last Sampling Edge to Data Input Not Valid	$t_{CCLK}+1$		ns
$t_{SDPPW}$ $\overline{SPIDS}$ Deassertion Pulsewidth (CPHASE = 0)	$t_{CCLK}$		ns
<i>Switching Characteristics</i>			
$t_{DSOE}$ $\overline{SPIDS}$ Assertion to Data Out Active	2	$0.5t_{CCLK}+5.5$	ns
$t_{DSDHI}$ $\overline{SPIDS}$ Deassertion to Data High Impedance	1.5	$0.5t_{CCLK}+5.5$	ns
$t_{DDSPIDS}$ SPICLK Edge to Data Out Valid (Data Out Delay Time)		$0.75t_{CCLK}+3$	ns
$t_{HDSPIDS}^1$ SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$0.25t_{CCLK}+3$		ns
$t_{HDL SBS}^1$ SPICLK Edge to Last Bit Out Not Valid (Data Out Hold Time) for LSB	$0.5t_{SPICLK}+4.5t_{CCLK}$		ns
$t_{DSOV}^2$ $\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0)		$1.5t_{CCLK}+7$	ns

<sup>1</sup>When CPHASE = 0 and baud rate is greater than 1,  $t_{HDL SBS}$  affects the length of the last bit transmitted.

<sup>2</sup>Applies to the first deassertion of  $\overline{SPIDS}$  only.

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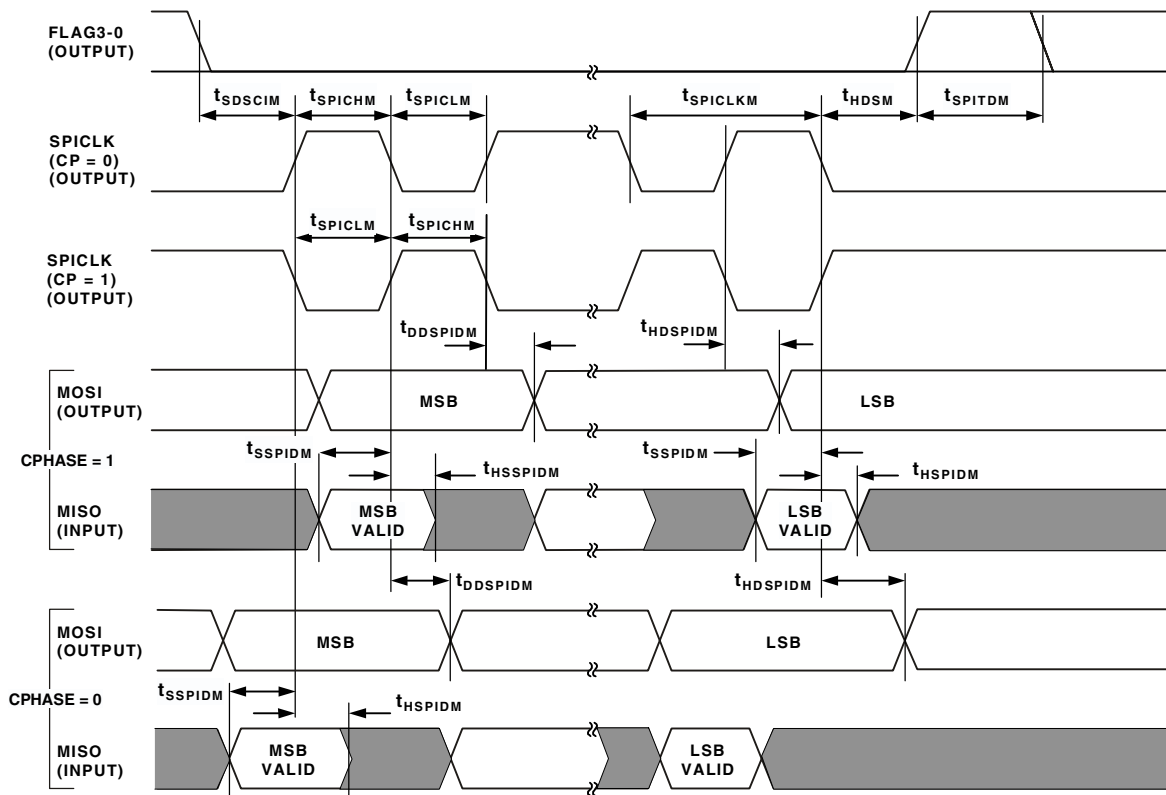


Figure 34. SPI Interface Protocol – Master Switching and Timing



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## JTAG Test Access Port and Emulation

**Table 37. JTAG Test Access Port and Emulation**

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
$t_{TCK}$ TCK Period	$t_{CK}$		ns
$t_{STAP}$ TDI, TMS Setup Before TCK High	5		ns
$t_{HTAP}$ TDI, TMS Hold After TCK High	6		ns
$t_{SSYS}$ System Inputs Setup Before TCK Low <sup>1</sup>	2		ns
$t_{HSYS}$ System Inputs Hold After TCK Low <sup>1</sup>	15		ns
$t_{TRSTW}$ $\overline{TRST}$ Pulsewidth	$4t_{CK}$		ns
<i>Switching Characteristics</i>			
$t_{DTDO}$ TDO Delay from TCK Low		13	ns
$t_{DSYS}$ System Outputs Delay After TCK Low <sup>2</sup>		30	ns

<sup>1</sup> System Inputs = DATA47-16, ADDR23-0,  $\overline{RD}$ ,  $\overline{WR}$ , ACK, RPBA,  $\overline{SPIDS}$ , EBOOT, LBOOT,  $\overline{DMAR2-1}$ , CLK\_CFG1-0, CLKDBL, CS, HBR,  $\overline{SBTS}$ , ID2-0,  $\overline{IRQ2-0}$ ,  $\overline{RESET}$ ,  $\overline{BMS}$ , MISO, MOSI, SPICLK, DxA, DxB, SCLKx, FSx, LxDAT7-0, LxCLK, LxACK,  $\overline{SDWE}$ ,  $\overline{HBG}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ , SDCLK0, SDCKE, BRST,  $\overline{BR6-1}$ , PA,  $\overline{MS3-0}$ , FLAG11-0.

<sup>2</sup> System Outputs =  $\overline{BMS}$ , MISO, MOSI, SPICLK, DxA, DxB, SCLKx, FSx, LxDAT7-0, LxCLK, LxACK, DATA47-16,  $\overline{SDWE}$ , ACK,  $\overline{HBG}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ , SDCLK1-0, SDCKE, BRST,  $\overline{RD}$ ,  $\overline{WR}$ ,  $\overline{BR6-1}$ , PA,  $\overline{MS3-0}$ , ADDR23-0, FLAG11-0,  $\overline{DMAG2-1}$ , DQM, REDY, CLKOUT, SDA10, TIMEXP, EMU, BMSTR, RSTOUT.

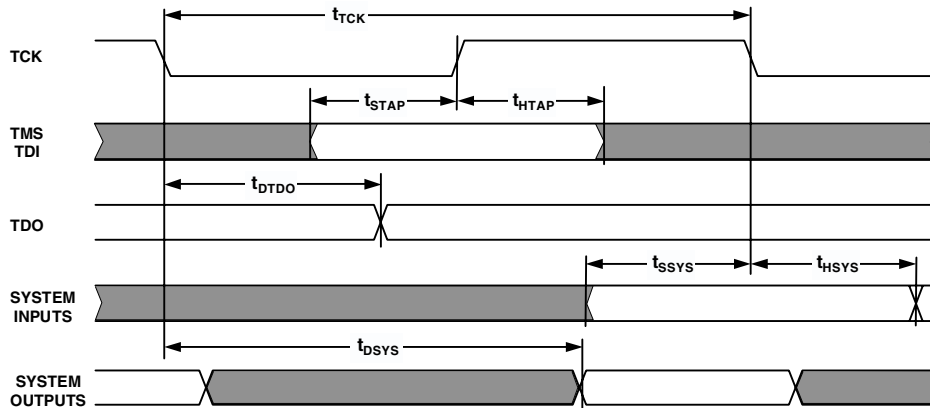


Figure 36. JTAG Test Access Port and Emulation

## Output Drive Currents

Figure 37 shows typical I-V characteristics for the output drivers of the ADSP-21161N. The curves represent the current drive capability of the output drivers as a function of output voltage.

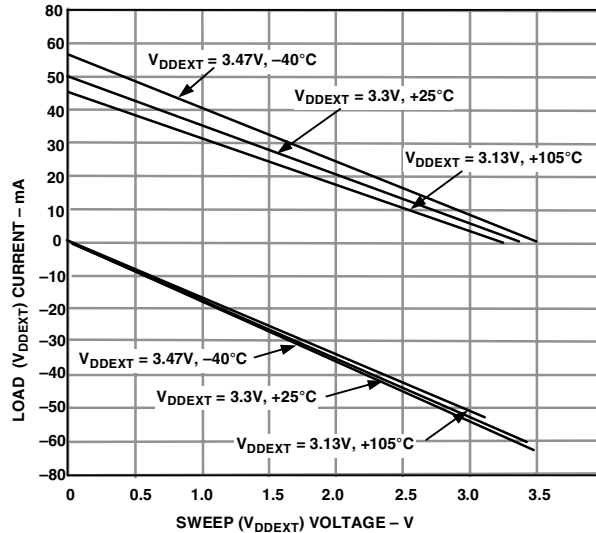


Figure 37. Typical Drive Currents

## Test Conditions

The DSP is tested for output enable, disable, and hold time.

### Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving. The output enable time  $t_{ENA}$  is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram (Figure 38). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

### Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by  $\Delta V$  is dependent on the capacitive load,  $C_L$  and the load current,  $I_L$ . This decay time can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \Delta V}{I_L}$$

The output disable time  $t_{DIS}$  is the difference between  $t_{MEASURED}$  and  $t_{DECAY}$  as shown in Figure 38. The time  $t_{MEASURED}$  is the interval from when the reference signal switches to when the output voltage decays  $\Delta V$  from the measured output high or output low voltage.  $t_{DECAY}$  is calculated with test loads  $C_L$  and  $I_L$ , and with  $\Delta V$  equal to 0.5 V.

### Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate  $t_{DECAY}$  using the equation given above. Choose  $\Delta V$  to be the difference between the ADSP-21161N's output voltage

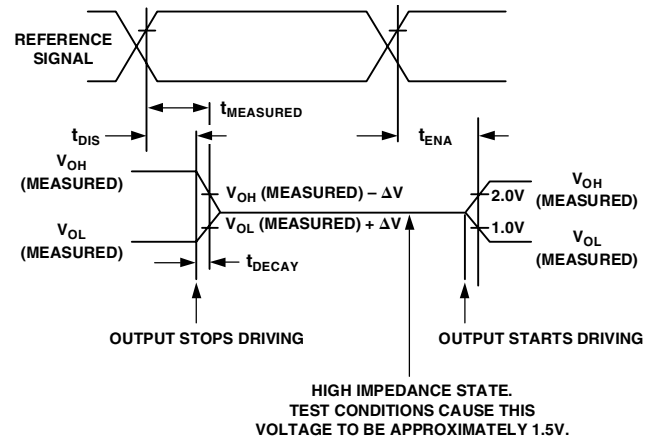


Figure 38. Output Enable/Disable

and the input threshold for the device requiring the hold time. A typical  $\Delta V$  will be 0.4 V.  $C_L$  is the total bus capacitance (per data line), and  $I_L$  is the total leakage or three-state current (per data line). The hold time will be  $t_{DECAY}$  plus the minimum disable time (i.e.,  $t_{DATRWH}$  for the write cycle).

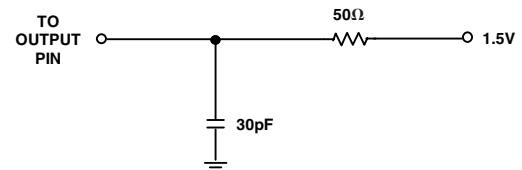


Figure 39. 31Equivalent Device Loading for AC Measurements (Includes All Fixtures)

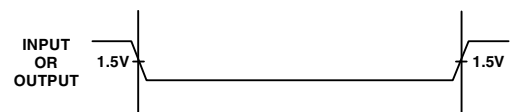


Figure 40. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

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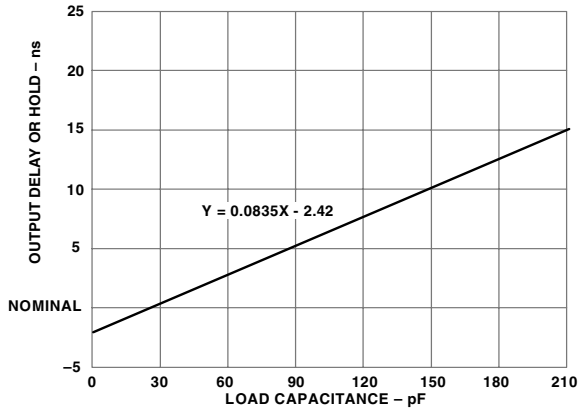


Figure 41. Typical Output Delay or Hold vs. Load Capacitance (at Max Case Temperature)

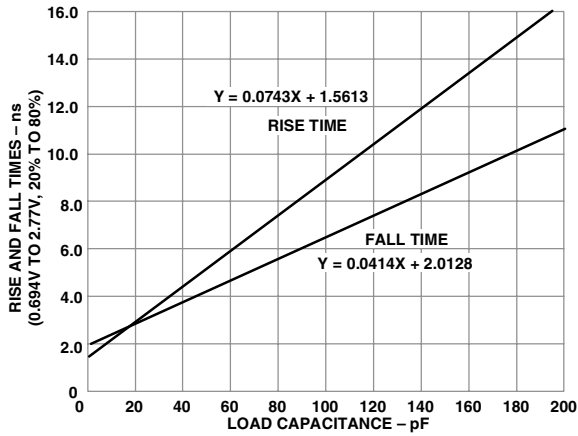


Figure 42. Typical Output Rise/Fall Time (20% - 80%,  $V_{DDEXT} = Max$ )

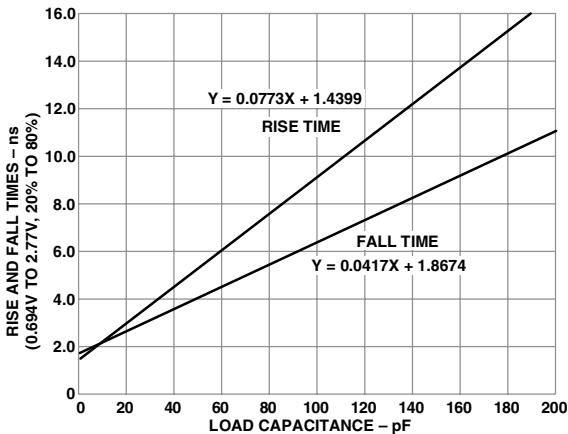


Figure 43. Typical Output Rise/Fall Time (20% - 80%,  $V_{DDEXT} = Min$ )

## Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 39 on Page 51). Figure 41 shows graphically how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see Output Disable Time on Page 51.) The graphs of Figure 41, Figure 42, and Figure 43 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% - 80%,  $V = Min$ ) vs. Load Capacitance.

## Environmental Conditions

The thermal characteristics in which the DSP is operating influence performance.

## Thermal Characteristics

The ADSP-21161N is packaged in a 225-ball Mini Ball Grid Array (MBGA). The ADSP-21161N is specified for a case temperature ( $T_{CASE}$ ). To ensure that the  $T_{CASE}$  data sheet specification is not exceeded, a heatsink and/or an air flow source may be used. Use the center block of ground pins (MBGA balls: F6-10, G6-10, H6-10, J6-10, K6-10) to provide thermal pathways to the printed circuit board's ground plane. A heatsink should be attached to the ground plane (as close as possible to the thermal pathways) with a thermal adhesive.

$$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$$

where:

- $T_{CASE}$  = Case temperature (measured on top surface of package)
- $PD$  = Power dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation).
- $\theta_{CA}$  = Value from Table 38.
- $\theta_{JB} = 8.0^\circ C/W$

Table 38. Airflow Over Package Versus  $\theta_{CA}$

Airflow (Linear Ft./Min.)	0	200	400
$\theta_{CA}$ ( $^\circ C/W$ ) <sup>1</sup>	17.9	15.2	13.7

<sup>1</sup> $\theta_{JC} = 6.8^\circ C/W$ .



225-BALL METRIC MBGA PIN CONFIGURATIONS

Table 39. 225-Ball Metric MBGA Pin Assignments

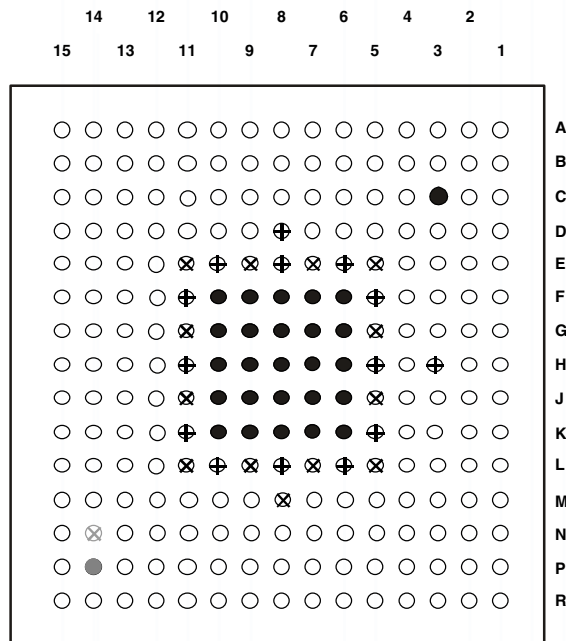
Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number
NC	A01	$\overline{\text{TRST}}$	B01	TMS	C01	TDO	D01
BMSTR	A02	TDI	B02	$\overline{\text{EMU}}$	C02	TCK	D02
$\overline{\text{BMS}}$	A03	RPBA	B03	GND	C03	FLAG11	D03
$\overline{\text{SPIDS}}$	A04	MOSI	B04	SPICLK	C04	MISO	D04
EBOOT	A05	FS0	B05	D0B	C05	SCLK0	D05
LBOOT	A06	SCLK1	B06	D1A	C06	D1B	D06
SCLK2	A07	D2B	B07	D2A	C07	FS1	D07
D3B	A08	D3A	B08	FS2	C08	V <sub>DDINT</sub>	D08
L0DAT4	A09	L0DAT7	B09	FS3	C09	SCLK3	D09
L0ACK	A10	L0CLK	B10	L0DAT6	C10	L0DAT5	D10
L0DAT2	A11	L0DAT1	B11	L1DAT7	C11	L0DAT3	D11
L1DAT6	A12	L1DAT4	B12	L1DAT3	C12	L1DAT5	D12
L1CLK	A13	L1ACK	B13	L1DAT1	C13	DATA42	D13
L1DAT2	A14	L1DAT0	B14	DATA45	C14	DATA46	D14
NC	A15	$\overline{\text{RSTOUT}}^1$	B15	DATA47	C15	DATA44	D15
FLAG10	E01	FLAG5	F01	FLAG1	G01	FLAG0	H01
$\overline{\text{RESET}}$	E02	FLAG7	F02	FLAG2	G02	$\overline{\text{IRQ0}}$	H02
FLAG8	E03	FLAG9	F03	FLAG4	G03	V <sub>DDINT</sub>	H03
D0A	E04	FLAG6	F04	FLAG3	G04	$\overline{\text{IRQ1}}$	H04
V <sub>DDEXT</sub>	E05	V <sub>DDINT</sub>	F05	V <sub>DDEXT</sub>	G05	V <sub>DDINT</sub>	H05
V <sub>DDINT</sub>	E06	GND	F06	GND	G06	GND	H06
V <sub>DDEXT</sub>	E07	GND	F07	GND	G07	GND	H07
V <sub>DDINT</sub>	E08	GND	F08	GND	G08	GND	H08
V <sub>DDEXT</sub>	E09	GND	F09	GND	G09	GND	H09
V <sub>DDINT</sub>	E10	GND	F10	GND	G10	GND	H10
V <sub>DDEXT</sub>	E11	V <sub>DDINT</sub>	F11	V <sub>DDEXT</sub>	G11	V <sub>DDINT</sub>	H11
L0DAT0	E12	DATA37	F12	DATA34	G12	DATA29	H12
DATA39	E13	DATA40	F13	DATA35	G13	DATA28	H13
DATA43	E14	DATA38	F14	DATA33	G14	DATA30	H14
DATA41	E15	DATA36	F15	DATA32	G15	DATA31	H15
$\overline{\text{IRQ2}}$	J01	TIMEXP	K01	ADDR19	L01	ADDR16	M01
ID1	J02	ADDR22	K02	ADDR17	L02	ADDR12	M02
ID2	J03	ADDR20	K03	ADDR21	L03	ADDR18	M03
ID0	J04	ADDR23	K04	ADDR2	L04	ADDR6	M04
V <sub>DDEXT</sub>	J05	V <sub>DDINT</sub>	K05	V <sub>DDEXT</sub>	L05	ADDR0	M05
GND	J06	GND	K06	V <sub>DDINT</sub>	L06	$\overline{\text{MS1}}$	M06
GND	J07	GND	K07	V <sub>DDEXT</sub>	L07	$\overline{\text{BR6}}$	M07
GND	J08	GND	K08	V <sub>DDINT</sub>	L08	V <sub>DDEXT</sub>	M08
GND	J09	GND	K09	V <sub>DDEXT</sub>	L09	$\overline{\text{WR}}$	M09
GND	J10	GND	K10	V <sub>DDINT</sub>	L10	SDA10	M10
V <sub>DDEXT</sub>	J11	V <sub>DDINT</sub>	K11	V <sub>DDEXT</sub>	L11	$\overline{\text{RAS}}$	M11
DATA26	J12	DATA22	K12	$\overline{\text{CAS}}$	L12	ACK	M12
DATA24	J13	DATA19	K13	DATA20	L13	DATA17	M13
DATA25	J14	DATA21	K14	DATA16	L14	$\overline{\text{DMAG2}}$	M14
DATA27	J15	DATA23	K15	DATA18	L15	$\overline{\text{DMAG1}}$	M15

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Table 39. 225-Ball Metric MBGA Pin Assignments (continued)

Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number
ADDR14	N01	ADDR13	P01	NC	R01
ADDR15	N02	ADDR9	P02	ADDR11	R02
ADDR10	N03	ADDR8	P03	ADDR7	R03
ADDR5	N04	ADDR4	P04	ADDR3	R04
ADDR1	N05	$\overline{MS2}$	P05	$\overline{MS3}$	R05
$\overline{MS0}$	N06	$\overline{SBTS}$	P06	$\overline{PA}$	R06
$\overline{BR5}$	N07	$\overline{BR4}$	P07	$\overline{BR3}$	R07
$\overline{BR2}$	N08	$\overline{BR1}$	P08	$\overline{RD}$	R08
BRST	N09	SDCLK1	P09	CLKOUT	R09
SDCKE	N10	SDCLK0	P10	$\overline{HBR}$	R10
$\overline{CS}$	N11	REDY	P11	$\overline{HBG}$	R11
CLK_CFG1	N12	CLKIN	P12	$\overline{CLKDBL}$	R12
CLK_CFG0	N13	DQM	P13	XTAL	R13
AVDD	N14	AGND	P14	$\overline{SDWE}$	R14
$\overline{DMAR1}$	N15	$\overline{DMAR2}$	P15	NC	R15

<sup>1</sup>  $\overline{RSTOUT}$  exists only for silicon revisions 1.2 and greater. Leave this pin unconnected for silicon revisions 0.3, 1.0, and 1.1.



KEY:

- ⊕ VDDINT
- GND\*
- ⊗ AVDD
- ⊗ VDEXT
- AGND
- SIGNAL

\* USE THE CENTER BLOCK OF GROUND PINS TO PROVIDE THERMAL PATHWAYS TO YOUR PRINTED CIRCUIT BOARD GROUND PLANE

Figure 44. 225-Ball Metric MBGA Pin Assignments (Bottom View, Summary)



# ADSP-21161N

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