Si321xPPx-EVB

EVALUATION BOARD FOR THE Si3210/15/16 PROSLIC®

Description

This document describes the operation of the Silicon Laboratories ProSLIC® device evaluation platform. The devices supported by this document are the Si3210/15/16 and Si3210M/15M/16M; both Si3201 and discrete interface topologies are included. Schematics and layouts are provided for both TSSOP and QFN packages of the various ProSLIC products. The ProSLIC evaluation platform is designed to provide observation of the ProSLIC's functionality. The ProSLIC platform consists of a ProSLIC motherboard, a device-specific daughter card, and the ProSLIC LINC™ software. The ProSLIC LINC software is a Windows®-based program that can run in Microsoft Windows environments.

Equipment requirements:

- PC running Windows 95, 98, NT, 2000, or XP
- 25-pin D male-male cable
- +5 V, 0.5 A power supply
- +3.3 V, 0.5 A power supply (optional)
- +12 V, 0.5 A power supply (Si3210, Si3215, Si3216)

Optional equipment:

- Balanced audio generator and analyzer
  (e.g., Audio Precision System 2 and/or HP TIMS set and/or Wandel and Goltermann PCM-4)
- 8 kHz PCM signal generator and analyzer
  (e.g., Audio Precision System 2 and Audio Precision SIA-2322 and/or Wandel and Goltermann PCM-4)

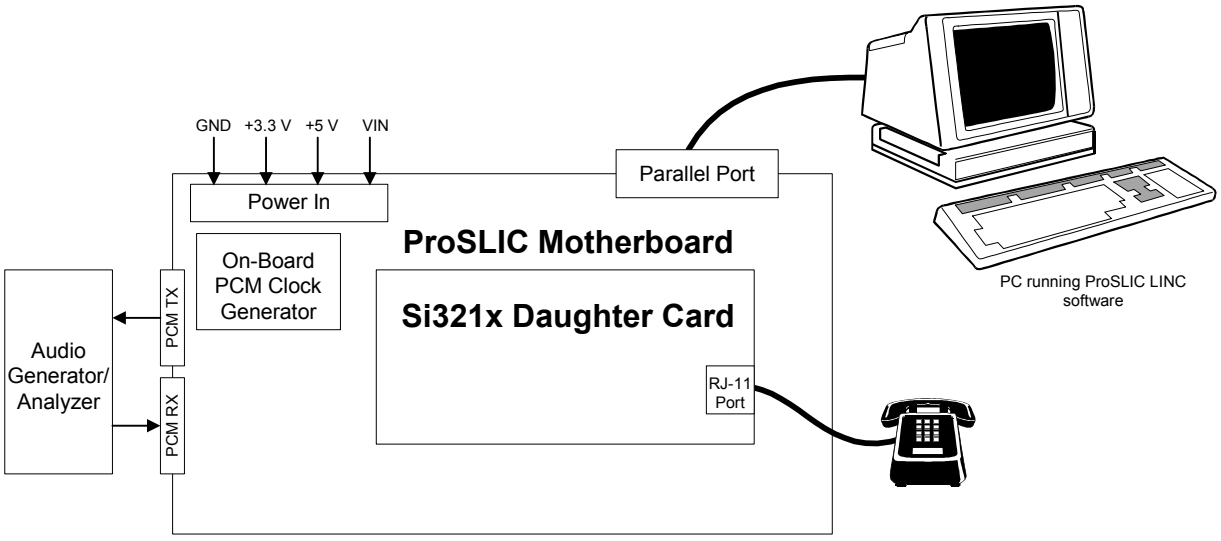
Features

- Silicon Laboratories ProSLIC device
- All components necessary for linecard implementation
- Selectable secondary protection
- Control I/O through standard Parallel Port
- On-board PCLK and FSYNC clock generation for stand-alone operation
- PCM I/O set up for Audio Precision System 2 or Wandel and Goltermann PCM-4
- Full access to PCM highway
- Multiple daughter cards may be stacked for multi-channel evaluation and daisy chain control
- ProSLIC power selection (3.3 or 5 V)

Related Documentation

- ProSLIC LINC™ User Guide

Functional Block Diagram



1. Introduction

The ProSLIC Si321x evaluation platform is a modular system consisting of a generic motherboard and one or more Si321x device-specific daughter cards. Using the EVB hardware and ProSLIC LINC™ software, one can easily configure, control, and monitor Si321x operation. Up to eight Si321x daughter cards may be stacked vertically and accessed using uniquely-assigned timeslots on the common PCM interface and the SPI in daisy-chain mode.

1.1. ProSLIC LINC evaluation software

The ProSLIC LINC software is an executable program that allows control and monitoring of the ProSLIC. It utilizes the primary LPT port of a standard PC to communicate to the ProSLIC's SPI port.

To install the software, insert the Silicon Laboratories ProSLIC CD into the computer. The setup routine can be invoked by running the setup.exe program in the root directory of the CD.

Invoking the ProSLIC LINC is achieved by double clicking the ProSLIC LINC icon. Refer to the ProSLIC LINC User Guide for software operation.

1.2. Si321xPPT-EVB ProSLIC Evaluation Board Description

Si321x EVB daughter cards currently supported by this hardware solution are listed in Table 1 along with supporting hardware schematics and layout references included in this data sheet.

Table 1. Supported Si321x EVB Daughter Cards

EVB Daughter Card Board Description	Schematic Figures	Layout Figures
Si3210/5/6 QFN with Si3201 integrated line interface	1, 2, 3	4, 5, 6
Si3210/5/6 QFN with discrete line interface	7, 8, 9	10, 11, 12
Si3210/5/6M QFN with Si3201 integrated line interface	13, 14, 15	16, 17, 18
Si3210/5/6M QFN with discrete line interface	19, 20, 21	22, 23, 24
Si3210/5/6 TSSOP with Si3201 integrated line interface	25, 26, 27	28, 29, 30
Si3210/5/6 TSSOP with discrete line interface	31, 32, 33	34, 35, 36
Si3210/5/6M TSSOP with Si3201 integrated line interface	37, 38, 39,	40, 41, 42
Si3210/5/6M TSSOP with discrete line interface	43, 44, 45	46, 47, 48

Motherboard hardware schematics are found in Figures 49, 50, and 51.

All power and signal connections are made to the motherboard as described in Table 2.

Signal requirements for ProSLIC operation are PCLK, FS, and Serial IO. The ProSLIC motherboard has a local oscillator with a programmable logic device to provide the ProSLIC PCLK FS signals. The DIP switch (S2) sets the PCLK frequency and controls the FS enable. See Table 3 for S2 settings. JP3 and JP4 select this internal clock source or an external PCM clock source. The ProSLIC motherboard has been designed to directly connect to an Audio Precision SIA-2322 Serial Interface Adapter through the 15 pin d-connectors, P2 and P3. See Table 4 for the Audio Precision settings. The ProSLIC evaluation board has also been designed to interface with a Wandel and Goltermann PCM-4 through J8, J9, J10, and J11. See Table 5 for PCM-4 settings. A header, J5, allows access to the ProSLIC's PCM signals for connection to other PCM testing devices or an actual telephone system PCM bus. TIP and RING of the two wire analog interface is present at the RJ-11 connector, J1.

The ProSLIC evaluation board is voltage-programmable with specific jumper settings. JP1 selects 3 or 5 V ProSLIC operation. JP2 selects 3 or 5 V PCM source level compatibility. These should be placed on the expected setting.

Power is connected to the ProSLIC at J3 and J4, and supply connections are summarized in Table 1. The 5 V is always required for the buffers, U2 and U3, to interface to the parallel port. The ProSLIC can be powered from 5 V or 3 V with the placement of a jumper on JP1. The Protection Return connections on J6 are to be connected to an appropriate ground for TIP/RING fault testing. This return is tied to signal ground on board, although it has a dedicated trace for high-current conditions. Serial control of the ProSLIC is achieved by toggling select bits of a standard parallel port. The parallel port connection is available at P1 and J1.

The ProSLIC card can be daisy-chained by simply stacking the cards. Stack up to eight cards by aligning JS1–JS6 and pressing together. The ProSLIC LINC Software allows channel-specific commands by clicking the *Daisy Chain* button.

Table 2. Motherboard Power Connections J2, J3, J4

	Si321xDC	Si321xMDC
VBRING	NC	NC
VBHI	NC	NC
VBLO	NC	NC
GND		
GND	GND[1]	GND[1]
GND		
+3 V	+3.3 V[2]	+3.3 V[2]
+5 V	+5 V	+5 V
+VIN	+9 to 12 V[3]	+5 V[3]

Notes:
1. All three GND connection points are electrically connected on the board.
2. +3.3 V is only necessary if that is the desired VDD for operation. Si321x chooses +3.3 V or +5 V based on the SP1 of the motherboard (see schematic).
3. This may be changed based on application-specific circuits. Consult the dc-dc converter spreadsheet for other possible values.

1.3. ProSLIC Evaluation Board Setup

To prepare the ProSLIC evaluation board for use, perform the following steps:

1. Set power supplies to 3.3 V, 5 V, and 12 V.
2. With these supplies off, connect them to J3 and J4 corresponding to the silk screen designators.
3. Connect the PC's parallel port (LPT1) to P1 (or J1) using a 25-pin D male-to-male cable.
4. Select the on-board PCM clock source, or select an external PCM source, and connect an Audio Precision SIA-2322 to P2 and P3 or a Wandel and Goltermann PCM-4 to J8, J9, J10, and J11.
5. TIP/RING connection can be made from the RJ-11 to a phone or telephony test equipment.
6. Invoke the ProSLIC LINC software.
7. Turn the power supplies on and press the ProSLIC evaluation board reset button (S1).
8. Click the "Reinitialize" button in the ProSLIC LINC software panel

The ProSLIC is now ready to perform its linecard function.

Table 3. On-Board PCLK Settings (S2)

S2-1,2,3	S2-4	S2-5	S2-6	S2-7	S2-8
PCLK frequency	unused	unused	unused	unused	FS enable
0,0,0 = 8.192 MHz 0,0,1 = 4.096 MHz 0,1,0 = 2.048 MHz 0,1,1 = 1.024 MHz 1,x,x = 512 kHz	x	x	x	x	0 = FS disabled 1 = FS enabled
Note: 1 = on.					

Table 4. Audio Precision SIA-2322 DIP Switch Setting

Receiver Mode				Transmitter Mode			
00111001	00000010	11111101	01111001	0000001	00000010	11111101	01111001
Note: 256 kHz PCLK and 8 kHz FS.							

Table 5. Wandel and Goltermann PCM-4 Settings

General Configuration	2.14
General Configuration	3.13
General Configuration	4.13
For μ-law add the following:	
General Configuration	7.12
General Configuration	7.22

2. Schematics

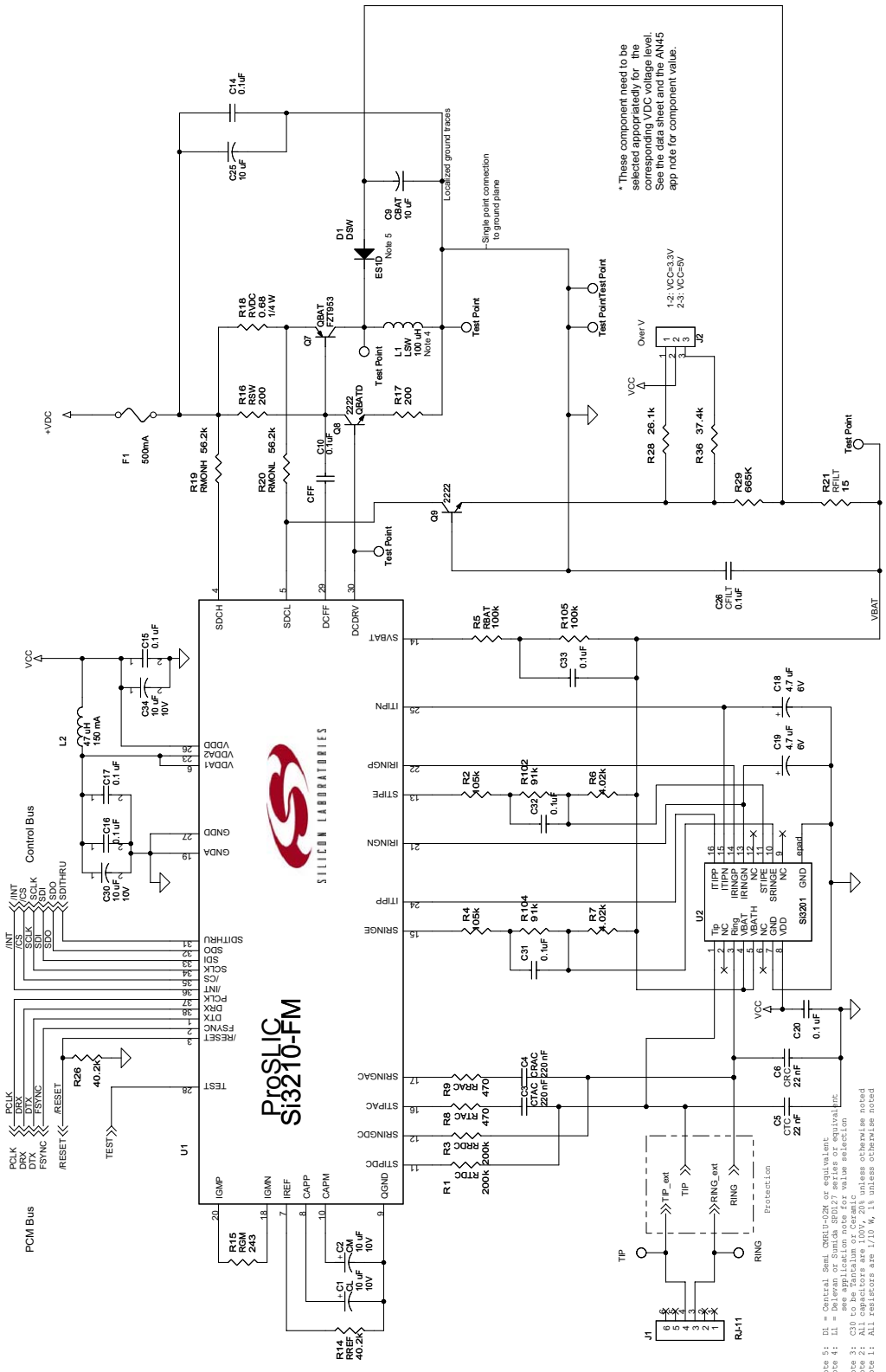


Figure 1. Si321x QFN with Si3201 Schematic (1 of 3)

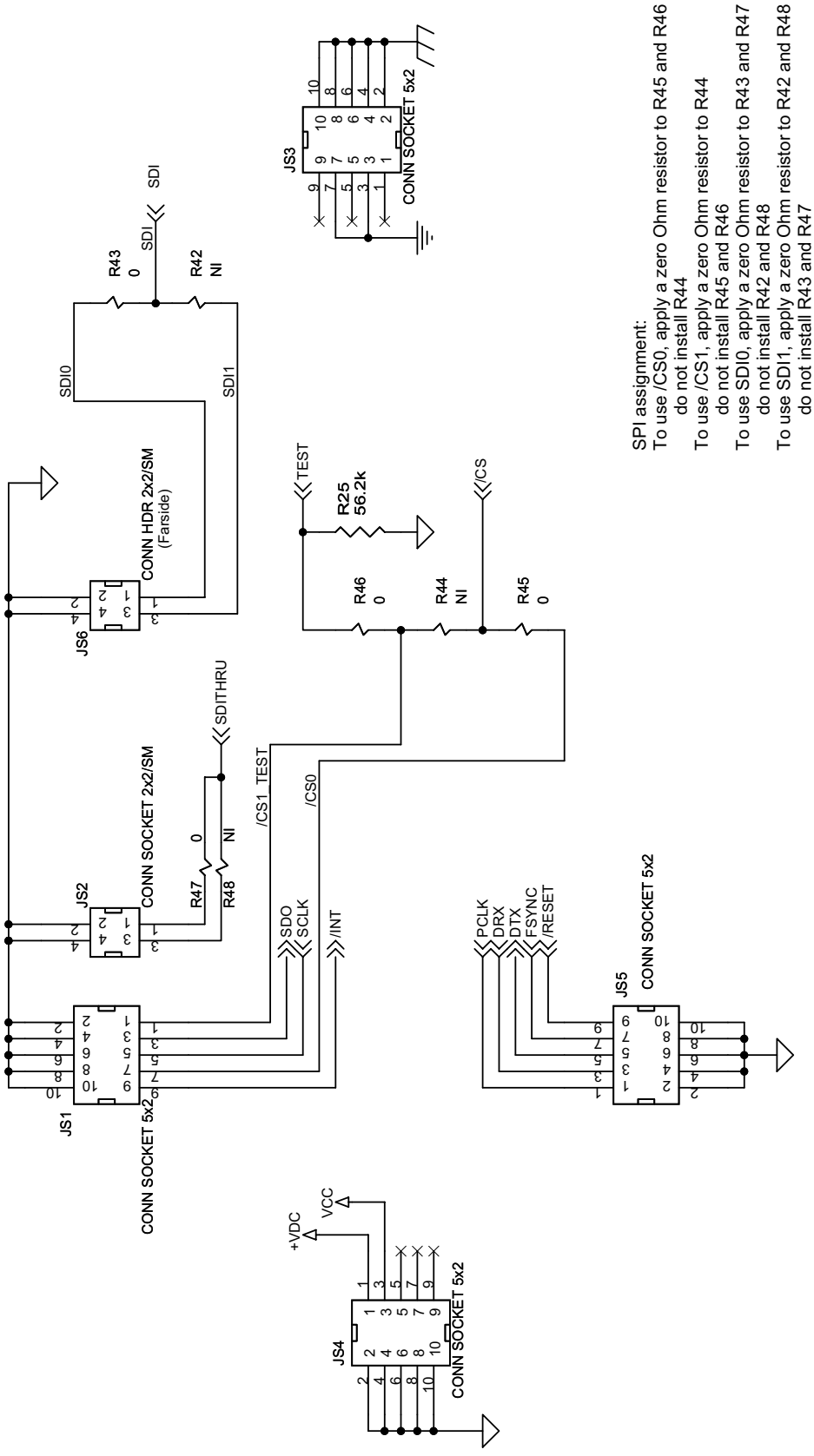


Figure 2. Si321x QFN with Si3201 Schematic (2 of 3)

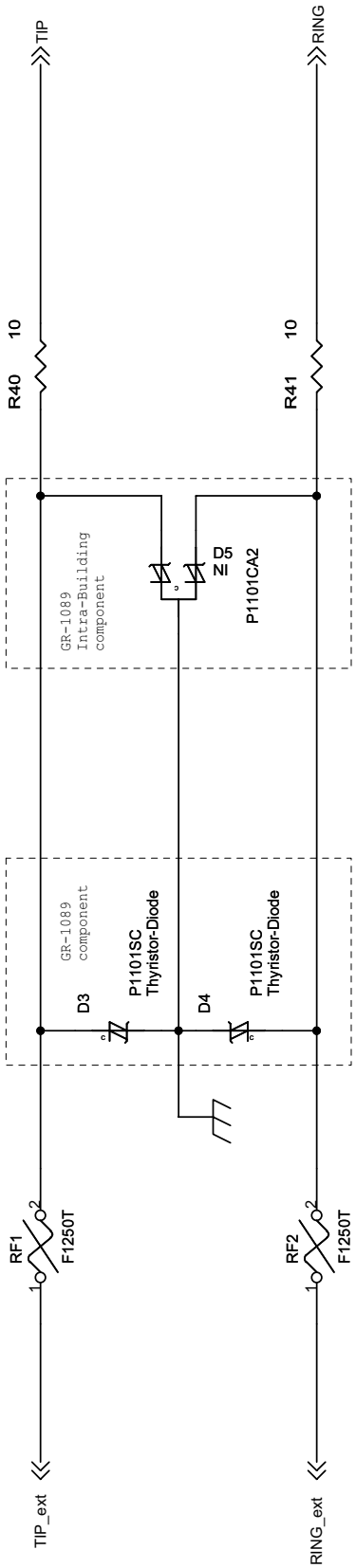


Figure 3. Si321x QFN with Si3201 Schematic (3 of 3)

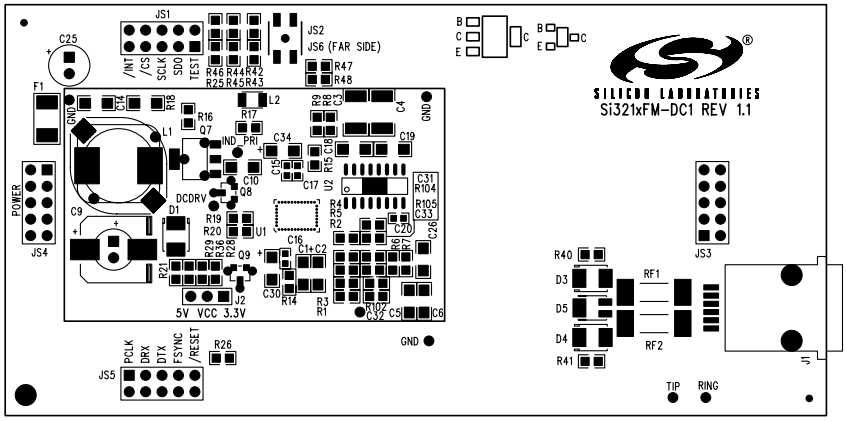


Figure 4. Si321xDCQ-EVB with Si3201 Silkscreen

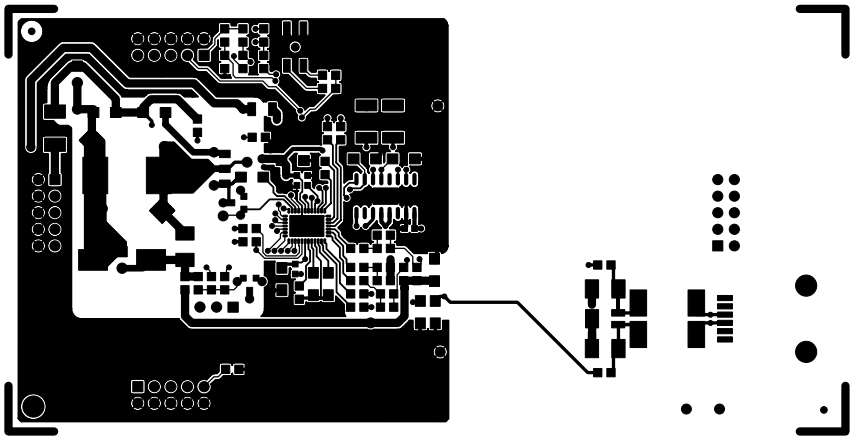


Figure 5. Si321xDCQ-EVB with Si3201 Component Side

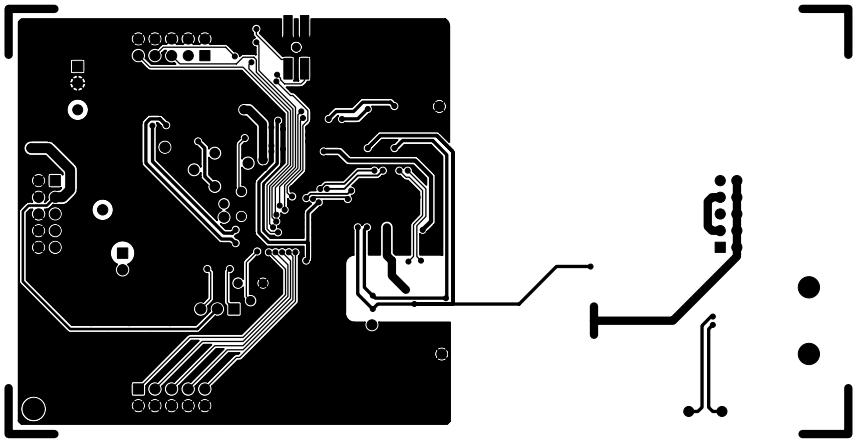


Figure 6. Si321xDCQ-EVB with Si3201 Solder Side

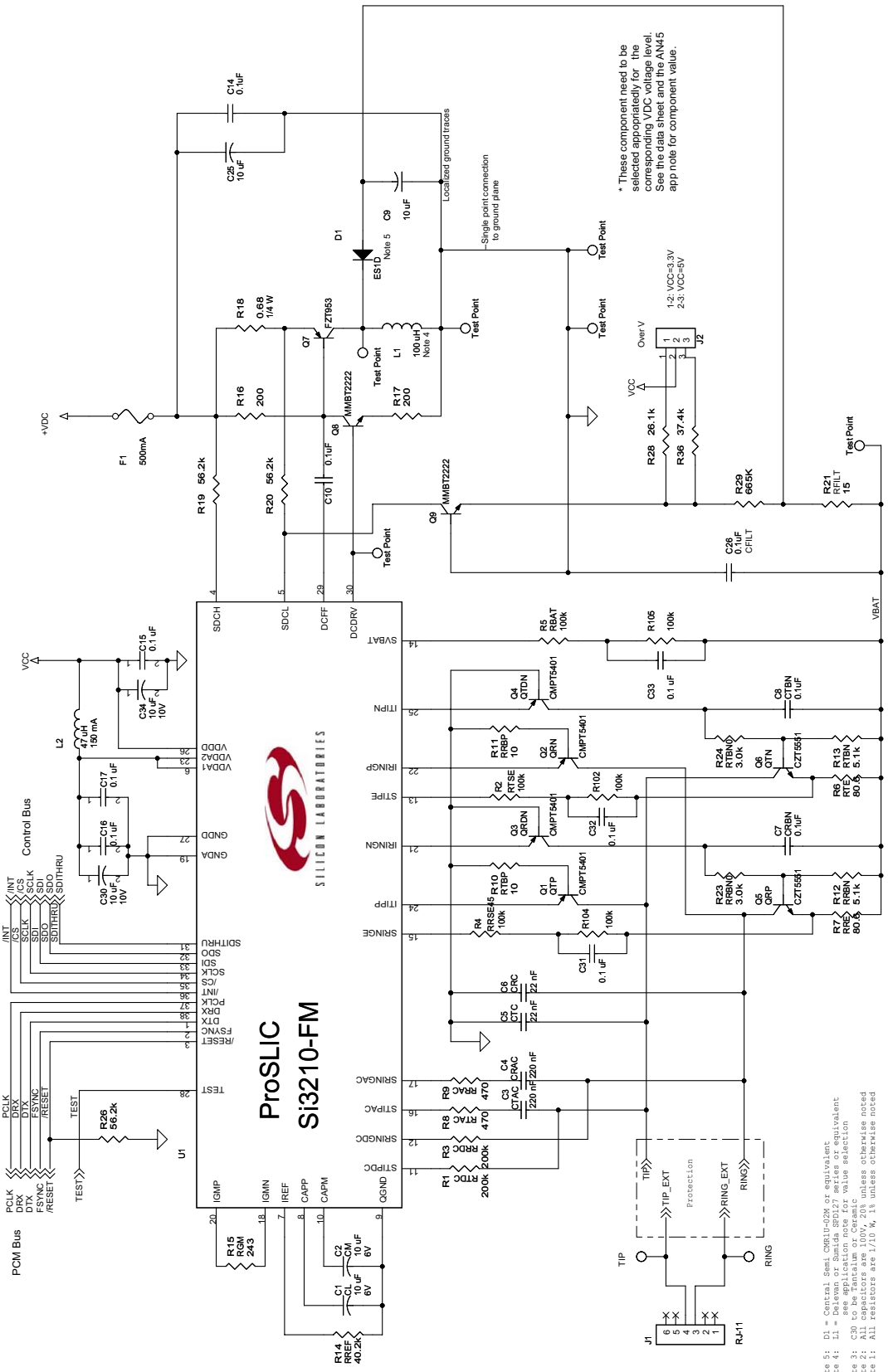


Figure 7. Si321x QFN with Discrete Evaluation Circuit (1 of 3)

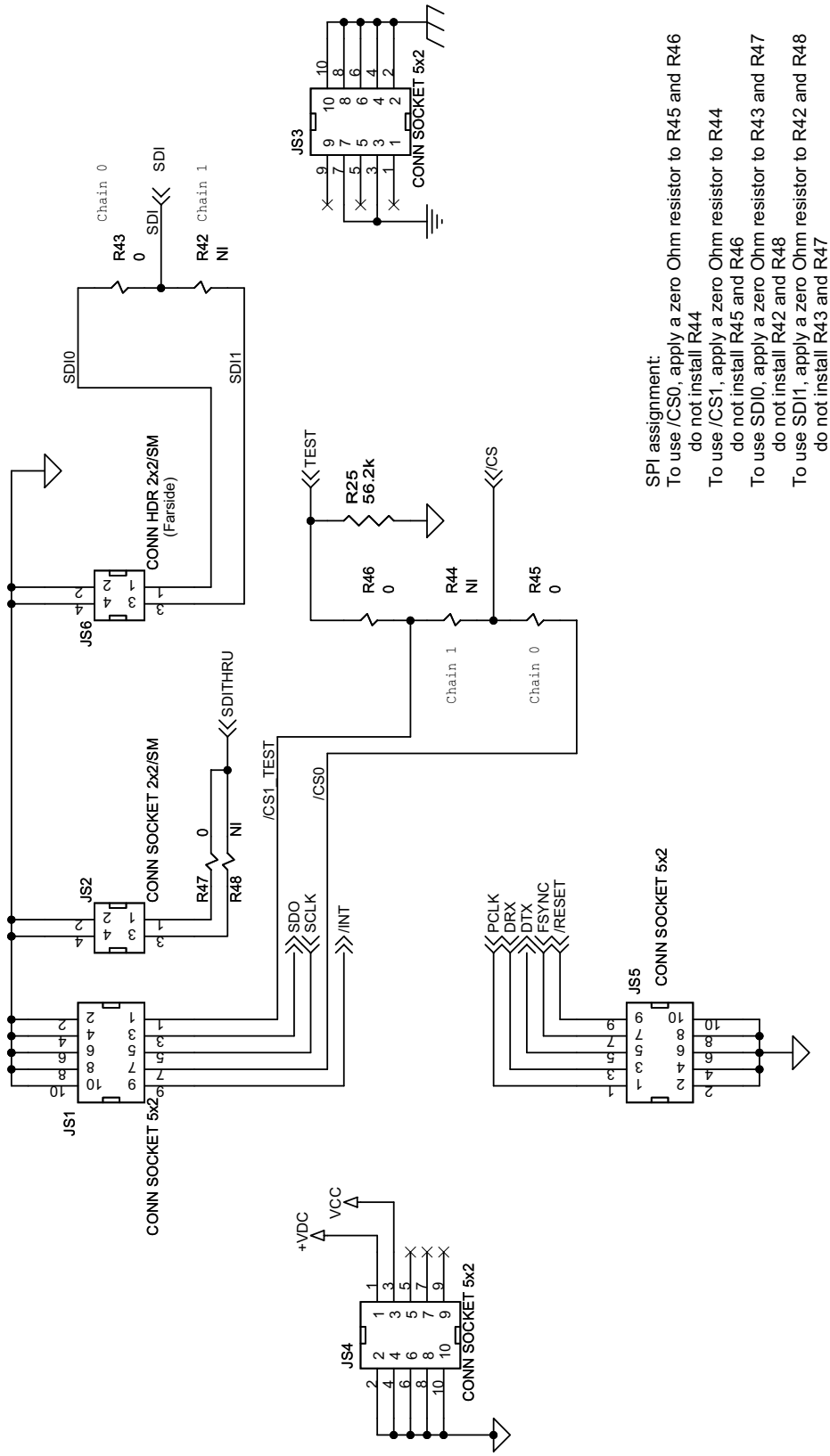


Figure 8. Si321x QFN with Discrete Evaluation Circuit (2 of 3)

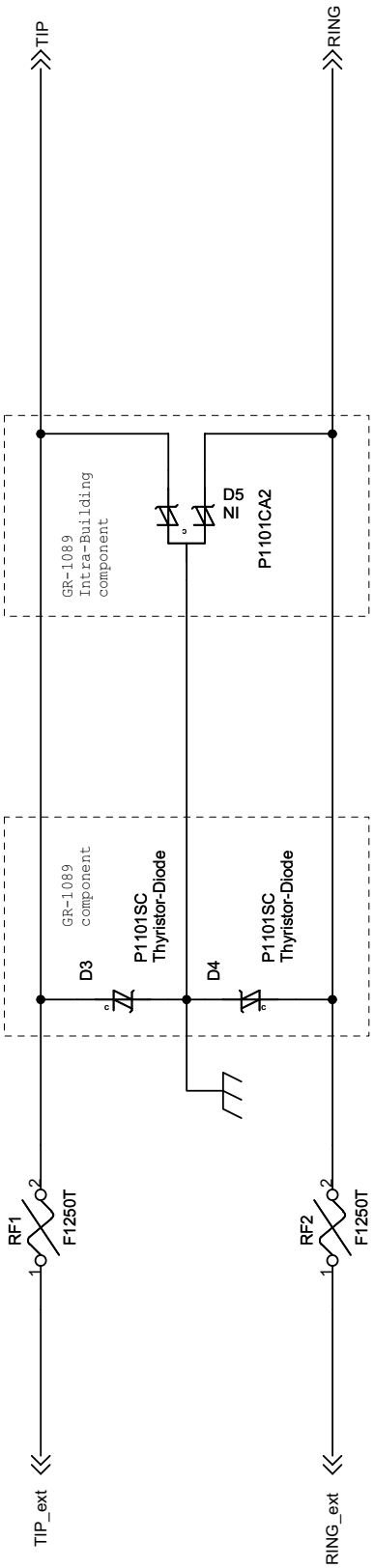


Figure 9. Si321x QFN with Discrete Evaluation Circuit (3 of 3)

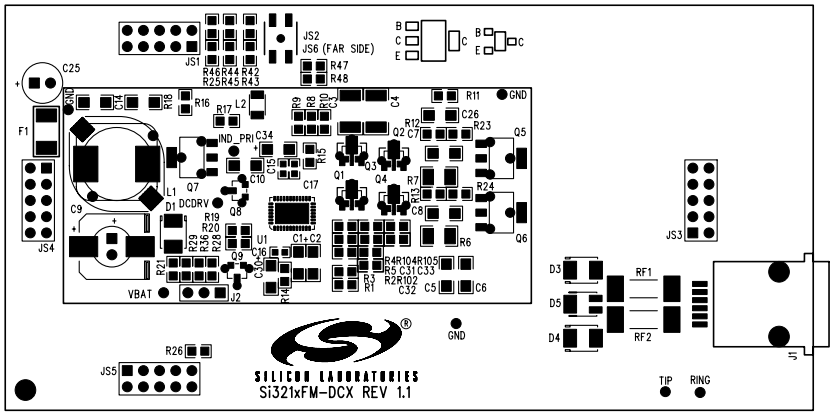


Figure 10. Si321xDCQ-EVB with Discretes Silkscreen

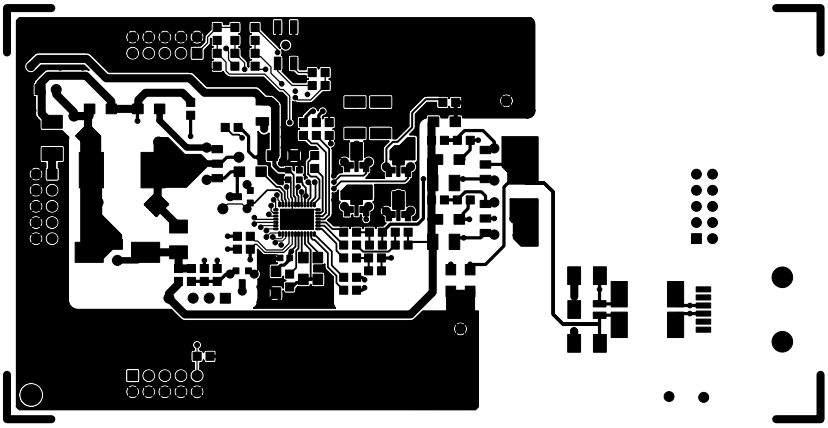


Figure 11. Si321xDCQ-EVB with Discretes Component Side

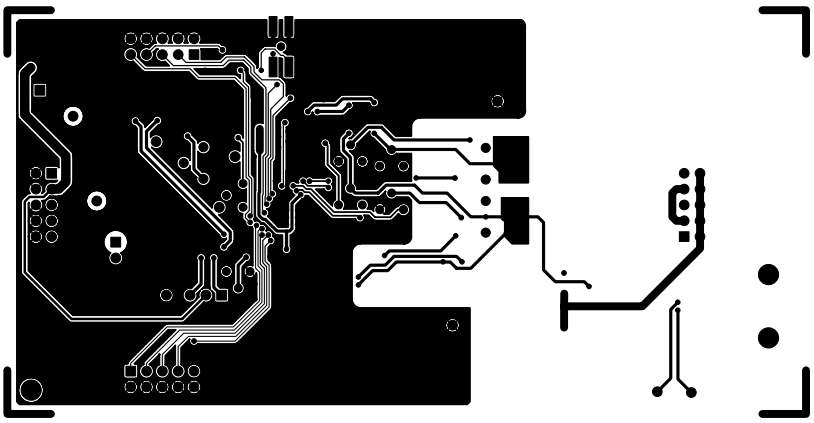


Figure 12. Si321xDCQ-EVB with Discretes Solder Side

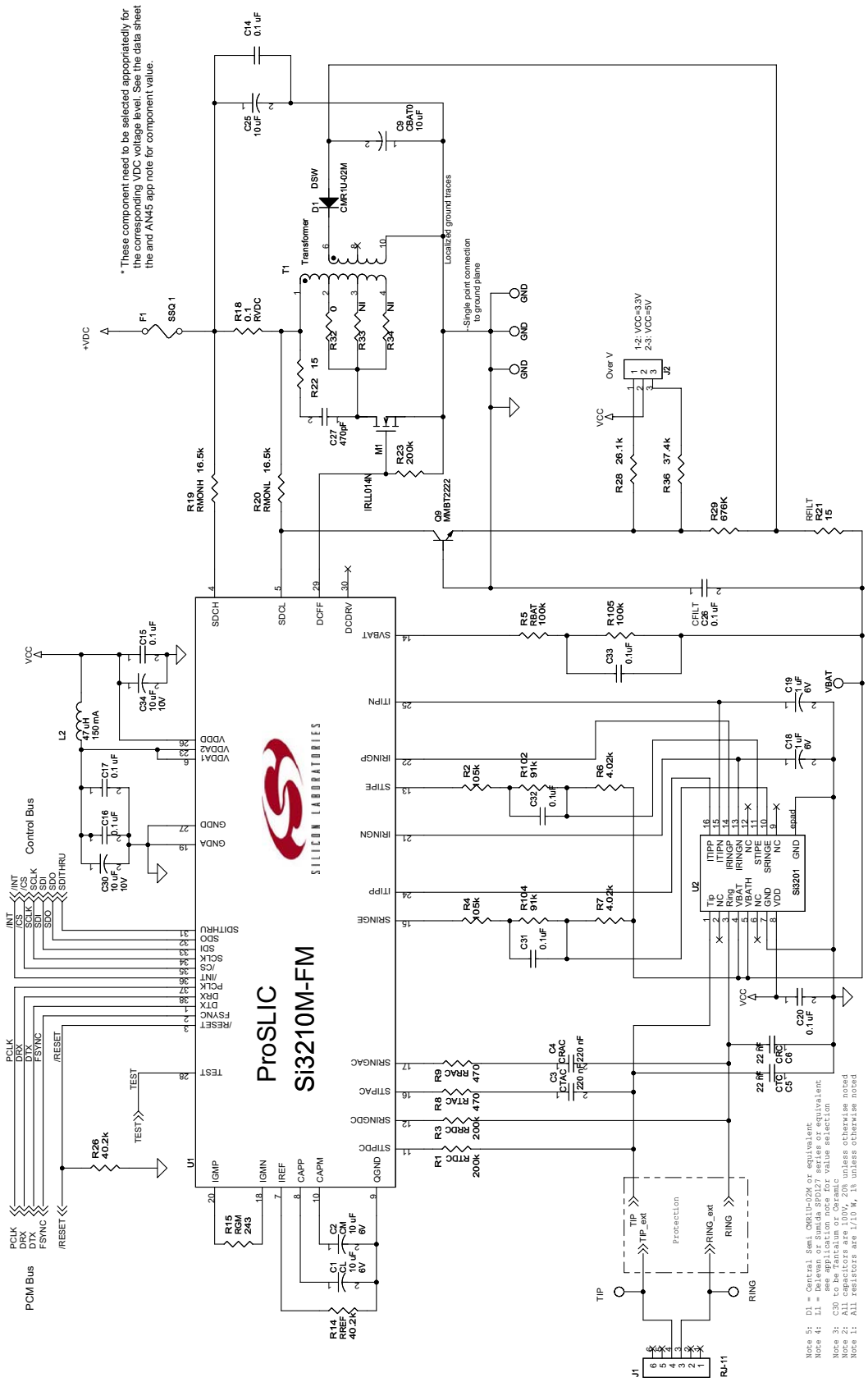


Figure 13. Si321xM QFN with Si3201 Schematic (1 of 3)

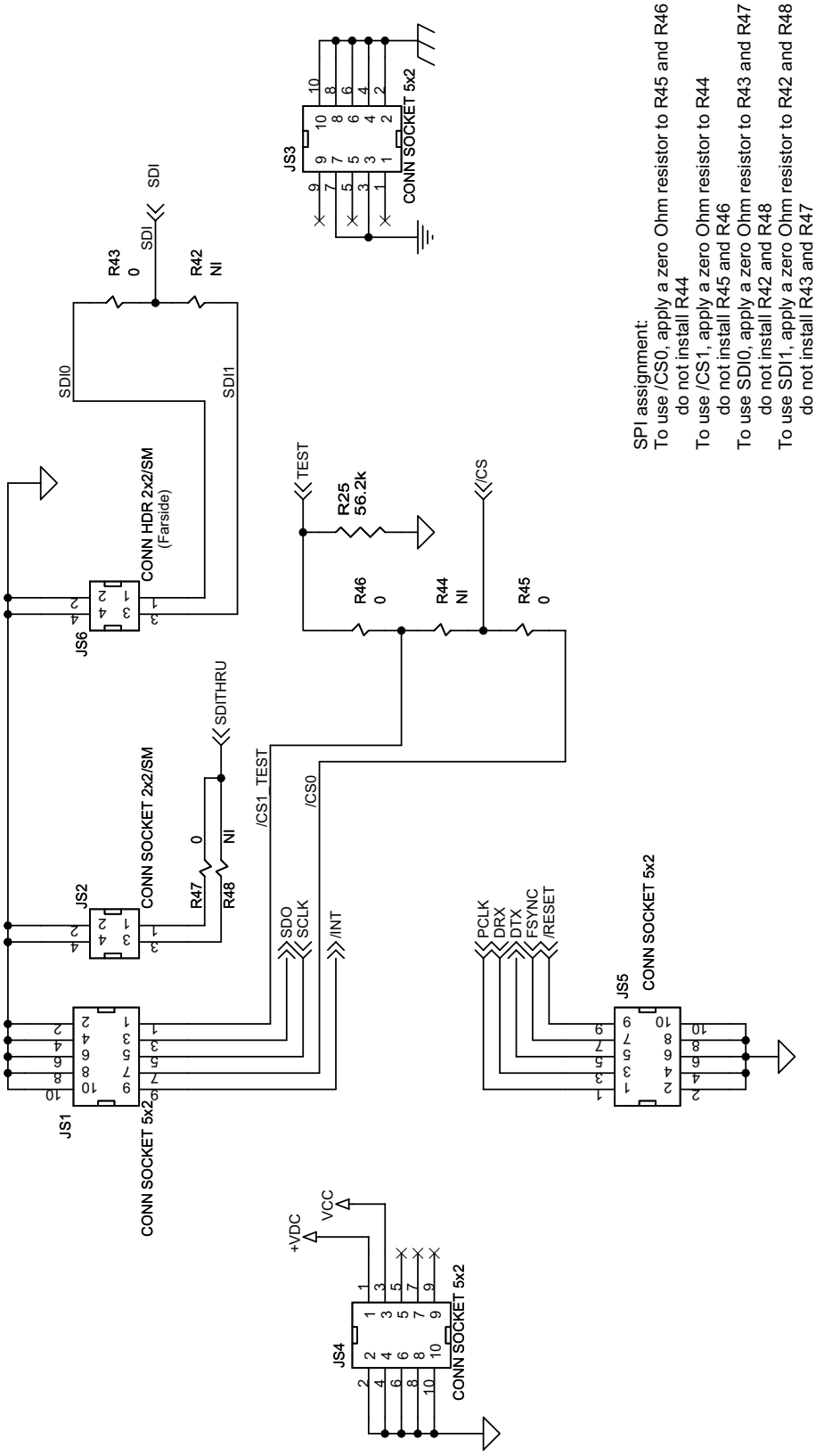


Figure 14. Si321xM QFN with Si3201 Schematic (2 of 3)

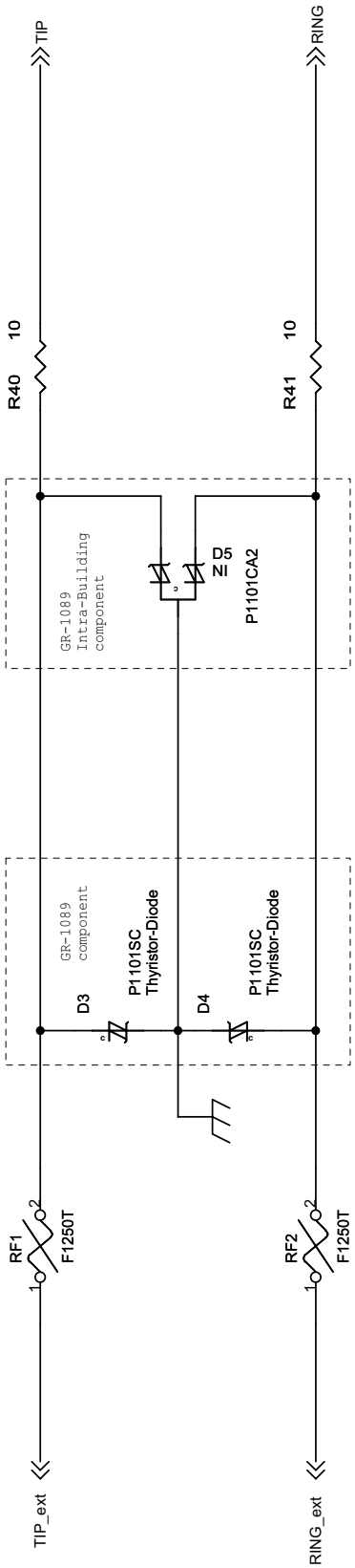


Figure 15. Si321xM QFN with Si3201 Schematic (3 of 3)

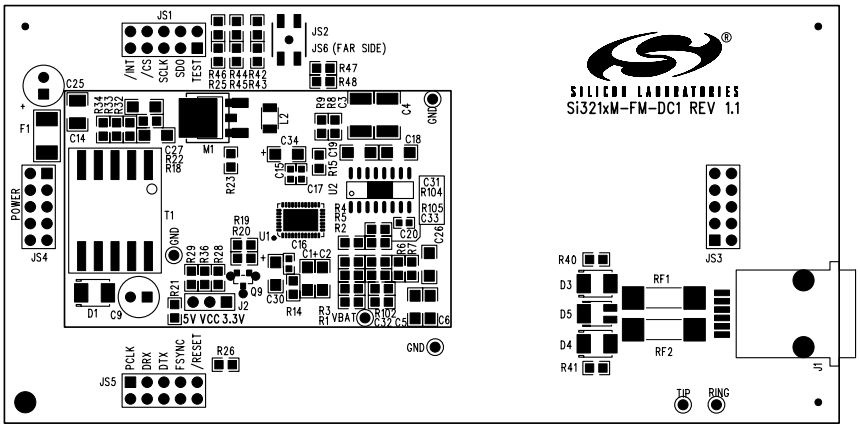


Figure 16. Si321xM-DCQ-EVB with Si3201 Silkscreen

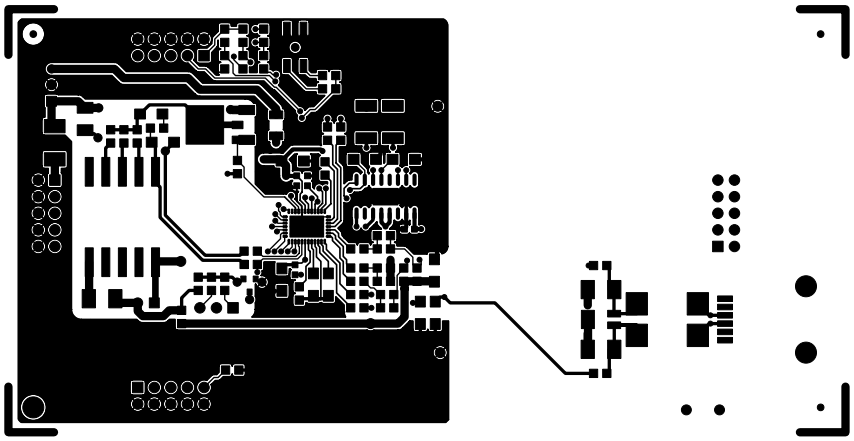


Figure 17. Si321xM-DCQ-EVB with Si3201 Component Side

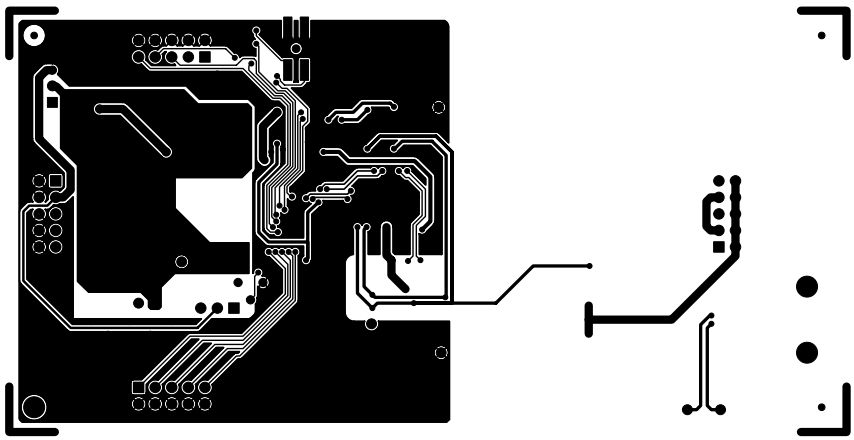


Figure 18. Si321xM-DCQ-EVB with Si3201 Solder Side

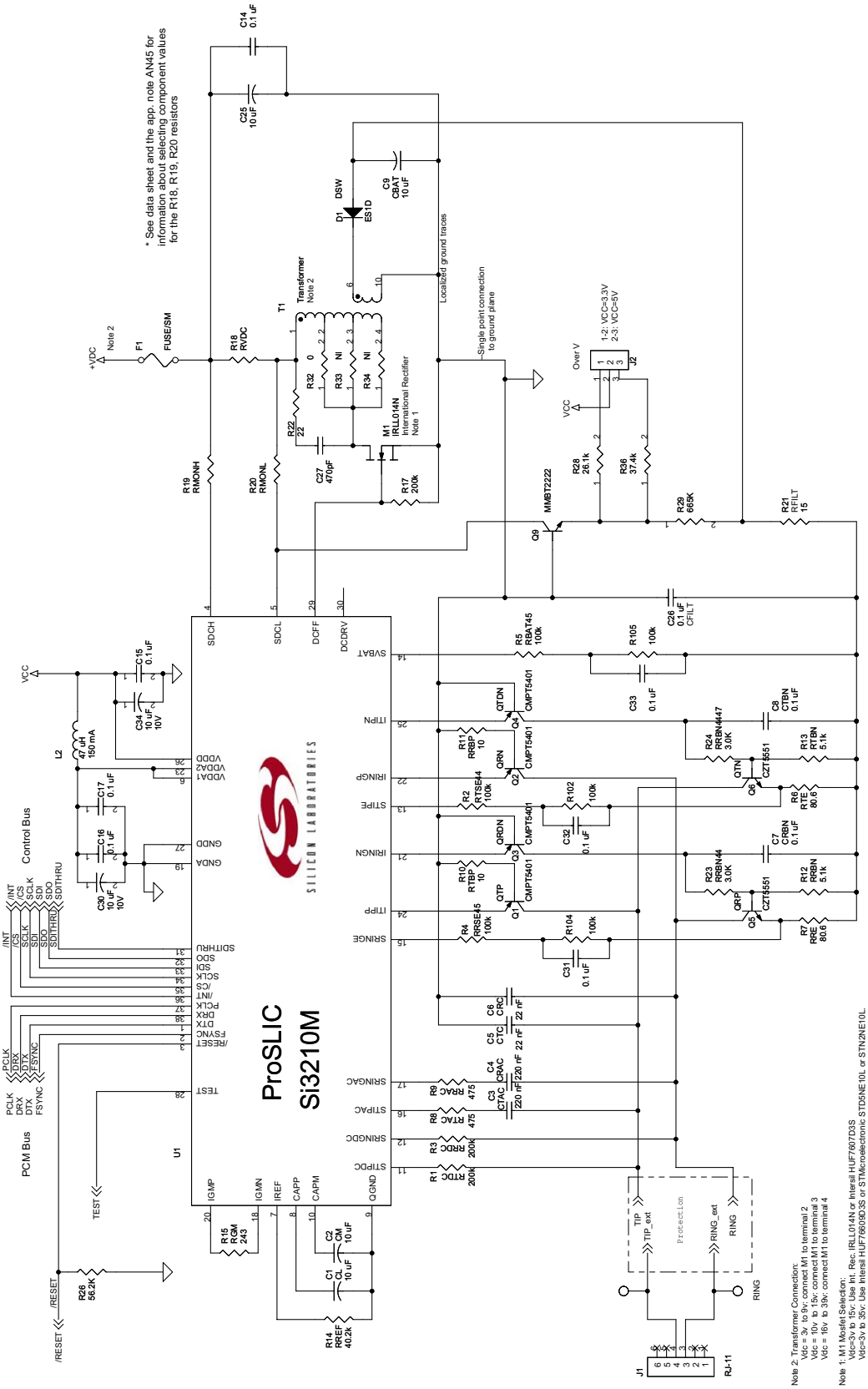


Figure 19. Si321xM QFN with Discrete Evaluation Circuit (1 of 3)

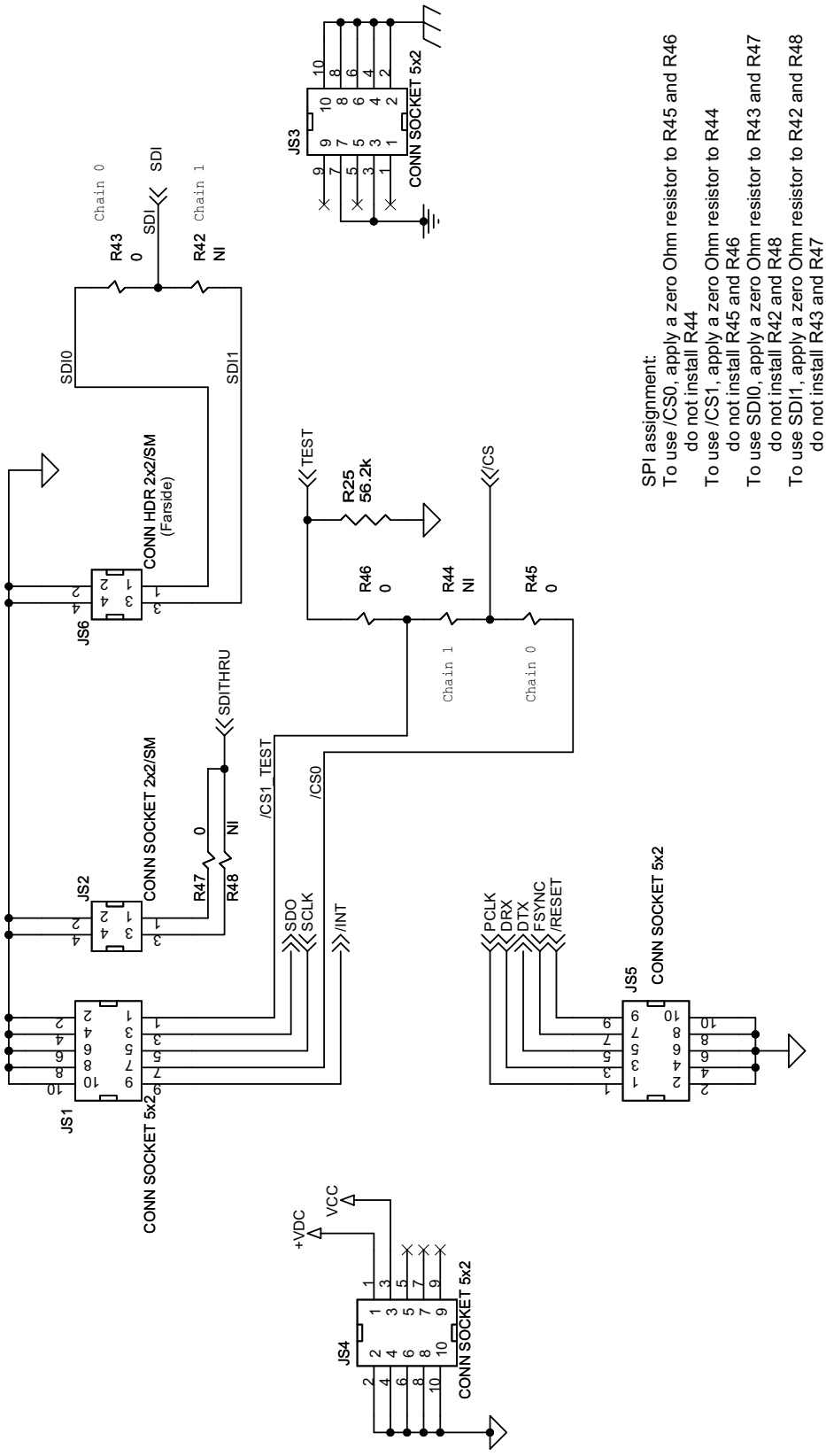


Figure 20. Si321xM QFN with Discrete Evaluation Circuit (2 of 3)

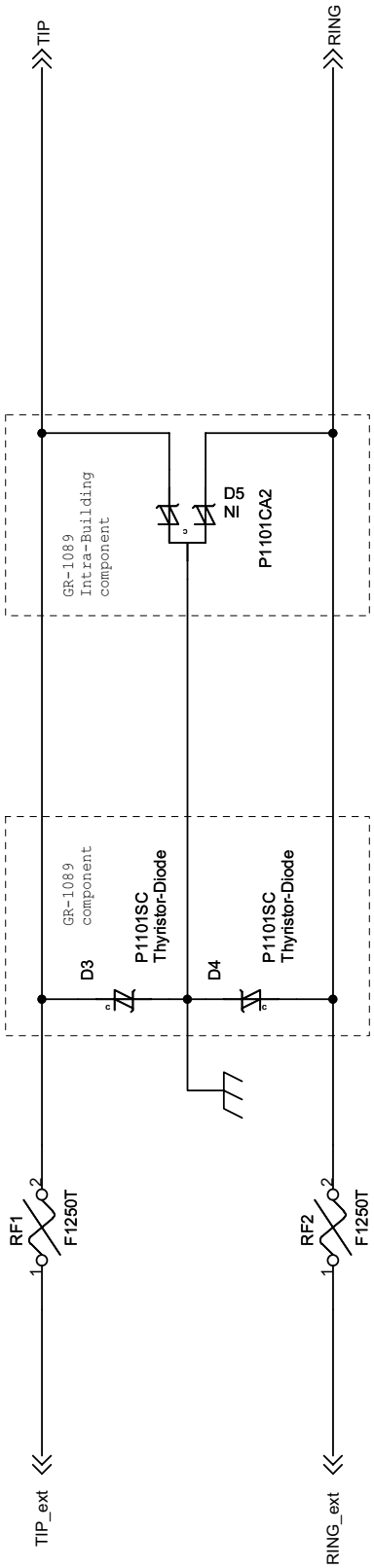


Figure 21. Si321xM QFN with Discrete Evaluation Circuit (3 of 3)

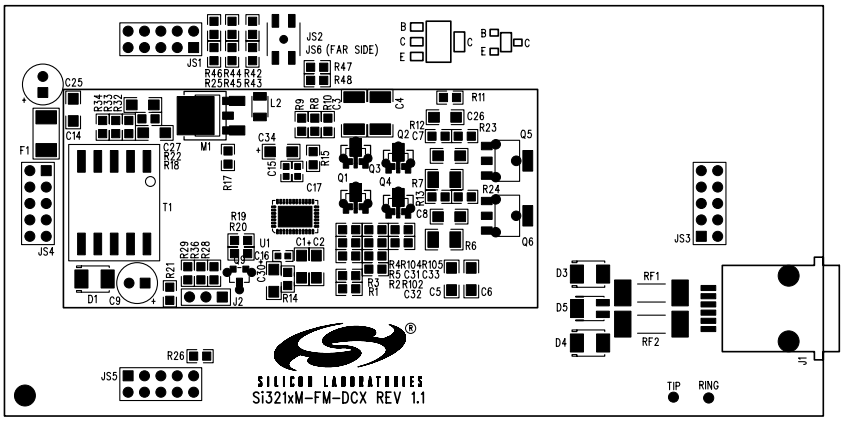


Figure 22. Si321xM-DCQ-EVB with Discretes Silkscreen

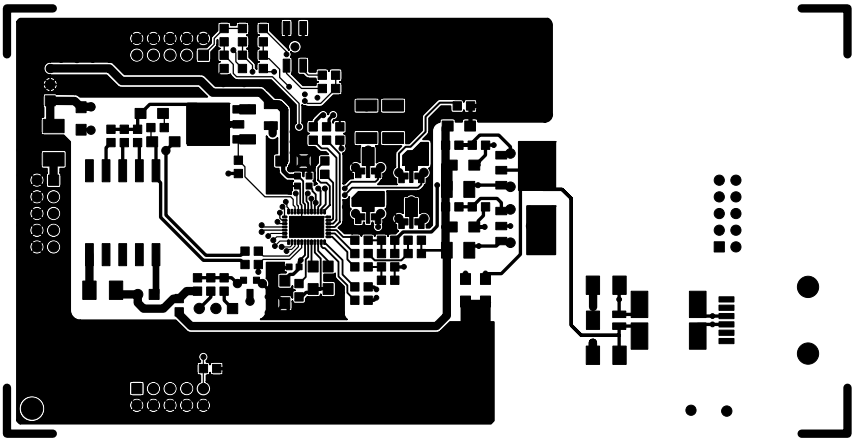


Figure 23. Si321xM-DCQ-EVB with Discretes Component Side

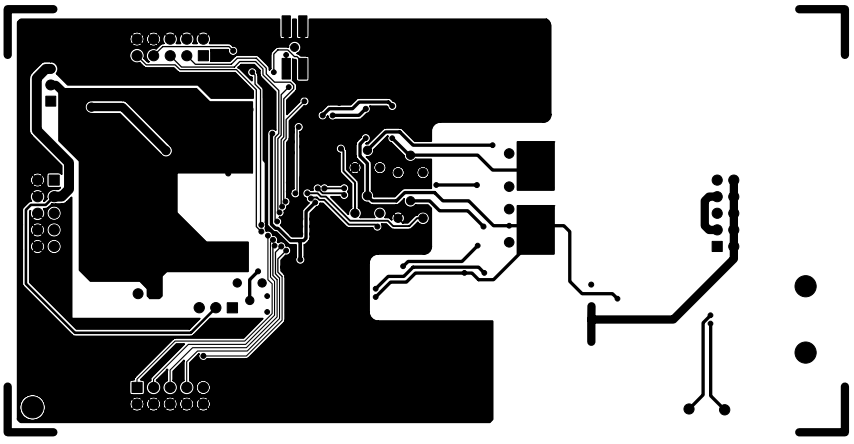


Figure 24. Si321xM-DCQ-EVB with Discretes Solder Side

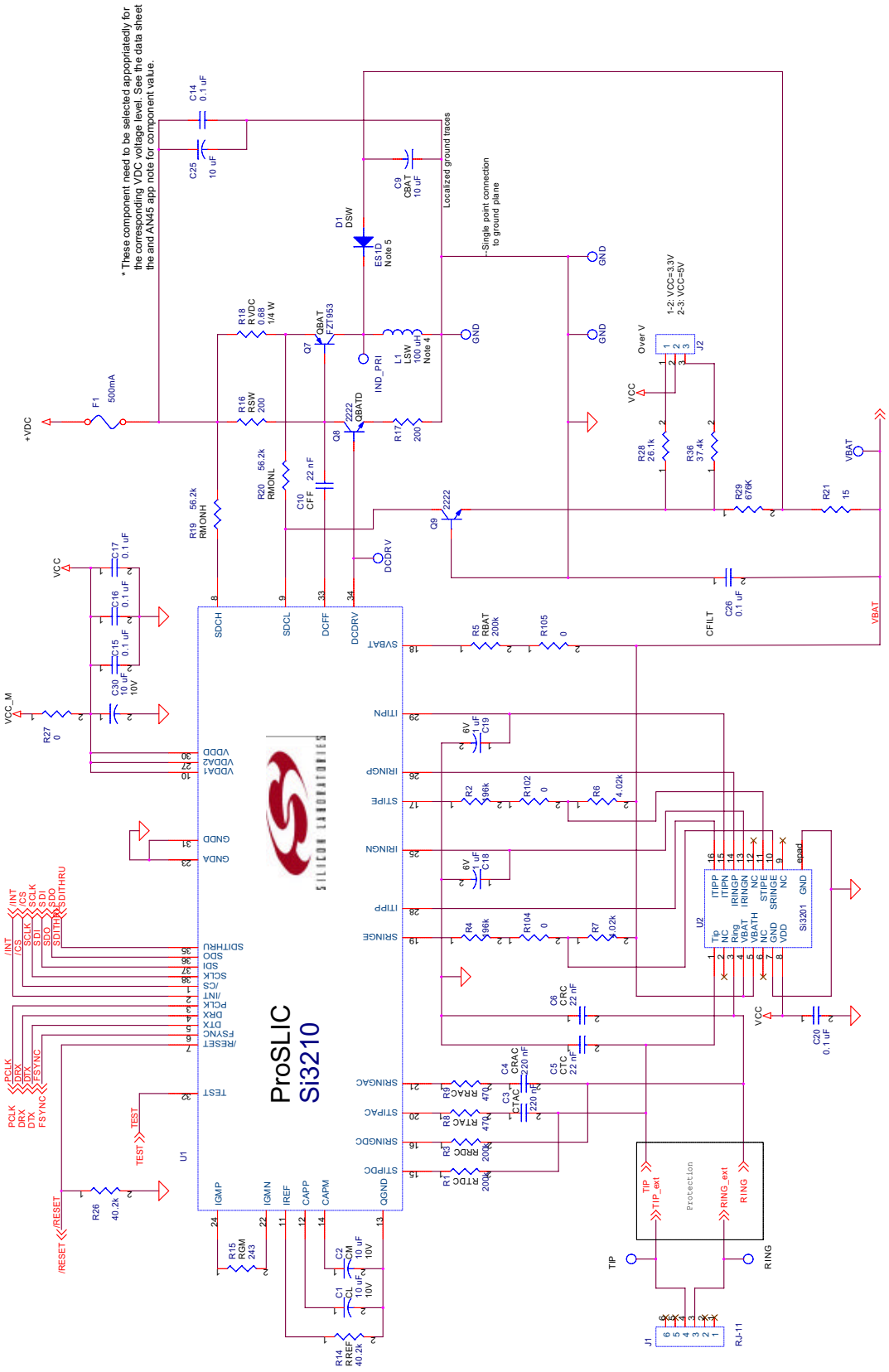


Figure 25. Si3210/15/16 TSSOP with Si3201 Schematic (1 of 3)

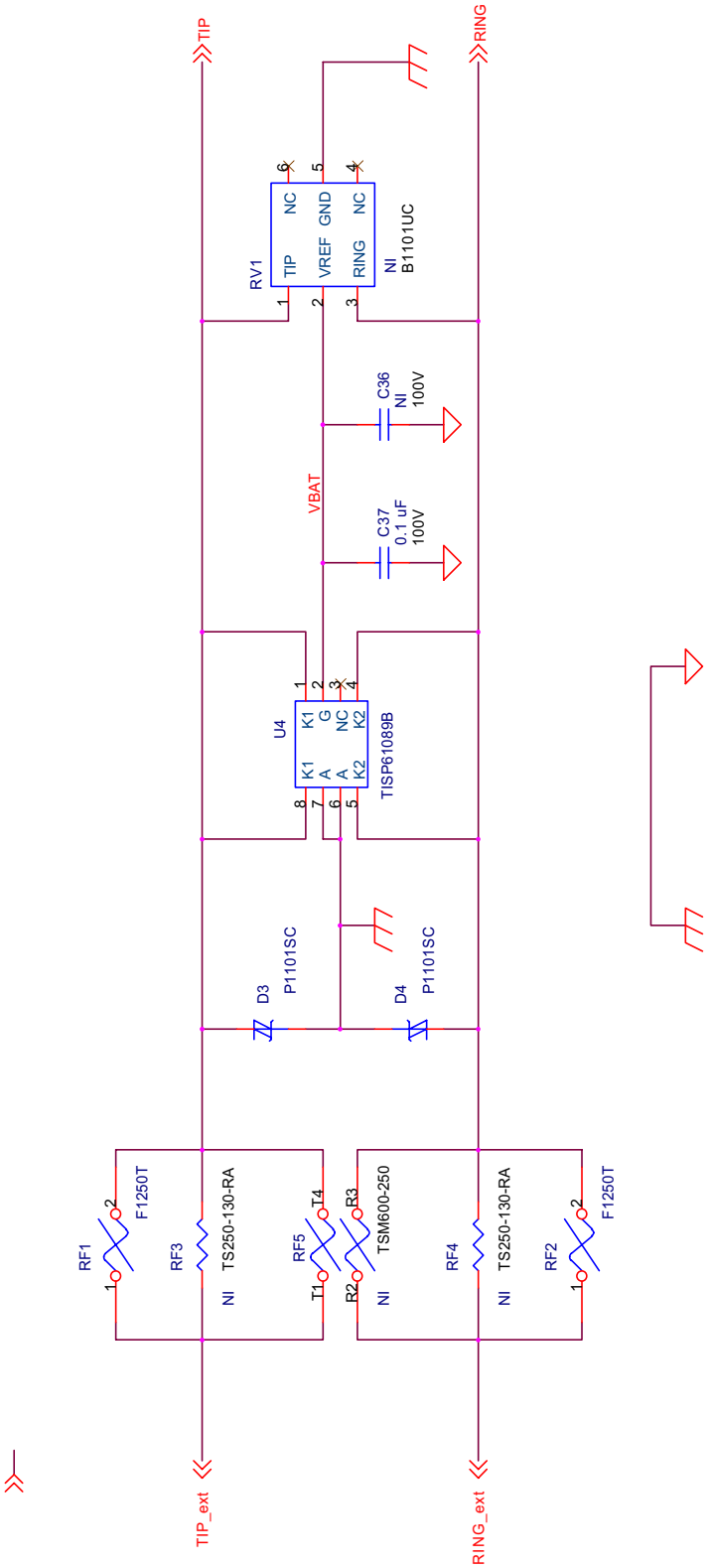


Figure 26. Si3210/15/16 TSSOP with Si3201 Schematic 2 of 3)

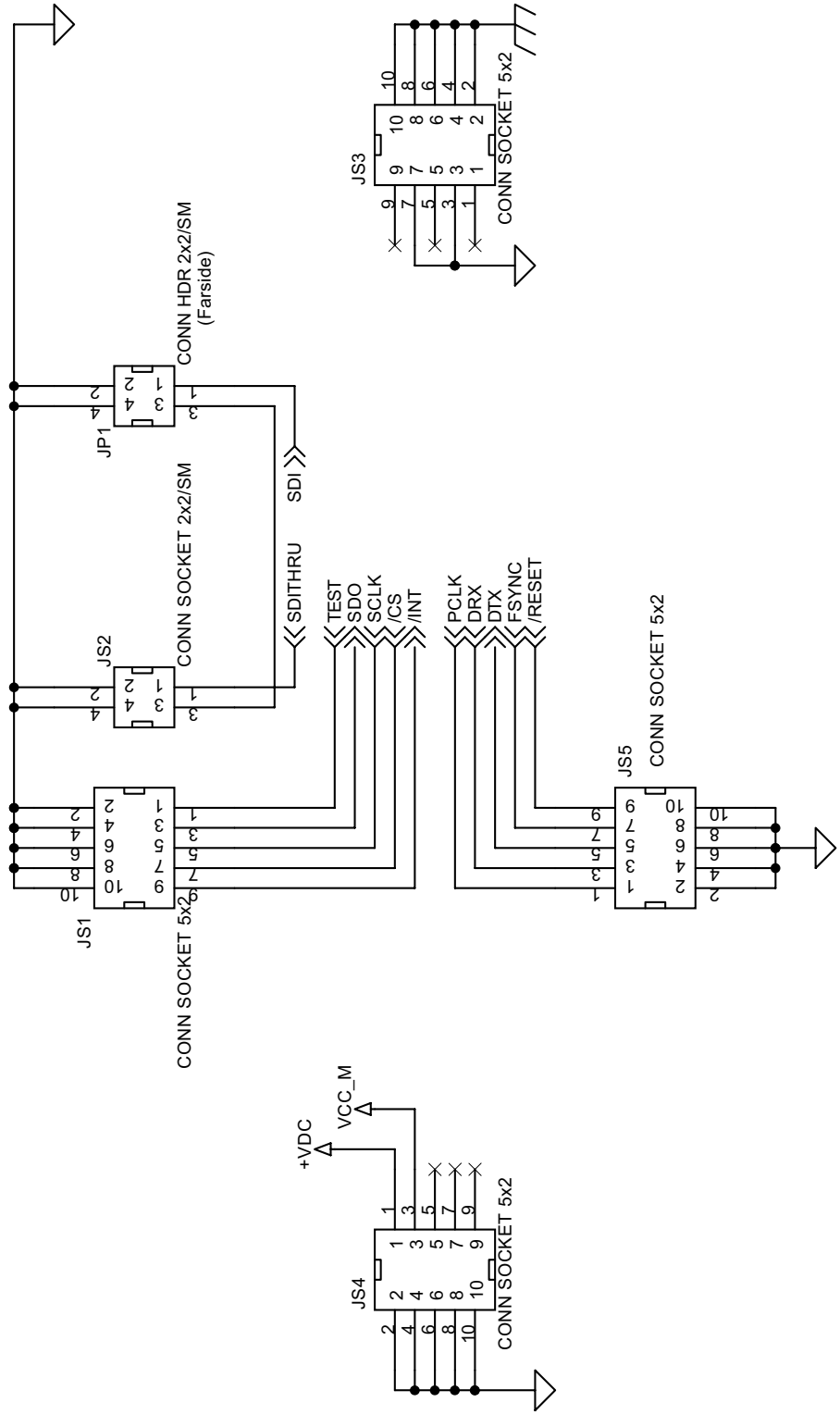


Figure 27. Si3210/15/16 TSSOP with Si3201 Schematic (3 of 3)

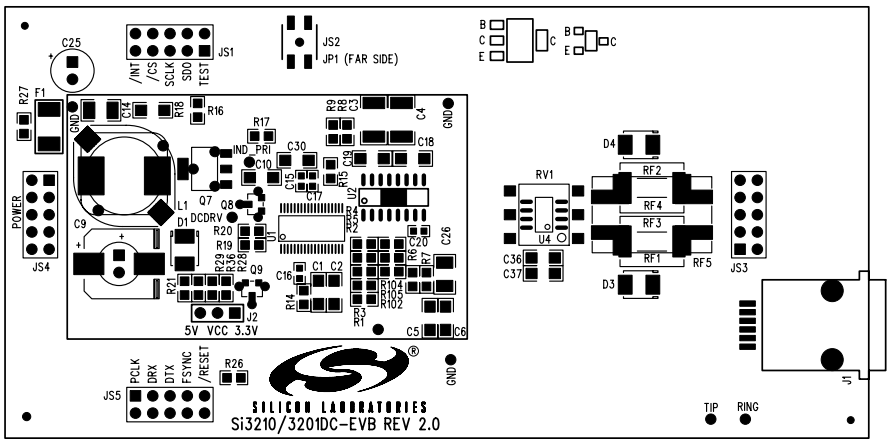


Figure 28. Si321xDC-EVB with Si3201 Silkscreen

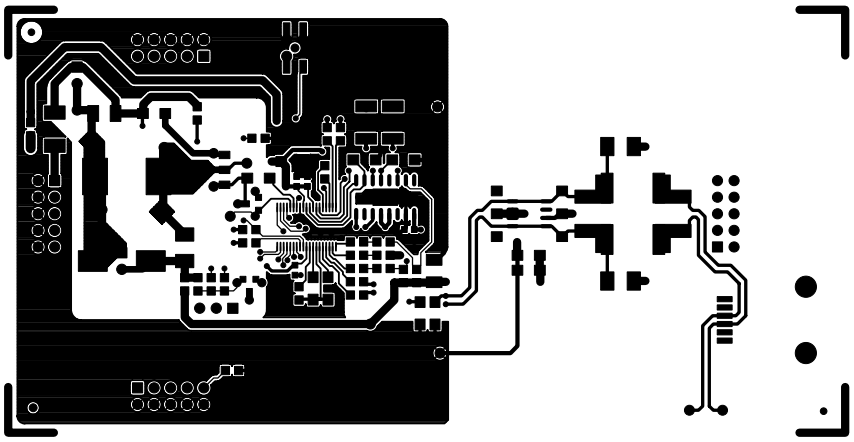


Figure 29. Si321xDC-EVB with Si3201 Component Side

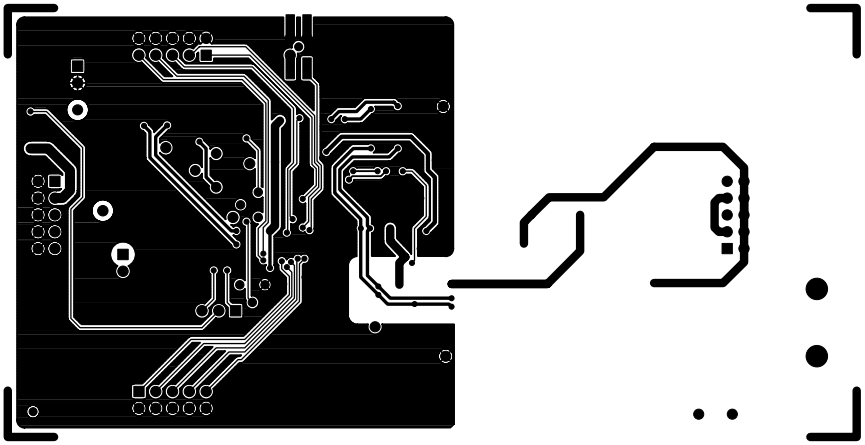


Figure 30. Si321xDC-EVB with Si3201 Solder Side

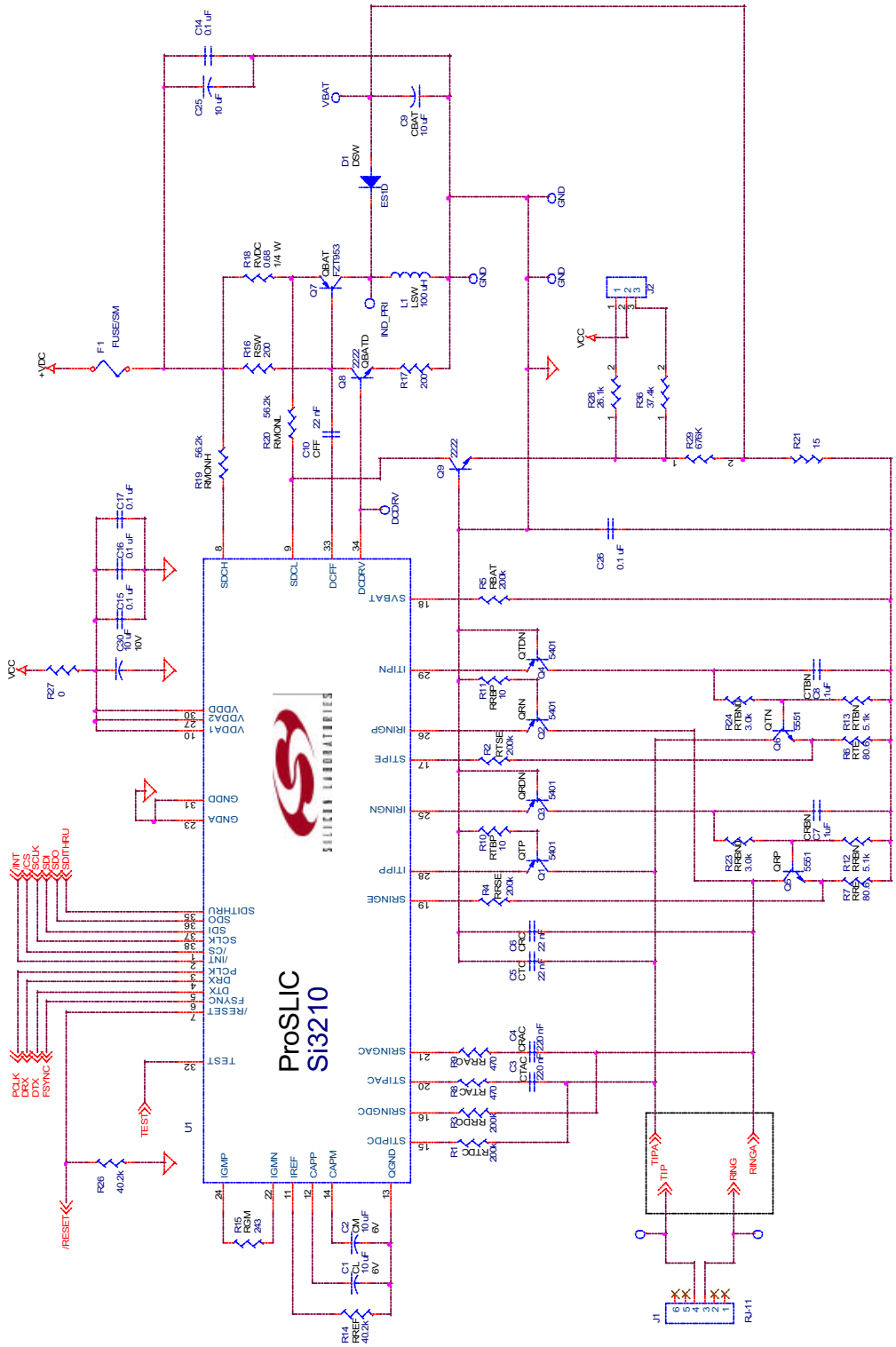


Figure 31. Si321xDC-EVB with Discretes Evaluation Circuit (1 of 3)

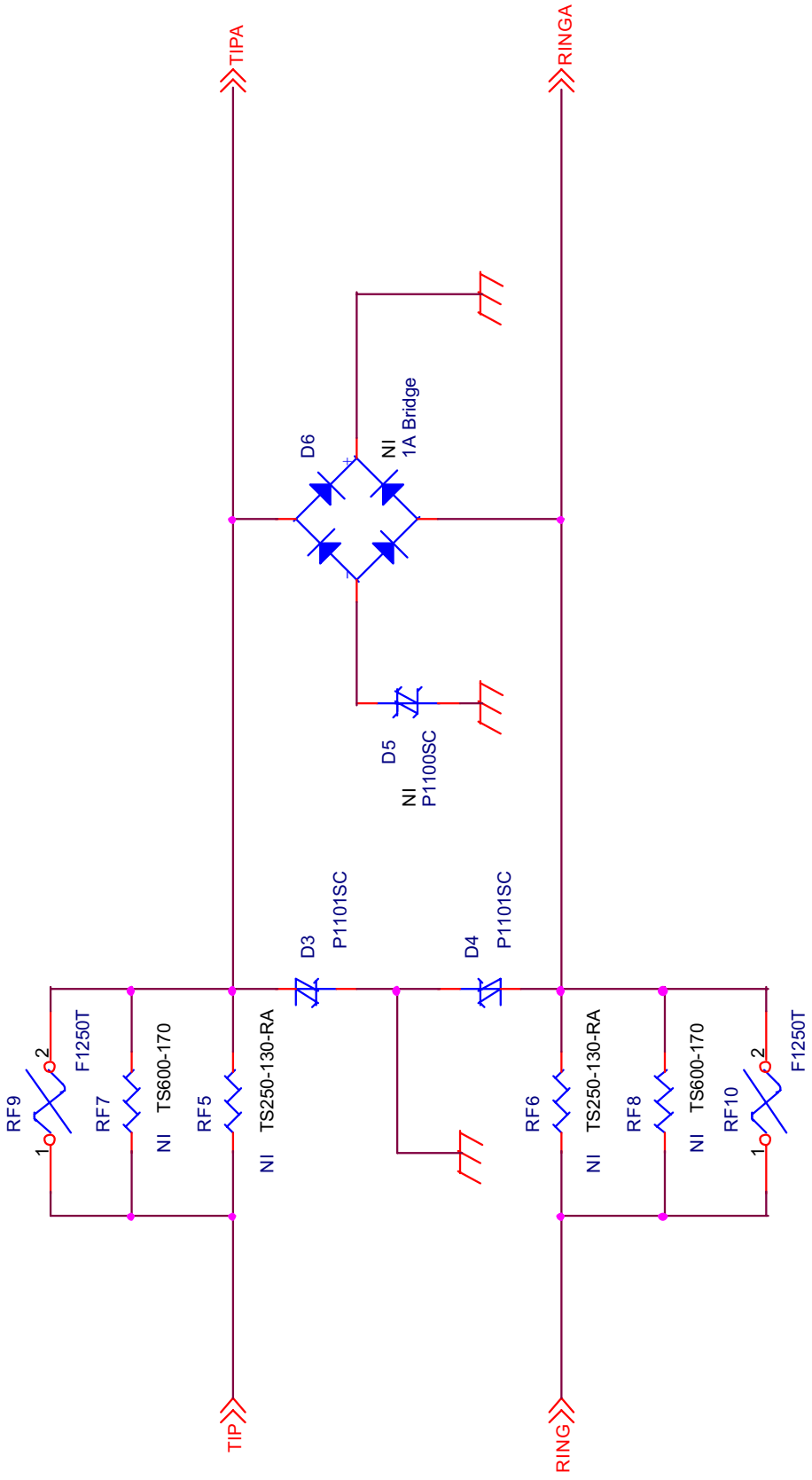


Figure 32. Si321xDC-EVB with Discretes Evaluation Circuit (2 of 3)

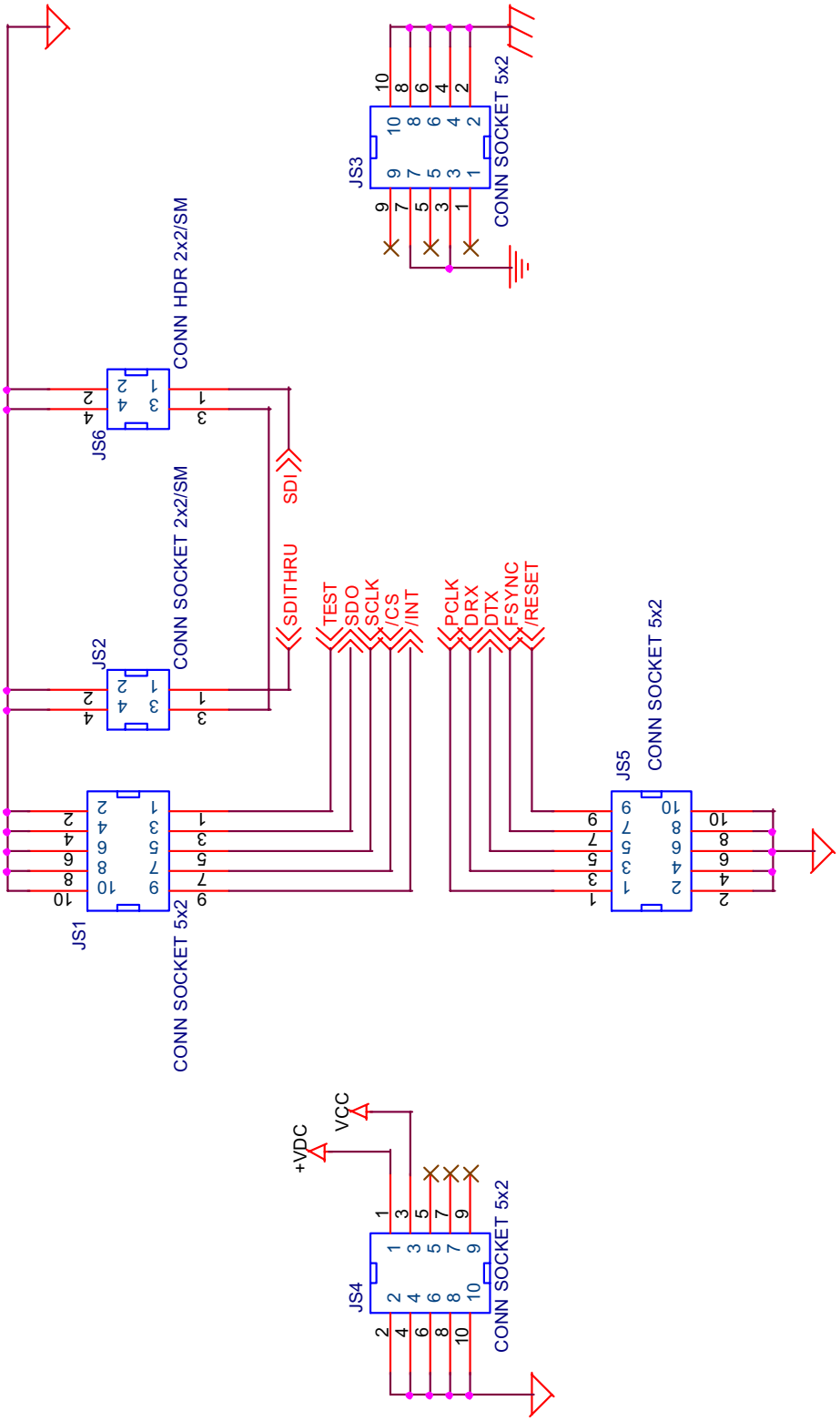


Figure 33. Si321xDC-EVB with Discretes Evaluation Circuit (3 of 3)

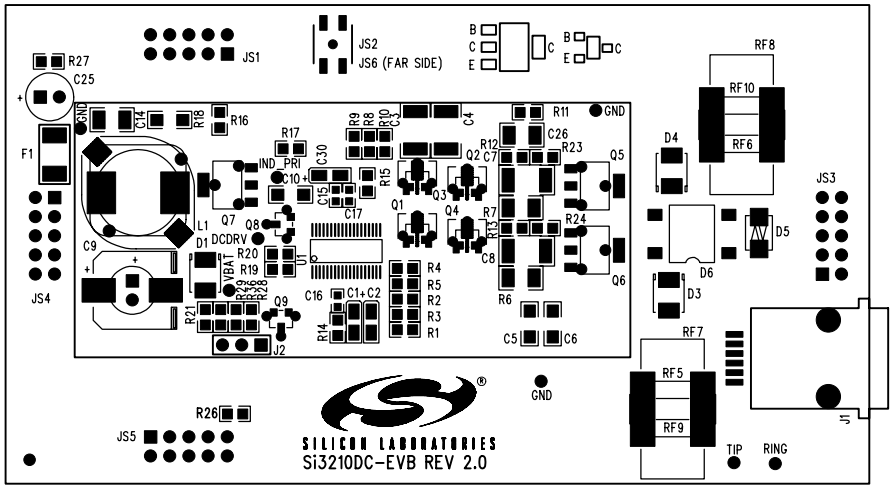


Figure 34. Si3210CARD-EVB with Discretes Silkscreen

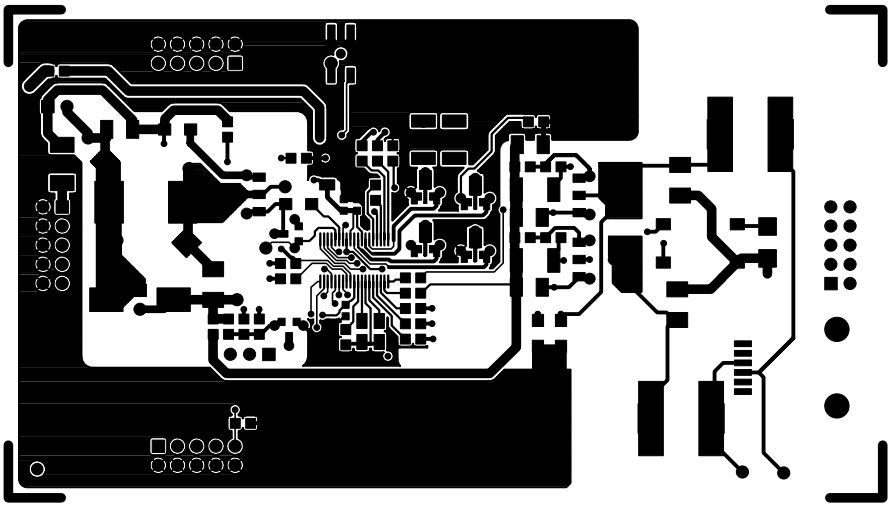


Figure 35. Si3210CARD-EVB with Discretes Component Side

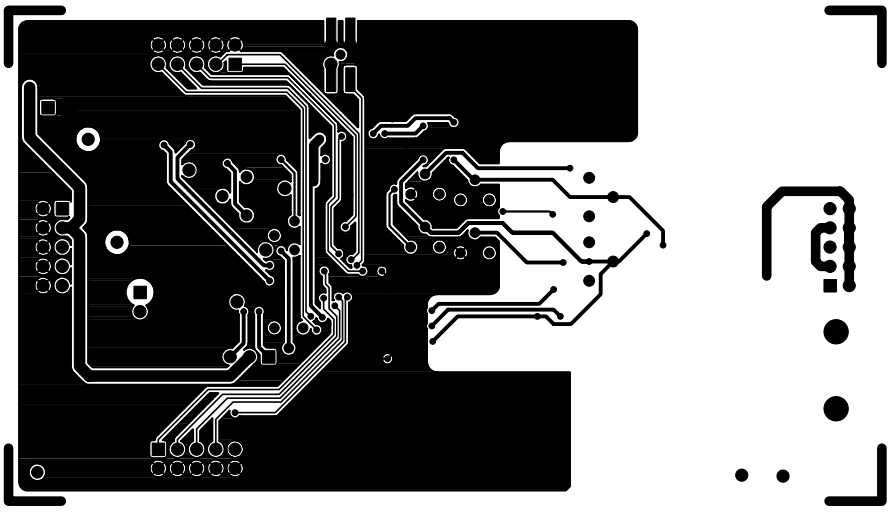


Figure 36. Si3210CARD-EVB with Discretes Solder Side

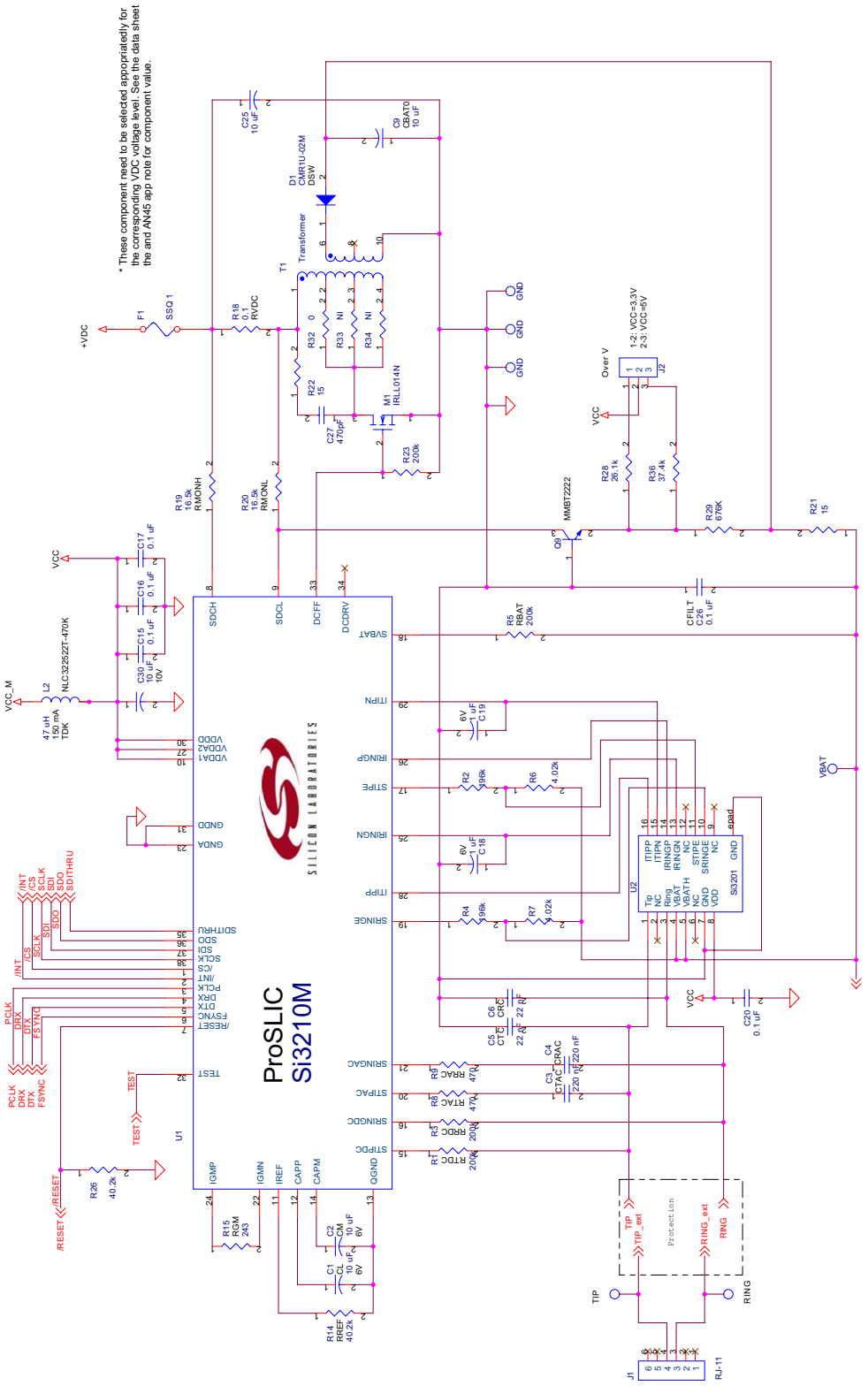


Figure 37. Si3210MCARD-EVB with Si3201 Evaluation Circuit (1 of 3)

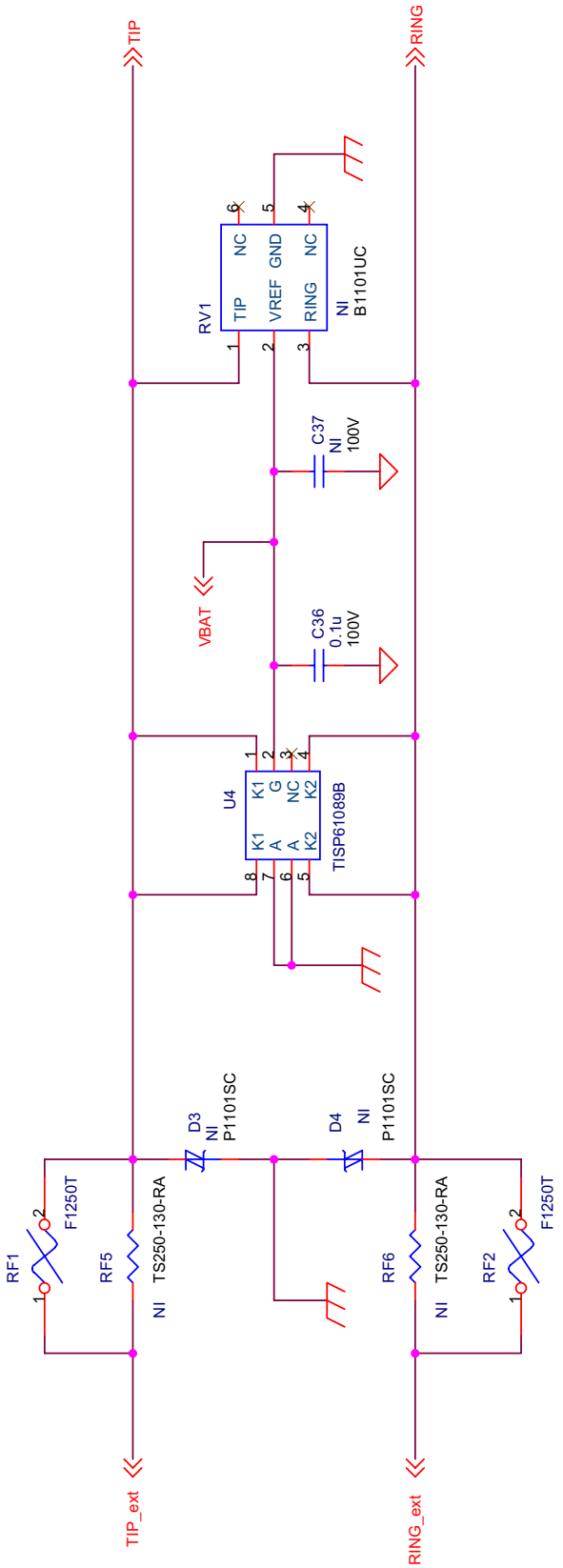


Figure 38. Si3210MCARD-EVB with Si3201 Evaluation Circuit (2 of 3)

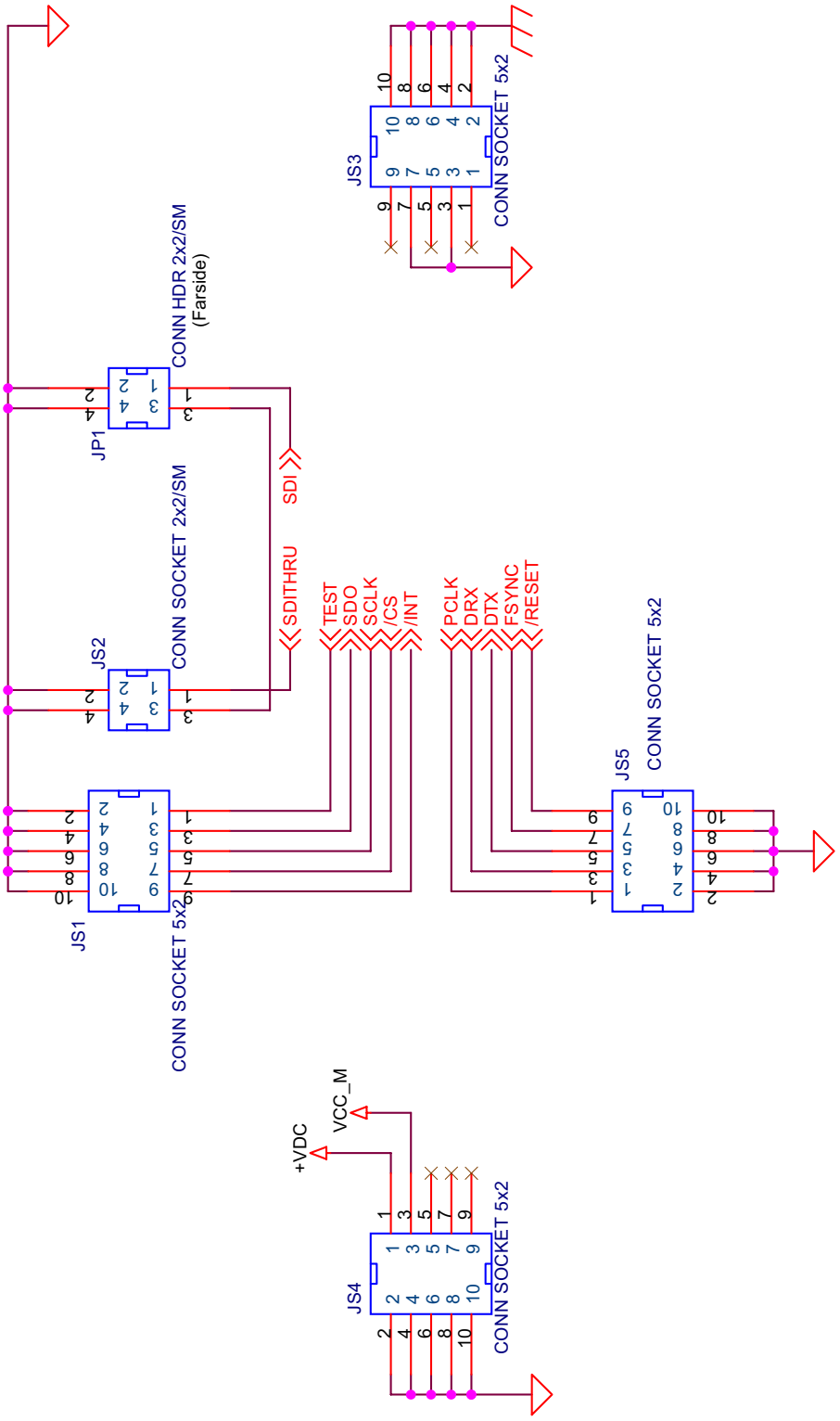


Figure 39. Si3210MCARD-EVB with Si3201 Evaluation Circuit (3 of 3)

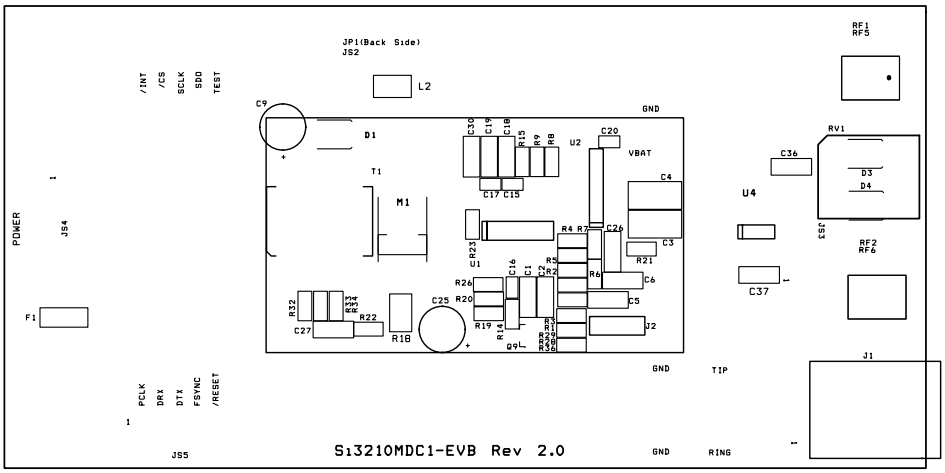


Figure 40. Si321xMDC-EVB with Si3201 Silkscreen

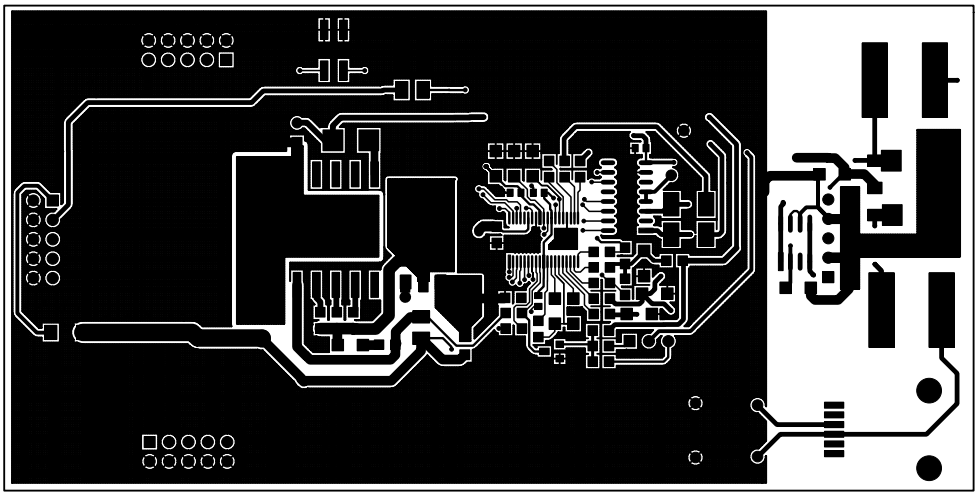


Figure 41. Si321xMDC-EVB with Si3201 Component Side

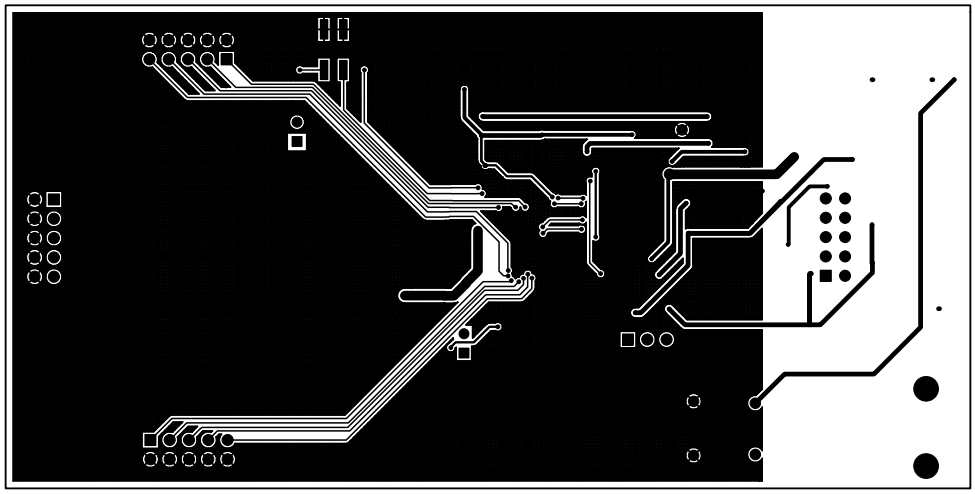


Figure 42. Si321xMDC-EVB with Si3201 Solder Side

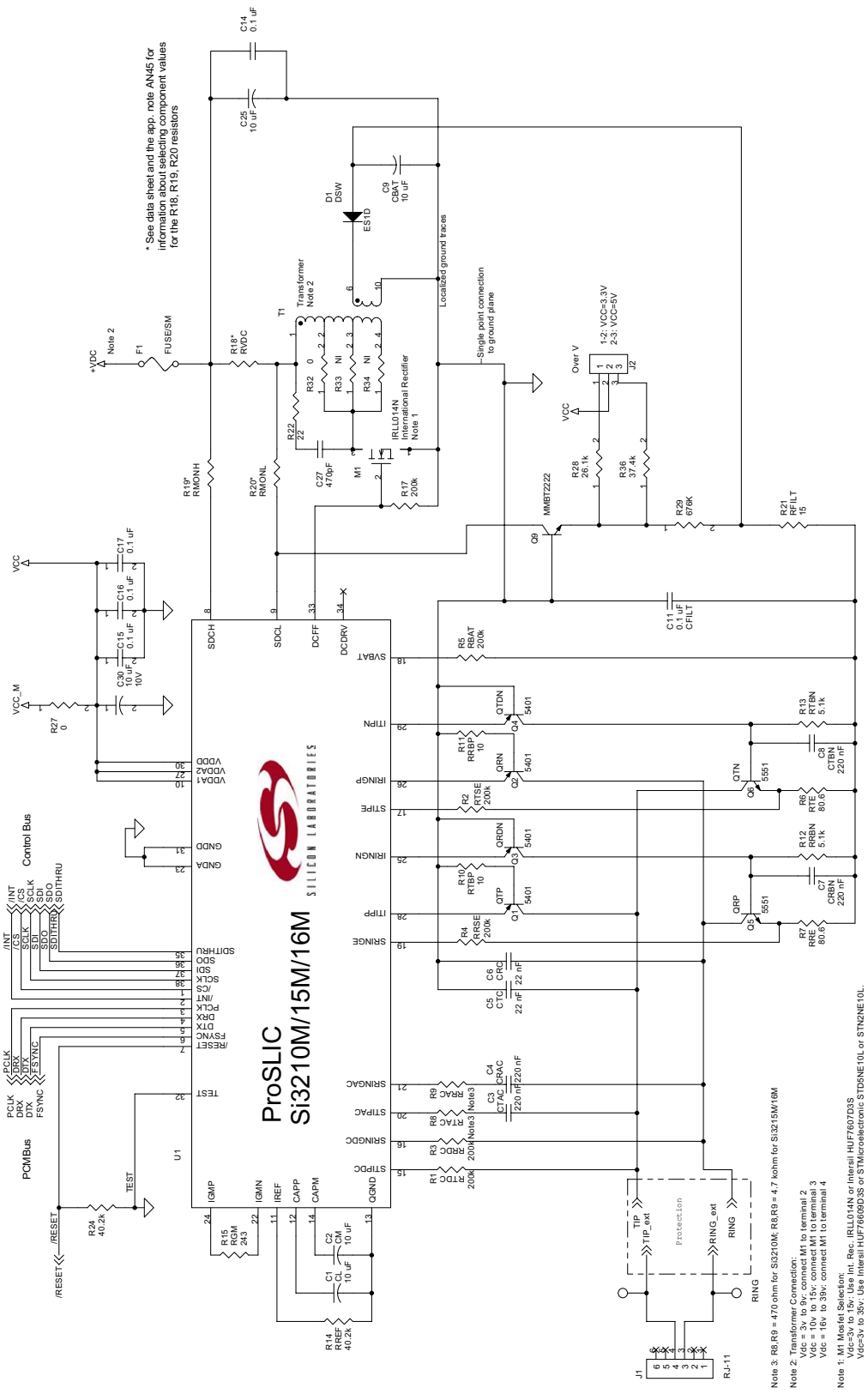


Figure 43. Si321xMDC-EVB with Discretes Evaluation Circuit (1 of 3)

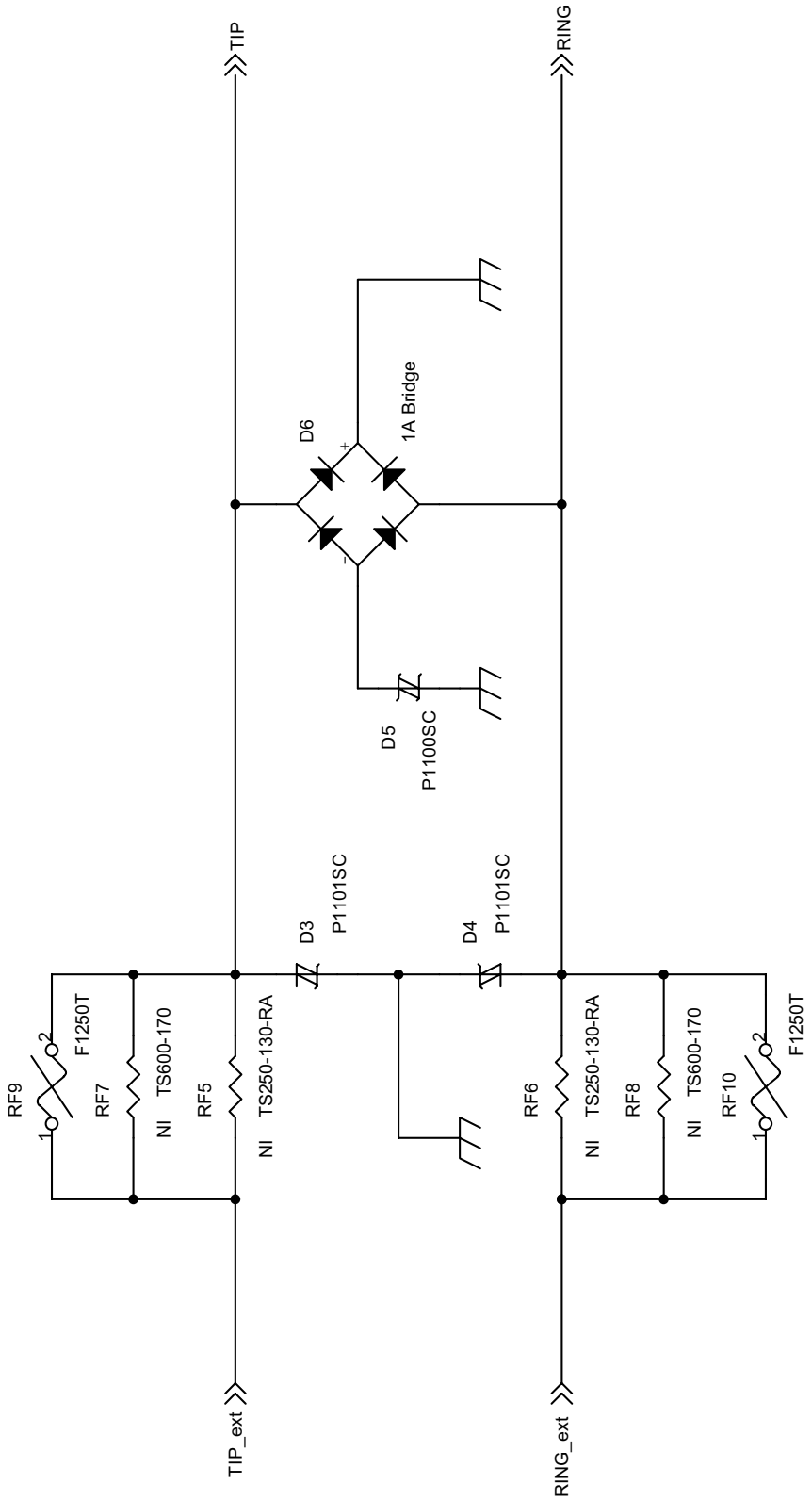


Figure 44. Si321xMDC-EVB with Discretes Evaluation Circuit (2 of 3)

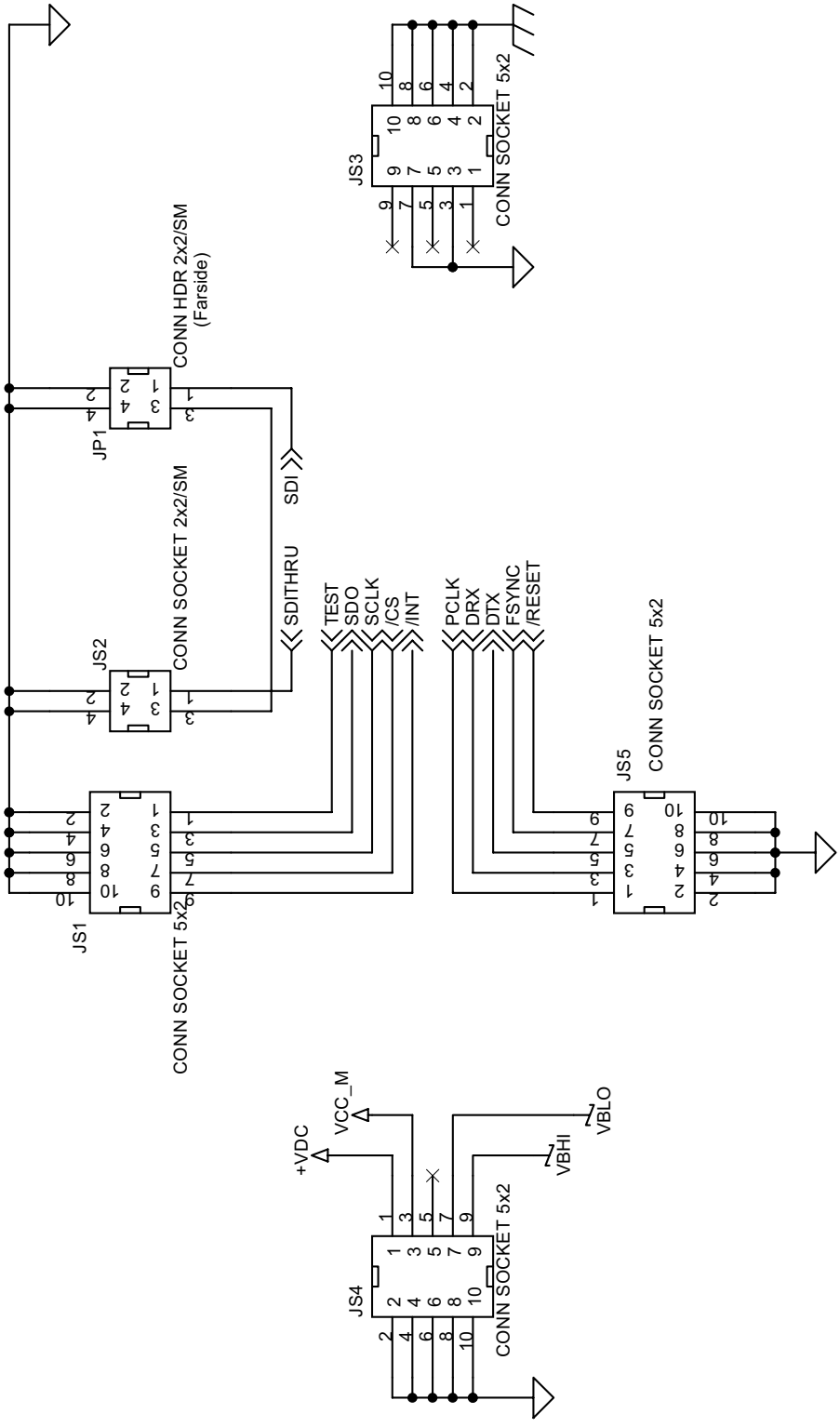


Figure 45. Si321xMDC-EVB with Discretes Evaluation Circuit (3 of 3)

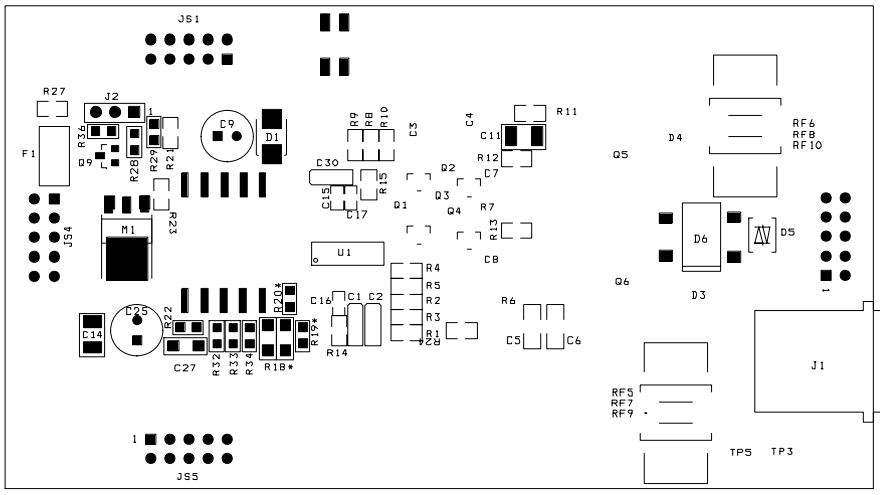


Figure 46. Si321xMDC-EVB with Discretes Silkscreen

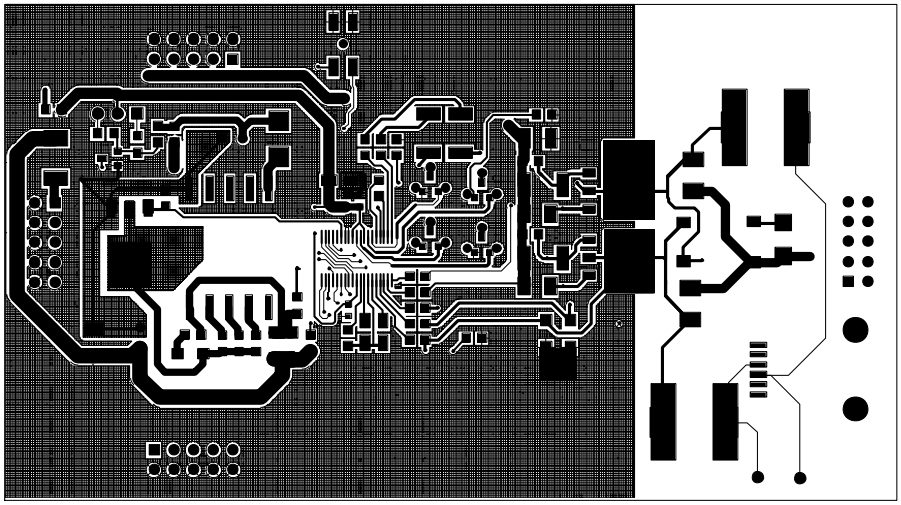


Figure 47. Si321xMDC-EVB with Discretes Component Side

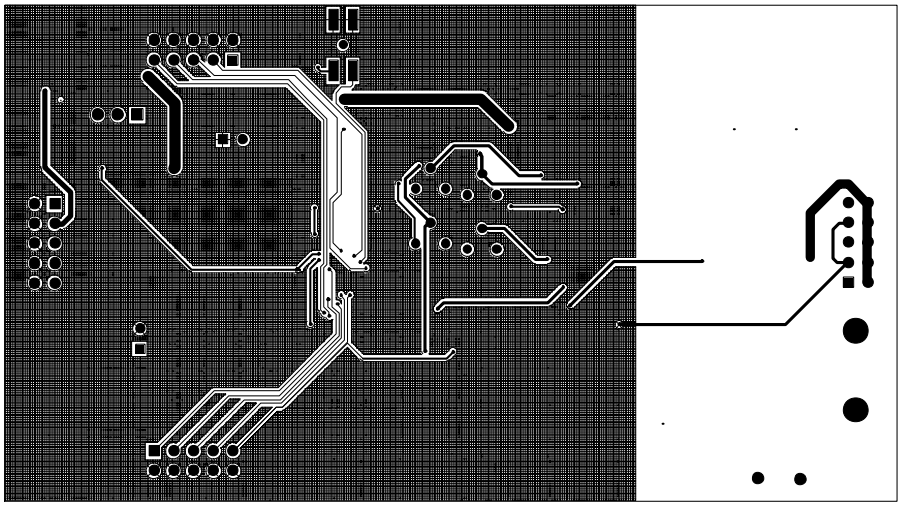


Figure 48. Si321xMDC-EVB with Discretes Solder Side

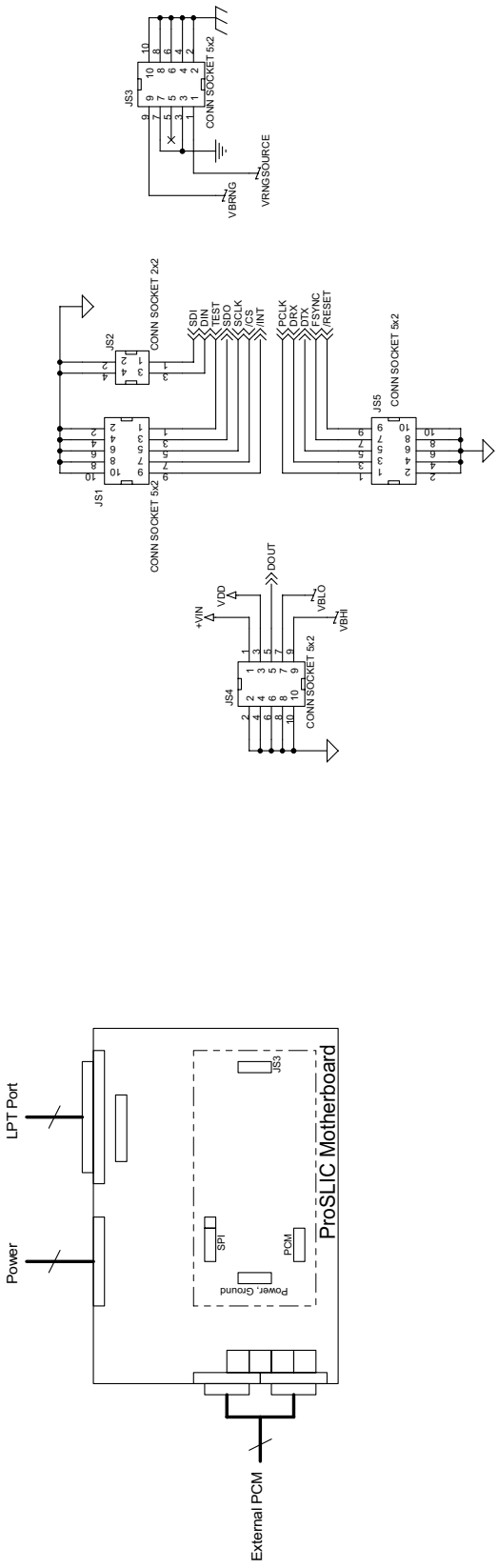


Figure 49. ProSLIC Motherboard (ProSLIC IF)

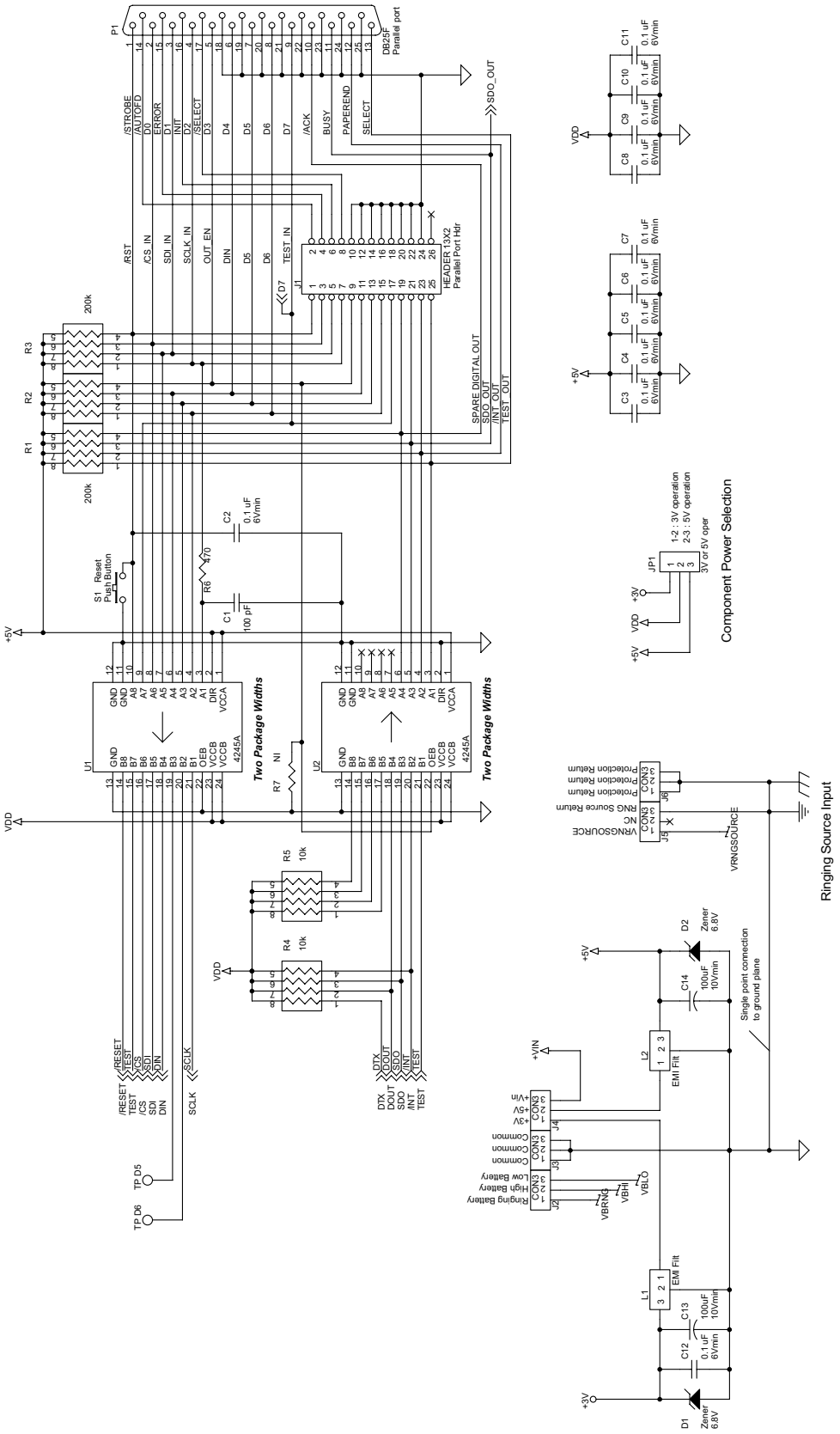


Figure 50. ProSLIC Motherboard (LPT to SPI)

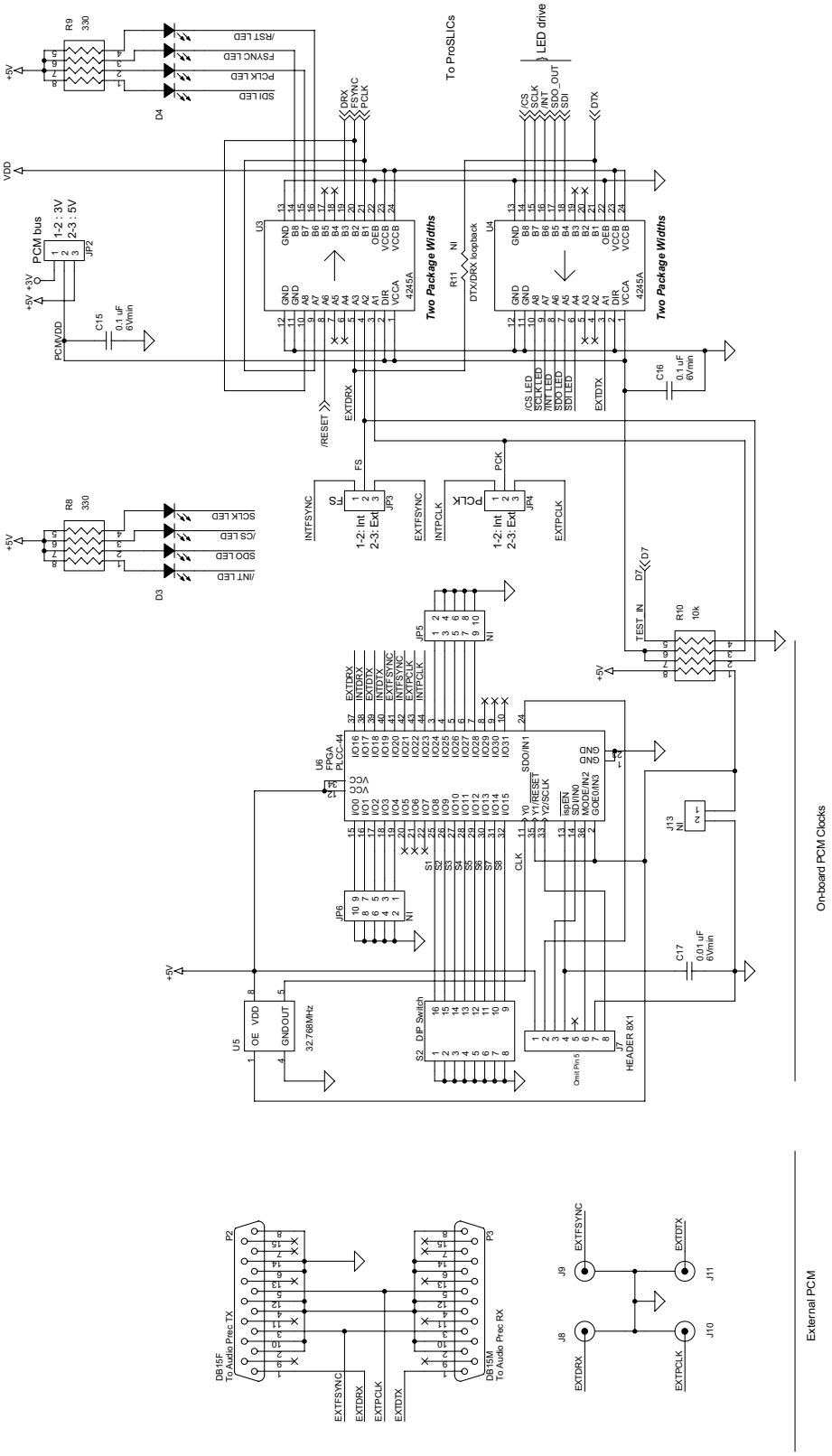


Figure 51. ProSLIC Motherboard (PCM)

3. Ordering Guide

Si3210	(M)	PP	I	X	–EVB
ProSLIC part Si3210 Si3215 Si3216	Inductor (No “M”)	PP - Parallel Port Motherboard	T = TSSOP	X = Discrete linefeed	
	Transformer (“M”)	DC - Daughter Card only	Q = QFN	1 = Si3201 linefeed	

DOCUMENT CHANGE LIST

Revision 0.9 to Revision 1.0

- Updated schematics
- Updated layouts

Revision 1.0 to Revision 1.1

- Added QFN schematics and layouts.

NOTES:

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