ADS-930

16-Bit, 500kHz Sampling A/D Converters

FEATURES

- 16-bit resolution
- 500kHz sampling rate
- Functionally complete
- Excellent dynamic performance
- 83dB SNR, –89dB THD
- No missing codes
- Small, 40-pin, TDIP package
- 3.5 Watts power dissipation
- On-board FIFO

PRODUCT OVERVIEW

The low-cost ADS-930 is a high-performance, 16-bit, 500kHz sampling A/D converter. This device accurately samples fullscale input signals up to Nyquist frequencies with no missing codes. The dynamic performance of the ADS-930 is optimized to achieve a THD of –89dB and an SNR of 83dB.

Packaged in a small, 40-pin, ceramic TDIP, the functionally complete ADS-930 contains a fast-settling sample-hold amplifier, a subranging (three-pass) A/D converter, an internal reference, an on-board FIFO, timing and control logic, three-state outputs and error-correction circuitry. Digital inputs/ outputs are TTL.

Requiring ±15V and +5V supplies, the ADS-930 typically dissipates 3.5 Watts. The unit is offered with a bipolar input range of ±5V or a unipolar input range of 0 to –10V. Models are available for use in either commercial (0 to +70°C) or HI-REL (–55 to +125°C) operating temperature ranges. Typical applications include radar, sonar, medical/graphic imaging, and FFT spectrum analysis.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+10V REF. OUT	40	$\overline{\text{BIT 1 (MSB)}}$
2	BIPOLAR	39	BIT 1 (MSB)
3	ANALOG INPUT	38	BIT 2
4	ANALOG GROUND	37	BIT 3
5	OFFSET ADJUST	36	BIT 4
6	GAIN ADJUST	35	BIT 5
7	+15V SUPPLY	34	BIT 6
8	$\overline{\text{COMP. BITS}}$	33	BIT 7
9	$\overline{\text{ENABLE}}$	32	BIT 8
10	FIFO READ	31	BIT 9
11	ANALOG GROUND	30	ANALOG GROUND
12	–15V SUPPLY	29	BIT 10
13	ANALOG GROUND	28	BIT 11
14	OVERFLOW	27	BIT 12
15	$\overline{\text{EOC}}$	26	BIT 13
16	+5V SUPPLY	25	BIT 14
17	START CONVERT	24	DIGITAL GROUND
18	DIGITAL GROUND	23	FIFO/$\overline{\text{DIR}}$
19	FSTAT1	22	BIT 15
20	FSTAT2	21	BIT 16 (LSB)

BLOCK DIAGRAM

POWER AND GROUNDING	
+5V SUPPLY	16
+15V SUPPLY	7
–15V SUPPLY	12
ANALOG GROUND	4, 11, 13, 30
DIGITAL GROUND	18, 24

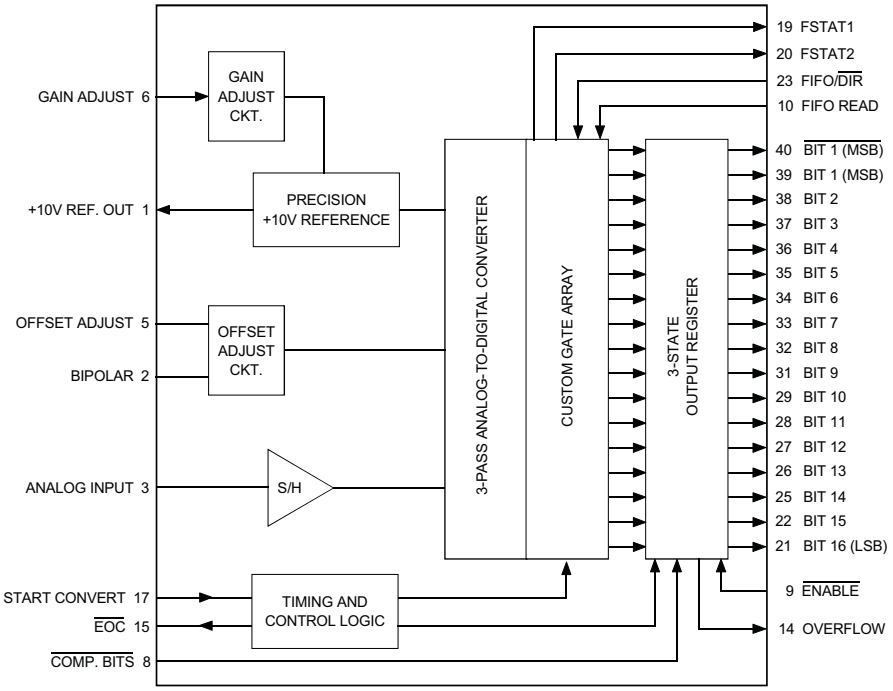


Figure 1. ADS-930 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 7)	0 to +16	Volts
–15V Supply (Pin 12)	0 to –16	Volts
+5V Supply (Pin 16)	0 to +6	Volts
Digital Inputs (Pin 8, 9, 10, 17, 23)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 3)		
Unipolar	–12.5 to +12.5	Volts
Bipolar	–7.5 to +12.5	Volts
Lead Temperature (10 seconds)	+300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS-930MC	0	—	+70	°C
ADS-930MM	–55	—	+125	°C
Thermal Impedance				
θjc	—	4	—	°C/Watt
θca	—	18	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	40-pin, metal-sealed, ceramic TDIP			
Weight	0.56ounces (16 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC}= ±15V +V_{DD} = +5V, 500kHz sampling rate, and a minimum 5 minute warmup ① unless otherwise specified.)

	+25°C			0 TO +70°C			–55 TO +125°C			
ANALOG INPUTS	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage Range										
Bipolar	—	±5	—	—	±5	—	—	±5	—	Volts
Unipolar	—	0 to –10	—	—	0 to –10	—	—	0 to –10	—	Volts
Input Resistance	1.4	1.5	1.7	1.4	1.5	1.7	1.4	1.5	1.7	kΩ
Input Capacitance	—	7	15	—	7	15	—	7	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0" ②	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	175	200	215	175	200	215	175	200	215	ns
STATIC PERFORMANCE										
Resolution	—	16	—	—	16	—	—	16	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±1.0	—	—	±1.5	—	—	±2.0	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	—	±0.75	—	—	±1.0	—	—	±1.5	—	LSB
Full Scale Absolute Accuracy	—	±0.05	±0.18	—	±0.2	±0.5	—	±0.5	±0.8	%FSR
Unipolar Zero Error (Tech Note 2)	—	±0.05	±0.085	—	±0.1	±0.2	—	±0.2	±0.3	%FSR
Bipolar Zero Error (Tech Note 2)	—	±0.05	±0.085	—	±0.15	±0.25	—	±0.25	±0.5	%FSR
Bipolar Offset Error (Tech Note 2)	—	±0.05	±0.15	—	±0.1	±0.25	—	±0.25	±0.5	%FSR
Gain Error (Tech Note 2)	—	±0.1	±0.15	—	±0.15	±0.35	—	±0.25	±0.65	%FSR
No Missing Codes (f_{in} = 10kHz)	16	—	—	16	—	—	16	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 100kHz	—	–91	—	—	–91	—	—	–87	—	dB
100kHz to 250kHz	—	–86	—	—	–86	—	—	–84	—	dB
Total Harmonic Distortion (–0.5dB)										
dc to 100kHz	—	–89	–81	—	–89	–81	—	–85	–76	dB
100kHz to 250kHz	—	–84	—	—	–84	—	—	–82	—	dB
Signal–to–Noise Ratio (w/o distortion, –0.5dB)										
dc to 100kHz	81	83	—	81	83	—	75	80	—	dB
100kHz to 250kHz	—	80	—	—	80	—	—	79	—	dB
Signal-to-Noise Ratio ④ (& distortion, –0.5dB)										
dc to 100kHz	78	81	—	77	81	—	72	78	—	dB
100kHz to 250kHz	—	78	—	—	78	—	—	76	—	dB
Two-tone Intermodulation Distortion (f_{in} = 100kHz, 240kHz, f_S = 500kHz, –0.5dB)	—	–82	—	—	–82	—	—	–81	—	dB
Noise	—	150	—	—	150	—	—	150	—	µVrms
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	2	—	—	2	—	—	2	—	MHz
Large Signal (–0.5dB input)	—	1.1	—	—	1.1	—	—	1.1	—	MHz
Feedthrough Rejection (f_{in} = 250kHz)	—	–96	—	—	–96	—	—	–96	—	dB
Slew Rate	—	±80	—	—	±80	—	—	±80	—	V/µs
Aperture Delay Time	—	±10	—	—	±10	—	—	±10	—	ns
Aperture Uncertainty	—	50	—	—	50	—	—	50	—	ps rms
S/H Acquisition Time (to ±0.003%FSR, 10V step)	—	680	720	—	680	720	—	680	720	ns
Overvoltage Recovery Time ⑤	—	600	1000	—	600	1000	—	600	1000	ns
A/D Conversion Rate	500	—	—	500	—	—	500	—	—	kHz

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG OUTPUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Internal Reference										
Voltage	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	Volts
Drift	—	±10	—	—	±10	—	—	±10	—	ppm/°C
External Current	—	—	1	—	—	1	—	—	1	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	–4	—	—	–4	—	—	–4	mA
Logic Loading "0"	—	—	+4	—	—	+4	—	—	+4	mA
Delay, Falling Edge of $\overline{\text{ENABLE}}$ to Output Data Valid	—	—	10	—	—	10	—	—	10	ns
Output Coding	Complementary Offset Binary; Complementary Two's Complement, Offset Binary, Two's Complement									
POWER REQUIREMENTS										
Power Supply Ranges										
+15V Supply	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	Volts
–15V Supply	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Currents										
+15V Supply	—	+110	+130	—	+110	+130	—	+110	+130	mA
–15V Supply	—	–100	–125	—	–100	–125	—	–100	–125	mA
+5V Supply	—	+80	+90	—	+80	+90	—	+80	+90	mA
Power Dissipation	—	3.5	4.25	—	3.5	4.25	—	3.5	4.25	Watts
Power Supply Rejection	—	—	±0.02	—	—	±0.02	—	—	±0.02	%FSR/%V

Footnotes:

① All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT) must be present during warmup periods. The device must be continuously converting during this time.

② When $\overline{\text{COMP. BITS}}$ (pin 8) is low, logic loading "0" will be –350µA.

③ A 200ns wide start convert pulse is used for all production testing. For applications requiring less than a 500kHz sampling rate, wider start convert pulses can be used.

④ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-930 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (4, 11, 13, 18, 24 and 30) directly to a large analog ground plane beneath the package.

   Bypass all power supplies and the +10V reference output to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible.

2. The ADS-930 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the adjustment circuitry shown in Figure 2. When using this circuitry, or any similar offset and gain calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain. Tie pins 5 and 6 to ANALOG GROUND (pin 4) if not using offset and gain adjust circuits.

3. Pin 8 ($\overline{\text{COMP. BITS}}$) is used to select the digital output coding format of the ADS-930. See Tables 3a and 3b. When this pin has a TTL logic "0" applied, it complements all of the ADS-930's digital outputs.

   When pin 8 has a logic "1" applied and the ADS-930 is operated within its unipolar (0 to –10V) input range, the output coding is straight binary. Applying a logic "0" to pin 8 under these conditions changes the output coding to complementary binary.

   When pin 8 has a logic "1" applied and the ADS-930 is operated within its bipolar (±5V) input range, the output coding is offset binary. Applying a logic "0" to pin 8 under these conditions changes the coding to complementary offset binary. Using the $\overline{\text{MSB}}$ output (pin 40) instead of the MSB output (pin 39) under these conditions changes the respective output codings to two's complement and complementary two's complement.

   Pin 8 is TTL-compatible and can be directly driven with digital logic in applications requiring dynamic control over its function. There is an internal pull-up resistor on pin 8 allowing it to be either connected to +5V or left open when a logic "1" is required.

4. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 9) to a logic "0" (low). To disable, connect pin 9 to a logic "1" (high).

5. Applying a start convert pulse while a conversion is in progress ($\overline{\text{EOC}}$ = logic "1") will initiate a new and probably inaccurate conversion cycle.

6. Do not enable/disable or complement the output bits or read from the FIFO during the conversion process (from the falling edge of START CONVERT to the falling edge of $\overline{\text{EOC}}$).

INTERNAL FIFO OPERATION

The ADS-930 contains an internal, user-initiated, 18-bit, 16- word FIFO memory. Each word in the FIFO contains the 16 data bits as well as the $\overline{\text{MSB}}$ and OVERFLOW bits. Pins 23 (FIFO/$\overline{\text{DIR}}$) and 10 (FIFO READ) control the FIFO's operation. The FIFO's status can be monitored by reading pins 19 (FSTAT1) and 20 (FSTAT2).

When pin 23 (FIFO/$\overline{\text{DIR}}$) has a logic "1" applied, the FIFO is inserted into the digital data path. When pin 23 has a logic "0" applied, the FIFO is transparent, and the output data goes directly to the output three-state register (whose operation is controlled by pin 9 ($\overline{\text{ENABLE}}$)). Read and write commands to the FIFO are ignored when the ADS-930 is operated in the "direct" mode. It takes a maximum of 20ns to switch the FIFO in or out of the ADS-930's operation.

FIFO WRITE and READ Modes

Once the FIFO has been enabled (pin 23 high), digital data is automatically written to it, regardless of the status of FIFO READ (pin 10). Assuming the FIFO is initially empty, it will accept data (18-bit words) from the next 16 consecutive A/D conversions. As a precaution, pin 10 (which controls the FIFO's READ function) should not be low when data is first written to an empty FIFO.

When the FIFO is initially empty, digital data from the first conversion (the "oldest" data) appears at the output of the FIFO immediately after the first conversion has been completed and remains there until the FIFO is read.

If the output three-state register has been enabled (logic "0" applied to pin 9), data from the first conversion will appear at the output of the ADS-930. Attempting to write a 17th word to a full FIFO will result in that data, and any subsequent conversion data, being lost.

Once the FIFO is full (indicated by FSTAT1 and FSTAT2 both = "1"), it can be read by dropping the FIFO READ line (pin 10) to a logic "0" and then applying a series of 15 rising edges to the read line. Since the first data word is already present at the FIFO output, the first read command (the first rising edge applied to FIFO READ) will bring data from the second conversion to the output. Each subsequent read command/rising edge brings the next word to the output lines.

If a read command is issued after the FIFO has been emptied, the last word (the 16th conversion) will remain present at the outputs.

FIFO Reset Feature

At any time, the FIFO can be reset to an empty state by putting the ADS-930 into its "direct" mode (logic "0" applied to pin 23, FIFO/$\overline{\text{DIR}}$) and also applying a logic "0" to the FIFO READ line (pin 10). The empty status of the FIFO will be indicated by FSTAT1 going to a "0" and FSTAT2 going to a "1". The status outputs will change 40ns after the control signals have been applied.

FIFO Status, FSTAT1 and FSTAT2

The status of the data in the FIFO can be monitored by reading the two status pins, FSTAT1 (pin 19) and FSTAT2 (pin 20).

CONTENTS	FSTAT1	FSTAT2
Empty (0 words)	0	1
<half full (≤7 words)	0	0
half-full or more (≥8 words)	1	0
Full (16 words)	1	1

DELAY	PIN	TRANSITION	MIN.	TYP.	MAX.	UNITS
Direct mode to FIFO enabled	23	0 → 1	–	10	20	ns
FIFO enabled to direct mode	23	1 → 0	–	10	20	ns
FIFO READ to output data valid	10	0 → 1	–	–	40	ns
FIFO READ to status update when changing from <half full (1 word) to empty	10	1 → 0	–	–	28	ns
FIFO READ to status update when changing from ≥half full (8 words) to <half full (7 words)	10	0 → 1	–	–	110	ns
FIFO READ to status update when changing from full (16 words) to ≥half full (15 words)	10	0 → 1	–	–	190	ns
Falling edge of $\overline{\text{EOC}}$ to status update when writing first word into empty FIFO	15	1 → 0	–	–	190	ns
Falling edge of $\overline{\text{EOC}}$ to status update when changing FIFO from <half full (7 words) to ≥half full (8 words)	15	1 → 0	–	–	110	ns
Falling edge of $\overline{\text{EOC}}$ to status update when filling FIFO with 16th word	15	1 → 0	–	–	28	ns

Table 1. FIFO Delays

CALIBRATION PROCEDURE (Refer to Figure 2 and Tables 3a and 3b)

Connect the converter per Table 2 for the appropriate input voltage range. Any offset/gain calibration procedures should not be implemented until the device is fully warmed up. To avoid interaction, adjust offset before gain. The ranges of adjustment for the circuits in Figure 2 are guaranteed to compensate for the ADS-930's initial accuracy errors and may not be able to compensate for additional system errors.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This is accomplished by connecting LED's to the digital outputs and performing adjustments until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-930, offset adjusting is normally accomplished when the analog input is 0 minus ½ LSB (–76µV). See Table 3b for the proper bipolar and unipolar output coding.

Gain adjusting is accomplished when the analog input is at nominal full scale minus 1½ LSB's (–9.999771V for unipolar and +4.999771V for bipolar).

Note: Connect pin 5 to ANALOG GROUND (pin 4) for operation without zero/offset adjustment. Connect pin 6 to pin 4 for operation without gain adjustment.

INPUT RANGE	INPUT PIN	TIE TOGETHER
0 to –10V	Pin 3	Pins 2 and 4
±5V	Pin 3	Pins 1 and 2

Table 2. Input Connections

OUTPUT FORMAT	PIN 8 LOGIC LEVEL
Straight Binary	1
Complementary Binary	0
Complementary Offset Binary	0
Offset Binary	1
Complementary Two's Complement (Using $\overline{MSB}$, pin 40)	0
Two's Complement (Using $\overline{MSB}$, pin 40)	1

Table 3a. Setting Output Coding Selection (Pin 8)

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 17) so that the converter is continuously converting.
2. For unipolar or bipolar zero/offset adjust, apply –76.3µV to the ANALOG INPUT (pin 3).
3. For a bipolar input - adjust the offset potentiometer until the code flickers between 1000 0000 0000 0000 and 0111 1111 1111 1111 with pin 8 tied high (offset binary) or between 0111 1111 1111 1111 and 1000 0000 0000 0000 with pin 8 tied low (complementary offset binary).

   For a unipolar input - adjust the offset potentiometer until all output bits are 0's and the LSB flickers between 0 and 1 with pin 8 tied high (straight binary) or until all output bits are 1's and the LSB flickers between 0 and 1 with pin 8 tied low (complementary binary).
4. Two's complement coding requires using $\overline{BIT\ 1\ (MSB)}$ (pin 40). With pin 8 tied high, adjust the trimpot until the output code flickers between all 0's and all 1's.

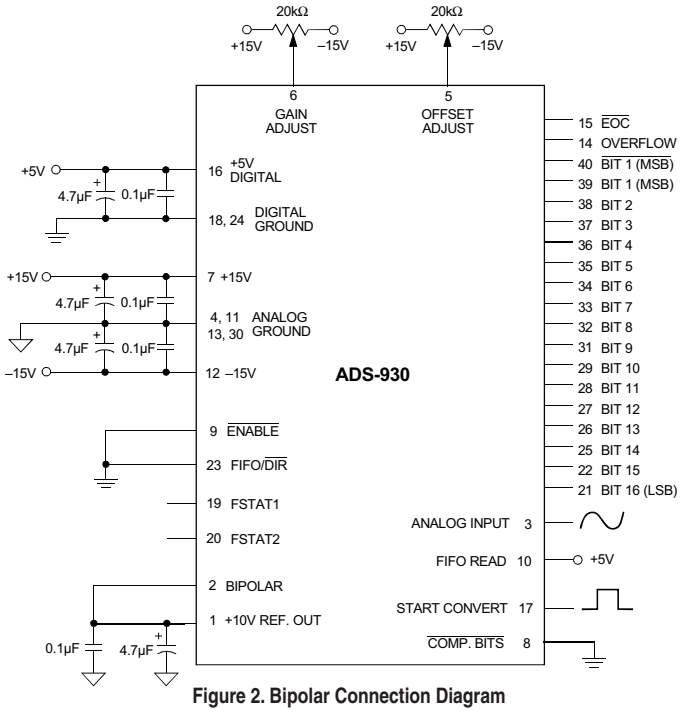


Figure 2. Bipolar Connection Diagram

		STRAIGHT BIN.		COMP. BINARY					
UNIPOLAR SCALE	INPUT RANGE 0 to –10V	OUTPUT CODING MSB	LSB	MSB	LSB	$\overline{MSB}$	LSB	$\overline{MSB}$	LSB	INPUT RANGE ±5V	BIPOLAR SCALE
–FS +1 LSB	–9.999847	1111 1111 1111 1111		0000 0000 0000 0000		0111 1111 1111 1111		1000 0000 0000 0000		+4.999847	+FS –1 LSB
–FS +1 1/2 LSB	–9.999771	LSB "1" to "0"		LSB "0" to "1"		LSB "1" to "0"		LSB "0" to "1"		+4.999771	+FS –1 1/2 LSB
–7/8 FS	–8.750000	1110 0000 0000 0000		0001 1111 1111 1111		0110 0000 0000 0000		1001 1111 1111 1111		+3.750000	+3/4 FS
–3/4 FS	–7.500000	1100 0000 0000 0000		0011 1111 1111 1111		0100 0000 0000 0000		1011 1111 1111 1111		+2.500000	+1/2 FS
–1/2FS	–5.000000	1000 0000 0000 0000		0111 1111 1111 1111		0000 0000 0000 0000		1111 1111 1111 1111		0.000000	0
–1/2FS –1/2LSB	–4.999924	0111 1111 1111 1111		1000 0000 0000 0000		1111 1111 1111 1111		0000 0000 0000 0000		–0.000076	–1/2 LSB
–1/4FS	–2.500000	0100 0000 0000 0000		1011 1111 1111 1111		1100 0000 0000 0000		0011 1111 1111 1111		–2.500000	–1/2 FS
–1/8FS	–1.250000	0010 0000 0000 0000		1101 1111 1111 1111		1010 0000 0000 0000		0101 1111 1111 1111		–3.750000	–3/4 FS
–1 LSB	–0.000153	0000 0000 0000 0001		1111 1111 1111 1110		1000 0000 0000 0001		0111 1111 1111 1110		–4.999847	–FS +1 LSB
–1/2LSB	–0.000076	LSB "0" to "1"		LSB "1" to "0"		LSB "0" to "1"		LSB "1" to "0"		–4.999924	–FS + 1/2 LSB
0	0.000000	0000 0000 0000 0000		1111 1111 1111 1111		1000 0000 0000 0000		01111111 1111 1111		–5.000000	–FS
		COMP. OFF. BIN.		OFFSET BINARY		COMP. TWO'S COMP.		TWO'S COMP.			

Table 3b. Output Coding

Gain Adjust Procedure

1. Apply +4.999771V to the ANALOG INPUT (pin 3) for bipolar gain adjust or apply –9.999771V to pin 3 for unipolar gain adjust.
2. For a unipolar input - adjust the gain potentiometer until all output bits are 1's and the LSB flickers between a 1 and 0 with pin 8 tied high (straight binary) or until all output bits are 0's and the LSB flickers between a 1 and 0 with pin 8 tied low (complementary binary).

   For a bipolar input - adjust the gain potentiometer until all output bits are 1's and the LSB flickers between a 1 and 0 with pin 8 tied low (complementary offset binary) or until all output bits are 0's and the LSB flickers between a 1 and 0 ith pin 8 tied high (offset binary).
3. Two's complement coding requires using pin 40. With pin 8 tied high, adjust the gain trimpot until the output code flickers equally between 1000 0000 0000 0000 and 1000 0000 0000 0001.

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to +125°C. All room-temperature (TA = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package. Electrically insulating, thermally conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

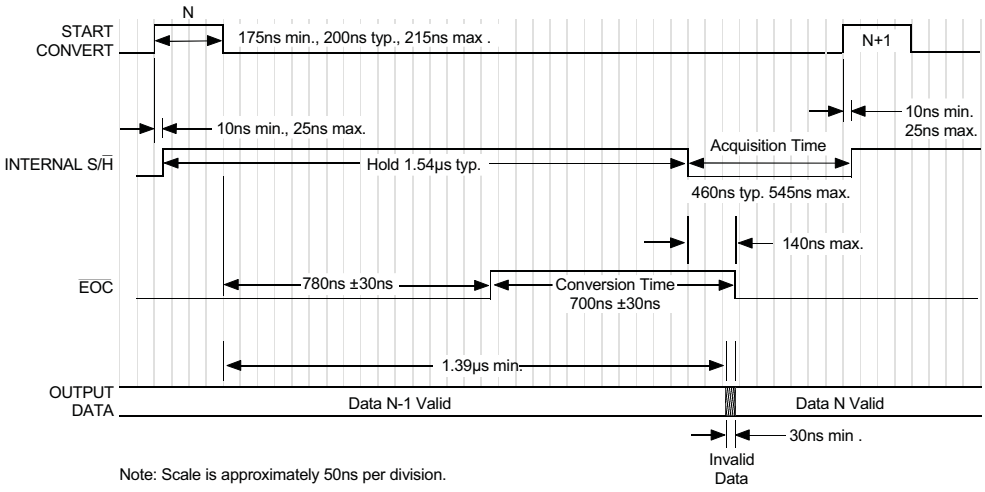


Figure 3. ADS-930 Timing Diagram

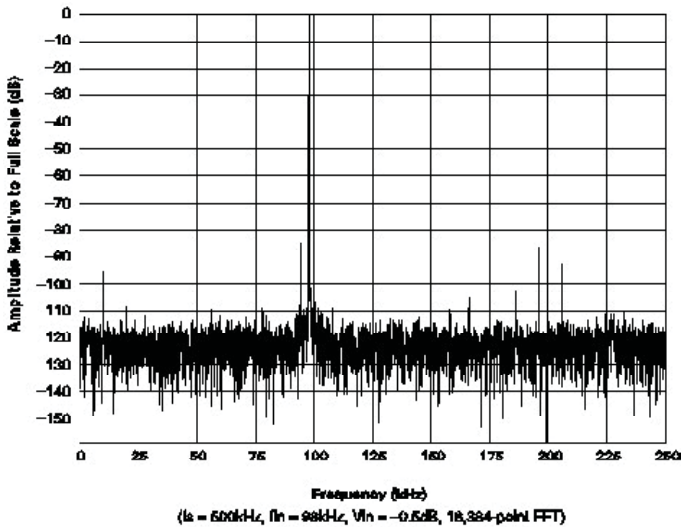


Figure 4. FFT Analysis of ADS-930

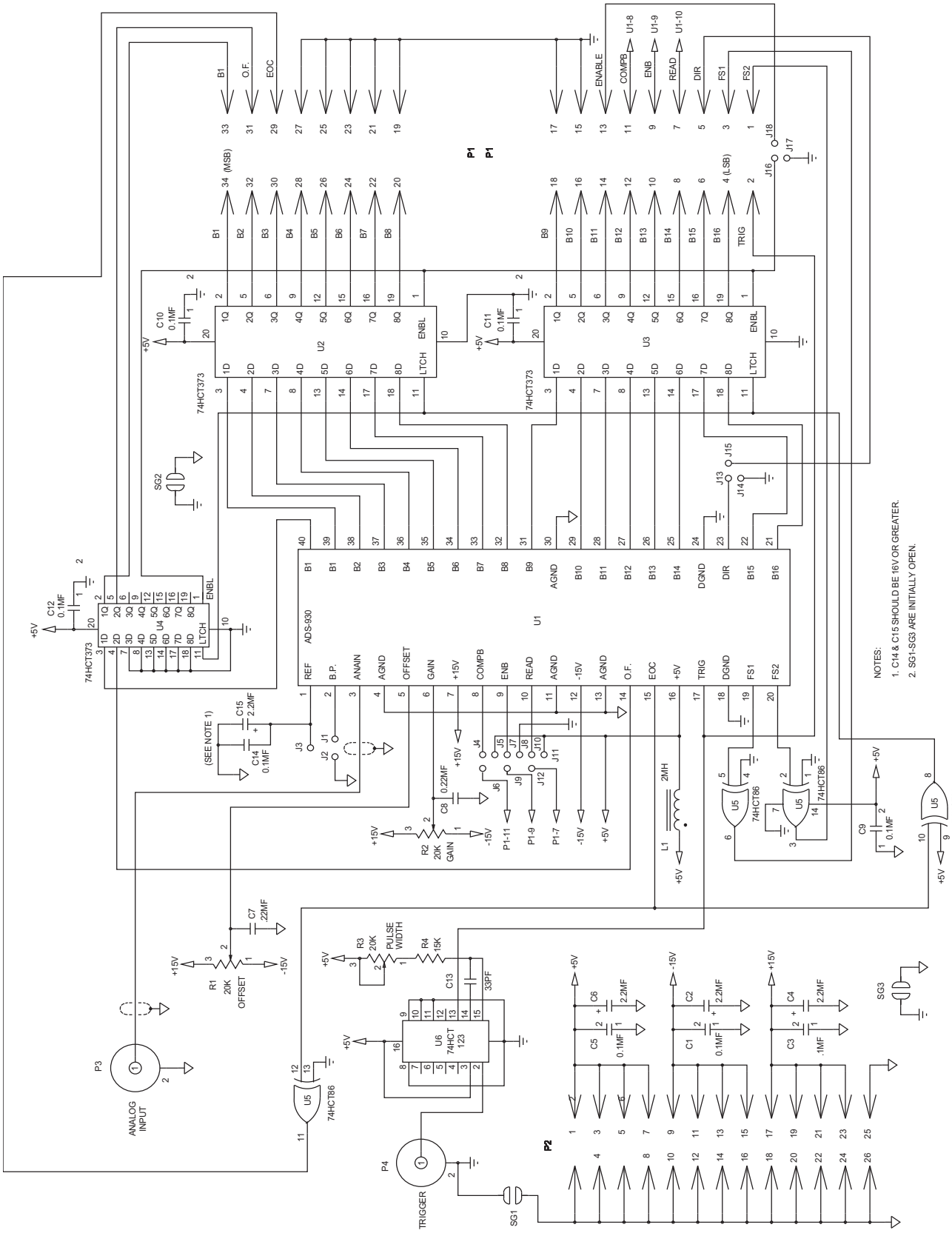
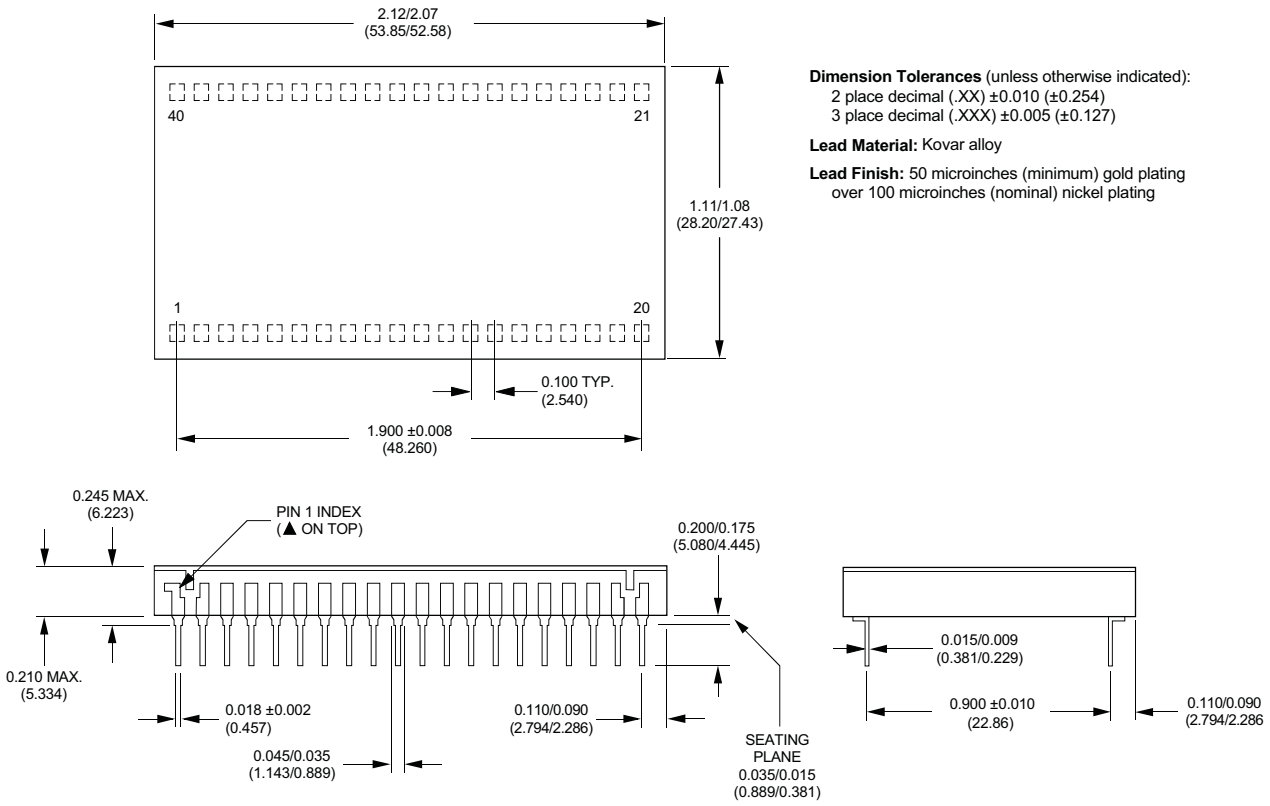


Figure 5. ADS-930 Evaluation Board Schematic

MECHANICAL DIMENSIONS - INCHES (mm)



Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	ANALOG INPUT	ACCESSORIES	
ADS-930MC	0 to +70°C	0 to –10V, ±5V	ADS-EVAL3	Evaluation Board (without ADS-930)
ADS-930MM	–55 to +125°C	0 to –10V, ±5V	HS-40	Heat Sink for all ADS-930 models

Receptacles for pc board mounting can be ordered through AMP, Inc., part # 3-331272-8 (Component Lead Socket), 40 required.
For MIL-STD-883 product, or surface mount packaging, contact DATEL.

11 Cabot Boulevard, Mansfield, MA 02048-1151 USA
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www.datel.com • e-mail: help@datel.com