IWE8

Interworking Element for 8 E1/T1 Lines

PXB4219E/PXB4220E/PXB4221E

Version 3.4

Datacom

Infineon technologies

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PXB4219E/PXB4220E/PXB4221E
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Page	Subjects (major changes since last revision)

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device name (IWE8), device number (PXB4219E/PXB4220E/PXB4221E), device version (Version 3.4),

and in the *body* of your e-mail:
document type (Preliminary Data Sheet), issue date (2001-07) and document revision number (DS1).

1 Overview

The Interworking Element for
8 E1/T1 Lines PXB4219E/PXB4220E/PXB4221E (IWE8) is a member of Infineon's ATM chip set. Together with framing and line interface components (e.g. Infineon's QuadFALC PEB 22554) the IWE8 serves as gateway between Asynchronous Transfer Mode (ATM) networks and timeslot based PDH networks.

Each of the 8 E1 or T1 input and output ports can be configured independently to operate in one of two basic modes:

ATM Mode

ATM mode ports operate as an ATM User Network Interface (UNI) at 2.048 Mbit/s (E1) or 1.544 Mbit/s (T1).

The device supports mapping of ATM cells in T1/E1 frames according to ITU-T G.804, "ATM Cell Mapping into Plesiochronous Digital Hierarchy (PDH)" [26] and ATM Forum, "ATM on Fractional E1/T1" [9].

It implements all Transmission Convergence (TC) sublayer functions of the Physical Layer (PHY) defined in ITU-T I.432, "B-ISDN User-network Interface - Physical layer Specification" [32]

AAL Mode

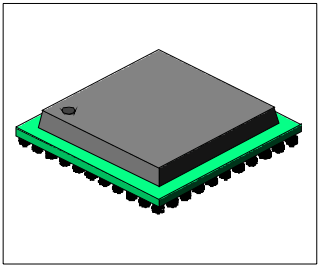
AAL mode ports operate as an ATM Circuit Emulation Service Interworking Function (CES-IWF) between Constant Bit Rate (CBR) equipment and an ATM network as described by the ATM Forum, "Circuit Emulation Services Version 2.0" [10]. (only PXB 4220/4221)

The CBR circuits are converted into ATM constant bit-rate virtual channels using the ATM Adaptation Layer type 1 (AAL1) as defined in I.363.1, "B-ISDN ATM Adaptation Layer Specification, Types 1 and 2" [31] or without any ATM Adaptation Layer overhead, which will be referred as AAL type 0 throughout the rest of this document.

The IWE8 provides the segmentation and reassembly function.

Both the "Unstructured DS1/E1 Service" and the "Structured DS1/E1 N x 64 kbit/s Basic Service" as described in the "Circuit Emulation Services Version 2.0" by the ATM Forum in [10] are supported. For simplicity reasons the shorthand notation "Unstructured CES" will be used to identify the "Unstructured DS1/E1 Service" while the "Structured DS1/E1 N x 64 kbit/s Service" will be referred to as "Structured CES" throughout the rest of this document.

1.1 Features



- Full duplex ATM Packetizer/Depacketizer for 8 E1/T1 highways
- Configurable to T1 or E1 mode via external pin
- 8 T1/E1 ports configurable independently to ATM or AAL Mode
- ATM Mode (PXB 4219/4220/4221):
  - ATM cell mapping into PDH according to ITU-T G.804 [26]
  - B-ISDN User-Network interface - Physical Layer according to ITU-T I.432 [32]
  - B-ISDN User-Network interface - Physical Layer operation at 1544 KBit/s and 2048 KBit/s according to ITU-T I.432.3 [34]
- AAL Mode (PXB 4220/4221):
  - AAL1 according to ITU-T I.363.1 [31] or transparent without any adaptation layer overhead (AAL0)
  - T1/E1 unstructured service according to ATM Forum af-vtoa-0078.000 [10] section 3
  - Structured T1/E1 N x 64 kbit/s service according to [10] section 2 with M channels of N x 64 kbit/s (M,N = 1to 24 for T1) (M,N = 1to 32 for E1)
  - Channel Associated Signalling (CAS) support according to [10]
  - Echo Canceller Mode
  - Partially filled cells with programmable filling thresholds
  - Selectable Sequence Count Algorithm:
    - Robust/Fast according to ITU-T I.363.1 [30]
    - According to ETSI (prl-ETS 300353 annex D) [17]
    - Fast: Saves 6 ms during reassembly for 1 x 64 kbit/s connection
  - AAL0 option: 48 Bytes user payload per ATM Cell, without AAL overhead
  - Reassembly buffer can compensate up to +/- 4 ms Cell Delay Variation (CDV)
  - Statistics counters per channel for lost/misinserted/errored cells etc.

Type	Package
PXB4219E/PXB4220E/PXB4221E	P-BGA-256

  - Internal clock recovery circuit using Synchronous Residual Time Stamp (SRTS, for fully filled cells only) or Adaptive Clock Method (ACM) for unstructured CES ports. For SRTS a patent fee needs to be paid. Optionally, it's possible to order the PXB 4221 device, which comes without SRTS clock recovery.
  - Trunk freezing and conditioning according to Bellcore TR-NWT-000170 [14]
- IMA interface:
  - Programmable threshold between read and write pointer of Mapping Buffer
  - Output Signal for buffer threshold crossing
  - Output Signal for discarded cell
  - Output pins for port number indication
- 8 generic framer interfaces with integrated transmit clock selector supporting
  - Synchronous Mode (SYM) for E1
  - Generic Interface Mode (GIM)
  - FALC Mode (FAM): Glue-less interface for Infineon's Framer and Line Interface Components (FALC)
  - Echo Canceller Mode (EC): ATM cells are duplicated internally and transmitted via two framer ports
- UTOPIA industry standard interface:
  - Level 2 in slave mode; 8 data, 5 address lines
  - Level 1 in master/slave mode
  - UTOPIA clock up to 38.88 MHz
- 16-bit generic microprocessor interface for control and configuration of the chip runs either in Intel 386EX or Motorola compatible mode
- External synchronous Flow-Through SSRAM 1 x 64k x 33 bit or 1 x 64k x 32 bit required
- Build-in data path loops for test
- Cell insertion/extraction via microprocessor interface
- 3.3 Volt power supply with 5 Volt tolerant inputs
- Typical power dissipation 1 Watt
- P-BGA-256 package
- Temperature range from -40° to +85°C

1.2 Logic Symbol

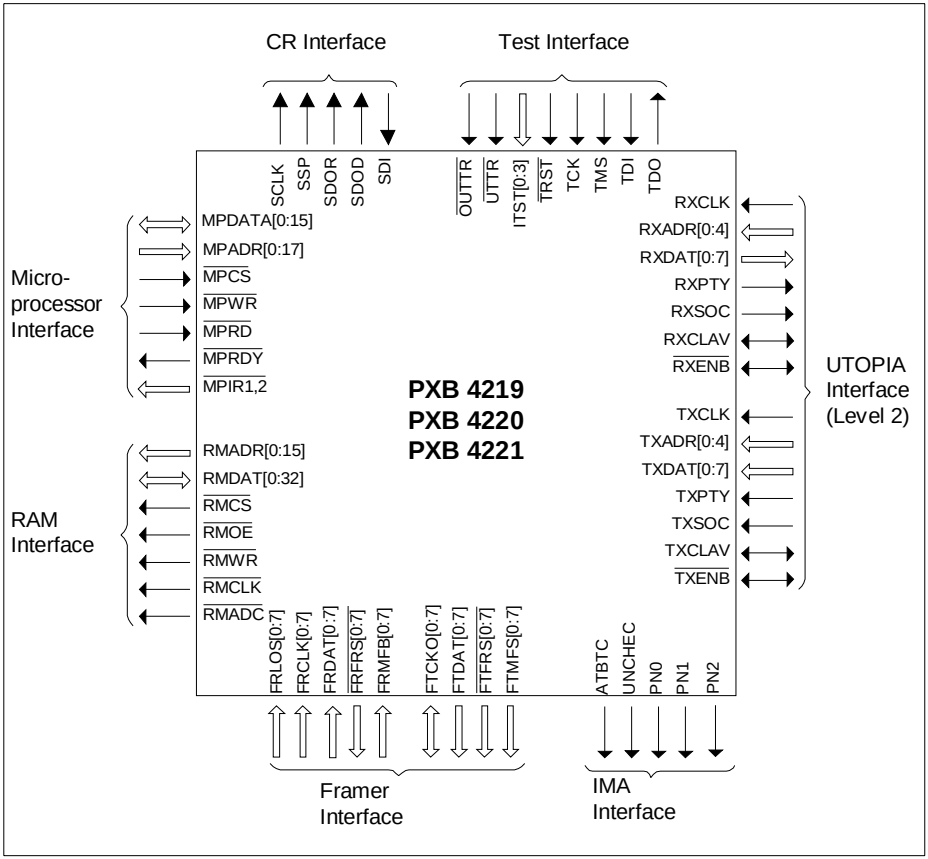


Figure 1 Logic Symbol

1.3 Typical Applications

Figure 2 illustrates three typical application areas which utilize the IWE8 chip in Line Interface Cards (LICs) or Network Interface Controllers (NICs).

Application 1 utilizes the IWE8 as an internetworking device for communication between a narrowband Time-Slot based network and an ATM network.

Application 2 utilizes the IWE8 chip to enable the use of an existing T1/E1 access line for connection to an ATM network.

In application 3, the IWE8 chip enables terminals using a Leased Line or Time-Slot based service to convert from T1/E1 network connection to ATM network connection without noticeable changes to the subscriber.

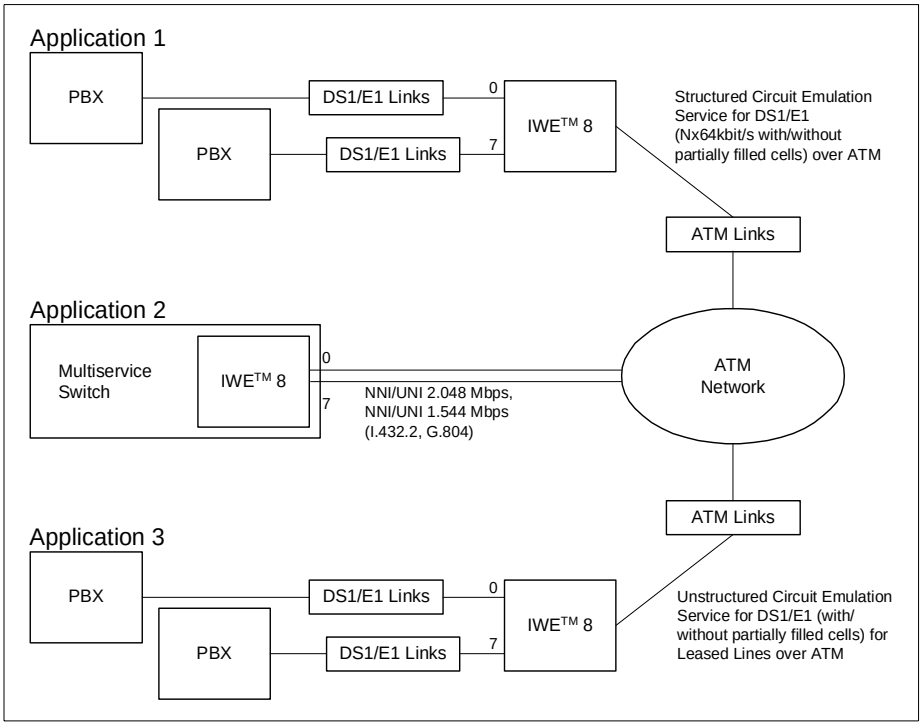


Figure 2 Typical IWE8 Applications

The PXB 4220 IWE8 chip is designed to handle up to eight T1/E1 ports. It transfers data between the Pulse Code Modulation (PCM)-highway and an UTOPIA ATM Interface.

1.3.1 Line Card

Figure 3 shows an example Line Interface Card (LIC) utilizing the IWE8 in a switch environment. Two Infineon Quad Framer and Line Interface Component (QuadFALC, PEB 22554) chips are connected at the PCM ports. An ATM Layer circuit is connected at the UTOPIA Interface port and could be implemented using Infineon PXB 4350 ATM Layer Processor (ALP) chip.

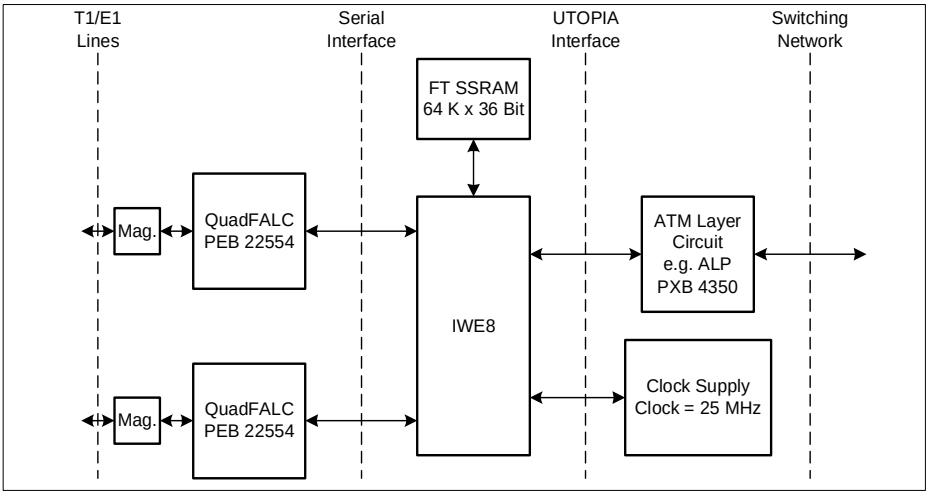


Figure 3 Line Card for 8 T1/E1 Channels

External synchronous SRAM is always required for proper IWE8 operation. The IWE8 requires only one main operating clock of 12 times the data rate of one port. An emergency clock of 32.768 MHz is optional. The Framer and Utopia interface clocks can be completely asynchronous with respect to the main clock. A microprocessor controls and operates the IWE8 via a generic 16-bit interface.

1.3.2 Echo Canceller

In communication links reflections resulting in an electrical echo are due to hybrid splits or imperfect terminations in subscriber loops. Acoustical echoes may occur due to poor isolation of microphone and speaker of some telephone systems. These electrical and acoustical echoes disturb the quality of the transmission. To ensure high quality, pure data transmission the ITU-T suggests in the recommendation G.131 [22] the use of echo cancellers. Echo cancellation is extremely desirable for data links with total round trip transmission times of more than 50 ms.

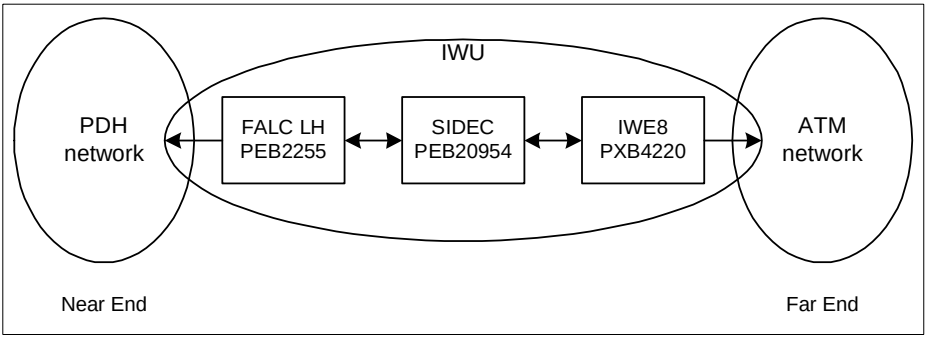


Figure 4 Echo Canceller Application

The echo cancelling function itself is performed in STM. In the application above the IWE8 is used to translate voice ATM channels into STM channels and vice versa. Infineon's Smart Integrated Digital Echo Canceller (SIDEC, PEB 20954) is used for cancellation of the echo that is generated by reflection on the near end side and heard by the far end speaker. The SIDEC can cancel end echo paths (SDH or PDH network on near end side) up to 128 ms. For details see [21]

1.4 Differences Between PXB4220 And PXB4219

The IWE8 type PXB4219 does only support the ATM mode used for ITU-T G.804 compliant ATM cell mapping into the plesiochronous digital hierarchy (PDH) at line rates of 1544 kbit/s and 2048 kbit/s. The AAL mode is not available.

1.5 Differences Between PXB4220 And PXB4221

The IWE8 type PXB4220 uses an internal clock recovery mechanism (SRTS) which is patented by Bellcore. SRTS is supported for fully filled cells only.

Related Patents are:

- Bellcore patent No. 5,260,978
  (Synchronous Residual Time Stamp for Timing Recovery in a broadband network)
- Bellcore patent No. 4,839,306
  (Method and apparatus for multiplexing circuit and packet traffic)

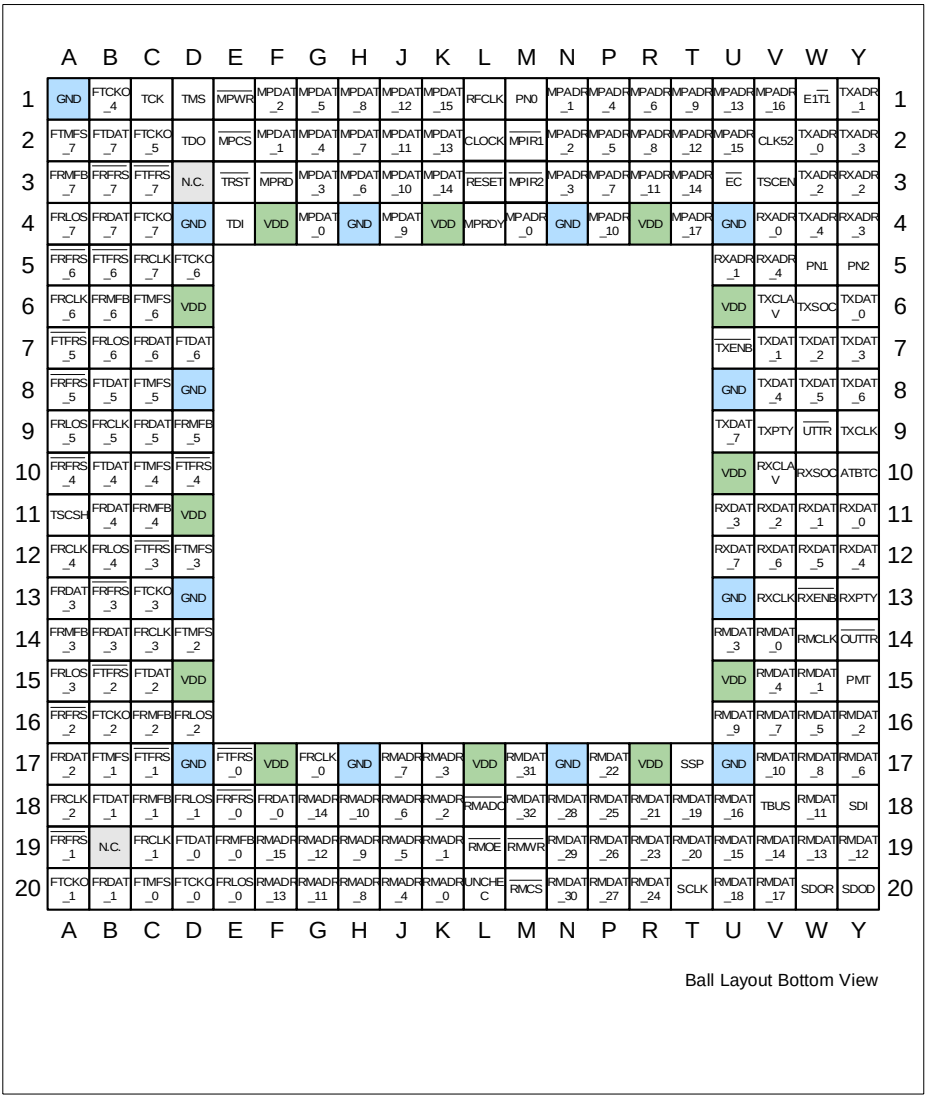
Infineon Technologies is not allowed to collect SRTS license fees on the IWE8 on behalf of Bellcore. Contacts for license issues are given in **Chapter 13**.

Every IWE8 customer must get in contact with Bellcore legal department by himself to clarify whether his application needs to license the SRTS functionality.

For customers who do not want to use the built-in SRTS mechanism, Infineon provides a special version of the IWE8. The name of this device is PXB4221 and covers the same functionality (pin and register compatible) like the PXB4220. SRTS is physically and permanently disabled, so that no patent fees have to be paid.

2 Pin Descriptions

2.1 Pin Diagram



Ball Layout Bottom View

Figure 5 Pin Configuration

2.2 Pin Definitions and Functions

Output Pull Up and Pull Down Type Definitions

PUx	Pull Up of strength x (x = A, B) is implemented. The corresponding current is specified in **Chapter 9.4**
PDx	Pull Down of strength x (x = A) is implemented. The corresponding current is specified in **Chapter 9.4**
Tri	Tri-stated when inactive

2.2.1 Generic Framer Interface

Table 1 Generic Framer Interface (73 pins)

Pin No.	Symbol	Input (I) Output (O)	Function
C5, A6, B9, A12, C14, A18, C19, G17	FRCLK[7:0]	I	**Framer Receive Clock** Receive clock for the framer interface
B4, C7, C9, B11, B14, A17, B20, F18	FRDAT[7:0]	I PDA	**Framer Receive Data** Receive data input of the framer interface
A3, B6, D9, C11, A14, C16, C18, E19	FRMFB[7:0]	I PUA	**Framer Receive Multiframe Begin** Indication that a new multi-/superframe is available on the receive side of the framer interface
B3, A5, A8, A10, B13, A16, A19, E18	$\overline{\text{FRFRS}}$[7:0]	O PUA	**Framer Receive Frame Synchronization Pulse** Indication that a new frame is available on the receive side of the framer interface
A4,B7, A9, B12, A15, D16, D18, E20	FRLOS[7:0]	I PDA	**Framer Receive Loss of Signalling** Indication that CAS bits are invalid, IWE8 will start CAS freezing

Table 1 Generic Framer Interface (73 pins) (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
C4, D5, C2, B1, C13, B16, A20, D20	FTCKO[7:0]	O/I PDA	**Framer Transmit Clock** Transmit clock for the framer interface. • Recovered clock output from the ICRC • Framer receive clock output from pin FRCLKN • Output of the clock derived from RFCLK • Input for an external clock recovery device
B2, D7, B8, B10, A13, C15, B18, D19	FTDAT[7:0]	O PUA	**Framer Transmit Data** Transmit data output of the framer interface
A2, C6, C8, C10, D12, D14, B17, C20	FTMFS[7:0]	O PUA	**Framer Transmit Multiframe Synchronization** Indication that a new multi-/superframe is available on the transmit side of the framer interface
C3, B5, A7, D10, C12, B15, C17, E17	$\overline{\text{FTFRS}}$[7:0]	O PUA	**Framer Transmit Frame Synchronization Pulse** Indication that a new frame is available on the transmit side of the framer interface
L1	RFCLK	I	**Reference Clock** SYM and EC mode: Central framer interface clock for all framer ports FAM and GIM: Optional SRTS/ACM reference or emergency clock for the framer receive interface in case of clock failure

2.2.2 UTOPIA Interface

Table 2 UTOPIA Interface (36 pins)

Pin No.	Symbol	Input (I) Output (O)	Function
U12, V12, W12, Y12, U11, V11, W11, Y11	RXDAT[7:0]	O PUA	**UTOPIA Receive Data Bus** Byte-wide data driven from PHY to ATM layer. RxData[7] is the MSB.
Y13	RXPTY	O PUA	**UTOPIA Receive Odd Parity Bit** Odd parity for RXDAT[0:7] driven by the PHY layer.
W10	RXSOC	O PDA	**UTOPIA Receive Start-of-Cell** Active high signal asserted by the PHY layer when RXDAT[0:7] contains the first valid byte of a cell.
V10	RXCLAV	**Slave**: O **Master**: I PDA	**UTOPIA Receive Cell Available** **Slave**: RXCLAV is an active high signal asserted by the PHY layer to indicate that it has data available for transfer to the ATM layer. **Master**: RXCLAV is an active high signal asserted by the ATM layer to indicate that it has data available for transfer to the PHY layer.
V13	RXCLK	I	**UTOPIA Receive Clock** Transfer/synchronization clock from the ATM layer to the PHY layer for synchronizing transfers on RXDAT[0:7].
W13	$\overline{\text{RXENB}}$	**Slave**: I **Master**: O PUA	**UTOPIA Receive Enable** **Slave:** Active low signal asserted by the ATM layer to indicate that RXDAT[0:7] and RXSOC will be sampled at the end of the next cycle. **Master:** Active low signal asserted by the PHY layer to indicate that RXDAT[0:7] and RXSOC will be sampled at the end of the next cycle.

Table 2 UTOPIA Interface (36 pins) (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
V5, Y4, Y3, U5, V4	RXADR[4:0]	I PUA	**UTOPIA Receive Address Bus** Five bit wide true data driven from the ATM to MPHY layer to select the appropriate MPHY device. RXADR[4] is the MSB.
U9, Y8, W8, V8, Y7, W7, V7, Y6	TXDAT[7:0]	I PUA	**UTOPIA Transmit Data Bus** Byte-wide true data driven from ATM to PHY layer. TXDAT[7] is the MSB.
V9	TXPTY	I PUA	**UTOPIA Transmit Odd Parity Bit** TXPTY is the odd parity bit over TXDAT[0:7] driven by the ATM layer.
W6	TXSOC	I PDA	**UTOPIA Transmit Start-of-Cell** Active high signal asserted by the ATM layer when TXDAT[0:7] contains the first valid byte of the cell.
V6	TXCLAV	**Slave**: O **Master**: I PDA	**UTOPIA Transmit Cell Available** **Slave:** TXCLAV is an active high signal asserted by the PHY layer to indicate it can accept data. **Master:** TXCLAV is an active high signal asserted by the ATM layer to indicate it can accept data.
Y9	TXCLK	I	**UTOPIA Transmit Clock** Data transfer/synchronization clock provided by the ATM layer to the PHY layer for synchronizing transfers on TXDAT[0:7].

Table 2 UTOPIA Interface (36 pins) (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
U7	$\overline{\text{TXENB}}$	**Slave**: I **Master**: O PUA	**UTOPIA Transmit Enable** **Slave**: Active low signal asserted by the ATM layer during cycles when TXDAT[0:7] contains valid cell data. **Master**: Active low signal asserted by the PHY layer during cycles when TXDAT[0:7] contains valid cell data.
W4, Y2, W3, Y1, W2	TXADR[4:0]	I PUA	**UTOPIA Transmit Address Bus** Five bit wide true data driven from the ATM to MPHY layer to poll and select the appropriate MPHY device. TXADR4 is the MSB.

2.2.3 IMA Interface

Table 3 IMA Interface

Pin No.	Symbol	Input (I) Output (O)	Function
Y10	ATBTC	O Tri	**ATM Transmit Buffer Threshold Crossing** Indicates if the difference between the write and read pointer of the mapping buffer became smaller than a SW selectable threshold
L20	UNCHEC	O Tri	**Uncorrectable HEC Error** Indicates if a cell has been discarded due to an uncorrectable HEC error
Y5, W5, M1	PN[2:0]	O Tri	**Port Number** Indicates the port number where the cell causing ATBT or UNCHEC being asserted came from

2.2.4 Clock Recovery Interface

Table 4 Clock Recovery Interface

Pin No.	Symbol	Input (I) Output (O)	Function
Y18	SDI	I	**Serial Data Input** Clock recovery frame input.
Y20	SDOD	O Tri	**Serial Data Output Data** Clock recovery frame output
W20	SDOR	O Tri	**Serial Data Output Reset** Clock recovery reset frame output
T17	SSP	O Tri	**Serial Synchronization Pulse** Frame synchronization pulse output
T20	SCLK	O Tri	**Serial Clock** Clock output of the clock recovery interface. Runs at the same frequency than the CLOCK input

2.2.5 Microprocessor Interface

Table 5 Microprocessor Interface

Pin No.	Symbol	Input (I) Output (O)	Function
K1, K3, K2, J1, J2, J3, J4, H1, H2, H3, G1, G2, G3, F1, F2, G4	MPDAT[15:0]	I/O PUA	**Microprocessor Data Bus** This bidirectional three-state bus provides the general-purpose data path between the IWE8 and an external master. The bus uses little endian word order. MPDAT15 is the MSB.
T4, V1, U2, T3, U1, T2, R3, P4, T1, R2, P3, R1, P2, P1, N3, N2, N1, M4	MPADR[17:0]	I	**Microprocessor Address Bus** Provides the address of the current bus cycle. Addresses are 16-bit aligned. MPADR17 is the MSB of the bus
E2	$\overline{\text{MPCS}}$	I	**Microprocessor Chip Select** This signal is driven by the bus master to indicate a read or write access.

Table 5 Microprocessor Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
E1	$\overline{\text{MPWR}}$/ MPR$\overline{\text{W}}$	I	**Microprocessor Write Enable (Intel Bus Mode)** This signal is driven by the bus master to indicate a write data transfer **Read/Write Enable (Motorola Bus Mode)** This three-state signal is driven by the bus master to indicate the direction of the bus's data transfer
F3	$\overline{\text{MPRD}}$/ $\overline{\text{MPTS}}$	I	**Microprocessor Read Enable (Intel Bus Mode)** This signal is driven by the bus master to indicate a read data transfer **Microprocessor Transfer Start (Motorola Bus Mode)** This signal is asserted by the bus master to indicate the start of a bus cycle that transfers data to or from the device
L4	MPRDY $\overline{\text{MPTA}}$	O Tri	**Microprocessor Ready (Intel Bus Mode)** This three-state output indicates that the device has accepted date from the master (write) or has driven the data bus with valid data (read) **Microprocessor Transfer Acknowledge (Motorola Bus Mode)** This three-state output indicates that the device has accepted date from the master (write) or has driven the data bus with valid data (read)
M2	$\overline{\text{MPIR1}}$	O PUB	**Microprocessor Interrupt Request 1** Main interrupt pin indicating a special event in the IWE8.
M3	$\overline{\text{MPIR2}}$	O PUB	**Microprocessor Interrupt Request 2** This signal is generated by timer set 2 to indicate that a counter expired

2.2.6 External RAM Interface

Table 6 External RAM Interface

Pin No.	Symbol	Input (I) Output (O)	Function
F19, G18, F20, G19, G20, H18, H19, H20, J17, J18, J19, J20, K17, K18, K19, K20	RMADR[15:0]	O Tri	**RAM Address Bus** This bus provides the address of the current bus cycle. RMADR15 is the MSB.
M18, M17, N20, N19, N18, P20, P19, P18, R20, R19, P17, R18, T19, T18, U20, V20, U18, U19, V19, W19, Y19, W18, V17, U16, W17, V16, Y17, W16, V15, U14, Y16, W15, V14	RMDAT[32:0]	I/O PUB	**RAM Data Bus** This bidirectional three-state bus provides the data path between the IWE8 and the external memory. RMDAT32 is parity bit, RMDAT31 is the MSB.
M20	$\overline{\text{RMCS}}$	O Tri	**RAM Chip Select** This signal enables read or write accesses to the external memory
L19	$\overline{\text{RMOE}}$	O Tri	**RAM Output Enable** This signal enables the outputs of the external memory
M19	$\overline{\text{RMWR}}$	O Tri	**RAM Write Enable** This output is asserted when a write access to the external memory

Table 6 External RAM Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
L18	$\overline{\text{RMADC}}$	O Tri	**RAM Address Control** This output is asserted to indicate a valid address on RMADR[15:0]
W14	RMCLK	O Tri	**RAM Clock** Clock output for the external RAM. It runs at the same frequency as CLOCK input

2.2.7 Test Interface

Table 7 Test Interface

Pin No.	Symbol	Input (I) Output (O)	Function
D2	TDO	O Tri	**Boundary Scan Test Data Output**
E4	TDI	I PUA	**Boundary Scan Test Data Input**
C1	TCK	I PUA	**Boundary Scan Test Clock**
D1	TMS	I PUA	**Boundary Scan Test Mode Select** 0 = normal operation 1 = Enable boundary scan test mode
E3	$\overline{\text{TRST}}$	I PDA	**Boundary Scan Test Reset**
V3	TSCEN	I PDA	**Internal Test Pins** TSCEN and TSCSH must be low for proper operation
A11	TSCSH		
Y15	PMT	PDA	**Internal Test Pins** 00 = Intel mode 01 = prohibited 10 = prohibited 11 = Motorola Mode
V18	TBUS		

Table 7 Test Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
W9	$\overline{\text{UTTR}}$	I PUA	**Utopia TRI-STATE** 0 = tristate all Utopia outputs 1 = normal operation
Y14	$\overline{\text{OUTTR}}$	I	**Output TRI-STATE** 0 = tristate all outputs and disable all pull-up and pull-down resistors 1 = normal operation

2.2.8 Miscellaneous

Table 8 Miscellaneous

Pin No.	Symbol	Input (I) Output (O)	Function
W1	E1/$\overline{\text{T1}}$	I PUA	**E1 or T1 Mode Select** 0 = T1 mode 1 = E1 mode
U3	$\overline{\text{EC}}$	I PUA	**Echo Canceller Mode Select** 0 = echo canceller mode 1 = standard mode
L2	CLOCK	I	**Master Clock** Used to clock the core of the device
L3	$\overline{\text{RESET}}$	I PDA	**Master Hardware Reset** Asynchronous reset of all flip-flops
V2	CLK52	I	**51.84 MHz SRTS Reference Clock** external reference clock for SRTS. If SRTS mode is not used, it can be connected to V_{SS}

2.2.9 Power Supply

Table 9 Power Supply

Pin No.	Symbol	Input (I) Output (O)	Function
D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15	VDD		**Power Supply Voltage**
A1, D4, D8, D13, D17, H4, H17, N4, N17, U4, U8, U13,U17	GND		**Ground**

2.2.10 Not Connected Pins

Table 10 Not Connected Pins

Pin No.	Symbol	Input (I) Output (O)	Function
B19, D3	N.C.		**Not Connected**

3 Functional Description

All functional parts of the device are implemented in hardware. Configuration of the functional blocks has to be done by software via the micro controller interface.

The IWE8 provides two independent data paths for upstream, towards the ATM network, and downstream, from the ATM network, direction. For dedicated functional tests loopbacks between both are available.

Each of the 8 ports connected to the data path works independent from the others. It can be switched to ATM or AAL mode and provides access to the E1/T1 Framer at different framer interface protocols.

3.1 Operating Modes

3.1.1 ATM Mode

A port that is configured to ATM mode offers ITU-T G.804 [26] compliant ATM cell mapping into PDH frames at E1 or T1 datarates. ATM mode can be enabled via “p_atm” in register “pcfN”.

3.1.2 AAL Mode

A port that is configured to AAL mode offers ATM Forum [10] compliant circuit emulation services via AAL1 as defined in ITU-T I.361.1 [31]. A port N can be configured to AAL mode via “p_atm” in register “pcfN”.

Some features of the AAL mode are controlled by the internal registers “acfg”, “caal”, “bp32”, “bp10” and “cfil”. The features controlled by these registers are common to all AAL ports.

Some features of the AAL mode can be controlled per port, by programming the port configuration registers “pcfN”.

Some features of the AAL mode can be controlled per channel, by programming the channel specific “AAL Reference Slot” in the internal configuration RAM’s (RAM1 for receive ports, RAM2, RAM3 and RAM4 for transmit ports).

3.1.2.1 Unstructured CES Mode

A 2.048 Mbit/s (E1) or 1.544 Mbit/s (T1) bitstream is packed into ATM cells without any framing. No alignment between octets in E1 or T1 frames and octets in the ATM cells is done.

For this Unstructured T1/E1 Circuit Emulation Service (CES) the ATM adaptation layer type 1(AAL1) with Unstructured Data Transfer (UDT) as defined in ITU-T I.363.1[31] is used. The use of partially filled cells is possible.

For clock recovery the IWE8 supports the Synchronous Residual Time Stamp (SRTS) method and Adaptive Clock Method (ACM).

- SRTS is possible on channels with completely filled cells
- ACM can be used on both, channels with partially and completely filled cells

A port is programmed to unstructured CES via “p_ces” in the Port Configuration Register “pcfN”.

Per port a Segmentation Buffer with a maximum size of 16 cells and a Reassembly Buffer with a maximum size of 256 cells is implemented in external RAM.

3.1.2.2 Structured CES Mode

A port is programmed for the Structured T1/E1 Nx64 kbit/s Basic Service (Structured CES) via the port configuration register “pcfN” (“p_ces” = 0).

The structured circuit emulation service is intended to carry N of the 24 (T1) or 32 (E1) timeslots across the ATM network.

An emulated Nx64 kbit/s circuit will be referred to as a channel throughout this document. It is possible that several channels share the same physical interface port.

In structured CES mode neither SRTS nor ACM clock recovery is possible.

3.2 Functional Block Diagram

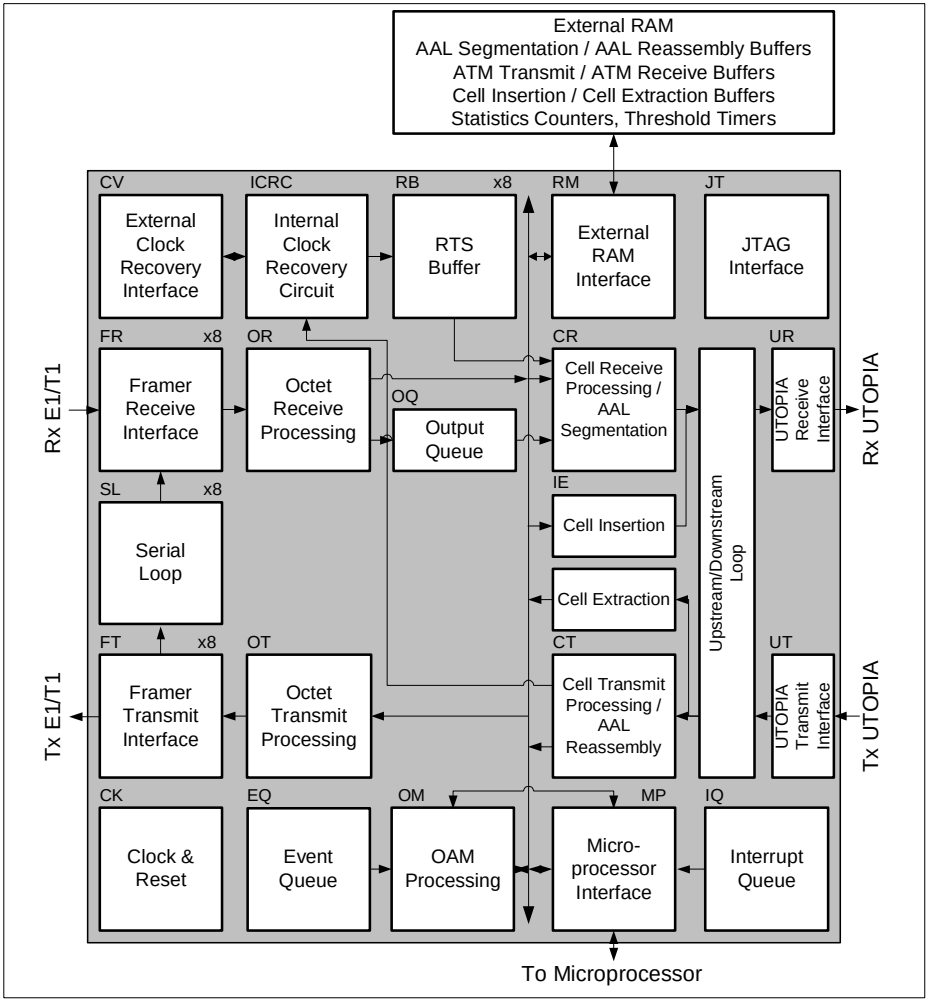


Figure 6 Block Diagram

3.3 Functional Block Description

Table 11 Functions of IWE8 Blocks

Block	Functions
FR	**Framer Receive interfaces** • FRCLK synchronization • 8 bit serial to parallel conversion • Frame and multiframe synchronization • Timeslot counter • Timeslot assignment and channel configuration (RAM1)
OR	**Octet Receive processing** ATM ports: • Cell delineation • HEC check: Header error detection and correction • Cell payload de scrambling • Idle or Unassigned Cell Deletion • Statistics counter event generation • Write to ATM Receive Buffer AAL ports: • Segmentation port de correlation • Segmentation • SN/SNP generation • SDT pointer generation • RTS value insertion • Statistics counter event generation • Write to Segmentation Buffer
OQ	**Output Queue** • FIFO containing 256 addresses of cells to be sent to UTOPIA Receive
CR	**Cell Receive processing** ATM ports: • Read cells from ATM receive buffer AAL ports: • Read cells from AAL segmentation buffer • Padding of partially filled cells
UR	**UTOPIA Receive interface** • Cell level handshake • Mapping of framer port number into ATM header in UTOPIA level 1 mode and UTOPIA level 2 single PHY mode • Output buffer for 4 cells

Table 11 Functions of IWE8 Blocks

Block	Functions
UL	**Upstream Loop** • Cell loopback from Cell Receive to Cell Transmit processing • Loopback buffer for 4 cells
DL	**Downstream Loop** • Cell loopback from UTOPIA Transmit to UTOPIA Receive • Loopback buffer for 4 cells
UT	**UTOPIA Transmit interface** • Cell level handshake • Evaluation of framer port number from ATM header in UTOPIA level 1 mode and UTOPIA level 2 singel PHY mode • Input buffer for 4 cells
CT	**Cell Transmit processing** Port and channel identification ATM ports: • Write cells to ATM transmit buffer AAL ports: • Port and channel identification • SNP field check • SN field check • SDT pointer detection and verification • RTS value extraction • Extracting reassembly buffer filling for ACM • CAS processing • Statistics counter event generation • Insertion of dummy cells at cell loss • Write to Reassembly Buffer

Table 11 Functions of IWE8 Blocks

Block	Functions
OT	**Octet Transmit processing** ATM ports: • Reading octets from ATM Transmit Buffer • Cell rate de coupling: idle/unassigned cell insertion • Cell payload scrambling • HEC generation AAL ports: • Read octets from Reassembly Buffer • Handling of Reassembly Buffer Overflow • Handling of Reassembly Buffer underflow • Reassembly Buffer initialization to compensate CDV • Synchronization of AAL1 start of structure with synchronization pulse of framer port • Statistics counter event generation
FT	**Framer Transmit interfaces** • FTCKO synchronization • 8 bit parallel to serial conversion • Generation of frame and multiframe synchronization signals • Timeslot counter • Timeslot assignment and channel configuration (RAM2, RAM3, RAM4)
SL	**Serial Loop** • Serial loopback from Framer Transmit to Framer Receive
OM	**OAM processing** • Processing of OAM counter events • Interrupt queue control • Microprocessor access control to external RAM
EQ	**Event Queue** • FIFO of 256 OAM counter events
MP	**Microprocessor interface** • Synchronization of asynchronous microprocessor interface signals • Internal registers • Interrupt generation
RM	**External RAM interface** • Generation of external RAM interface signals • Generation of basic RAM cycle • Access control to external RAM for different blocks • Parity generation and checking

Table 11 Functions of IWE8 Blocks

Block	Functions
CV	**External Clock Recovery interface** • Generation of serial communication frames to external clock recovery circuit, containing RTS values and or ACM buffer filling • Generation of synchronization for RTS generation by external clock recovery circuit. • Reception of frames with RTS values from external clock recovery circuit
RB	**RTS Buffer** • Buffer for 2 incoming RTS values per port
CK	**Clock & Reset** • Clock distribution • Reset control
JT	**JTAG interface** • Boundary Scan register • TAP controller
ICRC	**Internal Clock Recovery Circuit** • Synchronous Residual Time Stamp SRTS • Adaptive Clock Method ACM
External RAM	**ATM Transmit Buffer** • Compensate packetization delay on the PDH interface. • Maximum size of 256 ATM cells per port. • Maximum size of 64 octets per ATM cell. **ATM Receive Buffer** • Maximum size of 16 ATM cells per port. • Maximum size of 64 octets per ATM cell. **Segmentation Buffer** • Compensate segmentation delay in the ATM network. • 1024 bytes per port (unstructured CES) • 256 bytes per timeslot (structured CES) **Reassembly Buffer** • Compensate the Cell Delay Variation (CDV) of the ATM network. • 512 bytes per timeslot. (structured CES)

4 Operational Description

4.1 ATM Transmit Functions

For ports configured to ATM mode the following data flow is valid:

The Cell Transmit Processing block is responsible for:

- Cell discarding
- Write ATM cells except of UDF octet to ATM Transmit Buffer

The Octet Transmit Processing block is responsible for:

- Reading octets from ATM Transmit Buffer
- Cell rate de-coupling: idle/unassigned cell insertion
- Cell payload scrambling
- HEC generation

The ATM transmit functions are controlled by the internal registers “catm”, “atmc” and “txid”. The features controlled by these registers are common to all ATM ports.

Some features of the ATM transmit functions can be controlled per port, by programming the port specific “ATM Transmit Reference Slot” in the internal configuration RAM2

4.1.1 Operation

4.1.1.1 ATM Transmit Buffer Filling Level

The amount of buffered data in transmit direction of each port is adjustable in granularity of bytes or cells. This allows a controlled transmission delay while maintaining a continuous ATM cell flow. The feature is implemented using the port specific back pressure mechanism of the UTOPIA interface (**Chapter 5.2.2**).

The granularity and range of filling level are set independently per port in the “p_thr_m” bits of the Port Configuration Registers (“pcfN”, see **Chapter 7.1**). The port specific threshold value is defined via the corresponding Threshold Port Register (“thrspN”, see **Chapter 7.38** to **Chapter 7.41**)

2 Modes are supported:

- Mode 1 (p_thr_m = 01_B) allows the definition of threshold values in the range of 0 to 255 cells. The actual value equals the contents of thrspN.
- Mode 2 (p_thr_m = 10_B) allows the definition of threshold values in the range of 0 to 222 bytes. The actual value equals 53 * C + B, with C representing the 2 most significant bits of thrspN and B representing the 6 least significant bits of thrspN.

All other values of p_thr_m will switch off this feature and reset the internal counter.

To avoid deadlock conditions, the contents of the common 8 cell UTOPIA input buffer will always be flushed into the port specific Transmit Buffers independent from their back

pressure state. This results in two side effects, which have to be taken into account for the calculation of threshold values.

- After back pressure state has been entered, up to 8 additional cells may be transferred from the UTOPIA input buffer to the port buffer.
- Before a certain cell can cause port specific back pressure, it has to traverse the UTOPIA input buffer, resulting in a delay of 4.2 to 16.8 µs.

4.1.1.2 Cell Discarding

The discarding of cells is available for ATM ports. It can depend on

- Buffer filling level and CLP (Bit 0 of the 4th ATM header octet)
- Buffer filling level and CLPI (Cell Loss Priority Internal, bit 6 of the UDF octet at the UTOPIA interface)

The bit ENB, bit 5 of the UDF octet at the UTOPIA interface, is responsible for the decision if discarding shall base on CLP or CLPI. For bit locations see **Figure 30**.

The buffer threshold for discarding cells is configured by register “thrshld” and applies to all ports.

Cells that are going to be extracted via the microprocessor interface will be ignored by the cell discard mechanism

Table 12 ATM Cell Discarding

ENB	CLPI	CLP	Discarding
0	x	0	No
0	x	1	Yes, if buffer threshold has been exceeded
1	0	x	No
1	1	x	Yes, if buffer threshold has been exceeded

4.1.1.3 Cell rate de-coupling: Idle/Unassigned Cell Insertion

When the ATM Transmit Buffer of a port is empty, idle or unassigned cells are transmitted to provide cell rate de-coupling.

Idle cells are transmitted as defined in the ITU-T I.361 [30]. Unassigned cells can be inserted, as defined in the B-ISDN UNI and NNI physical layer generic criteria [15].

The 4 MSBs of header octet 1 and the 4 LSBs of header octet 4 are programmable in the “prg_tx_hd” field of the TX Idle/Unassigned Cell Control Register (txid, see **Chapter 7.10**). All other header bits will be 0.

octet 1	GFC[3:0]/VPI[11:8] = prg_tx_hd[7:4]	VPI[7:4] = 0000_B	
octet 2	VPI[3:0] = 0000_B	VCI[15:12] = 0000_B	
octet 3	VCI[11:4] = 0000_0000_B		
octet 4	VCI[3:0] = 0000_B	PTI[2:0] = prg_tx_hd[3:1]	CLP = prg_tx_hd[0]
octet 5	UDF		
octet 6	prg_tx_pl[7:0]		
.	.		
octet 53	prg_tx_pl[7:0]		

- If idle cell insertion according to ITU-T I.361 or ITU-T I.432.1 is desired, the “prg_tx_hd” field of “txid” should be set to 0000_0001_B.
- If unassigned cell insertion at the NNI or uncontrolled UNI according to ITU-T I.361 is desired, the “prg_tx_hd” field of “txid” should be set to 0000 XXX0. For X any value is allowed.

The payload of idle or unassigned cells consists of the same octet which is repeated 48 times. It is programmable by the “prg_tx_pl” field of the “txid” register.

- For ITU-T I.432.1 compliant idle cells, the “prg_tx_pl” field of “txid” should be set to 0110_1010_B.
- The pre-assigned values of the information field of all unassigned cells are for further study (ITU-T I.361 [30])

4.1.1.4 Cell Payload Scrambling

ITU-T I.432.3 [34] recommends the self-synchronizing scrambler $x^{43}+1$ for payload scrambling at E1 datarates. For T1 no scrambling is recommended, which the IWE8 supports.

The scrambler function is implemented in the device. It can be disabled per port by the x43_scrambling bit in the “ATM Transmit Reference Slot” in RAM2.

4.1.1.5 HEC Generation

The HEC generation is implemented according to ITU-T I.432.1 [33] using the generator polynomial $x^8 + x^2 + x + 1$. To significantly improve the cell delineation performance in the case of bit-slips it is recommended that

- the check bits are added (modulo 2) to an 8-bit pattern (coset) before being inserted in the last octet of the header.
- the recommended pattern is “0101 0101".

- the receiver must subtract (equal to add modulo 2) the same pattern from the 8 HEC bits before calculating the syndrome of the header.

As an example, if the first 4 octets of the header were all zeros the generated header before scrambling would be “00000000_00000000_00000000_00000000_01010101”. The starting value for the polynomial check is 0s (binary)

The coset value is programmable in the ATM Control Register (“atmc”, see **Chapter 7.8**).

4.1.2 Setup of ATM Transmit Ports

Each ATM transmit port can be configured in the “channel_mode” field of the “ATM Transmit Reference Slot” in RAM2 to operate in “Inactive”, “Active” or “Standby” mode.

In “Inactive” mode, byte-pattern 0 “bp0” is continuously sent to the framer transmit interface.

In “Active” mode, user cells or idle/unassigned cells are sent to the framer transmit interface.

In “Standby” mode, only idle/unassigned cells are sent to the framer transmit interface.

When activating ATM transmit ports, it is important to follow the initialization sequence as shown in **Table 13**. Step 2 must be held at least 250 µs to internally reset the ATM transmit port. During this time the device connected to the Framer Receive Interface has to be in normal operation allowing the IWE8 to synchronize itself on the frame pulse.

Table 13 Activation sequence for ATM transmit ports

Step	pcfN. p_tx_act	ATM Transmit Reference Slot. channel_mode	Minimum Time
1	0 = inactive	00 = Inactive	
2	1 = active	00 = Inactive	250 µs
3	1 = active	01 or 11 = Active	

4.2 ATM Receive Functions

For ports configured to ATM mode the following data flow is valid:

The Octet Receive Processing block is responsible for:

- Cell delineation
- HEC check: Header error detection and correction
- Cell payload de-scrambling
- Idle or Unassigned Cell Deletion
- Statistics counter event generation
- Write cells except of UDF octet to ATM Receive Buffer

The Cell Receive Processing block is responsible for:

- Read cells from ATM Receive Buffer

The ATM receive functions are controlled by the internal registers “catm”, “atmc” and “rxid”. The features controlled by these registers are common to all ATM ports.

Some features can be controlled per port. They were configured by programming the port specific “ATM Receive Reference Slot” in the internal configuration RAM.

4.2.1 Operation

4.2.1.1 Cell Delineation

The cell delineation algorithm is implemented according to the ITU-T Recommendation I.432.1 [33].

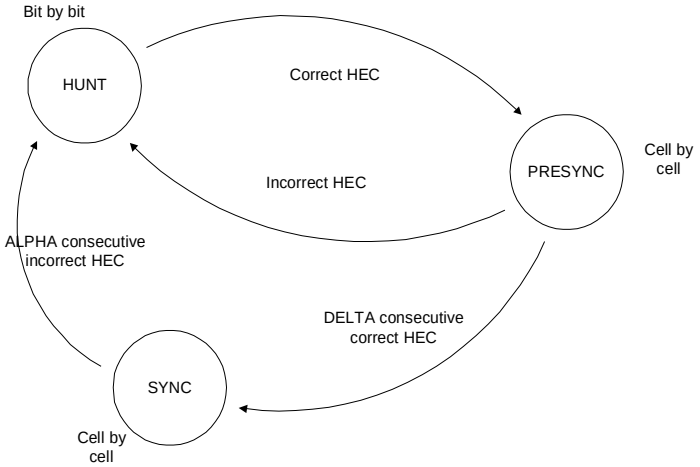
To support detection of “Out of Cell Delineation” (OCD) anomalies and “Loss of Cell Delineation” (LCD) defect, the IWE8 generates an interrupt in eis4 (**Chapter 7.22**) whenever the SYNC state is left or entered. The generation of interrupts is controllable on a per port basis through fields in the “ATM Receive Reference Slot” of RAM1 (**Chapter 6.1.1.1**). It is also possible to see the current state of the cell delineation FSM (Finite State Machine) in the Cell Delineation FSM Status Register (“cdfs”, see **Chapter 7.15**).

The software can then start a timer (e.g. timer_set_1 provided by the IWE8) to establish the LCD defect state.

As octet boundaries are available within the receive physical layer prior to cell delineation, the cell delineation process is performed octet by octet in the HUNT state. As long as the cell delineation is not in the SYNC state, received octets are discarded.

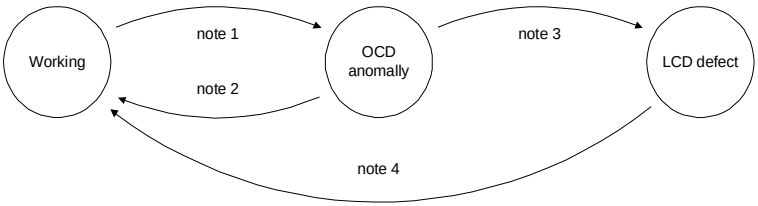
The ALPHA and DELTA parameters, which influence the robustness of the algorithm against false misalignment due to bit errors (ALPHA) and false delineation in the re synchronization process (DELTA), are programmable to values between 0 and 15 in the ATM Control Register (atmc, see **Chapter 7.8**), These settings are common for all ATM ports. ITU-T I.432.1 [33] recommends:

- for the Cell-based Physical Layer, ALPHA = 7 and DELTA = 8.
- for the Frame-based Physical Layer, ALPHA = 7 and DELTA = 6.
- for other systems, values for ALPHA and DELTA are for further study.



Note - The "correct HEC" means the header has no bit error (syndrome is zero) and has not been corrected

Figure 7 Cell delineation state diagram (Figure 5/I.432.1)



note1 Triggered by state transition (Case A) due to alpha consecutive incorrect HEC´s in the cell delineation process (Fig. 5 of ITU-T Recommendation I.432.1)

note2 Triggered by state transition (Case B) due to delta consecutive correct HEC´s in thecell delineation process (Fig. 5 of ITU-T Recommendation I.432.1)

note3 Triggered by 50 continuous ms in the OCD anomaly maintenance state

note4 Triggered by 50 continuous ms in the cell delineation "Sync" state (Fig.5 of ITU-T Recommendation I.432.1)"

Figure 8 Maintenance state transition diagram for cell delineation events (Figure 2/ I.432.3)

The Loss of Cell Delineation (LCD) state is entered whenever the Out of Cell (OCD) state is continuously active for more than an user defined period of time, ITU-T I.432.1 recommends a persistence time of 50ms.

For each port a separate timer is implemented. All timers can be enabled via the ´lcd_en´ bit in the LCD Timer Register (“lcdtimer”, see **Chapter 7.43**). The global preload value is defined by the “lcd_val” bits in lcdtimer. After expiration of each timer, an “lcd_start” interrupt is generated, indicated in the Interrupt Status Register 1 (isr1, see **Chapter 7.18**) and the Extended Interrupt Status Register 0 (eis0, see **Chapter 7.42**).

If enabled, the timer is started at the transition from SYNC to OCD-state. After expiration LCD state is entered. Whenever the SYNC state is entered before the timer expires, the timer is reset.

The transition from LCD to Working state follows the same procedure. If after the LCD state the SYNC state is entered again, the timer is started and after expiration the maintenance state machine is in working state again. In parallel an “lcd_end” interrupt is generated indicated in “isr1” and “eis0”. If synchronization is lost again during the timer period, LCD state is reentered and the timer is reset.

To force resynchronization of the cell delineation process, the microprocessor can force individual ports to enter the HUNT state, by setting the bit “go_hunt” in the corresponding “ATM Receive Reference Slot” of RAM1 (**Chapter 6.1.1.1**).

4.2.1.2 HEC Check: Header Error Detection and Correction

The Header Error Control (HEC) is implemented according to the ITU-T I.432.1 B-ISDN user-network interface - Physical layer specification [33].

According to the HEC algorithm, cells are discarded when a multi-bit header error is detected in the Correction mode or a header error is detected in the Detection mode.

According to the HEC algorithm, cells are corrected when a single-bit error is detected in the Correction mode.

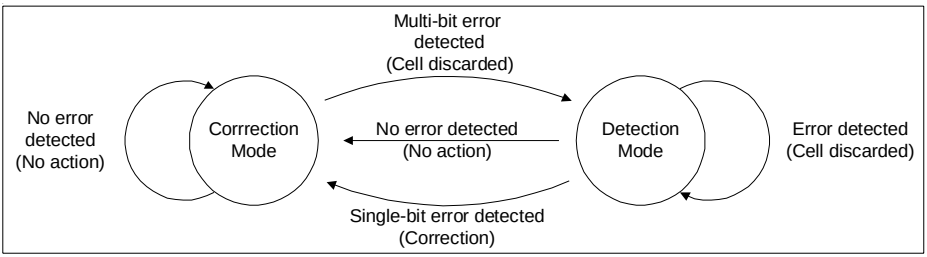


Figure 9 HEC: Receiver mode of Operation (Figure 3/ITU I.432.1)

The pure HEC detection mode as recommended by the ATM Forum is selectable via bit “a_hec_algor” in register acfg (see **Chapter 7.2**)

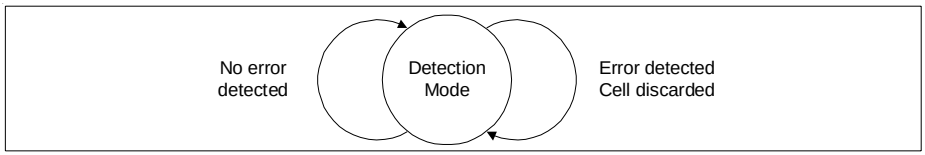


Figure 10 HEC Detection According to ATM Forum

No discarding of HEC errored cells as an option is available and selectable via bit “a_hec_mode” in the register acfg (**Chapter 7.2**). In this case an errored HEC is indicated by setting the most significant bit in the UDF field at the UTOPIA receive interface. For correct operation bit P_CELL_DIS must be cleared.

4.2.1.3 Cell Payload Descrambling

ITU-T I.432.3 [34] recommends the self-synchronizing scrambler $x^{43}+1$ for payload scrambling at E1 data rates. For T1 no scrambling is recommended.

The self-synchronizing scrambler function is implemented in the device. It can be disabled per port by the x43_descrambling bit in the “ATM Receive Reference Slot” in RAM1.

4.2.1.4 Idle, Physical Layer or Unassigned Cell Deletion

According to ITU-T I.361 [30], idle cells, physical layer OAM cells and cells reserved for use by the physical layer are not passed to the ATM layer at the UNI.

	Octet 1	Octet 2	Octet 3	Octet 4
Idle cell identification (Notes 1 and 2)	0000/0000	0000/0000	0000/0000	0000/0001
Physical OAM cell identification (Note 2) layer	0000/0000	0000/0000	0000/0000	0000/1001
Reserved for use of the physical layer (Notes 1, 2 and 3)	PPPP/0000	0000/0000	0000/0000	0000/PPP1

P: Indicates the bit is available for use by the physical layer
Values assigned to these but have no meaning with respect to the fields occupying the corresponding bit positions at the ATM layer

Notes:

1 In the case of physical layer cells, the bit in the location of the CLP indication is not used for the CLP mechanism as specified in 3.4.2.3.2/I.150.

2 Cells having header values which are identified as idle, physical layer OAM, and reserved for use by the physical layer are not passed to the ATM layer from the physical layer.

3 Specific pre-assigned physical layer cell header values are given in Recommendation I.432

Figure 11 Pre-assigned cell header values at the UNI for use by the physical layer (excluding the HEC field) (Table 1/I.361)

In contrast to this the ATM-Forum recommends in the User-network interface specification that the receiving ATM entity is responsible for extraction and discarding of unassigned and idle cells.

Use	Octet 1	Octet 2	Octet 3	Octet 4
invalid	XXXX/0000	0000/0000	0000/0000	0000/XXX1
unassigned	0000/0000	0000/0000	0000/0000	0000/XXX0

X: Indicates “don’t care” bits

Figure 12 Pre-defined header field values [11]

The RX Idle/Unassigned Cell Control Register (rxid, see **Chapter 7.9**) can be used in order to achieve ITU-T or ATM-Forum compliance.

The 4 MSBs of header octet 1 and the 4 LSBs of header octet 4 of the received cells to be discarded are programmable in bits “prg_rx_hd”. All other header bits must be 0. On top the “msk_rx_hd” field of “rxid” allows to mask all or some of these bits. The masked bits are considered as “don’t care”.

- If ITU-T I.361 compliance is desired, the “prg_rx_hd” field should be set to 0000 0001. If only idle cells should be deleted, the “msk_rx_hd” should be set to 0000 0000.

If all physical layer cells should be deleted, the “msk_rx_hd” should be set to 1111 1110.

- For ATM Forum compliance, the “prg_rx_hd” field should be set to 0000 0000. The “msk_rx_hd” should be set to 1111 1110. This configuration will delete all unassigned cells.

The deletion of idle, physical layer or unassigned cells can be enabled or disabled per port by “delete_idle_cells” in the “ATM Receive Reference Slot” of RAM1 (**Chapter 6.1.1.1**).

4.2.2 Setup of ATM Receive Ports

Each ATM receive port can be configured in the “channel_mode” field of the “ATM Receive Reference Slot” in RAM1 to operate in “Inactive”, “Active” or “Standby” mode.

In “Inactive” mode, no data is accepted from the framer receive interface.

In “Active” mode, data is accepted from the framer receive interface, cells are written into the ATM Receive Buffer and cell addresses are written into the Output Queue.

In “Standby” mode, data is accepted from the framer receive interface but no cells are written into the ATM Receive Buffer or the Output Queue. This mode can be used to test the cell delineation.

When activating ATM receive ports, it is important to follow the initialization sequence as shown in **Table 14**. Step 2 must be held at least 250 µs to internally reset the ATM receive port. During this time the device connected to the Framer Transmit Interface has to be in normal operation allowing the IWE8 to synchronize itself on the frame pulse.

Table 14 Activation sequence for ATM receive ports

Step	pcfN. p_rx_act	ATM Receive Reference Slot. channel_mode	Minimum Time
1	0 = inactive	00 = Inactive	
2	1 = active	00 = Inactive	250 µs
3	1 = active	01 or 11 = Active	

4.3 AAL Segmentation Functions

This function implements the Convergency Sublayer for Structured Data Transfer (SDT) and Unstructured Data Transfer as well as the Segmentation Sublayer for AAL type 1 as described in ITU-T recommendation I.363.1 [31]. The structure of AAL1 SAR-PDU is shown in **Chapter 12**.

The Octet Receive Processing block is responsible for:

- Segmentation port decorrelation
- Segmentation
- SN/SNP generation
- SDT pointer generation
- RTS value insertion
- Statistics counter event generation
- Write to Segmentation Buffer

The Cell Receive Processing block is responsible for:

- Read cells from Segmentation Buffer
- Padding of partially filled cells

4.3.1 Operation

4.3.1.1 Segmentation Port Decorrelation

In synchronous systems, the microprocessor may activate a number of channels consecutively, in phase with the segmentation period of a particular channel, causing a large number of cells to be generated within the same 125 µs period. This would result in a large number of cells residing in the Output Queue and increase the Cell Delay Variation (CDV).

To avoid this, a decorrelation circuit has been implemented in the “Octet Receive processing” (OR), that inserts a random waiting period between activation of a channel and start of cell segmentation. This feature can be activated by setting bit “dcor” in the “AAL Receive Reference Slot” of the channel in RAM1. Otherwise segmentation is started as soon as the channel has been activated by the microprocessor (field “channel_mode”)

The decorrelation circuit consists of a free-running 5-bit counter at a frequency of F_{CLOCK}/ 3360 (7.5 KHz if F_{CLOCK}= 25 MHz) a register containing a random number (bits “dcor_random_nr”) and a comparator. Each time an octet for this channel is received the counter is compared with the random value. Only when both values are equal, segmentation is started.

When using the decorrelation circuit make sure that the random number is written to the “dcor_random_nr” field of the “AAL Receive Reference Slot” before activating the channel with “channel_mode”

In SDT mode, the cells are segmented when the first (multi) frame synchronization pulse after segmentation start is received from the framer receive interface of that channel. The resulting SC value and pointer field of the first cell transmitted will both be 0.

4.3.1.2 Segmentation

The segmentation and reassembly function can be programmed to use, alternatively to the standard AAL type 1 SAR-PDU, a SAR-PDU that is referred to as AAL type 0 and consists of 48 octets payload without any overhead. The selection is done by programming the “AAL0” field in the “AAL Receive Reference Slot”.

AAL Type 0

Figure 13 shows the AAL type 0 SAR-PDU. It is possible to fill only part of the SAR-PDU payload with User Information octets by programming field “part_fill” in the “AAL Receive Reference Slot” of RAM1 to values smaller than 48.

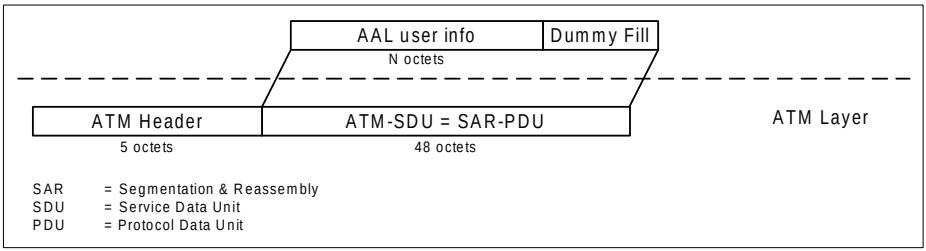


Figure 13 SAR-PDU of AAL Type 0

AAL Type 1 SDT Structure Length

For Structured Circuit Emulation Service as defined by the ATM-Forum in “Circuit Emulation Services Version 2.0" [10] Structured Data Transfer (SDT) is used. The structure length used for SDT in ATM cells is:

- N when frame-based SDT is selected
- N x 16 when CRC multiframe-based SDT is selected for E1 ports
- N x 24 when superframe-based SDT or extended superframe-based SDT is selected for T1 ports.

The selection between frame-based or multiframe-based SDT is done by the bit “sdt_mfs” in the “AAL Receive Reference Slot”.

4.3.1.3 Transport of the Framer Port Number

If the UTOPIA interface is configured for level 2 MPHY mode, the framer port number is transported via the UTOPIA address bits. In UTOPIA level 1 and UTOPIA level 2 single PHY mode the framer port number is mapped into the ATM Header (see **Chapter 5.2.3**).

4.3.1.4 Transport of CAS Information

The four CAS bits for each timeslot are transported within one multiframe from the framer to the IWE8. A signalling buffer in the internal RAM (256 x 4 x 2bit) holds the CAS bits from the framer interface. The activation of CAS packetization can be done via “p_cas” in the register “pcfN”.

The CAS bits will be packed in a signalling substructure after the payload of one multiframe has been packetized.

4.3.1.5 CAS Conditioning and Freezing Upstream

Normally the framer device is responsible for signalling freezing or signalling conditioning in case of line failure. If the framer doesn’t support the feature the IWE8 can also fulfill the requirements according to Bellcore TR-NWT-000170 [14].

Pin “FRLOS = 1" indicates that the CAS information from the framer device is invalid and CAS conditioning or freezing upstream is starting. This state remains active until valid CAS bits are available indicated by “FRLOS = 0".

CAS freezing means that the last valid CAS information is repeated as long as the error cause exists. In case of CAS conditioning for each timeslot individual CAS conditioning nibbles are sent instead. Selection between both procedures is done by setting “sig_cond” in the “AAL Receive Reference Slot”. If the channel bandwidth is one slot, the signalling conditioning nibbles are defined in the field “next_slot_nr” of the “AAL Receive Reference Slot”. If the channel bandwidth is more than one slot, the signalling conditioning nibbles are defined in the “sig_cond_nibble” of the “AAL Receive Continuation Slot”. In the latter case the signalling conditioning nibbles defined in the first “AAL Receive Continuation Slot” are used for the first two slots.

Table 15 Definition of the CAS Signalling Conditioning Nibbles.

Slot Number	Channel Bandwidth = 1 Slot	Channel Bandwidth >= 2 Slots
1	“next_slot_nr” of the “AAL Receive Reference Slot”	“sig_cond_nibble” of the first “AAL Receive Continuation Slot”
2	-	“sig_cond_nibble” of the first “AAL Receive Continuation Slot”
3	-	“sig_cond_nibble” of the second “AAL Receive Continuation Slot”
N	-	“sig_cond_nibble” of the N-1th “AAL Receive Continuation Slot”

4.3.1.6 Segmentation Buffer

The Segmentation Buffer is located in external RAM providing 256 bytes of memory for each timeslot, totalling to 64 KB for 8 ports with 32 timeslots each. The buffer for each timeslot consists of 4 blocks with 64 octets:

Buffer size = 8 Ports x 32 Channels x 4 Blocks x 64 Octets [1]

In unstructured CES mode, one Segmentation Buffer per port provides 16 blocks.

In structured CES mode, a Segmentation Buffer per channel with a variable capacity depending on the number of channels and the cell filling level is automatically configured by the IWE8. The number of memory blocks depends on the bandwidth of the channel. Thus for structured CES with N x 64-kbit/s there are N x 4 blocks per connection. Each channel can occupy 1, 2 or 4 block-groups (4, 8 or 16 blocks). The first block-group defines the reference slot number of the channel. The second, third and fourth block-groups define the number of the corresponding interface slot of the channel.

The one-to-one relationship between timeslots and groups of memory blocks allows dynamic re-configuration of a specific channel without disturbing other channels of the same port.

Table 16 Relationship between Cell Filling and Segmentation Buffer Subblock Size

Cell Filling AAL0 (octets)	Cell Filling AAL1, no SDT (octets)	Cell Filling AAL1, with SDT (octets)	Octets per block	Cells per block	Octets per cell
25-48	25-47	25–47	64	1	64
4-24	4-24	4–24	64	2	32

4.3.1.7 Padding Partially Filled Cells

The value, used for dummy fill of partially filled cells, is programmable in the Cell Fill Register for Partially Filled Cells (“cfil”, see **Chapter 7.12**). The fill octets carry no information and are ignored at the receiver.

Table 17 shows valid values for the cell filling level, which can be configured in the field part_fill of RAM1: AAL Receive Reference Slot (see **Chapter 6.1.1.3**) and RAM2: AAL Transmit Reference Slot (see **Chapter 6.1.2.3**). All other values are illegal.

Table 17 Cell Filling level values

ATM Adaptation Layer Type	Partially Filled		Completely Filled
	Minimum	Maximum	
AAL0	4	47	48
AAL1	4	46	47[1)2)]
AAL1 with CAS	4+Cb[3)]	46	47[2)]

1) If frame based SDT without CAS is used and filling level ≤ 45, the condition band_width ≤ part_fill has to be fulfilled for correct operation.
Multiframe based SDT without CAS should not be used.

2) non-P format, cell may have only 46 user data octets in P format

3) Cb: Required bytes for the CAS subblock in an ATM cell = RoundUp(N/2)

4.3.2 Setup of AAL Segmentation Channels

In “Inactive” mode, no data is accepted from the framer receive interface.

In “Active” mode, data is accepted from the framer receive interface, segmented and cells are written into the Segmentation Buffers and the Output Queue.

In “Standby” mode, data is accepted from the framer receive interface but no cells are written in the Segmentation Buffers.

In “Substitute” mode, data is accepted from the framer receive interface, but substituted by a programmable byte-pattern selected by “subst_bpslct” in the “AAL Receive Reference Slot”. Cells are written into the Segmentation Buffers and the Output Queue. This mode can be used for trunc conditioning to indicate idle (bit pattern = 0x7F) or out-of-service conditions (bit pattern = 0x1A) according to af-vtoa-0078 [10] and TR-NWT-000170 [14]

When activating the AAL segmentation channels, it is important to follow the initialization sequence as shown in **Table 18**. Step 2 must be held at least 250 µs to internally reset the AAL channel. During this time the device connected to the Framer Receive Interface has to be in normal operation allowing the IWE8 to synchronize itself on the frame pulse.

Table 18 Activation sequence for AAL segmentation channels

Step	pcfN p_rx_act	AAL Receive Reference Slot. channel_mode	Minimum Time
1	0 = inactive	00 = inactive	
2	1 = active	00 = inactive	250 µs
3	1 = active	01 or 11 = active	

The RTS value stored in the RTS buffer of the port is loaded from the Internal Clock Recovery Circuit ICRC or from the Clock Recovery Interface. A new value will be provided by the ICRC once every cycle of 8 cells. To guarantee that the value stored in the RTS buffer of the port is correct, the procedure indicated in **Figure 14** is followed.

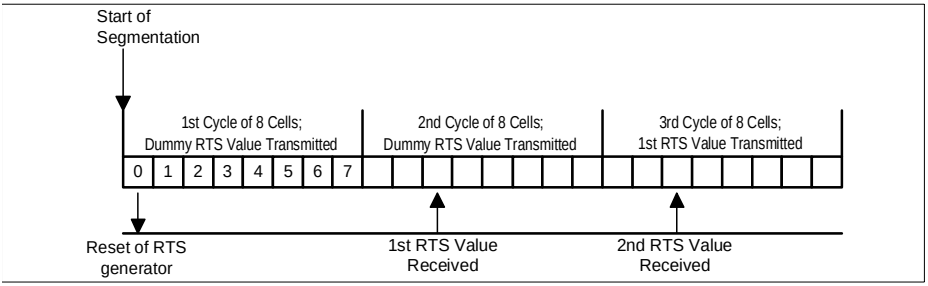


Figure 14 Synchronization of SRTS Generation with the Start of Segmentation

After the start of segmentation, during the 1st cycle of 8 cells, the RTS generator of the corresponding port is reset. If an external clock recovery circuit is used, it is reset by writing a reset frame for the corresponding port on the Clock Recovery Interface. During this cycle a dummy RTS value is transmitted.

During the 2nd cycle of 8 cells, the IWE8 expects to receive the first valid RTS value while transmitting a dummy RTS value.

During the following cycles of 8 cells the RTS value received in the previous cycle will be transmitted.

The dummy RTS value is programmable with “a_dummy_srts” in the register “acfg” and is common for all ports. It must be programmed before the a_crv_en bit in “acfg” is made active. Otherwise the first 2 RTS values transmitted will be fixed at “0000”.

If the ICRC does not provide new RTS values to the RTS Transmit Buffer (buffer underflow), the last received value is repeated. If too many RTS values are provided (buffer overflow), the values in excess will be omitted and a “rts_overflow” bit in the Extended Interrupt Status Register 2 “eis2” is set.

4.4 AAL Reassembly Functions

When AAL type 0 is enabled in the “AAL Transmit Reference Slot”, the SAR-PDU and SAR-SDU processing is disabled.

When AAL type 0 is disabled in the “AAL Transmit Reference Slot”, the SAR-PDU header is processed according to AAL type 1 as defined in ITU-T I.363.1 [31].

For ports configured to AAL mode the following data flow is valid:

The cell transmit processing block is responsible for:

- Port and channel identification
- SNP field check
- SN field check
- SDT pointer detection and verification
- SRTS value extraction
- CAS processing
- Statistics counter event generation
- Insertion of dummy cells at cell loss
- Write to Reassembly Buffer

The octet transmit processing block is responsible for:

- Read octets from Reassembly Buffer
- Handling of Reassembly Buffer Overflow
- Handling of Reassembly Buffer underflow
- Reassembly Buffer initialization to compensate CDV
- Synchronization of SDT structure with port structure
- Statistics counter event generation

4.4.1 Operation

4.4.1.1 Port and Channel Identification

Before an incoming cell is processed, it is determined to which port and channel the cell is destined. This information is retrieved from the UTOPIA interface (see **Chapter 5.2.3**).

4.4.1.2 Sequence Number Protection field check

When an un-correctable multi-bit error is detected the Sequence Number (SN) field of the SAR-PDU header is declared invalid, otherwise the SN field is valid. The function can be enabled or disabled by the bit “snp_check” in the “AAL Transmit Reference Slot”. If disabled the SN of all incoming cells are declared valid.

4.4.1.3 Sequence Number field check

This function implements the sequence number processing. It can be enabled via bit “sn_check” in the “AAL Transmit Reference Slot”. If enabled, selection can be made between Robust and Fast Sequence Count Algorithm as defined in the ITU-T I.363.1 [31] by “sn_fast” in the “AAL Transmit Reference Slot”. If SN check is disabled, all cells are accepted, no cells are discarded, lost and misinserted cells are not detected.

4.4.1.4 RTS Extraction and Verification

When the clock recovery verification is enabled (“crv_en” in the “AAL Transmit Reference Slot”), and the port is configured for SRTS (“p_rts” = 1), RTS values are extracted and verified.

The RTS value consists of the four CSI bits of the cells with odd SC values within a cycle of 8 cells. A RTS value is accepted as correct if the following condition is true:

- The SN field is valid
- Four consecutive odd SC values (1, 3, 5 or 7) were received in the previous cycle of 8 cells

Otherwise the dummy RTS-value is used.

When the start of a new cycle is detected, the RTS value of the previous cycle is written to the ICRC.

4.4.1.5 Pointer Field Detection and Verification

When SDT is enabled (“sdt” = 1 in the “AAL Transmit Reference Slot”), it is assumed that the channel is using Structured Data Transfer. The SAR-PDU payload is supposed to be of the P format under the following conditions:

- The SN field is valid
- Even SC value (0, 2, 4 or 6)
- The CSI field = 1

When the “sdt_once” bit in the “AAL Transmit Reference Slot” is set to 1, only the first cell with CSI bit = 1 in a cycle of 8 cells is supposed to contain a P format SAR-SDU. The other cells with CSI bit = 1 within the same cycle are treated as non-P format. This operation is recommended by ITU-T I.363.1 [31]

In the cells that are supposed to contain a P format SAR-SDU, the pointer field is verified and accepted under the following conditions:

- The parity bit is correct as defined in the ITU-T I.363.1 [31]
- The value of the offset field is between 0 and 93 or is the dummy value 127.

If an invalid pointer field (93 < pointer < 127) is detected, its content is replaced by the dummy value (127). The SAR-SDU is processed as if it would have been received with a dummy pointer value. The P format of the SAR-PDU payload is assumed and the first octet of the SAR-PDU payload is not processed as user information.

The bit “sdt_par” in the “AAL Transmit Reference Slot” allows to disable the verification of the parity bit in the pointer field.

For multiframe based SDT the bit “sdt_mfs” in the “AAL Transmit Reference Slot” has to be set.

4.4.1.6 CAS Conditioning and Freezing Downstream

An internal signalling buffer holds the CAS bits. In case of buffer underflow or pointer mismatch the IWE8 provides downstream CAS conditioning and freezing according to Bellcore TR-NWT-000170 [14].

The selection between both is done individually for each channel via Bit “cond_en” in the “AAL Transmit Conditioning Slot” of RAM4. Values for conditioning can be selected via the “cond_down_nibble” bits in the same register.

The spare and alarm indication bits of the first E1 frame can be programmed by setting bits cas0portN in the registers “cas1” and “cas2”. The CAS information of idle timeslots can be chosen by setting bits in the register “cas3”.

4.4.1.7 Insertion of Dummy Cells at Cell Loss

Upon cell loss detection, the sequence count algorithm will insert dummy cells into the Reassembly Buffer to maintain bit count integrity. The maximum amount of consecutively inserted cells is 6.

These dummy cells are physically inserted when reading the Reassembly Buffer. The Reassembly Buffer itself contains only control field in front of the payload of the next accepted cell, indicating the amount of dummy cells to be inserted.

Inserted dummy cells are not taken into account for the ACM Reassembly Buffer filling level calculation. This means that the buffer filling level is incorrect as long as dummy cells are physically inserted.

The data octet used for the dummy cells is the byte-pattern selected by the “starv_bpslct” field of the “AAL transmit reference slot” of RAM3.

4.4.1.8 Reassembly Buffer

The purpose of the Reassembly Buffer is to compensate the Cell Delay Variation (CDV) of the ATM network.

It is located in external RAM providing 512 byte of memory for each timeslot, totalling to 128 KB for 8 ports with 32 timeslots each. The buffer for each timeslot consists of 8 memory blocks with 64 octets:

Buffer size = 8 Ports x 32 Channels x 8 Blocks x 64 Octets [2]

The number of memory blocks used depends on the bandwidth of the channel (N*64-kbit/s). Thus for structured CES with N*64-kbit/s there are N x 8 memory blocks per connection.

The one-to-one relationship between timeslots and groups of memory blocks allows dynamic re-configuration of a specific channel without disturbing other channels of the same port.

4.4.1.9 Handling of Reassembly Buffer Overflow

Overflow is detected when, at the moment of storing an accepted cell, the extra payload of the new cell in the buffer would exceed the logical size of the Reassembly Buffer.

For AAL type 1 two possible actions exist:

- The cell is discarded.
  Re-initialization of the Reassembly Buffer as described in **Chapter 4.4.2.4** is in line with the ITU-T I.361.1 [31]
- The cell is accepted but the Reassembly Buffer is automatically re-initialized.
  Re-initialization is done automatically without disturbing the microprocessor.

The action chosen is determined by the “auto_reinit_of” field in the “AAL Transmit Reference Slot” in RAM3.

When using AAL type 0, the accepted cell is considered to be a misinserted cell and rejected.

4.4.1.10 Handling of Reassembly Buffer Underflow

An underflow period is detected when no octets are available in the Reassembly Buffer to be passed to the framer transmit interface. During the underflow period starvation octets are passed to the framer transmit interface and Statistics Counter 12 increments if enabled.

For AAL type 1, the underflow is considered to be caused by an extremely late cell. The length of the underflow period is measured by counting the number of transmitted starvation octets, expressed as a number of starvation cells that are counted by Statistics Counter 13 if enabled

For resolving the underflow two possibilities exist:

- Manual re-initialization:
  Re-initialization of the Reassembly Buffer as described in **Chapter 4.4.2.4** is in line with the ITU-T I.361.1 [31]
- Automatic re-initialization:
  As soon as start of underflow is detected, the Reassembly Buffer is re-initialized without disturbing the microprocessor. Thus, the underflow status for the device is no longer valid although the underflow condition still exists. No starvation cells due to underflow will be inserted and counter 13 will not increment

The action chosen is determined by the “auto_reinit_uf” field in the “AAL Transmit Reference Slot” in RAM3.

For AAL type 0 the detection of an underflow period is considered to be the detection of cell loss. For this reason a dummy cell is inserted. The inserted dummy cell must be reflected in the buffer filling level of the Reassembly Buffer.

4.4.1.11 Synchronization of SDT Structure with Port Structure

In normal operation the “ATM start of structure” is synchronized with the “Port start of structure”. Since this synchronization may get lost, the coincidence of both events is monitored. If they do mismatch, a two bit error counter is incremented. Upon reaching a programmable threshold, the Reassembly Buffer is re-initialized and Statistics Counter 14 is incremented if enabled. The threshold value is programmed in the “sdt_oos_nr” field of the “AAL Transmit Reference Slot” in RAM2. If the Statistics Counter 14 should reflect “atmfCESPointerReframes” as defined in [10], “sdt_oos_nr” should be set to “00”.

To compensate cell loss the Sequence Count algorithm inserts dummy cells filled with starvation octets. In case the cell filling level is 46 octets or less, the bit count integrity won’t be violated as the length of the AAL-user information within one SAR-SDU is always the same. When operating with a cell-filling of 47 octets, the AAL-user information maybe 47 octet in case of non-P format or 46 octet in case of P format SAR-PDU. As the information on the lost cell’s SAR-PDU format is not available, it is possible that an excess of starvation octets is transmitted. As a result, the “ATM start of structure” might be out of phase with the “Port start of structure”.

The following procedure is implemented for re-synchronization:

- At the end of expanding a burst of dummy cells a flag is set, indicating that a phase shift might occur. The maximum phase shift is 2 octets (e.g. 2 cells with pointers are lost within a sequence of eight cells)
- When an “ATM start of structure” is received and a positive phase shift is detected lower than or equal to 2 octets, an equal number of octets is deleted in the Reassembly Buffer and the flag is reset.
- When the detected phase shift is larger than the allowed value or negative the flag is reset and the Reassembly Buffer is re-initialized.
- When no phase shift is detected the flag is reset.

4.4.2 Setup

4.4.2.1 Setup of Reassembly Channels

Each AAL transmit channel can be configured in the “channel_mode” field of the “AAL Transmit Reference Slot” to operate in “Inactive”, “Standby” or “Active” mode.

- In “Inactive” mode, no cells are accepted from the “UTOPIA Transmit interface”, and byte-pattern 0 is sent to the framer transmit interface.
- In “Standby” mode, cells are accepted from the “UTOPIA Transmit interface”, but byte-pattern 0 is sent to the framer transmit interface.
- In “Active” mode, cells are accepted from the “UTOPIA Transmit interface”, and user data octets are sent to the framer transmit interface.

When activating the AAL reassembly channels, it is important to follow the initialization sequence as shown in **Table 19**. Step 2 must be held at least 250 µs to internally reset the AAL channel. During this time the device connected to the Framer Transmit Interface has to be in normal operation allowing the IWE8 to synchronize itself on the frame pulse.

Table 19 Activation sequence for AAL reassembly channels

Step	pcfN. p_tx_act	AAL Transmit Reference Slot. channel_mode	Minimum Time
1	0 = inactive	00 = Inactive	
2	1 = active	00 = Inactive	250 µs
3	1 = active	01 or 11 = Active	

4.4.2.2 Physical Reassembly Buffer Size

Based on the cell filling level, AAL type and use of SDT, a memory block can be divided into subblocks, where the user data octets of a single cell are stored. The size of the memory subblock per Reassembly Buffer is automatically adapted. **Table 20** shows this relationship.

Table 20 Relationship between Cell Filling and Reassembly Buffer Subblock Size

Cell Filling AAL0 (octets)	Cell Filling AAL1, no SDT (octets)	Cell Filling AAL1, with SDT (octets)	Octets per block	Cells per block	Octets per cell
33–48	32–47	31–47	64	1	64
17–32	16–31	15–30	64	2	32
9–16	8–15	7–14	64	4	16
4–8	4–7	4–6	64	8	8

The physical Reassembly Buffer size used for a N x 64 kbit/s connection is given by:

Physical Size(octets) = N x 8 x Cell Filling x Cells per Block. [3]

4.4.2.3 Initialization of the Reassembly Buffer

Before a channel is activated, the Reassembly Buffer must be configured properly to compensate Cell Delay Variation (CDV).

In order to avoid buffer underflow due to large cell distances the amount of initial starvation octets that are passed to the framer interface upon arrival of the first cell needs to be set. On the other hand this number needs to be as small as possible to avoid excessive delay. The logical Reassembly Buffer size can be adjusted in order to detect too small cell distances by Reassembly Buffer overflow.

All parameters are defined in the “AAL Transmit Reference Slot” in RAM3. The amount of starvation octets given to the framer transmit interface after arrival of the first cell is defined by “starv_ini”. The contents of the starvation octets can be defined by “starv_bpslct” and the logical Reassembly Buffer size can be configured with “buff_lsize”.

The following sections give an overview on the Reassembly Buffer operation and initialization.

Unstructured Data Transfer:

After activation of a channel both SAR Receiver and Framer Transmit Interface start operation. As long as no reassembled cell is available in the Reassembly Buffer it is considered to be in underflow condition and starvation octets are passed to the Framer Transmit Interface.

As soon as the first reassembled cell is available in the Reassembly Buffer the device starts building up the Reassembly Buffer threshold level. This is done by passing an additional amount of starvation octets to the framer Transmit Interface

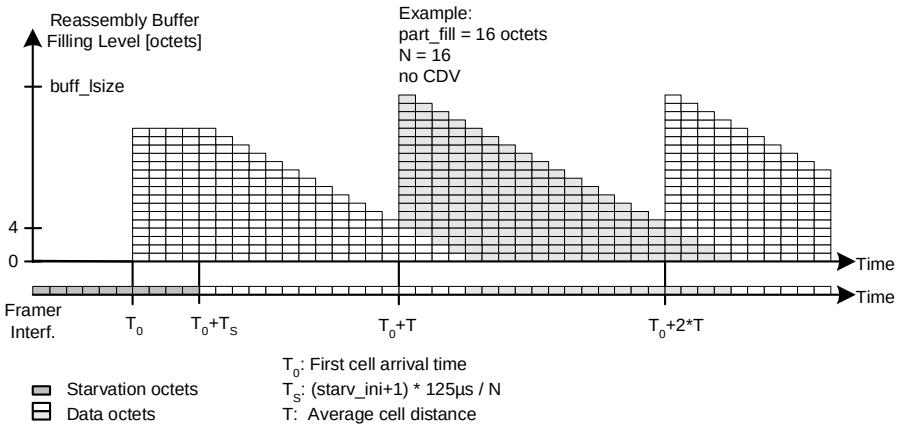


Figure 15 Reassembly Buffer Initialization: No CDV

As the transmission of the reassembled cell stream is delayed by “starv_ini”+1 octets, there will be “starv_ini”+1 octets of the previous cell left in the Reassembly Buffer if the following cell arrives without CDV.

If the maximum positive CDV is the same as the maximum negative CDV the expectation interval has a length of 2 x CDV. Assuming N octets of data are transmitted within one frame period of 125µs the amount of data transmitted in this interval is:

$$\Delta = 2 \times |\mathrm{CDV}| \times \frac{N}{125\mu s} \qquad [4]$$

The worst case for buffer underflow is given if the first cell has maximum positive CDV.

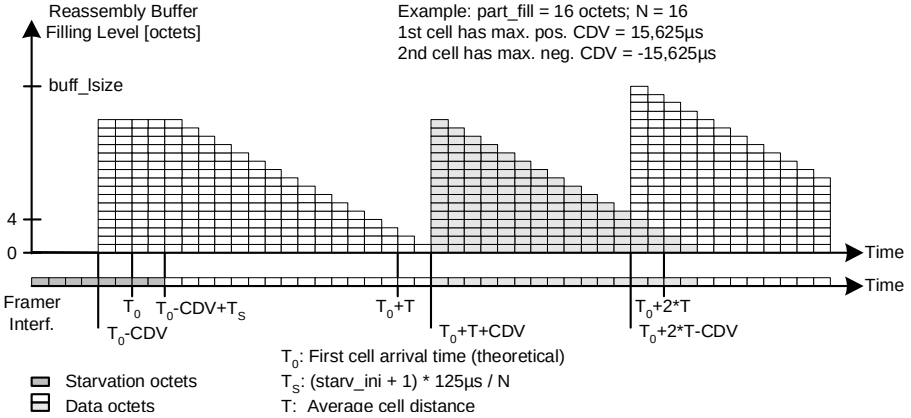


Figure 16 Reassembly Buffer Initialization: positive CDV at Start Up

In this case the amount of starvation octets inserted after receipt of the first cell has to be bigger than the amount of data transmitted during the expectation interval. Otherwise the Reassembly Buffer will enter underflow condition at any time a cell with maximum positive CDV is followed by a cell with maximum negative CDV.

$$\mathrm{starvini} \geq \Delta - 1 = 2 \times |\mathrm{CDV}| \times \frac{N}{125\mu s} - 1 \geq 0 \qquad [5]$$

The worst case for buffer overflow is given if the first cell has maximum negative CDV and then any cell with maximum negative CDV is followed by a cell with maximum positive CDV.

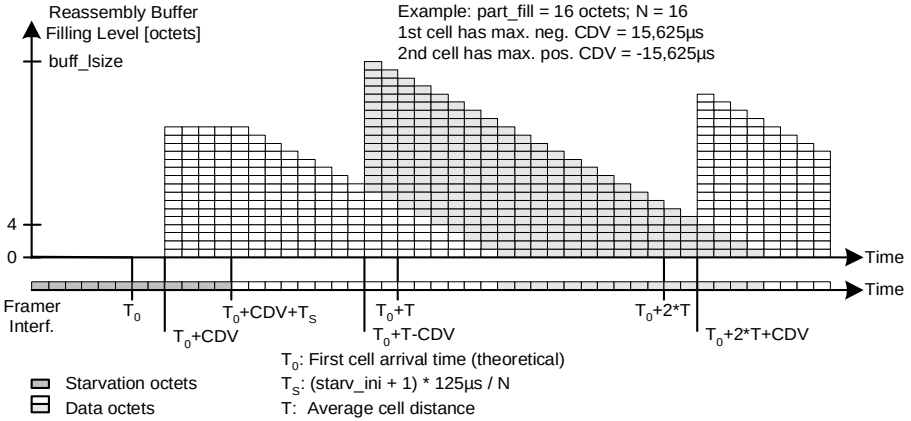


Figure 17 Reassembly Buffer Initialization: Negative CDV at Start Up

If the first cell has maximum negative CDV there will be “starv_ini” + 1 octets left in the Reassembly Buffer when the following cell arrives with maximum negative CDV. In case the following cell arrives with maximum positive CDV it will be “starv_ini” + 1 plus the amount of data to be transmitted in the expectation interval. Just after cell arrival the filling level of the Reassembly Buffer is at its maximum:

$$bufflsize \geq partfill + starvini + 1 + \Delta = partfill + 4 \times |CDV| \times \frac{N}{125\mu s} \quad [6]$$

The delay introduced by the Reassembly Buffer is:

$$delay = \frac{starvini \times 125\mu s}{N} \quad [7]$$

Structured Data Transfer:

After activation of a channel both SAR Receiver and Framer Transmit Interface start operation. As long as no reassembled cell in P format is accepted the Reassembly Buffer it is considered to be in underflow condition and starvation octets are passed to the Framer Transmit Interface.

After that, “starv_ini” + 1 starvation octets are given to the Framer Transmit Interface.

Then, the transmitter reads as many octets from the Reassembly Buffer as indicated by the pointer field. For each octet one starvation octet is given to the Framer Transmit Interface. The next octet to be read from the Reassembly Buffer is the “ATM Start of Structure” (The octet where the AAL1 pointer field points at).

After that, starvation octets are passed to the Framer Transmit Interface until the “Port Start of Structure” is detected. A “Port Start of Structure” occurs when the Framer

Transmit Interface requests the first time-slot octet belonging to the channel in the frame or the multiframe.

From that moment on, the “ATM Start of Structure” and “Port Start of Structure” are synchronous and the contents of the Reassembly Buffer are passed to the framer transmit interface.

The worst case for buffer underflow is given, if the first cell has maximum positive CDV, the contents of the pointer field is “0” and the “Port Start of Structure” occurs right after the transmission of “starv_ini” + 1 starvation octets.

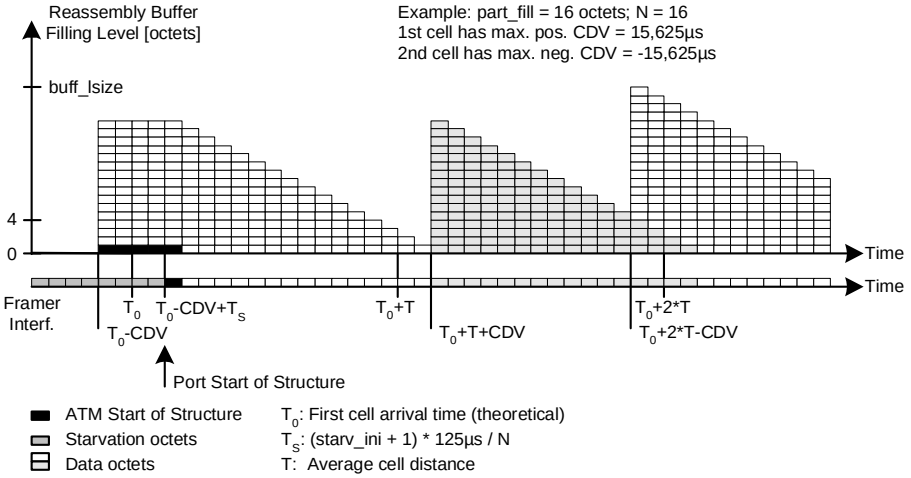


Figure 18 Reassembly Buffer Initialization for structured CES: positive CDV at Start Up

In this case the amount of starvation octets inserted after receipt of the first P format cell has to be bigger than the amount of data transmitted during the expectation interval as defined in (4). Otherwise the Reassembly Buffer will enter underflow condition at any time a cell with maximum positive CDV is followed by a cell with maximum negative CDV.

$$starvini \geq \Delta - 1 = \frac{2 \times CDV \times N}{125\mu s} - 1 \geq 0 \qquad [8]$$

The worst case for buffer overflow is given, if the first P format cell has maximum negative CDV, the contents of the pointer field is at its maximum value Pmax and the “Port Start of Structure” occurs right before the receipt of that P format cell. In that case the complete frame needs to be stored in the Reassembly Buffer

If the first cell has maximum negative CDV there will be “starv_ini” + 1 octets left in the Reassembly Buffer at any time a cell with maximum positive CDV is followed by a cell

with maximum negative CDV. the following cell arrives with maximum negative CDV. In case the following cell arrives with maximum positive CDV it will be “starv_ini” + 1 plus the amount of data to be transmitted in the expectation interval. Just after cell arrival the filling level of the Reassembly Buffer is at its maximum:

To allow CDV compensation and SDT structure synchronization, the logical size should be programmed to a minimum value given by:

$$\mathrm{bufflsize} \geq \mathrm{partfill} + \mathrm{starvini} + 1 + \Delta + \mathrm{FR} \times \mathrm{N} + \mathrm{Pmax} \quad [9]$$

$$\mathrm{bufflsize} \geq \mathrm{partfill} + 4 \times |\mathrm{CDV}| \times \frac{\mathrm{N}}{125\mu\mathrm{s}} + \mathrm{FR} \times \mathrm{N} + \mathrm{Pmax} \quad [10]$$

with FR being the number of frames in a structure:

FR = 0: when SDT is not used
FR = 1: for frame based SDT
FR = 16: for multi-frame based SDT in E1 mode
FR = 24: for multi-frame based SDT in T1 mode

Pmax is the maximum number of payload octets from the pointer field to the start of structure:

Pmax = N x FR, if N x FR < 2 x part_fill
Pmax = 2 x part_fill, if N x FR > 2 x part_fill

The logical Reassembly Buffer size is limited by its physical size. The relation is given by:

$$\mathrm{bufflsize} \leq 8 \times \mathrm{N} \times \mathrm{partfill} \times \mathrm{cellsperblock} - \mathrm{S} \times \mathrm{partfill} \quad [11]$$

where

S = 0: in case of Fast Sequence Count Algorithm
S = 1: in case of Robust Sequence Count Algorithm

When the robust SC algorithm is used, the decision on cell acceptance is delayed until the next cell is received. As the cell is temporarily stored in the Reassembly Buffer, there must always be space for that cell. Therefore, the physical size of the Reassembly Buffer must be at least the logical size plus one cell.

In the fast SC algorithm the intermediate storage of a cell is not required. The cell is stored immediately in the Reassembly Buffer, when accepted.

The delay introduced by the Reassembly Buffer is:

$$\frac{\mathrm{starvini} \times 125\mu\mathrm{s}}{\mathrm{N}} \geq \mathrm{delay} \leq \frac{(\mathrm{starvini} + \mathrm{FR} \times \mathrm{N} + \mathrm{Pmax}) \times 125\mu\mathrm{s}}{\mathrm{N}} \quad [12]$$

4.4.2.4 Re-Initialization of the Reassembly Buffer

For re-initialization of the Reassembly Buffer by the microprocessor, the processor has to set the “mcp_reinit” bit in the “AAL Transmit Reference Slot” in RAM2, wait for 1.5 frames and reset “mcp_reinit”.

4.5 Internal Clock Recovery Circuit (ICRC)

The Internal Clock Recovery Circuit (ICRC) may generate RTS values in upstream direction and a 8.192, 2.048 or 1.544 MHz transmit clock in downstream direction. Each port works independently using its own set of control registers and error counters. The Cell delay variation is assumed to be less than +/- 4 ms.

According to ITU-T 432.1 [33] SRTS clock recovery is only defined for unstructured CES. Therefore, ports supporting SRTS clock recovery have to be configured for only one channel in unstructured CES with completely filled ATM cells.

The ICRC supports two Framer Interface formats

- FALC Mode (FAM, see **Chapter 5.1.1**) with a transmit clock frequency of 8.192 MHz for both E1 and T1.
- Generic Interface Mode (GIM, see **Chapter 5.1.2**) with a transmit clock frequency of 2.048 MHz in case of E1 and 1.544 MHz in case of T1.

These modes can be selected via bits “om” in the Operation Mode Register (opmo, see **Chapter 7.24**) and bit “gim” in the Internal Clock Recovery Circuit Configuration Register (“icrcconf”, see **Chapter 7.46**).

Transmit clocks are generated by internal PLLs based on SRTS, ACM or both. The method of transmit clock generation is selected via bits "srt" and "acm" in the Configuration Register Downstream of Port N ("condN", see **Chapter 7.47**). Generation of RTS values is enabled via bit “rtsg” in the Configuration Register Upstream of Port N (“conuN”, see **Chapter 7.51**). If ACM is used, the corresponding RTS generator can be kept disabled.

For communication between the ICRC and the rest of the chip a frame based protocol is used. The internal interface as well as its protocol is the same as defined for the external clock recovery interface (see **Chapter 5.4**).

The ICRC contains the following sub blocks:

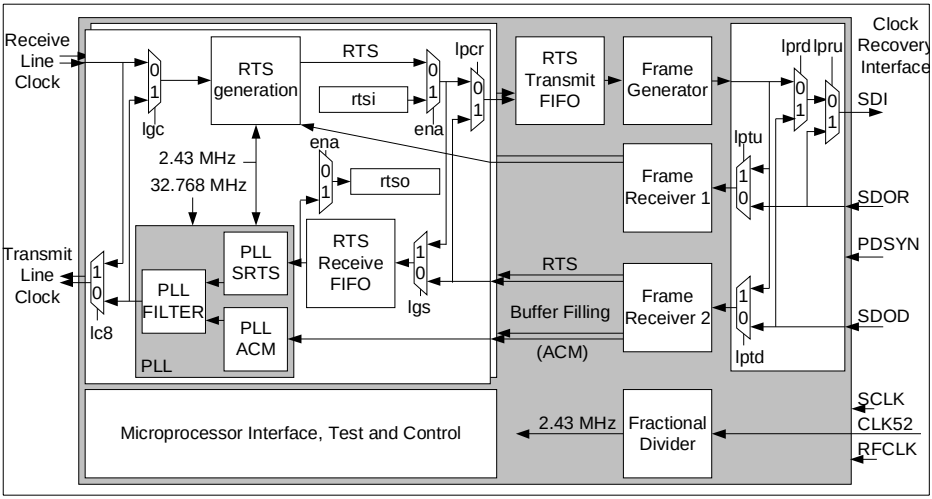


Figure 19 Block Diagram of the ICRC

4.5.1 Data Flow

In transmit direction the ICRC generates RTS values for each port independently and writes them into the RTS Transmit FIFO.

Received RTS values are written to the port specific RTS Receive FIFO to compensate cell delay variation. RTS values for each port are processed at a frequency equal to the SRTS period (8 cells). ACM values are processed immediately by the corresponding PLL.

4.5.2 Frame Generator

This block generates 32-bit control frames that are used for communication with the rest of the system.

For synchronization with the system the received synchronization signal PDSYN is used. However, if this signal can't be extracted from the received bit stream by the frame receiver, the frames are generated by means of an internal synchronization counter.

The frame output is put in tristate during power down of the internal interface. As soon as the internal synchronization counter is synchronized on PDSYN signal, the frame output is enabled.

4.5.3 Frame Receiver

This block is implemented twice. Once for SRTS and ACM data via port SDOD and once for the "reset SRTS logic" command via port SDOR.

The frame receiver is synchronized to the received synchronization signal PDSYN by means of an internal synchronization counter. In case no sync signal is received, frames are synchronized to the counter. The synchronization between PDSYN and the internal counter is checked each time PDSYN is received. A synchronization error is indicated via bit “scri” in the Interrupt Source Register (“irs”, see **Chapter 7.44**) at the start of a series of wrong synchronized frames. Synchronization errors are counted and the internal synchronization counter is synchronized on the new received synchronization pulse. An errored frame (parity error) is indicated via bit “per” in “irs” but processed as a normal frame.

In case the internal interface to the ICRC is switched off by the system, SCLK keeps working. The ICRC detects the following errors:

- Parity error: Because SDOD and SDOR are continuously high, the odd parity is violated.
- Synchronization error: Because PDSYN is continuously low, synchronization is not possible.

For ACM, the Reassembly Buffer filling level is measured in number of octets and passed to the ICRC each time a accepted cell is stored in the Reassembly Buffer.

The arrival time between 2 ACM data values is verified. The assumed maximum CDV is 4 ms. The maximum cell distance without CDV is 0.276 ms for T1 and 0.221 ms for E1. In case the next ACM data value is not arrived within 10 ms, an error indicated in register “atlN” is generated.

4.5.4 RTS Receive FIFO

This block is implemented for each port.

The RTS Receive FIFO compensates the Cell Delay Variation (CDV), the delay of the system interface with it's FIFO and the phase difference between reading and writing of the RTS Receive FIFO. Each RTS Receive FIFO provides space for 8 RTS values. After reaching the initial filling level of 5 RTS values, delay variations of +3 / -5 RTS values can be compensated. This corresponds to a maximum CDV of -4.4 / +7.3 ms (E1) or -5.8 / +9.7 ms (T1).

In case of overflow (register “sroN”) or underflow (register “sruN”) the PLL-SRTS is put in free running mode and the FIFO is restarted. These events are indicated in the SRTS Receive FIFO Underflow Register (sruN, see **Chapter 7.60**) and the SRTS Receive FIFO Overflow Register (sroN, see **Chapter 7.61**).

In case of SRTS the PLL start-up is delayed until 5 RTS values are received. This will take 7.3 ms for E1 and 9.7 ms for T1. During this time PLL-SRTS is free running (and bit “frr” of register “statN” is set).

If the PLL block does not use RTS values (bit “srt”=0 in register “condN”) or the port is in power down mode (bit “pwd”=1 in register “condN”) no data is written to this FIFO. In

case bit “ena” of register “tsinN” is set, a value from the SRTS Receive FIFO is read by reading register “tsout”.

In cases where the network clocks of RTS generator and RTS receiver have a frequency offset, the SRTS algorithm will generate a service frequency with the same frequency offset. The rate of RTS value generation and consumption depends on the service clocks. In this special case, the rate of RTS value consumption is different from the rate of RTS value generation. Enabling the ACM algorithm will not help as the FIFO is read by the clock generated by PLL-SRTS. As a result the SRTS Receive FIFO will generate regular (every 20 minutes) under- or overflows.

4.5.5 RTS Transmit FIFO

Each RTS generator stores the RTS value and its port number in the RTS Transmit FIFO. When the frame generator starts generating a new frame, it reads from the FIFO the source address and the next RTS value.

4.5.6 ICRC Loopback Modes

Loopbacks are available for each port and for the system interface of the circuit.

Each port has 2 loopbacks. The first, situated near the framer, performs a loopback on the clock signals. It is controlled by the bit “lgc” in the Configuration Register Downstream Direction of Port N (condN, see **Chapter 7.47**), which sends the generated clock back to the RTS generator, and “lc8” in “condN”, which sends the received clock back to the framer interface. The second has the same internal structure. It allows to send received RTS values of all ports back to the RTS Transmit FIFO (“lpcr”=1 in register “condN”). Thus, this loop has a variable delay with a guaranteed maximum of RTS Transmit FIFO depth x Frame-period. If “lgs”=1 in register “condN”, generated RTS values are sent via the receive FIFO to the PLL.

Another loopback block is situated at the clock recovery interface. It is controlled by the bits “lptd”, “lptu”, “lprd” and “lpru” in the ICRC configuration register “icrcconf”. Not all loop back possibilities of this block carry useful data, but the parity can always be tested.

4.5.7 RTS Injection

In case bit “ena” of the Test Input of Port N register (tsinN, see **Chapter 7.50**) is set, the RTS Transmit FIFO receives a new RTS value from field “rtsi” of “tsinN” at the moment the microprocessor writes data to that register. RTS values coming from the RTS generator of port N are ignored in this case. RTS values coming from the clock recovery interface and which have to be returned because of loopback “lpcr”, have priority over register “tsinN”.

During this test, the clock recovery or, in case of loopback, the receive FIFO receives the RTS values written in field rtsi. It is advisable to power down the circuit(s) which do not

work properly with these RTS values via bit “pwd” of “condN”. If “srt” in “condN” is reset, the output of the RTS Receive FIFO is not used by PLL-SRTS.

4.5.8 Fractional Divider

The fractional divider generates a 2.43 MHz clock from the 51.84 MHz clock provided via the CLK52 pin. This is done by selecting 3 out of 64 clock pulses of 51.84 MHz. The resulting 2.43 MHz clock contains jitter components of 810 kHz and above, with a maximum peak to peak jitter of 19 ns.

4.5.9 Clocks

For an overview on the required clocks for the ICRC please refer to **Chapter 8.1**.

4.5.10 Power Management

Different Power down modes are available for the ICRC:

- for each port via bit “pwd” in “condN”
- for the Clock Recovery Interface via bit “pdcri” in “icrcconf”.
- for the complete ICRC by means of the “a_icrc_dwn” bit in the “acfg”. This feature reduces the power consumption by approximately 50 mW. Once the ICRC is switched off, it can only be enabled by hardware reset of the whole device.

4.5.11 PLL Block

This block is implemented for each port. It consists of 3 PLLs: PLL-SRTS, PLL-ACM and PLL-FILTER.

The bits “srt” and “acm” in the register “condN” define, which PLL is connected to PLL-FILTER and used for clock recovery. Each PLL may be used exclusively or in combination.

4.5.11.1 PLL-SRTS:

PLL-SRTS is used for clock recovery using the SRTS method. It has a cut-off frequency of 20 to 50 Hz.

The phase detector of PLL-SRTS has a linear range which optimized for jitter tolerance requirements. It is defined by a “window” of accepted RTS values. Each time PLL-SRTS detects values, which fall out of the window, or processes invalid values, it is forced in hold over for 1 SRTS period, bit “hov” of register “statN” is set and the SRTS Invalid Value Processed Counter (“sriN”, see **Chapter 7.63**) is incremented. In case the number of out of window conditions during 16 SRTS periods exceeds the value given by field “tr_srts” of register “treshN”, an out of lock message, indicated with bit “ols” of register “oolN” is generated. During start-up of the RTS Receive FIFO, PLL-SRTS is free running and bit “frr” of register “statN” is set.

4.5.11.2 PLL-FILTER

The PLL “PLL-FILTER” has a very low cut off frequency and a tuning range of ±240 ppm. It reduces jitter which is generated in, or passed through PLL-SRTS. Although PLL-FILTER is placed behind PLL-ACM, it has little or no functionality in case of ACM, as PLL-ACM has a lower cut off frequency.

If more out of lock detections during 16 SRTS periods are detected than defined with “tr_filt” in “tresh”, an out of lock message, indicated by bit “olf” of register “oolN”, is generated.

4.5.11.3 PLL-ACM

The PLL-ACM is a control system with feedback of 2nd order. Its phase is adjusted according to the filling level of the Reassembly Buffer.

The average buffer filling level as defined in bits “avb” in the Average Buffer Filling Register (“avbN”, see **Chapter 7.52**) is subtracted from the current buffer filling level. The result is amplified in order to adjust the cut off frequency and to define the system’s damping (number of bytes, needed to drive the DCO over its tuning range. The loop gain is programmed in the ACM Shift Factor Register (asfN, see **Chapter 7.53**). Although adjustable, the PLL-cut-off frequency is generally less than 1 Hz. In conjunction with a low pass filter, CDV is very small.

The behavior of the PLL is characterized by rise time and lock in time. The rise time is the time when the clock output enters the predefined tuning range for the first time. The lock in time is defined as the time after which the clock stays within the accepted deviation.

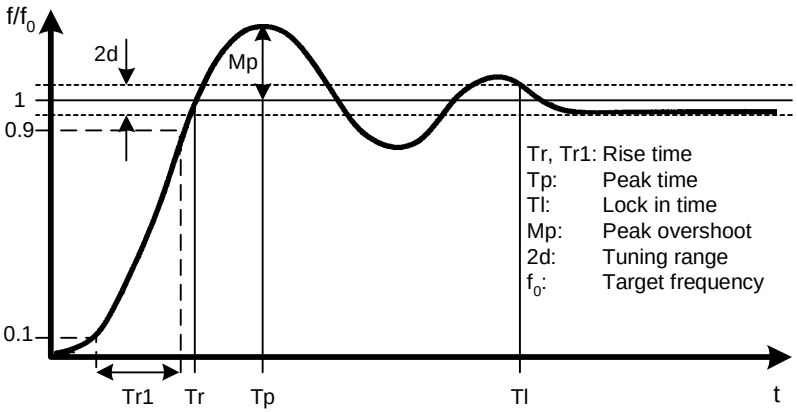


Figure 20 Transient Parameters

The tuning range of the DCO is limited to the value programmed to bits “tur” in register “condN”. If the phase detector requests a higher frequency deviation the DCO enters out-of-range condition. In this case the DCO’s output will be clipped and bit “max” of register “statN” will be set. If the number of out-of-range conditions during 16 ATM cells exceeds the value given by field “tr_acm” of register “treshN”, an out-of-lock message, indicated via field “ola” of register “oolN”, is generated.

Increasing the loop-gain reduces the damping of the PLL-ACM. This will reduce the rise time but results in overshoot and long lock-in times.

Reducing the loop-gain increases the damping. This results in lower cut off frequencies, and prevents overshoot. Thus, CDV is less likely to drive the PLL out of lock. The rise and lock-in time are increased. If the loop-gain is too low, the amount of bytes required to drive the DCO over it's tuning range could cause a data buffer over- or underflow.

Optimized damping allows minimum lock-in time without overshoot. In this case PLL-ACM’s frequency is moving asymptotically to the correct value.

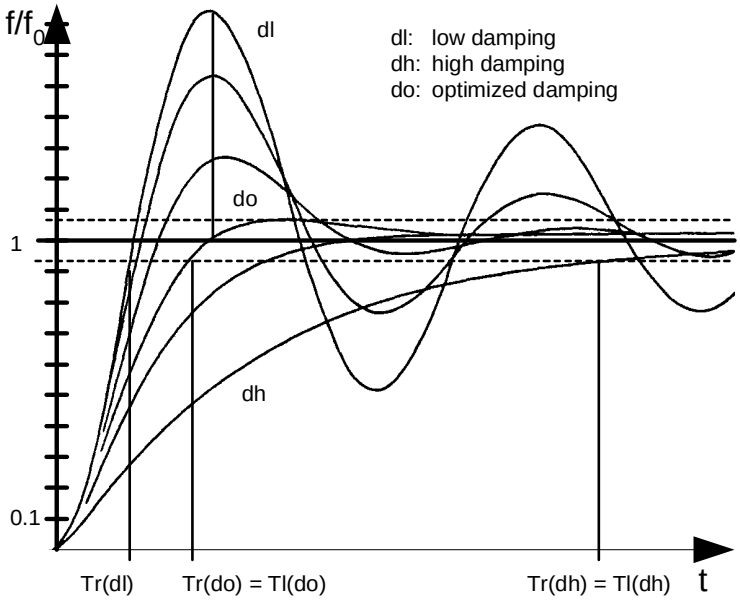


Figure 21 Influence of Damping on Lock in Time

PLL-ACM tries to keep the number of bytes in the Reassembly Buffer at the average buffer filling value programmed to register “avbN”. This value should be equivalent to the number of bytes stored in the Reassembly Buffer during start-up, as defined by the value programmed in the “starv_ini” field of the “AAL Transmit Reference Slot” in RAM3.

During start-up and restart, PLL-ACM will be free running for 8 x tiniN[tini] x T_{Data} as programmed in the Time of Initial Free Run Register (“tiniN”, see **Chapter 7.54**). During this time the data buffer is filled with an initial number of bytes. As tiniN[tini] is 2 bit longer than “stav_ini” in the AAL Transmit Reference Slot of RAM3 it is possible to choose a longer-than-necessary initialization time, to compensate start-up time differences.

After the initial free run, PLL-ACM will start locking in. The lock in time depends on:

- The difference between the initial number of bytes in the data buffer (see “starv_ini” of the “AAL Transmit Reference Slot” in RAM3) and the value programmed in register “avbN”.
- The damping, which is influenced by register “asfN”.
- The maximum allowed frequency deviation given by “tur” of register “condN”.
- The required frequency deviation.

During this lock-in process, the output frequency might temporarily reach the programmed minimum or maximum value. This strongly depends on the initial difference of the data buffer filling from the value given by “avbN”.

As re-initialization of the data buffer is not reported to the ICRC, PLL-ACM will detect a huge difference between data buffer filling and the value given by “avbN”. As a result the output frequency will be driven to it's lowest allowed value and stays there for a relative long period of time. For this reason it is important to program the field “tur” in register “condN” with the smallest possible value.

4.5.11.4 SRTS with ACM:

The combination of SRTS and ACM is used when the derived network clock of the SRTS generator differs from the derived network clock of the SRTS receiver. The maximum difference is relatively small (+/-4.6 ppm) and should be compensated by ACM. In this case the shifting of the difference between ACM data and register “avbN”, as programmed in register “asfN”, has to be reduced. Stable operation of PLL-ACM in parallel with PLL-SRTS can not be guaranteed if the shifting is not reduced. The cut off frequency of PLL-ACM has to be much lower than the cut off frequency of PLL-SRTS, as these PLLs are working in parallel in this case. This will also reduce the effects of CDV, because the cut off frequency of PLL-ACM is reduced. The tuning range (register “condN”, field “tur”) can not be reduced as PLL-ACM has to compensate jitter which is generated by or passed through PLL-SRTS.

4.6 Internal Queues

4.6.1 Event Queue

All the functional blocks that process octets or cells can generate counter events, i.e. commands to increment a particular counter in the external RAM. All counter events are written in a FIFO queue that can store 256 counter events.

A counter event contains the statistics counter address in external RAM and an increment value.

4.6.2 Output Queue

When a cell is completely stored in the ATM Receive or Segmentation Buffer, it is ready to be transmitted to the ATM layer over the UTOPIA receive interface. The external RAM address of the cell is stored in a common Output Queue (OQ).

The Output Queue is a First In First Out (FIFO) queue with a maximum of 256 cell address entries. It is common to ATM and AAL mode ports.

As long as the Output Queue is not empty, the Cell Receive processing (CR) will write the corresponding cell from external RAM to the UTOPIA Receive interface (UR).

4.6.3 Interrupt Queue

The Interrupt Queue in external RAM is handled as a FIFO which is written whenever a counter reaches its threshold value.

When there are interrupts in the Interrupt Queue, the “iq_ne” bit in the interrupt status register 1 “isr1” will be set to 1. When the corresponding bit is not masked in the “imr1” register an interrupt will be generated on the $\overline{\text{MPIR1}}$ pin.

The microprocessor should react on the interrupt by reading the Interrupt Queue. When “oam_act” is set to 1, the MPADR(12:1) address bits are don’t care. The next Interrupt Queue entry will automatically be provided.

Each Interrupt Queue entry identifies a particular OAM counter that has reached its threshold value. The counter is identified by its “port_nr”, “channel_nr” and “counter_nr”. When the microprocessor reads the counter value and the “dest_read” bit of the register oamc is set to 1, the counter is automatically reset.

Each Interrupt Queue entry also indicates whether there are still more interrupts in the queue in the “iq_ne” field of the interrupt status register “isr1”. This allows the software to read the Interrupt Queue until it is empty without having to read the interrupt status register “isr1” again.

When the statistics function is disabled (oamc[oam_act] = 0), the µP can read and write all addresses of the Interrupt Queue.

4.7 OAM Processing

The OAM processing block (OM) will read Statistics Counter events from the Event Queue as long as the Event Queue is not empty. The OM will read the Statistics Counter value “count_value” and the Statistics Counter threshold from external RAM. If the Statistics Counter is not yet at its maximum value 4000 0000_H, the value is increased with the increment value given by the counter event. If the Statistics Counter threshold is active (“thres_act” = 1) and the Statistics Counter equals or exceeds the threshold value “thres_value”, the OM block will write an interrupt entry in the Interrupt Queue in external RAM. The new Statistics Counter value with indication whether an interrupt was generated in the “int_gen” field will finally be written into external RAM.

The “dest_read” bit determines whether a read operation from the microprocessor in the Statistics Counter address space in external RAM causes a reset of the Statistics Counter value.

The OM block can be disabled via bit “oam_act” in the OAM control register (“oamc”, see **Chapter 7.3**).

In normal operation, counter event processing should be activated (oam_act = 1). In this case the microprocessor can only read indirectly in the Interrupt Queue.

For RAM test and initialization, the “oam_act” should be set to 0. In this mode, the microprocessor can write and read the complete external RAM.

The use of the Statistics Counter thresholds allows the software to reduce the number of generated interrupts and to decide at what error level an interrupt should be generated.

When the software wants to use polling mode, the thresholds can be made inactive, and no interrupts will be generated. The software will read all the Statistics Counters on regular time intervals in this mode.

A combination of both methods is also possible, all the Statistics Counters are read and reset on regular time intervals. However thresholds can be used as an extra guard: a Statistics Counter that reaches an exceptionally high value will cause an interrupt.

For a detailed list of all implemented Statistics Counters refer to **Chapter 6.2.1**. For information how to translate Statistics Counters into the ATM Forum CES MIB as defined in [10] refer to **Chapter 8.2**.

4.8 Loopback Modes

4.8.1 Upstream Loop

The Upstream Loop block (UL) allows cells that are received at the Framer Interface and forwarded to the UTOPIA Receive Interface to be send back via the UTOPIA Transmit Interface to the Transmitter Interface. The UL block contains a buffer of 4 ATM cells.

To activate the Upstream Loop, the “p_ulp” bit in the Port Configuration Register (pcfN, see **Chapter 7.1**) must be set to 1.

When a cell is available in the UL buffer, the UTOPIA transmit interface will de-assert the TXCLAV signal, to prevent the ATM layer component from sending cells during the processing of the loopback cell.

For ATM mode ports, all cells are looped regardless of their header. The loop is always transparent allowing looped cells to be visible on the UTOPIA receive interface.

For AAL mode ports, it is possible to make a single channel loop using a VCI filter. When the “vci_flt_ulp” bit in the Loopback Control Register (lpbc, see **Chapter 7.11**) is set to 0 all cells are looped. When the bit is set to 1, only those cells with the 5 LSB bits of the VCI matching the “vci_val_ulp” field of the “lpbc” register will be looped. Loopback can be switched from transparent to non-transparent by setting the “tulp” bit in the “lpbc” register. If the loopback is non-transparent, looped cells are not visible on the UTOPIA receive interface.

4.8.2 Downstream Loop

It is possible to loop ATM cells that are coming in on the UTOPIA transmit interface to the UTOPIA receive interface through the Downstream Loop (DL) block. The DL block contains a buffer of 4 ATM cells.

When a cell is available in the DL buffer and in the Output Queue, the UTOPIA receive interface will transmit cells from both buffers with alternating priority.

To activate the downstream UTOPIA loop, the “p_dlp” bit in the Port Configuration Register (pcfN, see **Chapter 7.1**) must be set to 1.

When the downstream UTOPIA loopback is active for at least one port, the UTOPIA transmit interface will only assert the RxCLAV signal to 1 when a free space of one ATM cell is available in both the DL buffer and the UT input buffer.

The loopback can be made transparent or non-transparent by setting the “tdlp” bit in the Loopback Control Register (lpbc, see **Chapter 7.11**). If the loopback is made non-transparent, the looped cells are not transferred to the “Cell Transmit Processing” block CT.

4.8.3 Serial Loop

The framer transmit clock, data, framesync and multi-framesync signals can be looped from the Framer Transmit Interface to the Framer Receive Interface per port. This feature can be enabled by setting the “p_slp” bit in the Port Configuration Register (pcfN, see **Chapter 7.1**).

The loopback can be made transparent or non-transparent by setting the “tslp” bit in the Loopback Control Register (lpbc, **Chapter 7.11**). If the loopback is made transparent, all transmitted data is also visible on FTDAT. Otherwise, if non-transparent, all 1s are transmitted on FTDAT.

4.9 Cell Insertion

This block allows the insertion of predefined cells stored in the Cell Insertion Buffer into the UTOPIA receive cell stream.

The Cell Insertion Buffer, located in external RAM, offers space for one ATM cell. The ATM cell except of the UDF octet needs to be written to the Cell Insertion Buffer via the Microprocessor interface. When transferring the cell to the UTOPIA receive interface an UDF of 00_H will be inserted.

Cell insertion is activated by setting the bit “insert_cell” in the Command Register (“cmd”, see **Chapter 7.31**) the cell is then read from the Cell Insertion Buffer and forwarded to the UTOPIA Receive Interface.

The port number is generated randomly. Depending on the UTOPIA mode selection, it will be mapped either on the UTOPIA address bus or in the ATM header (“mapping_mode” = 2, 3, 4 or 5 in register “utconf”) overwriting the predefined values.

4.10 Cell Extraction

Cells coming in downstream direction from the UTOPIA Transmit Interface can be extracted to the Cell Extraction Buffer instead of the Reassembly/ATM Transmit Buffer.

The Cell Extraction Buffer offers space for 254 ATM cells. It is located in the external RAM.

Incoming cells are written to the Extraction Buffer if

- their VCI matches to a pattern predefined in the Cell Filter VCI Pattern 1 Register (cfvp1, see **Chapter 7.26**) where each bit of the VCI can be masked via the Cell Filter VCI Mask Register 1 (cfvm1, **Chapter 7.27**)
- or their VCI matches to a pattern predefined in the Cell Filter VCI Pattern 2 Register (cfvp2, see **Chapter 7.28**) where each bit of the VCI can be masked via the Cell Filter VCI Mask Register 1 (cfvm1, **Chapter 7.29**)
- or their PTI matches to one of two pattern defined in the Cell Filter Payload Type Register (“cfpt”, see **Chapter 7.30**) each of these patterns can also be masked via “cfpt”.

Once a cell has been extracted to the cell Extraction Buffer, it is indicated by the bit “cf_fifo_n_empty” in the Extended Interrupt Status Register (“eis1”, see **Chapter 7.19**).

Cells can be read with the help of the read pointer (“rdptr”) in the Cell Filter Read Pointer Register (“cfrp”, **Chapter 7.32**). The rdptr can have values between 02_H and FF_H. This value is a pointer to the current base-address, at which the microprocessor can read the next extracted cell from the Extraction Buffer.

$$MPADR = 26000_H + 20_H \cdot rdptr \quad [13]$$

$$RMADR = 03000_H + 10_H \cdot rdptr \quad [14]$$

After reading the cell the rdptr has to be incremented by the microprocessor and written back. If the rdptr is incremented to its maximum value FF_H the value 02_H has to be written back instead.

4.11 Mapping of Channels to Timeslots

The two LSB bits of a slot entry identify the slot type:

Table 21 Coding of Slot Type in internal configuration RAMs

Slot Type	Bit 1	Bit 0
ATM/AAL Idle	0	0
ATM/AAL Continuation	1	0
ATM/AAL Reference	X	1

4.11.1 ATM Mode

The IWE8 supports any mapping scheme of ATM cells into N of the 32 timeslots of the framer interfaces.

The mapping scheme is defined by programming 32 slot positions in the internal RAMs. RAM1 is used for receive port configuration and RAM2 for transmit port configuration.

- For each configuration exactly one timeslot should be programmed as the “ATM Reference Slot”.
- Depending on the Link data rate 29 (E1) or 23 (T1) timeslots should be programmed as “ATM Continuation Slots”.
- The remaining unused slots should be programmed as “AAL Idle Slots”.

For mapping of ATM cells in T1/E1 frames according to ITU-T G.804 [26] the internal RAM slot positions should be programmed as shown in **Table 22**.

Table 22 RAM slot positions for ITU-T G.804 compliant ATM mapping

RAM	E1		T1 in FAM		T1 in GIM	
Slot	Slot	RAM Slot Type	Slot	RAM Slot Type	Slot	RAM Slot Type
0	0	ATM Idle		ATM Idle	1	ATM Continuation
1	1	ATM Reference	1	ATM Reference	2	ATM Reference
2	2	ATM Continuation	2	ATM Continuation	3	ATM Continuation
3	3	ATM Continuation	3	ATM Continuation	4	ATM Continuation
4	4	ATM Continuation		ATM Idle	5	ATM Continuation
5	5	ATM Continuation	4	ATM Continuation	6	ATM Continuation
6	6	ATM Continuation	5	ATM Continuation	7	ATM Continuation
7	7	ATM Continuation	6	ATM Continuation	8	ATM Continuation
8	8	ATM Continuation		ATM Idle	9	ATM Continuation
9	9	ATM Continuation	7	ATM Continuation	10	ATM Continuation

Table 22 RAM slot positions for ITU-T G.804 compliant ATM mapping

RAM	E1		T1 in FAM		T1 in GIM	
Slot	Slot	RAM Slot Type	Slot	RAM Slot Type	Slot	RAM Slot Type
10	10	ATM Continuation	8	ATM Continuation	11	ATM Continuation
11	11	ATM Continuation	9	ATM Continuation	12	ATM Continuation
12	12	ATM Continuation		ATM Idle	13	ATM Continuation
13	13	ATM Continuation	10	ATM Continuation	14	ATM Continuation
14	14	ATM Continuation	11	ATM Continuation	15	ATM Continuation
15	15	ATM Continuation	12	ATM Continuation	16	ATM Continuation
16	16	ATM Idle		ATM Idle	17	ATM Continuation
17	17	ATM Continuation	13	ATM Continuation	18	ATM Continuation
18	18	ATM Continuation	14	ATM Continuation	19	ATM Continuation
19	19	ATM Continuation	15	ATM Continuation	20	ATM Continuation
20	20	ATM Continuation		ATM Idle	21	ATM Continuation
21	21	ATM Continuation	16	ATM Continuation	22	ATM Continuation
22	22	ATM Continuation	17	ATM Continuation	23	ATM Continuation
23	23	ATM Continuation	18	ATM Continuation	24	ATM Continuation
24	24	ATM Continuation		ATM Idle		ATM Idle
25	25	ATM Continuation	19	ATM Continuation		ATM Idle
26	26	ATM Continuation	20	ATM Continuation		ATM Idle
27	27	ATM Continuation	21	ATM Continuation		ATM Idle
28	28	ATM Continuation		ATM Idle		ATM Idle
29	29	ATM Continuation	22	ATM Continuation		ATM Idle
30	30	ATM Continuation	23	ATM Continuation		ATM Idle
31	31	ATM Continuation	24	ATM Continuation		ATM Idle

However, it is possible to define other ATM cell mappings, e.g. ATM cells in less than 32 64 kbit/s channels. However, RAM slot 1 has always to be defined as Reference Slot.

4.11.2 AAL Mode

4.11.2.1 Unstructured CES

For unstructured CES according to ATM-Forums CES Specification [10] there is only one channel per port. Therefore, the internal configuration RAMs 1 to 3 have only to be

programmed with one Reference Slot at RAM slot 0. This slot number is used to identify the channel (“channel_nr” = 0).

4.11.2.2 Structured CES

For AAL ports with structured CES (Nx64 kbit/s) service, the timeslots are grouped into channels containing N of 32 timeslots. The mapping of the N x 64 kbit/s channels into an T1/E1 frame is done by programming the 32 positions of the internal configuration RAMs (RAM1 for receive ports, RAM2 and RAM3 for transmit ports).

It is possible to define more than one channel of N timeslots within one frame. In this case each channel has its own reference slot, followed by N-1 continuation slots. Additional unused frame slots that do not belong to any channel should be programmed as “AAL Idle Slot”.

The timeslot in the group of N timeslots with the lowest frame slot number is called the reference slot. The corresponding frame slot position in the internal RAM should be programmed as an “AAL Reference Slot”. The slot number of the AAL Reference Slot is used to identify the channel (“channel_nr”).

The other frame slot positions of the channel should be programmed as “AAL Continuation Slots”. The reference slot number, as defined by the “ref_slot_nr” field entry, is used to identify the channel the continuation slot belongs to. The N timeslots of a channel do not need to have consecutive frame slot numbers. They can be deliberately chosen out of the 32 frame slots.

Table 23 AAL Idle slot positions for structured CES in AAL mode

Slot number	E1	T1 in FAM	T1 in GIM
0	AAL Idle	AAL Idle	AAL Ref./Cont./Idle
1	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
2	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
3	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
4	AAL Ref./Cont./Idle	AAL Idle	AAL Ref./Cont./Idle
5	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
6	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
7	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
8	AAL Ref./Cont./Idle	AAL Idle	AAL Ref./Cont./Idle
9	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
10	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
11	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
12	AAL Ref./Cont./Idle	AAL Idle	AAL Ref./Cont./Idle

Table 23 AAL Idle slot positions for structured CES in AAL mode

Slot number	E1	T1 in FAM	T1 in GIM
13	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
14	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
15	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
16	AAL Idle	AAL Idle	AAL Ref./Cont./Idle
17	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
18	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
19	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
20	AAL Ref./Cont./Idle	AAL Idle	AAL Ref./Cont./Idle
21	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
22	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
23	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
24	AAL Ref./Cont./Idle	AAL Idle	AAL Idle
25	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Idle
26	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Idle
27	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Idle
28	AAL Ref./Cont./Idle	AAL Idle	AAL Idle
29	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Idle
30	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Idle
31	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Idle

The channel mapping can be dynamically reconfigured without disturbing other active channels of the same port.

Note: If frame based SDT without CAS is used and filling level ≤ 45, the condition band_width ≤ part_fill has to be fulfilled for correct operation.
Multiframe based SDT without CAS should not be used.

4.11.2.3 Structured CES with CAS

If a port is used for structured CES with CAS, additional signalling is inserted into the channel overhead. The associated RAM slots, 0 in T1 mode and RAM slots 0 and 16 in E1 mode, need to be configured as reference slots with “sdt_mfs” = 1.

Please note, that all settings of the AAL Reference Slot refer to the channel payload. Therefore, in case of T1 mode in FAM or E1 mode the channel has to be set to inactive (“channel_mode” = 0) with no bandwidth assigned (“band_width” = 0).

In T1 mode in GIM things are different. RAM slot 0 may also be used for user data, with “channel_mode” and “band_width” set according to the requirements of the user data carried via that slot.

Table 24 AAL Idle slot positions for structured CES with CAS in AAL mode

Slot number	E1	T1 in FAM	T1 in GIM
0	AAL Reference “channel_mode” = 0 “band_width” = 0 “sdt_mfs” = 1	AAL Reference “channel_mode” = 0 “band_width” = 0 “sdt_mfs” = 1	AAL Reference “sdt_mfs” = 1
1	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
2	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
3	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
4	AAL Ref./Cont./Idle	AAL Idle	AAL Ref./Cont./Idle
5	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
6	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
7	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
8	AAL Ref./Cont./Idle	AAL Idle	AAL Ref./Cont./Idle
9	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
10	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
11	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
12	AAL Ref./Cont./Idle	AAL Idle	AAL Ref./Cont./Idle
13	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
14	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
15	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
16	AAL Reference “channel_mode” = 0 “band_width” = 0	AAL Idle	AAL Ref./Cont./Idle
17	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
18	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
19	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
20	AAL Ref./Cont./Idle	AAL Idle	AAL Ref./Cont./Idle
21	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
22	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle

Table 24 AAL Idle slot positions for structured CES with CAS in AAL mode

Slot number	E1	T1 in FAM	T1 in GIM
23	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle
24	AAL Ref./Cont./Idle	AAL Idle	AAL Idle
25	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Idle
26	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Idle
27	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Idle
28	AAL Ref./Cont./Idle	AAL Idle	AAL Idle
29	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Idle
30	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Idle
31	AAL Ref./Cont./Idle	AAL Ref./Cont./Idle	AAL Idle

5 Interface Description

5.1 Generic Framer Interface

The selection of the Echo Canceller mode is done via an external pin (Pin $\overline{EC}$ = 0).

In standard mode (Pin $\overline{EC}$ = 1), 4 sub modes can be selected via the “om” bits in the Operation Mode Register (“opmo”, see **Chapter 7.24**)

- FALC mode (FAM)
- Generic Interface mode (GIM)
- Synchronous mode with an external reference clock of 8 MHz (SYM8)
- Synchronous mode with an external reference clock of 2 MHz (SYM2)

Depending on the level of the E1/$\overline{T1}$ pin FAM and GIM can run based on E1 or T1 frames. SYM2 and SYM8 will always use E1 frame formats.

A clock selector for the Framer transmit clock is integrated in the IWE8. Depending on bits “ftckn” in the FT Clock Select Register (“ftcs”, see **Chapter 7.25**) selection between the following clocks is done:

- the line clock FRCLK
- the SRTS regenerated clock from internal or external clock recovery circuit
- the clock derived from the external reference clock (pin RFCLK).

The data on the Generic Framer Interface is structured in frames repeated every 125µs. Each frame is divided into timeslots, where the least sigificant slot is transmitted first. The data bits in each slot are transmitted starting with the most significant bit.

5.1.1 FALC Mode (FAM)

The IWE8 can be directly connected to Infineon’s “Framer and Line interface components” (FALC) as shown in **Figure 22**.

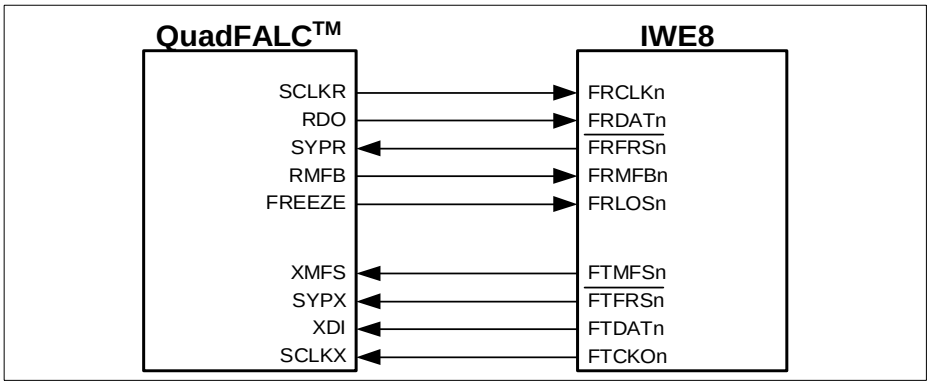


Figure 22 Connection of IWE8 to QuadFALC

The data is transferred between the FALC and the IWE8 via a system internal highway.

FRCLK[7:0] Framer Receive Clock
Receive system clock of 8.192 MHz (falling)

FRDAT[7:0] Framer Receive Data
FRDAT is sampled in the middle of the bit period on the falling edge of FRCLK

FRMFB[7:0] Framer Receive Multiframe Begin
Depending on bits “p_ces” in “pcfN”:

0 = Structured CES: A pulse on this pin designates the first frame of a new multiframe

1 = Unstructured CES: Unused

FRMFB is always sampled with the falling edge of FRCLK. If the framing is incorrect, the IWE8 stays in hunt mode.

$\overline{\text{FRFRS}}$[7:0] $\overline{\text{Framer}}$ Receive Frame Synchronization Pulse
$\overline{\text{FRFRS}}$ is generated at the beginning of timslot 1 of each frame

FRLOS[7:0] Framer Receive Loss of Signalling

FTCKO[7:0] Framer Transmit Clock
depending on bits ftckn in ftcs:

00 = depending on bit “rts_eval” in “opmo”:
0 = Transmit clock input with 8.192 MHz (falling)
1 = Clock of ICRC is used as transmit clock and is also switched to FTCKO pins (FTCKO is output pin)

01 = FRCLK (“rts_eval” = 1)

10 = Clock derived from RFCLK(“rts_eval” = 1)

11 = No clock (“rts_eval” = 1)

FTDAT[7:0] Framer Transmit Data
FTDAT is clocked with the falling edge of FTCKO:

FTMFS[7:0] Framer Transmit Multiframe Synchronization
Depending on bit p_ces in pcfN:

	0 =	Structured CES: Depending on “p_tx_mfs” in “pcfN”: 0 = Double frame mode: FTMFS is asserted every 2 frames (250 µs) 1 = E1 CRC multiframe mode: FTMFS is asserted every 16 frames (2 ms) T1 mode: every 3 ms T1 superframe mode: every 1.5 ms
	1 =	Unstructured CES: Unused, constant low level
$\overline{\text{FTFRS}}[7:0]$	Framer Transmit Frame Synchronization Pulse $\overline{\text{FTFRS}}$ is generated at the beginning of timslot 1 of every frame	
RFCLK	Reference Clock • Reference clock for the internal clock recovery circuit • Depending on p_rx_em in pcfN: Optional emergency clock if no transition on FRCLK is detected within 23 CLOCK cycles. The segmentation continues using the RFCLK divided by four, and using the byte-pattern programmed to a_emg_bpslct in acfg for the cell payload.	

The receive system clock and transmit system clock are both 8.192 MHz, and may be independent from each other. The data rate is 2048 Mbit/s. This means that each bit lasts for 4 clock cycles.

Data on the system internal highway is structured in frames of 256 bits every 125 µs. It is transmitted in 32 slots numbered from 0 to 31 with slot 0 transmitted first. The data bits of a slot are numbered from 1 to 8. The first transmitted bit ‘bit 1’ is the most significant bit. **Figure 23** shows the bit ordering.

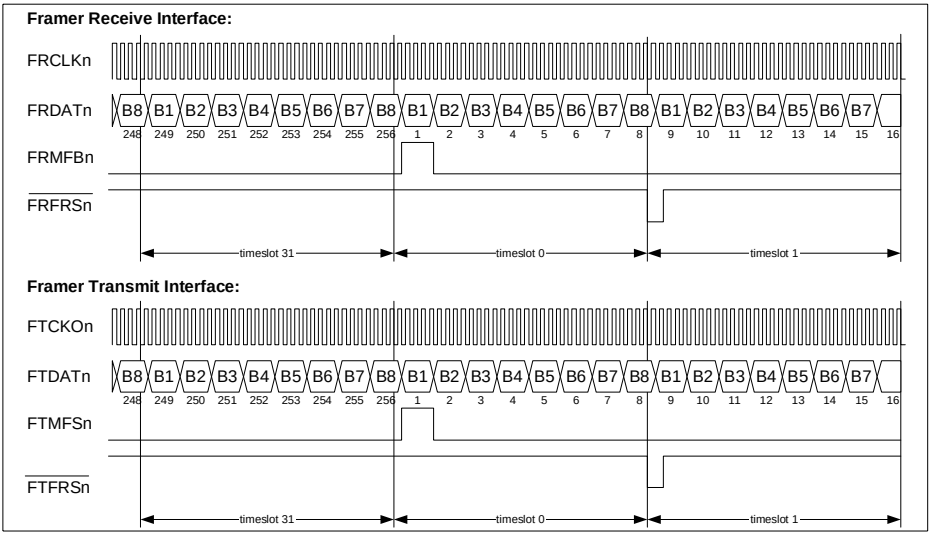


Figure 23 Framer Interface in FAM

5.1.1.1 T1 FALC Mode

In T1 mode (Pin E1/$\overline{T1}$ = 0) there is one F-channel carrying the F-bit (Frame Alignment Signal/Data Link (FS/DL)) and 24 data channels numbered from 1 to 24. When using the QuadFALC in translation mode 0 (See QuadFALC data sheet) these channels are mapped into the 32 frame slots as shown in **Table 25**

Table 25 Time slot Mapping in T1 Translation Mode 0

Frame slot	T1 channel	Frame slot	T1 channel
0	F channel (FS/DL)	16	
1	channel 1	17	channel 13
2	channel 2	18	channel 14
3	channel 3	19	channel 15
4		20	
5	channel 4	21	channel 16
6	channel 5	22	channel 17
7	channel 6	23	channel 18
8		24	
9	channel 7	25	channel 19

Table 25 Time slot Mapping in T1 Translation Mode 0 (cont'd)

Frame slot	T1 channel	Frame slot	T1 channel
10	channel 8	26	channel 20
11	channel 9	27	channel 21
12		28	
13	channel 10	29	channel 22
14	channel 11	30	channel 23
15	channel 12	31	channel 24

The F-channel only contains the F-bit. Its location in the F channel is shown in **Table 26**.

Table 26 F-Channel Format in T1 Mode

MSB			F channel				LSB
bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	bit 8
							F-bit

5.1.1.2 E1 FALC Mode

In E1 mode (Pin E1/$\overline{T1}$ = 1) there are 32 channels numbered from 0 to 31. The channels are directly mapped into the corresponding 32 frame slots.

5.1.2 Generic Interface Mode (GIM)

The Generic Interface Mode (GIM) makes the framer interface more universal, so that other framer/line interface units or T1/E1 transceivers can be connected directly to the IWE8. Depending on the E1/$\overline{T1}$ pin, the interface can be adopted to line bit rates of 1.544 MHz (T1 rate) or 2.048 MHz (E1 rate). The mode is enabled by setting bit om = 01_B in "opmo", see **Chapter 7.24**. Make sure that no clocks are applied to the transmitter when switching to GIM (FTCKOi has to be disconnected to ensure proper port function).

5.1.2.1 T1 Mode

FRCLK[7:0] Framer Receive Clock
Receive clock input at 1.544 MHz

FRDAT[7:0] Framer Receive Data
depending on bit "frri" in "opmo":

0 = FRDAT is sampled with the falling edge of FRCLK

1 = FRDAT is sampled with the rising edge of FRCLK

FRMFB[7:0] Framer Receive Multiframe Begin
Depending on bits p_ces in pcfN:

0 = Structured CES: A pulse on this pin designates the first frame of a new multiframe

1 = Unstructured CES: Unused, no constant level allowed

Depending on bit “rfpp” in “opmo”:

0 = FRMFB is active low

1 = FRMFB is active high

FRMFB is always sampled with the falling edge of FRCLK.

$\overline{\text{FRFRS}}$[7:0] Framer Receive Frame Synchronization Pulse
Permanently inactive

FRLOS[7:0] Framer Receive Loss of Signalling

FTCKO[7:0] Framer Transmit Clock
depending on bits ftckn in ftcs:

00 = depending on bit “rts_eval” in “opmo”:
0 = Transmit clock input with 1.544 MHz
1 = Clock of ICRC is used as transmit clock and is also switched to FTCKO pins (FTCKO is output pin)

01 = FRCLK

10 = Clock derived from RFCLK

11 = No clock

FTDAT[7:0] Framer Transmit Data
depending on bit “ftri” in “opmo”:

0 = FTDAT is clocked with the falling edge of FTCKO

1 = FTDAT is clocked with the rising edge of FTCKO

FTMFS[7:0] Framer Transmit Multiframe Synchronization

Depending on bit p_ces in pcfN:

0 = Structured CES: Depending on “p_tx_mfs” in “pcfN”:
0 = Superframe frame mode: FTMFS is asserted every 12 frames (1.5 ms)
1 = Extended superframe mode: FTMFS is asserted every 24 frames (3 ms)

1 = Unstructured CES: Inactive level

Depending on bit “tfpp” in “opmo”:

0 = FTMFS is active low

1 = FTMFS is active high

$\overline{\text{FTFRS}}$[7:0] Framer Transmit Frame Synchronization Pulse
$\overline{\text{FTFRS}}$ is asserted synchronously to the transmission of the F-bit of each frame.

RFCLK Reference Clock
- Reference clock for the internal clock recovery circuit
- Depending on p_rx_em in pcfN: Optional emergency clock if no transition on FRCLK is detected within 23 CLOCK cycles. The segmentation continues using the RFCLK divided by four, and using the byte-pattern programmed to a_emg_bpslct in acfg for the cell payload.

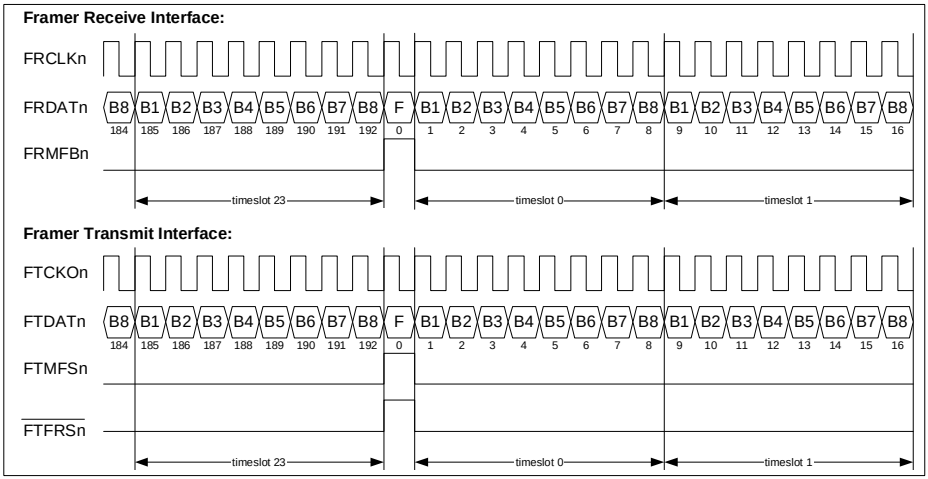


Figure 24 Framer Interface in GIM T1

5.1.2.2 E1 Mode

FRCLK[7:0] **Framer Receive Clock**
Receive clock input with 2.048 MHz

FRDAT[7:0] Framer Receive Data
depending on bit “frri” in “opmo”

0 = FRDAT is sampled with the falling edge of FRCLK

1 = FRDAT is sampled with the rising edge of FRCLK

FRMFB[7:0] Framer Receive Multiframe Begin
Depending on bits p_ces in pcfN:

0 = Structured CES: A pulse on this pin designates the first frame of a new multiframe

1 = Unstructured CES: Unused, no constant level allowed

depending on bit “rfpp” in “opmo”:

0 = FRMFB is active low

1 = FRMFB is active high

FRMFB is always sampled with the falling edge of FRCLK.

$\overline{\text{FRFRS}}$[7:0] Framer Receive Frame Synchronization Pulse
Permanently inactive

FRLOS[7:0] Framer Receive Loss of Signalling

FTCKO[7:0] Framer Transmit Clock
depending on bits ftckn in ftcs:

00 = depending on bit “rts_eval” in “opmo”:
0 = Transmit clock input with 2.048 MHz
1 = Clock of ICRC is used as transmit clock and is also switched to FTCKO pins (FTCKO is output pin)

01 = FRCLK

10 = Clock derived from RFCLK

11 = No clock

FTDAT[7:0] Framer Transmit Data
depending on bit “ftri” in “opmo”:

0 = FTDAT is clocked with the falling edge of FTCKO

1 = FTDAT is clocked with the rising edge of FTCKO

FTMFS[7:0] Framer Transmit Multiframe Synchronization

Depending on bit p_ces in pcfN:

0 = Structured CES: Depending on “p_tx_mfs” in “pcfN”:
0 = Double frame mode: FTMFS is asserted every 2 frames (250 µs)
1 = CRC multiframe mode: FTMFS is asserted every 16 frames (2 ms))

1 = Unstructured CES: Inactive level

Depending on bit “tfpp” in “opmo”:

0 = FTMFS is active low

1 = FTMFS is active high

$\overline{\text{FTFRS}}[7:0]$ Framer Transmit Frame Synchronization Pulse
$\overline{\text{FTFRS}}$ is asserted synchronously to the transmission of the first bit of the first timeslot of each frame.

RFCLK Reference Clock
- Reference clock for the internal clock recovery circuit
- Depending on p_rx_em in pcfN: Optional emergency clock if no transition on FRCLK is detected within 23 CLOCK cycles. The segmentation continues using the RFCLK divided by four, and using the byte-pattern programmed to a_emg_bpslct in acfg for the cell payload.

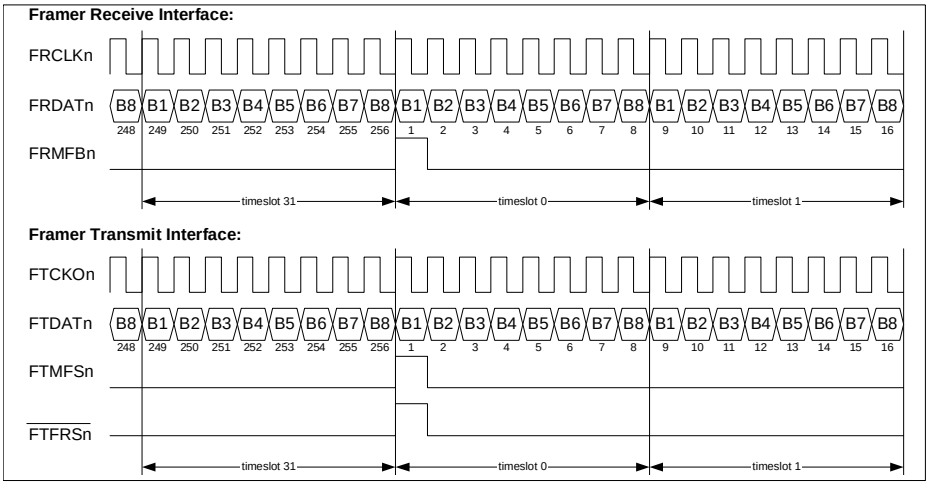


Figure 25 Framer Interface in GIM E1

5.1.3 Synchronous Modes (SYM)

In these modes, transmit and receive channels are synchronized. Therefore, they may be used for synchronization of frame and multiframe based protocols, e.g. Frame based SDT on E1-Lines.

Only one central clock, the external reference clock RFCLK, is used to clock the data on the different ports. Two synchronous modes working at 2.048 MHz and 8.192 MHz for E1lines are available. T1 is not supported.

For each of these modes a submode exists, providing global or port specific synchronization.

If global synchronization of all transmit and receive channels is desired, bit “symn” in “opmo” has to be deasserted. In this case FRMFB[0] is used for frame and multiframe synchronization in receive and transmit direction of all ports.

Port specific frame and multiframe synchronization of transmit and receive channels is enabled if bit “symn” in “opmo” is set. In this case frame and multiframe synchronization in receive and transmit direction of each port is based on the corresponding FRMFB.

After reset all outputs and input/output ports of the framer interface are in tristate mode. They will be enabled by setting bit “p_tx_act” of the corresponding “Port Configuration Register” (“pcfN”, see **Chapter 7.1**).

5.1.3.1 Synchronous Mode at 2.048 MHz (SYM2)

In SYM2 mode the framer interface is clocked with a 2.048 MHz clock connected to RFCLK. The mode is enabled by setting bit om = 11_B in “opmo”, see **Chapter 7.24**

All transmit and receive timeslots will be aligned to each other.

FRCLK[7:0] Framer Receive Clock
Unused

FRDAT[7:0] Framer Receive Data
depending on bit “frri” in “opmo”

0 = FRDAT is sampled with the falling edge of RFCLK

1 = FRDAT is sampled with the rising edge of RFCLK

FRMFB[7:0] Framer Receive Multiframe Begin
Depending on bits p_ces in pcfN:

0 = Structured CES: A pulse on this pin designates the first frame of a new multiframe

1 = Unstructured CES: Unused, no constant level allowed

depending on bit “rfpp” in “opmo”:

0 = FRMFB is active low

1 = FRMFB is active high

depending on bit “symn” in “opmo”:

0 = FRMFB[0] is used for frame and multiframe synchronization in receive and transmit direction of all ports. FRMFB[1:7] are unused

1 = FRMFB[N] is used for frame and multiframe synchronization in receive and transmit direction of corresponding ports

FRMFB is always sampled with the opposite clock-edge of FRDAT.

$\overline{\text{FRFRS}}$[7:0] Framer Receive Frame Synchronization Pulse
Unused

FRLOS[7:0] Framer Receive Loss of Signalling

FTCKO[7:0] Framer Transmit Clock
Unused

FTDAT[7:0] Framer Transmit Data
depending on bit “frri” in “opmo”:

0 = FTDAT is clocked with the rising edge of RFCLK

1 = FTDAT is clocked with the falling edge of RFCLK

FTMFS[7:0] Framer Transmit Multiframe Synchronization
Unused

$\overline{\text{FTFRS}}$[7:0] Framer Transmit Frame Synchronization Pulse
Unused

RFCLK Reference Clock
Central framer interface clock with 2.048 MHz

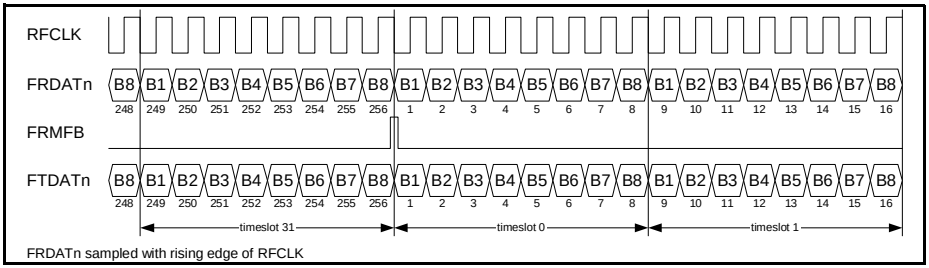


Figure 26 Framer Interface in SYM2 E1

5.1.3.2 Synchronous Mode at 8.192 MHz (SYM8)

In SYM8 mode the framer interface is clocked with an 8.192 MHz clock connected to RFCLK. The mode is enabled by setting bit om = 10_B in “opmo”, see **Chapter 7.24**

All timeslots (transmit and receive) will be aligned to each other.

FRCLK[7:0] Framer Receive Clock
Unused

FRDAT[7:0] Framer Receive Data
FRDAT is sampled in the middle of the bit period on the falling edge of RFCLK

FRMFB[7:0] Framer Receive Multiframe Begin
Depending on bits p_ces in pcfN:

0 = Structured CES: A pulse on this pin designates the first frame of a new multiframe

1 = Unstructured CES: Unused

depending on bit “rfpp” in “opmo”:

0 = FRMFB is active low

1 = FRMFB is active high

depending on bit “symn” in “opmo”:

0 = FRMFB[0] is used for frame and multiframe synchronization in receive and transmit direction of all ports. FRMFB[1:7] are unused

1 = FRMFB[N] is used for frame and multiframe synchronization in receive and transmit direction of corresponding ports

FRMFB is always sampled with the opposite clock-edge of FRDAT.

$\overline{\text{FRFRS}}$[7:0] Framer Receive Frame Synchronization Pulse
Unused

FRLOS[7:0] Framer Receive Loss of Signalling

FTCKO[7:0] Framer Transmit Clock
Unused

FTDAT[7:0] Framer Transmit Data
FTDAT is clocked with the falling edge of RFCLK:

FTMFS[7:0] Framer Transmit Multiframe Synchronization
Unused

$\overline{\text{FTFRS}}$[7:0] Framer Transmit Frame Synchronization Pulse
Unused

RFCLK Reference Clock
Central framer interface clock with 8.192 MHz

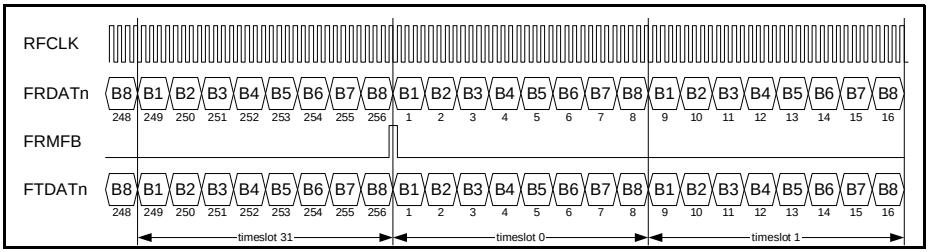


Figure 27 Framer Interface in SYM8 E1

5.1.4 Echo Canceller Mode (EC)

In this mode (pin $\overline{\text{EC}}$ = 0) transmit and receive channels are synchronized.

The framer interface is clocked with an 8.192 MHz clock connected to RFCLK.

All receive channels and the channels transmitted on even ports (near-end signal with echo) are synchronized by means of the $\overline{\text{FTFRS}}$[0] pin. Shift exists between odd and even FTDAT ports

FRCLK[7:0] Framer Receive Clock
Unused

FRDAT[7:0] Framer Receive Data
FRDAT is sampled in the middle of the bit period on the falling edge of RFCLK

FRMFB[7:0] Framer Receive Multiframe Begin
Unused

$\overline{\text{FRFRS}}$[7:0] Framer Receive Frame Synchronization Pulse
Unused

FRLOS[7:0] Framer Receive Loss of Signalling

FTCKO[7:0] Framer Transmit Clock
Unused

FTDAT[7:0] Framer Transmit Data
FTDAT is clocked with the falling edge of RFCLK:

FTMFS[7:0] Framer Transmit Multiframe Synchronization
Unused

$\overline{\text{FTFRS}}$[7:0] Framer Transmit Frame Synchronization Pulse
$\overline{\text{FTFRS}}$[0] is asserted synchronously to the transmission of the first bit of the first timeslot of each frame. $\overline{\text{FTFRS}}$[1:7] are unused

RFCLK Reference Clock
Central framer interface clock with 8.192 MHz

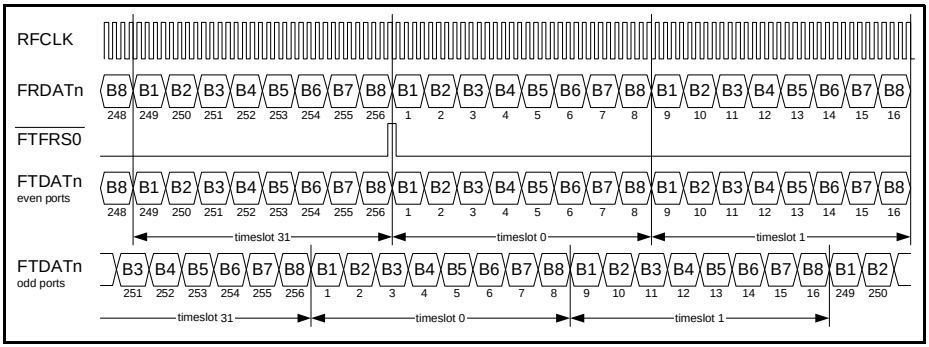


Figure 28 Framer Interface in EC Mode

5.2 UTOPIA Interface

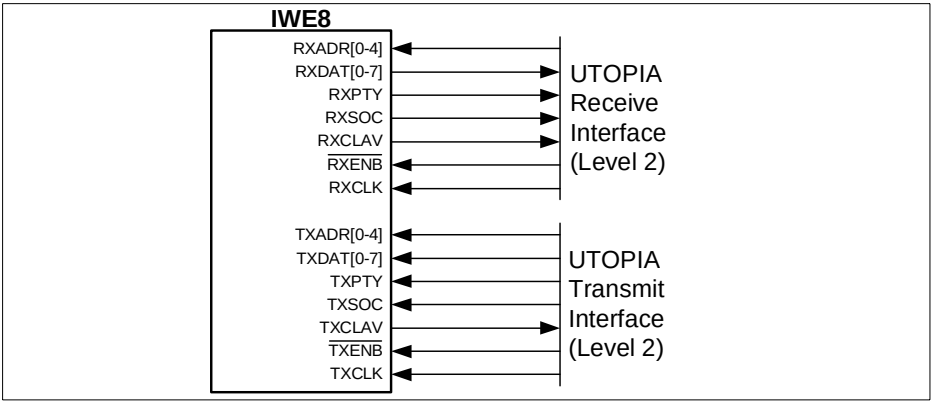


Figure 29 UTOPIA Receive and Transmit Interfaces in Slave Mode

The UTOPIA receive and transmit interfaces are implemented according to the ATM forum UTOPIA Level 2 Specification [6] and to the UTOPIA Level 1 Specification [5].

For UTOPIA level 2 compliant mode, the device is compatible to a PHY layer with 8 data lines and 5 address lines.

In UTOPIA level 1 compliant mode the interface can be configured to ATM and PHY layer with 8 data lines. In this case the address lines should be left unconnected.

According to the UTOPIA standard the ATM-Layer polls the PHY-Ports via the UTOPIA address lines. If the address matches the programmed address range, the PHY controls the flow of data via the TXCLAV or RXCLAV signal.

In transmit direction the PHY indicates via assertion of TXCLAV whether the corresponding port is capable of accepting data. In case data can not be transferred to the addressed port due to overrun of the programmed threshold of the port-specific cell buffer, the TXCLAV won't be activated.

In receive direction, RXCLAV is activated, if data is available at the addressed port.

Depending on the value of the "utmaster" bit in the "UTOPIA Configuration Register" ("utconf", see **Chapter 7.34**) the IWE8 will either act as an ATM -Layer (master mode) or PHY-Layer (slave mode). As an ATM-Layer, the IWE8 can only work in UTOPIA level 1 compliant mode. As PHY Layer, IWE8 supports both, single PHY in UTOPIA level 1 compliant mode and single/multi PHY in UTOPIA level 2 compliant mode. The selection between UTOPIA level 1 and level 2 can be done via the "utlevel" bit in "utconf".

5.2.1 Port Addresses

The device can implement up to 8 PHY-Ports (= framer ports).

In case it is configured for UTOPIA level 2 MPHY mode, the amount of implemented PHY ports can be selected via the associated address range (“utconf[utrange]” with utconf[mapping_mode] = 0).

In addition, the transmission of the UTOPIA port number via a user-defined field in the ATM header enables multi PHY operation even in UTOPIA level 1 mode and UTOPIA level 2 single PHY mode as described in **Chapter 5.2.3**.

In UTOPIA level 2 MPHY mode no port number mapping into the ATM header is done. However, using this feature in UTOPIA level 2 mode, will give access to all PHY ports while the UTOPIA interface block is running in single PHY mode. For UTOPIA level 2 compliant multi PHY operation, “mapping_mode” should be reset. In this case the UDF field is set to all zero.

In UTOPIA level 2 MPHY mode the port number is transported via the address pins. “utbaseadr” in “utconf” defines the base address under which the ports will be accessible. In UTOPIA level 1 mode, “utbaseadr” has to be set to "0" otherwise cells are discarded.

If the device is in single PHY mode, it will react on the address, written into “utbaseadr”. In multi PHY mode, the device will be accessible inside a window from “utbaseadr” to “utbaseadr” + “utrange”. Where the nth port can be accessed at “utbaseadr” + n.

5.2.2 Back Pressure/ATM Cell Discarding

Backpressure describes the mechanism that controls the TXCLAV signal in UTOPIA PHY mode. IWE8 supports two kinds of backpressure mechanisms, a general and a port specific one.

Cells that are destined to inactive ports or channels are generally discarded.

5.2.2.1 General Backpressure Mechanism

The general backpressure mechanism depends only on the filling level of the 4 cell UTOPIA input buffer.

General backpressure is active in all UTOPIA configurations:

- UTOPIA level 1compliant mode (utlevel=1)
- UTOPIA level 2 PHY mode, where the selection between ports is done by ATM header fields (mapping_mode!=0)
- UTOPIA level 2 PHY mode, with port selection by ATM header fields disabled (mapping_mode=0) and the port threshold mode (“p_thr_m” bits in “pcfN”) disabled.

The general threshold is defined in the “Threshold Register” (“thrshld”, see **Chapter 7.33**).

5.2.2.2 Port Specific Backpressure Mechanism

In addition to the general backpressure mechanism, port specific backpressure is available for ATM ports, when using the IWE8 as a UTOPIA level 2 PHY device (“utconf[utlevel]” =0, “utmaster” = 0, “mapping_mode” =0 and “pcfN[p_atm]” =1). It needs to be explicitly enabled with the “p_thr_m” bits in the “Port Configuration Registers” (“pcfN”, see **Chapter 7.1**).

Whenever the port transmit buffer filling level falls below the programmed value and the port is selected via the UTOPIA PHY address, the TXCLAV signal is activated, allowing another data transfer for that port. If this transfer exceeds the predefined buffer filling level, the UTOPIA interface immediately enters backpressure state for this port.

When using the port specific backpressure mechanism (“p_thr_m” = 01_B or 10_B) the general threshold defined in the “Threshold Register” (“thrshld”, see **Chapter 7.33**) should be higher than the port specific threshold defined in the “Threshold Port Register” (“thrspN”, see **Chapter 7.38** to **Chapter 7.41**).

5.2.3 Sideband Signals of the UTOPIA Interface

In UTOPIA level 1 mode or UTOPIA level 2 single PHY mode, the framer port number ("port_nr[2:0]") can be transmitted via the UTOPIA interface. The field contains the number of the physical (framer) port associated with that ATM cell. Its location inside the ATM header is configurable via the “mapping_mode” bits in “utconf” (**Chapter 7.34**). Possible locations are: GFC[3:1], VPI[7:5], VCI[15:13], VCI[7:5] or UDF[2:0].

In AAL mode, the channel number ("channel_nr", first timeslot number of a channel, reference timeslot) has to be transmitted on the UTOPIA transmit interface via VCI[4:0].

If no discarding of cells with uncorrectable HEC error is selected on a specific port via bits “a_hec_mode” in the register “acfg” (**Chapter 7.2**) and "p_cell_disc" in the register "pcfN" (**Chapter 7.1**) an HEC error flag (HEF) indicates corrupted HEC by setting the most significant bit in the user defined octet at the UTOPIA interface. For correct operation bit "p_cell_disc" must be cleared.

The bit ENB, bit 5 of the user defined octet, is responsible for the decision if cell discarding shall base on CLP or CLPI.

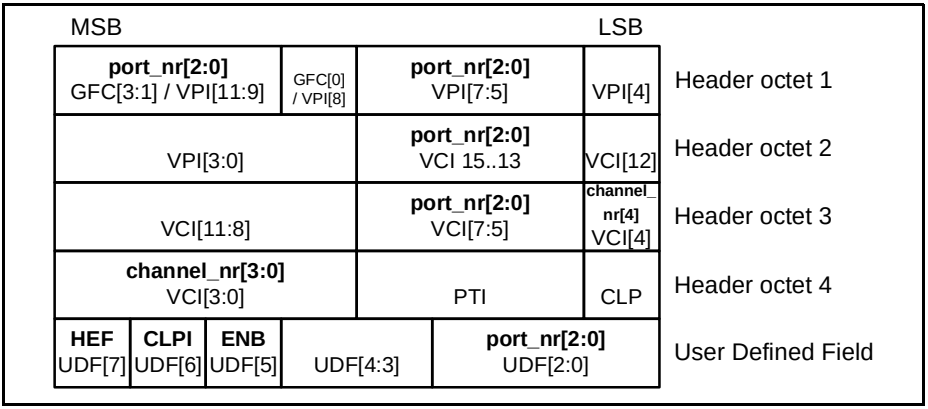


Figure 30 Utopia Sideband Signals

5.3 IMA Interface

The IWE8 has provisions to support the Inverse Multiplexing over ATM (IMA) protocol implemented in an external component. These are:

- An IMA interface
- A programmable threshold between read and write pointer of the mapping buffer.

If an Uncorrectable HEC Error (UNCHEC) is detected, the cell is discarded and the UNCHEC signal will be asserted. At the same time the port number, where the cell came from, will be available at pins PN[2:0].

The ATM Transmit Buffer Threshold Crossing (ATBTC) signal becomes active when the difference between write and read pointer of the ATM Transmit Buffer becomes smaller than the threshold selected with bits “bufthr” in the “Operation Mode Register” (“opmo”, see **Chapter 7.24**). At the same time the Port Number, where the cell came from, will be available at pins PN[2:0].

At the IMA interface the IWE8 operates in cycles of 12 system clocks. ATBTC can become active during cycle #3, the UNCHEC can become active during cycle #9. The Port number is always active for 6 cycles.

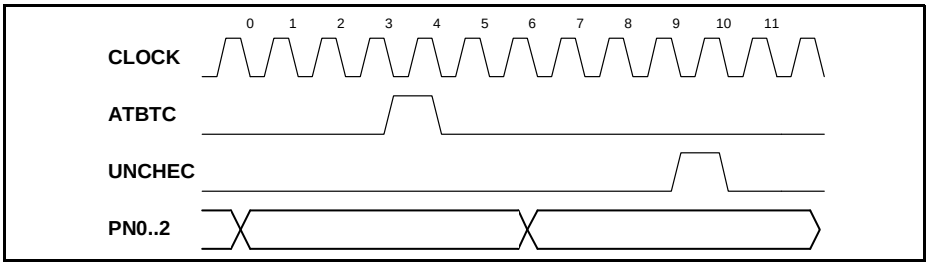


Figure 31 IMA Interface Protocol

For more detailed information on the IMA interface refer to the Application Hint “Inverse Multiplexing for ATM (IMA) with the Interworking Element IWE8”.

5.4 Clock Recovery Interface

It is possible to use an external device for clock recovery instead of the ICRC. Therefore an external clock recovery interface is provided.

It allows the transmission and reception of serial communication frames containing SRTS values or ACM buffer filling levels to and from an external clock recovery circuit.

The usage is controlled by the bits “rtsgen” and “rts_eval” in the Operation Mode Register (“opmo”, see **Chapter 7.24**).

The Clock Recovery Interface is a 5 line serial interface: 1 data input SDI, 2 data outputs SDOD and SDOR and 1 synchronization output SSP. The interface allows connection to external clock recovery circuits. Two methods for clock recovery are supported: Synchronous Residual Time Stamp (SRTS) and Adaptive Clock Method (ACM). The IWE8 also allows a combination of SRTS and ACM.

The data sent over the serial lines is always formatted in frames of 32 bits.

The SSP pulse indicates the frame start for both directions. The inter-frame delay should be equivalent to the payload of 8 ATM cells (e.g. for completely filled cells without SDT every 3008 clock periods). Each valid frame is supposed to contain a valid RTS value

Table 27 shows the interface frame format. Bit [31] is sent first. When no data is to be sent, idle frames are transmitted consisting of bits [31:1] all 1 and parity bit[0] = 0. **Table 27** also indicates which data fields are used on the different interface signals.

Table 27 Clock Recovery Interface frame format

Bits	Data field	SDI	SDOD	SDOR
31- 29	111	Yes	Yes	Yes
28 - 25	RTS[3:0]	Yes	Yes	No
24 - 11	buffer_fill[13:0]	No	Yes	No
10	RTS_valid	No	Yes	No
9 - 8	00	Yes	Yes	Yes
7 - 5	port_nr[2:0]	Yes	Yes	Yes
4 - 2	type[2:0] 001: RTS only 010: “buffer_fill” only 011: RTS + “buffer_fill” 111: reset RTS logic others: not used	 No No No No	 Yes Yes Yes No	 No No No Yes
1	frame_invalid	Yes	Yes	Yes
0	odd_parity	Yes	Yes	Yes

To allow the external SRTS generation logic to synchronize with the cell segmentation process, the IWE8 will output a frame with type = 111 on the SDOR signal when the segmentation of the first ATM cell for a selected channel starts. The first two sequences of 8 ATM cells will contain a dummy RTS value which is programmable in the “ASIC Configuration Register” (“acfg”, see **Chapter 7.2**). From the third sequence on the values received on the SDI input will be used.

The IWE8 has internal ‘RTS Buffers’ for 2 RTS values per port. When one of the ‘RTS Buffers’ overflows, the value in excess will be omitted and a bit in the Extended Interrupt Status Register 2 (eis2, see **Chapter 7.20**) will be set. When ‘RTS Buffer’ underflow occurs, the last received RTS value will be repeated in the next sequence of 8 ATM cells.

The RTS value extracted from a cycle of 8 ATM cells with sequence count 0 to 7, is transmitted on SDOD when the cell with sequence count 1 from the next cycle is received. The ‘RTS_valid’ field is used to indicate whether the extracted RTS value is correct or not. An extracted RTS is accepted as valid if in the previous cycle of 8 cells the cells with SN = 1, 3, 5 and 7 were present and were accepted as valid cells.

The buffer filling level is transmitted for use with the Adaptive Clock Method (ACM) and is expressed as a number of octets contained in the ‘Reassembly Buffer’. The buffer filling level is transmitted every time when a new ATM cell for the selected channel is received.

5.5 Microprocessor Interface

IWE8 contains internal registers, 4 internal RAMs and an external RAM that can be read and written via the Microprocessor Interface.

As access to the internal registers is 16-bit oriented, the Microprocessor Address Bus (MPADR) is designed for 16-bit boundaries. Access to the 32-bit-wide internal or external RAM has to be executed in two consecutive 16 bit cycles.

The Microprocessor data bus (MPDAT) has “little endian” word order. Little to big endian conversion may be implemented either by initialization of the microcontroller or by hardwiring MPDAT[7:0] to DATA[15:8] and MPDAT[15:8] to DATA[7:0] respectively,

The 32 bit oriented accesses have to be done by two consecutive 16 bit accesses, the first with MPADR[0] = 0 and the second with MPADR[0] = 1. The IWE8 will not verify whether the address bits MPADR[17:1] during the second access are the same as during the first access.

The data of the first of two consecutive write cycles (MPADR[0] = 0) is written temporarily into an internal write-cache register. The second write cycle (MPADR[0] = 1) causes the data to be written into internal or external RAM. Bits [15:0] are written from the internal write-cache register and bits [31:16] are transferred from MPDAT

During the first of two consecutive read cycles (MPADR[0] = 0), the 32 bit data are actually read from internal or external RAM. Bits [15:0] are transferred to the databus MPDAT. Bits [31:16] are written into an internal read-cache register. During the second read (MPADR[0] = 1) the read-cache register is transferred to the databus. When only bits [15:0] are needed, the second read cycle can be omitted.

For proper operation without acknowledge handshake via MPRDY 23 waitstates can be used.

5.5.1 Interrupt Handling

The IWE8 provides two independent interrupt pins MPIR1 and MPIR2. The interrupt handling software should read the interrupt status registers to identify the causes of the interrupt.

MPIR1 is the main interrupt pin indicating a special event in the IWE8. The interrupt cause can be determined by reading Interrupt Status Register 1 ("isr1", see **Chapter 7.18**). Each of the interrupt sources can be individually masked in the corresponding interrupt mask register. If the interrupt source is masked, the interrupt pin MPIR1 will not be asserted when the corresponding event occurs.

MPIR2 is an auxiliary interrupt pin. The IWE8 provides two sets of 8 independent timers in external RAM (timer set 1 and 2). Timer set 2 can be used independently from the rest of the IWE8 driver software. When one of the timers of timer set 2 expires, a bit will be set in the Interrupt Status Register 2 ("isr2", see **Chapter 7.23**) and MPIR2 will be asserted.

5.5.2 Microprocessor Interface Mode

The IWE8 microprocessor interface allows connection of Intel type microprocessors as well as Motorola type microprocessors (e.g. the PowerPC).

The Microprocessor Interface Mode is determined via the status of the pins PMT and TBUS at the positive edge of the internal reset. Therefore, PMT and TBUS levels have to be kept at least 3 clock cycles after deassertion of $\overline{\text{RESET}}$.

Table 28 Configuration of the Microprocessor Interface Mode via PMT and TBUS

PMT	TBUS	Mode
0	0	Intel Mode
1	1	Motorola Mode

The mode currently assigned to the microprocessor interface is visible via “mtypsel” in the “Version Register” (“vers”, see **Chapter 7.16**).

Intel Mode

The connection of the 16 bit Intel compatible asynchronous microprocessor interface to an Intel 386EX processor is shown in **Figure 32**.

If the ready signal at pin MPRDY shall be used, a glue logic between MPRDY of the IWE8 and RDY of the 386EX is required, which generates an active low signal with 1 microprocessor cycle length after a rising edge detection of the MPRDY signal.

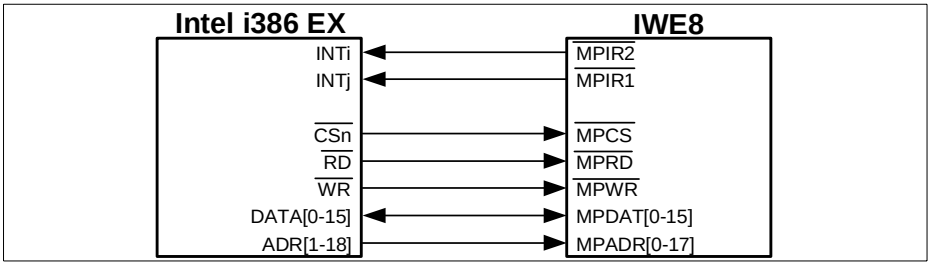


Figure 32 Connection of IWE8 to an Intel Type Microprocessor

Motorola Mode

Figure 33 shows the connection of the 16 bit Motorola compatible asynchronous interface to the MC68xxx.

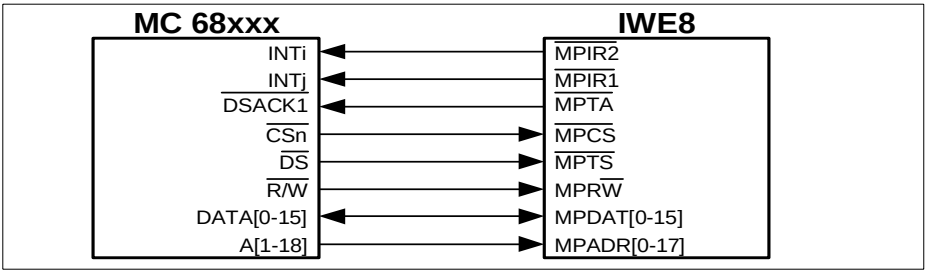


Figure 33 Connection of IWE8 to an Motorola Type Microprocessor

5.6 External RAM Interface

The IWE8 needs to be connected to an external synchronous SRAM of 64k x 33 bits with parity protection or 64k x 32 bits without parity protection.

For proper operation FT (Flow Through) SSRAM is needed. Pipelined SSRAM can not be used, as this type has additional registered outputs.

A possible connection with 1 SRAM 64k x 36 component is shown in **Figure 34**.

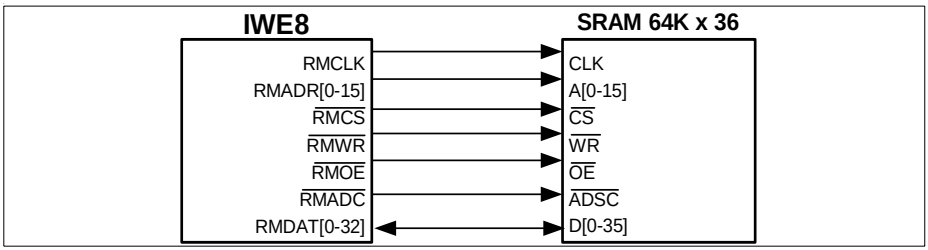


Figure 34 External RAM Connection

The IWE8 has a fixed RAM interface cycle of 12 clock periods. A sequence of 6 consecutive read cycles (addresses AR1 to AR6), a dummy address cycle and 5 consecutive write cycles (addresses AW1 to AW5) is continuously repeated. The timing of RMADC and RMOE is always fixed as shown in **Figure 35**. Whether the IWE8 reads data from the external RAM or writes data into the external RAM is controlled by the RMCS and RMWR signals. In **Figure 35**, data R1 and R3 are actually read by the IWE8, and data W1 and W3 are actually written into the external RAM.

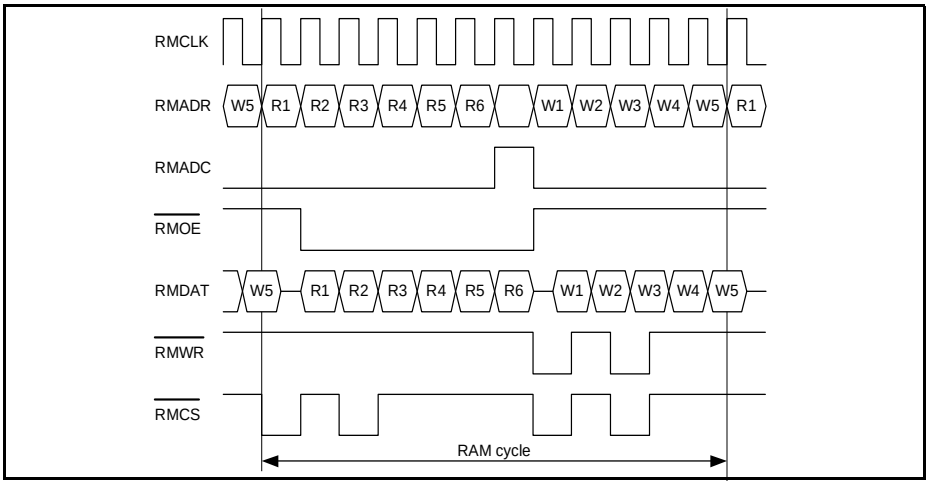


Figure 35 RAM Interface Protocol

5.7 Boundary Scan Interface

The boundary scan interface implements the Test Access Port (TAP) as defined in IEEE Standard 1149.1-1990 [19] including the optional $\overline{\text{TRST}}$ reset signal.

The device identification register, the instruction register and boundary-scan register are described in the electrical characteristics.

5.8 Master Clock

The basic processing time of an octet in the IWE8 is 12 clock cycles. As the time needed to process one octet for each of the 8 ports must be less than the time required to transfer one octet over a framer interface, this leads to the condition:

$$m \times o \times T_{CLOCK} < f \times b \times T_{FramerClk} \quad [15]$$

with:

m = 12 master-clock cycles needed for one octet per port

o = 8 ports

f = Framer-clock cycles per bit

b = 8 bits per octet

$$T_{Clock} > \frac{f}{12} \times T_{FramerClk} \quad [16]$$

Table 29 Master Clock Frequency Depending on Mode

Mode	T_{CLOCK}	F_{CLOCK}
FAM, SYM8 and EC	< 1/3 x $T_{FramerCLK}$	> 3 x $F_{FramerCLK}$ = 3 x 8.192 MHz
GIM E1 and SYM2	< 1/12 x $T_{FramerCLK}$	> 12 x $F_{FramerCLK}$ = 12 x 2.048 MHz
GIM T1	< 1/12 x $T_{FramerCLK}$	> 12 x $F_{FramerCLK}$ = 12 x 1.544 MHz

6 Memory Structure

The IWE8 occupies an address space of 256k x 16 bits. The lower 128k x 16 bits are used for internal registers and internal configuration RAM's. The upper 128k x 16 bits are used to address external RAM.

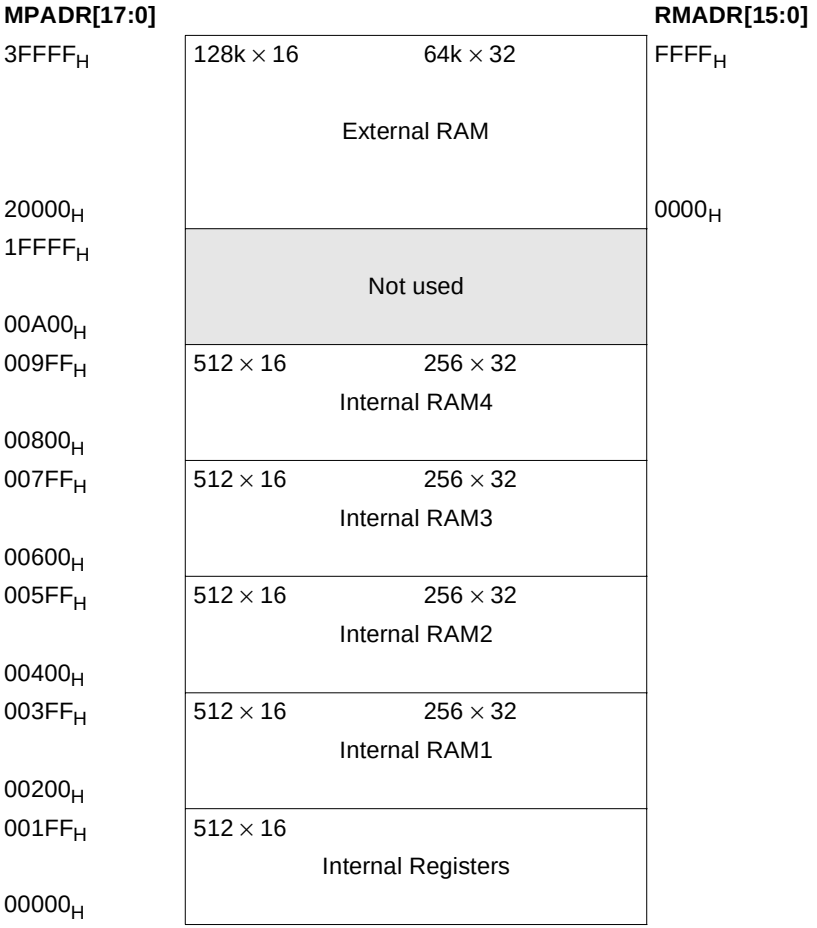


Figure 36 Memory Model

The 4 internal configuration RAMs are organized as 256 x 32 bit memories, but RAM4 has only 16 bits implemented (bit positions 16 to 31 are always read as "0").

The external RAM is organized as a 64k x 32 bit parity protected memory.
Accesses to internal configuration RAM's or external RAM are always 32 bit oriented.

6.1 Internal Configuration RAM's

The 4 internal 256 x 32 bit configuration RAM's (RAM1, RAM2, RAM3 and RAM4) are used to assign the timeslots of the Framer Receive and Framer Transmit interfaces to ATM channels. For each port there are 32 entries. RAM1 is used to define the timeslots of the Framer Receive ports, and RAM2 and RAM3 are used to define the Framer Transmit ports. RAM4 is responsible for CAS conditioning and freezing in transmit direction

When the contents of the internal RAMs have been altered by the software, the internal state machines will load the new values within the next 1.5 frame cycles (187.5 µs). Up to that point of time the previous values are used.

6.1.1 RAM1: Receive Port Configuration

Read/write Address 00200_H to $003FF_H$

Reset value: Not applicable. RAM must be reset and initialized via SW

Memory size 256K × 32 bits: 8 ports x 32 slots x 1 doubleword

MPADR	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	1	port_nr [2:0]			slot[4:0]					

6.1.1.1 RAM1: ATM Receive Reference Slot

Read/write Address 00200_H to $003FF_H$

Reset value: Not applicable. RAM must be reset and initialized via SW.

31							24
Not used							
23							**16**
Not used							
15							**8**
Not used							
7							**0**
ocd_start_intrpt	ocd_end_intrpt	go_hunt	delete_idle_cells	x43_descrambling	channel_mode[1:0]		ref_slot = 1

ocd_start_intrpt Generate interrupt when OCD state starts

0 = Disabled

1 = Enabled

ocd_end_intrpt Generate interrupt when OCD state ends

0 = Disabled

1 = Enabled

go_hunt Go to hunt state

0 = Cell delineation finite state machine normal operation

1 = Cell delineation finite state machine forced in hunt state
Only the transition 0 → 1 forces the hunt state. Counter (number of times SYNC state is left) is *not* incremented. Ocd_start interrupt is *not* generated.

delete_idle_cells Delete idle/unassigned cells enable

0 = Disabled

1 = Enabled

x43_de scrambling ATM cell payload descrambling enable

0 = Disabled

1 = Enabled

channel_mode Channel mode

00 = Inactive mode

01 = Active mode (normal mode)

10 = Standby mode

11 = Active mode (normal mode)

ref_slot Reference slot indicator

1 = This slot is a reference slot

Note: To allow IWE8 internal initialization, all channels must remain in inactive mode for at least 250 µs after activation of the port (i.e. setting pcfN[p_rx_act] = 1). During this time the device connected to the Framer Receive Interface has to be in normal operation.

6.1.1.2 RAM1: ATM Receive Continuation Slot

Read/write Address 00200_H to $003FF_H$
Reset value: Not applicable. RAM must be reset and initialized via SW.

31			24
Not used			
23			**16**
Not used			
15			**8**
Not used			
7			**0**
Not used	ref_slot_nr[4:0]	cont_slot = 1	ref_slot = 0

ref_slot_nr Reference slot number
Number of the reference slot of this channel

cont_slot Continuation slot indicator

1 = This slot is a continuation slot

ref_slot Reference slot indicator

0 = This slot is not a reference slot

6.1.1.3 RAM1: AAL Receive Reference Slot

Read/write Address 00200_H to $003FF_H$
Reset value: Not applicable. RAM must be reset and initialized via SW

31				24
next_slot_nr[4:0]		sdt_mfs	sig_cond	srts
23				**16**
subst_bpslct[1:0]	dcor	dcor_random_nr[4:0]		
15				**8**
aal0	part_fill[5:0]			band_ width[4]
7				**0**
band_width[3:0]	sdt	channel_mode[1:0]		ref_slot = 1

next_slot_nr Next slot number
If band_width > 0 next_slot_nr points to the next slot of this channel.
If band_width = 0 and CAS is activated next_slot_nr[3:0] will be used as signalling conditioning nibbles.
If band_width = 0 and CAS is not activated next_slot_nr is don't care.

sdt_mfs SDT multiframe pulse select

X = If [aal0] = 1 or [sdt] = 0 or pcfN[p_ces] = 1

0 = Start of structure is frame pulse

1 = Start of structure is multiframe pulse as defined by pcfN[p_tx_mfs]

sig_cond Signalling conditioning upstream

0 = CAS freezing upstream enabled in "loss of signal" condition

1 = CAS conditioning upstream enabled in "loss of signal" condition

srts SRTS enable
Enables RTS value insertion into AAL1 SAR-PDUs

X = If pcfN[p_srts] = 0 or [aal0] = 1

0 = Disabled

1 = Enabled

subst_bpslct Substitute byte-pattern select

00 = Select byte-pattern 0, defined in bp10[bp0]

01 = Select byte-pattern 1, defined in bp10[bp1]

10 = Select byte-pattern 2, defined in bp32[bp2]

11 = Select byte-pattern 3, defined in bp32[bp3]

dcor Decorrelation circuit enable

0 = Disabled

1 = Enabled

dcor_random_nr Decorrelation random Number

X = if [dcor] = 0

aal0 AAL0 enable

0 = Disabled (AAL1 is used)

1 = Enabled (instead of AAL1)

part_fill Partially filled cell filling level

	4 to 48	AAL0: [aal0] = 1
	4 to 47	AAL1 unstructured CES: [aal0] = 0, pcfN[p_ces] = 1
	4 to 47	AAL1 structured CES without CAS[1]: [aal0] = 0, pcfN[p_ces] = 0, pcfN[p_cas] = 0
	4+Cb to 46	AAL1 structured CES with CAS[2]: [aal0] = 0, pcfN[p_ces] = 0, pcfN[p_cas] = 1
band_width	band_width	
	N-1	Structured CES (with N = number of timeslots of the channel)
	$1F_H$	Unstructured CES (pcfN[p_ces] = 1)
sdt	SDT enable	
	X =	If pcfN[p_ces] = 1 or [aal0] = 1
	0 =	Disabled
	1 =	Enabled
channel_ mode	Channel mode	
	00 =	Inactive mode
	01 =	Active mode (normal mode)
	10 =	Standby mode
	11 =	Substitute mode
ref_slot	Reference slot indicator	
	1 =	This slot is a reference slot

1) non-P format, cell may have only 46 user data octets in P format

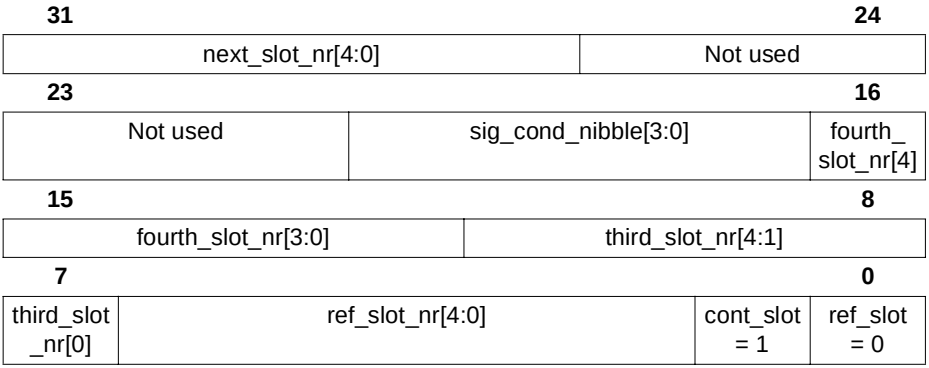
2) Cb: Required bytes for the CAS sub-block in an ATM cell

Note: To allow IWE8 internal initialization, all channels must remain in inactive mode for at least 250 µs after activation of the port (i.e. setting pcfN[p_rx_act] = 1). During this time the device connected to the Framer Receive Interface has to be in normal operation.

Note: If frame based SDT without CAS is used and filling level ≤ 45, the condition band_width ≤ part_fill has to be fulfilled for correct operation.
Multiframe based SDT without CAS should not be used.

6.1.1.4 RAM1: AAL Receive Continuation Slot

Read/write Address 00200_H to $003FF_H$
Reset value: Not applicable. RAM must be reset and initialized via SW.



next_slot_nr Next slot number
Number of the next slot of this channel. When no continuation slots exist, the entry “next_slot_nr” should refer to the reference slot.

sig_cond_ nibble 4 bits for signalling conditioning
It is possible to have different signalling conditioning nibbles for all slots of a channel except for the first two slots of a channel. The first slot in a channel will always use the same nibbles as the first continuation slot.

fourth_slot_ nr Fourth slot number
Number of the fourth slot of this channel

X = If [band_width] < 3

third_slot_ nr Third slot number
Number of the third slot of this channel

X = If [band_width] < 2

ref_slot_nr Reference slot number
Number of the reference slot of this channel

cont_slot Continuation slot indicator

1 = This slot is a continuation slot

ref_slot Reference slot indicator

0 = This slot is not a reference slot

6.1.1.5 RAM1: ATM or AAL Receive Idle Slot

Read/write Address 00200_H to $003FF_H$
Reset value: Not applicable. RAM must be reset and initialized via SW.

31								24
Not used								
23								**16**
Not used								
15								**8**
Not used								
7								**0**
Not used							cont_slot = 0	ref_slot = 0

cont_slot Continuation slot indicator
0 = This slot is not a continuation slot

ref_slot Reference slot indicator
0 = This slot is not a reference slot

6.1.2 RAM2: Transmit Port Configuration

Read/write Address 00400_H to $005FF_H$
Reset value: Not applicable. RAM must be reset and initialized via SW
Memory size 256K × 32 bits: 8 ports x 32 slots x 1 doubleword

MPADR	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	1	0	port_nr [2:0]			slot[4:0]					

6.1.2.1 RAM2: ATM Transmit Reference Slot

Read/write Address 00400_H to $005FF_H$
Reset value: Not applicable. RAM must be reset and initialized via SW.

31			24
Not used			
23			**16**
Not used			
15			**8**
Not used			
7			**0**
Not used	x43_ scram-bli ng	channel_mode[1:0]	ref_slot = 1

x43_scrambling ATM cell payload scrambling enable

0 = Disabled

1 = Enabled

channel_mode Channel mode

00 = Inactive mode

01 = Active mode (normal mode)

10 = Standby mode

11 = Active mode (normal mode)

ref_slot Reference slot indicator

1 = This slot is a reference slot

Note: RAM slot 1 has always to be configured always as reference slot.

Note: To allow IWE8 internal initialization, all channels must remain in inactive mode for at least 250 µs after activation of the port (i.e. setting pcfN[p_tx_act] = 1). During this time the device connected to the Framer Transmit Interface has to be in normal operation.

6.1.2.2 RAM2: ATM Transmit Continuation Slot

Read/write Address 00400_H to $005FF_H$
Reset value: Not applicable. RAM must be reset and initialized via SW.

31			24
next_slot_nr[4:0] = 00000		Not used	
23			**16**
Not used			
15			**8**
Not used			
7			**0**
Not used	ref_slot_nr[4:0]	cont_slot = 1	ref_slot = 0

next_slot_nr Next slot number

0 = This field must be all 0 for ATM continuation slots

ref_slot_nr Reference slot number
Number of the reference slot of this channel

cont_slot Continuation slot indicator

1 = This slot is a continuation slot

ref_slot Reference slot indicator

0 = This slot is not a reference slot

6.1.2.3 RAM2: AAL Transmit Reference Slot

Read/write Address 00400_H to $005FF_H$
Reset value: Not applicable. RAM must be reset and initialized via SW.

31						24
next_slot_nr[4:0]				Not used	snp_ check	sn_ check
23						**16**
sc_fast	sdt_mfs	sdt_oos_nr[1:0]	sdt_par	sdt_once	crv_en	mcp_ reinit
15						**8**
aal0	part_fill[5:0]					band_ width[4]
7						**0**

band_width[3:0]	sdt	channel_mode[1:0]	ref_slot = 1

next_slot_nr Next slot number
Number of the second slot of this channel. When no continuation slots exist, the entry “next_slot_nr” should refer to the reference slot.

X = If pcfN[p_ces] = 1

snp_check SNP field check enable

X = If [aal0] = 1 or [sn_check] = 0

0 = Disabled

1 = Enabled

sn_check SN field check enable

X = If [aal0] = 1

0 = Disabled

1 = Enabled

sc_fast SC algorithm select

X = If [aal0] = 1 or [sn_check] = 0

0 = Standard SC algorithm

1 = Fast SC algorithm

sdt_mfs SDT multiframe pulse select

X = If [aal0] = 1 or [sdt] = 0 or pcfN[p_ces] = 1

0 = Start of structure is frame pulse

1 = Start of structure is multiframe pulse

sdt_oos_nr Number of SDT out of sync errors before re-initialization buffer

X = If [aal0] = 1 or [sdt] = 0

00 = Re-initialize after 1 out of sync error (recommended)

01 = Re-initialize after 2 out of sync error

10 = Re-initialize after 3 out of sync error

11 = Not allowed, IWE8 will not be able to re-initialize

sdt_par SDT pointer parity check enable

X = If [aal0] = 1 or [sdt] = 0

0 = Disabled

1 = Enabled

sdt_once SDT pointer appears once in 8 cell cycle

X = If [aal0] = 1 or [sdt] = 0

0 = All cells with CSI bit = 1 and even SN are supposed to contain a P format SAR-SDU.

1 = Only the first cell with CSI bit = 1 and even SN in a cycle of 8 cells is supposed to contain a P format SAR-SDU. (recommended for SDT)

crv_en Data to Clock Recovery interface enable (RTS values and/or ACM buffer filling levels) This bit may only be set for one channel per port.

X = if (pcfN[p_srts] = 0 and pcfN[p_acm] = 0) or acfg[a_crv_en] = 0

0 = Disabled

1 = Enabled

Only one channel per port may have crv_en set to 1.

mcp_reinit Microprocessor forced reassembly buffer reinitialization
The SW should set and reset this bit to continue proper operation.

0 = Disabled

1 = Enabled

aal0 AAL0 enable

0 = Disabled (AAL1 is used)

1 = Enabled (instead of AAL1)

part_fill Partially filled cell filling level

4 to 48 AAL0:
[aal0] = 1

4 to 47 AAL1 unstructured CES:
[aal0] = 0, pcfN[p_ces] = 1

4 to 47 AAL1 structured CES without CAS[1]:
[aal0] = 0, pcfN[p_ces] = 0, pcfN[p_cas] = 0

4+Cb to 47 AAL1 structured CES with CAS[2]:
[aal0] = 0, pcfN[p_ces] = 0, pcfN[p_cas] = 1

band_width band_width

N (with N = number of timeslots for this channel)

X = if pcfN[p_ces] = 1

sdt Structured Data Transfer enable

X = If pcfN[p_ces] = 1 or [aal0] = 1
0 = Disabled
1 = Enabled

channel_mode Channel mode

00 = Inactive mode
01 = Active mode (normal mode)
10 = Standby mode
11 = Active mode (normal mode)

ref_slot Reference slot indicator

1 = This slot is a reference slot

1) non-P format, cell may have only 46 user data octets in P format

2) Cb: Required bytes for the CAS sub-block in an ATM cell

Note: To allow IWE8 internal initialization, all channels must remain in inactive mode for at least 250 µs after activation of the port (i.e. setting pcfN[p_rx_act] = 1). During this time the device connected to the Framer Transmit Interface has to be in normal operation.

Note: If frame based SDT without CAS is used and filling level ≤ 45, the condition band_width ≤ part_fill has to be fulfilled for correct operation.
Multiframe based SDT without CAS should not be used.

6.1.2.4 RAM2: AAL Transmit Continuation Slot

Read/write Address 00400_H to $005FF_H$
Reset value: Not applicable. RAM must be reset and initialized via SW.

31							24
next_slot_nr[4:0]							Not used
23							**16**
Not used							
15							**8**
Not used							slot_index[4:0]
7							**0**
Not used	ref_slot_nr[4:0]					cont_slot = 1	ref_slot = 0

next_slot_nr Next slot number
Number of the next slot of this channel. When no continuation slots exist, the entry “next_slot_nr” should refer to the reference slot.

slot_index Index number of the current slot

X = if pcfN[p_cas] = 0

2 = 1st continuation slot
3 = 2nd continuation slot
... ...
30 = 29th continuation slot

ref_slot_nr Reference slot number
Number of the reference slot of this channel

cont_slot Continuation slot indicator

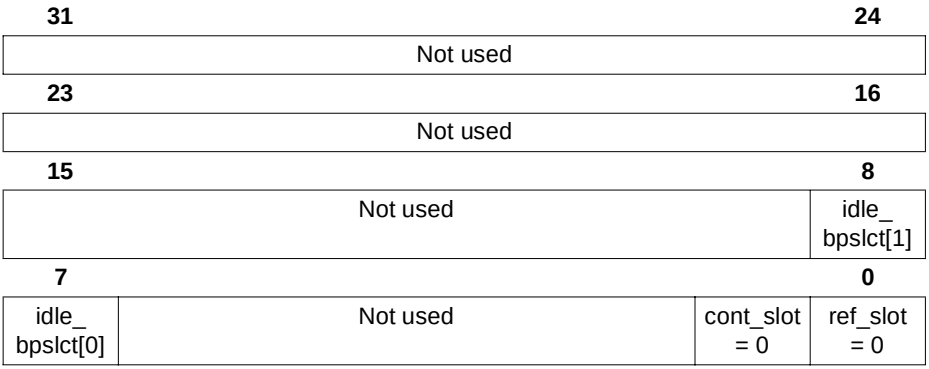
1 = This is a continuation slot

ref_slot Reference slot indicator

0 = This slot is not a reference slot

6.1.2.5 RAM2: ATM or AAL Transmit Idle Slot

Read/write Address 00400_H to $005FF_H$
Reset value: Not applicable. RAM must be reset and initialized via SW.



idle_bpslct Idle slot byte-pattern select

00 = Select byte-pattern 0, defined in bp10[bp0]

01 = Select byte-pattern 1, defined in bp10[bp1]

10 = Select byte-pattern 2, defined in bp32[bp2]

11 = Select byte-pattern 3, defined in bp32[bp3]

cont_slot Continuation slot indicator

0 = This is not a continuation slot

ref_slot Reference slot indicator

0 = This slot is not a reference slot

6.1.3 RAM3: Transmit Port Configuration Extended

Read/write Address 00600_H to $007FF_H$

Reset value: Not applicable. RAM must be reset and initialized via SW

Memory size 256K × 32 bits: 8 ports x 32 slots x 1 doubleword

MPADR

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	1	port_nr [2:0]			slot[4:0]					

RAM3 needs only to be programmed in the case of an “AAL Transmit Reference Slot’. In all other cases the RAM3 entry is don’t care.

6.1.3.1 RAM3: AAL Transmit Reference Slot

Read/write Address 00600_H to $007FF_H$

Reset value: Not applicable. RAM must be reset and initialized via SW.

31															24
Not used								starv_bpslct[1:0]		starv_ini[10:8]					
23															**16**
starv_ini[7:0]															
15															**8**
buff_lsize[13:6]															
7															**0**
buff_lsize[5:0]													auto_ reinit_of		auto_ reinit_uf

starv_bpslct Starvation byte-pattern select

00 = Select byte-pattern 0, defined in bp10[bp0]

01 = Select byte-pattern 1, defined in bp10[bp1]

10 = Select byte-pattern 2, defined in bp32[bp2]

11 = Select byte-pattern 3, defined in bp32[bp3]

starv_ini Number of starvation octets sent at reassembly buffer initialization.

0.. 2046 The actual number of starvation octets sent is starv_ini + 1

2047 An unlimited number of starvation octets will be sent

buff_lsize Logical size of reassembly buffer in octets

auto_reinit_of Automatic reassembly buffer reinitialization at overflow

X = If [aal0] =1

0 = µP controlled reassembly buffer initialization

1 = automatic reassembly buffer initialization

auto_reinit_uf Automatic reassembly buffer reinitialization at underflow

X = If [aal0] = 1

0 = µP controlled reassembly buffer initialization

1 = automatic reassembly buffer initialization

6.1.4 RAM4: Transmit Port Configuration Extended

Read/write Address 00800_H to $009FF_H$

Reset value: Not applicable. RAM must be reset and initialized via SW

Memory size 256K × 32 bits: 8 ports x 32 slots x 1 doubleword

MPADR

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	0	port_nr [2:0]			slot[4:0]					

RAM4 needs only to be programmed in the case of an “AAL Transmit Reference Slot” and in case of CAS usage. In all other cases the RAM4 entry is don’t care.

6.1.4.1 RAM4: AAL Transmit Conditioning Slot

Read/write Address 00800_H to $009FF_H$
Reset value: Not applicable. RAM must be reset and initialized via SW.

31							24
0	0	0	0	0	0	0	0
23							**16**
0	0	0	0	0	0	0	0
15							**8**
Not used							
7							**0**
Not used				cond_en	cond_down_nibble[3:0]		

cond_down_nibble CAS conditioning nibbles in downstream for the slot

cond_en Conditioning enable

0 = CAS downstream freezing enabled in underrun or pointer mismatch condition

1 = CAS downstream conditioning enabled in underrun or pointer mismatch condition

Note: Bit positions 16 to 31 are not implemented and always read as "0":

6.2 External RAM

The IWE8 requires an external 64K × 32 bit RAM. A 33th bit is added for parity.

MPADR[17:0]			RMADR[15:0]
$3FFFF_H$	64k × 16	32k × 32	$FFFF_H$
30000_H	Reassembly / ATM Transmit Buffers		8000_H
$2FFFF_H$	32k × 16	16k × 32	$7FFF_H$
28000_H	Segmentation / ATM Receive Buffers		4000_H
$27FFF_H$	8128 x 16	4064 x 32	$3FFF_H$
26040_H	Cell Extraction Buffer		3020_H
$2603F_H$	32 × 16	16 × 32	$301F_H$
26020_H	Cell Insertion Buffer		3010_H
$2601F_H$	32 × 16	16 × 32	$300F_H$
26000_H	Timers		3000_H
$25FFF_H$	8k × 16	4k × 32	$2FFF_H$
24000_H	Interrupt queue		2000_H
$23FFF_H$	8k × 16	4k × 32	$1FFF_H$
22000_H	Statistics Counter thresholds		1000_H
$21FFF_H$	8k × 16	4k × 32	$0FFF_H$
20000_H	Statistics Counters		0000_H

Figure 37 Structure of the IWE8 external RAM

6.2.1 Statistics Counters

Read/write Address 20000_H to $21FFF_H$

Reset value: Not applicable. RAM must be reset and initialized via SW

Memory size: 4K × 32 bits: 8 ports x 32 channels x 16 counters.

The statistics counters are incremented when the “channel_mode” is active or standby, and when the corresponding enable bit in the “catm” or “caal” register is set.

RMADR		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
MPADR	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	0	0	0	0	port_nr [2:0]			channel_nr[4:0]					counter_nr[3:0]				0

Table 30 Statistics Counters for ATM Ports [1)]

counter_nr	Counter contents
0 [2)]	Number of discarded cells due to output queue, ATM Receive Buffer overflow
1	Number of received cells with correctable HEC errors
2	Number of received cells with non-correctable HEC errors
3	Number of times cell delineation SYNC state is left, except when forced by the processor
4	Number of discarded cells due to ATM transmit buffer overflow
5	Number of cells which have been discarded because of CLP or CLPI
6	Not used
7	Not used
8	Not used
9	Not used
10	Not used
11	Not used
12	Not used
13	Not used
14	Not used
15	Not used

1) For ATM ports, the counters are located in channel_nr = 00000_B

2) Counter_nr 0 is common to all ports and is located in port_nr = 111_B channel_nr = 11111_B

Table 31 Statistics Counters for AAL Ports[1)]

Counter_nr	Counter contents
0 [2)]	Number of discarded cells due to Output Queue or Segmentation Buffer overflow
1	Not used
2	Number of cells written to the Reassembly Buffer. It excludes cells that were discarded for any reason and cells that are inserted instead of lost cells (atmfReassembledCells)
3	Number of times incoming MFB pulse is not synchronous to SDT start of structure upstream (AAL1)

Table 31 Statistics Counters for AAL Ports[1)] (cont'd)

4	Number of cells causing a Reassembly Buffer overflow (AAL0 & AAL1). It includes accepted cells that are causing the filling level to exceed the predefined threshold and discarded cells due to the attempt of writing to the Reassembly Buffer when the threshold is already exceeded.
5	Number of end of Reassembly Buffer overflow (AAL0 & AAL1). The value is incremented upon acceptance of the next cell after Reassembly Buffer overflow.
6	The count of the number of AAL1 header errors detected including those corrected. Header errors include correctable and uncorrectable CRC, plus bad parity. (atmfCESHdrErrors)
7	Number of times that the sequence number of an incoming AAL1 SAR-PDU causes a transition of the SC algorithm from "sync" to "out of sequence" and from "invalid" to "out of sync"
8	Number of downstream “misinserted cells” detected by the AAL1 sequence count algorithm (atmfCESMisinsertedCells)
9	Number of downstream cells discarded by the AAL1 sequence count algorithm
10	Number of rejected AAL1 SDT pointers due to parity error or wrong pointer value (93 < pointer <127)
11	Number of SC cycles with more than one AAL1 SDT pointer field if only one pointer is expected (sdt_once = 1)
12	Number of start of reassembly buffer underflow (AAL0 & AAL1) (atmfCESBufUnderflow)
13 [3)]	Number of inserted starvation cells (AAL0 & AAL1) due to reassembly buffer underflow
14	Number of times the Reassembly Buffer is re-initialized due to AAL1 start of structure is out of sync with port start of structure (see **Chapter 4.4.1.11**) This records the count of the number of events in which the AAL1 reassembler found that an SDT pointer is not where it is expected, and the pointer must be reacquired. This count is only meaningful for structured CES. (atmfCESPointerReframes)
15	Number of downstream “lost cells” detected by the AAL1 sequence count algorithm (atmfCESLostCells)

1) For AAL ports with unstructured CES, the counters are located in channel_nr = 00000_B

2) Counter_nr 0 is common for all ports and is located in port_nr = 111_B channel_nr = 11111_B

3) If the “auto-re-initialization on underflow” feature is enabled (RAM3.AAL Transmit Reference Slot.auto_reinit_uf = 1B), the re-initialization of the Reassembly Buffer will terminate an underflow status as soon as start of underflow is detected. Thus, the underflow status for the device is no longer valid although the underflow condition still exists. No starvation cells due to underflow will be inserted and counter 13 will not increment Therefore, it is recommended to disable “auto-re-initialization on underflow” (RAM3.AAL Transmit Reference Slot.auto_reinit_uf = 0B) and perform the re-initialization of the reassembly buffer by software.

The format of the counter entries is as follows:

31		24
int_gen	count_value[30:24]	
23		**16**
count_value[23:16]		
15		**8**
count_value[15:8]		
7		**0**
count_value[7:0]		

int_gen interrupt queue entry generated
Indicates if an interrupt queue entry was generated for this counter. Only one interrupt queue entry per counter can be generated.

0 = False

1 = True

count_value counter value
4000_0000_H indicates the maximum value. The counter will not increment beyond this value

6.2.2 Statistics Counter thresholds

Read/write Address 22000_H to $23FFF_H$

Reset value: Not applicable. RAM must be reset and initialized via SW

Memory size: 4K × 32 bits: 8 ports x 32 channels x 16 counter thresholds

RMADR		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
MPADR	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	0	0	0	1	port_nr [2:0]			channel_nr [4:0]					counter_nr [3:0]				0

The format of the counter threshold entries is as follows:

31															24
thres_act	thres_value[30:24]														
23															**16**
thres_value[23:16]															
15															**8**
thres_value[15:8]															
7															**0**
thres_value[7:0]															

thres_act threshold active

0 = Disabled

1 = Enabled

thres_value threshold value
Thresholds beyond 4000 0000_H will never create an interrupt queue entry as the counter stops at this value

6.2.3 Interrupt Queue

Read/write Address 24000_H to $25FFF_H$

Reset value: Not applicable. RAM must be reset and initialized via SW

Memory size: 4K × 32 bits

RMADR		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
MPADR	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	0	0	1	0	interrupt_queue_addr[11:0]												0

For reading the Interrupt Queue refer to **Chapter 4.6.3**.

Each interrupt queue entry identifies a particular statistics counter that has reached its threshold value. The format of the interrupt queue entries is as follows:

31			24
Not used			
23			**16**
Not used			
15			**8**
iq_ne	not used	port_nr [2:0]	channel_ nr[4]
7			**0**
channel_nr[3:0]		counter_nr[3:0]	

iq_ne interrupt queue not empty

0 = interrupt queue is empty, no further entries

1 = interrupt queue is not empty, further entries can be read

6.2.4 Timers

Read/write Address 26000_H to $2601F_H$

Reset value: Not applicable. RAM must be reset and initialized via SW

Memory size: 16 × 32 bits: 2 timer sets x 8 timers

RMADR		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
MPADR	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	0	0	1	1	0	0	0	0	0	0	0	0	timer_nr[3:0]				0

timer_nr[3] Timer number
Selects the timer set

0 = Timer set 2 indicated on MPIR2

1 = Timer set 1 indicated on MPIR1

timer_nr [2:0] Timer number
Number of the associated timer

The format of the timer entries is as follows:

31	24
Not used	
23	**16**
Not used	
15	**8**
timer_en	timer_value[14:8]
7	**0**
timer_value[7:0]	

timer_en Timer enable
The timer_en bit can be used by the SW to start/stop/pause the timer. Upon reaching timer_value = 0 the timer_en will be reset to 0

0 = Disabled

1 = Enabled

timer_value Timer value
When timer_en is set to 1, the timer_value will be decremented every 12 x 512 x T_{CLOCK} (245.8 µS if f_{CLOCK} = 25 MHz). The timer_value will stop at $7FFF_H$ indicated by an interrupt status bit in isr1 for timer set 1 or in isr2 for timer set 2.

Note: Internal register bit oamc[tim_set1_en] = 0 will disable all timers in set 1.
Internal register bit time[tim_set2_en] = 0 will disable all timers in set 2.

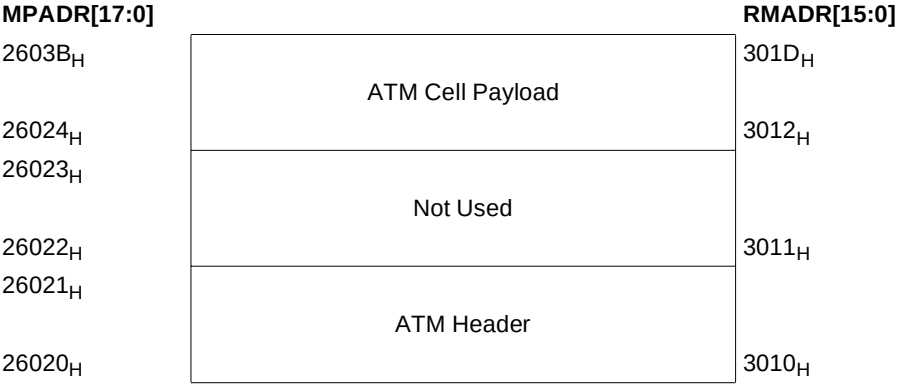
6.2.5 Cell Insertion Buffer

Read/write: Address 26020_H to $2603F_H$

Reset value: Not applicable. RAM must be reset and initialized via SW

Memory size: 16 × 32 bits: 1 cell x 16 doublewords

MPADR[17:0]		RMADR[15:0]
$2603F_H$	Not Used	$301F_H$
$2603C_H$		$301E_H$



The ATM header to be used for cell insertion has to be programmed at MPADR = 26020$_H$.

The format of the ATM Header entry is as follows:

31		24
VCI[3:0]	PTI[2:0]	CLP
23		**16**
VCI[11:4]		
15		**8**
VPI[3:0]	VCI[15:12]	
7		**0**
GFC[3:0] or VPI[11:8]	VPI[7:4]	

6.2.6 Cell Extraction Buffer

Read/write Address 26040$_H$ to 27FFF$_H$

Reset value: Not applicable. RAM must be reset and initialized via SW

Memory size: 8127 × 32 bits: 254 cells x 16 doublewords

RMADR		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
MPADR	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	0	0	1	1	cell_nr[7:0] + 2								double_word [3:0]				0

For reading the extraction buffer, refer to **Chapter 4.10**.

MPADR[17:0]		RMADR[15:0]
$27FFF_H$	Cell #254 .	$3FFF_H$
26060_H	Cell #2	3030_H
$2605F_H$	Not Used	$302F_H$
$2605A_H$		$302D_H$
26059_H	ATM Cell #1 Payload	$302C_H$
26042_H		3021_H
26041_H	ATM Cell #1 Header	
26040_H		3020_H

The format of the ATM header entry is as follows:

31		24
VCI[3:0]	PTI[2:0]	CLP
23		**16**
VCI[11:4]		
15		**8**
VPI[3:0]	VCI[15:12]	
7		**0**
GFC[3:0] or VPI[11:8]	VPI[7:4]	

6.2.7 Segmentation/ATM Receive Buffers

Read/write Address 28000_H to $2FFFF_H$

Reset value: Not applicable. RAM must be reset and initialized via SW

Memory size: 16K × 32 bits: 8 ports x 32 channels x 4 cells x 16 doublewords

RMADR		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
MPADR	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	0	1	port_nr [2:0]			channel_nr [4:0]					cell_nr [1:0]		double_word [3:0]				0

6.2.7.1 ATM Receive Buffer

The SW does not need to access the ATM Receive Buffers.

6.2.7.2 Segmentation Buffer

The ATM header to be used for each channel has to be programmed at the address given by:

RMADR		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
MPADR	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	0	1	port_nr[2:0]			ref_slot_nr[4:0]					00_B		0000_B				0

All other locations should never be accessed as the data changes continuously.

The format of the ATM header entry in the cell insertion buffer is as follows:

31		**24**
VCI[3:0]	PTI[2:0]	CLP
23		**16**
VCI[11:4]		
15		**8**
VPI[3:0]	VCI[15:12]	
7		**0**
GFC[3:0] or VPI[11:8]	VPI[7:4]	

6.2.8 Reassembly/ATM Transmit Buffers

Read/write Address 30000_H to $3FFFF_H$

Reset value: Not applicable. RAM must be reset and initialized via SW

Memory size 32K × 32 bits: 8 ports x 32 channels x 8 cells x 16 doublewords

RMADR		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
MPADR	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	1	port_nr [2:0]			channel_nr [4:0]					cell_nr [2:0]			double_word [3:0]				0

The SW does not need to access the Reassembly/ATM Transmit Buffers.

7 Register Description

The internal registers occupy the lowest addresses. Accesses to the internal registers are 16 bit oriented.

Entry size = 16 bit

Note: N = 0 .. 7

Table 32 Internal Registers

MPADR	Width	Name	Register
00000_H + N	15	pcfN	Port Configuration Register of Port N
00008_H	16	acfg	ASIC Configuration Register
00009_H	3	oamc	OAM Control Register
$0000A_H$	6	catm	OAM-Counter Enable Register for ATM Ports
$0000B_H$	16	caal	OAM-Counter Enable Register for AAL Ports
$0000C_H$	16	bp32	Byte-pattern Register 3 and 2
$0000D_H$	16	bp10	Byte-pattern Register 1 and 0
$0000E_H$	16	atmc	ATM Control Register
$0000F_H$	16	rxid	RX Idle/unassigned Cell Control Register
00010_H	16	txid	TX Idle/unassigned Cell Control Register
00011_H	9	lpbc	Loopback Control Register
00012_H	8	cfil	Cell Fill Register for Partially Filled Cells
00013_H	16	imr1	Interrupt Mask Register 1
00014_H	1	time	Timer Enable Register
00015_H	16	cdfs	Cell Delineation FSM Status Register
00016_H	9	vers	Version Register
00017_H	8	ckmo	Clock Monitor Register
00018_H	16	isr1	Interrupt Status Register 1
00019_H	2	eis1	Extended Interrupt Status Register 1
$0001A_H$	8	eis2	Extended Interrupt Status Register 2
$0001B_H$	8	eis3	Extended Interrupt Status Register 3
$0001C_H$	16	eis4	Extended Interrupt Status Register 4
$0001D_H$	8	isr2	Interrupt Status 2 Register
$0001E_H$	14	opmo	Operation Mode Register
$0001F_H$	16	ftcs	FT Clock Select Register
00020_H	16	cfvp1	Cell Filter VCI Pattern Register 1

Table 32 Internal Registers

MPADR	Width	Name	Register
00021_H	16	cfvm1	Cell Filter VCI Mask Register 1
00022_H	16	cfvp2	Cell Filter VCI Pattern Register 2
00023_H	16	cfvm2	Cell Filter VCI Mask Register 2
00024_H	12	cfpt	Cell Filter Payload Type Register
00025_H	5	cmd	Command Register
00026_H	8	cfrp	Cell Filter Read Pointer
00027_H	16	thrshld	Threshold Register
00028_H	14	utconf	UTOPIA Configuration Register
00029_H	16	cas1	CAS 1 Register
$0002A_H$	16	cas2	CAS 2 Register
$0002B_H$	4	cas3	CAS 3 Register
$0002C_H$	16	thrshp01	Threshold Register Ports 0 and 1
$0002D_H$	16	thrshp23	Threshold Register Ports 2 and 3
$0002E_H$	16	thrshp45	Threshold Register Ports 4 and 5
$0002F_H$	16	thrshp67	Threshold Register Ports 6 and 7
00030_H	16	eis0	Extended Interrupt Status Register 0
00031_H	16	lcdtimer	LCD Timer Register
00032_H- 00100_H			Unused
00101_H	11	irs	Interrupt Source Register
00102_H	11	irm	Interrupt Mask Register
00103_H	9	icrcconf	ICRC Configuration Register
00104_H+ N x 32	13	condN	Configuration Downstream Register of Port N
00105_H+ N x 32	7	irsN	Interrupt Source of Port N
00106_H+ N x 32	7	irmN	Interrupt Mask of Port N
00107_H+ N x 32	5	tsinN	Test input Register of Port N
00108_H+ N x 32	1	conuN	Configuration Upstream Register of Port N
$0010C_H$+ N x 32	14	avbN	Average Buffer Filling of Port N
$0010D_H$+ N x 32	4	asfN	ACM Shift Factor of Port N
$0010E_H$+ N x 32	13	tiniN	Time of Initial Free Run of Port N
$0010F_H$+ N x 32	12	treshN	Threshold Out Of Lock Detection of Port N
00110_H	6	per	Parity Errors at Clock Recovery Interface
00111_H	8	scri	Synchronization Errors at Clock Recovery Interface

Table 32 Internal Registers

MPADR	Width	Name	Register
00112_H	8	crifo	ICRC Clock Recovery Interface FIFO Overflow
00113_H	6	icrcv	ICRC Version Register
00114_H+ N x 32	8	sruN	SRTS FIFO Underflow of Port N
00115_H+ N x 32	8	sroN	SRTS FIFO Overflow of Port N
00116_H+ N x 32	8	srrN	SRTS Generator Reset of Port N
00117_H+ N x 32	8	sriN	SRTS Invalid Value Processed of Port N
00118_H+ N x 32	8	atlN	ACM Data Too Late of Port N
00119_H+ N x 32	3	oolN	Out of Lock Register of Port N
$0011A_H$+ N x 32	3	statN	Status Register of ICRC of Port N
$0011B_H$+ N x 32	5	tsoutN	Test Output Register of Port N

7.1 Port Configuration Registers (pcfN)

Read/write Address 00000_H + N
Reset value: 0000.

15							8
Not used	p_cell_ disc	p_thr_m[1:0]		p_cas	p_atm	p_ces	p_acm
7							**0**
p_srts	p_slp	p_ulp	p_dlp	p_rx_act	p_rx_em	p_tx_act	p_tx_mfs

p_cell_disc Port Cell Discard Enable

X = When p_atm = 0 or acfg.a_hec_mode = 0

0 = Port in IMA mode:
No cell discard upon detection of uncorrectable HEC error.
The MSB in the UDF field of the ATM cell header at UTOPIA interface will indicate the results of the HEC check

1 = Port in standard mode:
Cell discard upon detection of uncorrectable HEC error

p_thr_m Port threshold mode
This bit is relevant in ATM mode (p_atm=1) only.

00 = Port specific backpressure to UTOPIA is disabled. Entering this value causes a reset of the corresponding filling level counter. Resetting this counter during operation may result in an inappropriate backpressure.

01 = Port specific backpressure to UTOPIA is enabled
Crossing the value defined in thrspN will result in port specific backpressure. Values can range from 0 to 255 cells.

10 = Port specific backpressure to UTOPIA is enabled
Crossing the value defined in thrspN will result in port specific backpressure. The amount of bytes defining the threshold value equals 53 * C + B. With C representing the 2 most significant bits of thrspN and B representing the 6 least significant bits of thrspN. Values can range from 0 to 222 bytes.

11 = Port specific backpressure to UTOPIA is disabled

p_cas Port CAS enable

0 = Disabled

1 = Enabled

p_atm Port ATM mode

0 = AAL (CES) mode port

1 = ATM (PHY) mode port

p_ces Port circuit emulation service

X = When p_atm = 1 and for PXB 4219 version

0 = Structured (N × 64 kbit/s)

1 = Unstructured

p_acm Port ACM enable

X = When p_atm = 1

0 = Disabled

1 = Enabled

p_srts Port SRTS enable
For the PXB4220 this bit enables SRTS clock recovery. This is only useful for AAL ports in unstructured CES.
For the PXB4221 this bit is tied to "0". Writing "1" has no effect.

X = When p_atm = 1

0 = Disabled

1 = Enabled

p_slp Port serial loopback enable

0 = Disabled

1 = Enabled

p_ulp Port upstream UTOPIA loopback (works even if UTOPIA interface is disabled)

0 = Disabled

1 = Enabled

p_dlp Port downstream UTOPIA loopback

0 = Disabled

1 = Enabled

p_rx_act Port receive activate

0 = Disabled

1 = Enabled

p_rx_em Port receive emergency mode
Enables the automatic switch over to emergency mode

0 = Disabled

1 = Enabled

p_tx_act Port transmit activate

0 = Disabled (Framer outputs tristated)

1 = Enabled

p_tx_mfs Port transmit multiframe signal at pin FTMFS
E1/$\overline{T1}$ = 0:

0 = T1 Superframe mode (12 frames = 1.5 ms)

1 = T1 Extended superframe mode (24 frames = 3 ms)

E1/$\overline{T1}$ = 1:

0 = E1 Double frame mode (2 frames = 250 µs)

1 = E1 CRC multiframe mode (16 frames = 2 ms)

7.2 ASIC Configuration Register (acfg)

Read/write Address 00008_H
Reset value: 0000_H

15							8
a_icrc_dwn	a_hec_algor	a_hec_mode	a_sw_reset	a_ut_en	a_ur_en	a_crv_en	a_dummy_rts[3]

7							0
a_dummy_rts[2:0]			a_emg_bpslct[1:0]		a_ovf_cnt_en	a_ptr_prty	a_even_pck

a_icrc_dwn ICRC power down
Once the SRTS block is switched off, it can only be enabled by hardware reset of the whole device.

0 = Enabled

1 = Disabled

a_hec_algor HEC detection, correction

0 = HEC algorithm according to ITU-T

1 = HEC algorithm according to ATM Forum

a_hec_mode Handling in case of faulty HEC

0 = Standard mode:
Cell discard upon detection of uncorrectable HEC error

1 = as defined in pcfN.p_cell_disc

a_sw_reset Software reset
Reset registers 0000_H to 0031_H including this bit.

0 = Normal

1 = Reset

a_ut_en UTOPIA transmit enable

0 = Disabled

1 = Enabled

a_ur_en UTOPIA receive enable

0 = Disabled

1 = Enabled

a_crv_en Clock recovery interface enable

0 = Disabled

1 = Enabled

a_dummy_rts Dummy RTS value
Dummy RTS value that will be transmitted in the first and second SRTS period after start of segmentation.

a_emg_bpslct Emergency byte-pattern select

00 = Byte-pattern 0, defined in bp10[bp0] selected

01 = Byte-pattern 1, defined in bp10[bp1] selected

10 = Byte-pattern 2, defined in bp32[bp2] selected

11 = Byte-pattern 3, defined in bp32[bp3] selected

a_ovf_cnt_en Output queue overflow counter enable

0 = Disabled

1 = Enabled

a_ptr_prty SDT pointer even parity generation

0 = Disabled: Fixed value in bit 7 of pointer field: “0”.

1 = Enabled (recommended)

a_even_pck Even parity check for internal/external RAM and UTOPIA

0 = Odd parity check enabled (default operation)
The parity checkers expect the normal parity.

1 = Even parity check enabled
The parity checkers expect the inverse parity. This mode tests the proper operation of the parity generators/checkers.

7.3 OAM Control Register (oamc)

Read/write Address 00009_H
Reset value: 0000_H

15							8
Not used							
7							**0**
Not used					tim_ set1_en	dest_ read	oam_ act

tim_set1_en Timer set 1 enable

0 = Disabled

1 = Enabled

dest_read Destructive read mode

0 = Disabled

1 = Enabled: OAM counter values in the external RAM are reset after being read by the micro-processor.
(Only accepted if “oam_act” = 1)

oam_act OAM active

0 = The protocol monitoring is disabled and the microprocessor can read and write the complete external RAM for test.

1 = The protocol monitoring is enabled and the RAM arbiter grants both the protocol monitoring and the microprocessor access to the external RAM. Reading any address of Interrupt Queue by the microprocessor always yields the first interrupt in the queue.

7.4 OAM-Counter Enable Register for ATM Ports (catm)

Read/write Address $0000A_H$
Reset value: 0000_H

15							8
Not used							

7	5	0
Not used	cnt_atm_en[5:0]	

cnt_atm_en OAM-counter enable for ATM ports

X = When pcfN[p_atm] = 0

0 = Disabled

1 = Enabled

7.5 OAM-Counter Enable Register for AAL Ports (caal)

Read/write Address $0000B_H$
Reset value: 0000_H

15	8
cnt_aal_en[15:8]	
7	**0**
cnt_aal_en[7:0]	

cnt_aal_en OAM-counter enable for AAL ports

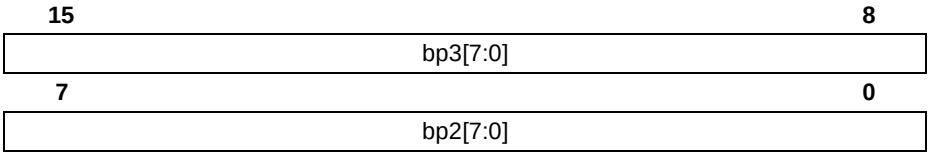
X = When pcfN[p_atm] = 1

0 = Disabled

1 = Enabled

7.6 Byte-Pattern Register bp3 and bp2 (bp32)

Read/write Address $0000C_H$
Reset value: $FFFF_H$

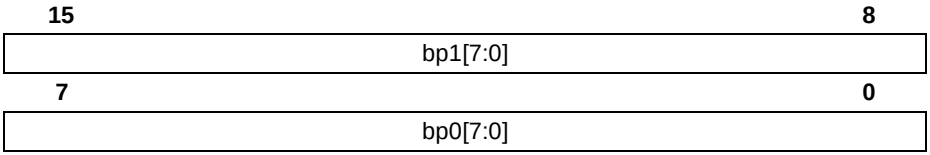


bp3 Byte-pattern 3

bp2 Byte-pattern 2

7.7 Byte-Pattern Register bp1 and bp0 (bp10)

Read/write Address $0000D_H$
Reset value: $FFFF_H$

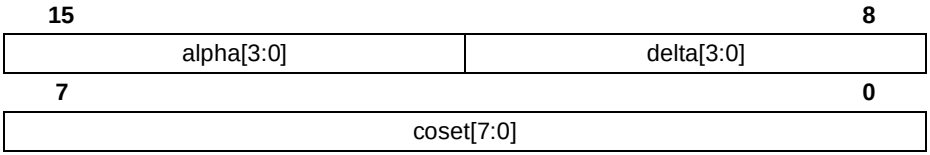


bp1 Byte-pattern 1

bp0 Byte-pattern 0

7.8 ATM Control Register (atmc)

Read/write Address $0000E_H$
Reset value: 7655_H



alpha Number of consecutive incorrect HEC (SYNC → HUNT)

delta Number of consecutive correct HEC (PRESYNC → SYNC)

coset Coset value x-ored with HEC

7.9 RX Idle/Unassigned Cell Control Register (rxid)

Read/write Address $0000F_H$
Reset value: 0101_H

15	8
prg_rx_hd[7:4]	prg_rx_hd[3:0]

7	0
msk_rx_hd[7:0]	

prg_rx_hd Programmable RX idle/unassigned cell header octet 1[7:4]
00_H according to I.361

prg_rx_hd Programmable RX idle/unassigned cell header octet 4[3:0]
01_H according to I.361

msk_rx_hd Mask RX idle/unassigned cell header bits
Each bit masks the corresponding bit in prg_rx_hd

0 = Not masked:

1 = Masked

Note: Other header bits must be zero

7.10 TX Idle/Unassigned Cell Control Register (txid)

Read/write Address 00010_H
Reset value: $016A_H$

15	8
prg_tx_hd[7:4]	prg_tx_hd[3:0]

7	0
prg_tx_pl[7:0]	

prg_tx_hd Programmable TX idle/unassigned cell header octet 1[7:4] 00_H according to I.361

prg_tx_hd Programmable TX idle/unassigned cell header octet 4[3:0] 01_H according to I.361

prg_tx_pl Programmable TX idle/unassigned cell payload octet $6A_H$ according to I.432

Note: Other header bits are fixed to zero

7.11 Loopback Control Register (lpbc)

Read/write Address 00011_H
Reset value: 0000_H

15							8
Not used							tslp
7							**0**
tulp	tdlp	vci_flt_ulp	vci_val_ulp[4:0]				

tslp Transparent serial loop
0 = Non-transparent
1 = Transparent

tulp Transparent upstream UTOPIA loop
X = When pcfN[p_atm] = 1
0 = Non-transparent
1 = Transparent

tdlp Transparent downstream UTOPIA loop
0 = Non-transparent
1 = Transparent

vci_flt_ulp VCI filter enable for upstream UTOPIA loop
0 = Disabled (all VCIs are looped)
1 = Enabled (VCI selected by vci_val_ulp is looped)

vci_val_ulp 5 LSB of the VCI value (i.e. channel number) to be looped on upstream UTOPIA loop

Note: Transparent loop: Data is looped and forwarded.
Non-transparent loop: Data is looped.

Note: For ATM ports with upstream UTOPIA loopback (pcfN[p_atm] = 1 and pcfN[p_ulp] = 1), all cells are looped regardless of their VCI value. The vci_flt_ulp and vci_val_ulp[4:0] bits are don't care.

7.12 Cell Fill Register for Partially Filled Cells (cfil)

Read/write Address 00012_H
Reset value: 0000_H

15	8
Not used	

7	0
cfil[7:0]	

cfil Dummy fill octet for partially filled cells

7.13 Interrupt Mask Register 1 (imr1)

Read/write Address 00013_H
Reset value: $FFFF_H$

15							8
imr1[15:8]							
7							**0**
imr1[7:0]							

imr1 Each bit masks the corresponding bit in isr1
0 = Not masked
1 = Masked

7.14 Timer Enable Register (time)

Read/write Address 00014_H
Reset value: 0000_H

15							8
Not used							
7							**0**
Not used							tim_set2_en

tim_set2_en Timer set 2 enable
0 = Disabled
1 = Enabled

7.15 Cell Delineation FSM Status Register (cdfs)

Read only Address 00015_H
Reset value: 0000_H

15			8
status_p7[1:0]	status_p6[1:0]	status_p5[1:0]	status_p4[1:0]
7			**0**
status_p3[1:0]	status_p2[1:0]	status_p1[1:0]	status_p0[1:0]

status_pN Cell Delineation FSM status of port N

XX = When pcfN[p_atm] = 0

00 = Hunt

01 = Presync

10 = Sync

7.16 Version Register (vers)

Read only Address 00016_H

15			9	8
Not used				mtypsel
7				**0**
ec	e1/t1	version[5:0]		

mtypsel Microcontroller type select
0 = Microcontroller Interface runs in Intel Mode
1 = Microcontroller Interface runs in Motorola Mode

ec Status of $\overline{EC}$ pin
0 = Echo Cancellation mode(EC)
1 = Normal operation mode

e1/t1 Status of E1/$\overline{T1}$ pin
0 = T1 mode
1 = E1 mode

version Version of IWE8
Value of $011\ 010_B$ for Version 3.2
Value of $011\ 011_B$ for Version 3.3
Value of $011\ 100_B$ for Version 3.4

7.17 Clock Monitor Register (ckmo)

Read only Address 00017_H
Reset value: 0000_H

15	8
Not used	

7	0
frclk_failure[7:0]	

frclk_failure FRCLK clock failure on port N
Bit remains active only as long as a clock failure on FRCLK is detected.

0 = False

1 = True

7.18 Interrupt Status Register 1 (isr1)

Read only, Address 00018_H
Reset value: 0000_H

15							8
iq_ne	eis4	eis3	eis2	eis1	eis0	Not used	

7							0
Not used	ut_soc	ut_par	ex_par	crv_par	oq_ovf	eq_ovf	ck_eme

iq_ne Interrupt queue not empty
0 = False
1 = True

eis4 A bit is set in eis4
0 = False
1 = True

eis3 A bit is set in eis3
0 = False
1 = True

eis2 A bit is set in eis2
0 = False
1 = True

eis1 A bit is set in eis1
0 = False
1 = True

eis0 A bit is set in eis0
0 = False
1 = True

ut_soc UTOPIA start of cell error,
indicates if SOC is activated too late or twice within one cell cycle. (corresponds to transmit direction in slave mode and receive direction in master mode).
0 = False
1 = True

ut_par Parity error on UTOPIA bus

ex_par Parity error on external RAM
In order to prevent external RAM parity errors, the external RAM should be written completely during board initialization by the microprocessor.

0 = False

1 = True

crv_par Parity error on clock recovery interface

0 = False

1 = True

oq_ovf Output queue overflow

0 = False

1 = True

eq_ovf Error queue overflow

0 = False

1 = True

ck_eme Emergency mode state change on one of the emergency mode enabled ports (see ckmo)

0 = False

1 = True

Note: Bits 6:0 are used for tracing error events. They are set on the occurrence of an error event and reset by a microprocessor read operation.
Bits 15:10 Bits are reset upon reading of the interrupt generating register.

7.19 Extended Interrupt Status 1 Register (eis1)

Destructive read Address 00019_H
Reset value: 0000_H

15							8
Not used							
7							**0**
Not used						cf_fifo_ n_empty	cf_fifo_ full

cf_fifo_full Cell filter FIFO full
0 = False
1 = True

cf_fifo_n_ empty Cell filter FIFO not empty
0 = False
1 = True

7.20 Extended Interrupt Status 2 Register (eis2)

Destructive read Address $0001A_H$
Reset value: 0000_H

15	8
Not used	

7	0
rts_overflow[7:0]	

rts_overflow RTS buffer overflow of IWE core at port N
Applicable for AAL ports in unstructured CES mode with SRTS.

X = When pcfN[p_atm] = 1 or pcfN[p_ces] = 0 or pcfN[p_srts] = 0

0 = False

1 = True

7.21 Extended Interrupt Status 3 Register (eis3)

Destructive read Address $0001B_H$
Reset value: 0000_H

15	8
Not used	
7	**0**
tim_set1_exp[7:0]	

tim_set1_exp Timer of set 1 expired
Each bit indicates if the corresponding timer expired
0 = False
1 = True

7.22 Extended Interrupt Status 4 Register (eis4)

Destructive read Address $0001C_H$
Reset value: 0000_H

15	8
ocd_end[7:0]	
7	**0**
ocd_start[7:0]	

ocd_end End of OCD (Out of cell delineation) state at port N
- X = When pcfN[p_atm] = 0
- 0 = False
- 1 = True

ocd_start Start of OCD (Out of cell delineation) state at port N
- X = When pcfN[p_atm] = 0
- 0 = False
- 1 = True

7.23 Interrupt Status Register 2 (isr2)

Destructive read Address $0001D_H$
Reset value: 0000_H

15	8
Not used	
7	**0**
tim_set2_exp[7:0]	

tim_set2_exp Timer of timer set 2 expired
Each bit indicates if the corresponding timer expired
0 = False
1 = True

7.24 Operation Mode Register (opmo)

Read/write Address $0001E_H$

Reset value 1100_H

15						8
Not used		symn	rts_gen	rts_eval	bufthr[3:1]	
7						**0**
bufthr0	tfpp	rfpp	ftri	frri	om[1:0]	cbb

symn SYMn mode
This bit is relevant only in SYM2 and SYM8

0 = FRMFB[0] is used for frame and multiframe synchronization in receive and transmit direction of all ports. FRMFB[1:7] are unused

1 = FRMFB[N] is used for frame and multiframe synchronization in receive and transmit direction of corresponding ports

rts_gen RTS generation

0 = Pin SDI is used for RTS

1 = RTS data are generated by ICRC

rts_eval RTS evaluation

0 = Pins FTCKO are used as transmit clock (*all* FTCKO[0:7] are input pins)

1 = Clock of ICRC is used as transmit clock and is also switched to FTCKO pins (FTCKO[0:7] *all* are output pins)

bufthr Buffer threshold
Determines the threshold for the ATM Transmit Buffer. If the buffer level remains under the threshold the signal ATBTC will be activated.

tfpp Transmit frame pulse polarity
valid for GIM

0 = FTMFS is active low

1 = FTMFS is active high

rfpp Receive frame pulse polarity
valid for GIM, SYM8 and SYM2

0 = FRMFB is active low

1 = FRMFB is active high

ftri Framer transmit rising edge
valid for GIM

0 = FTDAT outputs are clocked with the falling edge of FTCKO

1 = FTDAT outputs are clocked with the rising edge of FTCKO

frri Framer receive rising edge
valid for GIM:

0 = FRDAT inputs are sampled with the falling edge of FRCLK

1 = FRDAT inputs are sampled with the rising edge of FRCLK

valid for SYM2:

0 = FRDAT inputs are sampled with the falling edge of RFCLK
FTDAT outputs are clocked with the rising edge of RFCLK

1 = FRDAT inputs are sampled with the rising edge of RFCLK
FTDAT outputs are clocked with the falling edge of RFCLK

om Operation Mode

00 = FAM: FALC mode
FTCKO and FRCLK running at 8.192 MHz

01 = GIM: Generic Interface mode[1)]
FTCKO and FRCLK running at 2.048 (E1) or 1.544 (T1) MHz

10 = SYM8: E1 synchronous mode (RFCLK = 8.192 MHz)

11 = SYM2: E1 synchronous mode (RFCLK = 2.048 MHz)

cbb Clock Boost Bypass

0 = Normal operation: the external clock at RFCLK in internally doubled to serve as reference clock for the internal DPLL

1 = Clock boost function bypassed

1) Make sure that no clocks are applied to the transmitter when switching to GIM.

7.25 FT Clock Select Register (ftcs)

Read/write Address $0001F_H$
Reset value 0000_H

15			8
ftck7[1:0]	ftck6[1:0]	ftck5[1:0]	ftck4[1:0]
7			**0**
ftck3[1:0]	ftck2[1:0]	ftck1[1:0]	ftck0[1:0]

$ftck_i$ Clock Source for framer transmit interface
valid for FAM and GIM

00 = $FTCKO_i$ if opmo[rts_eval]=0
Recovered Clock of ICRC if opmo[rts_eval] = 1

01 = $FRCLK_i$ (opmo[rts_eval] = 1 is required)

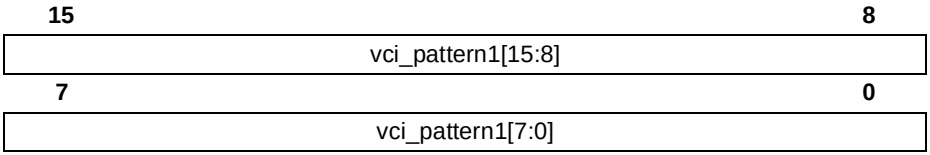
10 = Derived from RFCLK (opmo[rts_eval] = 1 is required)

11 = No clock

Note: Register opmo has to be set before ftcs is configured.

7.26 Cell Filter VCI Pattern 1 Register (cfvp1)

Read/write Address 20_H
Reset value: 0000_H



vci_pattern1 First VCI pattern the cell header is compared with.

7.27 Cell Filter VCI Mask 1 Register (cfvm1)

Read/write Address 00021_H
Reset value: 0000_H

15							8
vci_mask1[15:8]							
7							**0**
vci_mask1[7:0]							

vci_mask1 Each bit masks the corresponding bit in cfvp1

0 = Not masked

1 = Masked

7.28 Cell Filter VCI Pattern 2 Register (cfvp2)

Read/write Address 00022_H
Reset value: 0000_H

15	14	13	12	11	10	9	8
vci_pattern2[15:8]							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
vci_pattern2[7:0]							

vci_pattern2 Second VCI pattern the cell header is compared with.

7.29 Cell Filter VCI Mask 2 Register (cfvm2)

Read/write Address 00023_H
Reset value: 0000_H

15							8
vci_mask2[15:8]							
7							**0**
vci_mask2[7:0]							

vci_mask2 Each bit masks the corresponding bit in cfvp2

0 = Not masked

1 = Masked

7.30 Cell Filter Payload Type Register (cfpt)

Read/write Address 00024_H
Reset value: 0000_H

15			8
Not used		pt_pattern2[2:0]	pt_mask 2[2]

7		0
pt_mask2[1:0]	pt_pattern1[2:0]	pt_mask1[2:0]

pt_mask1 Each bit masks the corresponding bit in pt_pattern1.
0 = Not masked
1 = Masked

pt_pattern1 First PT pattern the cell header is compared with.

pt_mask2 Each bit masks the corresponding bit in pt_pattern2.
0 = Not masked
1 = Masked

pt_pattern2 Second PT pattern the cell header is compared with.

7.31 Command Register (cmd)

Read/write Address 00025_H
Reset value 0000_H

15					8
Not used					
7					**0**
Not used	insert_ cell	pt2_ comp	pt1_ comp	vci2_ comp	vci1_ comp

vci1_comp VCI comparison corresponding to register cfvp1 and cfvm1.
0 = Disabled
1 = Enabled

vci2_comp VCI comparison corresponding to register cfvp2 and cfvm2.
0 = Disabled
1 = Enabled

pt1_comp PT comparison corresponding to fields pt_pattern1 and pt_mask1 in register cfpt.
0 = Disabled
1 = Enabled

pt2_comp PT comparison corresponding to fields pt_pattern2 and pt_mask2 in register cfpt.
0 = Disabled
1 = Enabled

insert_cell Cell insertion via microprocessor.
A cell will be inserted in the data stream as soon as possible; when finished this bit will be reset.
0 = Disabled
1 = Enabled

7.32 Cell Filter Read Pointer Register (cfrp)

Read/write Address 00026_H
Reset value 0002_H

15	8
Not used	
7	**0**
rdptr[7:0]	

rdptr Read Pointer for the Cell Extraction Buffer

02_H to FF_H	This value is a pointer to the current address, at which the microprocessor will read the next extracted cell from the Cell Extraction Buffer

7.33 Threshold Register (thrshld)

Read/write Address 00027_H
Reset value $00FF_H$

15	8
Not used	
7	**0**
threshold[7:0]	

threshold Global ATM transmit buffer threshold for discarding cells

00_H to FF_H If the amount of cells stored in the ATM transmit buffer crosses this value cells will be discarded.

7.34 UTOPIA Configuration Register (utconf)

Read/write Address 00028_H
Reset value 0001_H

15			8
Not used	utrange[2:0]	utprtyen	utbaseadr[4:3]

7			0
utbaseadr[2:0]	utlevel	utmaster	mapping_mode[2:0]

utrange UTOPIA Port Range
Controls the supported port range if the device is configured as UTOPIA level 2 PHY-Layer (utlevel=0, utmaster=0, mapping_mode=000_B)

000 = Ports 0 to 7 enabled
001 = Port 0 enabled
010 = Ports 0 and 1 enabled
011 = Ports 0 to 2 enabled
100 = Ports 0 to 3 enabled
101 = Ports 0 to 4 enabled
110 = Ports 0 to 5 enabled
111 = Ports 0 to 6 enabled

utprtyen UTOPIA parity check enable

0 = Disabled
1 = Enabled

utbaseadr UTOPIA base address
Defines the base address under which the PHY-Layer is accessible. User has to set this value to 0 if device utlevel = 1.

utlevel UTOPIA interface level
In Master mode only UTOPIA level 1 is available.

0 = UTOPIA level 2
1 = UTOPIA level 1

utmaster UTOPIA Slave/Master configuration

0 = Slave mode (PHY-Layer)
1 = Master mode (ATM-Layer)

mapping_mode Mapping of the “port_nr” associated with the currently transferred cell into the UTOPIA datastream

- 000 = Disabled
- 001 = Mapping to UDF[2:0] field in ATM header
- 010 = Mapping toVCI[7:5] field in ATM header
- 011 = Mapping toVCI[15:13] field in ATM header
- 100 = Mapping toVPI[7:5] field in ATM header
- 101 = Mapping toGFC[3:1] field in ATM header

7.35 CAS 1 Register (cas1)

Read/write Address 00029_H
Reset value: $BBBB_H$

15			8
cas0port3[3:0]		cas0port2[3:0]	
7			**0**
cas0port1[3:0]		cas0port0[3:0]	

cas0port0 E1 CAS frame 0 pattern for port 0 (unused in T1 mode)

cas0port1 E1 CAS frame 0 pattern for port 1 (unused in T1 mode)

cas0port2 E1 CAS frame 0 pattern for port 2 (unused in T1 mode)

cas0port3 E1 CAS frame 0 pattern for port 3 (unused in T1 mode)

7.36 CAS 2 Register (cas2)

Read/write Address $0002A_H$
Reset value: $BBBB_H$

15		8
cas0port7[3:0]	cas0port6[3:0]	
7		**0**
cas0port5[3:0]	cas0port4[3:0]	

cas0port4 E1 CAS frame 0 pattern for port 4 (unused in T1 mode)

cas0port5 E1 CAS frame 0 pattern for port 5 (unused in T1 mode)

cas0port6 E1 CAS frame 0 pattern for port 6 (unused in T1 mode)

cas0port7 E1 CAS frame 0 pattern for port 7 (unused in T1 mode)

7.37 CAS 3 Register (cas3)

Read/write Address $0002B_H$
Reset value: $000D_H$

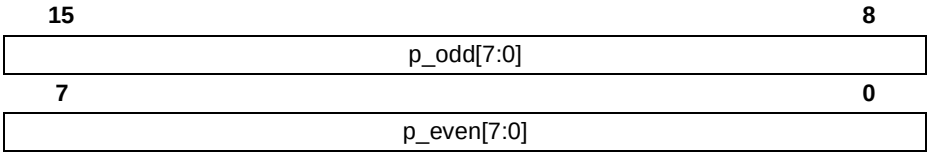
15							8
Not used							
7							**0**
Not used							cas_idle

cas_idle CAS idle pattern for unused timeslots of the Tx frame

7.38 Threshold Register for Ports 0 and 1 (thrsp01)

Read/write Address $0002C_H$

Reset value: $FFFF_H$



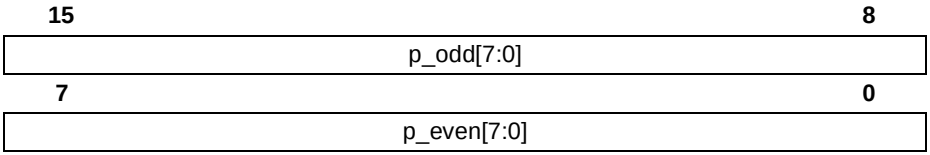
p_odd Port 1 threshold for backpressure of UTOPIA Tx

p_even Port 0 threshold for backpressure of UTOPIA Tx

7.39 Threshold Register for Ports 2 and 3 (thrsp23)

Read/write Address $0002D_H$

Reset value: $FFFF_H$



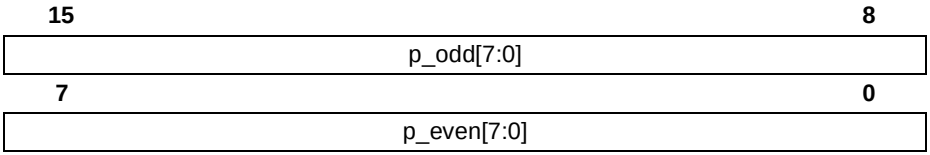
p_odd Port 3 threshold for backpressure of UTOPIA Tx

p_even Port 2 threshold for backpressure of UTOPIA Tx

7.40 Threshold Register for Ports 4 and 5 (thrsp45)

Read/write Address $02E_H$

Reset value: $FFFF_H$



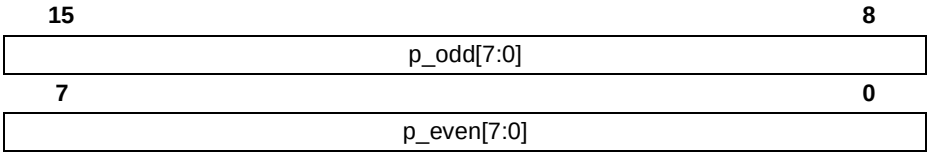
p_odd Port 5 threshold for backpressure of UTOPIA Tx

p_even Port 4 threshold for backpressure of UTOPIA Tx

7.41 Threshold Register for Ports 6 and 7 (thrsp67)

Read/write Address $0002F_H$

Reset value: $FFFF_H$



p_odd Port 7 threshold for backpressure of UTOPIA Tx

p_even Port 6 threshold for backpressure of UTOPIA Tx

7.42 Extended Interrupt Status 0 Register (eis0)

Destructive Read Address 00030_H

Reset value: 0000_H

15	14	13	12	11	10	9	8
lcd_end[7:0]							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
lcd_start[7:0]							

lcd_end End of LCD detect on port N

0 = False

1 = True

lcd_start Start of LCD detect on port N

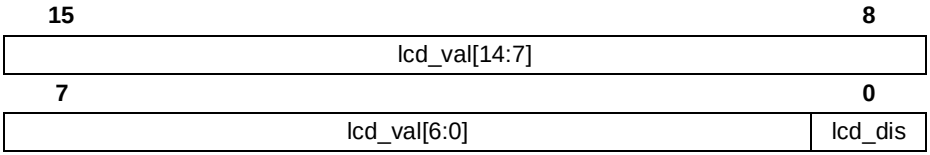
0 = False

1 = True

7.43 LCD Timer Register (lcdtimer)

Read/write Address 00031H

Reset value: $FFFF_H$



lcd_val LCD timer preload value
The port specific LCD timer is pre-loaded with 128 * lcd_val and clocked with CLOCK. After expiration an interrupt is issued in eis0.

lcd_dis LCD timer disable

0 = Enabled

1 = Disabled

7.44 Interrupt Source Register (irs)

Read only Address 00101_H
Reset value: 0000_H

15							8
Not used					irs7	irs6	irs5
7							**0**
irs4	irs3	irs2	irs1	irs0	crifo	scri	per

irsN IRS register of port N
These bits indicate if a bit is set in irsN
0 = False
1 = True

crifo Clock recovery interface FIFO overflow
This bit indicates if a bit is set in crifo
0 = False
1 = True

scri Synchronization errors at the internal clock recovery interface
This bit indicates if a bit is set in scri
0 = False
1 = True

per Parity errors at the clock recovery interface.
This bit indicates if a bit is set in per
0 = False
1 = True

Bits are reset after reading the corresponding registers.

7.45 Interrupt Mask (irm)

Read/Write Address 00102_H
Reset value: $07FF_H$

15							8
Not used					irm7	irm6	irm5
7							**0**
irm4	irm3	irm2	irm1	irm0	crifo	scri	per

irmN Each bit masks the corresponding irsN in irs
0 = Not masked
1 = Masked

crifo This bit masks the bit crifo in irs
0 = Not masked
1 = Masked

scri This bit masks the bit scri in irs.
0 = Not masked
1 = Masked

per This bit masks the bit per in irs
0 = Not masked
1 = Masked

7.46 Internal Clock Recovery Circuit Configuration Register (icrcconf)

Read/Write Address 00103_H
Reset value: 0020_H

15							8
Not used							gim
7							**0**
ds1	parc	pdcri	srst	lptd	lptu	lprd	lpru

gim Generic interface mode

0 = FAM: 8.192 MHz is expected/generated.

1 = GIM: 2.048 MHz (E1) or 1.544 MHz (T1) expected/generated.

ds1 DS1 Mode

0 = E1: The receive clocks are divided to 2.048 MHz. Output clocks are 8.192 MHz in case of FAM or 2.048 MHz in case of GIM.

1 = T1: The receive clocks are divided to 1.544 MHz. Output clocks are 8.192 MHz in case of FAM or 1.544 MHz in case of GIM.

parc Parity Check
Inverts all parity bits in the ICRC. All enabled parity checkers will generate interrupts

0 = Disabled

1 = Enabled

pdcri Power Down Clock Recovery Interface

0 = Normal operation

1 = The internal clock recovery interface is put in power down mode. No data is received, no errors are generated and the parity check is disabled.

srst Software Reset
The bit srst is set by the software, but reset by the ICRC. Reading this bit will always give the Reset value: “0”.

0 = Normal operation

1 = Reset ICRC

lptd Loop back clock recovery interface transmitted data downstream

0 = Disabled

1 = Enabled

lptu Loop back clock recovery interface transmitted data upstream

0 = Disabled

1 = Enabled

lprd Loop back clock recovery interface received data downstream

0 = Disabled

1 = Enabled

lpru Loop back clock recovery interface received data upstream

0 = Disabled

1 = Enabled

7.47 Configuration Register Downstream of Port N (condN)

Read/Write Address 00104_H + N x 32

Reset value: 0840_H

15							8
not used			tur[5:1]				
7							**0**
tur(0]	pwd	lgc	lc8	lgs	lpcr	srt	acm

tur Tuning range select of port N
The tuning range of PLL-ACM is limited to:
(frequency deviation of pin RFCLK in ppm) +/- ((4*tur) +/-5%)ppm.

pwd Power down of port N

0 = Normal operation

1 = Power down mode. No RTS values and no transmit clock are generated.

lgc Loop back generated clock

0 = Normal operation

1 = The clock generated by the PLL is looped into the RTS generator.

lc8 Loop back clock 8.192 MHz

0 = Normal operation

1 = The receive clock is looped to the transmit output of the ICRC.

lgs Loop back generated RTS

0 = Normal operation

1 = Generated RTS values are looped into the SRTS Receive FIFO.

lpcr Loop back clock recovery Interface

0 = Normal operation

1 = The clock recovery interface is bypassed. RTS values from the frame receiver are looped into the SRTS Transmit FIFO.

srt, acm Selectors for the clock generation algorithm

00 = The PLL is put in power down mode, and a free running clock is generated. In case pwd is set, all circuits of the port, including the RTS generator are disabled, no output clock is generated and all error counters are reset.

01 = Transmit clock generation of this port is based on the adaptive clock algorithm

10 = Transmit clock generation of this port is based on the SRTS algorithm.

11 = Transmit clock generation of this port is based on both algorithms. The tuning range of PLL-ACM can not be reduced (tur), because PLL-ACM has to accept the jitter passed through or generated in PLL-SRTS.

7.48 Interrupt Source of Port N (irsN)

Read only Address 00105_H + N x 32

Reset value: 0000_H

15							8
not used							
7							**0**
not used	srrn	tsoutn	srun	sron	srin	atln	ooln

srrn A bit is set in srrn.
0 = False
1 = True

tsoutn A bit is set in tsoutN.
0 = False
1 = True

srun A bit is set in sruN
0 = False
1 = True

sron A bit is set in sroN.
0 = False
1 = True

srin A bit is set in sriN.
0 = False
1 = True

atln A bit is set in atlN.
0 = False
1 = True

ooln A bit is set in oolN.
0 = False
1 = True

Bits are reset upon reading of the interrupt generating register.

7.49 Interrupt Mask of Port N (irmN)

Read/Write Address 00106_H + N x 32

Reset value: $007F_H$

15							8
not used							
7							**0**
not used	srrn	tsoutn	srun	sron	srin	atln	ooln

srrn This bit masks the bit srrN in irsN
0 = Not masked
1 = Masked

tsoutn This bit masks the bit tsoutN in irsN
0 = Not masked
1 = Masked

srun This bit masks the bit sruN in irsN.
0 = Not masked
1 = Masked

sron This bit masks the bit sroN in irsN
0 = Not masked
1 = Masked

srin This bit masks the bit sriN in irsN
0 = Not masked
1 = Masked

atln This bit masks the bit atlN in irsN
0 = Not masked
1 = Masked

ooln This bit masks the bit oolN in irsN
0 = Not masked
1 = Masked

7.50 Test Input of Port N (tsinN)

Read/Write Address 00107_H + N x 32

Reset value: 0000_H

15		8
not used		

7		0
not used	rtsi[3:0]	ena

rtsi RTS Input value of port N

ena Test Input Enable
Disconnect the RTS generator from the transmit FIFO. Each write command to this register injects the value rtsi into the transmit FIFO.

0 = Disabled

1 = Enabled:

Successive writes to this register should have a minimum distance of 8 x 32 x T_{CLOCK}. This is the (maximum) time needed to transmit the value rtsi to the clock recovery. In case bit lgs of register condN is set, this waiting time is not necessary.

7.51 Configuration Register Upstream Direction of Port N (conuN)

Read/Write Address 00108_H + N x 32

Reset value: 0000_H

15	8
not used	

7	0
not used	rtsg

rtsg RTS generator enable

0 = Disabled

1 = Enabled

7.52 Average Buffer Filling of Port N (avbN)

Read/Write Address $0010C_H$ + N x 32

Reset value: 2000_H

15	8
not used	avb[13:8]
7	**0**
avb[7:0]	

avb Average buffer filling of port N
This field defines the number of bytes ACM should try to keep in the data buffer of the clock recovery. This value should correspond with the number of bytes the clock recovery initially stores in the data buffer.

7.53 ACM Shift Factor of Port N (asfN)

Read/Write Address $0010D_H$ + N x 32

Reset value: 0000_H

15			8
not used			
7			**0**
not used	dir	ampl[2:0]	

dir Direction of shifting

0 = shift left = amplification

1 = shift right = attenuation

ampl Amplitude of shifting
This defines the loop-gain of PLL-ACM. It is equivalent to a multiplication with (or a division by) 2^{ampl}.

7.54 Time of Initial Free Run of Port N (tiniN)

Read/Write Address $0010E_H$ + N x 32

Reset value: 0400_H

15	8
not used	tini[12:8]
7	**0**
tini[7:0]	

tini[12:0] Time of initial free run of port N

7.55 Threshold Out of Lock Detection of Port N (tresh)

Read/Write Address $0010F_H$ + N x 32

Reset value: 0111_H

15	8
not used	tr_filt[3:0]
7	**0**
tr_srts[3:0]	tr_acm[3:0]

tr_filt Threshold for out of lock detection of PLL-FILTER
If more than tr_filt out of lock detections during 16 SRTS periods (128 ATM cells) are made, oolN[olf] is set

tr_srts Threshold for out of lock detection of PLL-SRTS
If more than tr_srts out of lock detections during 16 SRTS periods (128 ATM cells) are made, oolN[ols] is set

tr_acm Threshold for out of lock detection of PLL-ACM
If more than tr_acm out of lock detections during 16 ATM cells are made, oolN[ola] is set.

7.56 ICRC Parity Errors at Clock Recovery Interface (per)

Destructive read Address 00110_H
Reset value: 0000_H

15							8
perd[7:0]							
7							**0**
peru[7:0]							

perd Parity Errors at the Clock Recovery Interface Downstream Pin SDOD
This field counts the amount of parity errors at the internal clock recovery interface. In case there are more than 255 errors, the value is kept

peru Parity Errors at the Clock Recovery Interface Upstream Pin SDI
This field counts the amount of parity errors at the internal clock recovery interface. In case there are more than 255 errors, the value is kept

Note: A synchronization error (scri) generates a random number of parity errors

7.57 ICRC Synchronization Errors at Clock Recovery Interface (scri)

Destructive read Address 00111_H
Reset value: 0000_H

15	8
not used	

7	0
scri[7:0]	

scri Synchronization Error at the Clock Recovery Interface
This field counts the amount of synchronization errors at the internal clock recovery interface. In case there are more than 255 errors, the value is kept

Note: A synchronization error (scri) generates a random number of parity errors (per)

7.58 ICRC Clock Recovery Interface FIFO Overflow (crifo)

Destructive read Address 00112_H

Reset value: 0000_H

15	8
not used	
7	**0**
crifo[7:0]	

crifo Clock Recovery Interface FIFO Overflow
This field counts the number of times the SRTS transmit FIFO overflows. In case there are more than 255 errors, the value is kept

7.59 ICRC Version Register (icrcv)

Read only Address 00113_H
Reset value: 0034_H

15			8
not used			
7			**0**
not used	ver[2:0]		rel[2:0]

ver Version Number

rel Release Number

Note: The version and release number are defined as: IWE8 V<ver>.<rel>

7.60 SRTS Receive FIFO Underflow of Port N (sruN)

Destructive read Address 00114_H + N x 32

Reset value: 0000_H

15	8
not used	
7	**0**
sru[7:0]	

sru SRTS Receive FIFO underflow of port N
This field counts the amount of underflows of the SRTS Receive FIFO. Upon reaching FF_H it keeps its value.

7.61 SRTS Receive FIFO Overflow of Port N (sroN)

Destructive read Address 00115_H + N x 32

Reset value: 0000_H

15	8
not used	
7	**0**
sro[7:0]	

sro SRTS Receive FIFO overflow of port N
This field counts the amount of overflows of the SRTS Receive FIFO. Upon reaching FF_H it keeps its value.

7.62 SRTS Generator Reset of Port N (srrN)

Destructive read Address 00116_H + N x 32

Reset value: 0000_H

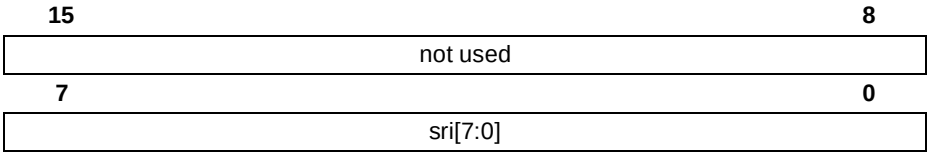
15	8
not used	
7	**0**
srr[7:0]	

srr SRTS generator reset command counter of port N
This field counts the number of times the SRTS generator is reset by frame receiver 1. Upon reaching FF_H it keeps its value.

7.63 SRTS Invalid Value Processed of Port N (sriN)

Destructive read Address 00117_H + N x 32

Reset value: 0000_H



sri SRTS invalid value processed counter of port N
This field counts the number of times PLL-SRTS and PLL-FILTER went in hold over due to invalid RTS values. Upon reaching FF_H it keeps its value.

7.64 ACM Data Too Late of Port N (atlN)

Destructive read Address 00118_H + N x 32

Reset value: 0000_H

15	8
not used	
7	**0**
atl[7:0]	

atl ACM data too late error counter of port N
This field counts the number of times the next ACM data arrived more than 10 ms too late. Upon reaching FF_H it keeps its value.

7.65 Out Of Lock Register of Port N (oolN)

Destructive read Address 00119_H + N x 32

Reset value: 0000_H

15			8
not used			
7			**0**
not used	olf	ols	ola

olf PLL-Filter out of lock at port N
This bit indicates that the number of times PLL-FILTER went out of lock exceeds treshN[tr_filt].

0 = False

1 = True

ols PLL-SRTS out of lock at port N
This bit indicates that the number of times PLL-SRTS went out of lock exceeds treshN[tr_srts].

0 = False

1 = True

ola PLL-ACM out of lock at port N
This bit indicates that the number of times PLL-ACM went out of lock exceeds treshN[tr_acm].

0 = False

1 = True

7.66 Status Register of Port N (statN)

Destructive read Address $0011A_H$ + N x 32

Reset value: 0001_H

15							8
not used							
7							**0**
not used					max	hov	frr

max Maximum frequency deviation
Indicates that PLL-ACM is clipped at its maximum frequency deviation.

0 = False

1 = True

hov Hold over
Indicates that PLL-SRTS is put in hold over because of error conditions in the SRTS processing.

0 = False

1 = True

frr Free running clock
Indicates that PLL-SRTS or PLL-ACM is put in free run during start-up.

0 = False

1 = True

7.67 Test Output Register of Port N (tsoutN)

Destructive read Address $0011B_H$ + N x 32

Reset value: 0000_H

15							8
not used							
7							**0**
not used					rtso[3:0]		dav

rtso RTS test output value of port N
If bit ena from register tsinN is set: RTS value at the output of the SRTS Receive FIFO of this port.

dav Data available
SRTS Receive FIFO of this port is not empty

0 = False

1 = True

Note: By verifying bit dav, the SRTS Receive FIFO can be read completely by successive reads of this register.

8 Application Hints

8.1 Clock Concept

Mode			BITS (cbb=0)			PINS					
E1 / T1	Framer Interface	Clock Recovery	om	ftck	rts_eval	RFCLK	FRCLK[0:7]	FTCKO[0:7]	CLK52	CLOCK	RXCLK TXCLK
E1	FAM	none	00	00	00	32.768 MHz OEC	8.192 MHz	8.192 MHz	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
E1	FAM	none	00	01	01	32.768 MHz OEC	8.192 MHz	FRCLK[0:7]	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
E1	FAM	none	00	10	01	32.768 MHz	8.192 MHz		unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
E1	FAM	SRTS	00	00	01	32.768 MHz +/- 50ppm	8.192 MHz	8.192 MHz from ICRC	51.84 MHz +/- 250ppm	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
E1	FAM	ACM	00	00	01	32.768 MHz +/- 130ppm	8.192 MHz	8.192 MHz from ICRC	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
E1	FAM	ECRC	00	00	00	32.768 MHz OEC	8.192 MHz	8.192 MHz from ECRC	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
E1	GIM	none	01	00	00	32.768 MHz OEC	2.048 MHz	2.048 MHz	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
E1	GIM	none	01	01	01	32.768 MHz OEC	2.048 MHz	FRCLK[0:7]	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
E1	GIM	none	01	10	01	32.768 MHz	2.048 MHz	RFCLK / 16	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
E1	GIM	SRTS	01	00	01	32.768 MHz +/- 50ppm	2.048 MHz	2.048 MHz from ICRC	51.84 MHz +/- 250ppm	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
E1	GIM	ACM	01	00	01	32.768 MHz +/- 130ppm	2.048 MHz	2.048 MHz from ICRC	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
E1	GIM	ECRC	01	00	00	32.768 MHz OEC	2.048 MHz	2.048 MHz from ECRC	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
E1	SYM8	none	10	x	x	8.192 MHz FIC	unused	unused	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
E1	SYM2	none	11	x	x	2.048 MHz FIC	unused	unused	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
E1	EC	none	x	x	x	8.192 MHz FIC	unused	unused	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
T1	FAM	none	00	00	00	32.768 MHz OEC	8.192 MHz	8.192 MHz	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
T1	FAM	none	00	01	01	32.768 MHz OEC	8.192 MHz	FRCLK[0:7]	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
T1	FAM	none	00	10	01	32.768 MHz	8.192 MHz		unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
T1	FAM	SRTS	00	00	01	32.768 MHz +/- 50ppm	8.192 MHz	8.192 MHz from ICRC	51.84 MHz +/- 250ppm	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
T1	FAM	ACM	00	00	01	32.768 MHz +/- 130ppm	8.192 MHz	8.192 MHz from ICRC	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
T1	FAM	ECRC	00	00	00	32.768 MHz OEC	8.192 MHz	8.192 MHz from ECRC	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
T1	GIM	none	01	00	00	24.704 MHz OEC	1.544 MHz	1.544 MHz	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
T1	GIM	none	01	01	01	24.704 MHz OEC	1.544 MHz	FRCLK[0:7]	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
T1	GIM	none	01	10	01	24.704 MHz	1.544 MHz	RFCLK / 16	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
T1	GIM	SRTS	01	00	01	24.704 MHz +/- 50ppm	1.544 MHz	1.544 MHz from ICRC	51.84 MHz +/- 250ppm	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
T1	GIM	ACM	01	00	01	24.704 MHz +/- 130ppm	1.544 MHz	1.544 MHz from ICRC	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
T1	GIM	ECRC	01	00	00	24.704 MHz OEC	1.544 MHz	1.544 MHz from ECRC	unused	12*FDATA < F_{CLOCK} < 39MHz	<= CLOCK
T1	SYM8	none	10	x	x	unused	unused	unused	unused	unused	unused
T1	SYM2	none	11	x	x	unused	unused	unused	unused	unused	unused
T1	EC	none	x	x	x	unused	unused	unused	unused	unused	unused

FIC = Framer Interface Clock for Rx and Tx; OEC = Optional Emergency Clock; x = Don't care; ECRC = External Clock Recovery Circuit;

Figure 38 Clock Concept

The PLLs for SRTS accept RFCLK deviations of at least + and - 50 ppm. However, in case of switchover to emergency mode, RFCLK will be used to generate the line clock, which has to fulfill specifications like "maximum 4.6 ppm deviation under ALL circumstances". In this case RFCLK accuracy has to be 4.6 ppm.

8.2 Translating AAL Statistics Counters into the ATM Forum CES Version 2 MIB

Reset Statistics Counters and µP RAM variables before connection setup

atmfCESReassCells

Accumulated values from IWE8 Statistics Counter #2 destructive read accesses

atmfCESHdrErrors

Accumulated values from IWE8 Statistics Counter #6 destructive read accesses

atmfCESPointerReframes

CES Version 2.0 MIB recommends "This records the count of the number of events in which the AAL1 reassembler found that an SDT pointer is not where it is expected, and the pointer must be reacquired.“

"Pointer is not where it is expected" can mean.

a) no pointer occurs within an 8-cell-cycle

b) two pointers occur within an 8-cell-cycle

c) pointer is not in the 2nd byte of ATM cell payload,

Error case a) and b) causes incrementation of Statistics Counter #11.

All error cases a), b) and c) causes loss of synchronization of AtmStartOfStructure (IWE8 reassembly buffer read pointer to structure start in ATM cell) with PortStartOfStructure (pointer to structure start in framer interface port), so that Statistics Counter #14 increments.

==> Accumulated values from IWE8 Statistics Counter #14 destructive read accesses.

atmfCESPointerParityErrors

Accumulated values from IWE8 Statistics Counter #10 destructive read accesses

atmfCESAal1SeqErrors

Accumulated values from IWE8 Statistics Counter #7 destructive read accesses

atmfCESLostCells

Accumulated values from IWE8 Statistics Counter #15 destructive read accesses

atmfCESMisinsertedCells

Accumulated values from IWE8 Statistics Counter #8 destructive read accesses

atmfCESBufUnderflows

Can be derived from IWE8 Statistics Counter #13

atmfCESBufOverflows

Can be derived from IWE8 Statistics Counter #4

atmfCESCellLossStatus

Can be derived from atmfCESBufUnderflows and EndOfUnderflow

"When cells are continuously lost for the number of milliseconds specified by atmfCESCellLossIntegrationPeriod, the value is set to loss (2). When cells are no longer lost, the value is set to noLoss (1).“

8.3 Jitter Characteristics of the Internal Clock Recovery Circuit

This section shows the results of jitter analysis of the ICRC. The device is intended to be used with an external jitter attenuator. For this purpose Infineon's FALC-LH was used. Results are shown with and without jitter attenuator. Measurements were done using a Wandel & Goltermann ANT20 for IWE8 in T1 mode with FALC-LH and Wandel & Goltermann PFJ-8 for the bare IWE8 in E1 or T1 mode.

8.3.1 ACM Jitter Tolerance in E1 Mode

The jitter tolerance falls with 20 dB per decade, It is independent from the PLL gain ("ASF").

For the bare device the jitter tolerance meets the requirements of ITU-T G.823 and I.431 at medium and low frequencies. At frequencies lower than 1 KHz the jitter tolerance is more than 20 UI. At high frequencies it is lower than the requirements.

In combination with an jitter attenuator the requirements are met. Jitter tolerance at high frequencies is better than 0.2 UI.

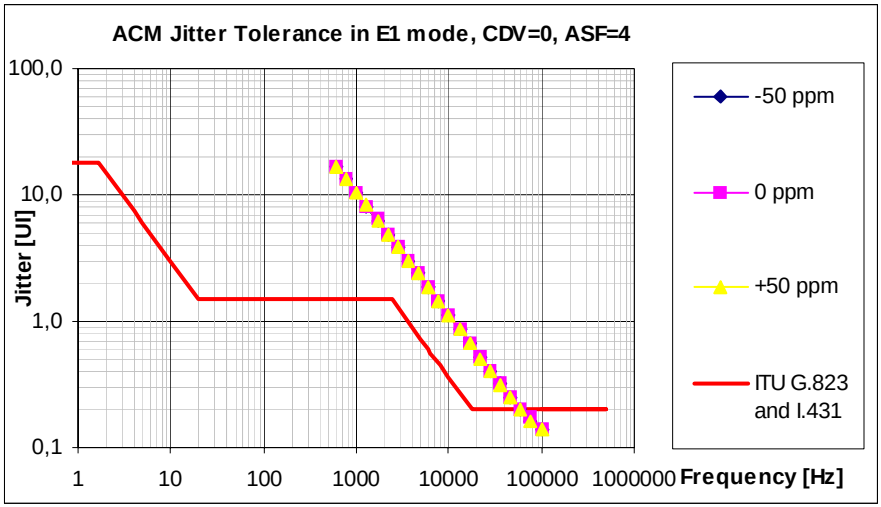


Figure 39 ACM Jitter Tolerance in E1 Mode without Jitter Attenuator

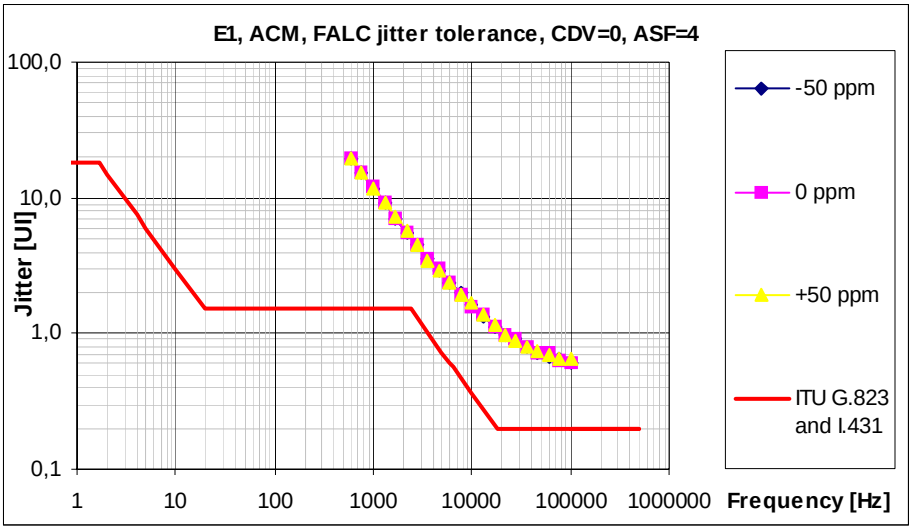


Figure 40 ACM Jitter Tolerance in E1 Mode with Jitter Attenuator

8.3.2 ACM Jitter Tolerance in T1 Mode

The jitter tolerance of the bare device in T1 mode exceeds the capabilities of the measurement equipment. This behavior is independent from frequency offset or PLL gain.

Using the jitter attenuator slightly reduces the jitter tolerance to a level which can be measured. All requirements are fulfilled.

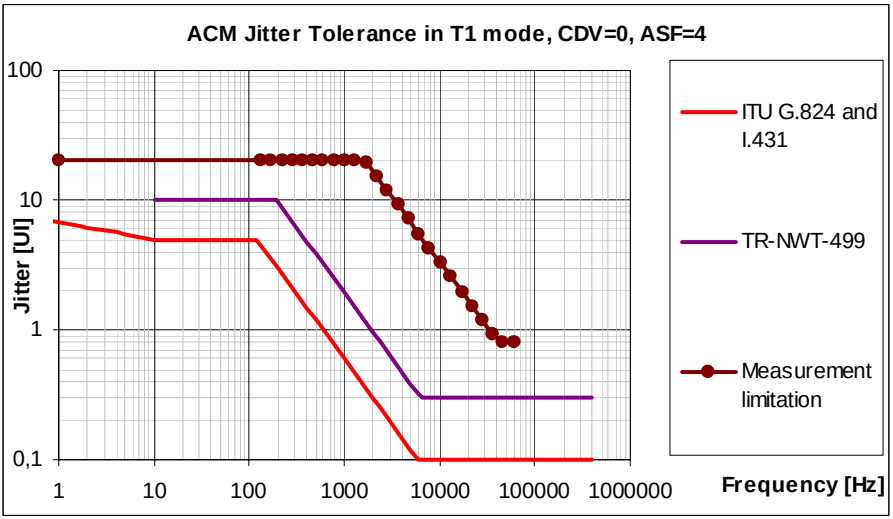


Figure 41 ACM Jitter Tolerance in T1 Mode without Jitter Attenuator

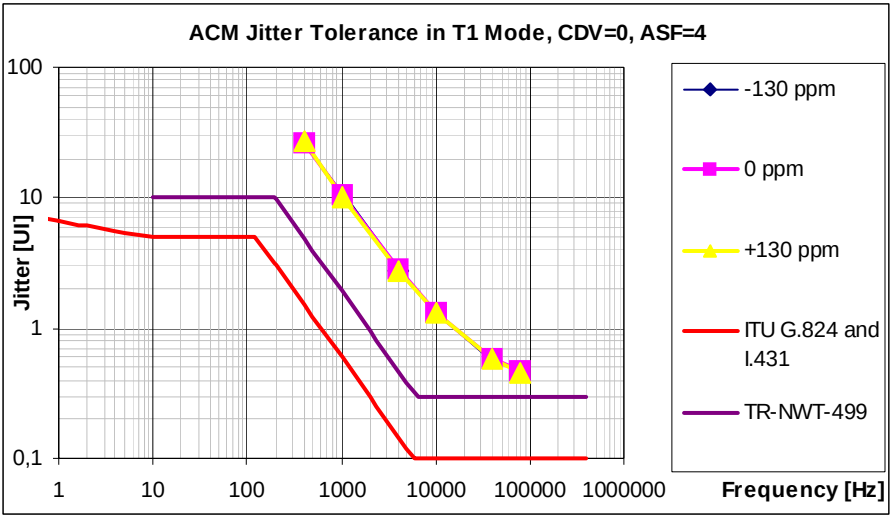


Figure 42 ACM Jitter Tolerance in T1 Mode with Jitter Attenuator

8.3.3 SRTS Jitter Tolerance in E1 Mode

The aliasing effect which is inherent to the SRTS algorithm causes the jitter tolerance at 681 Hz and all multiples of 681 Hz to be a copy of the jitter tolerance at 0 Hz.

The jitter tolerance of the bare device meets the requirements of ITU-T G.823 and I.431 only at medium and low frequencies. At high frequencies it is lower than the requirements.

In combination with an jitter attenuator the tolerance at high frequencies is better than 0.2 UI. All requirements are met.

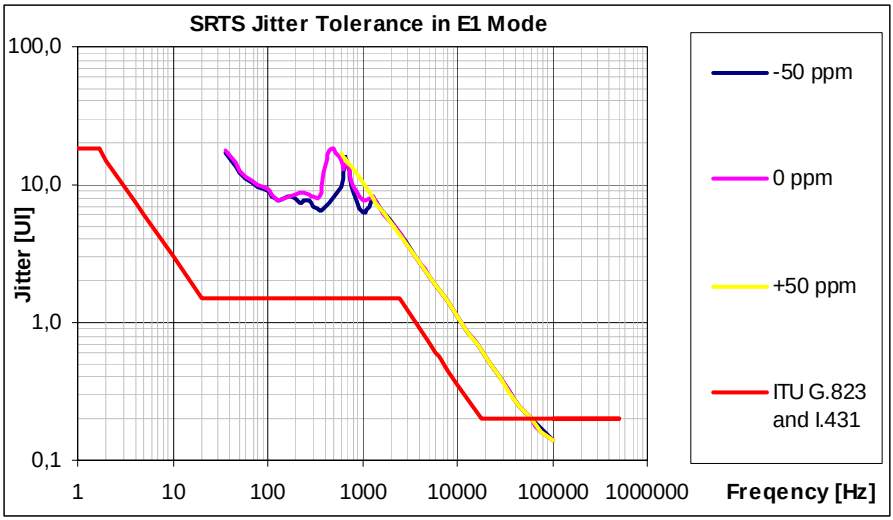


Figure 43 SRTS Jitter Tolerance in E1 Mode without Jitter Attenuator

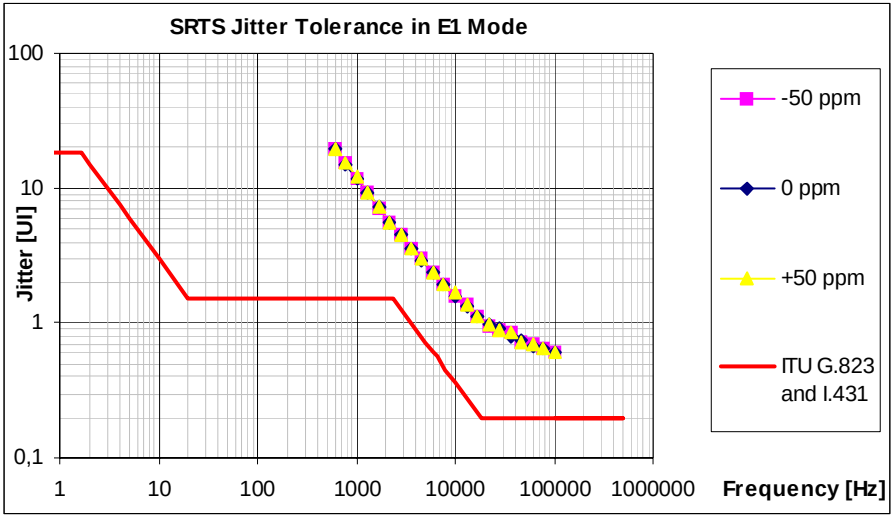


Figure 44 SRTS Jitter Tolerance in E1 Mode with Jitter Attenuator

8.3.4 SRTS Jitter Tolerance in T1 Mode

The aliasing effect which is inherent to the SRTS algorithm causes the jitter tolerance at 513 Hz and all multiples of 513 Hz to be a copy of the jitter tolerance at 0 Hz. Jitter Tolerance at low frequencies violate the requirements.

With jitter attenuator jitter tolerance at low frequencies is increased and all jitter frequencies above 20 Hz are removed. As a result no aliasing is possible. The jitter tolerance fulfills the requirements.

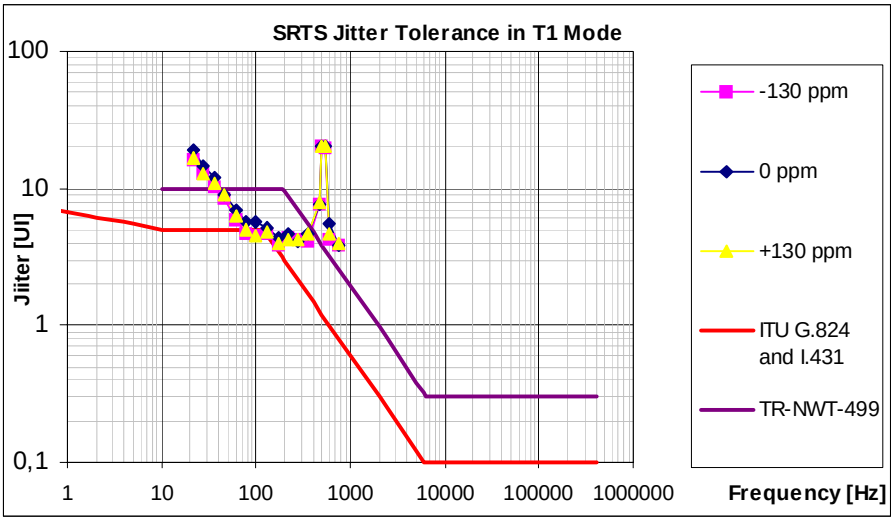


Figure 45 SRTS Jitter Tolerance in T1 Mode without Jitter Attenuator

Figure 46 SRTS Jitter Tolerance in T1 Mode with Jitter Attenuator

8.3.5 ACM Jitter Transfer in E1 Mode

The jitter transfer characteristics are much better than the requirements of ITU-T G.735 and I. 432.

The -3dB point of the transfer curve is proportional to the PLL-gain: 0.05 Hz for ASF=4, 0.2 Hz for ASF=16.

No impact of the jitter attenuator on the already very good jitter transfer behavior could be measured.

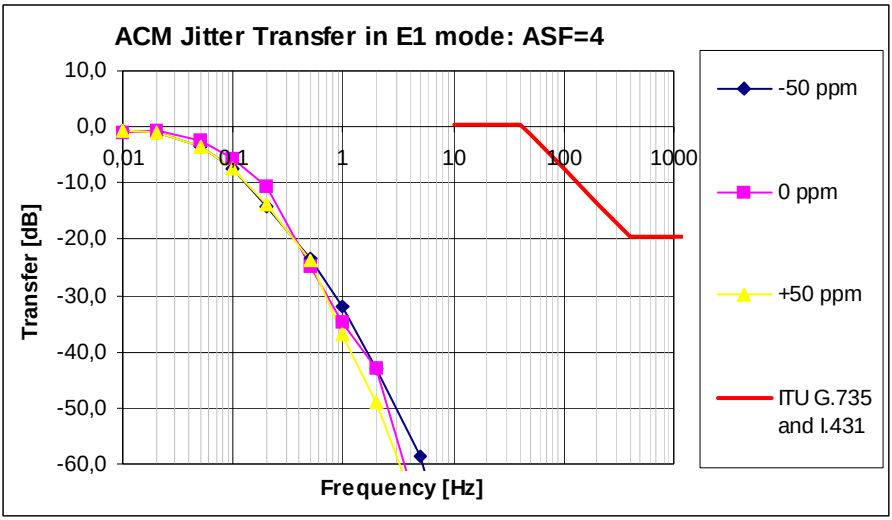


Figure 47 ACM Jitter Transfer in E1 Mode without Jitter Attenuator

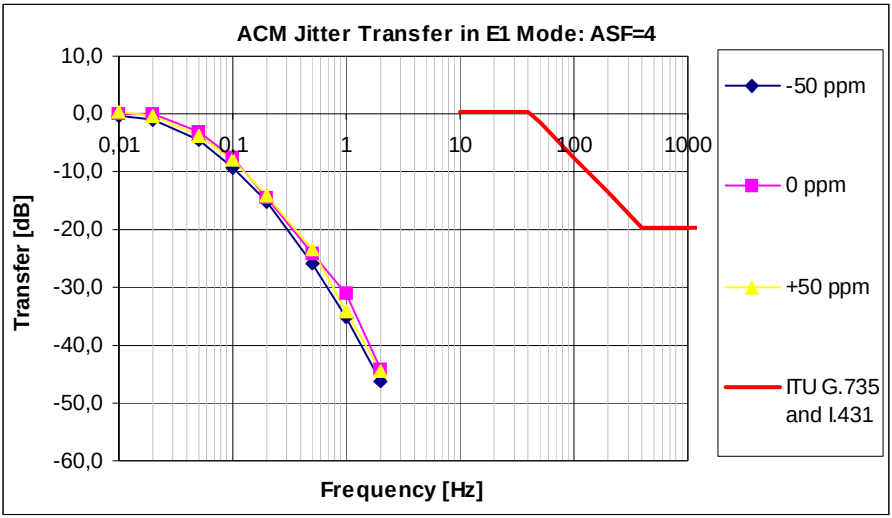


Figure 48 ACM Jitter Transfer in E1 Mode with Jitter Attenuator

8.3.6 ACM Jitter Transfer in T1 Mode

The jitter transfer characteristics are much better than the requirements of ITU-T G.735 and I. 432.

The -3dB point of the transfer curve is proportional to the PLL-gain: 0.075 Hz for ASF=4, 0.3 Hz for ASF=16.

The jitter attenuator improves the already very good jitter transfer behavior. At -130 ppm all jitter is removed.

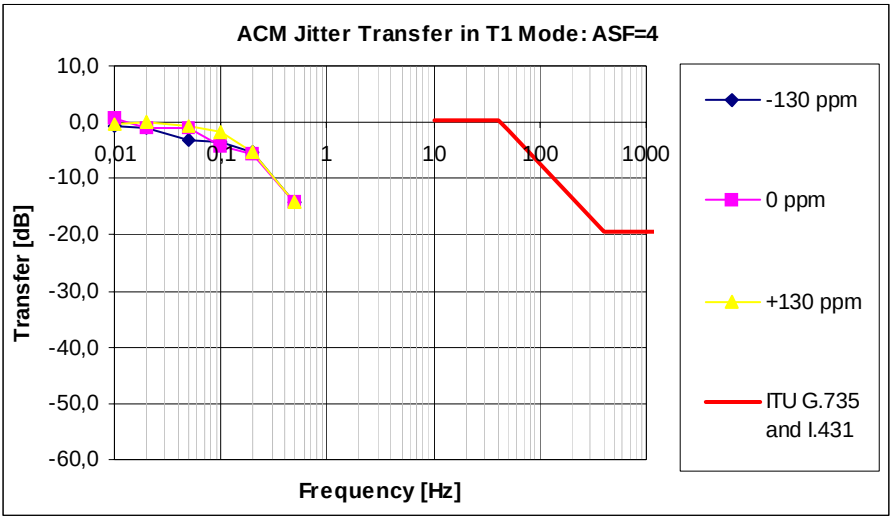


Figure 49 ACM Jitter Transfer in T1 Mode without Jitter Attenuator

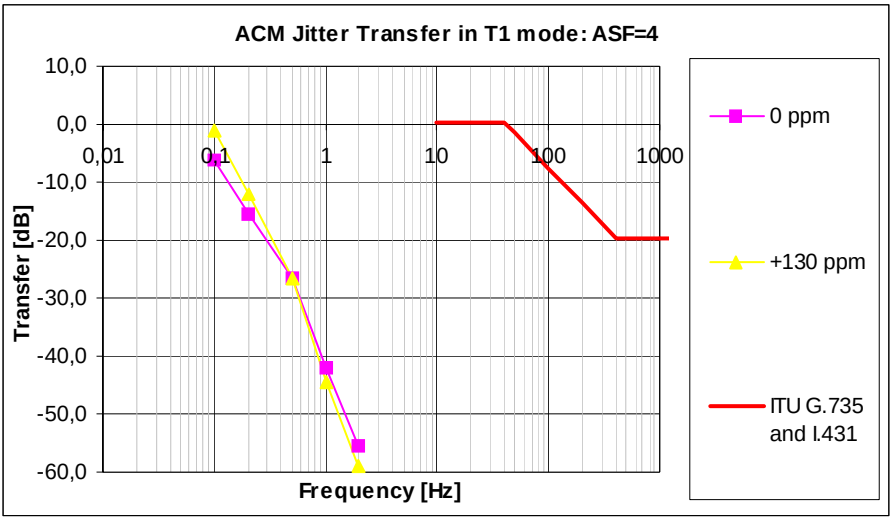


Figure 50 ACM Jitter Transfer in T1 Mode with Jitter Attenuator

8.3.7 SRTS Jitter Transfer in E1 Mode

The aliasing effect which is inherent to the SRTS algorithm causes the jitter transfer at 681 Hz and all multiples of 681 Hz to be a copy of the jitter transfer at 0 Hz. This violates the requirements.

The jitter attenuator removes jitter frequencies above 20 Hz. There is no aliasing and the requirements are met.

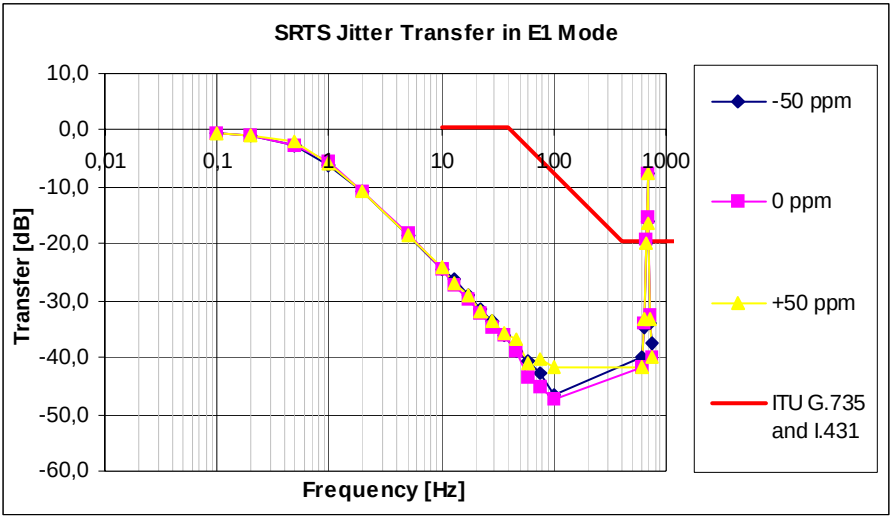


Figure 51 SRTS Jitter Transfer in E1 Mode without Jitter Attenuator

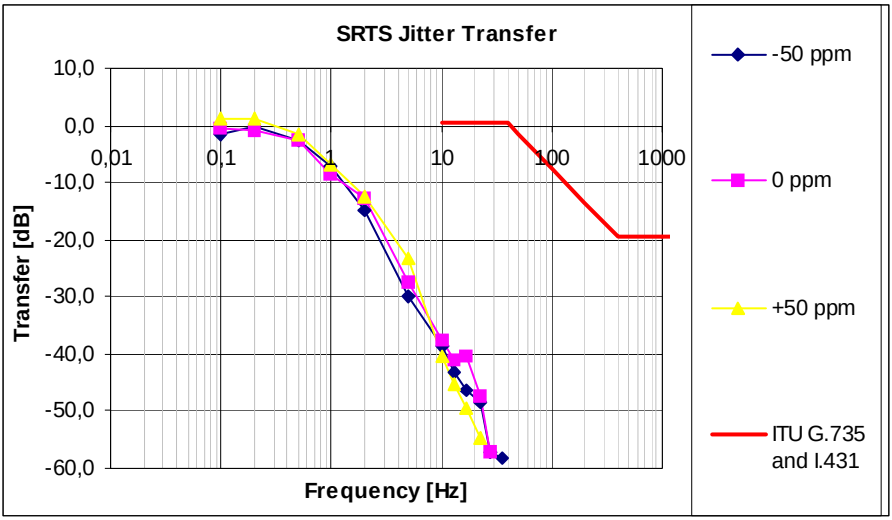


Figure 52 SRTS Jitter Transfer in E1 Mode with Jitter Attenuator

8.3.8 SRTS Jitter Transfer in T1 Mode

The aliasing effect which is inherent to the SRTS algorithm causes the jitter transfer at 513 Hz and all multiples of 513 Hz to be a copy of the jitter transfer at 0 Hz. This violates the requirements.

However, the measurement equipment was not able to measure jitter transfer above 100 Hz and the expected peaking is not measured.

The jitter attenuator removes jitter frequencies above 20 Hz. There is no aliasing and the requirements are met.

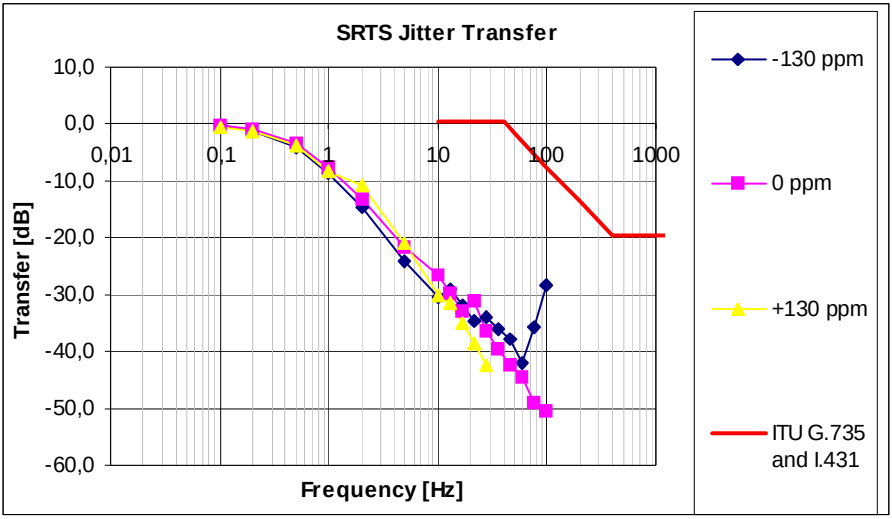


Figure 53 SRTS Jitter Transfer in T1 Mode without Jitter Attenuator

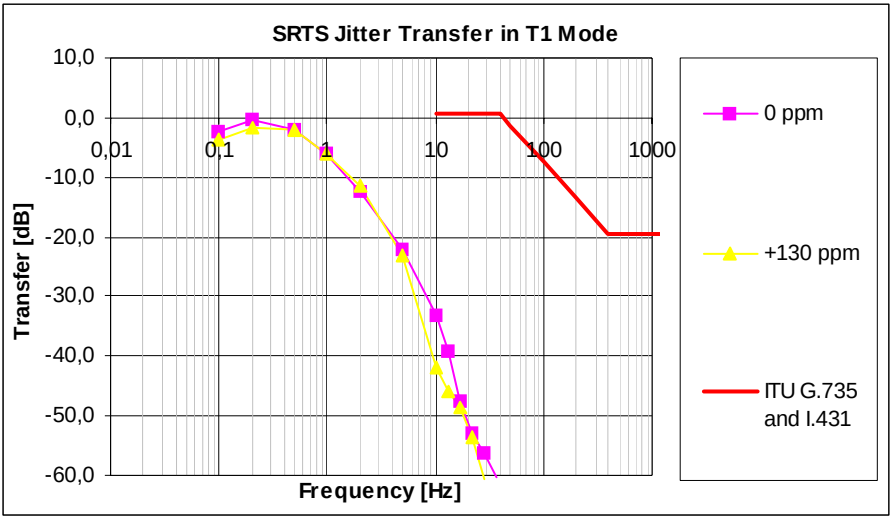


Figure 54 SRTS Jitter Transfer in T1 Mode with Jitter Attenuator

9 Electrical Characteristics

9.1 Absolute Maximum Ratings

Table 33 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	TA	-40 to 85	^{0}C
Junction temperature under bias	T_J	0 to 125	^{0}C
Storage temperature	T_{stg}	- 65 to 150	^{0}C
Supply voltage	V_{CC}	- 0.5 to 3.6	V
Input voltage (at any signal pin with respect to ground)	V_I	- 0.5 to 5.5	V
Output voltage level (at any signal pin with respect to ground)	V_O	- 0.5 to 5.5[1)]	V
ESD robustness[2)] HBM: 1.5 kW, 100 pF	$V_{ESD,HBM}$	1000	V

1) The maximum high output level is limited to V_{CC}. Due to 5V I/O tolerance output signals might be pulled to 5V level by external pull-up resistors.

2) According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993.
The RF Pins 20, 21, 26, 29, 32, 33, 34 and 35 are not protected against voltage stress > 300 V (versus V_S or GND). The high frequency performance prohibits the use of adequate protective structures.

Note: Stresses above those listed under “absolute maximum ratings” may cause permanent damage to the device. Exposure to “absolute maximum rating” conditions for extended periods may affect device reliability

9.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min	Max		
Ambient temperature	T_A	–40	85	°C	
Supply voltage	V_{CC}	3.15	3.45	V	3.3V ± 5%
Input voltage	V_I	0	5.5	V	5V I/O tolerance
Output voltage	V_O	0	5.5	V	
Input low voltage	V_{IL}	0	0.8	V	
Input high voltage	V_{IH}	2.1	5.5	V	

9.3 Thermal Package Characteristics

Parameter	Symbol	Limit Values	Unit	Test conditions
Thermal package resistance junction to ambient without airflow	$R_{JA(0,25)}$	25	°C/W	T_A=25°C

9.4 DC Characteristics

Parameter	Symbol	Limit Value		Unit	Test Condition
		Min	Max		
Input low voltage	V_{IL}	0	0.8	V	
Input high voltage	V_{IH}	2.1	5.5	V	
Output low voltage[1)]	V_{OL}		0.4	V	I_{OL} = 4 mA, 8 mA
Output high voltage[1)]	V_{OH}	V_{CC} - 0.6		V	I_{OH} = - 4 mA, - 8 mA
Low-level input leakage current	I_{LLI}		± 1	µA	$V_I = V_{IL(min)} = V_{SS}$
High-level input leakage current	$I_{HLI3.3}$ $I_{HLI5.5}$		± 1 ± 10	µA µA	$V_I = V_{IH(VCC)} = V_{CC}$ $V_I = V_{IH(max)}$ = 5.5 V
High-impedance state output current	I_{OZ}		± 1	µA	
Pull up current[2)]	I_{PUA}	1	12	µA	V_{CC} = 3.3V, $V_I = V_{IL(min)} = V_{SS}$
Pull up current[3)]	I_{PUB}	40	130	µA	V_{CC} = 3.3V, $V_I = V_{IL(min)} = V_{SS}$
Pull down current[4)]	I_{PDA}	1	12	µA	V_{CC} = 3.3V, $V_I = V_{IH(VCC)} = V_{CC}$
Power supply current during power-up	$I_{CCPwrUp}$		700	mA	V_{CC} = 3.3V, inputs at V_{SS}/V_{CC}, no output loads, F_{CLOCK} = 40 MHz
Average power supply current [5)]	$I_{CC\ Typ.}$		330	mA	V_{CC} = 3.3V, inputs at V_{SS}/V_{CC}, no output loads, F_{CLOCK} = 25 MHz
Average Power dissipation [5)]	$P_{Typ.}$		1.10	W	

1) All Utopia output buffers are 8 mA.

2) The current is applicable for all pins for which an type PUA has been specified in **Chapter 2.2**

3) The current is applicable for all pins for which an type PUB has been specified in **Chapter 2.2**

4) The current is applicable for all pins for which an type PDA has been specified in **Chapter 2.2**

5) Not tested in production.

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_a = 25 °C and the given supply voltage.

9.5 Capacitances

Parameter	Symbol	Limit Value		Unit	Test Condition
		Min	Max		
Input capacitance	C_{IN}		10	pF	
Output capacitance	C_{OUT}		15	pF	

Note: The listed characteristics are not tested in production.

9.6 AC Characteristics

T_A = -40 to 85 °C, V_{CC} = 3.3 V ± 5%, V_{SS} = 0 V

All inputs are driven to V_{IH} = 2.4 V for a logical “1” and to V_{IL} = 0.4 V for a logical “0”

All outputs are measured at V_H = 2.0 V for a logical “1”and at V_L = 0.8 V for a logical “0”

The AC testing input/output waveforms are shown below.

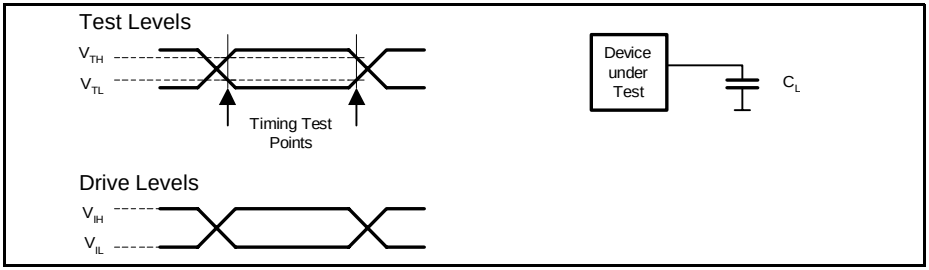


Figure 55 Input/Output Waveforms for AC Measurements

9.6.1 Clock and Reset Interface

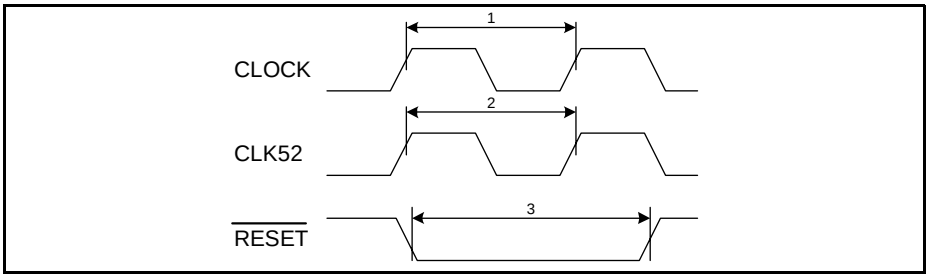


Figure 56 Clock and Reset Interface Timing Diagram

Table 34 Clock and Reset Interface AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{CLOCK}: Period CLOCK				
	GIM T1:	25,72	40	53,97	ns
	others:	25,72	40	40,69	ns
1A	F_{CLOCK}: Frequency CLOCK[1)]				

Table 34 Clock and Reset Interface AC Timing Characteristics (cont'd)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
	GIM T1:	18,53	25	38,88	MHz
	others:	24,58	25	38,88	MHz
2	T_{CLK52}: Period CLK52[2)]	-50 ppm	19.29	+50 ppm	ns
2A	F_{CLK52}: Frequency CLK52 [2)]	-50 ppm	51.84	+50 ppm	MHz
3	Pulse width $\overline{RESET}$ low	$3xT_{CLOCK}$			

1) The frequency should be equal or higher than RXCLK and TXCLK of the UTOPIA interface

2) Only required if the Internal Clock Recovery Circuit is used for SRTS

9.6.2 Framer Interface

9.6.2.1 Framer Interface in FAM

Framer Receive Interface

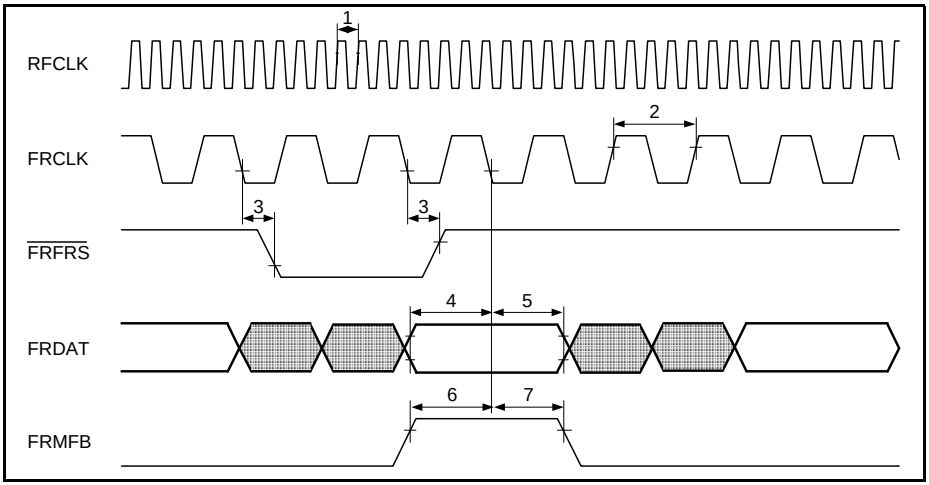


Figure 57 Framer Receive Interface Timing in FAM

Table 35 Framer Receive Interface Timing in FAM

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{RFCLK}: Period RFCLK [1)]		30,518		ns
1A	F_{RFCLK}: Frequency RFCLK [1)]		32,768		MHz
2	T_{FRCLK}: Period FRCLK	- 130 ppm	122	+130 ppm	ns
2A	F_{FRCLK}: Frequency FRCLK	- 130 ppm	8,192	+130 ppm	MHz
3	Delay FRCLK falling to $\overline{FRFRS}$	3		32	ns
4	Setup time FRDAT before FRCLK falling (center of bit period)	15			ns
5	Hold time FRDAT after FRCLK falling (center of bit period)	15			ns
6	Setup time FRMFB before FRCLK falling (center of bit period)	15			ns
7	Hold time FRMFB after FRCLK falling (center of bit period)	15			ns

1) In case the Internal Clock Recovery Circuit is used for SRTS, the frequency deviation should be +/- 10 ppm

Framer Transmit Interface

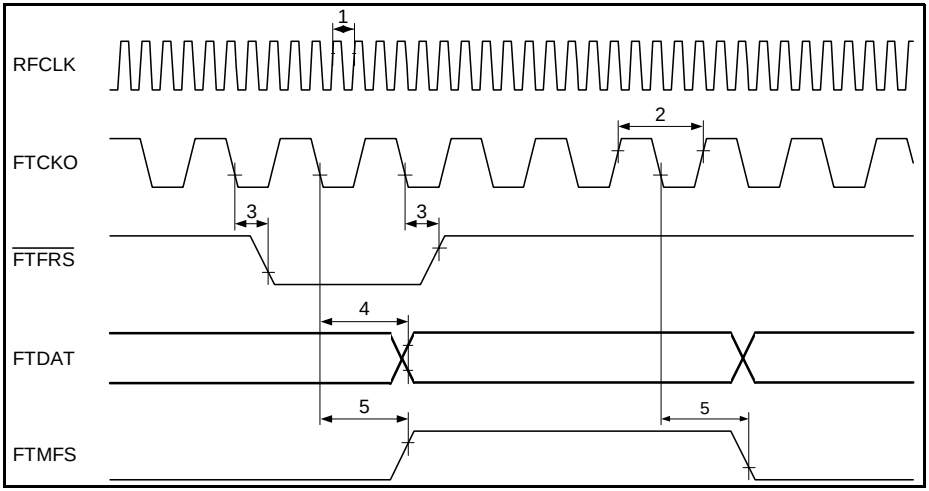


Figure 58 Framer Transmit Interface Timing in FAM

Table 36 Framer Transmit Interface Timing in FAM

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{RFCLK}: Period RFCLK [1)]		30,518		ns
1A	F_{RFCLK}: Frequency RFCLK [1)]		32,768		MHz
2	T_{FTCKO}: Period FTCKO	-130 ppm	122	+130 ppm	ns
2A	F_{FTCKO}: Frequency FTCKO	-130 ppm	8,192	+130 ppm	MHz
3	Delay FTCKO in falling to $\overline{FTFRS}$	3		32	ns
	Delay FTCKO out falling to $\overline{FTFRS}$	-3		32	ns
4	Delay FTCKO in falling to FTDAT	3		32	ns
	Delay FTCKO out falling to FTDAT	-3		32	ns
5	Delay FTCKO in falling to FTMFS	3		32	ns
	Delay FTCKO out falling to FTMFS	-3		32	ns

1) In case the Internal Clock Recovery Circuit is used for SRTS, the frequency deviation should be +/- 10 ppm

9.6.2.2 Framer Interface in GIM

Framer Receive Interface

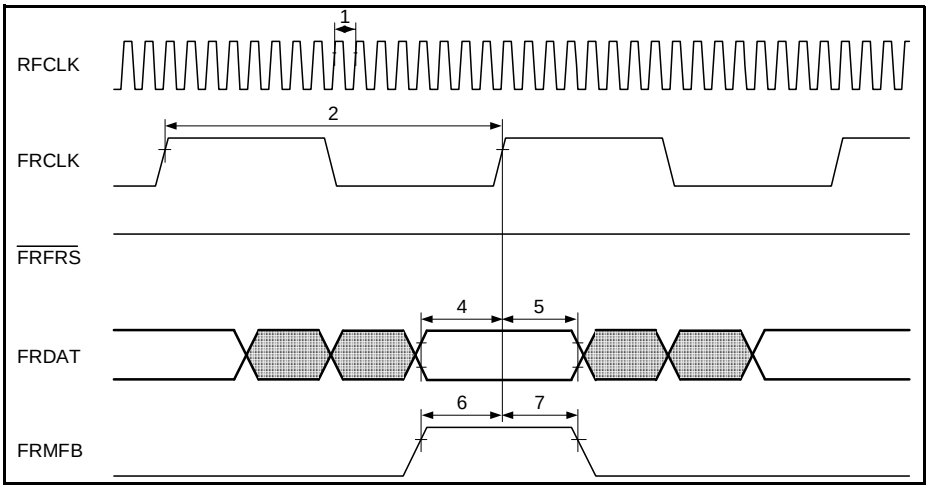


Figure 59 Framer Receive Interface Timing in GIM

Table 37 Framer Receive Interface Timing in GIM

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{RFCLK}: Period RFCLK [1)]				
	E1:		30,518		ns
	T1:		40,478		ns
1A	F_{RFCLK}: Frequency RFCLK [1)]				
	E1:		32,768		MHz
	T1:		24,704		MHz
2	T_{FRCLK}: Period FRCLK				
	E1:		488		ns
	T1:		647		ns
2A	F_{FRCLK}: Frequency FRCLK				
	E1:		2,048		MHz
	T1:		1,544		MHz

Table 37 Framer Receive Interface Timing in GIM (cont'd)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
4	Setup time FRDAT before FRCLK falling (center of bit period)	15			ns
5	Hold time FRDAT after FRCLK falling (center of bit period)	15			ns
6	Setup time FRMFB before FRCLK falling (center of bit period)	15			ns
7	Hold time FRMFB after FRCLK falling (center of bit period)	15			ns

1) In case the Internal Clock Recovery Circuit is used for SRTS, the frequency deviation should be +/- 10 ppm

Framer Transmit Interface

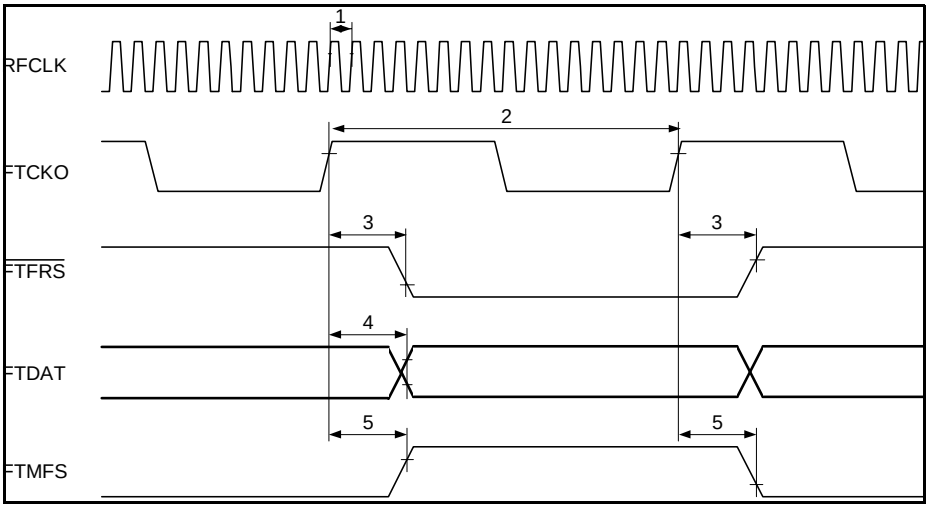


Figure 60 Framer Transmit Interface Timing in GIM

Table 38 Framer Transmit Interface Timing in GIM

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{RFCLK}: Period RFCLK[1)] E1:		 30,518		 ns

Table 38 Framer Transmit Interface Timing in GIM (cont'd)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
	T1:		40,478		ns
1A	F_{RFCLK}: Frequency RFCLK [1]				
	E1:		32,768		MHz
	T1:		24,704		MHz
2	T_{FTCKO}: Period FTCKO				
	E1:		488		ns
	T1:		647		ns
2A	F_{FTCKO}: Frequency FTCKO				
	E1:		2,048		MHz
	T1:		1,544		MHz
3	Delay FTCKO in falling to $\overline{\text{FTFRS}}$	3		32	ns
	Delay FTCKO out falling to $\overline{\text{FTFRS}}$	-3		32	ns
4	Delay FTCKO in falling to FTDAT	3		32	ns
	Delay FTCKO out falling to FTDAT	-3		32	ns
5	Delay FTCKO in falling to FTMFS	3		32	ns
	Delay FTCKO out falling to FTMFS	-3		32	ns

[1] In case the Internal Clock Recovery Circuit is used for SRTS, the frequency deviation should be +/- 10 ppm

9.6.2.3 Framer Interface in SYM Mode

Framer Interface in SYM2

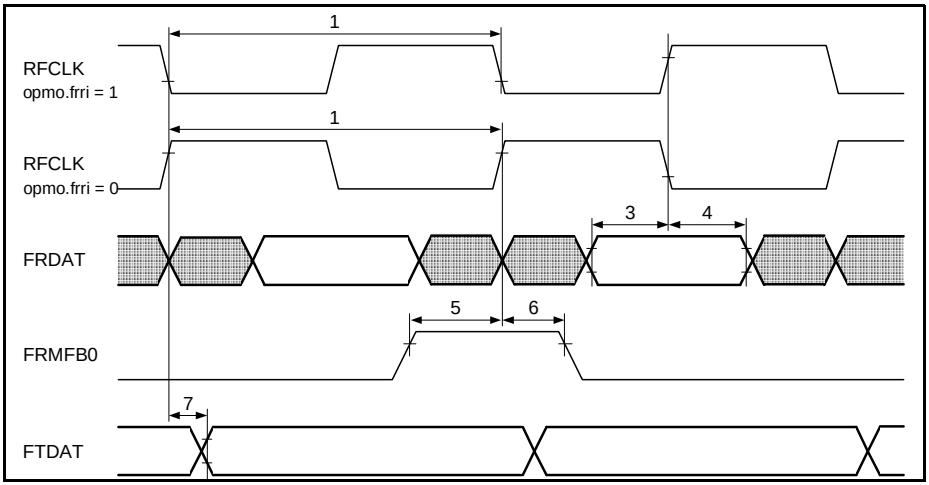


Figure 61 Framer Interface Timing for SYM 2.048 MHz

Table 39 Framer Interface AC Timing Characteristics in SYM2 Mode

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{RFCLK}: Period RFCLK		488		ns
1A	F_{RFCLK}: Frequency RFCLK		2,048		MHz
3	Setup time FRDAT before RFCLK falling/rising (center of bit period)	15			ns
4	Hold time FRDAT after RFCLK falling/ rising (center of bit period)	15			ns
5	Setup time FRMFBN[1)] before RFCLK falling/rising	15			ns
6	Hold time FRMFBN[1)] after RFCLK falling	15			ns
7	Delay RFCLK falling/rising to FTDAT	3		32	ns

1) For usage of FRMFBN in SYM mode see **Chapter 7.24**

Framer Interface in SYM8

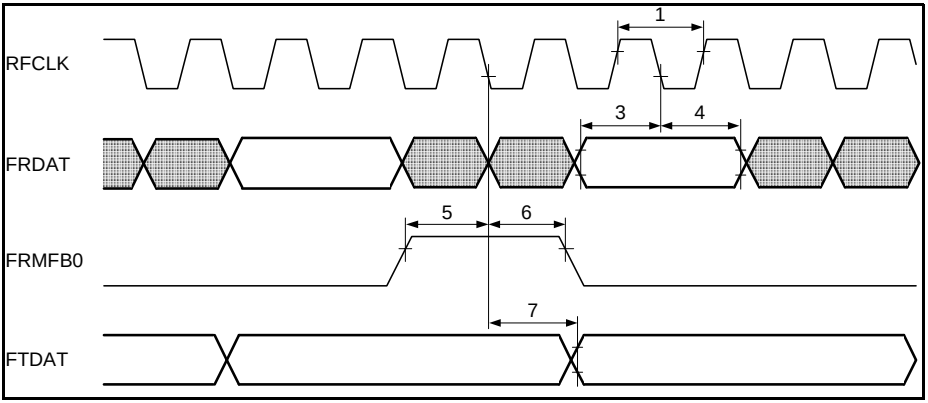


Figure 62 Framer Interface Timing in SYM 8.192 MHz

Table 40 Framer Interface Timing in SYM8

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{RFCLK}: Period RFCLK		122		ns
1A	F_{RFCLK}: Frequency RFCLK	-130 ppm	8,192	+130ppm	MHz
3	Setup time FRDAT before RFCLK falling/rising (center of bit period)	15			ns
4	Hold time FRDAT after RFCLK falling/ rising (center of bit period)	15			ns
5	Setup time FRMFBN[1)] before RFCLK falling/rising	15			ns
6	Hold time FRMFBN[1)] after RFCLK falling	15			ns
7	Delay RFCLK falling to FTDAT	3		32	ns

1) For usage of FRMFBN in SYM mode see **Chapter 7.24**

9.6.2.4 Framer Interface in EC Mode

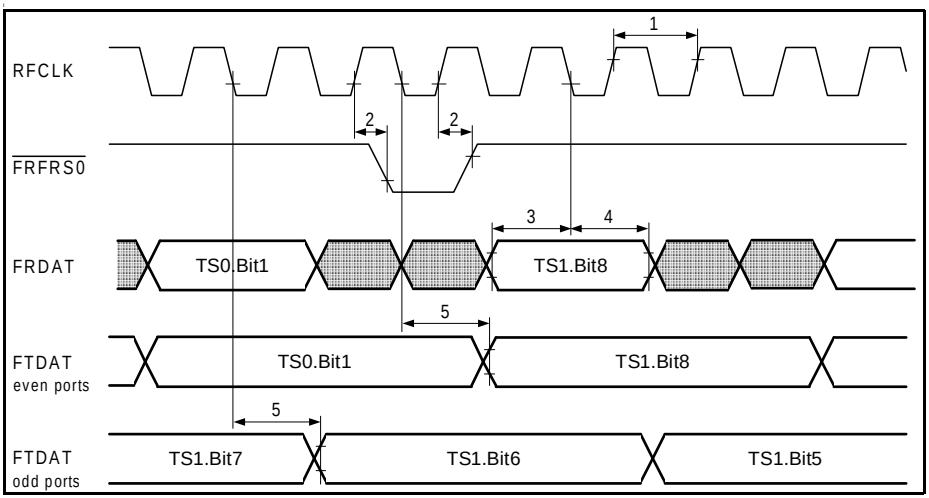


Figure 63 Framer Interface Timing in EC Mode

Table 41 Framer Interface Timing in EC Mode

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{RFCLK}: Period RFCLK		122		ns
1A	F_{RFCLK}: Frequency RFCLK	-130 ppm	8,192	+130ppm	MHz
2	Delay RFCLK rising to $\overline{FTFRS0}$	3		32	ns
3	Setup time FRDAT before RFCLK falling (center of bit period)	15			ns
4	Hold time FRDAT after RFCLK falling (center of bit period)	15			ns
5	Delay RFCLK falling to FTDAT	3		32	ns

9.6.3 UTOPIA Interface

The AC characteristics of the UTOPIA interface fulfills the ATM Forum “UTOPIA level 2 Specification, Version 1.0" as defined for the interface running at 33 MHz.

The AC characteristics are based on the timing specification for the receiver side of a signal.

The setup and the hold times are defined with regard to a positive clock edge, see **Figure 64**.

Taking the actual used clock frequency into account (e.g. up to the max. frequency), the corresponding (min. and max.) transmit side “clock to output” propagation delay specifications can be derived. The timing references (tT5 to tT12) are according to**Table 42** to **Table 45**.

In the following tables, A>P (column DIR, Direction) defines a signal from the ATM layer (transmitter, driver) to the PHY layer (receiver), A<P defines a signal from the PHY layer (transmitter, driver) to the ATM layer (receiver).

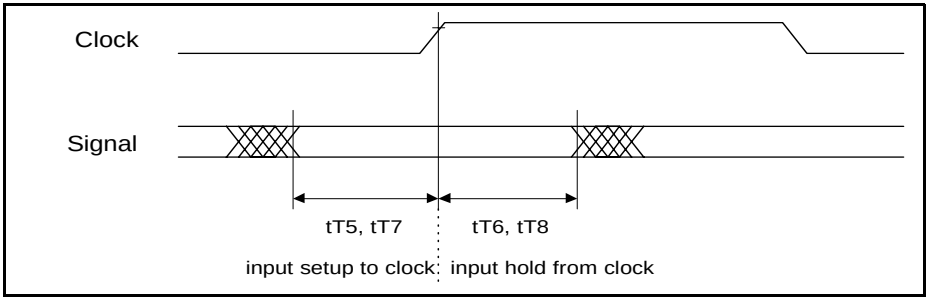


Figure 64 Setup and hold time definition (single- and multi PHY)

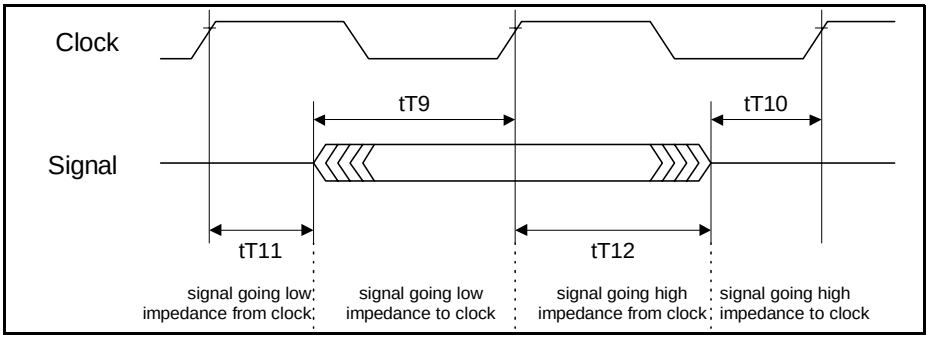


Figure 65 Tri-state timing (multi-PHY, multiple devices only)

Table 42 Transmit Timing (8-Bit Data Bus, 33 MHz at Cell Interface, Single PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
t1	TXCLK[1)]	A>P	TXCLK frequency (nominal)	0	33	MHz
tT2			TXCLK duty cycle	40	60	%
tT3			TXCLK peak-to-peak jitter	-	5	%
tT4			TXCLK rise/fall time	-	3	ns
tT5	TXDAT[7:0], TXPTY, TXSOC, TXENB	A>P	Input setup to TXCLK	8	-	ns
tT6			Input hold from TXCLK	1	-	ns
tT7	TXCLAV	A<P	Input setup to TXCLK	8	-	ns
tT8			Input hold from TXCLK	1	-	ns

1) The frequency should be equal or smaller than the coreclock CLOCK

Table 43 Receive Timing (8-Bit Data Bus, 33 MHz at Cell Interface, Single PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
t1	RXCLK[1)]	A>P	RXCLK frequency (nominal)	0	33	MHz
tT2			RXCLK duty cycle	40	60	%
tT3			RXCLK peak-to-peak jitter	-	5	%
tT4			RXCLK rise/fall time	-	3	ns
tT5	RXENB	A>P	Input setup to RXCLK	8	-	ns
tT6			Input hold from RXCLK	1	-	ns
tT7	RXDAT[7:0], RXPTY, RXSOC, RXCLAV	A<P	Input setup to RXCLK	8	-	ns
tT8			Input hold from RXCLK	1	-	ns

1) The frequency should be equal or smaller than the coreclock CLOCK

Table 44 Transmit Timing (8-Bit Data Bus, 33 MHz at Cell Interface, Multi-PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
t1	TXCLK[1)]	A>P	TXCLK frequency (nominal)	0	33	MHz
tT2			TXCLK duty cycle	40	60	%
tT3			TXCLK peak-to-peak jitter	-	5	%
tT4			TXCLK rise/fall time	-	3	ns
tT5	TXDAT[7:0], TXPTY, TXSOC, TXENB, TXADR[4:0]	A>P	Input setup to TXCLK	8	-	ns
tT6			Input hold from TXCLK	1	-	ns
tT7	TXCLAV	A<P	Input setup to TXCLK	8	-	ns
tT8			Input hold from TXCLK	1	-	ns
tT9			Signal going low impedance to TXCLK	8	-	ns
tT10			Signal going high impedance to TXCLK	0	-	ns
tT11			Signal going low impedance from TXCLK	1	-	ns
tT12			Signal going high impedance from TXCLK	1	-	ns

1) The frequency should be equal or smaller than the coreclock CLOCK

Table 45 Receive Timing (8-Bit Data Bus, 33 MHz at Cell Interface, Multi-PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
t1	RXCLK[1)]	A>P	RXCLK frequency (nominal)	0	33	MHz
tT2			RXCLK duty cycle	40	60	%
tT3			RXCLK peak-to-peak jitter	-	5	%
tT4			RXCLK rise/fall time	-	3	ns
tT5	RXENB, RXADR[4:0]	A>P	Input setup to RXCLK	8	-	ns
tT6			Input hold from RXCLK	1	-	ns

Table 45 Receive Timing (8-Bit Data Bus, 33 MHz at Cell Interface, Multi-PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
tT7	RXDAT[7:0], RXPTY, RXSOC, RXCLAV	A<P	Input setup to RXCLK	8	-	ns
tT8			Input hold from RXCLK	1	-	ns
tT9			Signal going low impedance to RXCLK	8	-	ns
tT10			Signal going high impedance to RXCLK	0	-	ns
tT11			Signal going low impedance from RXCLK	1	-	ns
tT12			Signal going high impedance from RXCLK	1	-	ns

1) The frequency should be equal or smaller than the coreclock CLOCK

9.6.4 IMA Interface

At the IMA interface the IWE8 operates in cycles of 12 system clocks. ATBTC can become active during cycle #3, the UNCHEC can become active during cycle #9. The Port number is always active for 6 cycles.

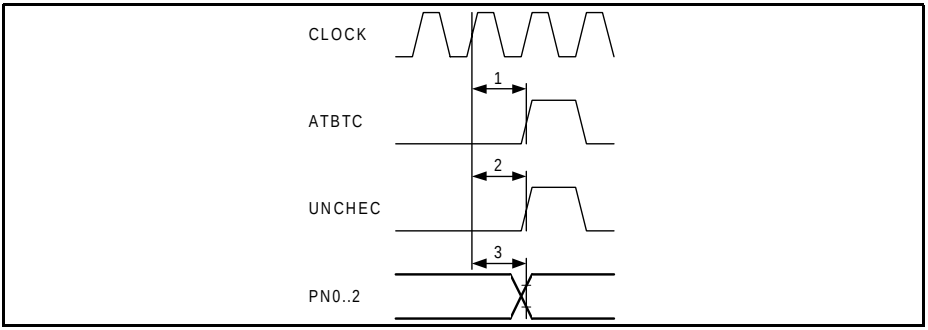


Figure 66 Timing of the IMA Interface

Table 46 IMA Interface AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	Delay master clock to ATBTC			26	ns
2	Delay master clock to UNCHEC			26	ns
3	Delay master clock to PN[0:2]			26	ns

9.6.5 Clock Recovery Interface

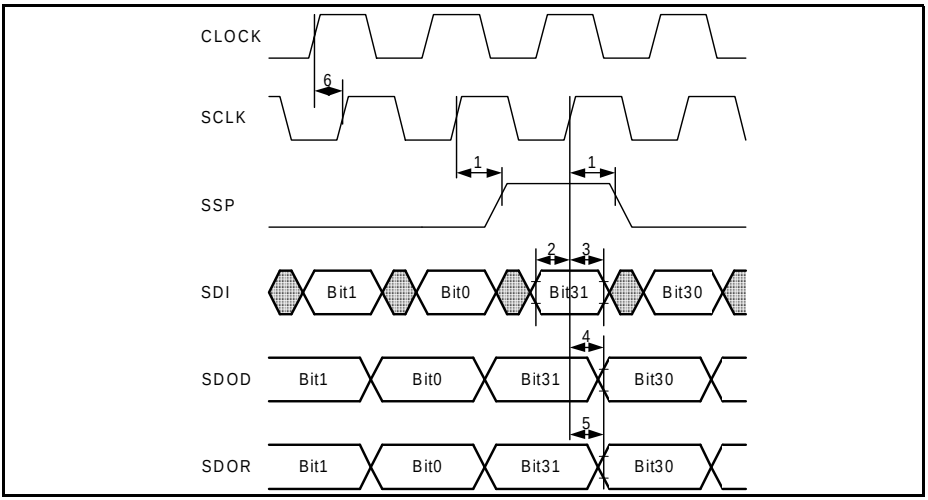


Figure 67 Clock Recovery Interface Timing Diagram

Table 47 Clock Recovery Interface AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	Delay SCLK rising to SSP	-1		11	ns
2	Setup time SDI before SCLK rising	20			ns
3	Hold time SDI after SCLK rising	0			ns
4	Delay SCLK rising to SDOD	0		11	ns
5	Delay SCLK rising to SDOR	0		11	ns
6	Delay CLOCK to SCLK	1		16	ns

9.6.6 Microprocessor Interface

9.6.6.1 Intel Mode

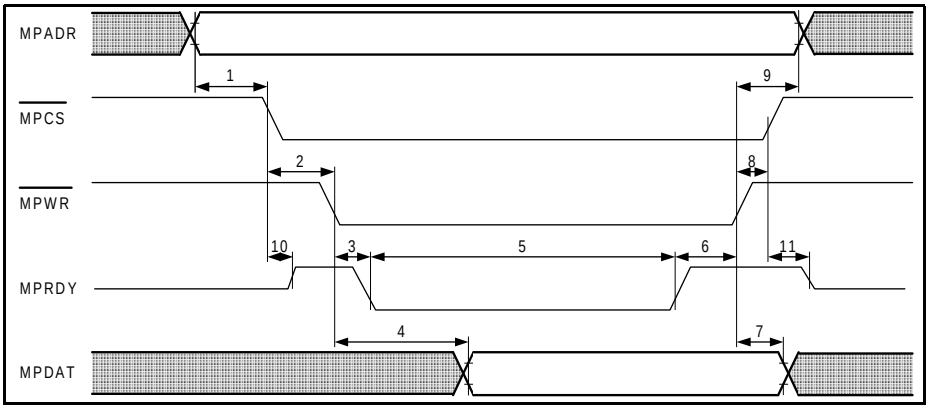


Figure 68 Intel Mode Write Cycle Timing Diagram

Table 48 Intel Mode Write Cycle AC Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	Setup time MPADR before $\overline{\text{MPCS}}$ low	0			ns
2	Setup time $\overline{\text{MPCS}}$ before $\overline{\text{MPWR}}$ low	0			ns
3	Delay MPRDY low after $\overline{\text{MPWR}}$ low	2		20	ns
4	MPDAT valid after $\overline{\text{MPWR}}$ low			2 x T_{clock}	ns
5	Pulse width MPRDY low	2 x T_{clock}		23xT_{clock}	ns
6	MPRDY high to $\overline{\text{MPWR}}$ high	10			ns
7	Hold time MPDAT after $\overline{\text{MPWR}}$ high	5			ns
8	Hold time $\overline{\text{MPCS}}$ after $\overline{\text{MPWR}}$ high	5			ns
9	Hold time MPADR after $\overline{\text{MPWR}}$ high	5			ns
10	Delay $\overline{\text{MPCS}}$ low to MPRDY high	2		20	ns
11	Delay $\overline{\text{MPCS}}$ high to MPRDY high impedance	2		20	ns

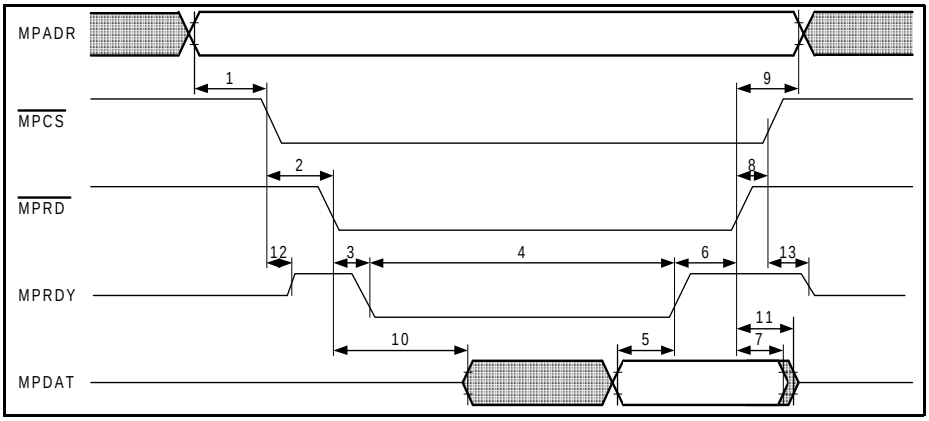


Figure 69 Intel Mode Read Cycle Timing Diagram

Table 49 Intel Mode Read Cycle AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	Setup time MPADR before $\overline{\text{MPCS}}$ low	0			ns
2	Setup time $\overline{\text{MPCS}}$ before $\overline{\text{MPRD}}$ low	0			ns
3	Delay MPRDY low after $\overline{\text{MPRD}}$ low	2		20	ns
4	Pulse width MPRDY low	2 x T_{clock}		23xT_{clock}	ns
5	MPDAT valid before MPRDY high	10			ns
6	MPRDY high to $\overline{\text{MPRD}}$ high	10			ns
7	Delay time MPDAT after $\overline{\text{MPRD}}$ high	3			ns
8	Hold time $\overline{\text{MPCS}}$ after $\overline{\text{MPRD}}$ high	5			ns
9	Hold time MPADR after $\overline{\text{MPRD}}$ high	5			ns
10	Delay $\overline{\text{MPRD}}$ low to MPDAT low impedance	4		20	ns
11	Delay $\overline{\text{MPRD}}$ high to MPDAT high impedance	5		20	ns
12	Delay $\overline{\text{MPCS}}$ low to MPRDY high	2		20	ns
13	Delay $\overline{\text{MPCS}}$ high to MPRDY high impedance	2		20	ns

9.6.6.2 Motorola Mode

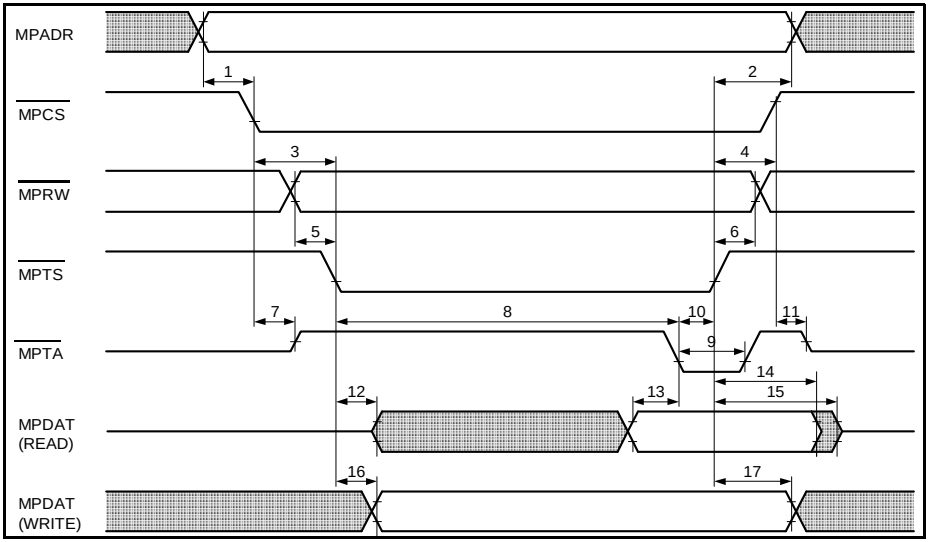


Figure 70 Motorola Mode Timing Diagram

Table 50 Motorola Mode AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	Setup time MPADR before $\overline{\text{MPCS}}$ low	0			ns
2	Hold time MPADR after $\overline{\text{MPTS}}$ high	5			ns
3	Setup time $\overline{\text{MPCS}}$ before $\overline{\text{MPTS}}$ low	0			ns
4	Hold time $\overline{\text{MPCS}}$ after $\overline{\text{MPTS}}$ high	5			ns
5	Setup time $\overline{\text{MPRW}}$ before $\overline{\text{MPTS}}$ low	10			ns
6	Hold time $\overline{\text{MPRW}}$ after $\overline{\text{MPTS}}$ high	0			ns
7	Delay $\overline{\text{MPCS}}$ low to $\overline{\text{MPTA}}$ high	5		15	ns
8	Delay $\overline{\text{MPTA}}$ low after $\overline{\text{MPTS}}$ low	2 x T_{clock}		23xT_{clock}	ns
9	Pulse width $\overline{\text{MPTA}}$ low	T_{clock}		T_{clock}	ns
10	$\overline{\text{MPTA}}$ low to $\overline{\text{MPTS}}$ high	0			ns
11	Delay $\overline{\text{MPCS}}$ high to $\overline{\text{MPTA}}$ high impedance	5		15	ns

Table 50 Motorola Mode AC Timing Characteristics (cont'd)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
12	Delay $\overline{\text{MPTS}}$ low to MPDAT low impedance	1		15	ns
13	MPDAT valid before $\overline{\text{MPTA}}$ high	5			ns
14	Delay time MPDAT after $\overline{\text{MPTS}}$ high	2			ns
15	Delay $\overline{\text{MPTS}}$ high to MPDAT high impedance	2		17	ns
16	MPDAT valid after $\overline{\text{MPTS}}$ low			2 x T_{clock}	ns
17	Hold time MPDAT after $\overline{\text{MPTS}}$ high	5			ns

9.6.7 RAM Interface

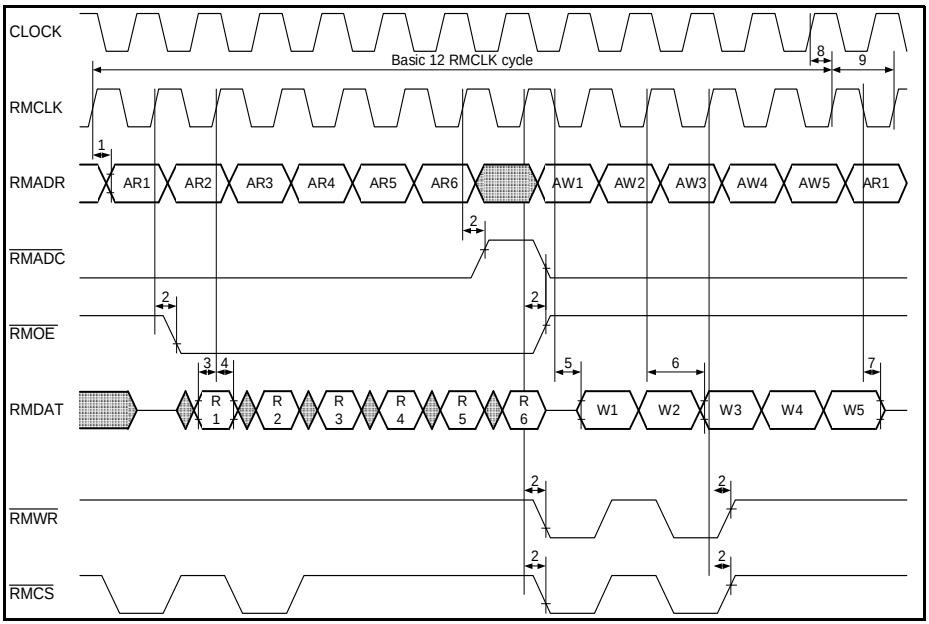


Figure 71 RAM Interface Timing Diagram

Table 51 RAM Interface AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	Delay RMCLK rising to RMADR	1		11	ns
2	Delay RMCLK rising to $\overline{\text{RMADC}}$	1		7	ns
	Delay RMCLK rising to $\overline{\text{RMOE}}$	1		7	ns
	Delay RMCLK rising to $\overline{\text{RMWR}}$	1		7	ns
	Delay RMCLK rising to $\overline{\text{RMCS}}$	1		7	ns
3	Setup time RMDAT before RMCLK rising (all read cycles)	11			ns
4	Hold time RMDAT after RMCLK rising (all read cycles)	0			ns
5	Delay RMCLK falling to RMDAT low impedance (write cycle W1)	0		8	ns
6	Delay RMCLK rising to RMDAT (write cycles W2 to W5)	6		12	ns
7	Delay RMCLK falling to RMDAT high impedance (write cycle W5)	0		8	ns
8	Delay CLOCK to RMCLK	6		12	ns
9	T_{RMCLK}: Period RMCLK		T_{CLOCK}		ns
9A	F_{RMCLK}: Frequency RMCLK		F_{CLOCK}		MHz

9.6.8 Boundary-Scan Test Interface

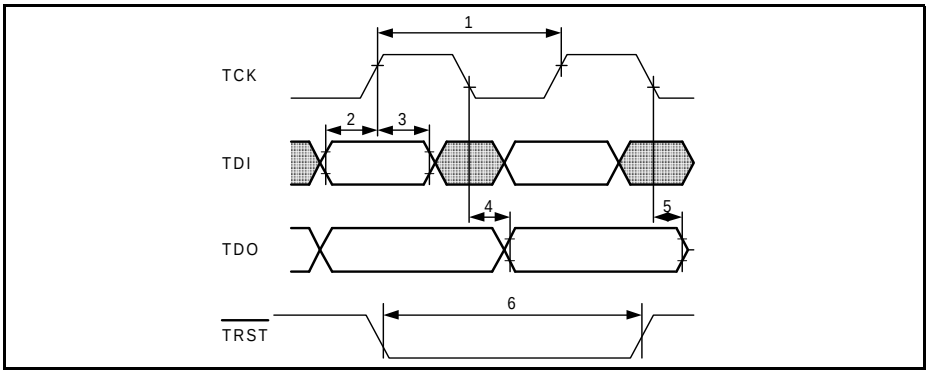


Figure 72 Boundary-Scan Test Interface Timing Diagram

Table 52 Boundary-Scan Test Interface AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{TCK}: Period TCK	160			ns
1A	F_{TCK}: Frequency TCK			6,25	MHz
2	Setup time TMS, TDI before TCK rising	10			ns
3	Hold time TMS, TDI after TCK rising	10			ns
4	Delay TCK falling to TDO valid	0		30	ns
5	Delay TCK falling to TDO high impedance	0		30	ns
6	Pulse width $\overline{TRST}$ low	2 x T_{TCK}			ns

10 Testmode

10.1 Device Identification Register

31 28	27 12	11 1	0
Version(3:0)	Partnumber(15:0)	Manufacturer-ID(10:0)	
0100_B	0000000001000110_B	00001000001_B	1

10.2 Instruction Register

The following table shows the instruction binary codes for the 4 bit instruction register.

Code Boundary-Scan Instruction Register Binary Codes

0000 = EXTEST
0001 = IDCODE
0101 = SAMPLE
0101 = INTEST
0111 = CLAMP
1111 = BYPASS

10.3 Boundary-Scan Register

Table 53 describes the Boundary-Scan register. The register contains 299 cells. The cells of type “control” will disable the corresponding outputs when set. The control cells are preset to a safe logic-1 during the TEST-LOGIC-RESET state of the TAP controller.

Table 53 Boundary Scan Register

Name	Name	Name
ftcko_4_o	rxdat_2_o	ftcko_0_o
ftcko_4_i	rxdat_3_o	ftcko_0_i
ftcko_4_c	rxdat_4_o	ftcko_0_c
ftcko_5_o	rxdat_5_o	frfrsn_0_o
ftcko_5_i	rxdat_6_o	frfrsn_0_c
ftcko_5_c	rxdat_7_o	ftdat_0_o
rtsen_n	rxprt_o[1)]	ftdat_0_c
mpcs_n	rxprt_c[1)]	ftmfs_0_o

Table 53 Boundary Scan Register (cont'd)

Name	Name	Name
mpwr_n	rxenb_o	ftmfs_0_c
mprd_n	rxenb_i	ftfrsn_0_o
mpdat_0_o	rxenb_c	ftfrsn_0_c
mpdat_0_i	rxclk	frlos_1
mpdat_c	rmclk	frclk_1
mpdat_1_o	pmt	frdat_1
mpdat_1_i	rmdat_0_o	frmfb_1
mpdat_2_o	rmdat_0_i	ftcko_1_o
mpdat_2_i	rmdat_c	ftcko_1_i
mpdat_3_o	rmdat_1_o	ftcko_1_c
mpdat_3_i	rmdat_1_i	frfrsn_1_o
mpdat_4_o	rmdat_2_o	frfrsn_1_c
mpdat_4_i	rmdat_2_i	ftdat_1_o
mpdat_5_o	rmdat_3_o	ftdat_1_c
mpdat_5_i	rmdat_3_i	ftmfs_1_o
mpdat_6_o	rmdat_4_o	ftmfs_1_c
mpdat_6_i	rmdat_4_i	ftfrsn_1_o
mpdat_7_o	rmdat_5_o	ftfrsn_1_c
mpdat_7_i	rmdat_5_i	frlos_2
mpdat_8_o	rmdat_6_o	frclk_2
mpdat_8_i	rmdat_6_i	frdat_2
mpdat_9_o	rmdat_7_o	frmfb_2
mpdat_9_i	rmdat_7_i	ftcko_2_o
mpdat_10_o	rmdat_8_o	ftcko_2_i
mpdat_10_i	rmdat_8_i	ftcko_2_c
mpdat_11_o	sdi	frfrsn_2_o
mpdat_11_i	rmdat_9_o	frfrsn_2_c
mpdat_12_o	rmdat_9_i	ftdat_2_o
mpdat_12_i	rmdat_10_o	ftdat_2_c
mpdat_13_o	rmdat_10_i	ftmfs_2_o

Table 53 Boundary Scan Register (cont'd)

Name	Name	Name
mpdat_13_i	rmdat_11_o	ftmfs_2_c
mpdat_14_o	rmdat_11_i	ftfrsn_2_o
mpdat_14_i	rmdat_12_o	ftfrsn_2_c
mpdat_15_o	rmdat_12_i	frlos_3
mpdat_15_i	tbus	frclk_3
rfclk	rmdat_13_o	frdat_3
clock	rmdat_13_i	frmfb_3
reset_n	sdod	ftcko_3_o
mprdy_o	sdor	ftcko_3_i
mprdy_c	rmdat_14_o	ftcko_3_c
pn_0	rmdat_14_i	frfrsn_3_o
mpir1_n	rmdat_15_o	frfrsn_3_c
mpir2_n	rmdat_15_i	ftdat_3_o
mpadr_0	rmdat_16_o	ftdat_3_c
mpadr_1	rmdat_16_i	ftmfs_3_o
mpadr_2	ssp	ftmfs_3_c
mpadr_3	rmdat_17_o	ftfrsn_3_o
mpadr_4	rmdat_17_i	ftfrsn_3_c
mpadr_5	rmdat_18_o	frlos_4
mpadr_6	rmdat_18_i	frclk_4
mpadr_7	rmdat_19_o	frdat_4
mpadr_8	rmdat_19_i	frmfb_4
mpadr_9	rmdat_20_o	tscsh
mpadr_10	rmdat_20_i	frfrsn_4_o
mpadr_11	sclk	frfrsn_4_c
mpadr_12	rmdat_21_o	ftdat_4_o
mpadr_13	rmdat_21_i	ftdat_4_c
mpadr_14	rmdat_22_o	ftmfs_4_o
mpadr_15	rmdat_22_i	ftmfs_4_c
mpadr_16	rmdat_23_o	ftfrsn_4_o

Table 53 Boundary Scan Register (cont'd)

Name	Name	Name
mpadr_17	rmdat_23_i	ftfrsn_4_c
licec	rmdat_24_o	frlos_5
clk52	rmdat_24_i	frclk_5
e1t1	rmdat_25_o	frdat_5
tscen	rmdat_25_i	frmfb_5
txadr_0	rmdat_26_o	frfrsn_5_o
txadr_1	rmdat_26_i	frfrsn_5_c
txadr_2	rmdat_27_o	ftdat_5_o
txadr_3	rmdat_27_i	ftdat_5_c
txadr_4	rmdat_28_o	ftmfs_5_o
rxadr_0	rmdat_28_i	ftmfs_5_c
rxadr_1	rmdat_29_o	ftfrsn_5_o
rxadr_2	rmdat_29_i	ftfrsn_5_c
rxadr_3	rmdat_30_o	frlos_6
rxadr_4	rmdat_30_i	frclk_6
pn_1	rmdat_31_o	frdat_6
pn_2	rmdat_31_i	frmfb_6
txcla_i[2)]	rmdat_32_o	frfrsn_6_o
txcla_o[2)]	rmdat_32_i	frfrsn_6_c
txcla_c[2)]	rmwr_n	ftdat_6_o
txenb_o	rmcs_n	ftdat_6_c
txenb_i	rmoe_n	ftmfs_6_o
txenb_c	rmadc_n	ftmfs_6_c
txsoc	unchec_4	ftfrsn_6_o
txdat_0	rmadr_0	ftfrsn_6_c
txdat_1	rmadr_1	frlos_7
txdat_2	rmadr_2	frclk_7
txdat_3	rmadr_3	frdat_7
txdat_4	rmadr_4	frmfb_7
txdat_5	rmadr_5	ftcko_6_o

Table 53 Boundary Scan Register (cont'd)

Name	Name	Name
txdat_6	rmadr_6	ftcko_6_i
txdat_7	rmadr_7	ftcko_6_c
txprt[3]	rmadr_8	ftcko_7_o
uttr_n	rmadr_9	ftcko_7_i
txclk	rmadr_10	ftcko_7_c
rxsoc_o	rmadr_11	frfrsn_7_o
rxsoc_c	rmadr_12	frfrsn_7_c
rxcla_o[4]	rmadr_13	ftdat_7_o
rxcla_i[4]	rmadr_14	ftdat_7_c
rxcla_c[4]	rmadr_15	ftmfs_7_o
atbtc_3	frlos_0	ftmfs_7_c
rxdat_0_o	frclk_0	ftfrsn_7_o
rxdat_c	frdat_0	ftfrsn_7_c
rxdat_1_o	frmfb_0	

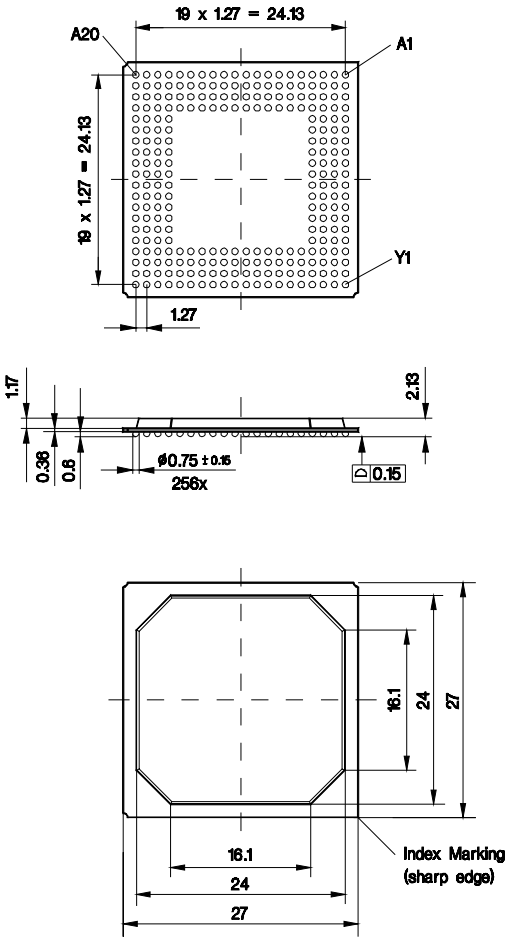
1) corresponds to pin RXPTY

2) corresponds to pin TXCLAV

3) corresponds to pin TXPTY

4) corresponds to pin RXCLAV

11 Package Outlines



Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

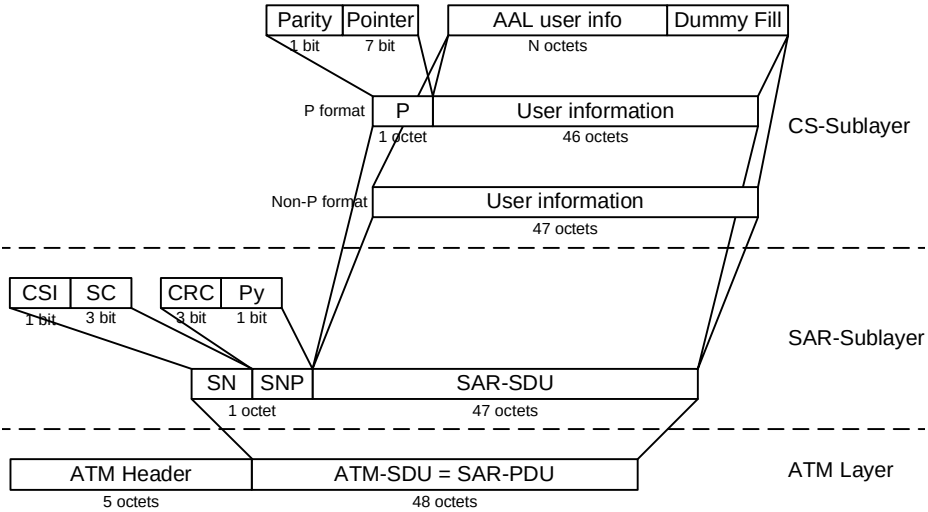
Figure 73 Package Outline: P-BGA-256 (Plastic Metric Quad Flat Package)

12 Appendix

12.1 ATM Adaptation Layer 1

The ATM Adaptation Layer 1 (AAL1) consists of two sublayers: The Segmentation and Reassembly Sublayer (SAR), which is responsible for sequence integrity of the transmitted ATM cell stream and the Convergency Sublayer, responsible for blocking of user data into 47-octet SAR boundaries.

Figure 74 gives an overview on the AAL1 frame-structure as defined in ITU-T I.363.1 [31].



Pointer = octet offset of data block over 2 cells (111 1111 if not required)
CSI = Convergency Sublayer Indication
Non-P Format: CSI = 0
P format: CSI = 1 if SC = 0,2,4 or 6, P-field may be inserted
CSI = 0 if SC = 1,3,5 or 7, P-field is unused (Non-P format used)
SC = Sequence Count
CRC = Cyclic Redundancy Check
Py = Even Parity bit
SN = Sequence Number incremented by 1 modulo 8 for each SAR-SDU
SNP = Sequence Number Protection
SAR = Segmentation & Reassembly
SDU = Service Data Unit
PDU = Protocol Data Unit

Figure 74 Structure of the AAL1 SAR-PDU

Robust Sequence Count Algorithm

This algorithm is completely described in annex D of the ETSI B-ISDN AAL type 1 Specification [17] and ITU-T I.363.1 [31] and is shown in Figure **Figure 75**.

The algorithm is described by a state machine of 5 states. A change in states within the state machine is indicated by an arrow, on which there are two distinct values represented. The first value refers to the event that originates the state change, and the second value refers to the action to be taken as a result of that event.

A decision in this algorithm is taken after evaluation of 2 consecutive SN. This means that when a cell is received it must be temporarily stored, waiting for the next cell before it is finally passed to the reassembly buffer. In the state machine, an action to be taken (accept or discard) always refers to the stored cell.

The sequence counting of modulo 8 permits that the algorithm detects a maximum of to 6 consecutive lost cells and 1 misinserted cell, assuming that misinsertion of one cell is at least as probable as the loss of 7 consecutive cells.

Lost cells are compensated by inserting an appropriate number of dummy cells into the transmitted data of the channel. This is required to maintain bit count integrity. The number of octets inserted per dummy cell is equal to the number of user information octets in the SAR-PDU payload of each cell.

When one misinserted cell is detected, the algorithm is able to delete the misinserted cell, because of the delay of one cell in taking a decision.

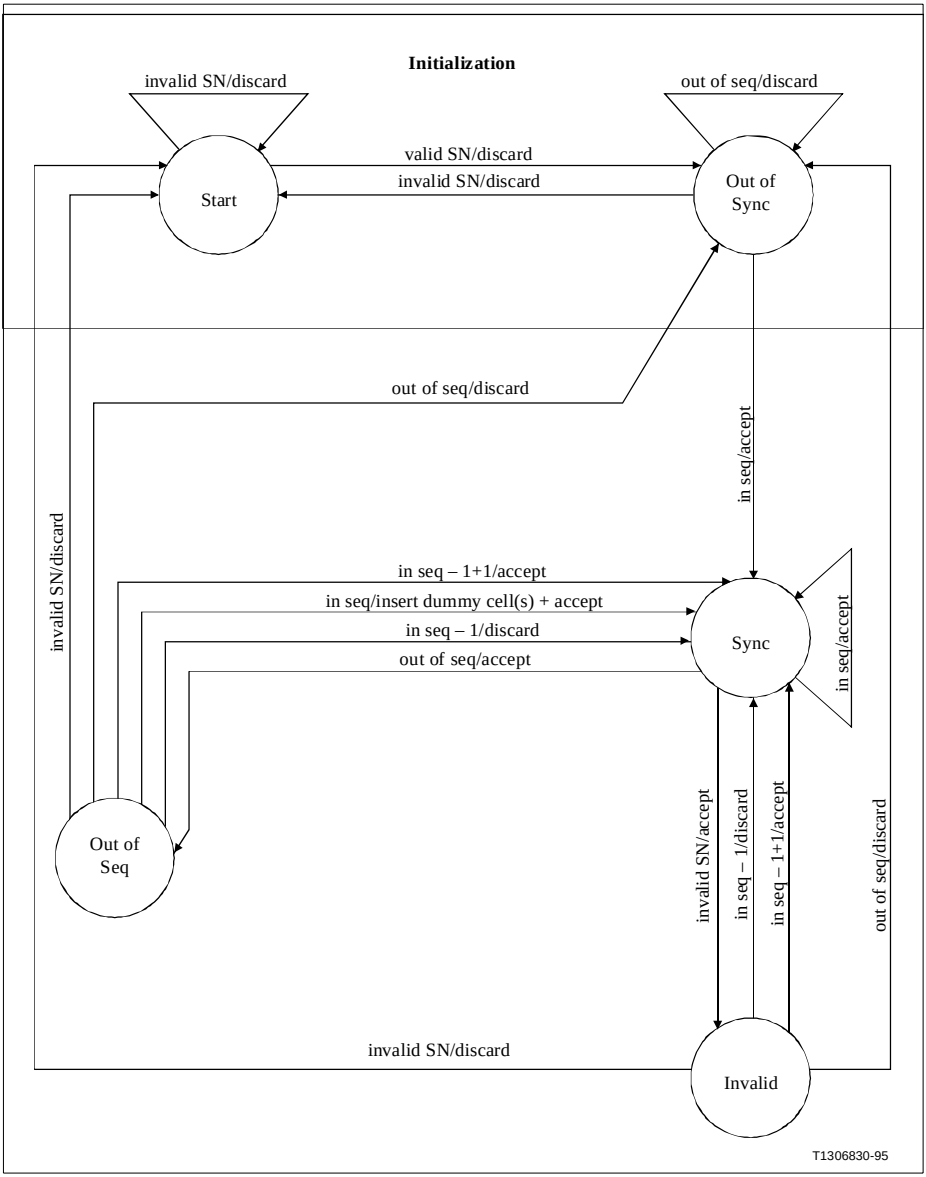


Figure 75 Informative and Example Algorithm State Machine (Fig. III.2/I.363.1)

Fast Sequence Count Algorithm

The state machines of the robust SC algorithm and the fast SC algorithm are the same. The only difference is that in the fast algorithm, the action to be taken always refers to the currently received cell, while in the standard algorithm it refers to the temporarily stored cell. Therefore the fast SC algorithm does not introduce additional one-cell delay.

In the fast SC algorithm, a misinserted cell is immediately accepted in the reassembly buffer. Only at the arrival of the next cell, it is detected that the previous cell was misinserted. Because the misinserted cell was already accepted, the current (in sequence) cell will be discarded instead. Lost cells are compensated with the insertion of dummy cells as in the standard algorithm.

Frequency and Value of the Pointer Field

The pointer field contains the binary value of the offset, measured in octets, between the end of the pointer field and the start of the structured block, in the 93 octet payload. The payload consists of the remaining 46 octets of this SAR-PDU payload and the 47 octets of the next SAR-PDU payload.

The frequency of occurrence of the pointer field is according to ITU-T I.363.1 [31]. The pointer field is used exactly once in every cycle, where a cycle is the sequence of eight consecutive SAR-PDUs with Sequence Count values 0, 1, to 7. The pointer field is used at the first available opportunity in a cycle to point to a start of a structured block. If a start of a structured block is not present in a cycle, then a pointer field containing a dummy offset value ‘127’ is used at the last opportunity in the cycle.

12.2 Synchronous Residual Time Stamp SRTS

This sub chapter contains a short description of the SRTS method, as defined in [12] and [31].

The SRTS algorithm is used to measure the frequency deviation of a data stream which is packetized in ATM cells. This frequency is coded in 4 bits and sent to the receiver. At the receiver, the correct frequency is regenerated.

The 4 RTS bits are spread over 8 ATM cells. These 8 ATM cells contain 8 x 47 byte x 8 bit/byte = 3008 bits of data. In case of an E1 line, the data arrives with 2.048 Mbit/s, thus after 3008 bit / 2.048 Mbit/s = 1,46875 ms a complete RTS value is received. The frequency of generated RTS values is 681 Hz.

The RTS value is calculated in the following way:

In N = 3008 cycles of Fdata, we have Mq cycles of the reduced network clock. The reduced network clock Fnx has to fulfil the following equation: 1 <= Fnx / Fdata < 2. This defines the value of x in the equation: Fnx = 8 kHz X 19440 / 2^x. For a full E1 line Fdata = 2.048 MHz, x = 6 and Fnx = 2.43 MHz. The maximum input frequency deviation of 200 ppm (E1 lines: less than 50 ppm) of the data clock translates in a deviation from Mq. At the receiving side, the same network clock is available and the numbers N and x are known. As a result, the nominal value Mnom of Mq is known, and only the deviation from Mnom has to be transmitted. The number of bits to transmit the deviation (p = 4) has to be sufficient for the maximum frequency deviation.

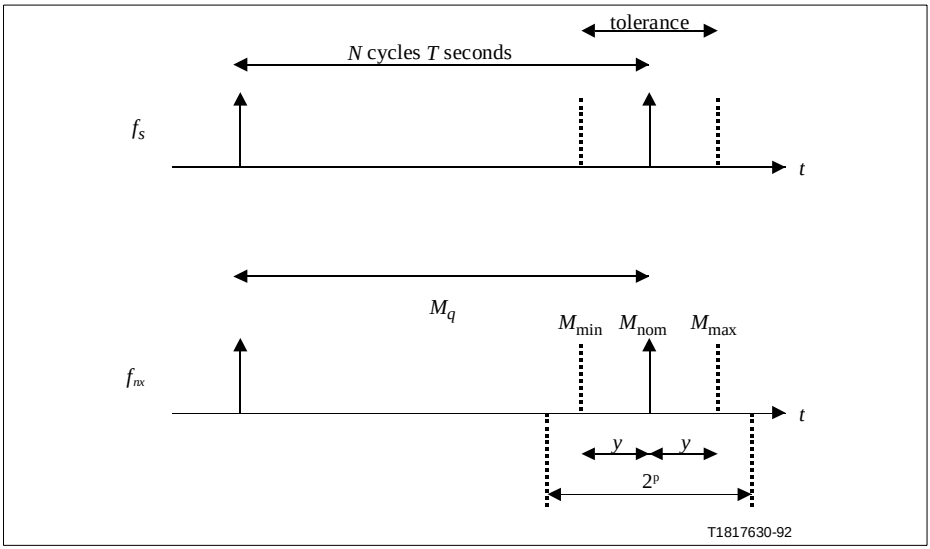


Figure 76 The Concept of Synchronous Residual Time Stamp (SRTS) (Fig. 5/ I.363.1)

RTS values are generated as follows:

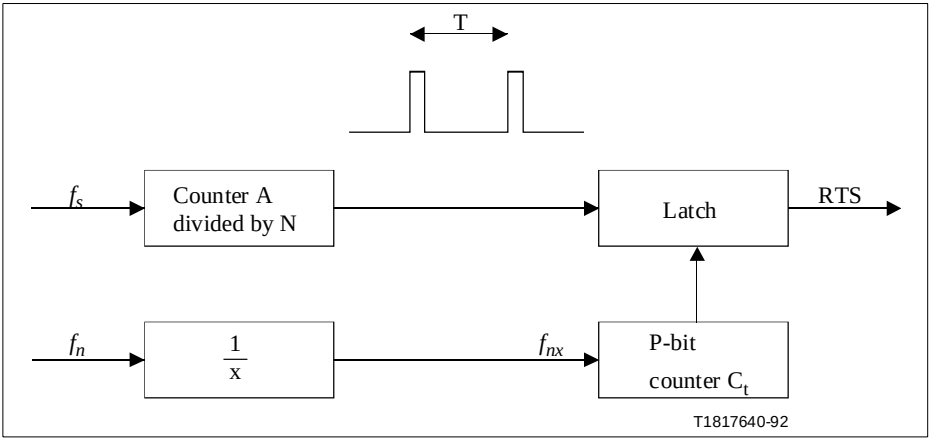


Figure 77 Generation of Residual Time Stamp (RTS) (Fig.6/ I.363.1)

The transformation of RTS values in a clock is not specified in the SRTS specifications. Basically (the implementation is slightly different), the ICRC calculates another RTS value based on the transmit clock. The difference between received RTS values and locally calculated RTS values, drives a DCO. This solution can be described as a PLL with an unusual phase comparator.

12.3 Adaptive Clock Method ACM

The adaptive clock method does not require information concerning the source clock transferred over the ATM network. The speed of the transmitter is adjusted to the filling level of the receive buffer. If the transmit clock is too slow, the buffer filling level will increase causing the clock recovery circuit to slow down the transmit clock. If the transmit clock is too fast the buffer filling level will decrease. In this case the clock recovery circuit will increase the transmit clock.

12.4 Channel Associated Signalling

ITU-T recommendation G.704 [24] defines Channel Associated Signalling (CAS) for interfaces at 2048 kbit/s (E1) and 1544 kbit/s (DS1) interfaces carrying 64 kbit/s channels. The mapping of E1 or DS1 multiframes containing CAS into ATM cells is defined in the ATM-Forum “Circuit Emulation Services Specification” [10].

In case of E1 and DS1 circuit emulation, the user information carried via AAL1 consists of a stream of payload substructures followed by an optional signalling substructure. Each payload and signalling substructure corresponds to one E1 multiframe / DS1 extended superframe. The payload substructure contains the channel slots and the optional signalling substructure contains the signalling bits associated with the channels. The following section gives an overview on this topic.

12.4.1 E1

An E1 multiframe comprises 16 consecutive frames. These are numbered from 0 to15. The multiframe alignement signal is 0000 and occupies digit time slots 1 to 4 of 64 kbit/s channel time slot 16 in frame 0.

When 64 kbit/s channel time slot 16 is used for channel-associated signalling, the 64 kbit/s capacity is sub-multiplexed into lower-rate signalling channels using the multiframe alignement signal as a reference.

Details of the bit allocation are given in **Table 54**

Table 54 Bit allocation of channel associated 64 kbit/s time slot 16 for channel associated signalling

E1 Multiframe	Bit allocation of time slot 16	
Frame 0 (CasBeginFrame)	0000	xyxx
Frame 1	abcd channel 1	abcd channel 16
Frame 2	abcd channel 2	abcd channel 17
...	...	...
Frame 15	abcd channel 15	abcd channel 30

x = spare bit, to be set to 1 if not used

y = Bit used for alarm indication to the remote end. In undisturbed operation, set to 0; in alarm condition, set to 1.

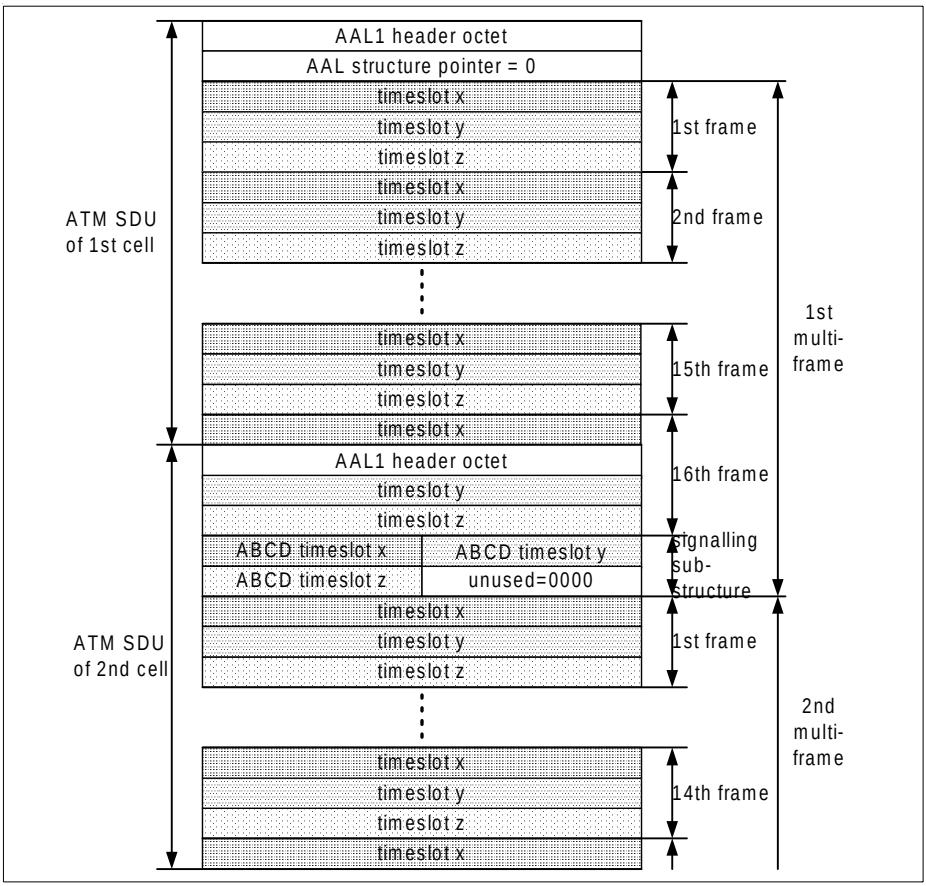


Figure 78 Example Multiframe Structure for 3x64 kbit/s E1 with CAS

12.4.2 DS1

A DS1 (T1) multiframe consists of 24 frames. They are numbered from 1 to 24. In the multiframe there are four different signalling bits (A, B, C and D) providing four independent 333 bit/s channels, two independent 667 bit/s channels or one 1333 bit/s channel. The four signalling bits for each time slot are transported in the last bit of each time slot of the frames 6, 12, 18, 24. In these frames only 7 bits are available for data transmission (Robbed Bit Signalling). When mapping DS1 Nx64 kbit/s frames into ATM cells the CAS bits may also be transmitted in the payload section. However, only the signalling bits of the CAS substructure are relevant.

Table 55 Allocation of Channel Associated Signalling Bits to 24 Frame Multiframe

DS1 Multiframe	Digit time slot in each channel used for		Signalling channel identifier		
	Characters	Signalling	333 bit/s	667 bit/s	1333 bit/s
Frame 1 (CasBeginFrame) - Frame 5	1-8	-	-	-	-
Frame 6	1-7	8	A	A	A
Frame 7 - Frame 11	1-8	-	-	-	-
Frame 12	1-7	8	B	B	A
Frame 13 - Frame 17	1-8	-	-	-	-
Frame 18	1-7	8	C	A	A
Frame 19 - Frame 23	1-8	-	-	-	-
Frame 24	1-7	8	D	B	A

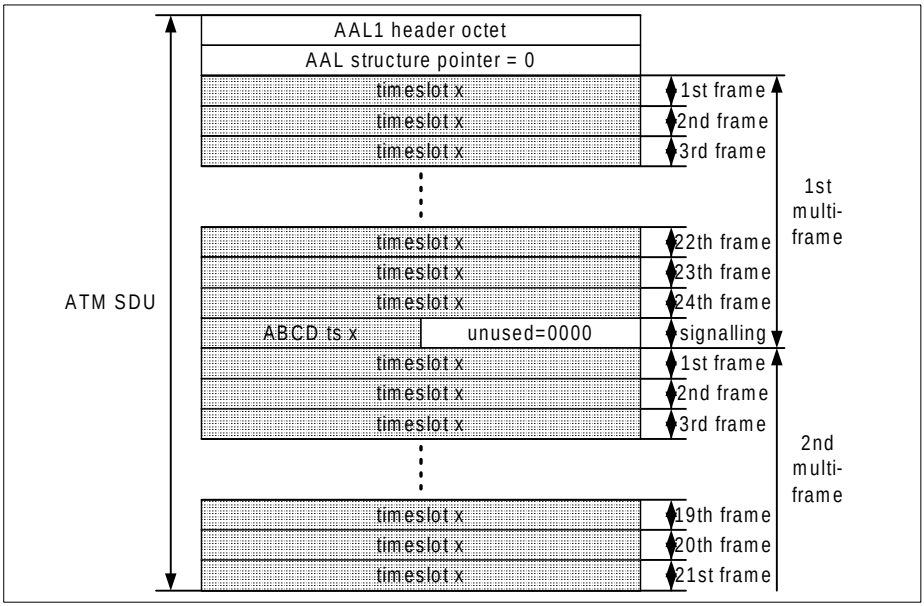


Figure 79 Example Multiframe Structure for 1x64 kbit/s DS1 with CAS

13 Contacts for SRTS Patent Fee

When using the PXB4220 a patent fee for the SRTS clock recovery needs to be paid to Telcordia Technologies, Inc.:

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14 Glossary

AAL	ATM Adaptation Layer
ACM	Adaptive Clock Method
ATM	Asynchronous Transfer Mode
B-ISDN	Broadband - Integrated Services Digital Network
CBR	Constant Bit Rate
CDV	Cell Delay Variation
CES	Circuit Emulation Service
CLP	Cell Loss Priority
CRC	Cyclic Redundancy Check
CS	Convergence Sublayer
CSI	Convergence Sublayer Indication
DCO	Digitally Controlled Oscillator
DS1	Digital Signal 1 (1.544 Mbit/s) (=T1)
EC	Echo Canceller
FALC	Framer And Line Interface Component
FAM	FALC Mode
FIFO	First In, First Out Buffer
FS/DL	Frame Sync/Data Link
FSM	Finite State Machine
GFC	Generic Flow Control
GIM	Generic Interface Mode
HEC	Header Error Control
I/O	Input/Output
ICRC	Internal Clock Recovery Circuit
ITU	International Telecommunications Union
ITU-T	International Telecommunications Union - Telecommunications Standardization Sector
IWE8	Interworking Element component for 8 channels PXB 4220
IWECORE	IWE8 without ICRC
LCD	Loss of Cell Delineation
LIC	Line Interface Card or Line Interface Circuit

LOS	Loss of Signal
LSB	Least Significant Bit
MSB	Most Significant Bit
NIC	Network Interface Controller or Card
NNI	Network-to-Network Interface
OAM	Operation, Administration, and Maintenance
OCD	Out of Cell Delineation
PDU	Protocol Data Unit
PHY	Physical Layer Device
PTI	Payload Type Identifier
RTS	Residual Time Stamp
SAR	Segmentation And Reassembly
SARE	Segmentation And Reassembly Element, PXB 4110
SC	Sequence Count
SDT	Structured Data Transfer
SN	Sequence Number
SNP	Sequence Number Protection
SRTS	Synchronous Residual Time Stamp
SSRAM	Synchronous Static RAM
SYM	Synchronous Mode
TAP	Test Access Port
TBD	To Be Defined
UDT	Unstructured Data Transfer
UNI	User-to-Network Interface
UTOPIA	Universal Test and Operations Physical Interface for ATM
UTOPIA Receive Interface (Upstream)	Data is transferred from the PHY Layer (in this case the IWE8) to the ATM Layer.
UTOPIA Transmit Interface (Downstream)	Data is transferred from the ATM Layer to the PHY Layer (in this case the IWE8).
VC	Virtual Channel

VCI	Virtual Channel Identifier
VP	Virtual Path
VPI	Virtual Path Identifier

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