Analog Frequency Multiplier

VCXO Family of Products

PRODUCT DESCRIPTION

PhaseLink's Analog Frequency Multiplier™ (AFMs) are the industry's first 'Balanced Oscillator' utilizing analog multiplication of the fundamental frequency (at double or quadruple frequency), combined with an attenuation of the fundamental of the reference crystal, without the use of a phase locked loop, in CMOS technology.

PhaseLink's patent pending PL56X family of AFM products can achieve up to 800 MHz output frequency with practically no jitter or phase noise deterioration. In addition, the low frequency input crystal requirement makes the AFMs the most affordable high performance timing source in the market.

PL560-XX family of products utilize a low-power CMOS technology and are housed in a 16-pin (T)SSOP, and 16-pin 3x3 QFN.

FEATURES

- Non Phase Locked Loop frequency multiplication
- Input frequency from 30-200 MHz
- Output frequency from 60-800-MHz
- Low Phase noise and jitter (equivalent to fundamental crystal at the output frequency)
- Unbeatably low jitter
  - RMS phase jitter < 0.25ps (12kHz-20MHz)
  - RMS period jitter < 2.5 ps
- Low Phase Noise
  - -142 dBc/Hz @100kHz Offset from 155.52MHz
  - -150 dBc/Hz @10MHz Offset from 155.52MHz
- High linearity pull range (typ. 5%)
- +/- 120 PPM pullability VCXO
- Low input frequency eliminates the need for expensive crystals
- Differential output levels (PECL, LVDS), or single-ended CMOS
- Single 2.5V or 3.3V +/- 10% power supply
- Optional industrial temperature range (-40°C to +85°C)
- Available in 16-pin (T) SSOP, and 3x3 QFN

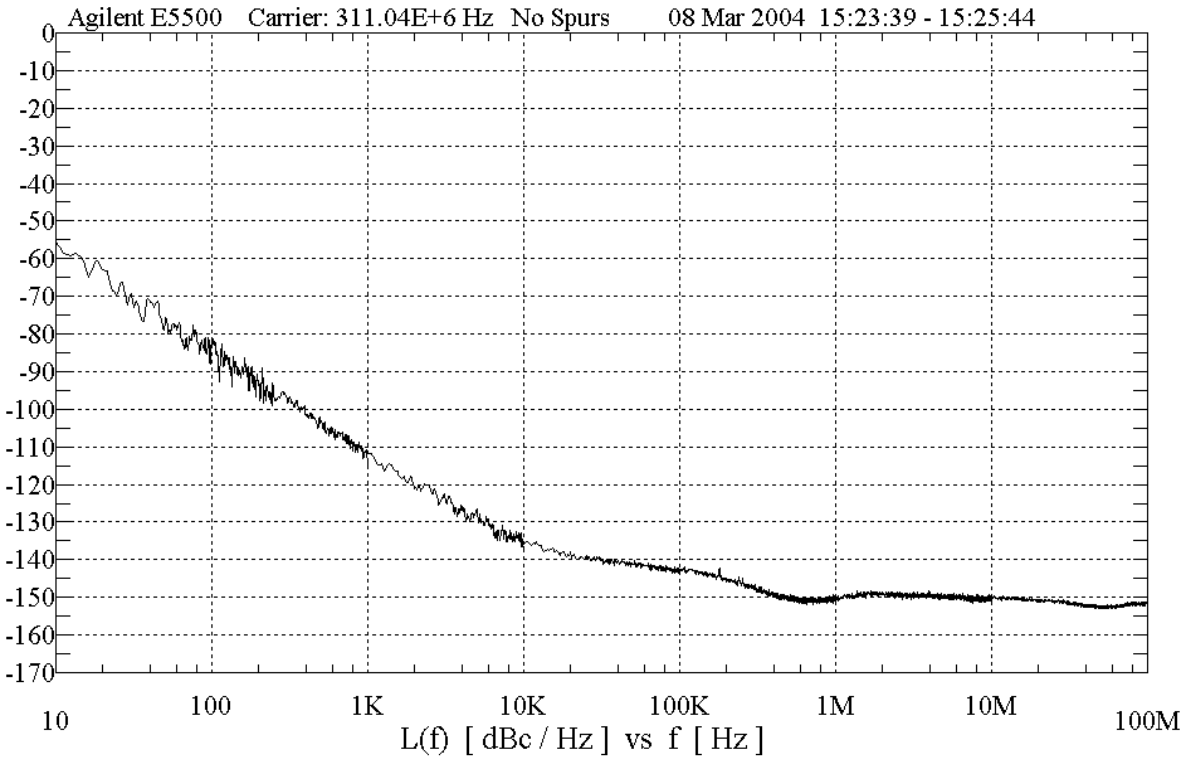


Figure 1: 2x AFM Phase Noise at 311.04MHz

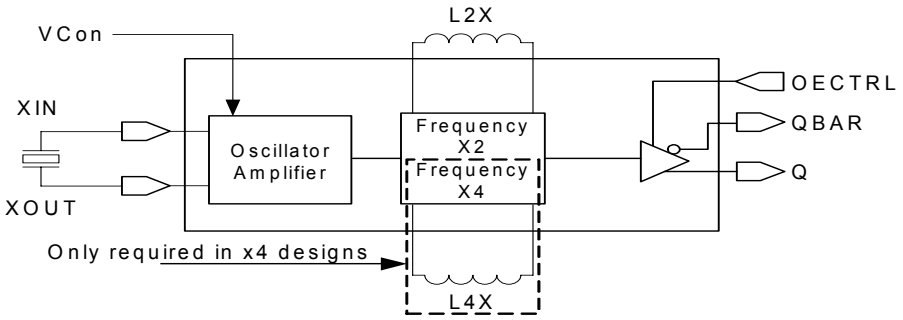


Figure 2: Overall VCXO AFM Block Diagram

Figure 3 shows the jitter histogram of the 2x Analog Frequency Multiplier at 155.52MHz, while figure 4 shows the very low rejection levels of sub-harmonics that correspond to the exceptionally low jitter performance.

Figure 3: Jitter Histogram at 311.04 MHz
Analog Frequency Multiplier (2x)
with 155.52MHz crystal

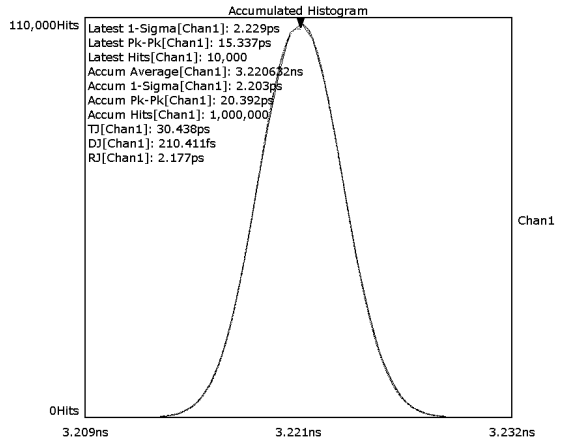
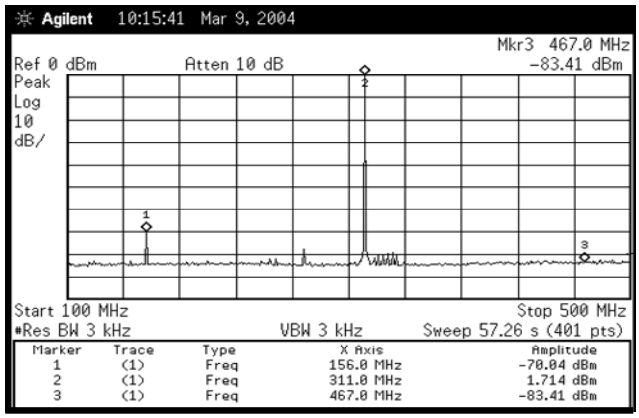


Figure 4: Spectrum Analysis at 311.04 MHz
Analog Frequency Multiplier (2x)
with sub-harmonic below –72 dBc



OE LOGIC SELECTION

OUTPUT	OESEL	OE	Output State
PECL	0 (Default)	0 (Default)	Enabled
		1	Tri-state
	1	0	Tri-state
		1 (Default)	Enabled
LVDS or CMOS	0 (Default)	0	Tri-state
		1 (Default)	Enabled
	1	0 (Default)	Enabled
		1	Tri-state

OESEL and OE: Connect to VDD to set to "1", connect to GND to set to "0". Internally set to default through pull-down / -up.

PRODUCT SELECTION GUIDE

FREQUENCY VERSUS PHASE NOISE PERFORMANCE

Part Number	Input Frequency Range (MHz)	Analog Frequency Multiplication Factor	Output Frequency Range (MHz)	Output Type	Phase Noise AT Frequency Offset From Carrier (dBc/Hz)							
					Carrier Freq. (MHz)	10 Hz	100 Hz	1 KHz	10 KHz	100 KHz	1 MHz	10 MHz
PL560-08	75 - 200	4	300 - 800	PECL	622.08	-55	-85	-110	-130	-137	-148	-150
PL560-09	75 - 200	4	300 - 800	LVDS	622.08	-55	-85	-110	-130	-137	-148	-150
PL560-37	30 - 80	4	120 - 320	CMOS	155.52	-50	-82	-110	-128	-142	-148	-150
PL560-38	30 - 80	4	120 - 320	PECL	155.52	-50	-82	-110	-128	-142	-148	-150
PL560-39	30 - 80	4	120 - 320	LVDS	155.52	-50	-82	-110	-128	-142	-148	-150
PL560-47	30 - 80	2	60 - 160	CMOS	155.52	-65	-95	-122	-138	-142	-148	-149
PL560-48	30 - 80	2	60 - 160	PECL	155.52	-65	-95	-122	-138	-142	-148	-149
PL560-49	30 - 80	2	60 - 160	LVDS	155.52	-65	-95	-122	-138	-142	-148	-149
PL560-68	75 - 200	2	150 - 400	PECL	311.04	-60	-85	-112	-135	-142	-150	-151
PL560-69	75 - 200	2	150 - 400	LVDS	311.04	-60	-85	-112	-135	-142	-150	-151

Phase Noise numbers were obtained using Agilent 5500.

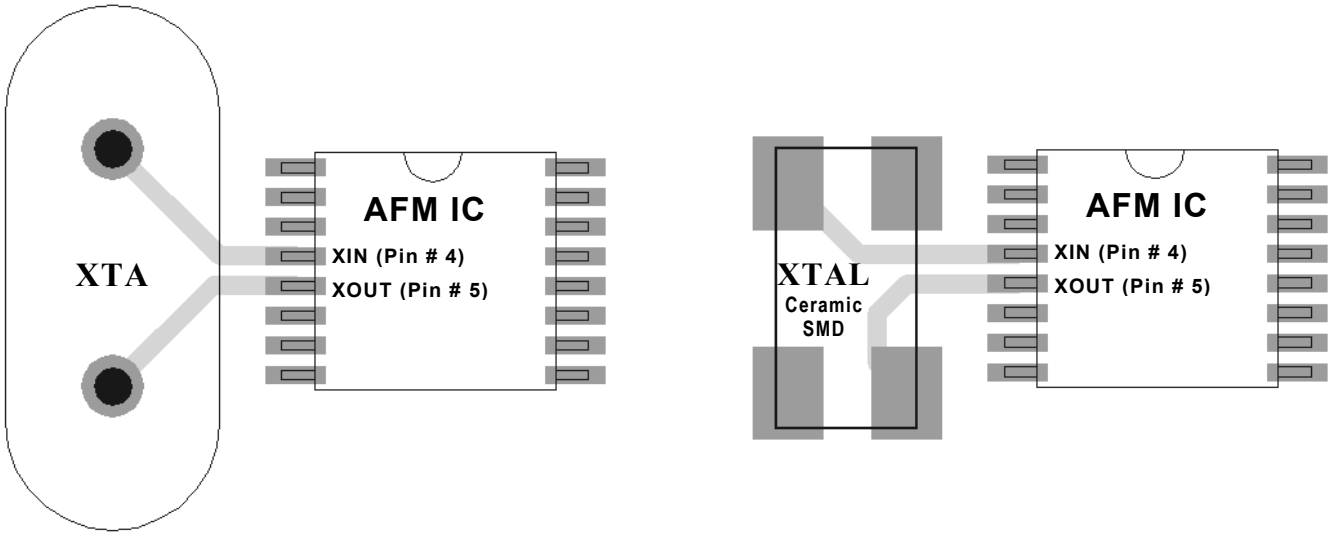
FREQUENCY VERSUS JITTER, AND SUB-HARMONIC PERFORMANCE

Part Number	Jitter Calc. Freq. (MHz)	RMS Period Jitter (Ps)			Peak to Peak Period Jitter (Ps)			RMS Accumulated (L.T.) Jitter (Ps)			Phase Jitter (12 KHz-20MHz) (Ps)			Spectral Specifications / Sub-harmonic Content (dB), Frequency (MHz)						
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Carrier Freq. (Fc)	@ -75% (Fc)	@ -50% (Fc)	@ -25% (Fc)	@ +25% (Fc)	@ +50% (Fc)	@ +75% (Fc)
PL560-08	622		4	6		25	30			6		0.09		622	-50	-50	-45	-47	-47	-55
PL560-09	622		4	6		25	30			6		0.09		622	-50	-50	-45	-47	-47	-55
PL560-37	155		2.5	3		18	20			3		0.25		155.52	-75	-62			-65	-75
PL560-38	155		2.5	3		18	20			3		0.25		155.52	-75	-62			-65	-75
PL560-39	155		2.5	3		18	20			3		0.25		155.52	-75	-62			-65	-75
PL560-47	155		2.5	3		18	20			3		0.25		155.52		-68			-68	
PL560-48	155		2.5	3		18	20			3		0.25		155.52		-68			-68	
PL560-49	155		2.5	3		18	20			3		0.27		155.52		-68			-68	
PL560-68	311		2.5	3		18	20			3		0.18		311.04		-72			-85	
PL560-69	311		2.5	3		18	20			3		0.18		311.04		-72			-85	

Note: Wavecrest Data 10,000 hits. No Filtering was used in Jitter Calculations.
Agilent 5500 was used for Phase Jitter Calculations.
Spectral Specifications were obtained using Agilent E7401A.

CRYSTAL SPECIFICATIONS AND BOARD LAYOUT CONSIDERATIONS

BOARD LAYOUT CONSIDERATIONS



To minimize parasitic effects, and improve performance:

- Place the crystal as close as possible to the IC.
- Make the board traces that are connected to the crystal pins symmetrical.
- The board trace symmetry is important, as it reduces the negative parasitic effects, for a clean frequency multiplication with low jitter. Parasitic have negative effect on frequency pulling of a VCXO and jitter.

CRYSTAL SPECIFICATIONS & TUNING PERFORMANCE

CRYSTAL SPECIFICATIONS						TUNING PERFORMANCE					
PART NUMBER	CRYSTAL RESONATOR FREQUENCY (FXIN)	MODE	CL (xtal)		ESR (R_E)	CRYSTAL				TUNING (Typical)	
			CONDI-TIONS	TYP.	Max.	CRYSTAL FREQ (MHz)	C0	C1	C0/C1	VC: 1.65V→ 0V	VC: 1.65V→ 3.4V
PL560-08/09 PL560-68/69	75~200MHz	Funda-mental	At Vcon = 1.65V	5pF	30 Ω	155.52	3.0pF	12.2fF	245	-145 ppm	+108 ppm
						155.52	1.8pF	5.7fF	316	-134 ppm	+87 ppm
PL560-37/38/39 PL560-47/48/49	30~80MHz	Funda-mental	At Vcon = 1.65V	5pF	30 Ω	30.72	2.8pF	12.4fF	228	-167ppm	+176ppm
						30.72	4.5pF	19.1fF	236	-163ppm	+167ppm
						38.88	5.1pF	20.9fF	242	-131ppm	+98ppm
						38.88	5.3pF	25.6fF	207	-157ppm	+141ppm
						77.76	2.0pF	6.7fF	305	-92ppm	+110ppm

Note: Non specified parameters can be chosen as standard values from crystal suppliers.
CL ratings larger than 5pF require a crystal frequency adjustment. Request detailed crystal specifications from PhaseLink.

VOLTAGE CONTROL SPECIFICATION

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range		XTAL C_0 /C_1 <300	200			ppm
CLK output pullability		VCON= 1.65V ± 1.65V XTAL C_0 /C_1 <300	±100	±120		ppm
Linearity				5	10	%
VCON input impedance			130			kΩ
VCON modulation BW		0V < VCON < 3.3V, -3dB	25			kHz

EXTERNAL COMPONENT VALUES

INDUCTOR VALUE OPTIMIZATION

The required inductor value(s) for the best performance depends on the operating frequency, and the board layout specifications. The listed values in this datasheet are based on the calculated parasitic values from PhaseLink's evaluation board design (Gerber file available upon request). These inductor values provide the user with a starting point to determine the optimum inductor values. Additional fine-tuning may be required to determine the optimal solution.

To assist with the inductor value optimization, PhaseLink has developed the "AFM Tuning Assistant" software. You can download this software from PhaseLink's web site (www.phaselink.com). The software consists of two worksheets. The first worksheet (named L2) is used to fine-tune the 'L2' inductor value, and the second worksheet (named L4) is used for fine tuning of the 'L4' (used in 4x AFMs only) inductor value.

For those designs using PhaseLink's recommended board layout, you can use the "AFM Tuning Assistant" to determine the optimum values for the required inductors. This software is developed based on the parasitic information from PhaseLink's board layout and can be used to determine the required inductor and parallel capacitor (see LWB1 and Cstray parameters) values. For those employing a different board layout in their design, we recommend to use the parasitic information of their board layout to calculate the optimized inductor values. Please use the following fine tuning procedure:

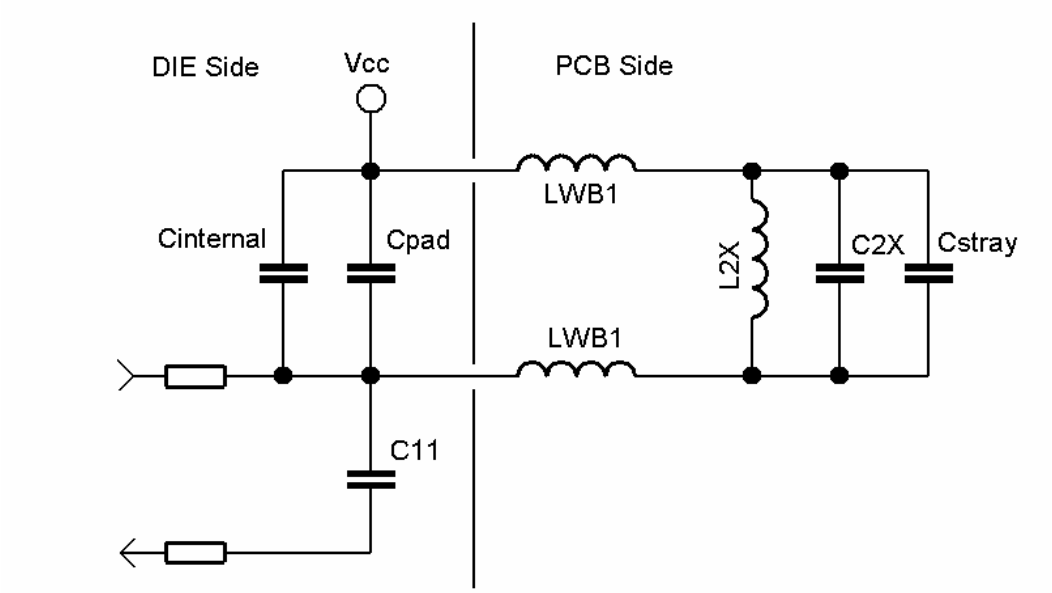


Figure 5: Diagram Representation of the Related System Inductance and Capacitance

DIE SIDE
- Cinternal = Based on AFM Device
- Cpad = 2.0 pF, Bond pad and its ESD circuitry
- C11 = 0.4 pF, The following amplifier stage

PCB side
- LWB1 = 2 nH, (2 places), Stray inductance
- Cstray = 1.0 pF, Stray Capacitance
- L2X (L4X) = 2x or 4x inductor
- C2X (C4X) = range (0.1 to 2.7), Fine tune inductor if used

- There are two default variables that normally will not need to be modified. These are Cpad, and C11 and are found in cells B22 and B27 of 'AFM Tuning Assistant', respectively.
- LWB1 is the combined stray inductance in the layout. The DIE wire bond is ~ 0.6 nH and in the case of a leaded part an additional 1.0 nH is added. Your layout inductance must be added to these. There are 2 of these and they are assumed to be approximately symmetrical so you only need to enter this inductance once in cell B23.
- Enter the stray parasitic capacitance into cell B26. An additional 0.5 pF must be added to this value if a leaded part is used.
- Enter the appropriate value for Cinternal into B21 based on the device used (see column D). Use the 'AFM Tuning Assistant' software to calculate L2X (and C2X if used) for your resonance frequency.
- For 4X AFMs, repeat the same procedure in the L4X worksheet.
- See the examples below.

DETERMINING STRAY L's AND C's IN A LAYOUT

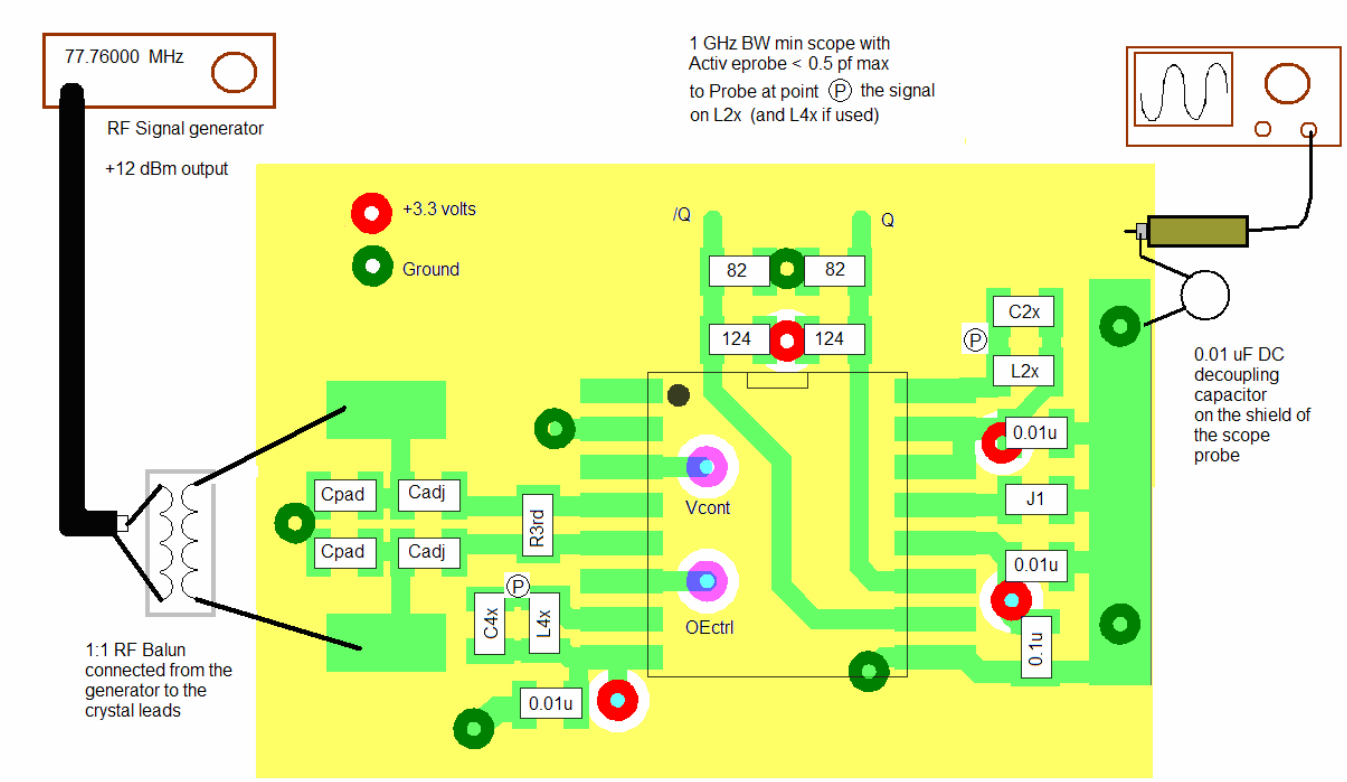


Figure 5: Diagram Representation of the Board Layout

Lets take the PL560-38 (4x VCXO) for example. This takes a crystal input range of 30 to 80 MHz and multiplies this to an output of 120 to 320 MHz. To determine the stray L's and C's of the layout we will assemble two test units. One AFM will be tuned to the lower range of the device (120 MHz), and the other to the upper range of the device (320 MHz).

120 MHz AFM Tuning: Using the "AFM Tuning Assistant" find the PL560-3x in the L2x worksheet. Enter the Cinternal value found next to it into cell B21. In cell B24 enter the closest standard inductor value (see CoilCraft 0603CS series for example) to achieve the closest peak frequency to 60 MHz. Repeat the same procedure for L4x at 120 MHz.
Results: L2X = 180 nH, L4X = 82 nH.

320 MHz AFM tuning: Repeat the previous procedure for L2x at 120 MHz and L4x at 320 MHz.
Results: L2X = 24 nH, L4X = 10 nH.

Proceed and assemble the test units.

Measuring 120 MHz L2x: Connect the RF generator and scope probe as shown in Figure 6, above. While power is applied to the PCB, set the generator output to +12 dBm and the frequency to 30 MHz. Since this is the 2x port, the scope will show 60 MHz with ~ 3v pk-pk amplitude. Vary the generator above and below 30 MHz until the amplitude on the scope is maximum and record the generator frequency. For example peak accorded at 29.8x2 or 59.6 MHz.

Measuring 320 MHz L2x: Connect the RF generator and scope probe as shown in Figure 6, above. While power is applied to the PCB, set the generator output to +12 dBm and the frequency to 80 MHz. Since this is the 2x port the scope will show 160 MHz with ~ 3v pk-pk amplitude. Vary the generator above and below 80 MHz until the amplitude on the scope is maximum and record the generator frequency. For example peak accorded at 78.0 x 2 = 156 MHz

In the AFM Tuning Assistant, add the scope's probe capacitance to the Cstray cell. For our example 0.5 pF + 1.0 pF = 1.5 pF. With L2X at 24 nH adjust LWB1 (cell B23) until the peak frequency reads 156 MHz. Next replace the L2x value with 180 nH and see if it peaks at 59.6 MHz. IF it it does not, adjust the Cstray until 59.4 MHz is achieved. Again enter 24 nH for L2x and fine tune LWB1 for 156 MHz.
Results: LWB1 = 1.6 nH, Cstray = 2.9 pF-0.5 pF = 2.4 pF (subtract scope probe stray)

Repeat the same steps for the L4X: Set the generator to 80 MHz. The 82 nH peaks at 118 MHz and the 10 nH peaks at 304 MHz.
Results: LWB1 = 1.8 nH, Cstray = 2.5 pF-0.5 pF = 2.0 pF (subtract scope probe stray)

Internal Capacitor Selection by Device		
Device Number	**Cinternal (pF)**	
	2X	**4X**
P560-0X	7.625	6.250
P560-3X	34.125	16.500
P560-4X	34.125	
P560-6X	7.625	

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

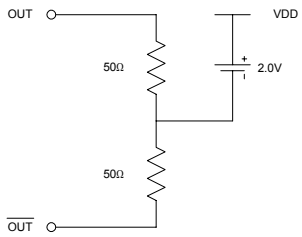
PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature	T_A	-40	+85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

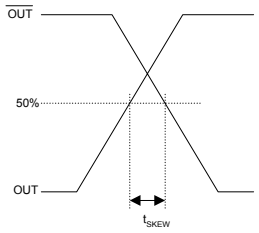
PECL ELECTRICAL CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (with loaded outputs)	I_{DD}	Fout = 622.08		75	80	mA
Operating Voltage	V_{DD}		2.25		3.63	V
Output Clock Duty Cycle		@ Vdd – 1.3V	45	50	55	%
Short Circuit Current				±50		mA
Output High Voltage	V_{OH}	R_L = 50 Ω to (V_{DD} – 2V)	V_{DD} – 1.025			V
Output Low Voltage	V_{OL}				V_{DD} – 1.620	V
Clock Rise Time	t_r	@20/80%		0.25	0.45	ns
Clock Fall Time	t_f	@80/20%		0.25	0.45	ns

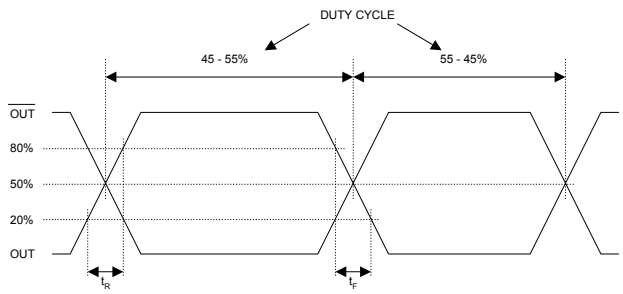
PECL Levels Test Circuit



PECL Output Skew



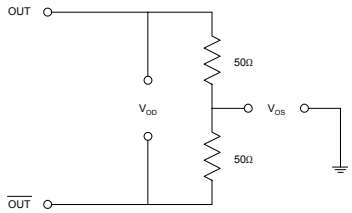
PECL Transistion Time Waveform



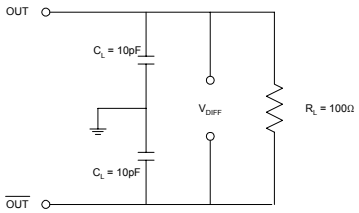
LVDS ELECTRICAL CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (with loaded outputs)	I_{DD}	Fout = 622.08, LVDS		55	60	mA
Operating Voltage	V_{DD}		2.97		3.63	V
Output Clock Duty Cycle		@ 1.25V (LVDS)	45	50	55	%
Short Circuit Current				±50		mA
Output Differential Voltage	V_{OD}	R_L = 100 Ω (see figure)	247	355	454	mV
VDD Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	V_{out} = V_{DD} or GND VDD = 0V		±1	±10	µA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA
Differential Clock Rise Time	t_r	R_L = 100 Ω CL = 10 pF (see figure)	0.2	0.5	0.7	ns
Differential Clock Fall Time	t_f		0.2	0.5	0.7	ns

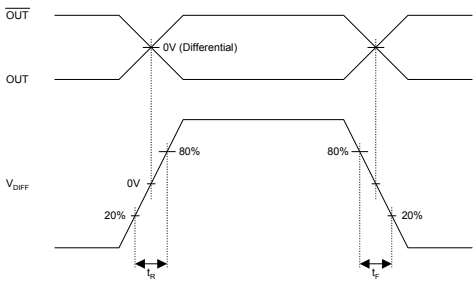
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



CMOS ELECTRICAL CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	At 100MHz, load=15pF		16	20	mA
Operating Voltage	V_{DD}		2.25		3.63	V
Output High Voltage	V_{OH}	I_{OH} = -8.5mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 8.5mA			0.4	V
Output High Voltage at CMOS level	V_{OHC}	I_{OH} = -4mA	V_{DD}– 0.4			V
Output drive current	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V (per output)		8.5		mA
Output Clock Rise/Fall Time	T_r/T_f	10% ~ 90% VDD with 10 pF load		1.2	1.6	ns
Output Clock Duty Cycle		Measured @ 50% VDD	45	50	55	%
Short Circuit Current	I_S			±50		mA

BOARD LAYOUT DESIGN CONSIDERATIONS FOR AFMs

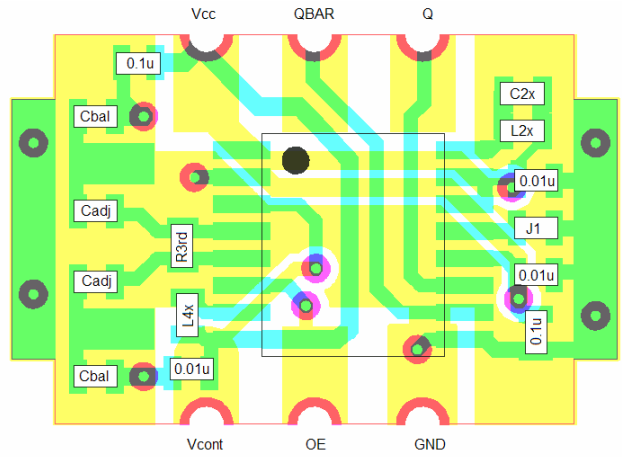
L2x and L4x: Try to reduce the PCB trace inductance to a minimum by placing L2x and L4x as physically close to their respective pins as possible. Also be sure to bypass each Vdd connection especially taking care to place a 0.01 uF bypass at the Vdd side of L2x and L4x (See recommended layout).

Crystal connections: Be sure to keep the ground plane under the crystal connections continuous so that the stray capacitace is consistent on both crystal connections. Also be sure to keep the crystal connections symmetrical with respect to one another and the crystal connection pins of the IC. If you chose to use a series capacitance and or inductor to fine tune the crystal frequency be sure to put symmetrical pads for this cap on both crystal pins (see Cadj in recommended layout). Even if one of the capacitors with be a 0.01 uf and the other is used to tune the frequency. And to further maintain a symmetrical balance on a crystal that may have more internal Cstray on one pin or the other. Place capacitor pads (Cbal) on each crystal lead to ground (see recommended layout). You can refer to (xxx) if tuning of Cbal is required. R3rd is only required if a 3rd overtone crystal is used.

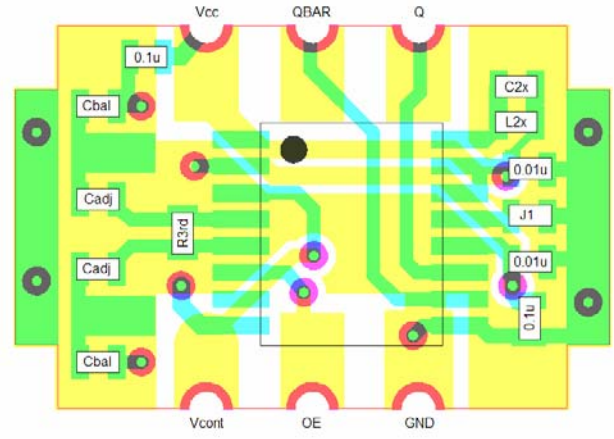
Vdd and Gnd: Bypass VDDANA and VDDBUF with separate bypass capacitors and if a Vdd plane is used feel each bypass cap with its own via. And be sure to connect any ground pin including the bypass caps with short via connection to the ground plane.

OESEL: J1 is recommended so the same PCB layout can be used for both Output Enable low (No J1) or Output Enable high (J1 = ohms) if this function is chosen.

Note: Please contact PhaseLink for the Gerber files of the board layouts.

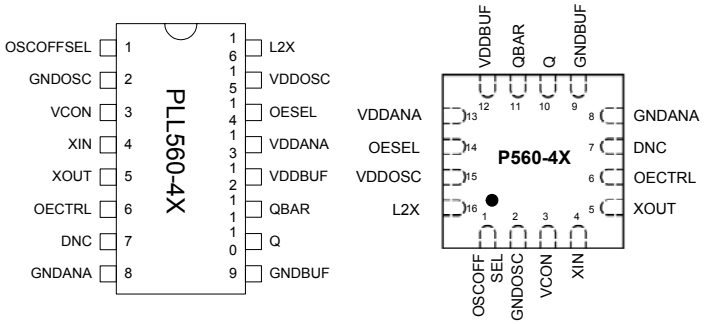


4X Layout

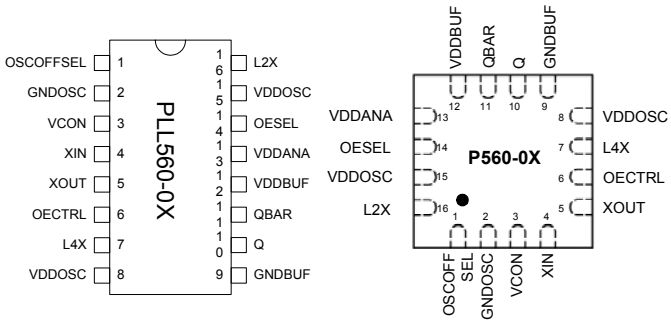


2X Layout

PACKAGE PIN DESCRIPTION AND ASSIGNMENT



2X AFM Package Pin Out



4X AFM Package Pin Out

PIN ASSIGNMENTS

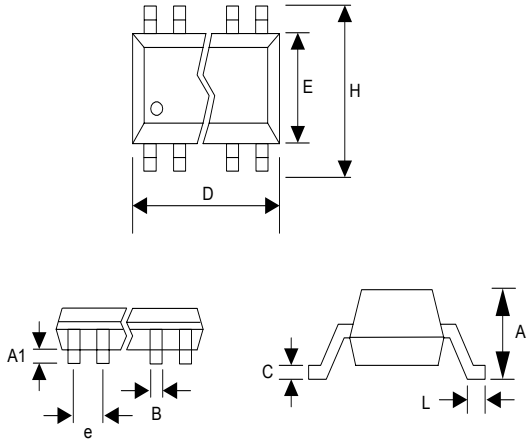
Name	Pin#	Type	Product	Description
OSCOFFSEL	1	I	2X & 4X	Set to "0" (GND) to choose to turn off the oscillator when outputs are disabled (OE). Default (no connect) is OSC always on.
GNDOSC	2	P	2X & 4X	GND connection for oscillator circuitry.
VCON	3	I	2X & 4X	Control Voltage input. Use this pin to change the output frequency by varying the applied Control Voltage.
XIN	4	I	2X & 4X	Input from crystal oscillator circuitry.
XOUT	5	O	2X & 4X	Output from crystal oscillator circuitry.
OECTRL	6	I	2X & 4X	Output Enable input (see "OE LOGIC SELECTION TABLE").
DNC	7	I	2X	Do Not Connect.
L4X			4X	External inductor connection. The inductor is recommended to be a high Q small size 0402 or 0603 SMD component, and must be placed between L4X and adjacent VDDOSC. Place inductor as close to the IC as possible to minimize parasitic effects and to maintain inductor Q. This inductor is used with 4X AFMs.
GNDANA	8	P	2X	GND connection.
VDDOSC			4X	VDD connection for oscillator circuitry. VDDOSC should be separately decoupled from other VDDs whenever possible.
GNDBUF	9	P	2X & 4X	GND connection for output buffer circuitry.
Q	10	O	2X & 4X	PECL/LVDS or CMOS output.
QBAR	11	O	2X & 4X	Complementary PECL/LVDS output or in phase CMOS.
VDDBUF	12	P	2X & 4X	VDD connection for output buffer circuitry. VDDBUF should be separately decoupled from other VDDs whenever possible.
VDDANA	13	P	2X & 4X	VDD connection for analog circuitry. VDDANA should be separately decoupled from other VDDs whenever possible.
OESEL	14	I	2X & 4X	Selector input to choose the OE control logic (see "OE SELECTION TABLE".
VDDOSC	15	P	2X & 4X	VDD connection for oscillator circuitry. VDDOSC should be separately decoupled from other VDDs whenever possible.
L2X	16	I	2X & 4X	External inductor connection. The inductor is recommended to be a high Q small size 0402 or 0603 SMD component, and must be placed between L2X and adjacent VDDOSC. Place inductor as close to the IC as possible to minimize parasitic effects and to maintain inductor Q.

PACKAGE INFORMATION

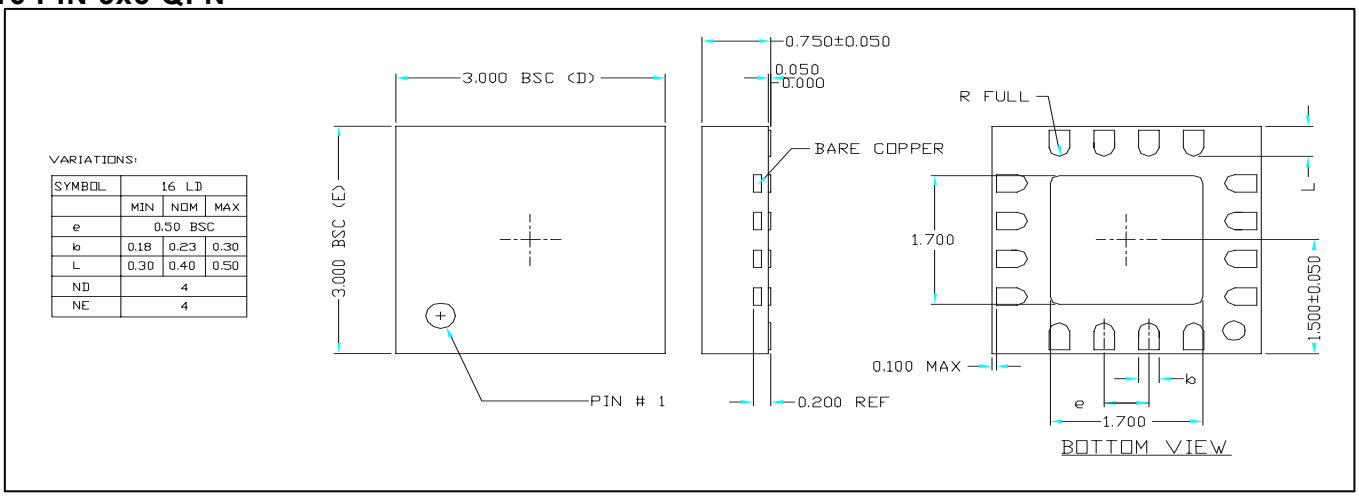
16 PIN SSOP

16 PIN SSOP (inch)

	SSOP		
Symbol	Min.	Nom.	Max.
A	.053	.064	.069
A1	.004	.006	.010
B	.008	-	.012
C	.007	-	.010
D	.189	.193	.197
E	.150	.154	.157
H	.228	.236	.244
L	.016	.025	.050
e	.025 BASIC		



16 PIN 3x3 QFN



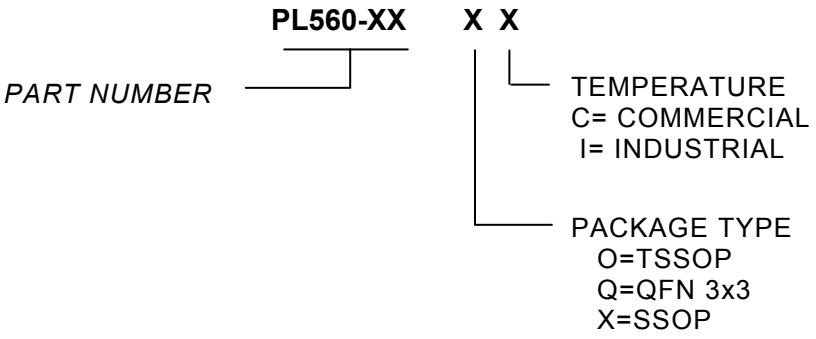
ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



Order Number	Marking	Package Option
PL560-XXOC-R	P560-XX OC	TSSOP – Tape and Reel
PL560-XXQC-R	P560-XX QC	QFN – Tape and Reel
PL560-XXXC-R	P560-XX XC	SSOP – Tape and Reel
PL560-XXOC	P560-XX OC	TSSOP – Tube
PL560-XXQC	P560-XX QC	QFN – Tube
PL560-XXXC	P560-XX XC	SSOP – Tube