Le79Q2241/2242/2243

Quad Intelligent Subscriber Line Audio-processing Circuit

VoiceChip™ Family 790 Series

APPLICATIONS

- **Voice over IP/DSL — Integrated Access Devices (IAD), Smart Residential Gateways (SRG), Home Gateway/ Router**
- **Cable Telephony — NIU, Set-Top Box, Home Side Box, Cable Modem, Cable PC**
- **Fiber — Fiber in the Loop (FITL), Fiber to the Home (FTTH)**
- **Wireless Local Loop, Intelligent PBX**
- **DLC-MUX**
- **CO**

FEATURES

- **High performance digital signal processor provides programmable control of all major line card functions**
  - A-law/µ-law and linear codec
    - Transmit and receive gain
    - Two-wire AC impedance
    - Transhybrid balance
    - Equalization
  - DC loop feeding
    - Smooth or abrupt polarity reversal
  - Loop supervision
    - Off-hook debounce circuit
    - Ground-key and ring-trip filters
  - Ringing generation and control
  - Line and circuit testing
  - Tone generation
  - Metering generation at 12 kHz and 16 kHz
    - Envelope shaping and level control
  - Modem Tone Detection
- **Selectable PCM/MPI or GCI digital interfaces**
  - Supports most available master clock frequencies from 512 kHz to 8.192 MHz
- **General purpose I/O pins**
- **+3.3 V DC operation**
- **Exceeds LSSGR and ITU requirements**
- **Supports external ringing with on-chip ring-trip circuit**
  - Automatic or manual ring-trip modes
- **Supports CallerNumber Identification (CID)**

ORDERING INFORMATION

Device	Package
Le79Q2241VC	64-pin TQFP
Le79Q2242JC	68-pin PLCC
Le79Q2243VC	80-pin TQFP

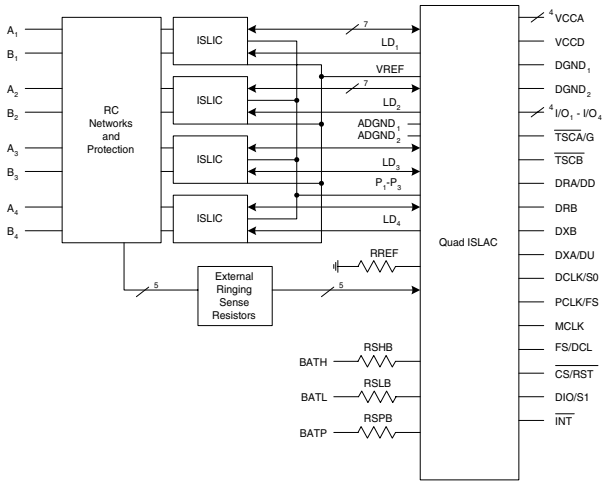
DESCRIPTION

The Le79Q2241/2242/2243 codec, in combination with a 790 series SLIC device, implements a fourchannel universal telephone line interface. This enables the design of a single, low cost, high performance, fully software programmable line interface for multiple country applications. All AC, DC, and signaling parameters are fully programmable via microprocessor or GCI interfaces. Additionally, the Le79Q2241/2242/2243codec has integrated self-test and line-test capabilities to resolve faults to the line or line circuit. The integrated test capability is crucial for remote applications where dedicated test hardware is not cost effective.

RELATED LITERATURE

- **080248 Le79231 790 Series SLIC Data Sheet**
- **080249 Le79R241 790 Series SLIC Data Sheet**
- **080253 Le79R251 790 Series SLIC Data Sheet**
- **080804 Le79R2xx/Le79Q224x Chip Set User's Guide**

BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The 790 series voice chip sets integrate all functions of the subscriber line for four subscriber lines. One or more of two chip types are used to implement the line card; a 790 series SLIC device and a Le79Q2241/2242/2243 codec. These provide the following basic functions:

1. The 790 series SLIC device: A high voltage, bipolar IC that drives the subscriber line, maintains longitudinal balance and senses line conditions.
2. The Le79Q2241/2242/2243 codec: A low voltage CMOS IC that provides conversion and DSP functions for all four channels.

Complete schematics of line cards using the Le79Q2241/2242/2243 codec for internal and external ringing are shown in *Application Circuits*, on page 30.

The 790 series SLIC device uses reliable, bipolar technology to provide the power necessary to drive a wide variety of subscriber lines. It can be programmed by the codec to operate in eight different modes that control power consumption and signaling. This enables it to have full control over the subscriber loop. The 790 series SLIC device is designed to be used exclusively with the Le79Q2241/2242/2243 codec as part of a multiple-line chip set.

The 790 series SLIC device implements a linear loop-current feeding method with the enhancement of intelligent thermal management in a controlled manner. This limits the amount of power dissipated on the 790 series SLIC chip by dissipating excess power in external resistors.

Each Le79Q2241/2242/2243 codec contains high-performance codec circuits that provide A/D and D/A conversion for voice (codec), DC-feed and supervision signals for four subscriber channels. The Le79Q2241/2242/2243 codec contains a DSP core that handles signaling, DC-feed, supervision and line diagnostics for all four channels.

The DSP core selectively interfaces with three types of backplanes:

- Standard PCM/MPI
- Standard GCI
- Modified GCI with a single analog line per GCI channel

The Le79Q2241/2242/2243 codec provides a complete software configurable solution to the BORSCHT functions as well as complete programmable control over subscriber line DC-feed characteristics, such as current limit and feed resistance. In addition, these chip sets provide system level solutions for the loop supervisory functions and metering. In total, they provide a programmable solution that can satisfy worldwide line card requirements by software configuration.

Software programmed filter coefficients, DC-feed data and supervision data are easily calculated with the WinSLAC™ software. This PC software is provided free of charge and allows the designer to enter a description of system requirements. WinSLAC then computes the necessary coefficients and plots the predicted system results.

The 790 series SLIC device interface unit inside the Le79Q2241/2242/2243 codec processes information regarding the line voltages, loop currents and battery voltage levels. These inputs allow the Le79Q2241/2242/2243 codec to place several key 790 series SLIC device performance parameters under software control.

The main functions that can be observed and/or controlled through the Le79Q2241/2242/2243 codec backplane interface are:

- DC-feed characteristics
- Ground-key detection
- Off-hook detection
- Metering signal
- Longitudinal operating point
- Subscriber line voltage and currents
- Ring-trip detection
- Abrupt and smooth reversal
- Subscriber line matching
- Ringing generation
- Sophisticated line and circuit tests

To accomplish these functions, the 790 series SLIC device collects the following information and feeds it, in analog form, to the Le79Q2241/2242/2243 codec:

- The metallic (IMT) and longitudinal (ILG) loop currents
- The AC (VTX) and DC (VSAB) loop voltages

The outputs supplied by the Le79Q2241/2242/2243 codec to the 790 series SLIC device are then:

- A voltage (VHL_i*) that provides control for the following high-level 790 series SLIC device outputs:
- DC loop current

- Internal ringing signal
- 12 or 16 kHz metering signal
- A low-level voltage proportional to the voice signal ($VOUT_i$)
- A voltage that controls longitudinal offset for test purposes (VLB_i)

The Le79Q2241/2242/2243 codec performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the two-wire termination impedance and provide frequency attenuation adjustment (equalization) of the receive and transmit paths. Transhybrid balancing is also included. All programmable digital filter coefficients can be calculated using WinSLAC™ software. The PCM codes can be either 16-bit linear two's-complement or 8-bit companded A-law or µ-law.

Besides the codec functions, the Le79Q2241/2242/2243 codec provides all the sensing, feedback, and clocking necessary to completely control 790 series SLIC device functions with programmable parameters. System-level parameters under programmable control include active loop current limits, feed resistance, and feed mode voltages.

The Le79Q2241/2242/2243 codec supplies complete mode control to the 790 series SLIC device using the control bus and (P1-P3) tri-level load signal (LD_i).

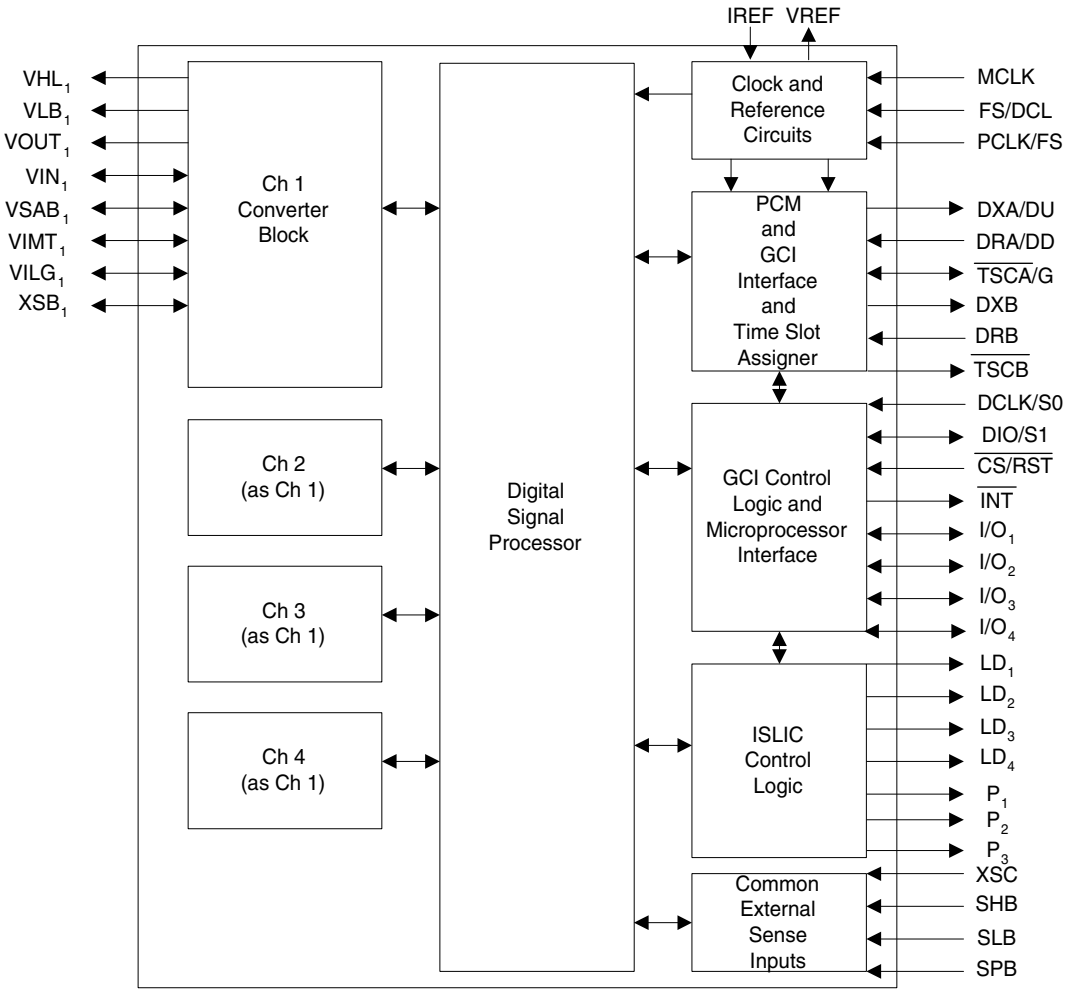
The Le79Q2241/2242/2243 codec provides extensive loop supervision capability including off-hook, ring-trip and ground-key detection. Detection thresholds for these functions are programmable. A programmable debounce timer is available that eliminates false detection due to contact bounce.

For subscriber line diagnostics, AC and DC line conditions can be monitored using built in test tools. Measured parameters can be compared to programmed threshold levels to set a pass/fail bit. The user can choose to send the actual PCM measurement data directly to a higher level processor by way of the voice channel. Both longitudinal and metallic resistance and capacitance can be measured, which allows leakage resistance, line capacitance, and telephones to be identified.

Note:

"i" denotes channel number

Le79Q2241/2242/2243 Device Internal Block Diagram



Features of the Le79Q2241/2242/2243 Chip Set

- Performs all battery feed, ringing, signaling, hybrid and test (BORSCHT) functions
- Two chip solution supports high density, multi-channel architecture
- Single hardware design meets multiple country requirements through software programming of:
  - Ringing waveform and frequency
  - DC loop-feed characteristics and current-limit
  - Loop-supervision detection thresholds
  - Off-hook debounce circuit
  - Ground-key and ring-trip filters
  - Off-hook detect de-bounce interval
  - Two-wire AC impedance
  - Transhybrid balance
  - Transmit and receive gains
  - Equalization
  - Digital I/O pins
  - A-law/µ-law and linear selection
- Supports internal and external battery-backed ringing
  - Self-contained ringing generation and control
  - Supports external ringing generator and ring relay
  - Ring relay operation synchronized to zero crossings of ringing voltage and current
  - Integrated ring-trip filter and software enabled manual or automatic ring-trip mode
- Supports metering generation with envelope shaping
- Smooth or abrupt polarity reversal
- Adaptive transhybrid balance
  - Continuous or adapt and freeze
- Supports both loop-start and ground-start signaling
- Exceeds LSSGR and CCITT central office requirements
- Selectable PCM or GCI interface
  - Supports most available master clock frequencies from 512 kHz to 8.192 MHz
- On-hook transmission
- Power/service denial mode
- Line-feed characteristics independent of battery voltage
- Only 5 V, 3.3 V and battery supplies needed
- Low idle-power per line
- Linear power-feed with intelligent power-management feature
- Compatible with inexpensive protection networks; Accommodates low-tolerance fuse resistors while maintaining longitudinal balance
- Monitors two-wire interface voltages and currents for subscriber line diagnostics
- Built-in voice-path test modes
- Power-cross, fault, and foreign voltage detection
- Integrated line-test features
  - Leakage
  - Line and ringer capacitance
  - Loop resistance
- Integrated self-test features
  - Echo gain, distortion, and noise
- Small physical size
- Up to three relay drivers per 790 series SLIC device
  - Configurable as test load switches

CONNECTION DIAGRAMS

Figure 1. 68-Pin PLCC Connection Diagram

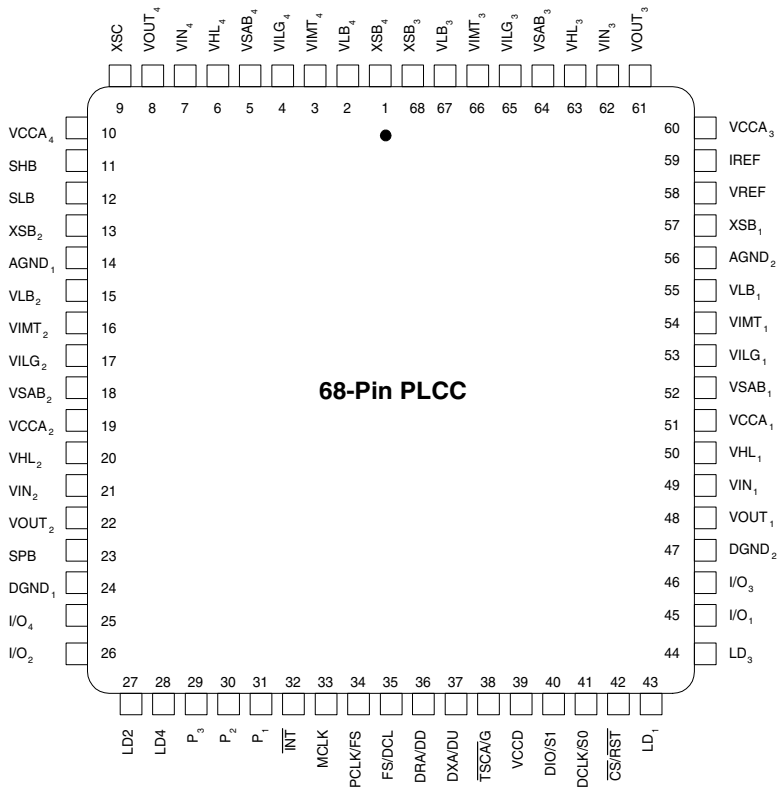


Figure 2. 64-Pin TQFP Connection Diagram

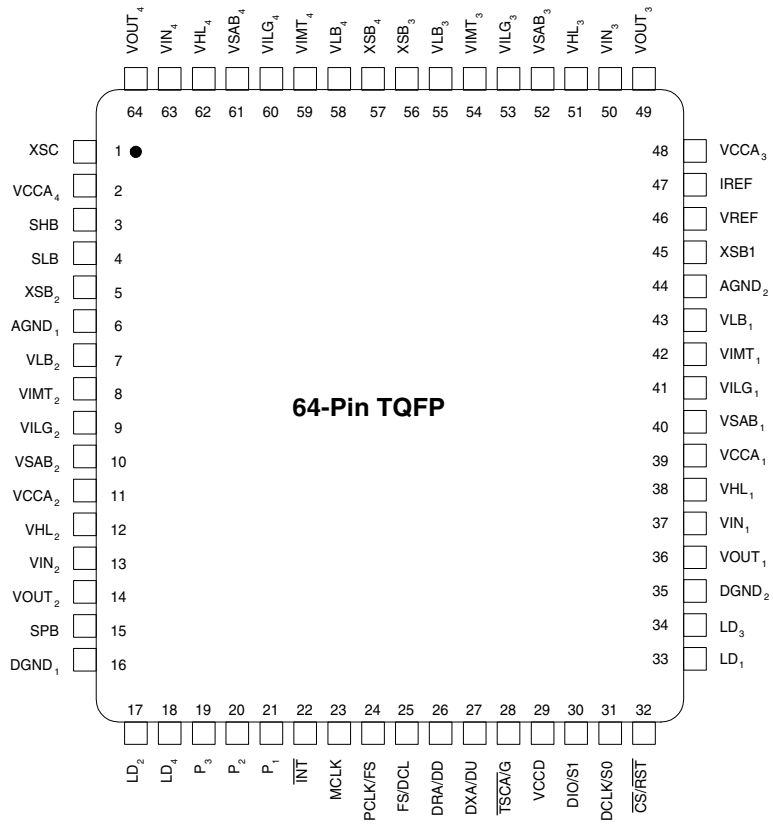
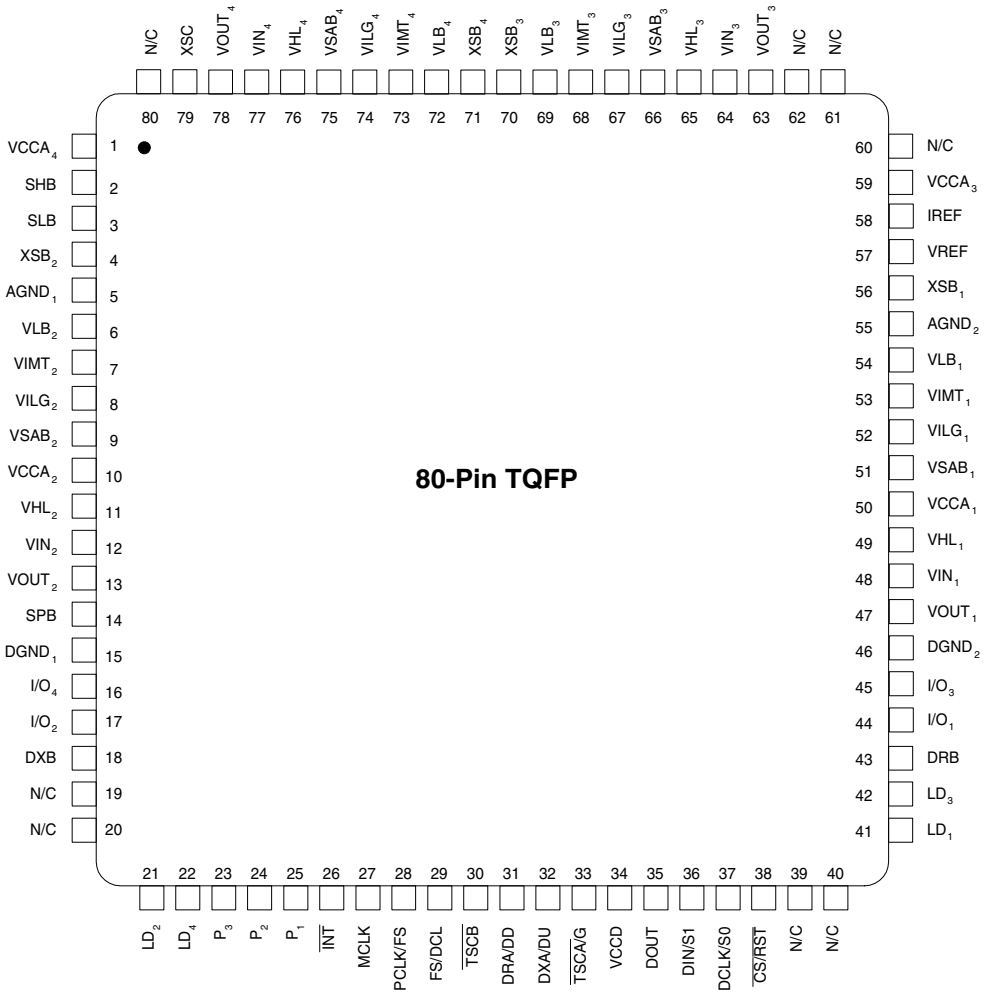


Figure 3. 80-Pin TQFP Connection Diagram



PIN DESCRIPTIONS

Pin Name	Type	Description
$AGND_1$, $AGND_2$	Ground	Analog circuitry ground returns
$\overline{CS}/\overline{RST}$	Input	For PCM backplane operation, a logic low on this pin for 16 or more DCLK cycles resets the sequential logic in the Le79Q2242241/2242/2243 codec into a known mode. A logic low placed on this pin for less than 15 DCLK cycles is a chip select and enables serial data transmission into or out of the DIO port. For GCI operation, a logic low on this pin for 1 µs or longer resets the sequential logic into a known mode. This pin is 5-V tolerant.
DCLK/S0	Input	Provides data control for MPI interface control. For GCI operation, this pin is device address bit 0. This pin is 5-V tolerant.
$DGND_1$, $DGND_2$	Ground	Digital ground returns
DIN/S1	Input	For PCM backplane operation, control data is serially written into the Le79Q2242241/2242/2243 codec codec via the DIN pin with the MSB first. The data clock (DCLK) determines the data rate. For GCI operation, this pin is device address bit 1. This pin is 5 V tolerant.
DIO/S1	Input/ Output	For PCM backplane operation, control data is serially written into and read out of the Le79Q2242241/2242/2243 codec via the DIO pin with the MSB first. The data clock (DCLK) determines the data rate. DIO is high impedance except when data is being transmitted from the Le79Q2242241/2242/2243 codec under control of $\overline{CS}/\overline{RST}$. For GCI operation, this pin is device address bit 1. This pin is 5 V tolerant.
DOUT	Output	For PCM backplane operation, control data is serially read out of the Le79Q2242241/2242/2243 codec via the DOUT pin with the MSB first. The data clock (DCLK) determines the data rate. DOUT is high impedance except when data is being transmitted from the Le79Q2242241/2242/2243 codec under control of $\overline{CS}/\overline{RST}$. This pin is 5-V tolerant.
DRA/DD, DRB	Input	For the PCM highway, the receive PCM data is input serially through the DRA or DRB pins. The data input is received every 125 µs and is shifted in, MSB first, in 8-bit PCM or 16-bit linear bursts at the PCLK rate. The receive port can receive information for direct control of the 790 series SLIC device. This mode is selected in Device Configuration Register 2 (RTSEN=1, RTSMD=1). When selected, this data is received in an independently programmable timeslot from the PCM data. For the GCI mode, downstream receive and control data is accepted on this pin. The DRB pin is available only on the 80-pin TQFP package. This pin is 5 V tolerant.
DXA/DU, DXB	Output	For the PCM highway, the transmit PCM data is transmitted serially through the DXA or DXB pins. The transmission data output is available every 125 µs and is shifted out, MSB first, in 8-bit PCM or 16-bit linear bursts at the PCLK rate. DXA and DXB are high impedance between bursts and while the device is in the inactive mode. Can also select a mode (RTSEN= 1, RTSMD=1 or 0 in Device Configuration Register 2) that transmits the Signaling Register MSB contents first, in an independently programmable timeslot from the PCM data. This data is transmitted in all modes except disconnect. For the GCI mode, upstream transmit and signaling data is transferred on this pin. The DXB pin is available only on the 80-pin TQFP package. This pin is 5 V tolerant.
FS/DCL	Input	For PCM operation, pin is Frame Sync. PCM operation is selected by the presence of an 8 kHz Frame Sync signal on this pin in conjunction with the PCLK on the PCLK/FS pin (see below). This 8 kHz pulse identifies the beginning of a frame. The Le79Q2242241/2242/2243 codec references individual timeslots with respect to this input, which must be synchronized to PCLK. GCI operation is selected by the presence of the downstream clock DCL, on this pin in conjunction with the presence of a FS on the PCLK/FS pin. In GCI mode, the data rate is 2 MHz and DCL must be either 2 or 4 MHz. This pin is 5 V tolerant.
$VILG_1$– $VILG_4$	Input	Longitudinal current input from SLIC. Voltage generated by RLG is sensed by this pin.
$VIMT_1$– $VIMT_4$	Input	Metallic current input from SLIC. Voltage generated by RMT is sensed by this pin.
$\overline{INT}$	Output	For PCM operation, when a subscriber line requires service, this pin goes to a logic 0 to interrupt a higher level processor. Several registers work together to control operation of the interrupt: Signaling and Global Interrupt Registers with their associated Mask Registers, and the Interrupt Register. See the description at channel configuration register 6 (Mask) for operation. Logic drive is selectable between open drain and TTL-compatible outputs.
I/O_1–I/O_4	Input/ Output	General purpose logic input/output connections for each of four channels. These control lines each can be programmed as an input or output in the Global I/O Direction Register. When programmed as outputs, they can control an external logic device. When programmed as inputs, they can monitor external logic circuits. Data for these pins can be written or read individually (from the channel specific I/O Register) or as a group (from the Global I/O Data Register). Not available on the 64-pin package.
IREF	Input	External resistor (R_{REF}) connected between this pin and analog ground generates an accurate, on-chip reference current for the A/D's and D/A's on the Le79Q2242241/2242/2243 codec.

Pin Name	Type	Description
LD_1–LD_4	Output	The LD pins output 3-level voltages. When LD_i is a logic 0 (< 0.4 V), the destination of the code on P_1–P_3 is the relay control latches in the 790 series SLIC device control register. When LD_i is a logic 1 (>V_{CC}–0.4 V), the destination of P_1–P_3 is the mode control latches. LD_i is driven to VREF when the contents of the ISLIC control register must not change.
MCLK	Input	For PCM backplane operation, the DSP master clock may connect here. A signal is required only for PCM backplane operation when PCLK is not used as the master clock. MCLK can be a wide variety of frequencies, but must be synchronous to FS. Upon initialization, the MCLK input is disabled, and relevant circuitry is driven by a connection to PCLK. 5 V tolerant.
PCLK/FS	Input	For PCM operation, this is PCM Clock. PCM operation is selected by the presence of a PCLK signal on this pin in conjunction with the FS on the FS/DCL pin (see below). For PCM backplane operation, connect a data clock, which determines the rate at which PCM data is serially shifted into or out of the PCM ports. PCLK can be any integer multiple of the FS frequency. The minimum clock frequency for linear/ companded data plus signaling data is 256 kHz. For GCI operation, this pin is Frame Sync. The FS signal is an 8 kHz pulse that identifies the beginning of a frame. The Le79Q2242241/2242/2243 codec references individual timeslots with respect to this input, which must be synchronized to DCL. This pin is 5-V tolerant.
P_1–P_3	Output	Control the operating modes of the four 790 series SLIC devices connected to the Le79Q2242241/2242/2243 codec.
SHB, SLB, SPB	Input	Resistors that sense the high, low and positive battery voltages connect here. If only one negative battery is used, connect both resistors at the supply. If the positive battery is not used, leave the pin unconnected. These pins are current inputs whose voltage is held at VREF.
$\overline{TSCA}$/G	Output (PCM) Input (GCI)	For PCM backplane operation, $\overline{TSCA}$ or $\overline{TSCB}$ is active low when PCM data is output on the DXA or DXB pins, respectively. The outputs are open-drain and are normally inactive (high impedance). Pull-up loads should be connected to VCCD. $\overline{TSCB}$ is only available on the 80-pin TQFP package. When GCI mode is selected, one of two GCI modes may be selected by connecting $\overline{TSCA}$/G to DGND or VCCD.
$\overline{TSCB}$	Output	
$VCCA_1$–$VCCA_4$	Supply	+3.3 VDC supplies to the analog sections in each of the four channels.
VCCD	Supply	+3.3 VDC supply to all digital sections.
VHL_1–VHL_4	Output	High-level loop control voltages on these pins are used to control DC-feed, internal ringing, metering and polarity reversal for each 790 series SLIC device.
VIN_1–VIN_4	Input	Analog transmit signals (VTX) from each 790 series SLIC device connect to these pins. The Le79Q2242241/2242/2243 codec converts these signals to digital words and processes them. After processing, they are multiplexed into serial time slots and sent out of the DXA/DU pin.
$VOUT_1$–$VOUT_4$	Output	Analog receive voltage signals are sent out of the Le79Q2242241/2242/2243 codec from these pins. A resistor converts these signals to currents which drive the 790 series SLIC device.
VLB_1–VLB_4	Output	Normally connected to VCCA internally. They supply longitudinal reference voltages to the 790 series SLIC devices during certain test procedures. These outputs are connected internally to VCCA during 790 series SLIC Active, Standby, Ringing, and Disconnect modes. During test modes, it can be connected to the receive D/A.
VREF	Output	This pin provides a 1.4 V, single-ended reference to the four 790 series SLIC devices to which the Le79Q2242241/2242/2243 codec is connected.
$VSAB_1$–$VSAB_4$	Input	Connect to the VSAB pins of four 790 series SLIC devices.
XSB_1–XSB_4	Input	External ringing sense pin. This pin senses the current through RSRB to measure the ringing voltage on the line.
XSC	Input	External ring generator sense. This pin senses the current RSRC to measure the ringing bus voltage.

Pin Options	Package Type		
	80 pin	68 pin	64 pin
DRB	÷	x	x
DXB	÷	x	x
TSCB	÷	x	x
I/O_1–I/O_4	÷	÷	x
DIN	÷	x	x
DOUT	÷	x	x
DI/O	x	÷	÷

Note:
For the 80-pin TQFP package, DOUT and DIN/S1 can be connected together. The combined functionality is then equivalent to the DIO/S1 pin of the 68-pin package.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage Temperature	–60ºC ≤ T_A ≤ +125ºC
Ambient Temperature, under Bias	–40ºC ≤ T_A ≤ +85ºC
Ambient relative humidity (non condensing)	5 to 95%
V_{CCA} with respect to (AGND or DGND)	–0.4 to + 4.0 V
V_{CCD} with respect to (AGND or DGND)	–0.4 to + 4.0 V
V_{CCA} with respect to V_{CCD}	±0.4V
V_{IN} with respect to (AGND or DGND)	–0.4 to (V_{CCA} + 0.4 V)
5 V tolerant pins	–0.4 to (V_{CCD} + 2.37) or 5.5 V, whichever is less
AGND	DGND ± 0.4 V
Latch up immunity (any pin)	±100 mA
Any other pin with respect to DGND	–0.4 V to V_{CC}

Operating Ranges

Legerity guarantees the performance of this device over commercial (0º to 70ºC) and industrial (–40º to 85ºC) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore TR-TSY-000357 Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	–40 to +85ºC
Ambient Relative Humidity	15 to 85%

Electrical Ranges

Analog Supply V_{CCA}	+3.3 V ± 5%, V_{CCD} ± 50 mV
Digital Supply V_{CCD}	+3.3 V ± 5%
DGND	0 V
AGND	DGND ±10 mV
5V tolerant pins with respect to DGND	DGND to 5.25V

SPECIFICATIONS

DC Specifications

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	Input Low Voltage, I/O_1–I/O_4		–0.05	—	1.36 V	V	
	All other digital inputs		–0.50	—-	0.80 V		
2	Input High Voltage, I/O_1–I/O_4		2.46	—-	V_{CC}+0.4		
	All other digital inputs		2.0	—	5.25		
3	Input Leakage Current, I/O_1–I/O_4	0 to V_{CC}	–10	—-	+10	µA	
	All other digital inputs	0 to 5.25 V	–120	—-	+180		
4	Input hysteresis (PCLK/FS, FS/DCL, MCLK, DIO, DRA, DRB)		.15	.225	.3	V	2
	I/O1–I/O4		.16	.25	.34		
5	Ternary output voltages, LD_1–LD_4						
	High voltage	Iout = 1 mA	V_{CC}–.4	—	—		
	Low voltage	Iout = 2 mA	—	—	0.4		
	Medium voltage	±10 µA	—	VREF	—		
6	Output Low Voltage (DXA/DU, DIO, I/O_1–I/O_4, $\overline{INT}$, $\overline{TSCA}$, $\overline{TSCB}$, DXB)	Iol = 10mA	—	—-	0.4	V	
7	Output Low Voltage (P_1-P_3)	Iol = 5 mA	—	—	0.4		
8	Output High Voltage (All digital outputs except $\overline{INT}$ in open drain mode and $\overline{TSCA}$, $\overline{TSCB}$)	Ioh = 400 µA	V_{CC}–0.4	—	—		
9	Input Leakage Current (VIN_1–VIN_4, $VSAB_1$–$VSAB_4$, $VILG_1$_$VILG_4$, $VIMT_1$_$VIMT_4$)		–1	±0.2	1	µA	
10	Input Voltage ($VSAB_1$–$VSAB_4$ or $VIMT_1$–$VIMT_4$ or $VILG_1$–$VILG_4$)	|Vov–VREF| where Vov is input overload voltage		1.02		V	
11	Full scale input voltage (VIN_1–VIN_4)					V	
	µ-law	3.205 dBm0	—	VREF ±1.02	—		
	A-law	3.14 dBm0					
12	Offset voltage allowed on VIN_1–VIN_4		–50	—	+50	mV	4
13	$VOUT_1$–$VOUT_4$ offset Voltage	DISN off	–40	—	+40		
		DISN on	–80	—	+80		
14	Output voltage, VREF	Load current = 0 to 10 mA, Source or Sink	1.32	1.4	1.48	V	
15	Output drive current, $VOUT_1$–$VOUT_4$ or VLB_1–VLB_4	Source or Sink	–1	—	+1	mA	2
16	Maximum output voltage on $VOUT_1$–$VOUT_4$	|VOUT – VREF| with peak digital input		1.02		V	
17	Maximum output voltage on VLB_1–VLB_4	|VLB – VREF| with peak digital input		1.02			
18	Maximum output voltage on VHL_1–VHL_4, VFD = 0, Hook Bit = OFF	|VHL–VREF| with peak digital input		1.02			
19	VHL_1–VHL_4 D/A absolute error	% of D/A code	(–15) – 4%		(+15) + 4%	mV	
20	$VSAB_i$ A/D absolute error	% of input voltage	(–40) – 5%		(+40) + 5%		
21	$VIMT_i$ A/D absolute error	% of input voltage	(–20) – 2.5%		20 + 2.5%		
22	$VILG_i$ A/D absolute error	% of input voltage	(–20) –2.5%		20 + 2.5%		
23	Battery read A/D absolute error	% of input voltage	(–10) – 6%		10 + 6%		
24	VLB_1–VLB_4 D/A absolute error	% of D/A code	(–40) – 5%		(+40) + 5%	V	
25	$VSAB_i$ to VHL_i output offset (KRFB)	VFD = 1	–50	0	50	mV	

No.	Item	Condition	Min	Typ	Max	Unit	Note
26	Gain from $VSAB_i$ to VHL_i (KRFB)	VFD = 1	–4.8	–5	–5.2	V/V	
27	Gain from $VSAB_i$ to VHL_i	VFD = 0, On hook	–	–0.128	–	V/V	
29	Capacitance load on VLB_1–VLB_4		0	—	120	pF	2
30	Capacitance load on XSB_1–XSB_4, XSC		0	—	400		
31	Capacitance load on VREF or $VOUT_1$–$VOUT_4$		0	—	200	pF	
32	Power Dissipation	One channel active (790 series SLIC state register set to active); three channels inactive (790 series SLIC state register set to Standby)	—	162	185	mW	9
		All channels active (790 series SLIC state register set to Active)	—	204	235		
		All channels inactive (790 series SLIC state register set to Standby)	—	120	140		

Transmission and Signaling Specifications

Table 1. 0 dBm0 Voltage Definitions with Unity Gain in X, R, GX, GR, AX, and AR

Signal at Digital Interface	Transmit	Receive	Unit
A-law digital mW or equivalent (0 dBm0)	0.5026	0.5026	Vrms
µ-law digital mW or equivalent (0 dBm0)	0.4987	0.4987	
±5,800 peak linear coded sine wave	0.5026	0.5025	

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	Insertion Loss A-D D-A A-D + D-A	Input: 1014Hz, –10dBm0 AR = AX = GR = GX = 0 dB, DISN, R, X, B and Z disabled	–0.25	0	+0.25	dB	3, 7
		Temperature = 25°C	–0.15	0	+0.15		
		Variation over temperature	–0.1	0	+0.1		
2	Level set error (Error between setting and actual value)	A-D AX + GX D-A AR + GR	–0.1	0	0.1		
3	DR to DX gain in full digital loopback mode	DR Input: 1014 Hz, –10 dBm0 AR=AX=GR=GX=0 dB, DISN, R, X, B and Z filters default	–0.3	0	+0.3		
4	Idle Channel Noise, Psophometric Weighted (A-law)	A-D (PCM output)	—	—	–69	dBm0p	5
		D-A (V_{OUT})	—	—	–78		
5	Idle Channel Noise, C Message weighted (µ-law)	A-D (PCM output)	—	—	+19	dBrnC0	
		D-A (V_{OUT}	—	—	+12		
6	Coder Offset decision value, Xn	A-D, Input signal = 0 V	–7	0	+7	Bits	2
7	PSRR Image frequency (VCC) A-D	Input: 4.8 to 7.8 kHz, 200 mVp-p	37	—	—	dB	1
8	PSRR Image frequency (VCC) D-A	Measure at: 8000 Hz – Input frequency	37	—	—		
9	DISN gain accuracy	Gdisn = –0.9375 to 0.9375 Vin = 0 dBm0		+0.2		dB	
10	End-to-end group delay	1014Hz; –10dBm0 B = Z = 0; X = R = 1	—	—	525	µS	2, 6, 8
11	Crosstalk TX to RX same channel RX to TX	0 dBm0 300 Hz to 3400 Hz	—	—	–75	dBm0	2
		0 dBm0 300 Hz to 3400 Hz	—	—			
12	Crosstalk TX or RX to TX other channel TX or RX to RX	0 dBm0 1014 Hz	—	—	–76	dBm0	
		0 dBm0 1014 Hz	—	—	–78		

Note:

1. *Not tested or partially tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
2. *Guaranteed by design.*
3. *Overall 1.014 kHz insertion loss error of the 790 series chip set is guaranteed to be 0.34 dB*
4. *These voltages are referred to VREF.*
5. *When relative levels (dBm0) are used, the specification holds for any setting of (AX + GX) gain from 0 to 12 dB or (AR + GR) from 0 to –12 dB.*
6. *Group delay spec valid only when channels 11–4 occupy consecutive time slots in the frame. Programming channels in non-consecutive timeslots can add up to 1 frame delay in the Group delay measurements. The Group delay specification is defined as the sum of the minimum values of the group delays for transmit and the receive paths when the B, X, R, and Z filters are disabled with null coefficients. See Figure 6 for Group Delay Distortion.*
7. *Requires that the calibration command (7Ch) must be performed to achieve this performance.*
8. *An additional frame delay can be added if PCLK frequency is less than 1.536 MHz.*
9. *SLIC device channels 1 and 2 SLIC states are Disconnect. Codec channels 1 and 2 are inactive.*

TRANSMIT AND RECEIVE PATHS

In this section, the transmit path is defined as the analog input to the Le79Q2241/2242/2243 codec (VIN_n) to the PCM voice output of the Le79Q2241/2242/2243 codec A-law/µ-law speech compressor. The receive path is defined as the PCM voice input to the Le79Q2241/2242/2243 codec speech expander to the analog output of the Le79Q2241/2242/2243 codec ($VOUT_n$). All limits defined in this section are tested with B = 0, Z = 0 and X = R = GR = 1.

When AR is enabled, a nominal gain of –6.02 dB is added to the analog section of the receive path.

When AX is enabled, a nominal gain of +6.02 dB is added to the analog section of the transmit path.

When relative levels (dBm0) are used in any of the following transmission characteristics, the specification holds for any setting of (AX + GX) gain from 0 to 12 dB or (AR + GR) from 0 to –12 dB.

These transmission characteristics are valid for 0 to 70° C.

Attenuation Distortion

The attenuation of the signal in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in Figure 4 and Figure 5. The reference signal level is –10 dBm0. The minimum transmit attenuation at 60 Hz is 24 dB.

Figure 4. Transmit Path Attenuation vs. Frequency

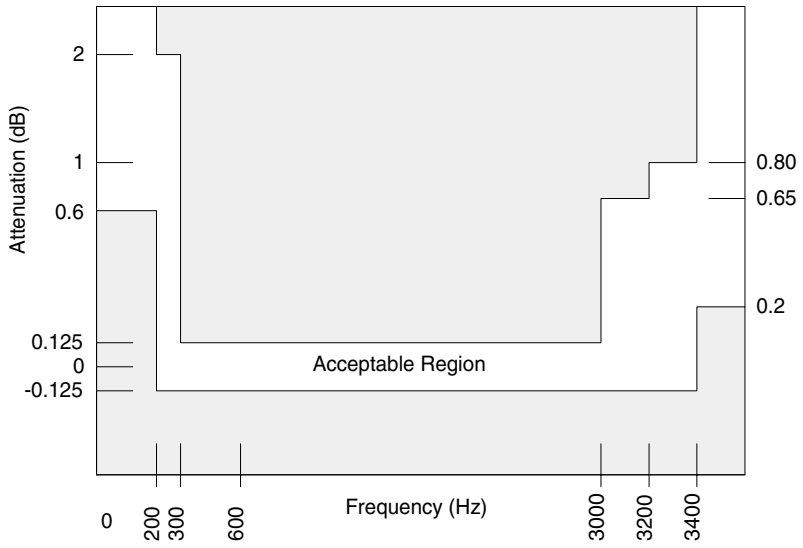
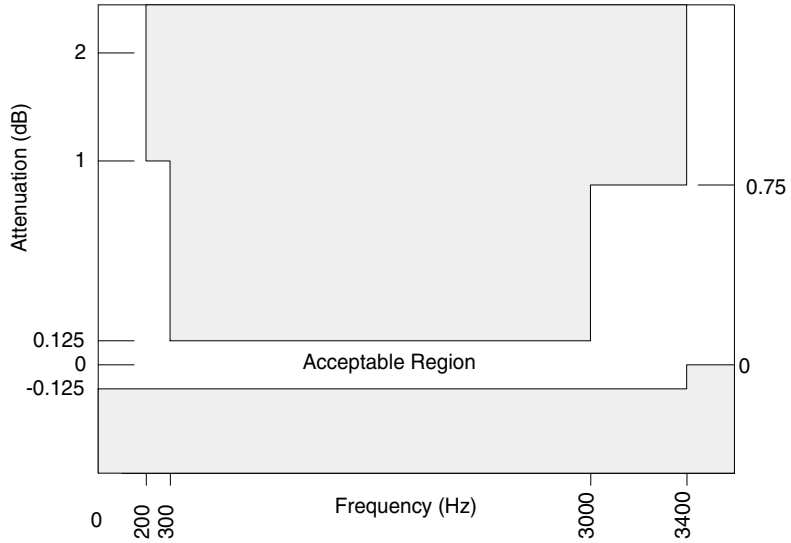


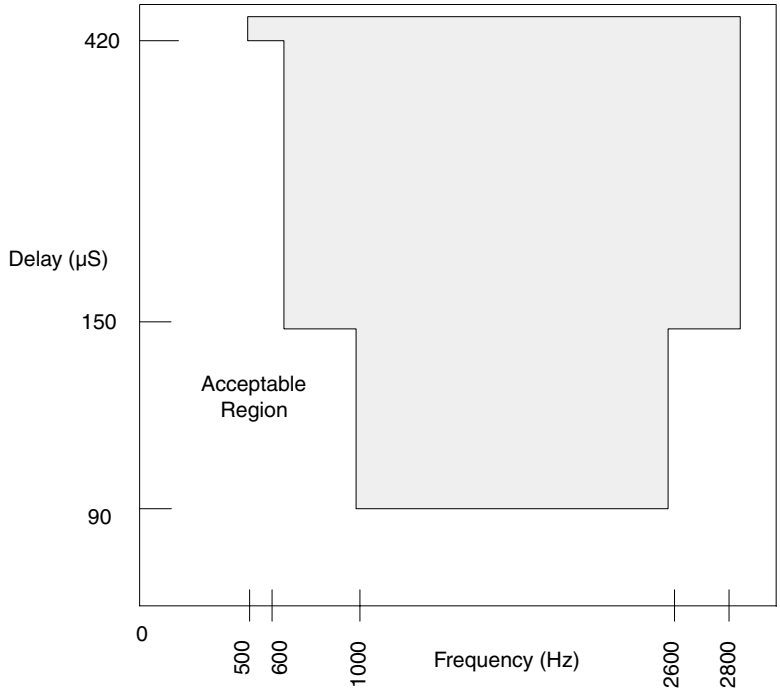
Figure 5. Receive Path Attenuation vs. Frequency



Group Delay Distortion

For either transmission path, the group delay distortion is within the limits shown in Figure 6. The minimum value of the group delay is taken as the reference. The signal level is –10 dBm0.

Figure 6. Group Delay Distortion



Single Frequency Distortion

The output signal level, at any single frequency in the range of 300 to 3400 Hz, other than that due to an applied 0 dBm0 sine wave signal with frequency f in the same frequency range, is less than –46 dBm0. With f swept between 0 to 300 Hz and 3.4 to 12 kHz, any generated output signals other than f are less than –28 dBm0. This specification is valid for either transmission path.

Gain Linearity

The gain deviation relative to the gain at –10 dBm0 is within the limits shown in Figure 7 (A-law) and Figure 8 (μ-law) for either transmission path when the input is a sine wave signal of 1014 Hz.

Figure 7. A-law Gain Linearity with Tone Input (Both Paths)

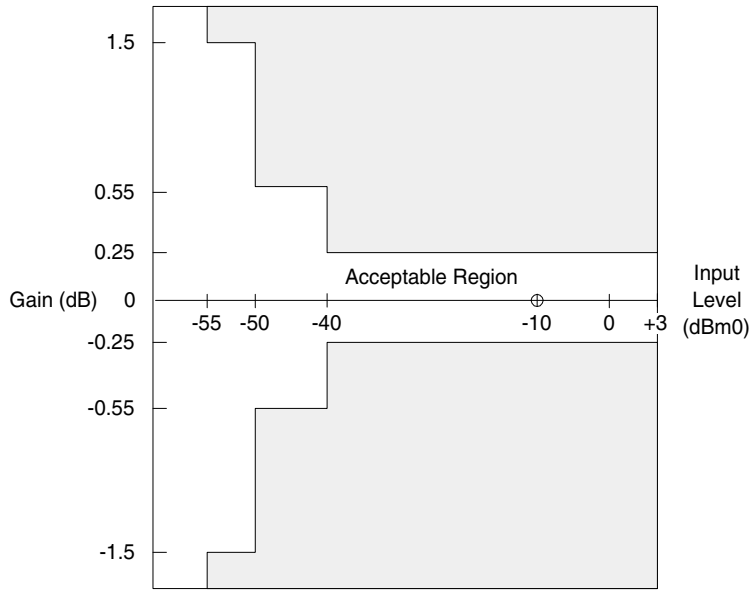
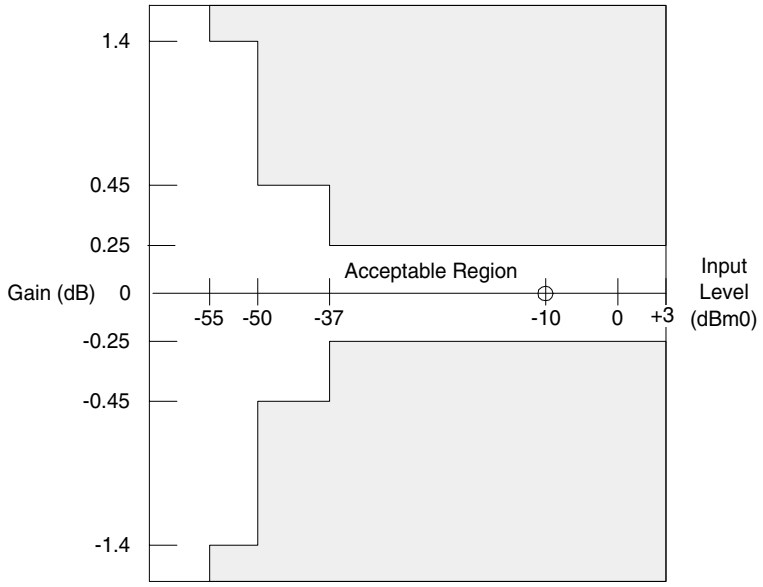


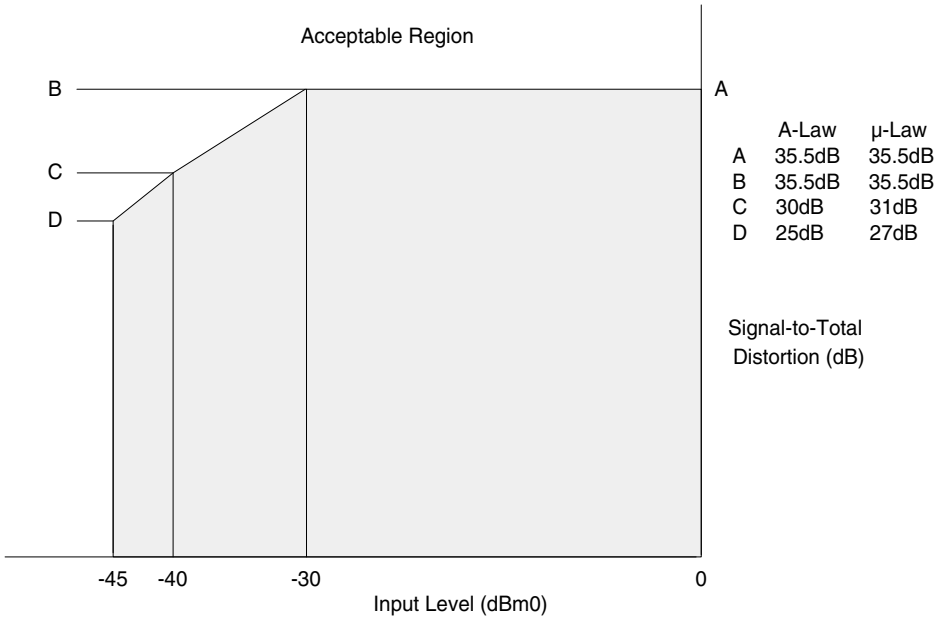
Figure 8. μ-law Gain Linearity with Tone Input (Both Paths)



Total Distortion Including Quantizing Distortion

The signal to total distortion ratio will exceed the limits shown in Figure 9 for either path when the input signal is a sine wave signal of frequency 1014 Hz.

Figure 9. Total Distortion with Tone Input, Both Paths

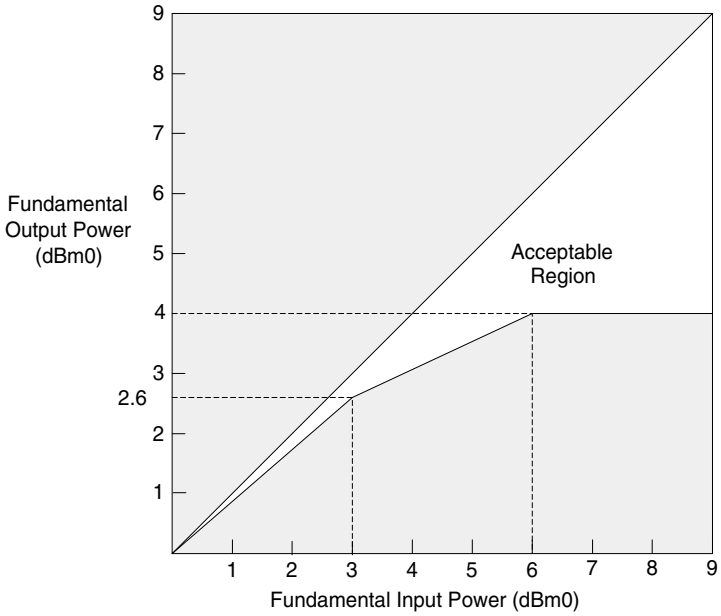


Overload Compression

Figure 10 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are:

(1) 1 dB < GX ≤ +12 dB; (2) –12 dB ≤ GR < –1 dB; (3) Digital voice output connected to digital voice input; and (4) measurement analog to analog.

Figure 10. A/A Overload Compression



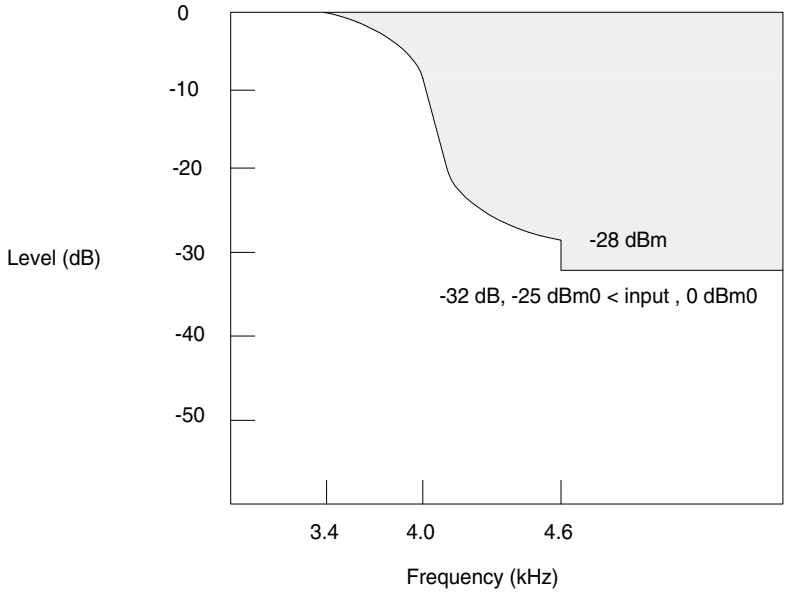
Discrimination Against Out-of-Band Input Signals

When an out-of-band sine wave signal with frequency and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output which are caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014 Hz sine wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are shown in the following table

Table 2. Minimum Specifications for Out-of-Band Input Signals

Frequency of Out-of-Band Signal	Amplitude of Out-of-Band Signal	Level below A
16.6 Hz < f < 45 Hz	–25 dBm0 < A ≤ 0 dBm0	18 dB
45 Hz < f < 65 Hz	–25 dBm0 < A ≤ 0 dBm0	25 dB
65 Hz < f < 100 Hz	–25 dBm0 < A ≤ 0 dBm0	10 dB
3400 Hz < f < 4600 Hz	–25 dBm0 < A ≤ 0 dBm0	see Figure 11
4600 Hz < f < 100 kHz	–25 dBm0 < A ≤ 0 dBm0	32 dB

Figure 11. Discrimination Against Out-of-Band Signals



Note:

The attenuation of the waveform below amplitude A between 3400 Hz and 4600 Hz is given by the formula:

$$\text{Attenuation (db)} = 14 - 14\sin\left(\frac{\pi(4000 - f)}{1200}\right)$$

Spurious Out-of-Band Signals at the Analog Output

With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious out-of-band signals at the analog output is less than the limits shown below.

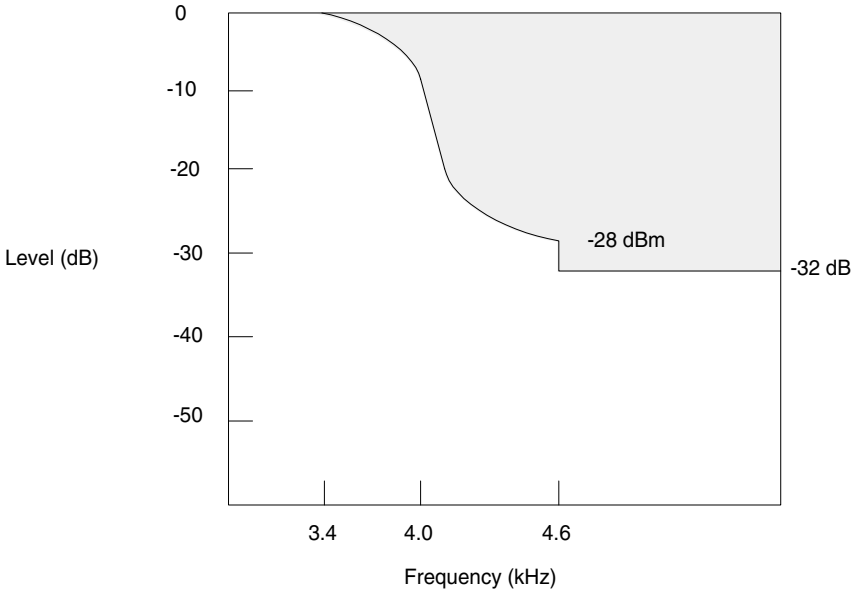
Table 3. Limits for Spurious Out-of-Band Signals

Frequency	Level
4.6 kHz to 40 kHz	–32 dBm0
40 kHz to 240 kHz	–46 dBm0
240 kHz to 1 MHz	–36 dBm0

With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 12. The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:

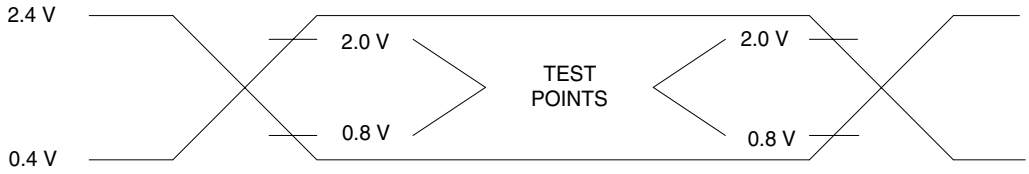
$$A = \left[-14 - 14\sin\left(\frac{\pi(f - 4000)}{1200}\right)\right] \text{ dBm0}$$

Figure 12. Spurious Out-of-Band Signals



SWITCHING CHARACTERISTICS

Figure 13. Switching Characteristics



VCC = 3.3 V ±5%, AGND = DGND = 0 V.

TIMING SPECIFICATIONS

Microprocessor Interface Timing

Min and max values are valid for all digital outputs with a 100 pF load, except DIO,DXA, $\overline{INT}$, $\overline{TSCA}$, $\overline{TSCB}$ and DXB which are valid with 150 pF loads. Pictorial definitions for these parameters can be found on page 26–page 25..

No.	Symbol	Parameter	Min	Typ	Max	Unit	Note
1	t_{DCY}	Data clock period	122	—	—	ns	
2	t_{DCH}	Data clock HIGH pulse width	48	—	—		1
3	t_{DCL}	Data clock LOW pulse width	48	—	—		1
4	t_{DCR}	Rise time of clock	—	—	15		
5	t_{DCF}	Fall time of clock	—	—	15		
6	t_{ICSS}	Chip select setup time, Input mode	30	—	t_{DCY}–10		
7	t_{ICSH}	Chip select hold time, Input mode	0	—	t_{DCY}–20		
8	t_{ICSL}	Chip select pulse width, Input mode	—	$8t_{DCY}$	—		7
9	t_{ICSO}	Chip select off time, Input mode	2000	—	—		1,6
10	t_{IDS}	Input data setup time	25	—	t_{DCY}–10		
11	t_{IDH}	Input data hold time	30	—	t_{DCY}–10		
13	t_{OCSS}	Chip select setup time, Output mode	30	—	t_{DCY}–10		
14	t_{OCSH}	Chip select hold time, Output mode	0	—	t_{DCH}–20		
15	t_{OCSL}	Chip select pulse width, Output mode	—	$8t_{DCY}$	—		
16	t_{OCSO}	Chip select off time, output Mode	2000	—	—		1,6
17	t_{ODD}	Output data turn on delay	—	—	50		5
18	t_{ODH}	Output data hold time	3	—	—		
19	t_{ODOF}	Output data turn off delay	3	—	50		
20	t_{ODC}	Output data valid	3	—	50		

MPI Waveforms

Figure 14. Microprocessor Interface (Input Mode)

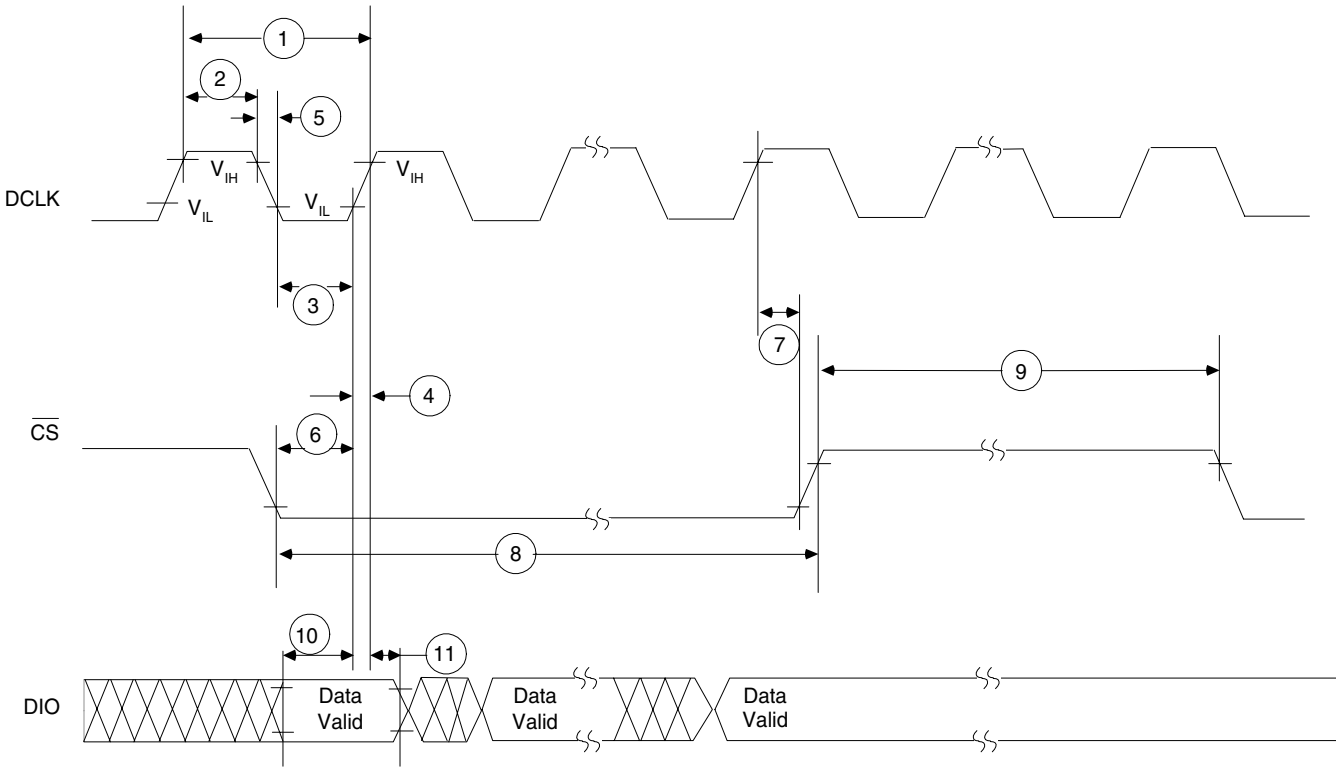
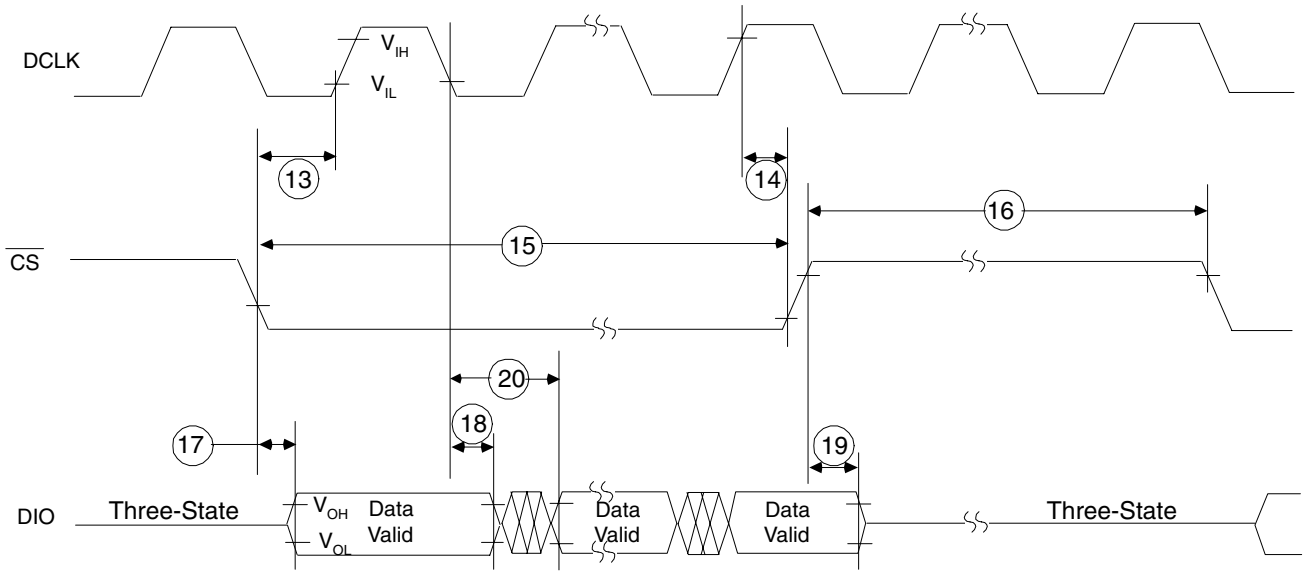


Figure 15. Microprocessor Interface (Output Mode)



PCM Interface Timing

No.	Symbol	Parameter	Min.	Typ	Max	Unit	Note
22	t_{PCY}	PCM clock period	122	—	7812.5	ns	2,9
23	t_{PCH}	PCM clock HIGH pulse width	48	—	—		
24	t_{PCL}	PCM clock LOW pulse width	48	—	—		
25	t_{PCF}	Fall time of clock	—	—	15		
26	t_{PCR}	Rise time of clock	—	—	15		
27	t_{FSS}	FS setup time	30	—	t_{PCY}–30		
28	t_{FSH}	FS hold time	50	—	125000-3t_{PCY}-30		
29	t_{TSD}	Delay to $\overline{TSC}$ valid	5	—	40		3
30	t_{TSO}	Delay to $\overline{TSC}$ off	5	—	40		4
31	t_{DXD}	PCM data output delay	5	—	40		
32	t_{DXH}	PCM data output hold time	5	—	40		
33	t_{DXZ}	PCM data output delay to high-Z	10	—	40		4
34	t_{DRS}	PCM data input setup time	25	—	t_{PCY}–10		
35	t_{DRH}	PCM data input hold time	5	—	t_{PCY}–20		
36	t_{FST}	PCM or frame sync jitter time	–97	—	97		

PCM Waveforms

Figure 16. PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)

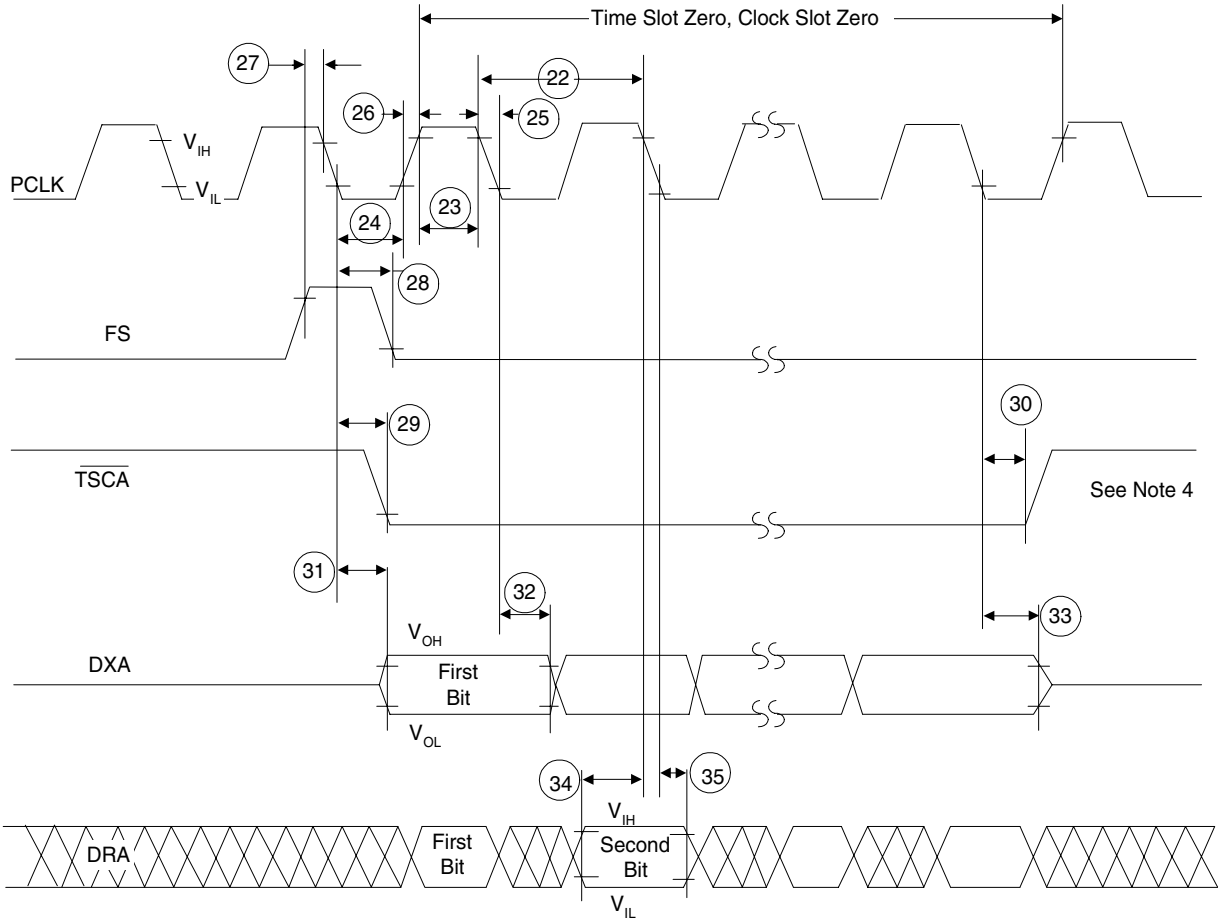
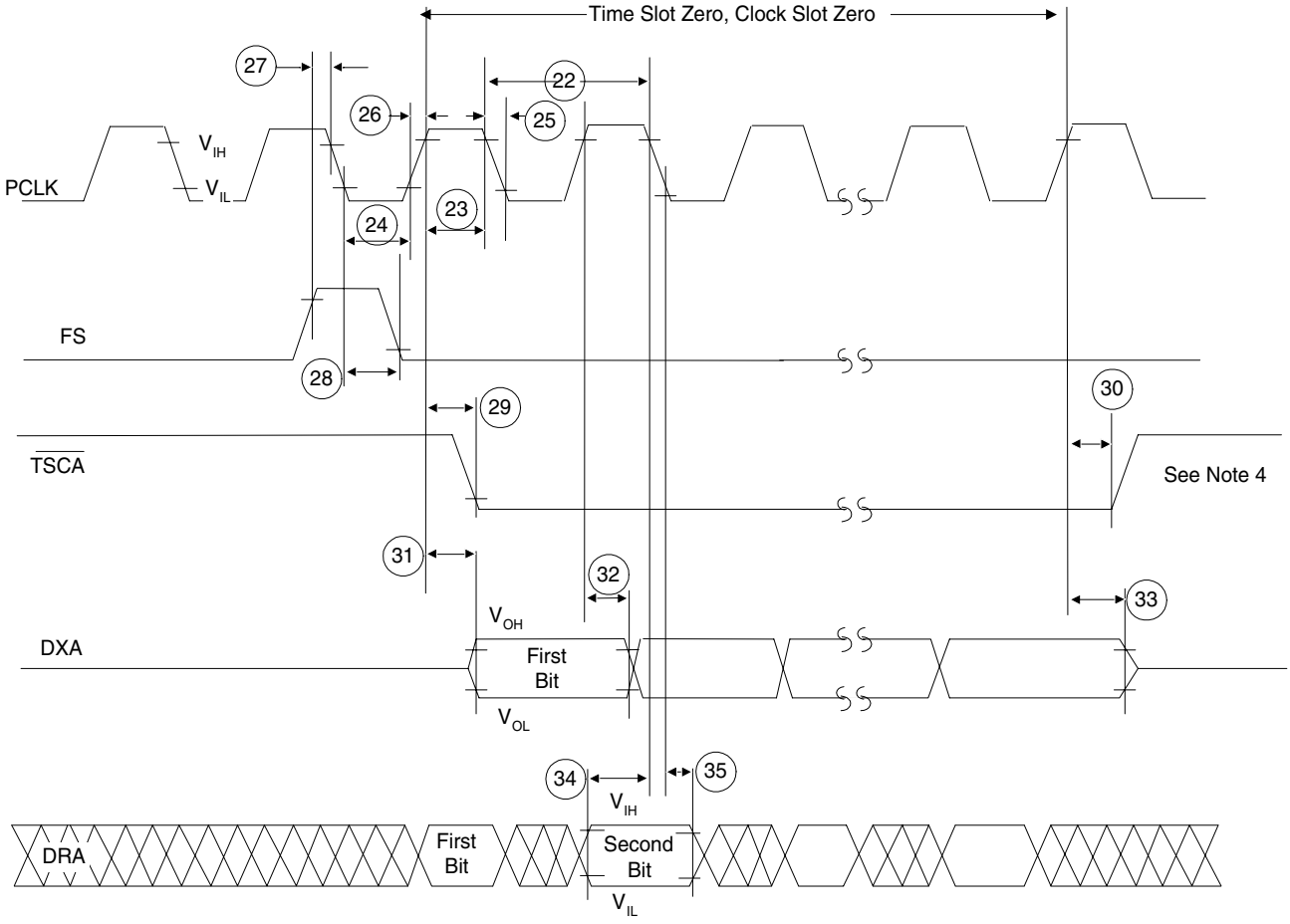


Figure 17. PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)



Master Clock Timing

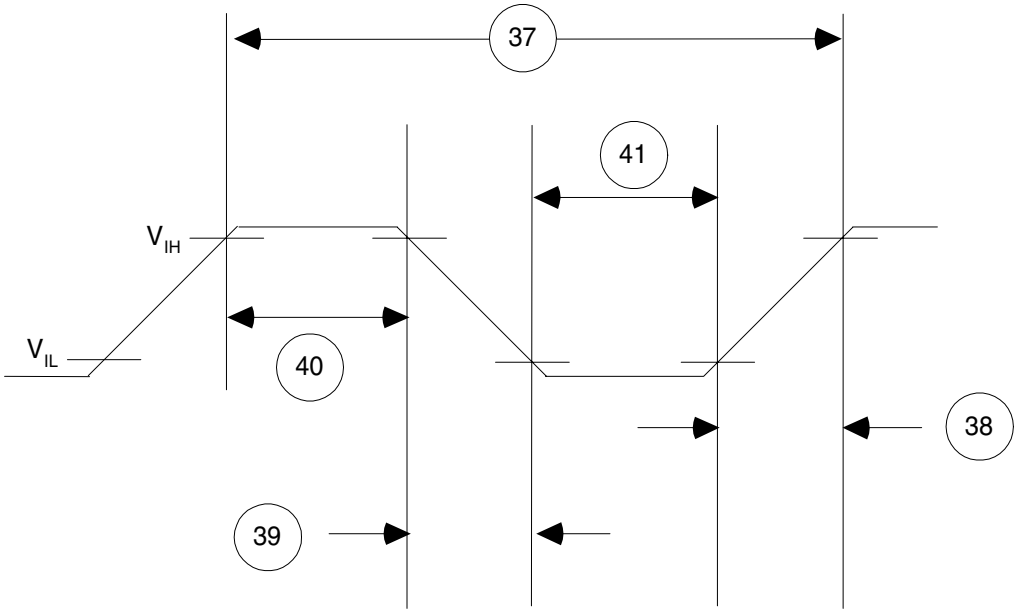
Master Clock can be sourced by MCLK or PCLK input by appropriate configuration of DCR1 (see Figure 18, on page 26). For a 2.048 mHz ± 100 PPM, 4.096 mHz ± 100 PPM, or 8.192 ± 100 PPM operation:

No.	Symbol	Parameter	Min	Typ	Max	Unit	No
37	t_{MCY}	Period	122	—	7812	ns	2,8,9
38	t_{MCR}	Rise time of clock	—	—	15		
39	t_{MCF}	Fall time of clock	—	—	15		
40	t_{MCH}	Master Clock HIGH pulse width	48	—	—		
41	t_{MCL}	Master Clock LOW pulse width	48	—	—		

Note:

1. *DCLK may be stopped in the High or Low state indefinitely without loss of information. When $\overline{CS}$ makes a transition to the High state, the last byte received will be interpreted by the Microprocessor Interface logic.*
2. *The PCM clock (PCLK) frequency must be an integer multiple of the frame sync (FS) frequency and synchronous to the MCLK frequency. The actual PCLK rate is dependent on the number of channels allocated within a frame. A PCLK of 1.544 mHz can be used for standard US transmission systems. The minimum clock frequency is 128 kHz.*
3. *$\overline{TSCA}$ is delayed from FS by a typical value of N • t_{PCY}, where N is the value stored in the time/clock slot register.*
4. *$\overline{TSCA}$ is an open drain driver. t_{TSO} is defined as the delay time the output driver turns off after the PCLK transaction. The actual delay time is dependent on the load circuitry. The maximum load capacitance on $\overline{TSCA}$ is 150 pF and the minimum pull-up resistance is 360 Ω.*
5. *The first data bit is enabled on the falling edge of $\overline{CS}$ or on the falling edge of DCLK, whichever occurs last.*
6. *The Le79Q2241/2242/2243 codec requires 2.0 µs between MPI operations. If the MPI is being accessed while the MCLK (or PCLK if combined with MCLK) input is not active, a Chip Select Off time of 20 µs is required when accessing coefficient RAM. Immediately after reset, $t_{ICSO} = \frac{2\mu s \cdot 8.192\ MHz}{f_{PCLK}}$, where f_{PCLK} is the applied PCLK frequency. Once DCR1 is programmed for the applied PCLK and MCLK, t_{ICSO} is per table specification.*
7. *If chip select is held low for 16 or more DCLK cycles, the part will reset.*
8. *Master Clock's frequency can range from 512 kHz to 8.192 MHz and can be set with: Write/Read Device Configuration Register 1, and if necessary Write/Read Master Clock Correction Register.*
9. *If PCLK is greater or equal to 512 kHz, the preferred configuration is Master Clock derived from PCLK. If a separate MCLK is used, it must be synchronous to PCLK. If PCLK is less than 512 kHz, a separate MCLK (synchronous with PCLK) with f_0 greater or equal to 512 kHz must be used.*

Figure 18. Master Clock Timing Waveform

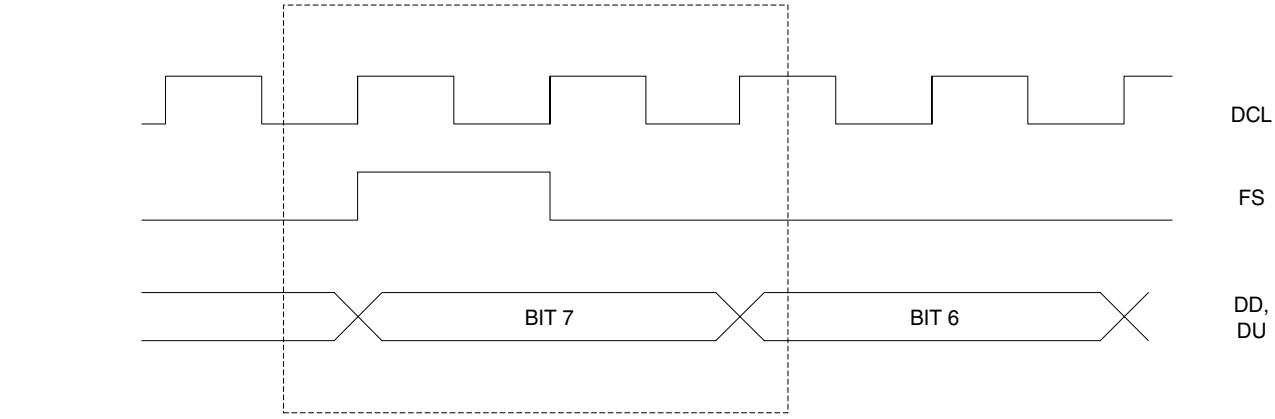


GCI Timing

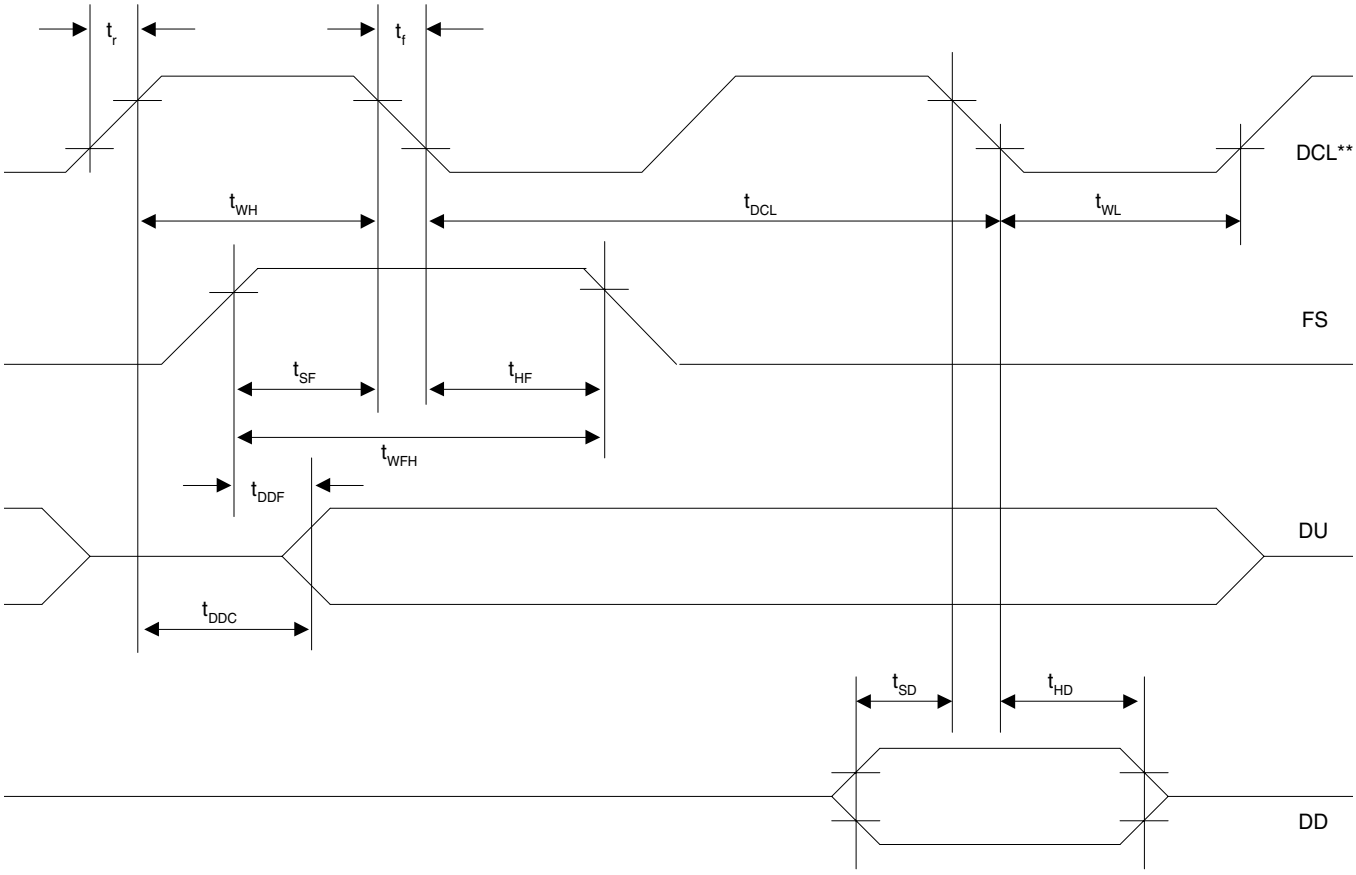
For a 2.048 mHz ± 100 PPM, 4.096 mHz ± 100 PPM, or 8.192 ± 100 PPM operation.

Symbol	Signal	Parameter	Min	Typ	Max	Unit
t_R, t_F	DCL	Rise/fall time	—	—	60	ns
t_{DCL}	DCL	Period, F_{DCL} = 2048 kHz F_{DCL} = 4096 kHz	478 239	—	498 249	
t_{WH}, t_{WL}	DCL	Pulse width	90	—	—	
t_R, t_F	FS	Rise/fall time	—	—	60	
t_{SF}	FS	Setup time	70	—	t_{DCL}–50	
t_{HF}	FS	Hold time	50	—	—	
t_{WFH}	FS	High pulse width	130	—	—	
t_{DDC}	DU	Delay from DCL edge	—	—	100	
t_{DDF}	DU	Delay from FS edge	—	—	150	
t_{SD}	DD	Data setup	t_{WH}+20	—	—	
t_{HD}	DD	Data hold	50	—	—	

Figure 19. GCI Waveforms



DETAIL A



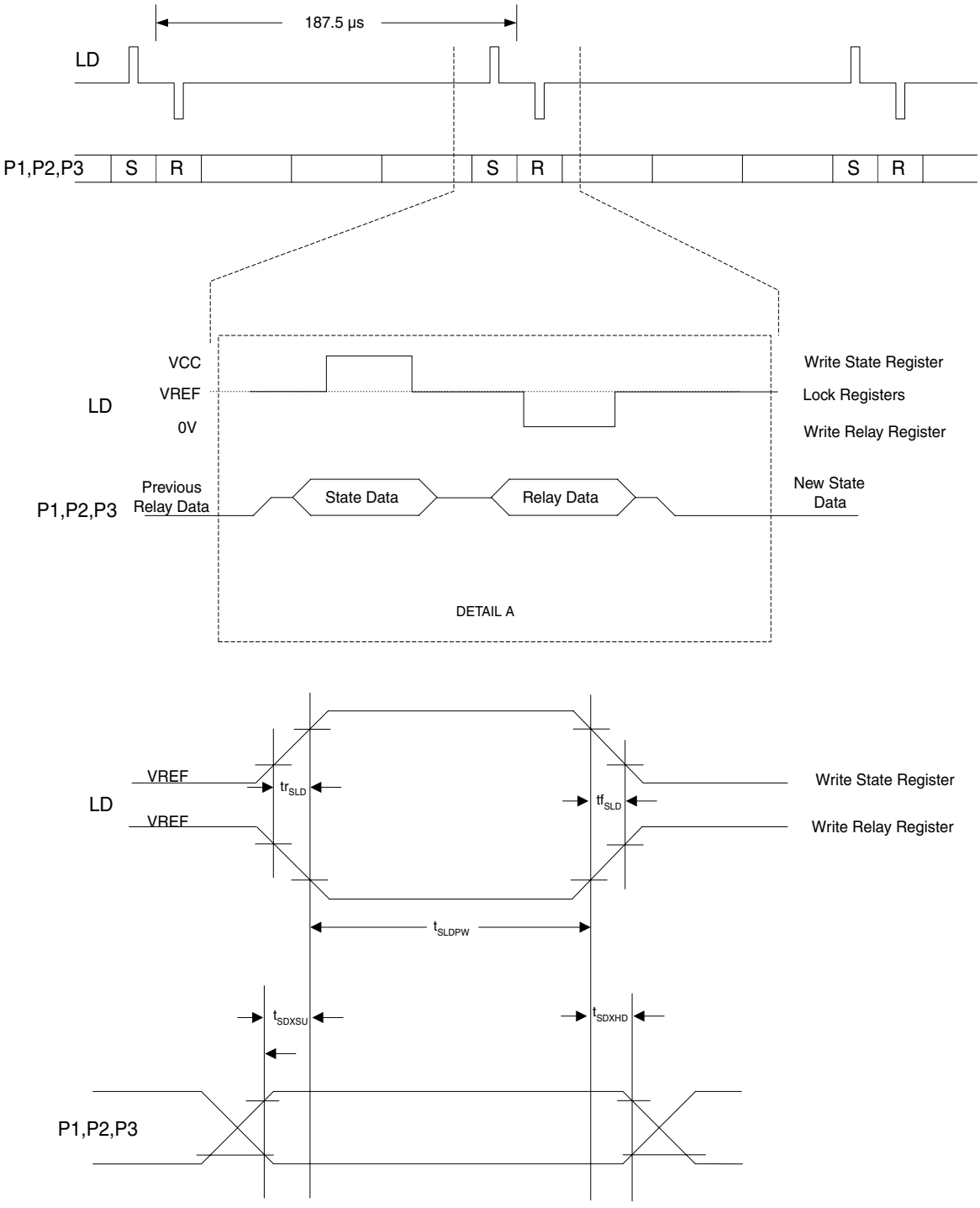
** Timing diagram valid for
F_{DCL} = 2048 or 4096 KHz

SLIC Device Timing

(See Figure 20.)

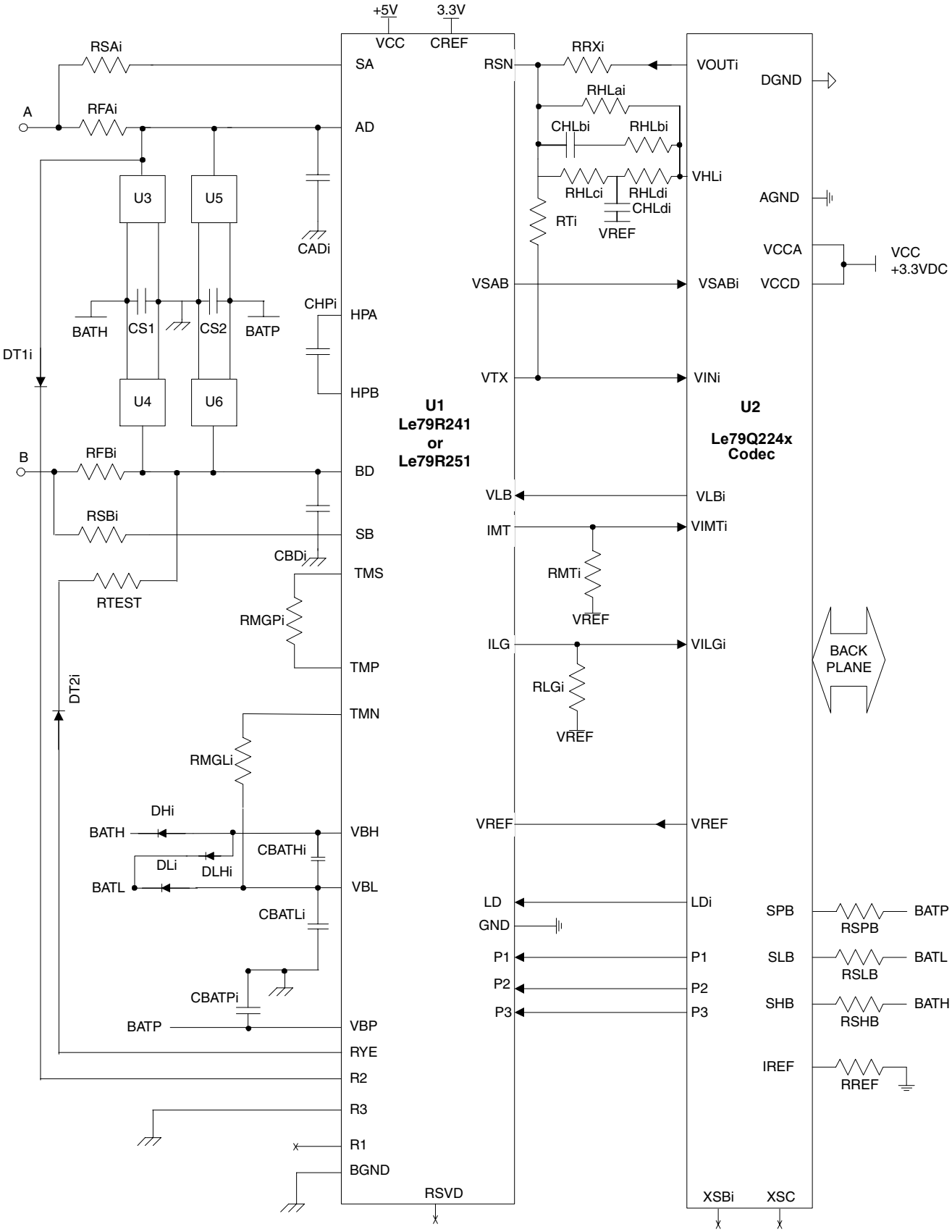
Symbol	Signal	Parameter	Min	Typ	Max	Unit
tr_{SLD}	LD	Rise time			2	ms
tf_{SLD}	LD	Fall time			2	
t_{SLDPW}	LD	LD minimum pulse width	3			
t_{SDXSU}	P1,P2,P3	P1–3 data Setup time	4.5			
t_{SDXHD}	P1,P2,P3	P1–3 data hold time	4.5			

Figure 20. SLIC Device Bus Timing Waveform



APPLICATION CIRCUITS

Figure 21. Internal Ringing Line Schematic



* Connections shown for one channel

LINE CARD PARTS LIST- INTERNAL RINGING

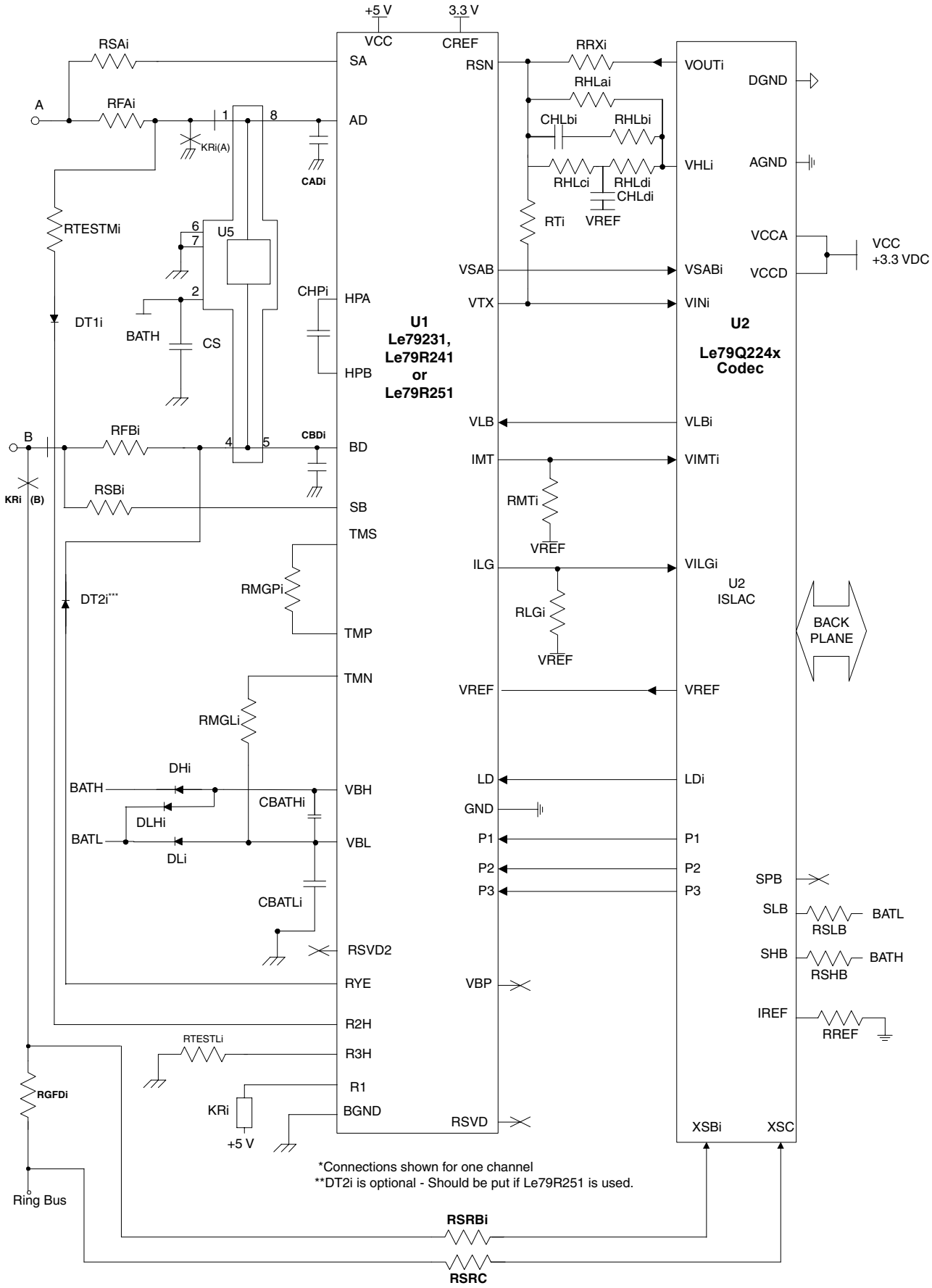
The following list defines the parts and part values required to meet target specification limits for channel i of the line card (i = 1,2,3,4).

Item	Type	Value	Tol.	Rating	Comments
U1	Le79R241, Le79R251		-		790 series SLIC device
U2	Le79Q224x		-		codec
U3, U4, U5, U6	B1100CC		-	100 V	TECCOR Battrax protector
$DT1_i$, $DT2_i$	Diode	1 A	-	100 V	
DH_i[1], DL_i, $DT1_i$, $DT2_i$, DLH_i	Diode	100 mA	-	100 V	50 ns response time
RFA_i, RFB_i	Resistor	50 Ω	2%	2 W	Fusible or PTC protection resistors
RSA_i, RSB_i	Resistor	200 kΩ	2%	1/4 W	Sense resistors
RT_i	Resistor	80.6 kΩ	1%	1/8 W	Impedance control resistor
RRX_i	Resistor	90.9 kΩ	1%	1/8 W	Receive path gain resistor
RREF	Resistor	69.8 kΩ	1%	1/8 W	Current reference setting resistor
RSHB, RSLB, RSPB	Resistor	750 kΩ	1%	1/8 W	Battery sense resistors
$RHLa_i$	Resistor	40.2 kΩ	1%	1/10 W	Feed/metering resistor
$RHLb_i$	Resistor	4.32 kΩ	1%	1/10 W	Feed/metering resistor
$RHLc_i$	Resistor	2.87 kΩ	1%	1/10 W	Feed/metering resistor
$RHLd_i$	Resistor	2.87 kΩ	1%	1/10 W	Feed/metering resistor
$CHLb_i$	Capacitor	3.3 nF	10%	10 V	Feed/metering capacitor - Not Polarized
$CHLd_i$	Capacitor	0.82 µF	10%	10 V	Feed/metering capacitor -Ceramic
RMT_i	Resistor	3.01 kΩ	1%	1/8 W	Metallic loop current gain resistor
RLG_i	Resistor	6.04 kΩ	1%	1/8 W	Longitudinal loop current gain resistor
RTEST	Resistor	2 kΩ	1%	1 W	Test board
CAD_i, CBD_i[2]	Capacitor	22 nF	10%	100 V	Ceramic
$CBATH_i$, $CBATL_i$, $CBATP_i$	Capacitor	100 nF	20%	100 V	Ceramic
CHP_i	Capacitor	22 nF	20%	100 V	High pass filter capacitor - Ceramic
$CS1_i$, $CS2_i$[2]	Capacitor	100 nF	20%	100 V	Protector speed up capacitor
$RMGL_i$	Resistor	1 kΩ	5%	2 W	Thermal management resistor
$RMGP_i$	Resistor	1 kΩ	5%	2 W	Thermal management resistor

Note:

1. *Required to insure VBH < VBL during startup. May not be needed for some supplies.*
2. *DT2i is optional - Should be put if the Le79R251 device is used.*
3. *Value can be adjusted to suit application.*

Figure 22. External Ringing Line Schematic



LINE CARD PARTS LIST - EXTERNAL RINGING

The following list defines the parts and part values required to meet target specification limits for channel i of the line card (i = 1, 2, 3, 4).

Item	Type	Value	Tol.	Rating	Comments
U1	Le79231, Le79R241, Le79R251		-		790 series SLIC device
U2	Le79Q224x		-		codec
U5	TISP61089			80 V	Transient Voltage Suppressor, Power Innovations
DLH_i[1], DH_i, DL_i, $DT1_i$ $DT2i$[2]	Diode	100 mA		100 V	50 ns response time
RFA_i, RFB_i	Resistor	50 Ω	2%	2 W	Fusible or PTC protection resistors
RSA_i, RSB_i	Resistor	200 kΩ	2%	1/4 W	Sense resistors
RT_i	Resistor	80.6 kΩ	1%	1/8 W	Impedance control resistor
RRX_i	Resistor	90.9 kΩ	1%	1/8 W	Receive path gain resistor
RREF	Resistor	69.8 kΩ	1%	1/8 W	Current reference setting resistor
$RMGL_i$, $RMGP_i$	Resistor	1 kΩ	5%	1 W	Thermal management resistors
RSHB, RSLB	Resistor	750 kΩ	1%	1/8 W	Battery Sense Resistors
$RHLa_i$	Resistor	40.2 kΩ	1%	1/10 W	Feed/Metering resistor
$RHLb_i$	Resistor	4.32 kΩ	1%	1/10 W	Feed/Metering resistor
$RHLc_i$	Resistor	2.87 kΩ	1%	1/10 W	Feed/Metering resistor
$RHLd_i$	Resistor	2.87 kΩ	1%	1/10 W	Feed/Metering resistor
$CHLb_i$	Capacitor	3.3 nF	10%	10 V	Feed/Metering capacitor - Not Polarized
$CHLd_i$	Capacitor	0.82 mF	10%	10 V	Feed/Metering capacitor - Ceramic
RMT_i	Resistor	3.01 kΩ	1%	1/8 W	Metallic Current Sense Resistors
RLG_i	Resistor	6.04 kΩ	1%	1/8 W	Longitudinal Current Sense Resistors
$RTESTM_i$	Resistor	2 kΩ	1%	1 W	Metallic test
$RTESTL_i$	Resistor	2 kΩ	1%	1 W	Longitudinal test
CAD_i, CBD_i [3]	Capacitor	22 nF	10%	100 V	Ceramic
$CBATH_i$, $CBATL_i$	Capacitor	100 nF	20%	100 V	Ceramic
CHP_i	Capacitor	22 nF	20%	100 V	Ceramic
CS_i[3]	Capacitor	100 nF	20%	100 V	Protector speed up capacitor
$RGFD_i$	Resistor	510 Ω	2%	2 W	1.2 W typ
$RSRB_i$, RSRC	Resistor	750 kΩ	1%	1/4 W	External Ringing sense resistors
KR_i	Relay	5 V Coil			DPDT

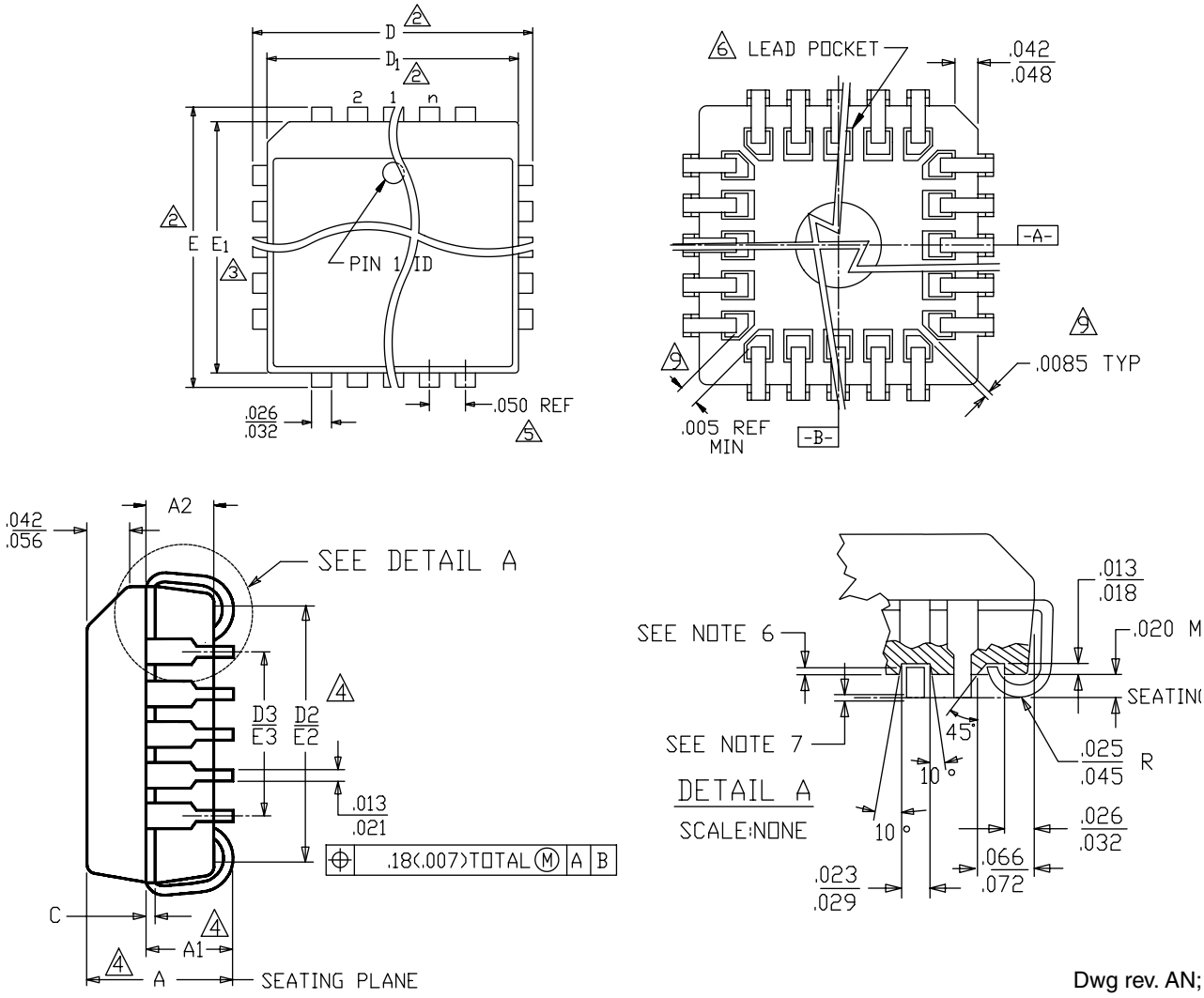
Note:

1. *Required to insure VBH < VBL during startup. May not be needed for some supplies.*
2. *DT2i is optional - Should be put if Le79R251 device is used.*
3. *Value can be adjusted to suit application.*

PHYSICAL DIMENSIONS

68-Pin PLCC

PLCC 068



Dwg rev. AN;

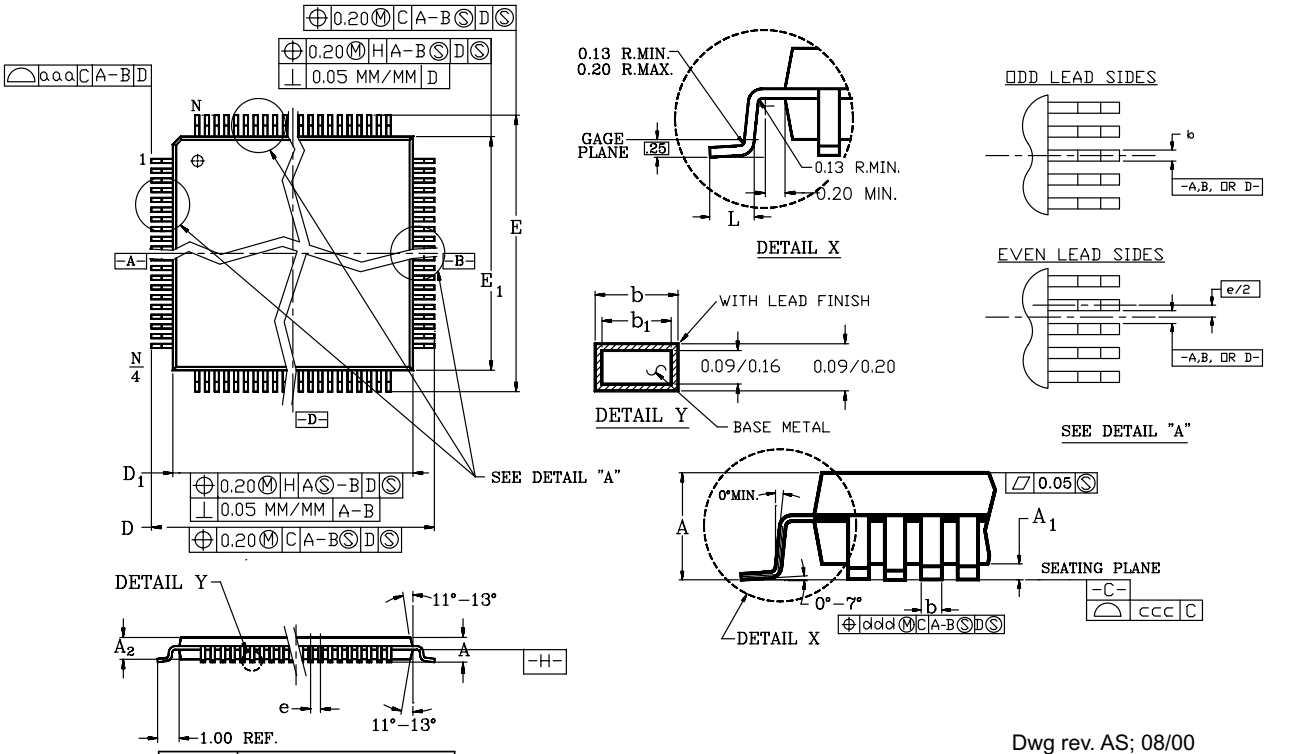
PACKAGE	PLCC 068	
JEDEC	MO-047(B)AE	
SYMBOL	MIN	MAX
A	.165	.180
A1	.090	.130
A2	.062	.083
D	.985	.995
D1	.950	.956
D2	.890	.930
D3	.800	REF
E	.985	.995
E1	.950	.956

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONS "D" AND "E" ARE MEASURED FROM OUTERMOST POINT.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE CORNER MOLD FLASH. ALLOWABLE CORNER MOLD FLASH IS .010
4. DIMENSIONS "A", "A1", "D2" AND "E2" ARE MEASURED AT THE POINTS OF CONTACT TO BASE PLAN
5. LEAD SPACING AS MEASURED FROM CENTERLINE TO CENTERLINE SHALL BE WITHIN ±.005 INCH.
6. J-LEAD TIPS SHOULD BE LOCATED INSIDE THE "POCKET.
7. LEAD COPLANARITY SHALL BE WITHIN .004 INCH AS MEASURED FROM SEATING PLANE. COPLANARITY IS MEASURED PER AMD 06-500.
8. LEAD TWEEZE SHALL BE WITHIN .0045 INCH ON EACH SIDE

64-Pin Thin Quad Flat Pack (TQFP)

PQT 064



Dwg rev. AS; 08/00

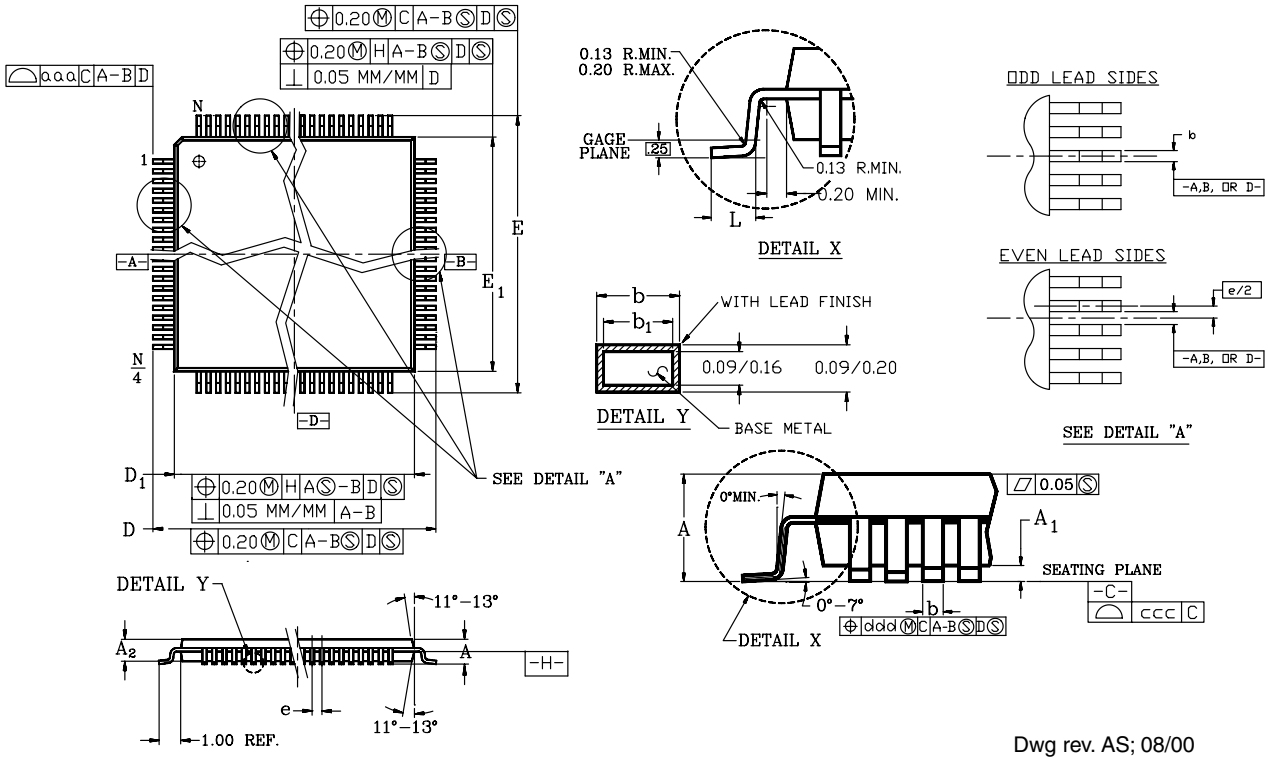
PACKAGE	PQT 064		
JEDEC	MS-026 (C) ACD		
SYMBOL	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	--	0.15
A2	0.95	1.00	1.05
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
L	0.45	0.60	0.75
N	64		
e	0.50 BSC.		
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
TOLERANCES OF FORM AND POSITION			
ccc	0.08		
ddd	0.08		
aaa	0.20		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DATUM PLANE -H- IS LOCATED AT THE MOLD PARTING LINE AND IS COINCIDENT WITH THE BOTTOM OF THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY.
3. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254mm PER SIDE. DIMENSIONS "D1" AND "E1" INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-
4. DIMENSION "B" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
5. CONTROLLING DIMENSIONS: MILLIMETER.
6. DIMENSIONS "D" AND "E" ARE MEASURED FROM BOTH INNERMOST AND OUTERMOST POINTS.
7. DEVIATION FROM LEAD-TIP TRUE POSITION SHALL BE WITHIN ±0.076 MM. FOR PITCH >0.5mm. AND WITHIN ±0.04 FOR PITCH ≤ 0.5 mm.
8. LEAD COPLANARITY SHALL BE WITHIN: (REFER TO 06-500)
   1- 0.10 mm FOR DEVICES WITH LEAD PITCH OF 0.65-0.80 mm.
   2- 0.076 mm FOR DEVICES WITH LEAD PITCH OF 0.50 mm.
   COPLANARITY IS MEASURED PER SPECIFICATION 06-500.
9. HALF SPAN (CENTER OF PACKAGE TO LEAD TIP) SHALL BE 15.30±.165{.602"±.0065"}
10. "N" IS THE TOTAL NUMBER OF TERMINALS.
11. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF THE PACKAGE BY 0.15 MILLIMETERS.
12. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026.
13. THE 160 LEAD IS A COMPLIANT DEPOPULATION OF THE 176 LEAD MS-026 VARIATION BGA.

80-Pin Thin Quad Flat Pack (TQFP)

PQT 080



Dwg rev. AS; 08/00

PACKAGE	PQT 080		
JEDEC	MS-026 (C) ADD		
SYMBOL	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
D	14.00 BSC		
D1	12.00 BSC		
E	14.00 BSC		
E1	12.00 BSC		
L	0.45	0.60	0.75
N	80		
e	0.50 BASIC		
b	0.17	0.22	0.27
b1	0.16	0.20	0.23
TOLERANCES OF FORM AND POSITION			
ccc	—	—	0.08
ddd	—	—	0.08
aaa	—	—	0.20

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. DATUM PLANE -H- IS LOCATED AT THE MOLD PARTING LINE AND IS COINCIDENT WITH THE BOTTOM OF THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY.
3. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254mm PER SIDE. DIMENSIONS "D1" AND "E1" INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-
4. DIMENSION "B" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
5. CONTROLLING DIMENSIONS: MILLIMETER.
6. DIMENSIONS "D" AND "E" ARE MEASURED FROM BOTH INNERMOST AND OUTERMOST POINTS.
7. DEVIATION FROM LEAD–TIP TRUE POSITION SHALL BE WITHIN ±0.076 MM. FOR PITCH >0.5mm. AND WITHIN ±0.04 FOR PITCH ≤ 0.5 mm.
8. LEAD COPLANARITY SHALL BE WITHIN: (REFER TO 06–500)
   1– 0.10 mm FOR DEVICES WITH LEAD PITCH OF 0.65–0.80 mm.
   2– 0.076 mm FOR DEVICES WITH LEAD PITCH OF 0.50 mm.
   COPLANARITY IS MEASURED PER SPECIFICATION 06–500.
9. HALF SPAN (CENTER OF PACKAGE TO LEAD TIP) SHALL BE 15.30±.165{.602"±.0065"}
10. "N" IS THE TOTAL NUMBER OF TERMINALS.
11. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF THE PACKAGE BY 0.15 MILLIMETERS.
12. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS–026.

REVISION HISTORY

Revision A to B

- Revision A was a condensed version of the datasheet while Revision B contains the full version.

Revision B to C

- Page 14, Line card Parts List, Rows CHLbi and CHLdi: switched the numbers in the “Values” column.

Revision C to D

- Page 12, Figure 5, DT1i was added and the last note was modified.
- Page 14, Line card Parts List, Item U3, U4 Type information was changed.

Revision D to E

- Updated document to new format.
- In Pin Descriptions Table, changed I/O status of $\overline{\text{TSCB}}$ to "O"
- In DC Specifications Table, the following changes were made:
  - changed information for "Quad ISLAC Power Dissipation".
  - Updated "Min", "Max", and "Typ" values for Input Leakage Current (VIN1-4, VSAB1-4, VILG1-4, VIMT1-4, VSAB1-4)
  - Updated "Min", "Max", and "Typ" values for Output Leakage Current (VOUT1-4 or VLB1-4)
- Made the following changes to the Transmission and Signaling Specifications table:
  - Reformatted table
  - For Insertion Loss, changed one of the "A-D + D-A" items to "A-D – D-A"
  - For PSRR, added "A-D" to item; added Min value of 37
  - For Image frequency, added "D-A" to item; added Min value of 37
  - For DISN gain accuracy, changed conditions to: Gdisn = –0.9375 to 0.9375; Vin = 0 dBm0
  - For Crosstalk TX or RX to TX; TX or RX to RX, added 0dBm0 to conditions
- Divided Transmit and Receive Path Attenuation vs. Frequency graphic into two separate graphics
- In the "Intermodulation Distortion" section, changed text to "TBD"
- Updated PCM Switching Characteristics graphic.
- In "Master Clock" section, added information for t_{MCY}; added Note 8
- Updated External Ringing Line card schematic.
- Added a line card parts list.
- Updated all "Physical Dimensions" graphics.

Revision E to F

- In Pin Descriptions Table, pins LD1-LD4, changed description for logic 0 to < 0.4 V; changed description for logic 1 to (V_{CC} – 0.4 V)
- In DC Specifications Table, item 6, removed "Output current" row; inserted "Medium Voltage" row.
- Subscripted channel numbers throughout document.

Revision F to G

- Corrected physical dimensions for 64-Pin TQFP.

Revision G to H

- Updated device name from Am79Q2241/2242/2243 to Le79Q2241/2242/2243 throughout document
- The following pin changes were made to the 80-pin TQFP Connection Diagram:
  - Pin 35 changed from DIO/S1 to DOUT
  - Pin 36 changed from DCLK/S0 to DIN/S1
  - Pin 37 changed from $\overline{\text{CS}}$/$\overline{\text{RST}}$ to DCLK/S0
  - Pin 38 changed from N/C to $\overline{\text{CS}}$/$\overline{\text{RST}}$
- In "Transmission and Signaling Specifications," DISN Gain Accuracy, the following changes were made:
  - Changed Min from -0.25 to -.05

  - Changed Typ from 0 to +0.2
  - Changed Max from +0.25 to +0.45
- Added SLIC Timing Specifications Table
- Added waveform graphic
- Updated internal and external ringing line card schematics and line card parts lists
- Removed Note 13 from 80-pin TQFP physical dimensions graphic

Revision H to I1

- In *Pin Descriptions*, revised I/O pin description
- In *DC Specifications*, the following changes were made:
  - Item 2, Input High Voltage, changed Min from 2.36 to 2.46
  - Item 11, Input Voltage, removed Min/Max values
  - Added item 14A, VHL gain error
  - Item 18, Max Output Voltage on VOUT, removed Min/Max values
  - Item 20, Max Output Voltage on VHL, modified item description; removed Min/Max values
  - Removed item 21, VSAB A/D gain error
  - Removed item 23, VIMT A/D gain error
  - Removed item 25, VILG A/D gain error
  - Removed item 27, Battery read A/D gain error
  - Items 22, 24, 26, 28: changed offset error to absolute error; modified Min/Max values
- In *Transmission Specifications*, item 9 DISN Gain Accuracy, removed Min/Max values

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