POP-12™ Device

OC-12 SONET/SDH Path Overhead Processor, Retimer, and Cross Connect

TXC-06603

DATA SHEET

FEATURES

- Path overhead (POH) processing for up to 12 x STS-1 SPEs or 4 x VC-4/STS-3c SPEs
- 4 Tx and 4 Rx Pointer Tracking State Machines (PTSM). Each performs pointer tracking of up to three STS-1 pointers in STS-3 mode, or a single STS-3c pointer in STS-3c mode, or a single AU-4 pointer in STM-1 mode.
- Non-blocking cross connects allow AU-3s or AU-4s to be routed to any like direction Telecom Bus
- Four full duplex 19.44 Mbyte/s Telecom Bus interfaces
- Supports STS-3, STS-3c, or STM-1 SPE/VCs on a per Telecom Bus basis
- Standard 8-bit wide host microprocessor interface (selectable between Intel or Motorola)
- Maskable interrupt request bits for host interface
- Performance counters for receive B3 errors and REI
- Retimer modules for each Telecom Bus can retime data and optionally track SONET/SDH pointers in either the TX or RX direction
- Loss of Pointer (LOP), Path AIS (PAIS), and POH alarm interrupt request bits provided for each STS/AU-4
- Boundary scan capability (IEEE 1149.1)
- + 3.3V power supply
- 456-lead plastic ball grid array package (PBGA), 27 mm x 27 mm

DESCRIPTION

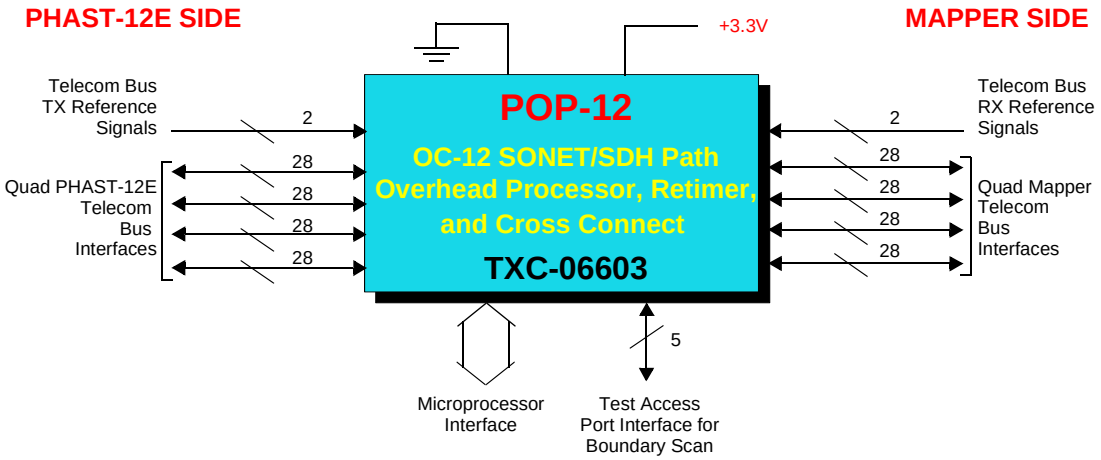
The POP-12™ integrates STS-1-SPE/STS-3c-SPE/VC-4 POH processing, AU-3/AU-4 pointer processing/retiming, and AU-3/AU-4 cross connect for four Telecom Bus interfaces into one package. It provides an interface to high density mapper applications when used with the TranSwitch PHAST-12E (TXC-06212), and mapper and framer devices. The POP-12 device is designed to provide a seamless interface with the PHAST-12E device.

In SDH mode, the POP-12 can interface up to four Telecom Buses, and simultaneously terminate and process up to four individual VC-4 POH streams, while providing pointer retiming at the outputs of the Telecom Buses. The two integrated non-blocking cross connects can cross connect AU-4s to any Telecom Bus (in the same direction).

In SONET mode, the POP-12 provides the same functions as in SDH mode for STS-3c payloads, plus, it can alternatively terminate and process up to twelve individual STS-1-SPE POH streams for four individual STS-3s. Its two integrated non-blocking cross connects allow either AU-3 or AU-4 level cross connecting to any Telecom Bus (in the same direction), and perform pointer retiming at the outputs of the Telecom Buses.

APPLICATIONS

- Auxiliary POH processor for PHAST-12E
- Interconnects multiple or single SONET/SDH Overhead Terminators and mapper devices
- IXC/ILEC Central Office Equipment
- OC-12/48 Add/Drop Mux
- Multiple STM-1/STS-3c/STS-3 Add/Drop Mux
- Grooming Switching for Metro Networks
- TransMux for DS-3 to VT mapping
- T1/E1 or T3/E3 aggregation
- Protection Applications



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APPLICABLE STANDARDS DOCUMENTATION

Standards documents applicable to the functions of the POP-12 are listed in the table below. The addresses and other contact information for the organizations that publish or distribute them are provided at the rear of this document. References to these documents are made in the text by showing the document number in brackets, e.g., [G.707].

Document No.	Description
G.707	ITU-T, Network Node Interface for the Synchronous Digital Hierarchy, (03/96)
G.783	ITU-T, Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks, (04/97)
GR-253	Bellcore, GR-253-CORE, Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria, Issue 2, (12/95), Revision 2 (01/99)
IEEE 1149.1	IEEE Standard Access Port and Boundary Scan Architecture (1990, supplement a 1993, and supplement b 1994)

SCOPE

This document provides a detailed description of the features, characteristics and operation of the TranSwitch POP-12 (12-Channel Path Overhead Processor Retimer, and Cross Connect) device. The primary application of the POP-12 is to provide the Path Overhead Processing for the PHAST-12E device in Telecom applications.

Throughout this document, SONET and SDH terminologies are used interchangeably when describing portions of the payload or overhead of a SONET/SDH frame. SDH terminology provides more “granularity” for describing parts of a frame and hence is used more often. e.g., An STS-3c-SPE can be referred to as a VC-4 in this document, an STS-3c-SPE plus its pointer is referred to as an AU-4, etc.

OVERVIEW

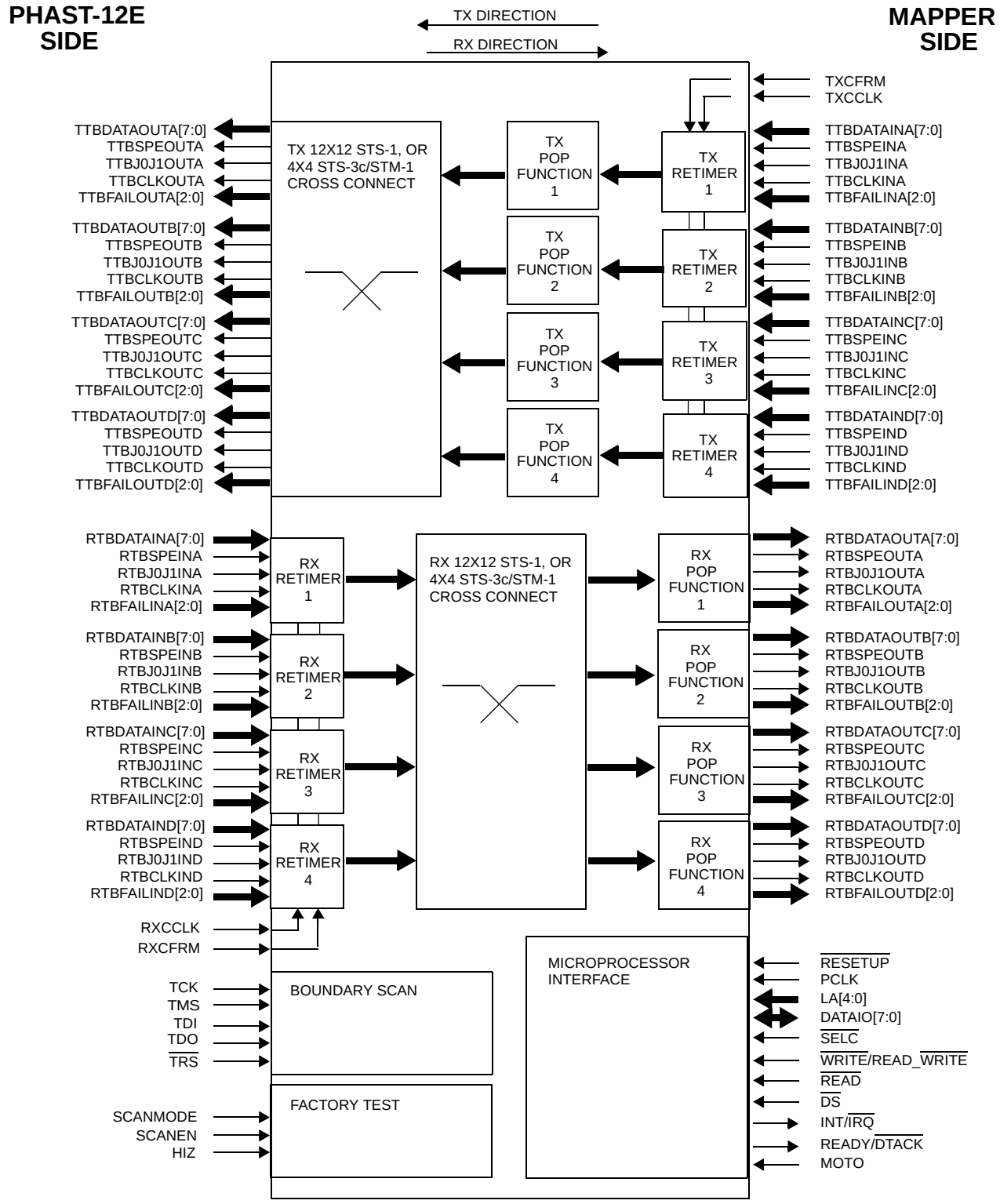


Figure 1. POP-12 TXC-06603 High Level Block Diagram

The POP-12, integrates STS-1-SPE/STS-3c-SPE/VC-4 POH processing, AU-3/AU-4 pointer processing/retiming, and AU-3/AU-4 cross connect for four telecom bus interfaces into one package. It provides an interface to high density mapper applications when used with TranSwitch's PHAST-12E and mapper and framer devices. In fact the POP-12 device is designed to provide a seamless interface with the PHAST-12E device.

In SDH mode, the POP-12 can interface up to four telecom buses, and simultaneously terminate and process up to four individual VC-4 POH streams, while providing pointer retiming at the output telecom busses. The two integrated non-blocking cross connects can cross connect AU-4s to any telecom bus (in the same direction).

In SONET mode, the POP-12 provides the same functions as in SDH mode for STS-3c payloads, plus, it can alternatively terminate and process up to twelve individual STS-1-SPE POH streams for four individual STS-3s. Its two integrated non-blocking cross connects allow either AU-3 or AU-4 level cross connecting to any telecom bus (in the same direction), and perform pointer retiming at the output telecom busses.

Standard compliant performance monitoring and alarm processing is provided and can be accessed through a generic microprocessor interface that can be configured to support either an INTEL or MOTOROLA style bus. Detected alarms can generate maskable interrupts to the host microprocessor.

Table 1. Signals Terminated By The POP-12

Signal	Number of Signals that can be terminated	Payload Granularity	Total Number of Payloads that can be Simultaneously Processed	Cross Connect Type available
STS-3	4	STS-1-SPE	12xSTS-1-SPE	AU-3
STS-3c	4	STS-3c-SPE	4xSTS-3c-SPE	AU-4
STM-1	4	VC-4	4xVC-4	AU-4

GENERAL DEVICE LEVEL

- Four full duplex telecom bus interfaces.
- Supports STS-3, STS-3c, or STM-1 SPE/VCs on a per Telecom Bus basis.
- Standard 8-bit wide microprocessor Interface (lead selectable between Intel or Motorola).
- Performance counters.
- Maskable interrupt request bits.
- Retimer modules for each telecom bus can retime data and optionally track SONET/SDH pointers in either the TX or RX direction.
- Non-blocking cross connects allow AU-3/AU-4s to be routed to any Telecom Bus. The granularity for payloads that can be handled by the cross connect is shown in Table 1 above.
- POH processing for up to 12xSTS-1-SPEs or 4xVC-4/STS-3c-SPE.

TELECOM BUS INTERFACE

- 8-bit wide data interface
- 19.44 MHz clock (± 20ppm)
- SPE indication
- J0, J1, and optionally V1 pulses.
- In the TX direction, the transmitted H4 byte can optionally be synchronized to the input V1 pulse.
- In the RX direction, V1 pulses can optionally be output which are synchronized to the received H4 byte.

- Fail signals. Input fail signals can be used to force all 1s in its corresponding SPE/AU. Output Fail signals indicate that either the corresponding fail input has been activated or that Loss of Pointer or Path AIS have been detected while the pointer tracking state machine in the retimer block has not been bypassed. The Fail inputs go through a cross connect so that they are cross connected along with their corresponding SPE/VC to the corresponding fail output.

MICROPROCESSOR INTERFACE

- 8-bit wide data bus
- 3 internal registers are used to access the internal 16-bit address space. Two address registers contain the address to be accessed. The third register is used to read or write to the address pointed to by the two address registers.
- Intel or Motorola style bus interfaces selected by hardware strap.
- Asynchronous microprocessor interface clock from 8-20 MHz.
- Interrupt lead driven by maskable interrupt request bits. Active high for Intel interface and active low for Motorola Interface.
- READY/$\overline{\text{DTACK}}$ lead.
- Provides access to all control bits, interrupt request bits, and performance counters. All interrupt request bits latch the interrupt request and clear on read. They become set again if the causing alarm persists. Counters are non-saturating and roll over when they overflow.

RETIMER BLOCK

Retimer blocks are identical for both the TX and RX directions. The POP-12 contains 4 retimer blocks in the TX direction and 4 in the RX direction. This allows up to 12 STS-1-SPEs to be processed in each direction. The features of an individual Retimer Block is given below:

- Telecom Bus interface for input and output.
- Supports STS-3, STS-3c, or STM-1 traffic.
- Can be programmed to find pointers using C1 byte pulse or $A2_3$ byte pulse from input Telecom Bus.
- Pointer Tracking State Machine (PTSM) performs pointer tracking of up to three STS-1 pointers in STS-3 mode, or a single STS-3c pointer in STS-3c mode, or a single AU-4 pointer in STM-1 mode.
- 8-bit counters are provided for counting positive pointer justifications detected.
- 8-bit counters are provided for counting negative pointer justifications detected.
- Loss of Pointer (LOP) and Path AIS (PAIS) detected interrupt request bits provided for each STS/AU-4 pointer.
- All 1s signal is generated downstream if LOP or PAIS are detected.
- Output of PTSM is buffered in a 64-byte FIFO. There are three 64-byte FIFOs, one for each STS. The three 64-byte FIFOs operate in parallel as a single FIFO when in STS-3c or STM-1 modes.
- A retimer block takes data from the FIFOs and retimes them to a reference clock.
- The output frame can be synchronized to an optional frame pulse with programmable delays of 1, 4, 7, 10, 13, 16, or 19. There is one reference clock and frame input for the TX Retimer Blocks and there is another reference clock and frame input for the RX Retimer Blocks.
- The PTSM can be bypassed and the input Telecom Bus signal can just be retimed. In this case the SPE J0 and J1 signals are required.
- When bypassed or not bypassed, the Retimer Blocks can accept an optional V1 pulse without causing problems. However, in the TX direction, the V1 pulse can be used to synchronize the TX H4 POH byte to provide a multiframe indication for VT and Low Order VC applications.

CROSS CONNECT BLOCK

The TX and RX cross connect blocks are identical.

- The cross connect blocks have four Telecom Bus inputs and four Telecom Bus outputs.
- Any of the AU-3/AU-4 output from the Retimer Block can be cross connected and applied to any of the Cross Connects output Telecom Busses, in the same direction. e.g., STS-1 #3 of input TX Telecom Bus 1 can be cross connected to STS-1 #2 of output TX Telecom Bus 3.
- Broadcasting of AU-3/AU-4 can be done.

RX POPFUNCTION BLOCK

- Can support STS-3/STS-3c/STM-1 POH bytes.
- All RX POH bytes are written to on chip memory and can be read.
- 64-byte circulating buffer for RX J1 bytes.
- 16-bit counter for counting RX B3 errors.
- 16-bit counter for counting RX FEBE/REI. RX FEBE/REI greater than 8H are counted as 0H.
- C2 Mismatch (SLM) detection based on microprocessor written expected C2 byte. RX C2 byte=01H is not considered a mismatch. An SLM interrupt request bit is provided.
- RX Unequipped Signal Label (UNEQ) detection. An UNEQ interrupt request bit is provided.
- Path Trace Mismatch (TIM) alarm detection (64-byte or 16-byte) based on microprocessor written expected J1 message. A TIM interrupt request bit is provided.
- 1-bit or 3-bit path RDI can be detected. The detection of LOP or PAIS disables RDI detection. A RDI interrupt request bit is provided.
- V1 pulse generated on output Telecom Bus interface based on RX H4 byte=00H.
- Control bits provided for enabling disabling RX C2 byte processing, RX V1 pulse generation, RX J1 byte processing, RX FEBE reception.
- RX All1s signal is generated when LOP or PAIS are detected by the PTSM.
- RX All 1s signal is generated when SLM, UNEQ, or TIM are detected and the appropriate POH byte processing is enabled.

TX POPFUNCTION BLOCK

- Can support STS-3/STS-3c/STM-1 POH bytes.
- The J1, C2, F2, F3, K3, and N1 POH bytes can be inserted by the POP-12 or can be passed through unaltered based on control bit settings.
- 64-byte TX J1 buffer can be used to transmit 64-byte or 16-byte J1 message.
- B3 can be recalculated or passed through.
- G1 byte can be passed through or generated based on received alarms and B3 errors.
    - TX FEBE is generated based on received B3 errors. A 10-nibble deep FIFO is used to buffer the transfer of B3 errors from the RX to the TX Popfunction Blocks. TX FEBE counts are zeroed out during detection of RX LOP or PAIS.
    - TX RDI is generated as single bit (STM-1 mode) or three bit (STS-3/STS-3c modes) for at least 10 frames according to the table below:

TX RDI Generation

Mode	Alarm	RDI Code	Priority
STS-3/STS-3c	LOP, Path AIS	101	1
	UNEQ, TIM	110	2
	SLM[a]	010	3
	No Alarm	001	4
STM-1[a]	LOP, Path AIS, UNEQ, TIM	100	N/A
	No Alarm	000	N/A

a. A control bit exists for enabling/disabling SLM from generating an RDI. In STM-1 mode that control bit should be set to disable RDI generation. However, RDI can be generated in STM-1 mode if the control bit is set to do so.

- TX H4 byte can be passed through, or a fixed value can be transmitted, or a multiframe count that is synchronized to an input V1 pulse can be generated.
- Control bits provided to replace the input data with all 0s. When used with the TX POH control bits, either Unequipped or Supervisory Unequipped signals can be transmitted in any STS-1-SPE, STS-3c-SPE, or VC-4.

MECHANICAL AND PACKAGING REQUIREMENTS

- 456 lead, 27mm x 27mm plastic Ball Grid Array (BGA)

POWER

- 2.0 Watts.

BOUNDARY SCAN

The Boundary Scan Port includes a five-lead TAP (Test Access Port) that conforms to the IEEE 1149.1-1994 standard for JTAG testing. This TAP provides external boundary scan to read and write the POP-12 input and output leads from the TAP for board and component testing.

LEAD DIAGRAM

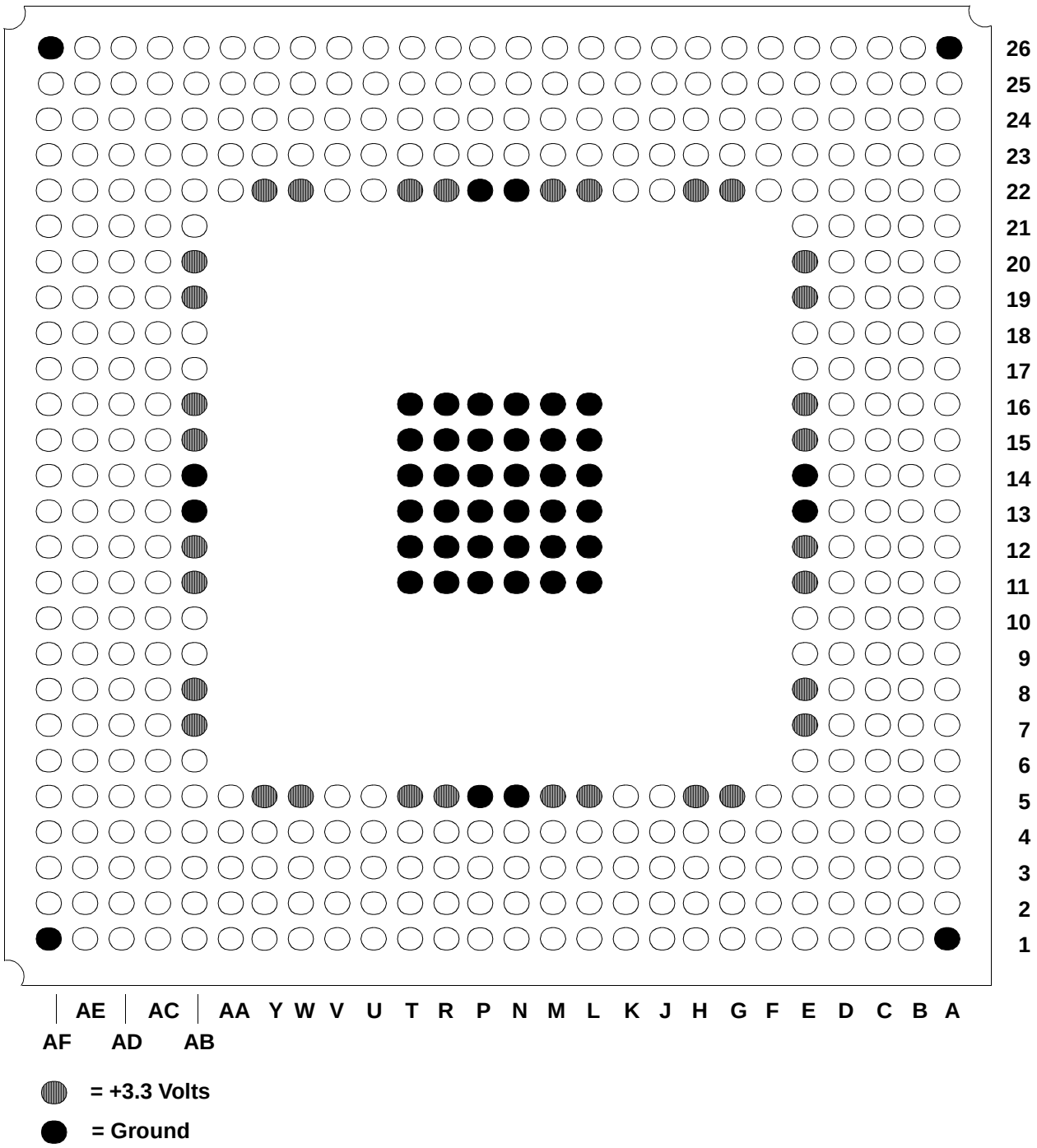


Figure 2. POP-12 TXC-06603 Lead Diagram (Bottom View)

LEAD DESCRIPTIONS

Please note that none of these leads are 5 V tolerant.

The electrical characteristics of the I/O types (e.g., LVTTL, LVTTLp, etc.) can be found in the section “Input, Output and Input/Output Parameters” on page 29.

POWER AND GROUND LEADS

Lead Name	Lead No.	Lead Description
GND	A1, A26, E13, E14, L11, L12, L13, L14, L15, L16, M11, M12, M13, M14, M15, M16, N5, N11, N12, N13, N14, N15, N16, N22, P5, P11, P12, P13, P14, P15, P16, P22, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16, AB13, AB14, AF1, AF26	**Ground:** 0-volt reference.
VDD	E7, E8, E11, E12, E15, E16, E19, E20, G5, G22, H5, H22, L5, L22, M5, M22, R5, R22, T5, T22, W5, W22, Y5, Y22, AB7, AB8, AB11, AB12, AB15, AB16, AB19, AB20	**Power (Digital):** +3.3V ± 5% power supply.
NC	A2, A3, A9, A22, A25, B1, B2, B3, B7, B9, B14, B16, B18, B20, B21, B24, B25, B26, C1, C2, C3, C11, C12, C17, C23, C24, C25, D3, D4, D5, D7, D18, D23, D24, D25, E4, E5, E9, E22, E23, F2, F22, G2, G23, G24, H1, J2, J22, J23, K23, K25, L3, M2, M24, N2, P23, T1, T25, U2, U26, V2, W3, W4, Y25, Y26, AA4, AA22, AA25, AB1, AB4, AB5, AB9, AB10, AB21, AB22, AB23, AB24, AC3, AC4, AC21, AC22, AC23, AC24, AC25, AD2, AD3, AD5, AD10, AD21, AD22, AD23, AD24, AD25, AD26, AE1, AE2, AE3, AE6, AE13, AE22, AE23, AE24, AE25, AE26, AF2, AF8, AF10, AF11, AF23, AF24, AF25	**No Connect:** NC leads are not to be connected, not even to another NC lead, but must be left floating. Connection of NC leads may impair performance or cause damage to the device. If future revisions of the device are made, then these leads may have functions associated with them.

TELECOM BUS INTERFACE LEADS

Lead Name	Lead No.	I/O	Type	Lead Description
TXCCLK	A4	I	LVTTLp	**Transmit Reference Clock:** TXCCLK is provided as a transmit reference timebase for devices connected to the transmit Telecom Bus interface. TXCCLK is configured to be 19.44 MHz ± 20ppm. The TX Telecom Bus inputs are retimed to this clock. All Telecom Bus 1-4 transmit output signals are clocked out of the POP-12 on the rising edge of this clock.
TXCFRM	B4	I	LVTTLd	**Transmit Reference Frame Pulse:** TXCFRM along with TXCCLK can be used to synchronize the data that is input to the Telecom Bus ports to a common frame reference. If this lead is not used it must be grounded, in which case the output TX Telecom Bus signals will be aligned to an internally generated frame reference.

Lead Name	Lead No.	I/O	Type	Lead Description
TTBDATAINA(7) TTBDATAINA(6) TTBDATAINA(5) TTBDATAINA(4) TTBDATAINA(3) TTBDATAINA(2) TTBDATAINA(1) TTBDATAINA(0)	V3 U5 U4 V1 U3 U1 T4 T3	I	LVTTLp	**Telecom Bus 1 Transmit Input Data:** This data is clocked into the POP-12 on the rising edge of TTBCLKINA. Bit 7 is the MSB and is transmitted first.
TTBCLKINA	R3	I	LVTTLp	**Telecom Bus 1 Transmit Input Clock:** All of the input signals for Telecom Bus 1 are clocked into the POP-12 on the rising edge of this clock. The clock frequency is 19.44 MHz ± 20ppm.
TTBJ0J1INA	T2	I	LVTTLd	**Telecom Bus 1 Transmit Input Slot Indication:** When the TTBSPEINA signal is high, TTBJ0J1INA indicates the position of the J1 byte(s) on Telecom Bus 1. When the TTBSPEINA signal is low, TTBJ0J1INA indicates the position of the J0 byte (**CPOST**=1) or A23 byte (**CPOST**=0). The J1 and J0/A23 pulses are required if the TX Pointer Tracking State Machine is bypassed. If it is not bypassed then only valid pointer bytes and either a J0 or A23 pulse are needed.
TTBSPEINA	R4	I	LVTTLd	**Telecom Bus 1 Transmit Input Synchronous Payload Envelope Signal:** This signal is high for the SPE bytes and is low for the TOH bytes on input Telecom Bus 1. If the TX PTSM is not bypassed, and only a J0/A23 pulse is present on TTBJ0J1INA, then this lead can be grounded.
TTBFAILINA(2) TTBFAILINA(1) TTBFAILINA(0)	W1 W2 V4	I	LVTTLp	**Telecom Bus 1 Transmit Input Failure Indications:** TTBFAILINA(2:0) are used to force the respective STS in Telecom Bus 1 to All 1s. The state of these leads are routed to their corresponding TTBFAILOUTx(y) leads according to the setting of the control bits in the TCC1-6 registers. e.g., If STS-1 #1 going into the POP-12 is routed to STS-1 #8 going out of the POP-12, then the TTBFAILINA(0) signal is routed to the TTBFAILOUTC(1) output.
TTBDATAINB(7) TTBDATAINB(6) TTBDATAINB(5) TTBDATAINB(4) TTBDATAINB(3) TTBDATAINB(2) TTBDATAINB(1) TTBDATAINB(0)	AF5 AC7 AD6 AE5 AF4 AC6 AE4 AF3	I	LVTTLp	**Telecom Bus 2 Transmit Input Data:** This data is clocked into the POP-12 on the rising edge of TTBCLKINB. Bit 7 is the MSB and is transmitted first.
TTBCLKINB	AD4	I	LVTTLp	**Telecom Bus 2 Transmit Input Clock:** All of the input signals for Telecom Bus 2 are clocked into the POP-12 on the rising edge of this clock. The clock frequency is 19.44 MHz ± 20ppm.

Lead Name	Lead No.	I/O	Type	Lead Description
TTBJ0J1INB	AB6	I	LVTTLd	**Telecom Bus 2 Transmit Input Slot Indication:** When the TTBSPEINB signal is high, TTBJ0J1INB indicates the position of the J1 byte(s) on Telecom Bus 2. When the TTBSPEINB signal is low, TTBJ0J1INB indicates the position of the J0 byte (**CPOST**=1) or A23 byte (**CPOST**=0). The J1 and J0/A23 pulses are required if the TX Pointer Tracking State Machine is bypassed. If it is not bypassed then only valid pointer bytes and either a J0 or A23 pulse are needed.
TTBSPEINB	AC5	I	LVTTLd	**Telecom Bus 2 Transmit Input Synchronous Payload Envelope Signal:** This signal is high for the SPE bytes and is low for the TOH bytes on input Telecom Bus 2. If the TX PTSM is not bypassed, and only a J0/A23 pulse is present on TTBJ0J1INB, then this lead can be grounded.
TTBFAILINB(2) TTBFAILINB(1) TTBFAILINB(0)	AC8 AF6 AD7	I	LVTTLp	**Telecom Bus 2 Transmit Input Failure Indications:** TTBFAILINB(2:0) are used to force the respective STS in Telecom Bus 1 to All 1s. The state of these leads are routed to their corresponding TTBFAILOUTx(y) leads according to the setting of the control bits in the TCC1-6 registers. e.g., If STS-1 #5 going into the POP-12 is routed to STS-1 #8 going out of the POP-12, then the TTBFAILINB(1) signal is routed to the TTBFAILOUTC(1) output.
TTBDATAINC(7) TTBDATAINC(6) TTBDATAINC(5) TTBDATAINC(4) TTBDATAINC(3) TTBDATAINC(2) TTBDATAINC(1) TTBDATAINC(0)	AF15 AC14 AD14 AE14 AF14 AF13 AD13 AC13	I	LVTTLp	**Telecom Bus 3 Transmit Input Data:** This data is clocked into the POP-12 on the rising edge of TTBCLKINC. Bit 7 is the MSB and is transmitted first.
TTBCLKINC	AD12	I	LVTTLp	**Telecom Bus 3 Transmit Input Clock:** All of the input signals for Telecom Bus 3 are clocked into the POP-12 on the rising edge of this clock. The clock frequency is 19.44 MHz ± 20ppm.
TTBJ0J1INC	AF12	I	LVTTLd	**Telecom Bus 3 Transmit Input Slot Indication:** When the TTBSPEINC signal is high, TTBJ0J1INC indicates the position of the J1 byte(s) on Telecom Bus 3. When the TTBSPEINC signal is low, TTBJ0J1INC indicates the position of the J0 byte (**CPOST**=1) or A23 byte (**CPOST**=0). The J1 and J0/A23 pulses are required if the TX Pointer Tracking State Machine is bypassed. If it is not bypassed then only valid pointer bytes and either a J0 or A23 pulse are needed.

Lead Name	Lead No.	I/O	Type	Lead Description
TTBSPEINC	AE12	I	LVTTLd	**Telecom Bus 3 Transmit Input Synchronous Payload Envelope Signal:** This signal is high for the SPE bytes and is low for the TOH bytes on input Telecom Bus 3. If the TX PTSM is not bypassed, and only a J0/A23 pulse is present on TTBJ0J1INC, then this lead can be grounded.
TTBFAILINC(2) TTBFAILINC(1) TTBFAILINC(0)	AC15 AD15 AE15	I	LVTTLp	**Telecom Bus 3 Transmit Input Failure Indications:** TTBFAILINC(2:0) are used to force the respective STS in Telecom Bus 1 to All 1s. The state of these leads are routed to their corresponding TTBFAILOUTx(y) leads according to the setting of the control bits in the TCC1-6 registers. e.g., If STS-1 #1 going into the POP-12 is routed to STS-1 #8 going out of the POP-12, then the TTBFAILINA(0) signal is routed to the TTBFAILOUTC(1) output.
TTBDATAIND(7) TTBDATAIND(6) TTBDATAIND(5) TTBDATAIND(4) TTBDATAIND(3) TTBDATAIND(2) TTBDATAIND(1) TTBDATAIND(0)	AC20 AF22 AE21 AD20 AF21 AC19 AE20 AB18	I	LVTTLp	**Telecom Bus 4 Transmit Input Data:** This data is clocked into the POP-12 on the rising edge of TTBCLKIND. Bit 7 is the MSB and is transmitted first.
TTBCLKIND	AE19	I	LVTTLp	**Telecom Bus 4 Transmit Input Clock:** All of the input signals for Telecom Bus 4 are clocked into the POP-12 on the rising edge of this clock. The clock frequency is 19.44 MHz ± 20ppm.
TTBJ0J1IND	AD19	I	LVTTLd	**Telecom Bus 4 Transmit Input Slot Indication:** When the TTBSPEIND signal is high, TTBJ0J1IND indicates the position of the J1 byte(s) on Telecom Bus 4. When the TTBSPEIND signal is low, TTBJ0J1IND indicates the position of the J0 byte (**CPOST**=1) or A23 byte (**CPOST**=0). The J1 and J0/A23 pulses are required if the TX Pointer Tracking State Machine is bypassed. If it is not bypassed then only valid pointer bytes and either a J0 or A23 pulse are needed.
TTBSPEIND	AF20	I	LVTTLd	**Telecom Bus 4 Transmit Input Synchronous Payload Envelope Signal:** This signal is high for the SPE bytes and is low for the TOH bytes on input Telecom Bus 4. If the TX PTSM is not bypassed, and only a J0/A23 pulse is present on TTBJ0J1IND, then this lead can be grounded.

Lead Name	Lead No.	I/O	Type	Lead Description
TTBFAILIND(2) TTBFAILIND(1) TTBFAILIND(0)	AB25 AC26 AA23	I	LVTTLp	**Telecom Bus 4 Transmit Input Failure Indications:** TTBFAILIND(2:0) are used to force the respective STS in Telecom Bus 4 to All 1s. The state of these leads are routed to their corresponding TTBFAILOUTx(y) leads according to the setting of the control bits in the TCC1-6 registers. e.g., If STS-1 #1 going into the POP-12 is routed to STS-1 #8 going out of the POP-12, then the TTBFAILINA(0) signal is routed to the TTBFAILOUTC(1) output.
TTBDATAOUTA(7) TTBDATAOUTA(6) TTBDATAOUTA(5) TTBDATAOUTA(4) TTBDATAOUTA(3) TTBDATAOUTA(2) TTBDATAOUTA(1) TTBDATAOUTA(0)	R23 T26 T24 T23 U25 U24 V26 U23	O	LVTTL	**Telecom Bus 1 Transmit Output Data:** This data is clocked out of the POP-12 on the rising edge of TXCCLK. Bit 7 is the MSB and is transmitted first. The TOH bytes are outputs as 0s. The pointer bytes are always provided.
TTBCLKOUTA	R24	O	LVTTL	**Telecom Bus 1 Transmit Output Clock:** All of the output signals for Telecom Bus 1 are clocked out of the POP-12 on the rising edge of TXCCLK. The clock frequency is 19.44 MHz ± 20ppm and is derived directly from TXCCLK.
TTBJ0J1OUTA	R26	O	LVTTL	**Telecom Bus 1 Transmit Output Slot Indication:** When the TTBSPEOUTA signal is high, TTBJ0J1OUTA indicates the position of the J1 byte(s) on Telecom Bus 1. When the TTBSPEOUTA signal is low, TTBJ0J1OUTA indicates the position of the J0 byte.
TTBSPEOUTA	R25	O	LVTTL	**Telecom Bus 1 Transmit Output Synchronous Payload Envelope Signal:** This signal is high for the SPE bytes and is low for the TOH bytes on output Telecom Bus 1. Note that this signal dynamically adjusts when an output pointer adjustment occurs.
TTBFAILOUTA(2) TTBFAILOUTA(1) TTBFAILOUTA(0)	P26 P24 P25	O	LVTTL	**Telecom Bus 1 Transmit Output Failure Indications:** TTBFAILOUTA(2:0) follow their corresponding TTBFAILINx(y) leads according the routing set by the control bits in the TCC1-6 registers. e.g., If STS-1 #1 going into the POP-12 is routed to STS-1 #8 going out of the POP-12, then the TTBFAILOUTA(0) signal is routed to the TTBFAILOUTC(1) output. Also, these leads will be set to a 1 if the input PTSM is not bypassed and is generating Path AIS in its corresponding STS.

Lead Name	Lead No.	I/O	Type	Lead Description
TTBDATAOUTB(7) TTBDATAOUTB(6) TTBDATAOUTB(5) TTBDATAOUTB(4) TTBDATAOUTB(3) TTBDATAOUTB(2) TTBDATAOUTB(1) TTBDATAOUTB(0)	G25 H24 G26 H25 J24 H26 K22 J25	O	LVTTL	**Telecom Bus 2 Transmit Output Data:** This data is clocked out of the POP-12 on the rising edge of TXCCLK. Bit 7 is the MSB and is transmitted first. The TOH bytes are outputs as 0s. The pointer bytes are always provided.
TTBCLKOUTB	H23	O	LVTTL	**Telecom Bus 2 Transmit Output Clock:** All of the output signals for Telecom Bus 2 are clocked out of the POP-12 on the rising edge of TXCCLK. The clock frequency is 19.44 MHz ± 20ppm and is derived directly from TXCCLK.
TTBJ0J1OUTB	F25	O	LVTTL	**Telecom Bus 2 Transmit Output Slot Indication:** When the TTBSPEOUTB signal is high, TTBJ0J1OUTB indicates the position of the J1 byte(s) on Telecom Bus 2. When the TTBSPEOUTB signal is low, TTBJ0J1OUTB indicates the position of the J0 byte.
TTBSPEOUTB	F26	O	LVTTL	**Telecom Bus 2 Transmit Output Synchronous Payload Envelope Signal:** This signal is high for the SPE bytes and is low for the TOH bytes on output Telecom Bus 2. Note that this signal dynamically adjusts when an output pointer adjustment occurs.
TTBFAILOUTB(2) TTBFAILOUTB(1) TTBFAILOUTB(0)	E25 F24 F23	O	LVTTL	**Telecom Bus 2 Transmit Output Failure Indications:** TTBFAILOUTB(2:0) follow their corresponding TTBFAILINx(y) leads according to the routing set by the control bits in the TCC1-6 registers. e.g., If STS-1 #1 going into the POP-12 is routed to STS-1 #8 going out of the POP-12, then the TTBFAILOUTA(0) signal is routed to the TTBFAILOUTC(1) output. Also, these leads will be set to a 1 if the input PTSM is not bypassed and is generating Path AIS in its corresponding STS.
TTBDATAOUTC(7) TTBDATAOUTC(6) TTBDATAOUTC(5) TTBDATAOUTC(4) TTBDATAOUTC(3) TTBDATAOUTC(2) TTBDATAOUTC(1) TTBDATAOUTC(0)	A19 B19 A20 C19 E18 D19 A21 C20	O	LVTTL	**Telecom Bus 3 Transmit Output Data:** This data is clocked out of the POP-12 on the rising edge of TXCCLK. Bit 7 is the MSB and is transmitted first. The TOH bytes are outputs as 0s. The pointer bytes are always provided.
TTBCLKOUTC	C18	O	LVTTL	**Telecom Bus 3 Transmit Output Clock:** All of the output signals for Telecom Bus 3 are clocked out of the POP-12 on the rising edge of TXCCLK. The clock frequency is 19.44 MHz ± 20ppm and is derived directly from TXCCLK.

Lead Name	Lead No.	I/O	Type	Lead Description
TTBJ0J1OUTC	D17	O	LVTTL	**Telecom Bus 3 Transmit Output Slot Indication:** When the TTBSPEOUTC signal is high, TTBJ0J1OUTC indicates the position of the J1 byte(s) on Telecom Bus 3. When the TTBSPEOUTC signal is low, TTBJ0J1OUTC indicates the position of the J0 byte.
TTBSPEOUTC	E17	O	LVTTL	**Telecom Bus 3 Transmit Output Synchronous Payload Envelope Signal:** This signal is high for the SPE bytes and is low for the TOH bytes on output Telecom Bus 3. Note that this signal dynamically adjusts when an output pointer adjustment occurs.
TTBFAILOUTC(2) TTBFAILOUTC(1) TTBFAILOUTC(0)	A17 B17 A18	O	LVTTL	**Telecom Bus 3 Transmit Output Failure Indications:** TTBFAILOUTC(2:0) follow their corresponding TTBFAILINx(y) leads according to the routing set by the control bits in the TCC1-6 registers. e.g., If STS-1 #1 going into the POP-12 is routed to STS-1 #8 going out of the POP-12, then the TTBFAILOUTA(0) signal is routed to the TTBFAILOUTC(1) output. Also, these leads will be set to a 1 if the input PTSM is not bypassed and is generating Path AIS in its corresponding STS.
TTBDATAOUTD(7) TTBDATAOUTD(6) TTBDATAOUTD(5) TTBDATAOUTD(4) TTBDATAOUTD(3) TTBDATAOUTD(2) TTBDATAOUTD(1) TTBDATAOUTD(0)	B10 A10 D11 B11 A11 D12 B12 A12	O	LVTTL	**Telecom Bus 4 Transmit Output Data:** This data is clocked out of the POP-12 on the rising edge of TXCCLK. Bit 7 is the MSB and is transmitted first. The TOH bytes are outputs as 0s. The pointer bytes are always provided.
TTBCLKOUTD	C10	O	LVTTL	**Telecom Bus 4 Transmit Output Clock:** All of the output signals for Telecom Bus 2 are clocked out of the POP-12 on the rising edge of TXCCLK. The clock frequency is 19.44 MHz ± 20ppm and is derived directly from TXCCLK.
TTBJ0J1OUTD	A8	O	LVTTL	**Telecom Bus 4 Transmit Output Slot Indication:** When the TTBSPEOUTD signal is high, TTBJ0J1OUTD indicates the position of the J1 byte(s) on Telecom Bus 3. When the TTBSPEOUTD signal is low, TTBJ0J1OUTD indicates the position of the J0 byte.
TTBSPEOUTD	D10	O	LVTTL	**Telecom Bus 4 Transmit Output Synchronous Payload Envelope Signal:** This signal is high for the SPE bytes and is low for the TOH bytes on output Telecom Bus 4. Note that this signal dynamically adjusts when an output pointer adjustment occurs.

Lead Name	Lead No.	I/O	Type	Lead Description
TTBFAILOUTD(2) TTBFAILOUTD(1) TTBFAILOUTD(0)	D9 C9 E10	O	LVTTL	**Telecom Bus 4 Transmit Output Failure Indications:** TTBFAILOUTD(2:0) follow their corresponding TTBFAILINx(y) leads according to the routing set by the control bits in the TCC1-6 registers. e.g., If STS-1 #1 going into the POP-12 is routed to STS-1 #8 going out of the POP-12, then the TTBFAILOUTA(0) signal is routed to the TTBFAILOUTC(1) output. Also, these leads will be set to a 1 if the input PTSM is not bypassed and is generating Path AIS in its corresponding STS.
RXCCLK	D2	I	LVTTLp	**Receive Reference Clock:** RXCCLK is provided as a receive reference timebase for devices connected to the receive Telecom Bus interface. RXCCLK is configured to be 19.44 MHz ± 20ppm. The RX Telecom Bus inputs are retimed to this clock. All Telecom Bus 1-4 receive output signals are clocked out of the POP-12 on the rising edge of this clock
RXCFRM	F4	I	LVTTLd	**Receive Reference Frame Pulse:** RXCFRM along with RXCCLK can be used to synchronize the data that is input to the RX Telecom Bus ports to a common frame reference. If this lead is not used it must be grounded, in which case the output RX Telecom Bus signals will be aligned to an internally generated frame reference.
RXMF1 RXMF2 RXMF3 RXMF4	D1 E3 E1 E2	O	LVTTL	**Multiframe Reference Outputs:** These four signals are identical and provide a one RXCCLK clock cycle wide pulse every 500 microseconds. They are clocked out of the POP-12 device on the falling edge of the RXCCLK signal. These signals provide a four frame multi-frame reference for downstream mapper devices that may require such a reference and use the same clock for transmitting as is applied to the RXCCLK input.
RTBDATAOUTA(7) RTBDATAOUTA(6) RTBDATAOUTA(5) RTBDATAOUTA(4) RTBDATAOUTA(3) RTBDATAOUTA(2) RTBDATAOUTA(1) RTBDATAOUTA(0)	AC1 AB3 AB2 AA3 Y4 AA2 Y3 AA1	O	LVTTL	**Telecom Bus 1 Receive Output Data:** Bit 7 is the MSB and is received first. Bit 0 is the LSB and is received last. The data on these leads are clocked out of the POP-12 on the rising edge of RXCCLK. The TOH bytes are output as 0s, but the pointer bytes are always provided.
RTBCLKOUTA	Y1	O	LVTTL	**Telecom Bus 1 Receive Output Clock:** All Telecom Bus 1 receive output signals are clocked out of the POP-12 on the rising edge of RXCCLK. This clock is directly derived from RXCCLK.

Lead Name	Lead No.	I/O	Type	Lead Description
RTBJ0J1OUTA	Y2	O	LVTTL	**Telecom Bus 1 Receive Output J0J1 Signal:** This signal identifies the J0 byte position in the RTBDATAOUTA(7**:**0) stream when RTBJ0J1OUTA is high and RTBSPEOUTA is low. The J1 byte(s) are identified when RTBJ0J1OUTA is high and RTBSPEOUTA is high.
RTBSPEOUTA	V5	O	LVTTL	**Telecom Bus 1 Receive Output SPE Signal:** RTBSPEOUTA is high during the SPE bytes of RTBDATAOUTA(7:0) and is low otherwise. Note that this signal dynamically adjusts when a pointer adjustment is output.
RTBFAILOUTA(2) RTBFAILOUTA(1) RTBFAILOUTA(0)	AA5 AD1 AC2	O	LVTTL	**Telecom Bus 1 Receive Output Failure Indications:** These signals go high when the POP-12 detects Loss of Pointer or Path AIS when the PTSM is not bypassed. RTBFAILOUTA(n) will stay active as long as the failure condition exists in its corresponding STS. This lead also follows the state of its corresponding RTBFAILINx(y) input as set by the control bits in the RCC1-6 registers.
RTBDATAOUTB(7) RTBDATAOUTB(6) RTBDATAOUTB(5) RTBDATAOUTB(4) RTBDATAOUTB(3) RTBDATAOUTB(2) RTBDATAOUTB(1) RTBDATAOUTB(0)	AE10 AC11 AC10 AF9 AE9 AD9 AC9 AE8	O	LVTTL	**Telecom Bus 2 Receive Output Data:** Bit 7 is the MSB and is received first. Bit 0 is the LSB and is received last. The data on these leads are clocked out of the POP-12 on the falling rising edge of RXCCLK. The TOH bytes are output as 0s, but the pointer bytes are always provided.
RTBCLKOUTB	AE7	O	LVTTL	**Telecom Bus 2 Receive Output Clock:** All Telecom Bus 2 receive output signals are clocked out of the POP-12 on the rising edge of RXCCLK. This clock is directly derived from RXCCLK.
RTBJ0J1OUTB	AF7	O	LVTTL	**Telecom Bus 2 Receive Output J0J1 Signal:** This signal identifies the J0 byte position in the RTBDATAOUTB(7:0) stream when RTBJ0J1OUTB is high and RTBSPEOUTB is low. The J1 byte(s) are identified when RTBJ0J1OUTB is high and RTBSPEOUTB is high.
RTBSPEOUTB	AD8	O	LVTTL	**Telecom Bus 2 Receive Output SPE Signal:** RTBSPEOUTB is high during the SPE bytes of RTBDATAOUTB(7:0) and is low otherwise. Note that this signal dynamically adjusts when a pointer adjustment is output.
RTBFAILOUTB(2) RTBFAILOUTB(1) RTBFAILOUTB(0)	AC12 AE11 AD11	O	LVTTL	**Telecom Bus 2 Receive Output Failure Indications:** These signals go high when the POP-12 detects Loss of Pointer or Path AIS when the PTSM is not bypassed. RTBFAILOUTB(n) will stay active as long as the failure condition exists in its corresponding STS. This lead also follows the state of its corresponding RTBFAILINx(y) input as set by the control bits in the RCC1-6 registers.

Lead Name	Lead No.	I/O	Type	Lead Description
RTBDATAOUTC(7) RTBDATAOUTC(6) RTBDATAOUTC(5) RTBDATAOUTC(4) RTBDATAOUTC(3) RTBDATAOUTC(2) RTBDATAOUTC(1) RTBDATAOUTC(0)	AE18 AB17 AC17 AF18 AD17 AE17 AF17 AC16	O	LVTTL	**Telecom Bus 3 Receive Output Data:** Bit 7 is the MSB and is received first. Bit 0 is the LSB and is received last. The data on these leads are clocked out of the POP-12 on the rising edge of RXCCLK. The TOH bytes are output as 0s, but the pointer bytes are always provided.
RTBCLKOUTC	AF16	O	LVTTL	**Telecom Bus 3 Receive Output Clock:** All Telecom Bus 3 receive output signals are clocked out of the POP-12 on the rising edge of RXCCLK. This clock is directly derived from RXCCLK.
RTBJ0J1OUTC	AD16	O	LVTTL	**Telecom Bus 3 Receive Output J0J1 Signal:** This signal identifies the J0 byte position in the RTBDATAOUTC(7:0) stream when RTBJ0J1OUTC is high and RTBSPEOUTC is low. The J1 byte(s) are identified when RTBJ0J1OUTC is high and RTBSPEOUTC is high.
RTBSPEOUTC	AE16	O	LVTTL	**Telecom Bus 3 Receive Output SPE Signal:** RTBSPEOUTC is high during the SPE bytes of RTBDATAOUTC(7:0) and is low otherwise. Note that this signal dynamically adjusts when a pointer adjustment is output.
RTBFAILOUTC(2) RTBFAILOUTC(1) RTBFAILOUTC(0)	AC18 AF19 AD18	O	LVTTL	**Telecom Bus 3 Receive Output Failure Indications:** These signals go high when the POP-12 detects Loss of Pointer or Path AIS when the PTSM is not bypassed. RTBFAILOUTC(n) will stay active as long as the failure condition exists in its corresponding STS. This lead also follows the state of its corresponding RTBFAILINx(y) input as set by the control bits in the RCC1-6 registers.
RTBDATAOUTD(7) RTBDATAOUTD(6) RTBDATAOUTD(5) RTBDATAOUTD(4) RTBDATAOUTD(3) RTBDATAOUTD(2) RTBDATAOUTD(1) RTBDATAOUTD(0)	V23 W26 W25 W24 V22 W23 AA26 Y24	O	LVTTL	**Telecom Bus 4 Receive Output Data:** Bit 7 is the MSB and is received first. Bit 0 is the LSB and is received last. The data on these leads are clocked out of the POP-12 on the rising edge of RXCCLK. The TOH bytes are output as 0s, but the pointer bytes are always provided.
RTBCLKOUTD	AA24	O	LVTTL	**Telecom Bus 4 Receive Output Clock:** All Telecom Bus 4 receive output signals are clocked out of the POP-12 on the rising edge of RXCCLK. This clock is directly derived from RXCCLK.
RTBJ0J1OUTD	AB26	O	LVTTL	**Telecom Bus 4 Receive Output J0J1 Signal:** This signal identifies the J0 byte position in the RTBDATAOUTD(7:0) stream when RTBJ0J1OUTD is high and RTBSPEOUTD is low. The J1 byte(s) are identified when RTBJ0J1OUTD is high and RTBSPEOUTD is high.

Lead Name	Lead No.	I/O	Type	Lead Description
RTBSPEOUTD	Y23	O	LVTTL	**Telecom Bus 4 Receive Output SPE Signal:** RTBSPEOUTD is high during the SPE bytes of RTBDATAOUTD(7:0) and is low otherwise. Note that this signal dynamically adjusts when a pointer adjustment is output.
RTBFAILOUTD(2) RTBFAILOUTD(1) RTBFAILOUTD(0)	V25 U22 V24	O	LVTTL	**Telecom Bus 4 Receive Output Failure Indications:** These signals go high when the POP-12 detects Loss of Pointer or Path AIS when the PTSM is not bypassed. RTBFAILOUTD(n) will stay active as long as the failure condition exists in its corresponding STS. This lead also follows the state of its corresponding RTBFAILINx(y) input as set by the control bits in the RCC1-6 registers.
RTBDATAINA(7) RTBDATAINA(6) RTBDATAINA(5) RTBDATAINA(4) RTBDATAINA(3) RTBDATAINA(2) RTBDATAINA(1) RTBDATAINA(0)	L26 M23 M25 M26 N23 N24 N25 N26	I	LVTTLp	**Telecom Bus 1 Receive Input Data:** Bit 7 is the MSB and is received first. Bit 0 is the LSB and is received last. The data on these leads are clocked into the POP-12 on the rising edge of RTBCLKINA. When **RB1**=0, valid pointer bytes are required to be present in the data stream. Otherwise if **RB1**=1, the J0J1 signal provides the location of the J1 bytes and the pointer bytes do not need to be present in the data stream.
RTBCLKINA	L25	I	LVTTLp	**Telecom Bus 1 Receive Input Clock:** All Telecom Bus 1 receive input signals are clocked into the POP-12 on the rising edge of RTBCLKINA. This clock is 19.44MHz ± 20ppm.
RTBJ0J1INA	L23	I	LVTTLd	**Telecom Bus 1 Receive Input J0J1 Signal:** This signal identifies the J0 byte position in the RTBDATAINA(7**:**0) stream when RTBJ0J1INA is high and RTBSPEINA is low and **CPOSR**=1. When **CPOSR**=0 this signal identifies the A23 byte position in the RTBDATAINA(7:0) stream when RTBJ0J1INA is high and RTBSPEINA is low. The J1 byte(s) are identified when RTBJ0J1INA is high and RTBSPEINA is high. When **RB1**=0, the J1 pulses are ignored. When **RB1**=1, the J0J1 pulses are required.
RTBSPEINA	L24	I	LVTTLd	**Telecom Bus 1 Receive Input SPE Signal:** RTBSPEINA is high during the SPE bytes of RTBDATAINA(7:0) and is low otherwise. Note that this signal needs to be dynamically adjusted when a pointer adjustment is input.
RTBFAILINA(2) RTBFAILINA(1) RTBFAILINA(0)	K26 K24 J26	I	LVTTLp	**Telecom Bus 1 Receive Input Failure Indications:** RTBFAILINA(2:0) are used to force the respective STS in RX Telecom Bus 1 to All 1s. The state of these leads are routed to their corresponding RTBFAILOUTx(y) leads according to the setting of the control bits in the RCC1-6 registers. e.g., If STS-1 #1 going into the POP-12 is routed to STS-1 #8 going out of the POP-12, then the RTBFAILINA(0) signal is routed to the RTBFAILOUTC(1) output.

Lead Name	Lead No.	I/O	Type	Lead Description
RTBDATAINB(7) RTBDATAINB(6) RTBDATAINB(5) RTBDATAINB(4) RTBDATAINB(3) RTBDATAINB(2) RTBDATAINB(1) RTBDATAINB(0)	E21 C22 D22 A24 C26 E24 D26 E26	I	LVTTLp	**Telecom Bus 2 Receive Input Data:** Bit 7 is the MSB and is received first. Bit 0 is the LSB and is received last. The data on these leads are clocked into the POP-12 on the rising edge of RTBCLKINB. When **RB2**=0, valid pointer bytes are required to be present in the data stream. Otherwise if **RB2**=1, the J0J1 signal provides the location of the J1 bytes and the pointer bytes do not need to be present in the data stream.
RTBCLKINB	B23	I	LVTTLp	**Telecom Bus 2 Receive Input Clock:** All Telecom Bus 2 receive input signals are clocked into the POP-12 on the rising edge of RTBCLKINB. This clock is 19.44MHz ± 20ppm.
RTBJ0J1INB	D21	I	LVTTLd	**Telecom Bus 2 Receive Input J0J1 Signal:** This signal identifies the J0 byte position in the RTBDATAINB(7:0) stream when RTBJ0J1INB is high and RTBSPEINB is low and **CPOSR**=1. When **CPOSR**=0 this signal identifies the A23 byte position in the RTBDATAINB(7:0) stream when RTBJ0J1INB is high and RTBSPEINB is low. The J1 byte(s) are identified when RTBJ0J1INB is high and RTBSPEINB is high. When **RB2**=0, the J1 pulses are ignored. When **RB2**=1, the J0J1 pulses are required.
RTBSPEINB	A23	I	LVTTLd	**Telecom Bus 2 Receive Input SPE Signal:** RTBSPEINB is high during the SPE bytes of RTBDATAINB(7:0) and is low otherwise. Note that this signal needs to be dynamically adjusted when a pointer adjustment is input.
RTBFAILINB(2) RTBFAILINB(1) RTBFAILINB(0)	C21 D20 B22	I	LVTTLp	**Telecom Bus 2 Receive Input Failure Indications:** RTBFAILINB(2:0) are used to force the respective STS in RX Telecom Bus 1 to All 1s. The state of these leads are routed to their corresponding RTBFAILOUTx(y) leads according to the setting of the control bits in the RCC1-6 registers. e.g., If STS-1 #1 going into the POP-12 is routed to STS-1 #8 going out of the POP-12, then the RTBFAILINA(0) signal is routed to the RTBFAILOUTC(1) output.
RTBDATAINC(7) RTBDATAINC(6) RTBDATAINC(5) RTBDATAINC(4) RTBDATAINC(3) RTBDATAINC(2) RTBDATAINC(1) RTBDATAINC(0)	D14 A15 B15 C15 D15 A16 C16 D16	I	LVTTLp	**Telecom Bus 3 Receive Input Data:** Bit 7 is the MSB and is received first. Bit 0 is the LSB and is received last. The data on these leads are clocked into the POP-12 on the rising edge of RTBCLKINC. When **RB3**=0, valid pointer bytes are required to be present in the data stream. Otherwise if **RB3**=1, the J0J1 signal provides the location of the J1 bytes and the pointer bytes do not need to be present in the data stream.

Lead Name	Lead No.	I/O	Type	Lead Description
RTBCLKINC	C14	I	LVTTLp	**Telecom Bus 3 Receive Input Clock:** All Telecom Bus 3 receive input signals are clocked into the POP-12 on the rising edge of RTBCLKINC. This clock is 19.44MHz ± 20ppm.
RTBJ0J1INC	A13	I	LVTTLd	**Telecom Bus 3 Receive Input J0J1 Signal:** This signal identifies the J0 byte position in the RTBDATAINC(7:0) stream when RTBJ0J1INC is high and RTBSPEINC is low and **CPOSR**=1. When **CPOSR**=0 this signal identifies the A23 byte position in the RTBDATAINC(7:0) stream when RTBJ0J1INC is high and RTBSPEINC is low. The J1 byte(s) are identified when RTBJ0J1INC is high and RTBSPEINC is high. When **RB3**=0, the J1 pulses are ignored. When **RB3**=1, the J0J1 pulses are required.
RTBSPEINC	A14	I	LVTTLd	**Telecom Bus 3 Receive Input SPE Signal:** RTBSPEINC is high during the SPE bytes of RTBDATAINC(7:0) and is low otherwise. Note that this signal needs to be dynamically adjusted when a pointer adjustment is input.
RTBFAILINC(2) RTBFAILINC(1) RTBFAILINC(0)	D13 C13 B13	I	LVTTLp	**Telecom Bus 3 Receive Input Failure Indications:** RTBFAILINC(2:0) are used to force the respective STS in RX Telecom Bus 1 to All 1s. The state of these leads are routed to their corresponding RTBFAILOUTx(y) leads according to the setting of the control bits in the RCC1-6 registers. e.g., If STS-1 #1 going into the POP-12 is routed to STS-1 #8 going out of the POP-12, then the RTBFAILINA(0) signal is routed to the RTBFAILOUTC(1) output.
RTBDATAIND(7) RTBDATAIND(6) RTBDATAIND(5) RTBDATAIND(4) RTBDATAIND(3) RTBDATAIND(2) RTBDATAIND(1) RTBDATAIND(0)	A6 B6 E6 C7 D8 C8 A7 B8	I	LVTTLp	**Telecom Bus 4 Receive Input Data:** Bit 7 is the MSB and is received first. Bit 0 is the LSB and is received last. The data on these leads are clocked into the POP-12 on the rising edge of RTBCLKIND. When **RB4**=0, valid pointer bytes are required to be present in the data stream. Otherwise if **RB4**=1, the J0J1 signal provides the location of the J1 bytes and the pointer bytes do not need to be present in the data stream.
RTBCLKIND	C6	I	LVTTLp	**Telecom Bus 4 Receive Input Clock:** All Telecom Bus 1 receive input signals are clocked into the POP-12 on the rising edge of RTBCLKIND. This clock is 19.44MHz ± 20ppm.

Lead Name	Lead No.	I/O	Type	Lead Description
RTBJ0J1IND	A5	I	LVTTLd	**Telecom Bus 4 Receive Input J0J1 Signal:** This signal identifies the J0 byte position in the RTBDATAIND(7:0) stream when RTBJ0J1IND is high and RTBSPEIND is low and **CPOSR**=1. When **CPOSR**=0 this signal identifies the A23 byte position in the RTBDATAIND(7:0) stream when RTBJ0J1IND is high and RTBSPEIND is low. The J1 byte(s) are identified when RTBJ0J1IND is high and RTBSPEIND is high. When **RB4**=0, the J1 pulses are ignored. When **RB4**=1, the J0J1 pulses are required.
RTBSPEIND	B5	I	LVTTLd	**Telecom Bus 1 Receive Input SPE Signal:** RTBSPEIND is high during the SPE bytes of RTBDATAIND(7:0) and is low otherwise. Note that this signal needs to be dynamically adjusted when a pointer adjustment is input.
RTBFAILIND(2) RTBFAILIND(1) RTBFAILIND(0)	C4 C5 D6	I	LVTTLp	**Telecom Bus 1 Receive Input Failure Indications:** RTBFAILIND(2:0) are used to force the respective STS in RX Telecom Bus 1 to All 1s. The state of these leads are routed to their corresponding RTBFAILOUTx(y) leads according to the setting of the control bits in the RCC1-6 registers. e.g., If STS-1 #1 going into the POP-12 is routed to STS-1 #8 going out of the POP-12, then the RTBFAILINA(0) signal is routed to the RTBFAILOUTC(1) output.

MICROPROCESSOR INTERFACE LEADS

Lead Name	Lead No.	I/O	Type	Lead Description
PCLK	P1	I	LVTTLp	**Microprocessor Interface Clock:** Clock for the microprocessor interface in the POP-12 device. This clock is always required to operate the µP interface. The frequency range for this clock is 8 MHz to 20 MHz.
DATAIO(7) DATAIO(6) DATAIO(5) DATAIO(4) DATAIO(3) DATAIO(2) DATAIO(1) DATAIO(0)	H2 G1 H3 J5 H4 F1 G3 F5	I/O	LVTTL	**Microprocessor Interface Data:** (true) Bidirectional bus for data to/from the POP-12 µP interface. Bit (0) is the LSB.
LA(4) LA(3) LA(2) LA(1) LA(0)	J1 K4 K5 J3 J4	I	LVTTLp	**Microprocessor Interface Address:** The 5-bit address that is used to access the address and data registers. Bit (0) is the LSB.
$\overline{\text{WRITE}}$/READ_$\overline{\text{WRITE}}$	N1	I	LVTTLp	**Microprocessor Write:** This signal is high during a data read operation and is low for a data write operation. A low enables data from the DATAIO(7:0) bus to be written into the addressed location.
$\overline{\text{READ}}$	N3	I	LVTTLp	**Microprocessor Read:** For Intel mode, this signal is high during a data write operation and is low during a data read operation. A low enables data to be read from the addressed location. This lead must be tied high for Motorola Mode.
$\overline{\text{DS}}$	R1	I	LVTTLp	**Data Strobe:** Tie high for Intel mode. In Motorola mode, this lead is driven low to indicate that there is valid data on the DATAIO bus.
READY/$\overline{\text{DTACK}}$	M1	O	LVTTL	**Ready:** In Intel mode, this signal is asserted high to tell the external microprocessor that it can end the bus cycle. In Motorola mode, this lead is driven low, to tell the external microprocessor that it can end the bus cycle. ***This lead is not tristated.***
$\overline{\text{SELC}}$	P2	I	LVTTLp	**POP-12 Chip Select:** Enable signal used to validate the address bus for read and write transfers from/to this particular POP-12 device.
INT/$\overline{\text{IRQ}}$	N4	O	LVTTL	**Interrupt:** Interrupt to microprocessor. It is active high for Intel mode and active low for motorola mode.

Lead Name	Lead No.	I/O	Type	Lead Description
$\overline{\text{RESETUP}}$	K1	I	LVTTLp	**Device Reset:** Active low reset that must be applied at power up for at least 150ns after power and all clocks (except TCK) are stable. Also, WRITE/$\overline{\text{READ\_WRITE}}$ must be held high during the time that $\overline{\text{RESETUP}}$ is held low and for 10 ns after $\overline{\text{RESETUP}}$ is brought high.
MOTO	R2	I	LVTTLp	**Motorola Mode Select:** When set high the microprocessor interface is set to Motorola mode. When set low, the Microprocessor interface is set to Intel mode.

TEST AND MISCELLANEOUS LEADS

Lead Name	Lead No.	I/O	Type	Lead Description
TCK	M3	I	LVTTLp	**JTAG Port Clock:** Boundary scan input clock.
TMS	M4	I	LVTTLp	**JTAG Port TMS:** Boundary scan TMS input signal.
$\overline{\text{TRS}}$	L1	I	LVTTLp	**JTAG Port Reset:** Active low asynchronous reset for the boundary scan logic. Holding this lead low for at least 50ns will reset all of the boundary scan logic to disabled state, such that normal operation of the POP-12 is not affected in any way.
TDI	L4	I	LVTTLp	**JTAG Port Data Input:** Boundary scan input data.
TDO	L2	O	LVTTLp	**JTAG Port Data Output:** Boundary scan output data.
SCANMODE	K3	I	LVTTLp	**SCAN Mode Enable:** This lead must be tied low for normal operation. When set high or left floating, the manufacturing scan test is enabled.
SCANEN	K2	I	LVTTLp	**SCAN Enable:** This lead must be tied low for normal operation. When set high or left floating, the manufacturing scan test is enabled.
HIZ	G4	I	LVTTLp	**HI-Z TEST:** This lead must be tied low for normal operation. Setting this lead high puts all outputs in high impedance state, except lead TDO, and all bidirectional outputs in input mode.
TESTOUT	F3	O	- -	**Test Output:** Leave this lead unconnected.
TESTIN1 TESTIN2	P4 P3	I	- -	**Test Input:** Tie these leads to VDD.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply Voltage - digital I/O	VDD	-0.3	3.9	V	
Input Voltage (LVTTL)	V_{IN}	-0.3	VDD	V	
Storage Temperature	T_S	-40	125	^oC	
Ambient operating temperature range	T_A	-40	85	^oC	0 ft./min. linear air flow
Operating junction temperature range	T_J	-40	125	^oC	
Moisture Exposure level	ME	5		Level	Per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	absolute value 2		kV	Note 3

Notes:

1. Conditions exceeding the Min. or Max values may cause permanent failure. Exposure to conditions near the Min. or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the “CAUTION” label on the drypack bag in which devices are supplied.
3. Test Method for ESD per MIL-STD-883D, Method 3015.7.

THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Thermal Resistance - junction to ambient	θ_{JA}		20		$^oC/W$	Note 4

Note 4: Test done with package assembled on JEDEC standard Multi-Lager test board with 0 ft/min. linear airflow.

POWER REQUIREMENTS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD	3.14	3.30	3.46	V
Power Dissipation	P_{DD}			2.0	W

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

For I/Os that have internal pull up resistors, a logic 1 is guaranteed to be applied at the internal circuit if the corresponding lead is left open. However, this does not mean that a logic 1 will be present at that lead. If it is required to have a logic 1 at such a **floating lead**, then an external pull-up will need to be supplied. On-chip pull-up resistors are about 30-150 kΩ and on chip pull-down resistors are about 30-150 kΩ. This implies that pulling the voltage up or down on a floating lead requires hundreds of nanoseconds. Transitions will be slower with large capacitive loads.

Input Parameters for LVTTL (3.3 Volt compatible LVTTL input or LVTTL input/output when in input mode)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.00		VDD	V	VDD = 3.14V - 3.46V.
V_{IL}	0.00		0.80	V	VDD = 3.14V - 3.46V.
Input leakage current	-10		10	µA	
Input capacitance			10	pF	

Input Parameters for LVTTLp (3.3 Volt compatible LVTTL input with internal pull-up resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.10		VDD	V	VDD = 3.14V - 3.46V.
V_{IL}	0.00		0.80	V	VDD = 3.14V - 3.46V.
Input leakage current	-117		0	µA	
Input capacitance			10	pF	

Input Parameters for LVTTLd (3.3 Volt compatible LVTTL input with internal pull-down resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.00		VDD	V	VDD = 3.14V - 3.46V.
V_{IL}	0.00		0.80	V	VDD = 3.14V - 3.46V.
Input leakage current	0		117	µA	
Input capacitance			10	pF	

Output Parameters for LVTTL (3.3 Volt LVTTL output or LVTTL input/output when in output mode)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4		VDD	V	VDD = 3.14V - 3.46V.
V_{OL}	0.00		0.4	V	VDD = 3.14V - 3.46V.
I_{OL}		8		mA	V_{OL}= 0.4V, VDD = 3.14V, junction temperature = 125 ^{o}C
I_{OH}		8		mA	V_{OH}= 2.4V, VDD = 3.14V, junction temperature = 125^{o}C
Tristate leakage current	-10		-10	µA	Worst case
Output capacitance			10	pF	

TIMING CHARACTERISTICS

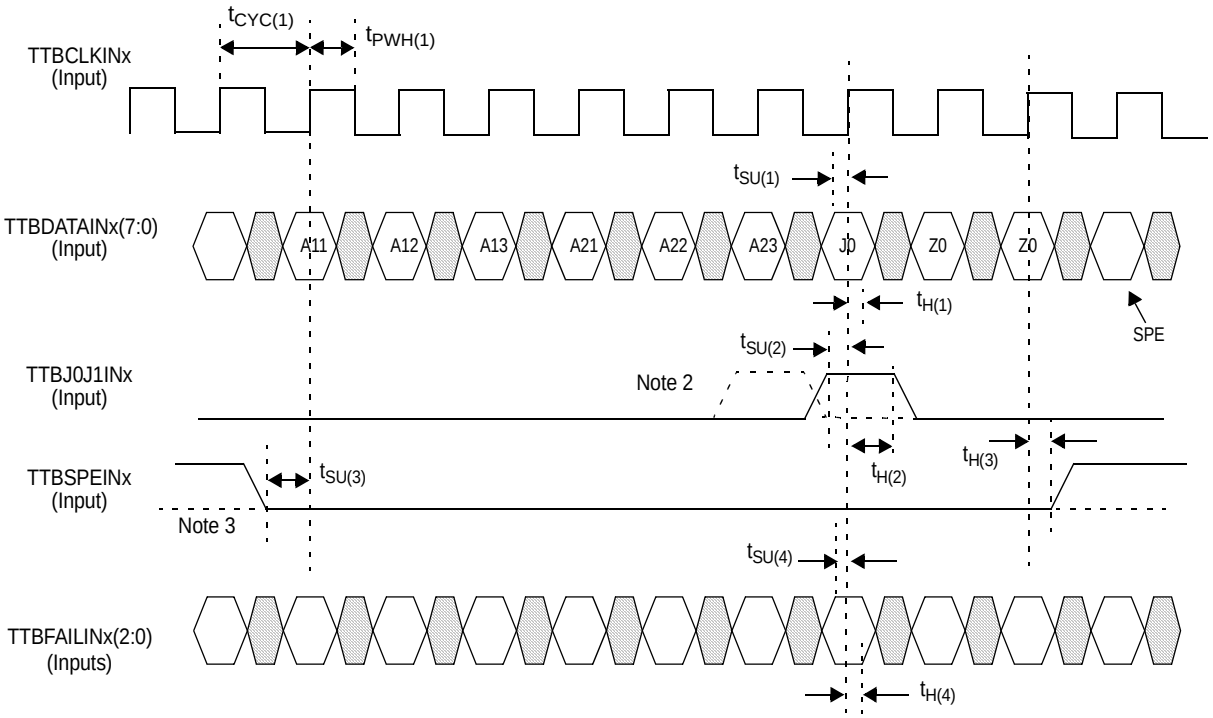
This section presents the detailed timing characteristics for the POP-12 in Figures 3 through 11. The load capacitances for the output times are indicated in each Figure as applicable. Unless otherwise indicated, timing parameters are measured at specific signal voltage levels:

1. TTL Inputs - 0.80V / 2.00V
2. TTL Outputs - 0.80V / 2.00V

The specifications given in this section cover the following environmental condition:

T_A = -40 ^oC to +85 ^oC, VDD = 3.3 V ± 5%

Figure 3. Transmit Telecom Bus (x = A,B,C,D) Input Timing



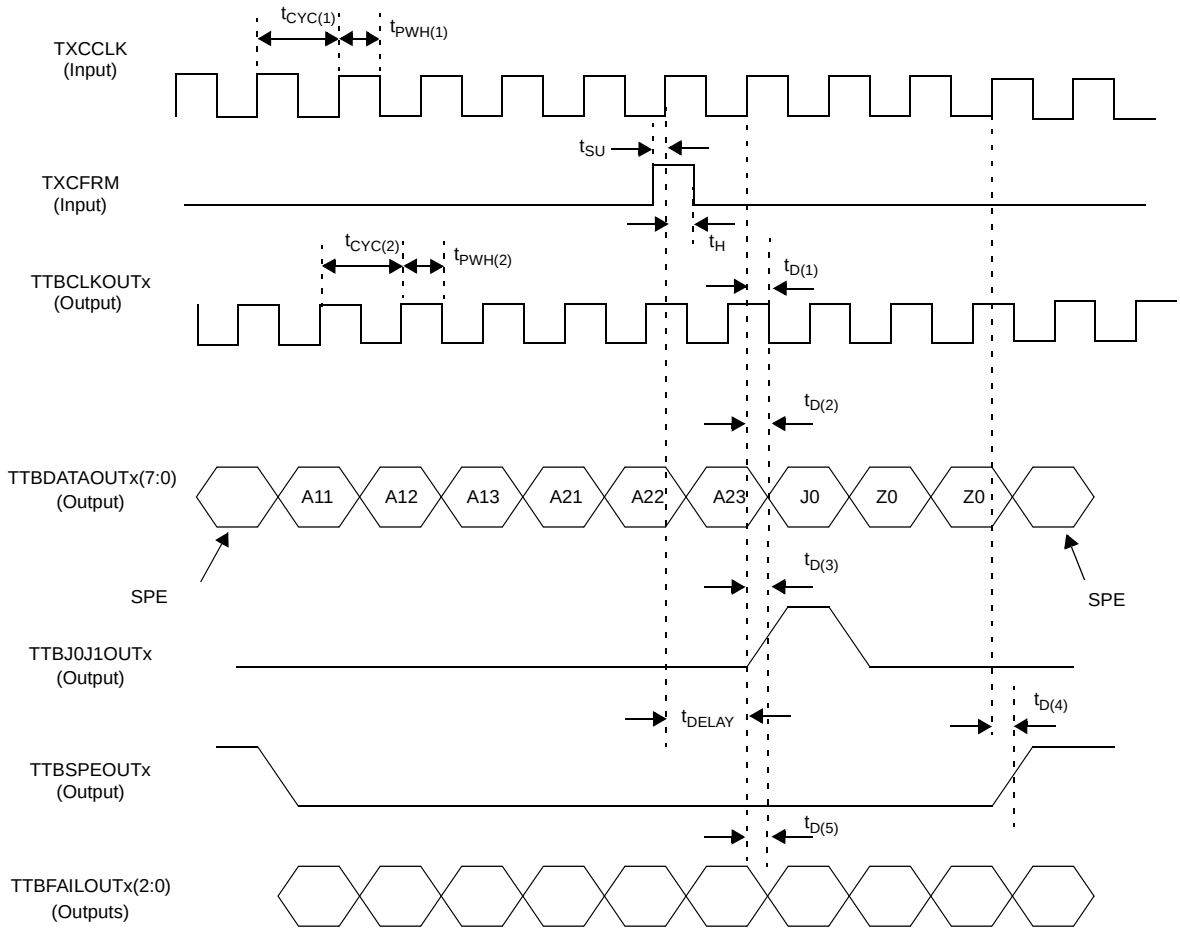
See parameter table on next page.

Parameter	Symbol	Min	Typ	Max	Unit
TTBCLKINx clock period	$t_{CYC(1)}$		51.44		ns
TTBCLKINx duty cycle	$t_{PWH(1)}/t_{CYC(1)}$	45		55	%
TTBDATAINx(7:0) set-up time to TTBCLKINx↑	$t_{SU(1)}$	7.0			ns
TTBDATAINx(7:0) hold time after TTBCLKINx↑	$t_{H(1)}$	7.0			ns
TTBJ0J1INx set-up time to TTBCLKINx↑	$t_{SU(2)}$	7.0			ns
TTBJ0J1INx hold time after TTBCLKINx↑	$t_{H(2)}$	7.0			ns
TTBSPEINx set-up time to TTBCLKINx↑	$t_{SU(3)}$	7.0			ns
TTBSPEINx hold time after TTBCLKINx↑	$t_{H(3)}$	7.0			ns
TTBFAILINx(2:0) set-up time to TTBCLKINx↑	$t_{SU(4)}$	7.0			ns
TTBFAILINx(2:0) hold time after TTBCLKINx↑	$t_{H(4)}$	7.0			ns

Notes:

1. The J1 pulse is not shown in the timing diagram but has the same timing parameters as the J0 pulse. If the corresponding **TBx** bit is set to a 1, the SPE signal and the J0 and J1 pulses are required but valid pointer bytes are not. If the corresponding **TBx** bit is set to a 0, only the J0 (or A23) pulse is required, as determined by the **CPOST** bit, the J1 pulse(s) are ignored; however valid pointer bytes are required.
2. When TTBSPEINx is low, the TTBJ0J1INx signal is used to identify either the A23 or J0 byte position as selected by the **CPOST** control bit.
3. When **TBx** is set to 0, the TTBSPEINx signal can be tied low (as shown by the dashed lines in the TTBSPEINx signal in Figure 3) if there is no J1 pulse in the TTBJ0J1INx signal. Otherwise, if there is a J1 pulse in the TTBJ0J1INx signal, then the TTBSPEINx signal needs to be high coincident with the J1 pulse(s), even though they would be ignored. In either case, the TTBSPEINx signal needs to be low coincident with the A23 or J0 pulse in the TTBJ0J1INx signal. When **TBx** is set to 1, then the TTBSPEINx signal must be 1 during the SPE byte times and 0 otherwise.

Figure 4. Transmit Telecom Bus (x = A,B,C,D) Output Timing



100 pF Load

See parameter table on next page.

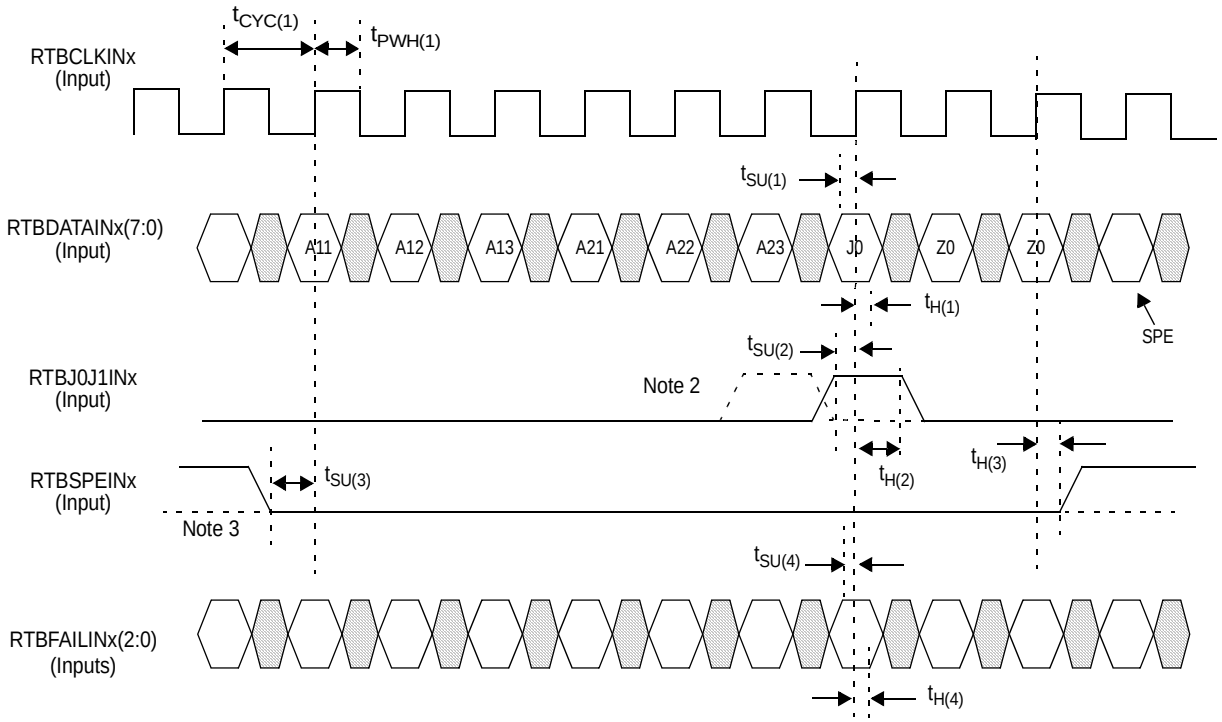
Parameter	Symbol	Min	Typ	Max	Unit
TXCCLK clock period	$t_{CYC(1)}$		51.44		ns
TXCCLK duty cycle	$t_{PWH(1)}/t_{CYC(1)}$	45		55	%
TTBCLKOUTx clock period	$t_{CYC(2)}$		51.44		ns
TTBCLKOUTx duty cycle	$t_{PWH(2)}/t_{CYC(2)}$	40		60	%
TXCFRM set-up time to TXCCLK↑	t_{SU}	7.0			ns
TXCFRM hold time after TXCCLK↑	t_H	7.0			ns
TTBCLKOUTx↓ delay from TXCCLK↑	$t_{D(1)}$	7.0		16	ns
TTBDATAOUTx(7:0) delay from TXCCLK↑	$t_{D(2)}$	7.0		22	ns
TTBJ0J1OUTx delay from TXCCLK↑	$t_{D(3)}$	7.0		22	ns
TTBSPEOUTx delay from TXCCLK↑	$t_{D(4)}$	7.0		22	ns
TTBFAILOUTx(2:0) delay from TXCCLK↑	$t_{D(5)}$	7.0		22	ns
Delay from TXCFRM high and TXCCLK↑ to J0 byte position clocked out on TXCCLK↑	t_{DELAY}		Note 4		TXCCLK Cycles
Transmit Telecom Bus interface output rise and fall times	t_r,t_f	3.8		4.1	ns

Notes:

1. The J1 pulse(s) is(are) not shown in the timing diagram but has(have) the same timing parameters as the J0 pulse.
2. $t_{D(n)(min)}$ represents the earliest time that the corresponding signal starts to change.
3. $t_{D(n)(max)}$ represents the latest time at which the corresponding signal becomes stable.
4. t_{DELAY} is determined by the settings of the **DELAYT** control bits as follows:

DELAYT	t_{DELAY}	Units
00	1	TXCCLK Cycles
01	4	TXCCLK Cycles
02	7	TXCCLK Cycles
03	10	TXCCLK Cycles
04	13	TXCCLK Cycles
05	16	TXCCLK Cycles
06	19	TXCCLK Cycles

Figure 5. Receive Telecom Bus (x = A,B,C,D) Input Timing



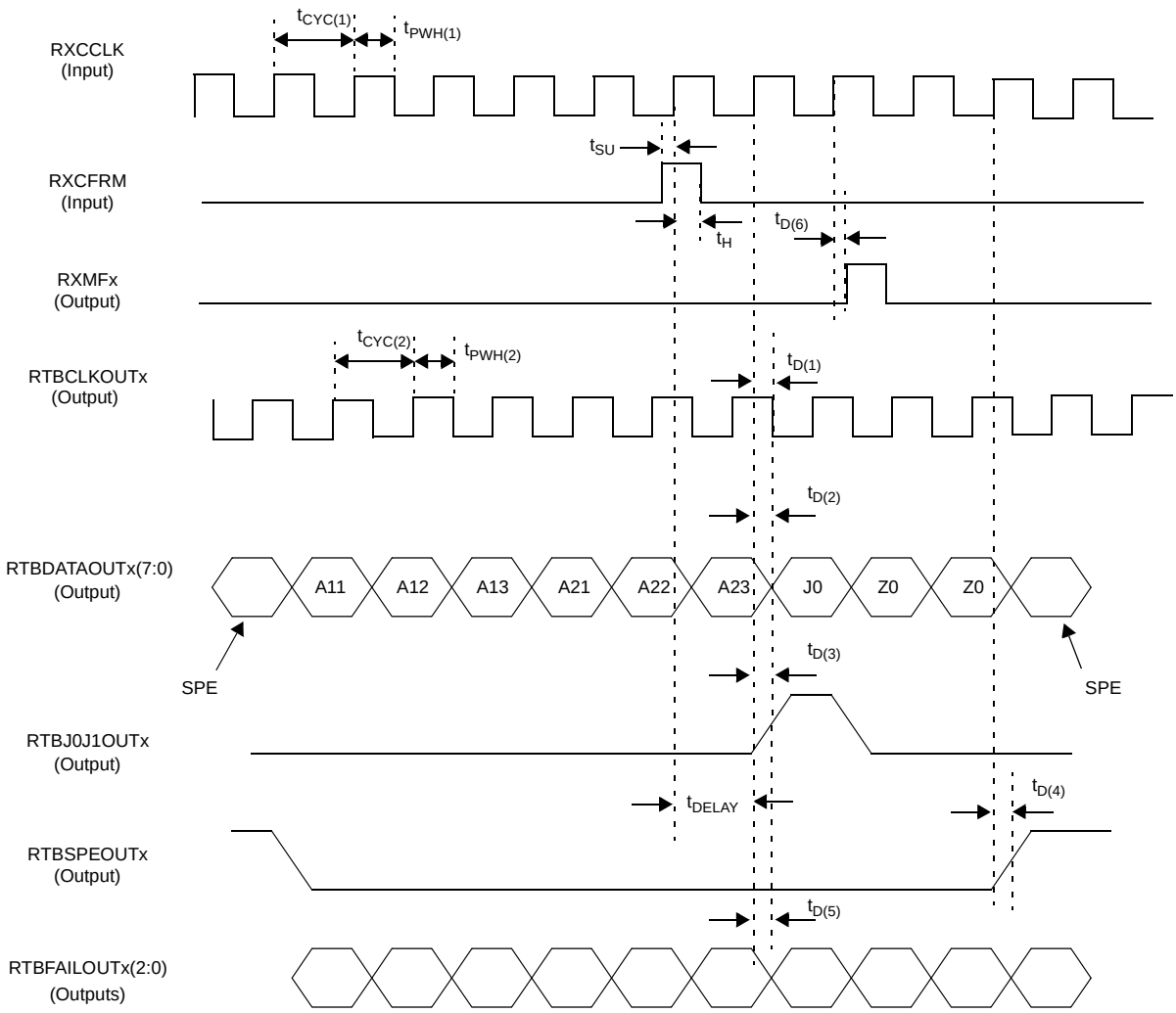
See parameter table on next page.

Parameter	Symbol	Min	Typ	Max	Unit
RTBCLKINx clock period	$t_{CYC(1)}$		51.44		ns
RTBCLKINx duty cycle	$t_{PWH(1)}/t_{CYC(1)}$	45		55	%
RTBDATAINx(7:0) set-up time to RTBCLKINx↑	$t_{SU(1)}$	7.0			ns
RTBDATAINx(7:0) hold time after RTBCLKINx↑	$t_{H(1)}$	7.0			ns
RTBJ0J1INx set-up time to RTBCLKINx↑	$t_{SU(2)}$	7.0			ns
RTBJ0J1INx hold time after RTBCLKINx↑	$t_{H(2)}$	7.0			ns
RTBSPEINx set-up time to RTBCLKINx↑	$t_{SU(3)}$	7.0			ns
RTBSPEINx hold time after RTBCLKINx↑	$t_{H(3)}$	7.0			ns
RTBFAILINx(2:0) set-up time to RTBCLKINx↑	$t_{SU(4)}$	7.0			ns
RTBFAILINx(2:0) hold time after RTBCLKINx↑	$t_{H(4)}$	7.0			ns

Notes:

1. The J1 pulse is not shown in the timing diagram but has the same timing parameters as the J0 pulse. If the corresponding **RBx** bit is set to a 1, the J0 and J1 pulses are required but valid pointer bytes are not. If the corresponding **RBx** bit is set to a 0, only the J0 (or A23) pulse is required, as determined by the **CPOSR** bit, but the J1 pulse(s) are ignored; however valid pointer bytes are required.
2. When RTBSPEINx is low, the RTBJ0J1INx signal is used to identify either the A23 or J0 byte position as selected by the **CPOSR** control bit.
3. When **RBx** is set to 0, the RTBSPEINx signal can be tied low (as shown by the dashed lines in the RTBSPEINx signal in Figure 3) if there is no J1 pulse in the RTBJ0J1INx signal. Otherwise, if there is a J1 pulse in the RTBJ0J1INx signal, then the RTBSPEINx signal needs to be high coincident with the J1 pulse(s), even though they would be ignored. In either case, the RTBSPEINx signal needs to be low coincident with the A23 or J0 pulse in the RTBJ0J1INx signal. When **RBx** is set to 1, then the RTBSPEINx signal must be 1 during the SPE byte times and 0 otherwise.

Figure 6. Receive Telecom Bus (x = A,B,C,D) Output Timing



100 pF Load

See parameter table on next page.

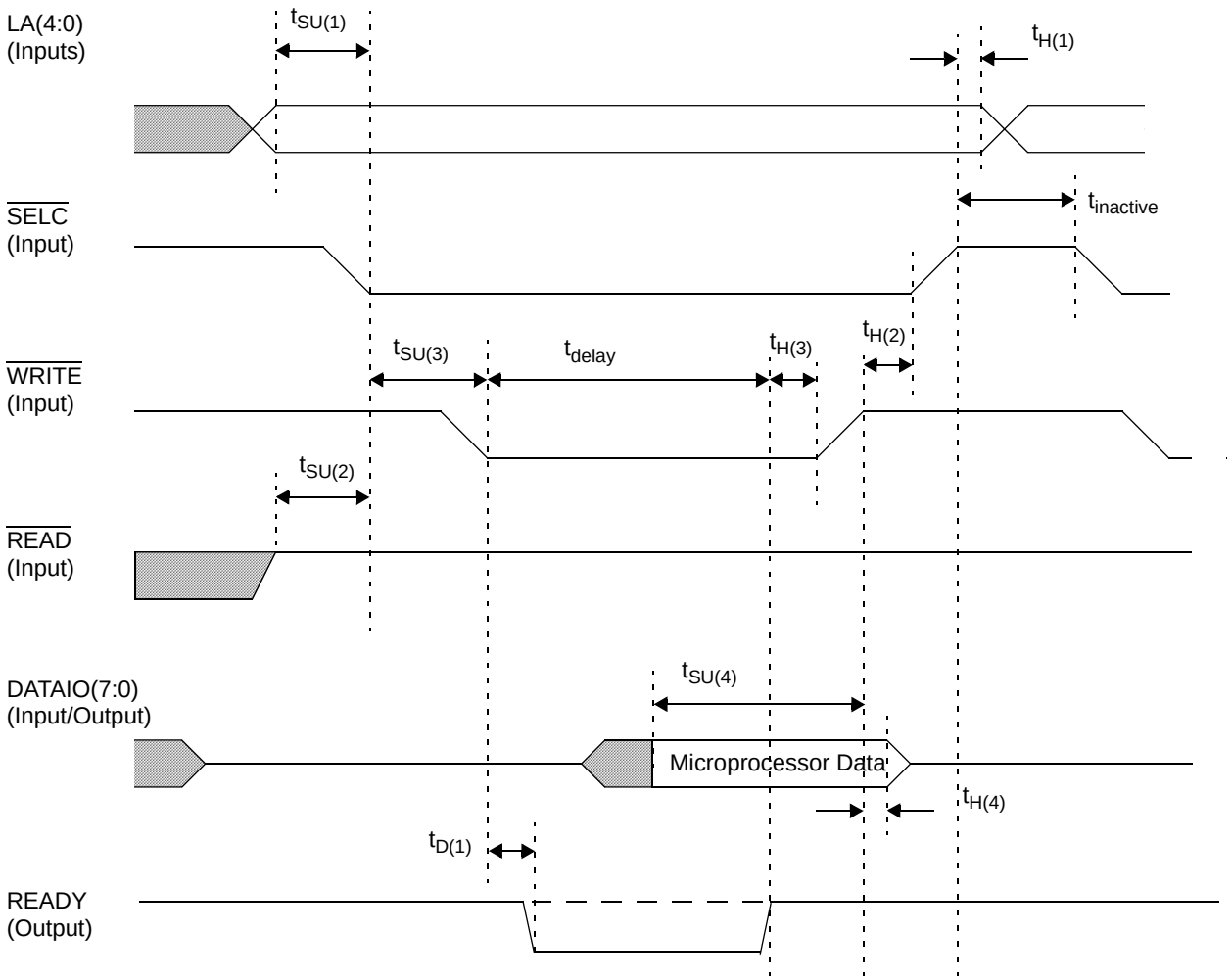
Parameter	Symbol	Min	Typ	Max	Unit
RXCCLK clock period	$t_{CYC(1)}$		51.44		ns
RXCCLK duty cycle	$t_{PWH(1)}$/ $t_{CYC(1)}$	45		55	%
RTBCLKOUTx clock period	$t_{CYC(2)}$		51.44		ns
RTBCLKOUTx duty cycle	$t_{PWH(2)}$/ $t_{CYC(2)}$	40		60	%
RXCFRM set-up time to RXCCLK↑	t_{SU}	7.0			ns
RXCFRM hold time after RXCCLK↑	t_H	7.0			ns
RTBCLKOUTx↓ delay from RXCCLK↑	$t_{D(1)}$	14		35	ns
RTBDATAOUTx(7:0) delay from RXCCLK↑	$t_{D(2)}$	7.0		22	ns
RTBJ0J1OUTx delay from RXCCLK↑	$t_{D(3)}$	7.0		22	ns
RTBSPEOUTx delay from RXCCLK↑	$t_{D(4)}$	7.0		22	ns
RTBFAILOUTx(2:0) delay from RXCCLK↑	$t_{D(5)}$	7.0		22	ns
RXMFx delay from RXCCLK↑	$t_{D(6)}$	7.0		22	ns
Delay from RXCFRM high and RXCCLK↑ to J0 byte position clocked out on RXCCLK↑	t_{DELAY}		Note 4		RXCCLK Cycles
Receive Telecom Bus interface output rise and fall times	t_r,t_f	3.8		4.1	ns

Notes:

1. The J1 pulse(s) is(are) not shown in the timing diagram but has(have) the same timing parameters as the J0 pulse.
2. $t_{D(n)(min)}$ represents the earliest time that the corresponding signal starts to change.
3. $t_{D(n)(max)}$ represents the latest time at which the corresponding signal becomes stable.
4. RXMFx occurs once every 500 microseconds. It is not aligned to RXCFRM or RTBDATAOUTx(7:0) or any other signals.
5. t_{DELAY} is determined by the settings of the **DELAYR** control bits as follows:

DELAYR	t_{DELAY}	Units
00	1	RXCCLK Cycles
01	4	RXCCLK Cycles
02	7	RXCCLK Cycles
03	10	RXCCLK Cycles
04	13	RXCCLK Cycles
05	16	RXCCLK Cycles
06	19	RXCCLK Cycles

Figure 7. Asynchronous Microprocessor Interface: Intel-type Write Cycle Timing



100 pF Load

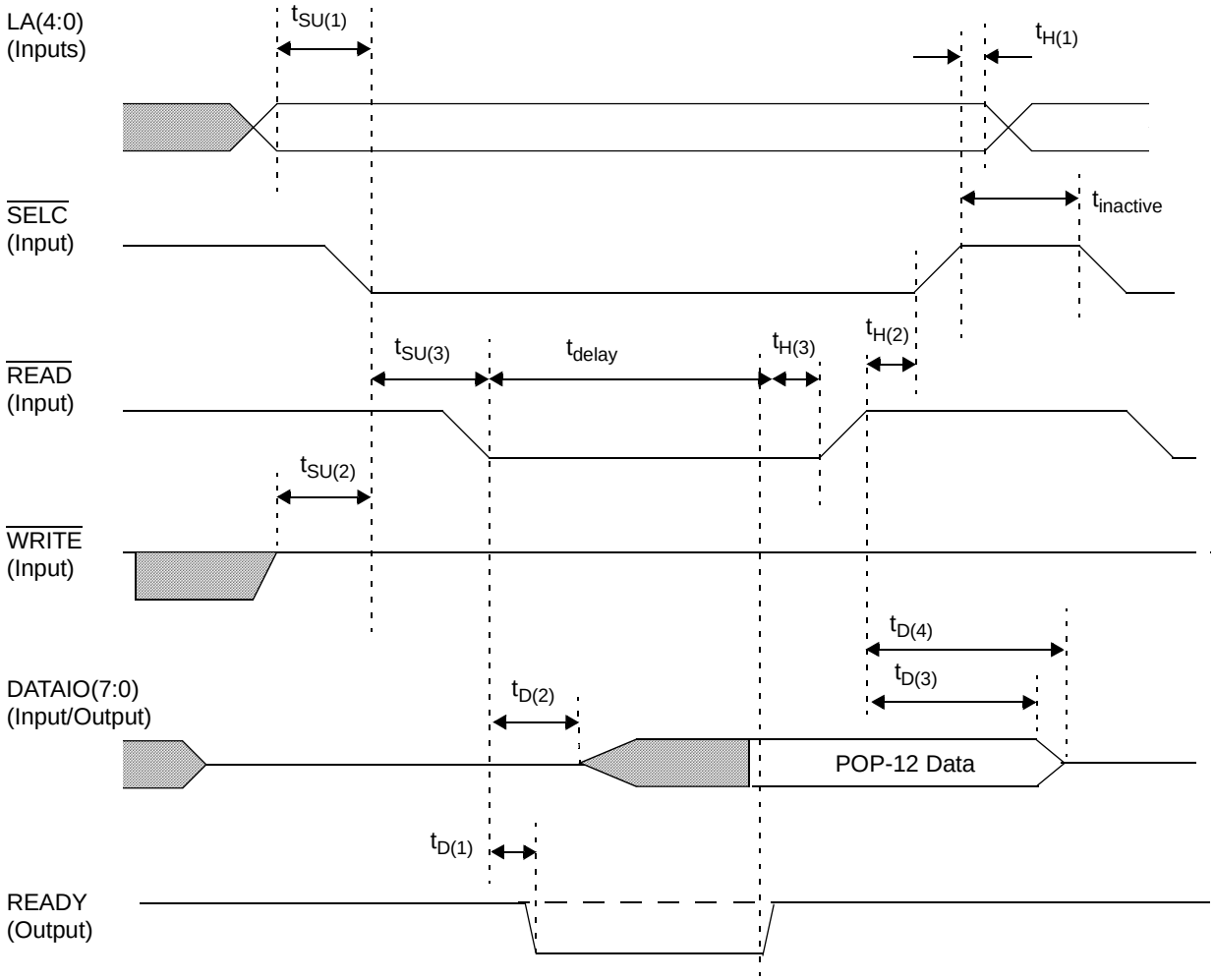
See parameter table on next page.

Parameter	Symbol	Min	Typ	Max	Unit
PCLK clock period (not shown in diagram)[1]	t_{CYC}	50		125	ns
PCLK duty cycle	t_{PWH}/t_{CYC}	45		55	%
LA(4:0) set-up time to $\overline{\text{SELC}}$ assertion	$t_{SU(1)}$	0.0			ns
LA(4:0) hold time from $\overline{\text{SELC}}$ de-assertion	$t_{H(1)}$	6.0			ns
$\overline{\text{READ}}$ de-assertion set-up time to $\overline{\text{SELC}}$ assertion	$t_{SU(2)}$	10			ns
$\overline{\text{SELC}}$ assertion set-up time to $\overline{\text{WRITE}}$ assertion	$t_{SU(3)}$	0.0			ns
$\overline{\text{WRITE}}$ assertion to READY valid delay	$t_{D(1)}$	0.0		23	ns
$\overline{\text{SELC}}$ de-assertion (high) time between accesses	$t_{INACTIVE}$	t_{CYC}			ns
$\overline{\text{SELC}}$ hold time from $\overline{\text{WRITE}}$ de-assertion	$t_{H(2)}$	2.0			ns
$\overline{\text{WRITE}}$ hold time from READY assertion	$t_{H(3)}$	0.0			ns
DATAIO(7:0) input set-up time to $\overline{\text{WRITE}}$ de-assertion	$t_{SU(4)}$	7.0			ns
DATAIO(7:0) input hold from $\overline{\text{WRITE}}$ de-assertion	$t_{H(4)}$	4.0			ns
READY assertion from $\overline{\text{WRITE}}$ assertion[2]	t_{delay}	t_{CYC}		Note 2	ns

Notes:

1. GPPCLK must always be applied to the POP-12 to run the microprocessor interface.
2. When accessing the global registers at virtual address 0000H-0FFFH the READY signal will always remain high, as shown by the dashed line above. The maximum value of tdelay is 3*tCYC + (the larger of either 43*TXCCLKperiod or 43*RTBCLKINx).

Figure 8. Asynchronous Microprocessor Interface: Intel-type Read Cycle Timing



100 pF Load

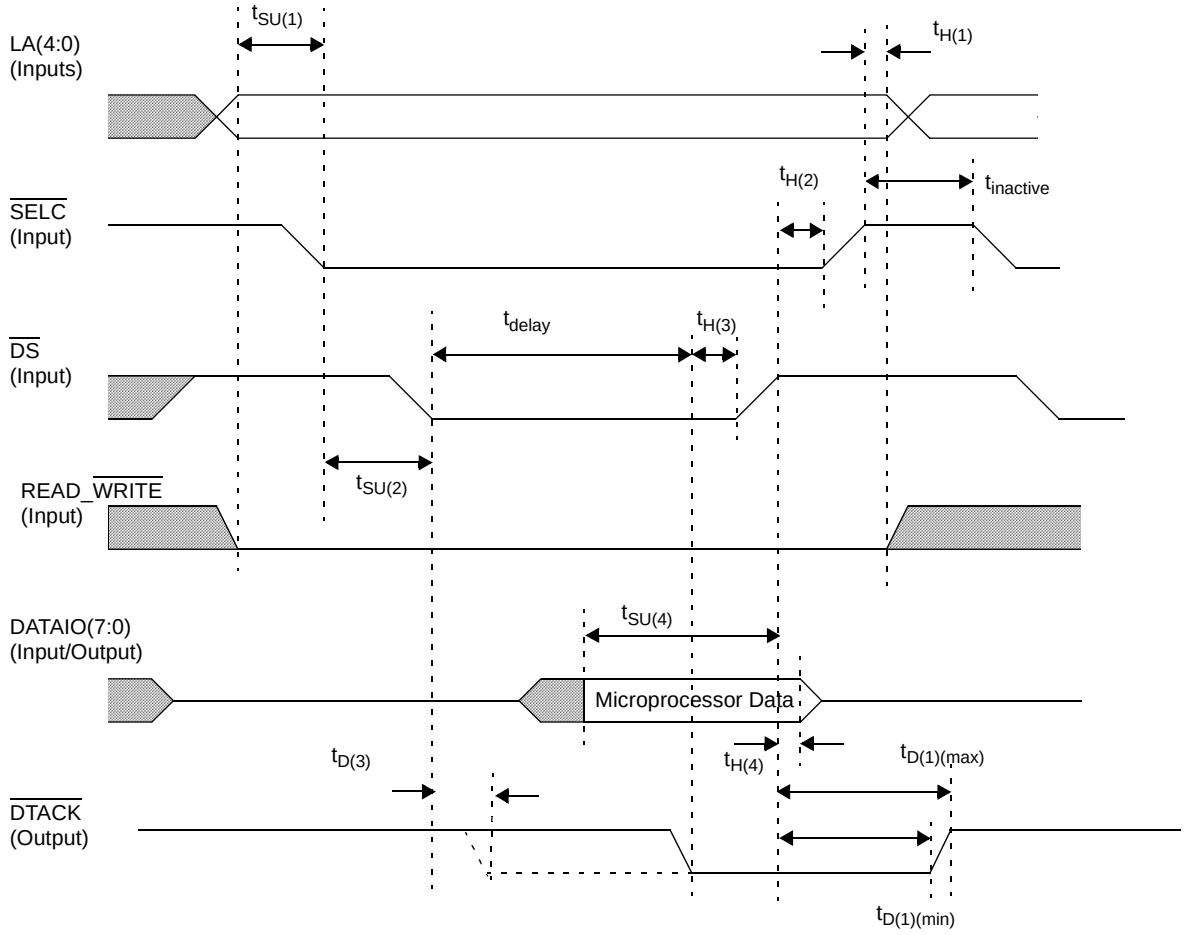
See parameter table on next page.

Parameter	Symbol	Min	Typ	Max	Unit
PCLK clock period (not shown in diagram)[1]	t_{CYC}	50		125	ns
PCLK duty cycle	t_{PWH}/t_{CYC}	45		55	%
LA(4:0) set-up time to $\overline{SELC}$ assertion	$t_{SU(1)}$	0.0			ns
LA(4:0) hold time from $\overline{SELC}$ de-assertion	$t_{H(1)}$	6.0			ns
$\overline{WRITE}$ de-assertion set-up time to $\overline{SELC}$ assertion	$t_{SU(2)}$	0.0			ns
$\overline{SELC}$ assertion set-up time to $\overline{READ}$ assertion	$t_{SU(3)}$	0.0			ns
$\overline{READ}$ and $\overline{SELC}$ assertion to $\overline{READY}$ valid delay	$t_{D(1)}$	0.0		23	ns
$\overline{SELC}$ de-assertion (high) time between accesses	$t_{INACTIVE}$	t_{CYC}			ns
$\overline{SELC}$ hold time from $\overline{READ}$ de-assertion	$t_{H(2)}$	3.0			ns
$\overline{READ}$ hold time from $\overline{READY}$ assertion	$t_{H(3)}$	0.0			ns
$\overline{READY}$ assertion from $\overline{READ}$ and $\overline{SELC}$ assertion[2]	t_{delay}	t_{CYC}		Note 2	ns
DATAIO(7:0) output tristate turned off from $\overline{READ}$ and $\overline{SELC}$ assertion	TD(2)	3.0		17	ns
DATAIO(7:0) output valid delay from $\overline{READ}$ or $\overline{SELC}$ de-assertion	TD(3)	1.0			ns
DATAIO(7:0) output tristate delay from $\overline{READ}$ or $\overline{SELC}$ de-assertion	TD(4)	3.0		14	ns
DATAIO output rise and fall times	t_r,t_f	4.8		5.3	ns

Notes:

1. The GPPCLK must always be applied to the POP-12 to run the microprocessor interface.
2. When accessing the global registers at virtual address 0000H-0FFFH the READY signal will always remain high, as shown by the dashed line above. The maximum value of t_{delay} is $3*t_{CYC}$ + (the larger of either 43*TXCCLKperiod or 43*RTBCLKINx).

Figure 9. Asynchronous Microprocessor Interface: Motorola-type Write Cycle Timing



100 pF Load

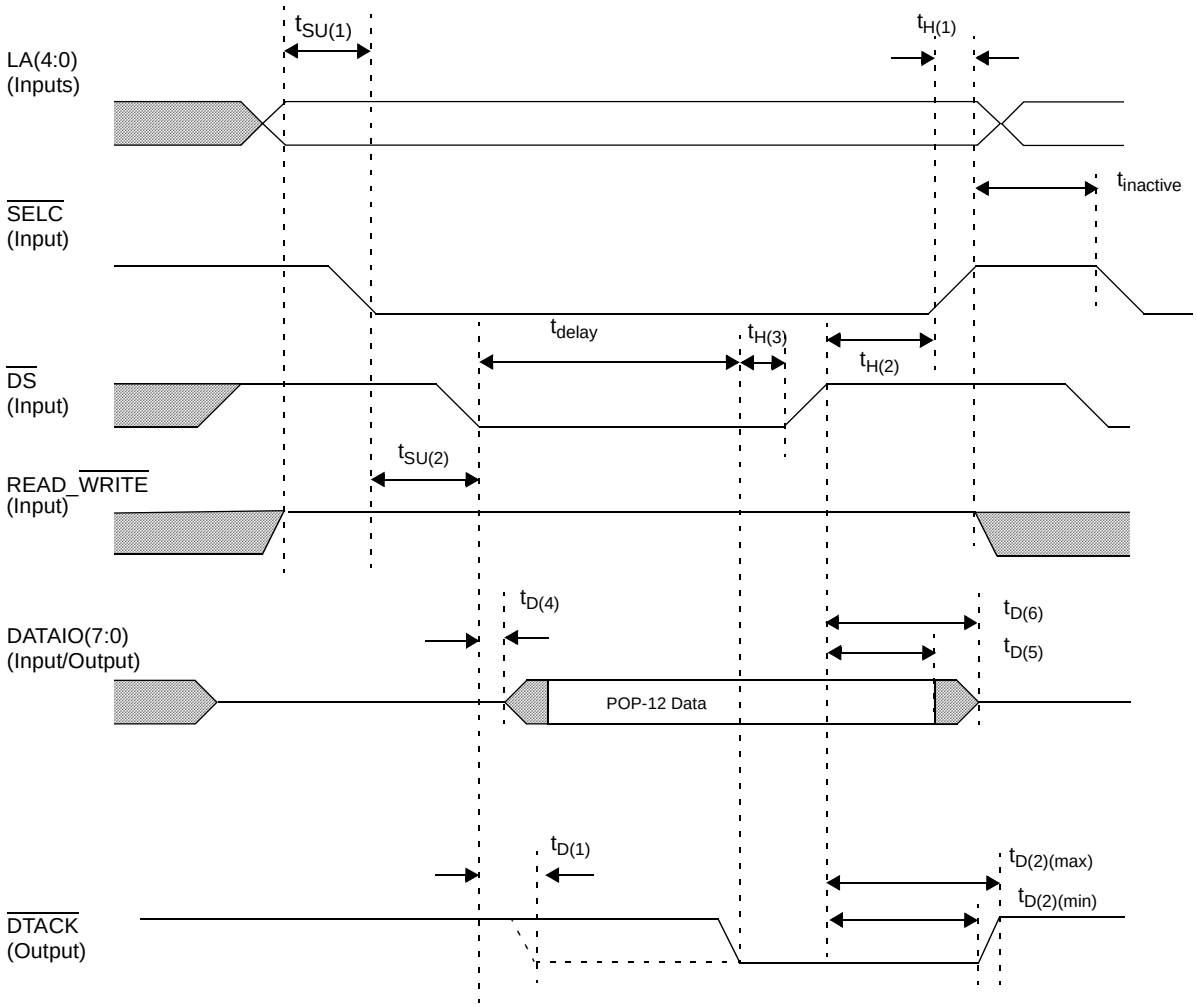
See parameter table on next page.

Parameter	Symbol	Min	Typ	Max	Unit
PCLK clock period (not shown in diagram)[1]	t_{CYC}	50		125	ns
PCLK duty cycle	t_{PWH}/t_{CYC}	45		55	%
LA(4:0)/READ_$\overline{\text{WRITE}}$ set-up time to $\overline{\text{SELC}}$ assertion	$t_{SU(1)}$	0.0			ns
LA(4:0)/READ_$\overline{\text{WRITE}}$ hold time from $\overline{\text{SELC}}$ de-assertion	$t_{H(1)}$	6.0			ns
$\overline{\text{SELC}}$ assertion set-up time to $\overline{\text{DS}}$ assertion	$t_{SU(2)}$	0.0			ns
$\overline{\text{SELC}}$ and $\overline{\text{DS}}$ assertion to $\overline{\text{DTACK}}$ valid delay	$t_{D(3)}$	0.0		23	ns
$\overline{\text{SELC}}$ or $\overline{\text{DS}}$ de-assertion to $\overline{\text{DTACK}}$ de-assertion delay	$t_{D(1)}$	1.0		23	ns
$\overline{\text{SELC}}$ de-assertion (high) time between accesses	$t_{INACTIVE}$	t_{CYC}			ns
$\overline{\text{SELC}}$ hold time from $\overline{\text{DS}}$ de-assertion	$t_{H(2)}$	3.0			ns
$\overline{\text{DS}}$ hold time from $\overline{\text{DTACK}}$ assertion	$t_{H(3)}$	0.0			ns
DATAIO(7:0) input set-up time to $\overline{\text{DS}}$ de-assertion	$t_{SU(4)}$	7.0			ns
DATAIO(7:0) input valid hold from $\overline{\text{DS}}$ de-assertion	$t_{H(4)}$	4.0			ns
$\overline{\text{DTACK}}$ assertion from $\overline{\text{DS}}$ assertion[2]	t_{delay}	t_{CYC}		Note 2	ns

Notes:

1. The GPPCLK must always be applied to the POP-12 to run the microprocessor interface.
2. When accessing the global registers at virtual address 0000H-0FFFH the $\overline{\text{DTACK}}$ signal will go low as soon as $\overline{\text{SELC}}$ and $\overline{\text{DS}}$ are asserted, as shown by the dashed line above. The maximum value of t_{delay} is $3*t_{CYC}$ + (the larger of either 43*TXCCLKperiod or 43*RTBCLKINx).

Figure 10. Asynchronous Microprocessor Interface: Motorola-type Read Cycle Timing



100 pF Load

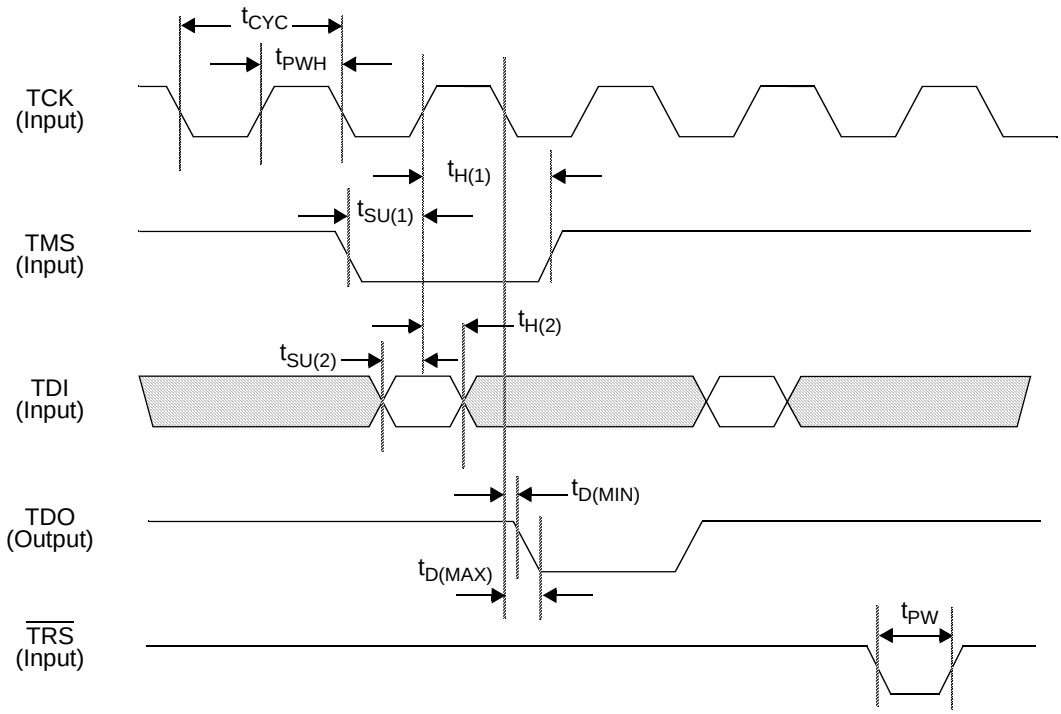
See parameter table on next page.

Parameter	Symbol	Min	Typ	Max	Unit
PCLK clock period (not shown in diagram)[1]	t_{CYC}	50		125	ns
PCLK duty cycle	t_{PWH}/t_{CYC}	45		55	%
LA/READ_$\overline{\text{WRITE}}$ set-up time to $\overline{\text{SELC}}$ assertion	$t_{SU(1)}$	0.0			ns
LA/READ_$\overline{\text{WRITE}}$ hold time from $\overline{\text{SELC}}$ de-assertion	$t_{H(1)}$	6.0			ns
$\overline{\text{SELC}}$ assertion set-up time to $\overline{\text{DS}}$ assertion	$t_{SU(2)}$	0.0			ns
$\overline{\text{SELC}}$ and $\overline{\text{DS}}$ assertion to $\overline{\text{DTACK}}$ valid delay	$t_{D(1)}$	0.0		23	ns
$\overline{\text{SELC}}$ or $\overline{\text{DS}}$ de-assertion to $\overline{\text{DTACK}}$ de-assertion delay	$t_{D(2)}$	1.0		23	ns
$\overline{\text{SELC}}$ de-assertion (high) time between accesses	$t_{INACTIVE}$	t_{CYC}			ns
$\overline{\text{SELC}}$ hold time from $\overline{\text{DS}}$ de-assertion	$t_{H(2)}$	6.0			ns
$\overline{\text{DS}}$ hold time from $\overline{\text{DTACK}}$ assertion	$t_{H(3)}$	0.0			ns
$\overline{\text{DTACK}}$ assertion from $\overline{\text{DS}}$ assertion[2]	t_{delay}	t_{CYC}		Note 2	ns
DATAIO(7:0) output tristate turned off from $\overline{\text{DS}}$ and $\overline{\text{SELC}}$ assertion	$t_{D(4)}$	3.0		17	ns
DATAIO(7:0) output valid hold from $\overline{\text{DS}}$ or $\overline{\text{SELC}}$ de-assertion	$t_{D(5)}$	1.0			ns
DATAIO(7:0) output tristated from $\overline{\text{DS}}$ or $\overline{\text{SELC}}$ de-assertion	$t_{D(6)}$	3.0		14	ns
DATAIO(7:0) output rise and fall times	t_r,t_f	4.8		5.3	ns

Notes:

1. The GPPCLK must always be applied to the POP-12 to run the microprocessor interface.
2. When accessing the global registers at virtual address 0000H-0FFFH the $\overline{\text{DTACK}}$ signal will go low as soon as $\overline{\text{SELC}}$ and $\overline{\text{DS}}$ are asserted, as shown by the dashed line above. The maximum value of t_{delay} is 3*t_{CYC} + (the larger of either 43*TXCCLKperiod or 43*RTBCLKINx).

Figure 11. Boundary Scan Timing



100 pF Load

Parameter	Symbol	Min	Max	Unit
TCK clock period	t_{CYC}	50		ns
TCK clock duty cycle	$t_{PWH/TCYC}$	40	60	%
TMS setup time to TCK↑	$t_{SU(1)}$	3.0		ns
TMS hold time after TCK↑	$t_{H(1)}$	15		ns
TDI setup time to TCK↑	$t_{SU(2)}$	3.0		ns
TDI hold time after TCK↑	$t_{H(2)}$	15		ns
TDO delay from TCK↓	t_D	3.0	20	ns
$\overline{TRS}$ pulse width	t_{PW}	50		ns

OPERATION

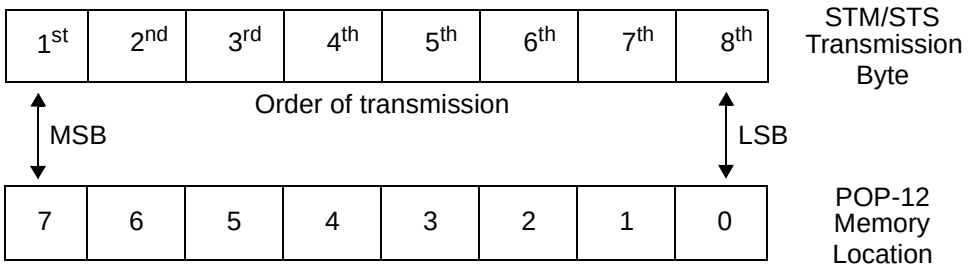
This Operation section provides additional detailed information on the operation of the functional units and processes of the POP-12 device. It is by no means exhaustive and should be read in conjunction with the information contained in the other sections of this Data Sheet.

It should be noted that interrupt requests are not all rationalized in the POP-12 hardware. That is, lower level alarms are not inhibited by higher level alarms except when indicated. The rationalization of alarms needs to be handled in the software that monitors the POP-12 device.

GENERAL INFORMATION AND MEMORY MAP BIT ORDERING

The memory map of the POP-12 device is partitioned into thirteen segments, as shown in "POP-12 Memory Map" on page 59. The first block, called Common Control, contains all of the global configuration parameters and cross connect settings for the POP-12 device. The other twelve blocks, called POP Function 1 -12, contain the individual control and status for each of up to twelve channels that can be processed by the POP-12.

Memory map address locations are stated in Hexadecimal (H). The bit placement relationship between a receive and transmit serial SDH/SONET (STM/STS) byte (e.g., J1) and its corresponding storage location in the POP-12 memory map is shown below:



CLOCKS

The PCLK input clock needs to be present to enable the microprocessor interface to operate. The corresponding clocks and Telecom Bus signals for the other blocks need to be present or access to those chiplets via the microprocessor interface will not succeed and will result in an internal watchdog timer timing out. The watchdog timer causes the READY/DTACK signal to go active after 255 PCLK cycles if the internal logic is unable to generate one, such as would occur if a clock was missing. This keeps the microprocessor from hanging up.

POP-12 POWER-UP-RESET SEQUENCE

The RESETUP lead is used to perform a synchronous reset of the POP-12 device. At power up, after the power and all clocks (except TCK) have stabilized, this lead must be held low for at least 150ns and then brought high before the POP-12 can be configured for operation. Also, WRITE/READ_WRITE must be held high during the time that RESETUP is held low and for 10 ns after RESETUP is brought high.

POP-12 OPERATIONAL OVERVIEW

The POP-12 supports three modes of operation: STS-3, STS-3c, and STM-1. Each full duplex channel interface is able to be configured to one of the three modes independent of the other Telecom Bus. The only constraint that needs to be observed is in the cross connecting of data from one Telecom Bus to another. e.g., If data arriving at Telecom Bus 1 is to be cross connected to Telecom Bus 3, then both Telecom Bus 1 and 3 need to be configured for the same mode.

RXCCLK and optionally RXCFRM are used to retime all four RX Telecom Bus interface inputs. TXCCLK and optionally TXCFRM are used to retime all four TX Telecom Bus interface inputs. However, the individual Telecom Bus inputs can operate independently of each other, provided that the input clock rate is 19.44 MHz ± 20 ppm.

A block diagram of the POP-12 device is shown in the figures below.

In the RX direction, there are four Telecom Bus inputs called TBI. These Telecom Bus inputs accept either a J0J1 or a frame pulse aligned to the A23 byte. The data formats on each Telecom Bus can either be 1xVC-4/STS-3c-SPE or 3xSTS-1-SPE. Pointer processing and/or retiming are performed in order to locate the VC-4/STS-3c-SPE or STS-1-SPEs and to align the Telecom Bus (TB) signals to a common frame reference for cross connecting latter. The Output of the Pointer Retiming Block is also in Telecom Bus format, (path AIS is added in the event that an LOP-P or AIS-P has been detected as indicated in [1] R6-170, provided that the corresponding pointer tracking state machine is not bypassed). The telecom bus data is then passed to an AU-3/AU-4 cross connect where they can be time slot interchanged at the AU-3/AU-4 level and then applied to the POP-12 RX block. The POP-12 RX block processes the Path Overhead of up to four groups of 3xSTS-1-SPE or up to 4xVC-4/STS-3c-SPE or any combination and passes FEBE and RDI information to the POP-12 TX block as shown in the following figure. Additionally, the RX Loss of Pointer and Path AIS alarms are routed to the appropriate RX POH processor according to the AUCC R control bit settings. e.g., If RX input STS-1 #3 is routed to RX output STS-1 #5, then the RX LOP and Path AIS from the Pointer Tracking State Machine that processes the input STS-1 #3 are routed to the RX POH processor that corresponds to RX output STS-1 #5.

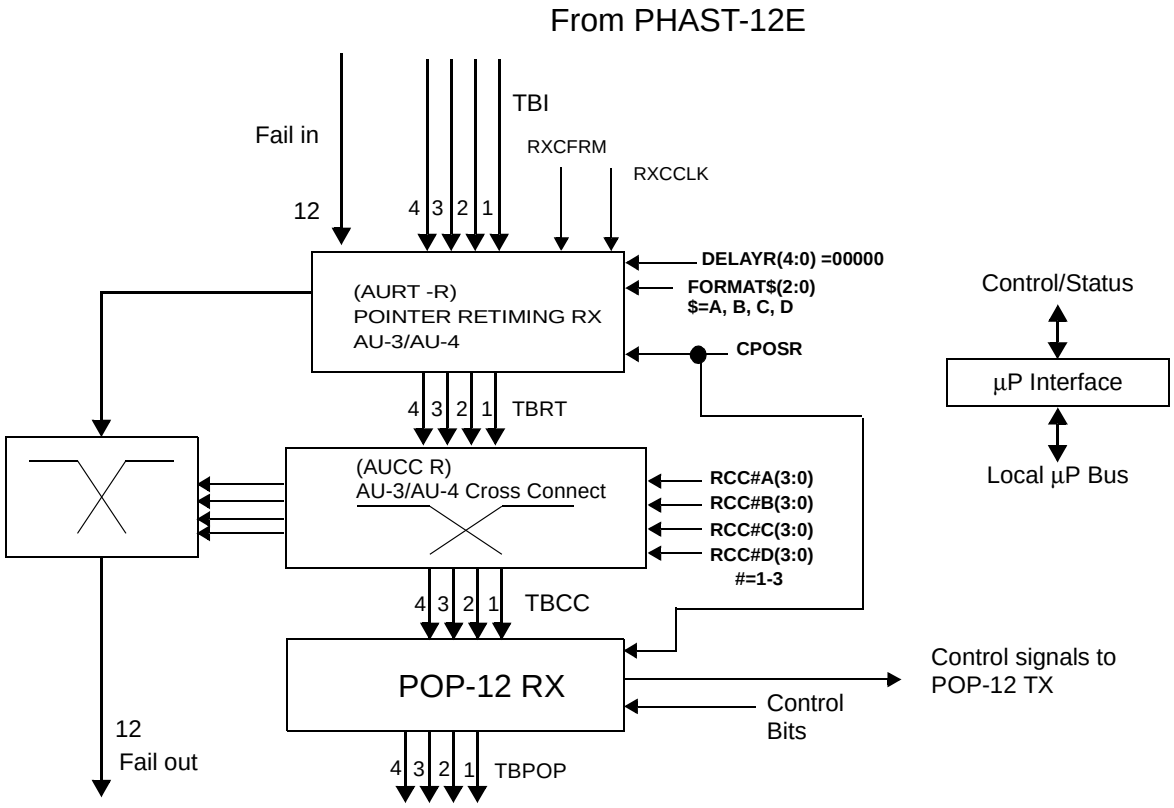


Figure 12. Block Diagram of POP-12 Device RX Direction

In the TX direction, basically the same functionality occurs. Telecom Bus data is accepted, and the pointers are processed and the payloads are aligned to a common frame reference, which is the PHAST-12E's TXCCLK and TXCFRM signals. This is mandatory since the PHAST-12E must be in AU-4 mode in order to trick it into accepting the STS-1-SPEs. The PHAST-12E can do this in AU-4 mode, because, in AU-4 mode it blindly accepts an AU-4 structure from its Telecom Bus interface. The AU-4 structure not only is capable of housing an AU-4, but it is capable of housing three byte interleaved STS-1s, and hence, three STS-1-SPE. The PHAST-12E requires that the data it receives be aligned to the TXCCLK and TXCFRM signals. So to compensate for the delays through the AUCC and POP-12 functions, a delay function has been added which allows the internal frame reference of the retiming circuit to be placed a programmable number of clock cycles ahead/behind of the TXCFRM signal from the PHAST-12E. If the TXCFRM (or RXCFRM) signal is not provided, then it must be tied low. Of course, in that case, the retiming circuit won't be aligned to anything in particular. However, the TXCCLK and RXCCLK clocks are always required. They are a 19.44MHz ± 20 ppm clock with a 45%-55% duty cycle. The POP-12 TX block takes alarm and error information from the RX side of the device and generates path FEBE and RDI.

The AUCC and AURT blocks are identical to those used on the RX side. The POP-12 TX and RX blocks are composed of four full duplex POH processing blocks.

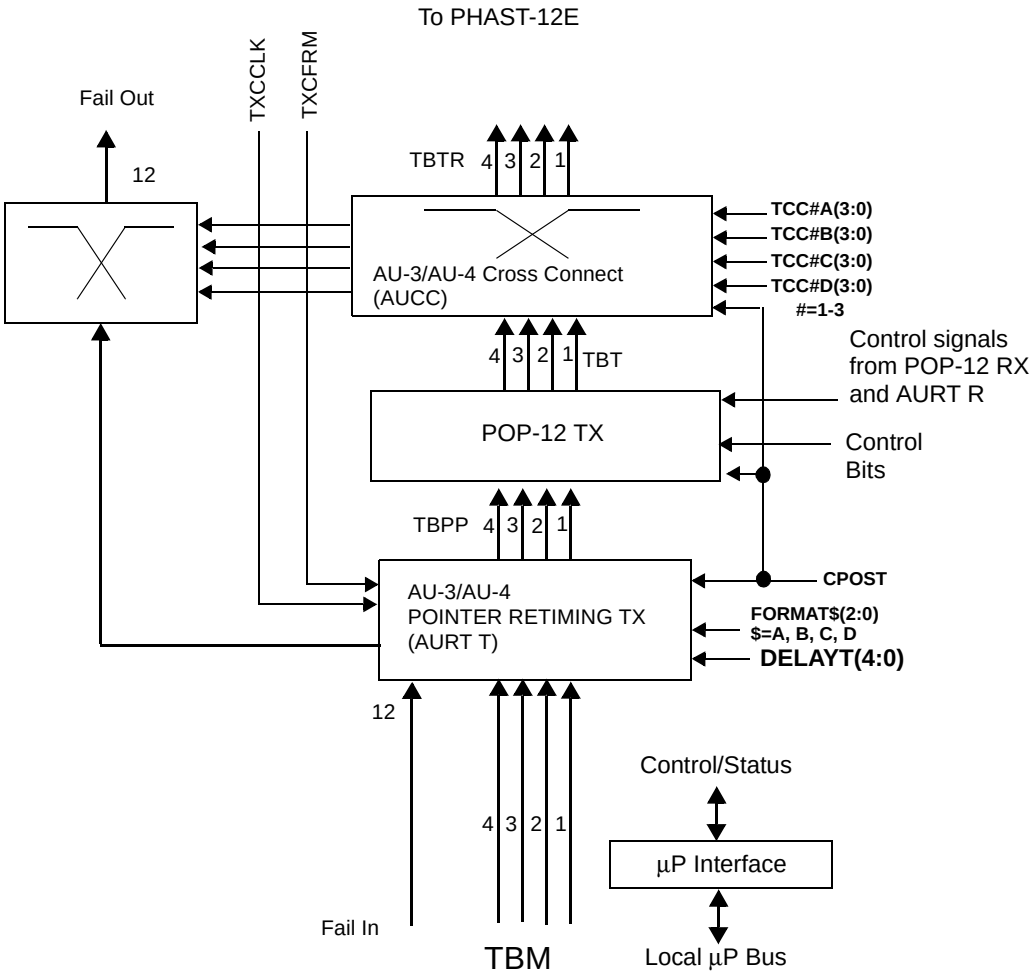


Figure 13. Block Diagram of POP-12 Device TX Direction

Also included in both the TX and RX directions are fail inputs and outputs. There are twelve in each direction. In STS-3 mode, by setting a fail input high, the corresponding STS payload are forced to all 1s. In STS-3c/STM-1 modes, fail inputs 1, 4, 7, and 10 control all three of their respective STSs. Cross connects are also provided as shown in the figures above so that the fail signals can be cross connected to the fail output that corresponds to its associated STS from the input. The fail outputs go high when the corresponding Retimer detects either a Loss of Pointer or Path AIS when the Pointer Tracking State Machine is not bypassed, or when the corresponding Fail input is asserted.

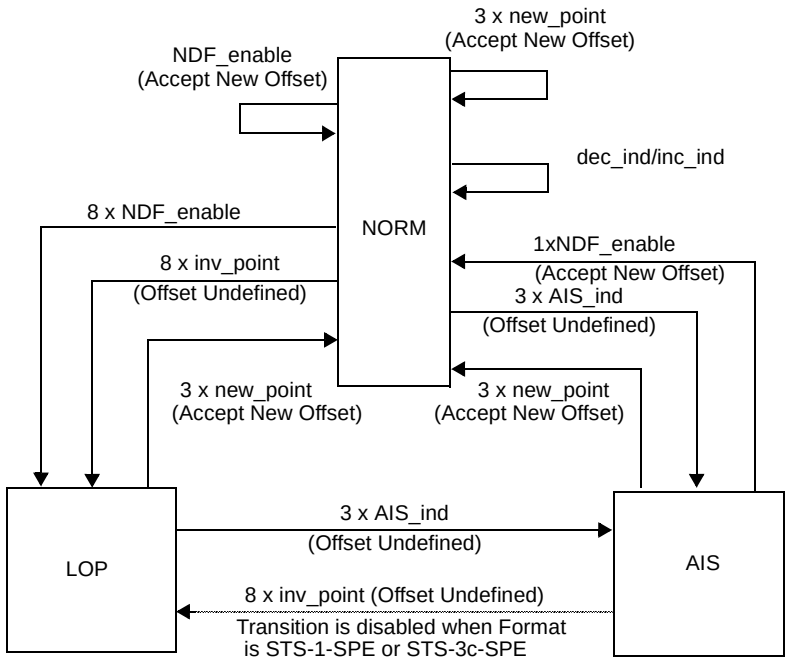
AURT (AU/STS RETIMING BLOCK)

There are four AURT blocks in the TX direction and four AURT blocks in the RX direction of the POP-12. Each of these blocks accepts a byte wide Telecom Bus signal formatted as either an STM-1, STS-3c, or an STS-3, and performs pointer tracking and retiming to a common reference clock and optional reference frame input. For the TX direction, the reference clock and frame are called TXCCLK and TXCFRM. For the RX direction, the reference clock and frame are called RXCCLK and RXCFRM. If the frame pulses are used they must be one reference clock wide and occur once every 2430 cycles (i.e., 125 microseconds). The four corresponding Telecom Bus outputs will be aligned to the frame pulse according to the settings of the **DELAYT** or **DELAYR** bits and they will all be timed by the reference clock. The pointer tracking can be bypassed through software control. In this case, the Telecom Bus signals (SPE, J0J1, Data) are applied directly to the retiming logic.

The formats of the signals presented to the AURT are important for proper operation. Connecting the POP-12 to TranSwitch's PHAST-12E guarantee's the proper operation of the POP-12. However, for applications where the POP-12 may be used by itself, the following needs to be observed:

- Pointer tracking is not bypassed:
  - The Telecom Bus Data needs to contain valid pointers
  - The J0J1 input must contain either a J0 or an A23 byte pulse. J1 pulses are optional. V1 pulses will not interfere with normal operation.
  - The SPE signal needs to be low during the J0 or A23 pulse/byte. It can be high all other times as the POP-12 regenerates the SPE signal internally based on the received pointers and J0/A23 position.
- Pointer tracking is bypassed:
  - The Telecom Bus Data does not need to contain valid pointers
  - The J0J1 input must contain J1 byte pulses (1 for each J1 byte). J0/A23 pulses are optional. V1 pulses will not interfere with normal operation.
  - The SPE signal needs to be high during SPE/VC byte times and low during non-SPE/VC byte times. This includes when pointer adjustments occur.

Figure 14 below is a composite of the Bellcore and ITU-T specifications for one of the point Pointer Tracking State Machines (PTSM) used in the POP-12. Those bits can also generate a maskable interrupt to the external microprocessor. These specifications are found in Reference [1] as R3-89, R3-90, R3-91, R3-92, R3-93, R3-95, R3-96, R3-99 (performed by the muxes between the PTSM and FIFOs), R3-102 (performed by the muxes between the PTSM and FIFOs), R6-172, R6-173 (except that for STS-3c mode the concatenation indicators are not monitored, only the STS pointers are monitored) and Reference [2] sections 8.1.4, 8.1.6, and Reference [3] Annex C.1. Loss of Pointer and Path AIS are detected and reported via latched status bits. All 1s is inserted into the output of the AURT in the corresponding STS/VC when Loss of Pointer or Path AIS is detected, except when the PTSM is bypassed.



new_point: Normal NDF AND (ss bits=10 for VC-4 format OR ss bits ignored for NOT VC-4 format) AND pointer offset in range.
NDF_enable: NDF enabled AND (ss bits=10 for VC-4 format OR ss bits ignored for NOT VC-4 format) AND pointer offset in range.
AIS_ind: H1H2 pointer bytes set to all 1s.
inc_ind: Normal NDF AND (ss bits=10 for VC-4 format OR ss bits ignored for NOT VC-4 format) AND majority of I bits inverted AND no majority of D bits inverted.
dec_ind: Normal NDF AND (ss bits=10 for VC-4 format OR ss bits ignored for NOT VC-4 format) AND majority of D bits inverted AND no majority of I bits inverted.
inv_point: Any other pointer or a new_point with a pointer offset not equal to the current offset.
NDF enabled = 1001, 0001, 1101, 1011, 1000.
Normal NDF = 0110, 1110, 0010, 0100, 0111.
3xAIS_ind= 3 consecutive AIS_ind.
8xinv_point= 8 consecutive inv_point.
8xNDF_enable= 8 consecutive NDF_enable.
3xnew_point = 3 consecutive and identical new pointers.
After reset, the PTSM block starts off in the LOP state.
LOP or AIS states cause all 1s to be generated at the output of the PTSM.
When the selected format is STM-1 (VC-4) or STS-3c the PTSM for slots B and C always passes the data straight through.

Figure 14. Pointer Tracking State Machine

AUCC (AU/STS CROSS CONNECT BLOCK)

The POP-12 contains two non-blocking cross connects. One in the TX direction and one in the RX direction. Refer to Figure 1. These cross connects allow traffic at the AU-3 or AU-4 level to be cross connected to any co-directional POP Function/Telecom Bus through software control. The AUCC cross connects allow data to be broadcast/bridged to multiple AU/STSs or selected from multiple AU/STSs for protection purposes.

POP (PATH OVERHEAD PROCESSING)

A high level block diagram of the POP functionality is shown below. A single POP function supports POH processing for a single STS-1-SPE or a single VC-4/STS-3c-SPE as determined by the **FORMAT$(2:0)** bits. Three of the POP functions are combined together to support STS-3 POH processing. The sequencer provides

an enable signal which tells the POP function when there is valid data (i.e. it identifies the appropriate slots to process). In the RX direction the data is passed through unmodified unless a path AIS needs to be generated. The POH bytes are written to registers for microprocessor access. In the TX direction, the option exists to pass through or provide the POH bytes on a per POH byte option. The sections below describe in more detail the functions of the blocks in Figure 15 and Figure 16.

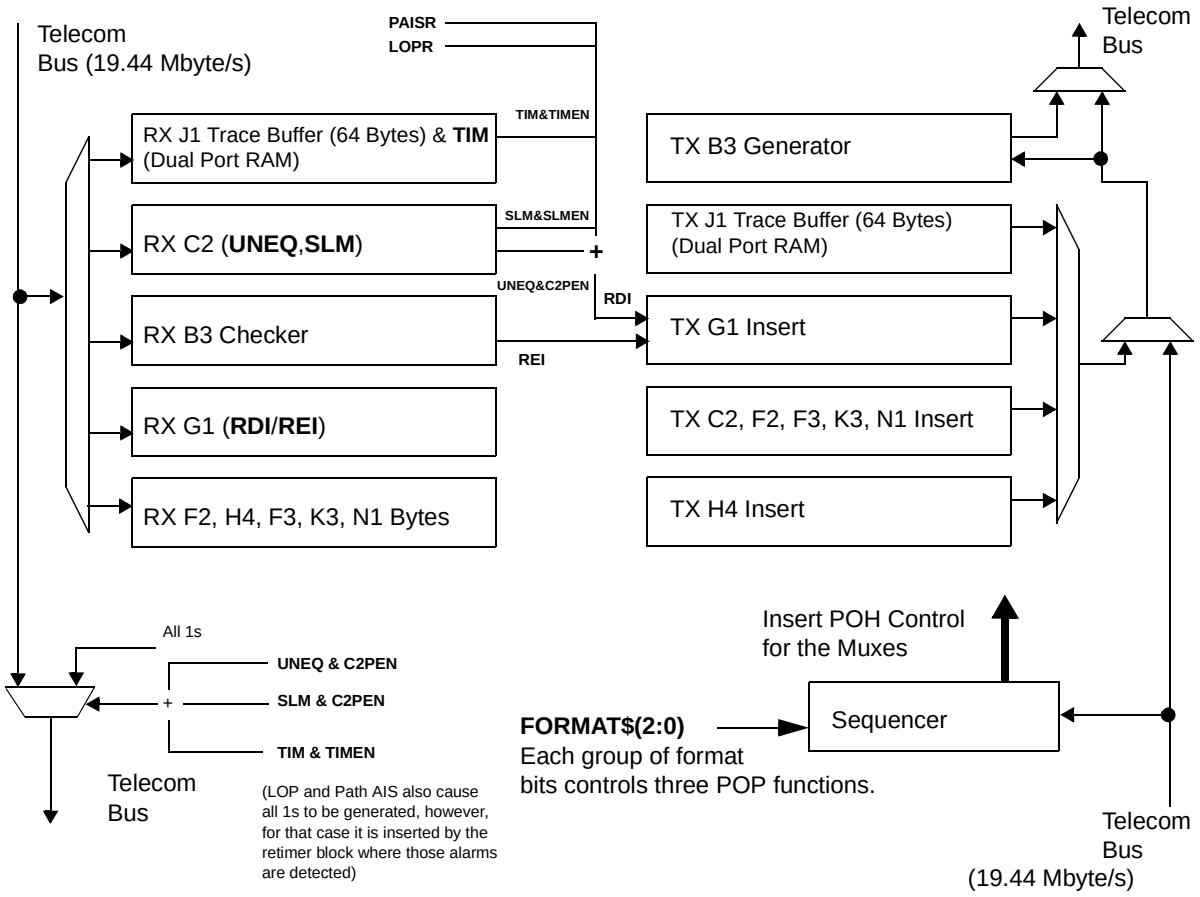


Figure 15. High Level Block Diagram of 1/12 of POP-12 Function

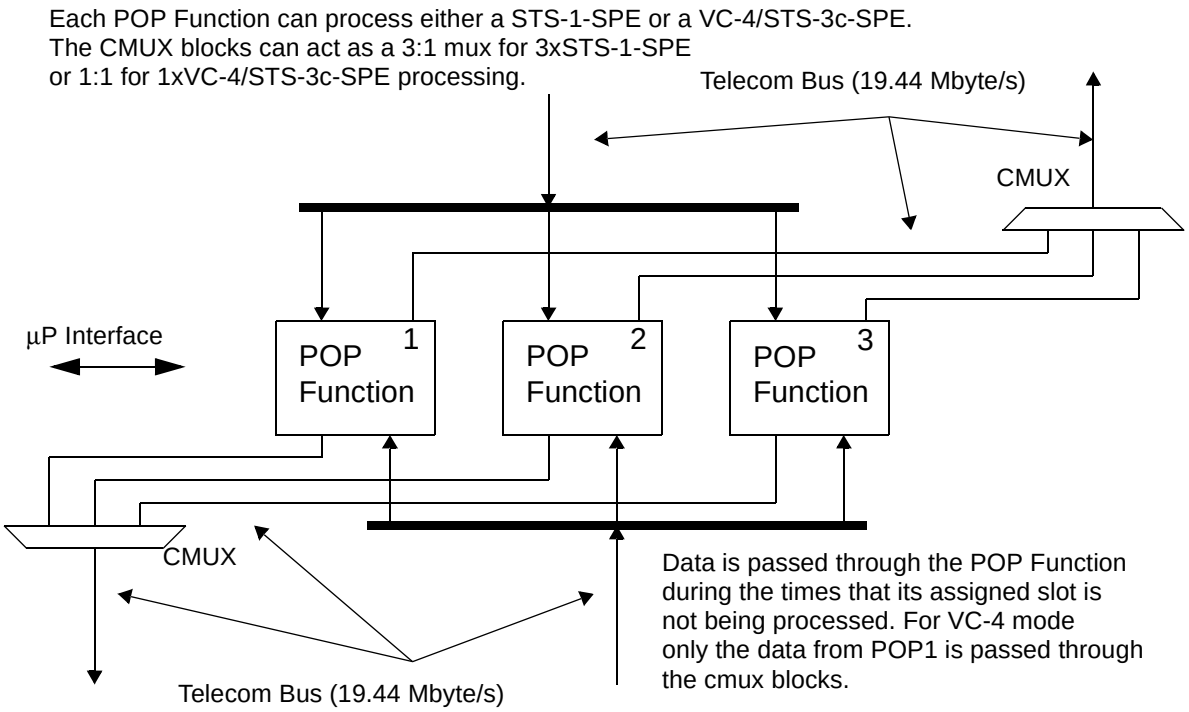


Figure 16. Muxing of 3 POP Functions for STS-3

TX J1 TRACE BUFFER

This is a 64 byte circular buffer that is used to transmit the Path Trace Message. These bytes are written by the microprocessor. This allows both a 64 byte and a 16 byte message (repeated 4 times of course) to be supported per Reference [1] R6-150 and Reference [2] section 9.3.1.1. The J1 Path Trace can be either be derived from the TX J1 Trace Buffer or from the input Telecom Bus signal under software control using the **J1EN** bit.

TX C2, F2, F3, K3, N1 INSERT

The C2, F2, F3, K3, and N1 bytes are written by the microprocessor, to their corresponding registers, from where they can be transmitted if enabled by their enable bits (**C2EN**, **F2EN**, **F3EN**, **K3EN**, **N1EN**). These bytes can also be derived from the input Telecom Bus signal if their enable bits are set accordingly.

TX H4 INSERT

The H4 Insert logic has three modes of operation. The first is pass through, that is, it passes the H4 through that it receives on its Telecom Bus. The second mode is fixed pattern mode. In this mode, a fixed pattern written by the microprocessor is continuously transmitted. The third mode is VT (Virtual Tributary Mode). In this mode, a count which indicates the multiframe number is inserted based upon the position of a V1 pulse, in the J0J1 signal. Reference [1] section 3.4.1 and Reference [2] sections 8.3.1 and 8.3.8 indicate what is shown in the table below:

H4 Byte Bits								V1 through V4 byte in the next frame
1(msb)	2	3	4	5	6	7	8(lsb)	
0	0	0	0	0	0	0	0	V1
0	0	0	0	0	0	0	1	V2
0	0	0	0	0	0	1	0	V3
0	0	0	0	0	0	1	1	V4

On the input telecom bus signal, there is expected to be a V1 pulse following the J1 pulse in the same STS slot. A synchronizer circuit is used to reset the H4 byte generator to follow the H4 sequence in the table above. The V1 indication should cause the TX H4 byte to be initialized to 01H, then in the next frame, as indicated by the J1 pulse, it should be set to 02H, etc. The two control bits, **H4M(1:0)**, control the mode of operation.

TXG1 INSERT

This logic either allows the G1 to be passed through or to be generated based on RX alarms or errors. This is selected through the **G1EN** control bit. When in VC-4 mode and configured to generate the G1 based on RX alarms and errors an RDI will be generated as 100 in bits 5-7 when either an externally indicated (from the PTSM) Path AIS or LOP occur as well as if an **SLM** (Path Signal Label Mismatch), **UNEQ** (Unequipped), or **TIM** (Path Trace Identifier Mismatch) is detected and their appropriate control bits are set. **SLMEN** is used to enable/inhibit **SLM** from causing RDI to be transmitted apart from the **C2PEN** bit since **SLM** is not supposed to cause RDI to be generated but it is supposed to cause AIS to be generated when in SDH mode; but in SONET mode, it causes both RDI and path AIS to be generated. If no alarms are detected in SDH mode then the RDI bits are transmitted as 000. In STS-3 or STS-3c mode, the RDI will be a three bit RDI. If LOP or Path AIS is detected the RDI is 101; if **TIM** is detected and **TIMEN**=1 then the transmitted RDI=110; if **SLM** is detected then the transmitted RDI is 010 and if no alarms are detected then the RDI bits are transmitted as 001. Bit 8 is always set to a 0.
For TX RDI generation, the following Bellcore requirements are supported per reference [1]: O6-208, R6-209, O6-210, R6-211, R6-212, R6-214, O6-215. A paraphrase of Table 6-4 in [1] is given below for convenient reference.

3-Bit RDI for STS-3c/STS-3 modes

G1 Bits 5-7	Priority	Trigger	
000	Not Applicable	No defects	This code is transmitted by devices not supporting 3-bit RDI.
001	4	No defects	
010	3	SLM	
011	Not Applicable	No defect	This code is transmitted by devices not supporting 3-bit RDI.
100	Not Applicable	No Defect	This code is transmitted by devices not supporting 3-bit RDI. This code is detected by devices that support 3-bit RDI.
101	1	AIS-P, LOP-P	
110	2	UNEQ, TIM	RDI based upon TIM is transmitted only when TIM is activated.
111	Not Applicable		This code is detected by devices that support 3-bit RDI.

Bits 1-4 transmit the REI as provided by the RX B3 Checker. A small FIFO of 10 nibbles deep is used to buffer the data and take care of any clock frequency differences between the TX and RX sides. This will allow the REI generation logic to sustain a continuos burst of B3 errors for over 30 seconds (i.e. 240,000+ frames of errored B3). When the FIFO is empty, zeros are transmitted in bits 1-4. The read port of the FIFO contains synchronization logic to synchronize it to the TX clock.

For TX REI generation, the following Bellcore standard is supported per reference [1]: R3-24.

For both TX REI and RDI generation, the POP-12 complies with ITU-T recommendation reference [2] section 9.3.1.4 and Reference [3] sections 2.2.3.2, 2.2.3.3, 2.2.3.4, 6.2.1.1, 6.2.1.2, 6.2.3.1, and 6.2.3.2.

TX B3 GENERATOR

This logic either allows the B3 to be passed through or to be recalculated. This is selected through the **B3EN** control bit. The B3 calculation, when performed, is performed after all of the other POH bytes have been inserted, including the B3 (which should have been calculated during the previous frame. The B3 calculation is performed over all of the bits of the previous STS-1-SPE/VC-4/STS-3c-SPE using even parity as per Reference [2] section 9.3.2.1. and Reference [1] R3-21.

Although a misnomer, frame boundaries will be determined by the J1 byte position.

TX ALL ZEROS GENERATOR

A control bit **AZSPE** is provided to force the TX input data to the POP-12 to all zeros on a per VC/STS basis. When used with the control bits in the TXCNTL1 and 2 register either Unequipped or Supervisory Unequipped signals can be inserted into any of the TX STS-1-SPE, STS-3c-SPE or VC-4 signals. The unequipped and supervisory unequipped signals are defined as follows per Reference [2] sections 6.2.4.2.2 and 6.2.4.3.2:

Unequipped for network not supporting Tandem Connection Signals: The VC-3/4 C2 and J1 bytes are all 0s. The B3 is valid. The payload and remaining POH bytes are unspecified.

Supervisory Unequipped for network not supporting Tandem Connection Signals: The VC-3/4 C2 byte is all 0s. The J1, B3, and G1 bytes are valid. The remaining POH bytes are for further study. The payload is unspecified.

Unequipped as mentioned Reference [1], R3-23 is defined as an all zeros SPE (Synchronous Payload Envelope).

The Table below shows the settings of the bits in the TXCNTL1 and 2 registers in order to transmit the unequipped or supervisory unequipped signals when the **AZSPE** bit is set to a 1.

J1EN	B3EN	C2EN	G1EN	F2EN	H4M1	H4M0	F3EN	K3EN	N1EN	TYPE OF TX UNEQUIPPED SIGNAL
0	1	0	0	0	0	0	0	0	0	Unequipped (Bellcore or ITU-T modes of operation)
1	1	0	1[a]	0	0	0	0	0	0	Supervisory (defined only for ITU-T)

a. The corresponding REIEN, C2PEN, and TIMEN bits should be set to 1 as appropriate to ensure that the path RDI and REI functions are operating.

RX J1 TRACE BUFFER

The Received J1 bytes are written in circular fashion into this 64 byte buffer if TIM processing is not enabled. The microprocessor has access to it and can read the bytes. A separate 64 byte buffer is provided for checking if the received J1 message matches an expected value if TIM processing is enabled. When TIM processing is

enabled, the received J1 byte is compared byte by byte with the expected J1 byte. If all 64 bytes match then the **TIM** clears. If two out of 64 bytes don't match then **TIM** is set. **TIM** is also set after reset while initially acquiring the message if TIM processing is enabled via the **TIMEN** bit. Also long as **TIM** persists, an all 1s signal will be generated downstream.

RX C2

The RX C2 bytes are written frame by frame into a register for access by the microprocessor. The C2 byte is monitored for SLM (signal label mismatch) and UNEQ (unequipped). **SLM** is declared/cleared when the RX C2 byte, does not match / does match, a microprocessor written C2 compare register or a hard coded 01H value for 5 consecutive frames. **UNEQ** is declared/cleared when the RX C2 byte, does not match / does match, 00H for 5 consecutive frames. Also long as **SLM** or **UNEQ** persists, an all 1s signal will be generated downstream. RX C2 byte processing can be enabled or disabled via the **C2PEN** bit.

RX C2 processing is performed per Reference [1] R6-124, O6-125, R6-126, O6-127, R6-131, O6-132, R6-133, and O6-134 and Reference [3] sections 2.2.2.2 and 2.2.2.7.

RX F2, F3, K3, N1 BYTES

These bytes are simply written to registers for access by the microprocessor.

RX B3 CHECKER

The RX B3 byte is checked against a B3 byte calculated for the previously received STS-1-SPE/VC-4/STS-3c-SPE. If any errors are found, the number of bits that are in error are summed up and added to a 16-bit B3 error counter and are also passed to the TX G1 Insert logic for transmission as Path REI. The RX B3 byte is also written to a register for access by the microprocessor. B3 Processing can be enabled or disabled through the **REIEN** bit.

RX G1

In VC-4 mode, bit 5 of the RX G1 byte will be examined for RDI. If it is set to a 1 for 10 consecutive frames, while the LOP and Path AIS alarms are not active, then the **PRDI** bit will be set to 1. If it is set to 0 for 10 consecutive frames or the LOP or Path AIS alarms are active, then the **PRDI** alarm will go inactive.

In STS-3c-SPE or STS-1-SPE modes, bits 5-7 of the RX G1 byte will be examined for RDI. If one of the following 3-bit RDI codes: 010, 100, 101, 110, 111 is detected for 10 consecutive frames, while the LOP and Path AIS alarms are not active, then the corresponding **PRDI** bit (STS-3c) or bit(s) (STS-3) will be set to 1. If bits 5-7 are set to 000, 001, or 011 for 10 consecutive frames or the LOP or Path AIS alarms are active, then the **PRDI** alarm will go inactive.

RX RDI processing is performed per Reference [1] R6-218 and R6-220 and Reference [3] section 2.2.2.6.

Bits 1-4 will be monitored for REI. Any count less than but not equal to 9H will be added to a 16-bit REI counter which can be accessed by the microprocessor.

RX H4 BYTE

Under the control of the **RV1EN** bit an optional V1 pulse can be generated and added to the RX J0J1 signal. This is accomplished by synching up to the H4 byte and noticing when the 2 LSBs are 00. When this occurs an extra pulse is output after the J1 pulse (3 clocks after J1 pulse in STS-1-SPE mode or VC-4/STS-3c-SPE mode).

SEQUENCER

The sequencer block receives its synchronization from the TX AURTs and controls the muxing function. It uses the enable bytes to determine which POH bytes are passed through and which ones are processed. It also performs the timing of when to insert the bytes when in STS-1-SPE and VC-4/STS-3c-SPE mode.

CMUX

The CMUX blocks basically take the Telecom Bus streams and recombine them. If a POP Function is programmed for VC-4/STS-3c-SPE mode then the CMUX just passes the data from POP 1 through; this includes all control signals. If the POP functions are programmed to support STS-1-SPEs then the CMUX byte interleaves STS-1 1 from POP1, with STS-1 2 from POP 2, with STS-1 3 of POP 3. The CMUX gets its synchronization from POP Function 1; although it could get it from any of the other POP functions since the entire Telecom Bus is passed through including the synchronization signals; only the POH of the selected VC/STS is modified. The CMUX block is controlled by the **FORMAT$(2:0)** control bits.

MICROPROCESSOR INTERFACE

The POP-12 can support either Motorola or Intel microprocessor bus types. All of the bus transactions are asynchronous with respect to the microprocessor clock and signals are synchronized internally to the external PCLK signal.

An internal watchdog timer is provided to allow transactions to a specific block to be terminated when a timer runs out, even if the clock for the block being accessed is not present. If a timeout occurs (255 PCLK cycles) the READY/$\overline{\text{DTACK}}$ signal goes active to terminate the cycle.

BOUNDARY SCAN INTERFACE

A boundary scan interface compliant with IEEE Standard 1149.1-1994 (JTAG) is provided for board level testing of the POP-12. Details of the POP-12 boundary scan operation are provided in “Boundary Scan” on page 88.

THROUGHPUT DELAY

The worst case throughput delays for the POP-12 are listed in the table below.

Path that Data Travels	Worst Case Throughput Delay in microseconds
TX Telecom Bus in to TX Telecom Bus out	12
RX Telecom Bus in to RX Telecom Bus out	12

MEMORY MAP

This section contains the address map and register bit descriptions for the internal memory locations of the POP-12 device. The Access columns of the tables specify bit access as Read-only (R), Write-only (W) or Read/Write (R/W). When writing to registers that contain bits designated in the following tables as Reserved or Not Used, care should be taken to write those bits with their default values (if specified), or with 0 if no default value is specified.

The POP-12 is controlled through its microprocessor interface; through which control bits, performance counters, and status bits can be accessed. A high level representation of the POP-12's memory map is shown below.

POP-12 Memory Map

Virtual Address Offset (Hex)			Functional Block	Notes
0000	-	0FFF	Common Control	These Function Are Common to all blocks.
1000	-	1FFF	POP Function 1	
2000	-	2FFF	POP Function 2	
3000	-	3FFF	POP Function 3	
4000	-	4FFF	POP Function 4	
5000	-	5FFF	POP Function 5	
6000	-	6FFF	POP Function 6	
7000	-	7FFF	POP Function 7	
8000	-	8FFF	POP Function 8	
9000	-	9FFF	POP Function 9	
A000	-	AFFF	POP Function 10	
B000	-	BFFF	POP Function 11	
C000	-	CFFF	POP Function 12	

The memory map is accessible through a 16-bit address register and an 8-bit data register. All of the POP-12 registers are accessed through these three registers. To access one of the virtual addresses, the 16-bit address register is written with the virtual address. Then whatever is written to or read from the 8-bit data register, is written or read from the virtual address. These registers are mapped as shown below.

Address and Data Registers

Physical Address (hex)	Register
00	lower 8-bits of virtual address
01	upper 8-bits of virtual address
02	data register

Control and Status Registers (y=1,2,..B, C)

Virtual Address Offset (Hex)	Register Name	Access	Bit Names							
			7	6	5	4	3	2	1	0
0000	GCNLT1	R/W			CPOST	DELAYT(4:0)				
0001	GCNTL2	R/W			CPOSR	DELAYR(4:0)				
0002	FMT1	R/W	--	FORMATB(2:0)			--	FORMATA(2:0)		
0003	FMT2	R/W	--	FORMATD(2:0)			--	FORMATC(2:0)		
0004	TCC1	R/W	TCC1B(3:0)				TCC1A(3:0)			
0005	TCC2	R/W	TCC1D(3:0)				TCC1C(3:0)			
0006	TCC3	R/W	TCC2B(3:0)				TCC2A(3:0)			
0007	TCC4	R/W	TCC2D(3:0)				TCC2C(3:0)			
0008	TCC5	R/W	TCC3B(3:0)				TCC3A(3:0)			
0009	TCC6	R/W	TCC3D(3:0)				TCC3C(3:0)			
000A	RCC1	R/W	RCC1B(3:0)				RCC1A(3:0)			
000B	RCC2	R/W	RCC1D(3:0)				RCC1C(3:0)			
000C	RCC3	R/W	RCC2B(3:0)				RCC2A(3:0)			
000D	RCC4	R/W	RCC2D(3:0)				RCC2C(3:0)			
000E	RCC5	R/W	RCC3B(3:0)				RCC3A(3:0)			
000F	RCC6	R/W	RCC3D(3:0)				RCC3C(3:0)			
0010	TBP1	R/W	TB4	TB3	TB2	TB1	RB4	RB3	RB2	RB1
0011-00EF	--	--	Not Used							
00F0	ID1	R	MI6=1	MI5=1	MI4=0	MI3=1	MI2=0	MI1=1	MI0=1	1
00F1	ID2	R	PN3=1	PN2=0	PN1=1	PN0=1	MI10=0	MI9=0	MI8=0	MI7=0
00F2	ID3	R	PN11=1	PN10=0	PN9=0	PN8=1	PN7=1	PN6=1	PN5=0	PN4=0
00F3	ID4	R	RN3=0	RN2=0	RN1=0	RN0=1	PN15=0	PN14=0	PN13=0	PN12=1
00F4	ID5	R	0	0	0	0	0	0	0	0
00F5-0FFF	--	--	Not Used							
y000	STAT1	R	LOPR	PAISR	LOPT	PAIST	PRDI	SLM	UNEQ	TIM
y001	STAT1_M	R/W	LOPR_M	PAISR_M	LOPT_M	PAIST_M	PRDI_M	SLM_M	UNEQ_M	TIM_M
y002	TEST	R	TEST							
y003-y1FF	--	--	Not Used							
y200	B3CNT	R	B3 Error Counter (lower 8-bits)							
y201	REICNT	R	REI Counter (lower 8-bits)							
y202	PJTCNT	R	+ PAT							
y203	NJTCNT	R	- PAT							
y204	PJRCNT	R	+ PAR							
y205	NJRCNT	R	- PAR							
y206-y3FE	--	--	Not Used							
y3FF	CHB	R	Common High Byte (for 16-bit counters)							
y400-y43F	TXJ1	R/W	TX J1 Buffer							
y440	--	--	Not Used							

Control and Status Registers (y=1,2,..B, C)

Virtual Address Offset (Hex)	Register Name	Access	Bit Names							
			7	6	5	4	3	2	1	0
y441	TXC2	R/W	TX C2 Byte							
y442	--	--	Not Used							
y443	TXF2	R/W	TX F2 Byte							
y444	TXH4	R/W	TX H4 Byte							
y445	TXF3	R/W	TX F3 Byte							
y446	TXN1	R/W	TX N1Byte							
y447	TXK3	R/W	TX K3 Byte							
y448	TXCNTL1	R/W	J1EN	B3EN	C2EN	G1EN	F2EN	F3EN	K3EN	N1EN
y449	TXCNTL2	R/W	--	--	--	--	--	--	H4M1	H4M0
y44A-y5FF	--	--	Not Used							
y600-y63F	RXJ1	R	RX J1 Buffer							
y640	RXB3	R	RX B3 Byte							
y641	RXC2	R	RX C2 Byte							
y642	RXG1	R	RX G1 Byte							
y643	RXF2	R	RX F2 Byte							
y644	RXH4	R	RX H4 Byte							
y645	RXF3	R	RX F3 Byte							
y646	RXN1	R	RX N1Byte							
y647	RXK3	R	RX K3 Byte							
y648-y68F	--	--	Not Used							
y690	EXC2	R/W	Expected C2 Byte							
y691	RXCNTL1	R/W	--	--	AZSPE	SLMEN	RV1EN	REIEN	C2PEN	TIMEN
y692-y6BF	--	--	Not Used.							
y6C0-y6FF	EXJ1	R/W	Expected J1 Message							
y700-yFFF	--	--	Not Used.							

R= Read only, R/W = Read and Write access.

CONTROL AND STATUS REGISTERS

GCNTL1 Register (0000H)

Bit Name	Bit Number	Default	Description
--	7-6	00	Not Used. These bits must always be written with a zero.
CPOST	5	0	0 = The pulse on the J0J1 input to the AUCC T block while the SPE input is low, is aligned to the $A2_3$ byte. If there is also a pulse on the J0J1 input that identifies the location of the J1 bytes, then the SPE signal must be high during those byte positions. 1 = The pulse on the J0J1 input to the AUCC T block while the SPE input is low, is aligned to the J0 byte. If there is also a pulse on the J0J1 input that identifies the location of the J1 bytes, then the SPE signal must be high during those byte positions.
DELAYT4 DELAYT3 DELAYT2 DELAYT1 DELAYT0	4 3 2 1 0	0 0 0 0 0	The AURT T blocks have a reference clock and frame input which is used to generate the output frame. The DELAYT bits are used to control the delay between the output J0 byte position and the reference frame input.

Start of AURT T Frame Reference

DELAYT4	DELAYT3	DELAYT2	DELAYT1	DELAYT0	Output J0 byte position with respect to the reference frame input (bytes)
0	0	0	0	0	1
0	0	0	0	1	4
0	0	0	1	0	7
0	0	0	1	1	10
0	0	1	0	0	13
0	0	1	0	1	16
0	0	1	1	0	19
0	0	1	1	1	Do Not Use
X	1	X	X	X	Do Not Use
1	X	X	X	X	Do Not Use.

GCNTL2 Register (0001H)

Bit Name	Bit Number	Default	Description
--	7-6	00	Not Used. These bits must always be written with a zero.
CPOSR	5	0	0 = The pulse on the J0J1 input to the AUCC R block while the SPE input is low, is aligned to the $A2_3$ byte. If there is also a pulse on the J0J1 input that identifies the location of the J1 bytes, then the SPE signal must be high during those byte positions. 1 = The pulse on the J0J1 input to the AUCC R block while the SPE input is low, is aligned to the J0 byte. If there is also a pulse on the J0J1 input that identifies the location of the J1 bytes, then the SPE signal must be high during those byte positions.

GCNTL2 Register (0001H)

Bit Name	Bit Number	Default	Description
DELAYR4	4	0	The AURT R blocks have a reference clock and frame input which is used to generate the output frame. The DELAYR bits are used to control the delay between the output J0 byte position and the reference frame input.
DELAYR3	3	0	
DELAYR2	2	0	
DELAYR1	1	0	
DELAYR0	0	0	

Start of AURT R Frame Reference

DELAYR4	DELAYR3	DELAYR2	DELAYR1	DELAYR0	Output J0 byte position with respect to the reference frame input (bytes)
0	0	0	0	0	1
0	0	0	0	1	4
0	0	0	1	0	7
0	0	0	1	1	10
0	0	1	0	0	13
0	0	1	0	1	16
0	0	1	1	0	19
0	0	1	1	1	Do Not Use
X	1	X	X	X	Do Not Use
1	X	X	X	X	Do Not Use.

FMT1 Register (0002H)

Bit Name	Bit Number	Default	Description
--	7	0	Not used. Always write a 0 to this bit.
FORMATB(2:0)	6	0	
	5	0	
	4	0	
--	3	0	Not used. Always write a 0 to this bit.

Format of TX and RX Telecom Bus B Data

FORMATB2	FORMATB1	FORMATB0	Description
0	0	0	STS-1-SPE (i.e. 3 byte interleaved STS-1-SPEs)
0	0	1	STS-3c-SPE
0	1	0	Reserved for Future Use.
0	1	1	Reserved for Future Use.
1	0	0	Reserved for Future Use.
1	0	1	VC-4
1	1	0	Reserved for Future Use.
1	1	1	Reserved for Future Use.

FMT1 Register (0002H)

Bit Name	Bit Number	Default	Description
FORMATA(2:0)	2 1 0	0 0 0	**Format of TX and RX Telecom Bus A Data**

FORMATA2	FORMATA1	FORMATA0	Description
0	0	0	STS-1-SPE (i.e., 3 byte interleaved STS-1-SPEs)
0	0	1	STS-3c-SPE
0	1	0	Reserved for Future Use.
0	1	1	Reserved for Future Use.
1	0	0	Reserved for Future Use.
1	0	1	VC-4
1	1	0	Reserved for Future Use.
1	1	1	Reserved for Future Use.

FMT2 Register (0003H)

Bit Name	Bit Number	Default	Description
--	7	0	Not used. Always write a 0 to this bit.
FORMATD(2:0)	6 5 4	0 0 0	**Format of TX and RX Telecom Bus D Data**
--	3	0	Not used. Always write a 0 to this bit.

FORMATD2	FORMATD1	FORMATD0	Description
0	0	0	STS-1-SPE (i.e. 3 byte interleaved STS-1-SPEs)
0	0	1	STS-3c-SPE
0	1	0	Reserved for Future Use.
0	1	1	Reserved for Future Use.
1	0	0	Reserved for Future Use.
1	0	1	VC-4
1	1	0	Reserved for Future Use.
1	1	1	Reserved for Future Use.

FMT2 Register (0003H)

Bit Name	Bit Number	Default	Description
FORMATC(2:0)	2	0	
	1	0	
	0	0	

Format of TX and RX Telecom Bus C Data

FORMATC2	FORMATC1	FORMATC0	Description
0	0	0	STS-1-SPE (i.e. 3 byte interleaved STS-1-SPEs)
0	0	1	STS-3c-SPE
0	1	0	Reserved for Future Use.
0	1	1	Reserved for Future Use.
1	0	0	Reserved for Future Use.
1	0	1	VC-4
1	1	0	Reserved for Future Use.
1	1	1	Reserved for Future Use.

1. Please note that for STM-1 or STS-3c applications TCC1-TCC6 and RCC1-RCC6 should be set to route the three slots from the input Telecom Bus together to the same output Telecom Bus.

TCC1 Register (0004H)

Bit Name	Bit Number	Default	Description
TCC1B3	7	0	
TCC1B2	6	0	
TCC1B1	5	0	
TCC1B0	4	0	

Source of Slot 1 Data for TX Telecom Bus 2

TCC1B3	TCC1B2	TCC1B1	TCC1B0	Description
0	0	0	0	TX TBT 1 Slot 1
0	0	0	1	TX TBT 1 Slot 2
0	0	1	0	TX TBT 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	TX TBT 2 Slot 1
0	1	0	1	TX TBT 2 Slot 2
0	1	1	0	TX TBT 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	TX TBT 3 Slot 1
1	0	0	1	TX TBT 3 Slot 2
1	0	1	0	TX TBT 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	TX TBT 4 Slot 1
1	1	0	1	TX TBT 4 Slot 2
1	1	1	0	TX TBT 4 Slot 3
1	1	1	1	Not used.

TCC1 Register (0004H)

Bit Name	Bit Number	Default	Description
TCC1A3	3	0	
TCC1A2	2	0	
TCC1A1	1	0	
TCC1A0	0	0	

Source of Slot 1 Data for TX Telecom Bus 1

TCC1A3	TCC1A2	TCC1A1	TCC1A0	Description
0	0	0	0	TX TBT 1 Slot 1
0	0	0	1	TX TBT 1 Slot 2
0	0	1	0	TX TBT 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	TX TBT 2 Slot 1
0	1	0	1	TX TBT 2 Slot 2
0	1	1	0	TX TBT 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	TX TBT 3 Slot 1
1	0	0	1	TX TBT 3 Slot 2
1	0	1	0	TX TBT 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	TX TBT 4 Slot 1
1	1	0	1	TX TBT 4 Slot 2
1	1	1	0	TX TBT 4 Slot 3
1	1	1	1	Not used.

TCC2 Register (0005H)

Bit Name	Bit Number	Default	Description
TCC1D3	7	0	
TCC1D2	6	0	
TCC1D1	5	0	
TCC1D0	4	0	

Source of Slot 1 Data for TX Telecom Bus 4

TCC1D3	TCC1D2	TCC1D1	TCC1S0	Description
0	0	0	0	TX TBT 1 Slot 1
0	0	0	1	TX TBT 1 Slot 2
0	0	1	0	TX TBT 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	TX TBT 2 Slot 1
0	1	0	1	TX TBT 2 Slot 2
0	1	1	0	TX TBT 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	TX TBT 3 Slot 1
1	0	0	1	TX TBT 3 Slot 2
1	0	1	0	TX TBT 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	TX TBT 4 Slot 1
1	1	0	1	TX TBT 4 Slot 2
1	1	1	0	TX TBT 4 Slot 3
1	1	1	1	Not used.

TCC2 Register (0005H)

Bit Name	Bit Number	Default	Description
TCC1C3	3	0	
TCC1C2	2	0	
TCC1C1	1	0	
TCC1C0	0	0	

Source of Slot 1 Data for TX Telecom Bus 3

TCC1C3	TCC1C2	TCC1C1	TCC1C0	Description
0	0	0	0	TX TBT 1 Slot 1
0	0	0	1	TX TBT 1 Slot 2
0	0	1	0	TX TBT 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	TX TBT 2 Slot 1
0	1	0	1	TX TBT 2 Slot 2
0	1	1	0	TX TBT 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	TX TBT 3 Slot 1
1	0	0	1	TX TBT 3 Slot 2
1	0	1	0	TX TBT 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	TX TBT 4 Slot 1
1	1	0	1	TX TBT 4 Slot 2
1	1	1	0	TX TBT 4 Slot 3
1	1	1	1	Not used.

TCC3 Register (0006H)

Bit Name	Bit Number	Default	Description
TCC2B3	7	0	
TCC2B2	6	0	
TCC2B1	5	0	
TCC2B0	4	0	

Source of Slot 2 Data for TX Telecom Bus 2

TCC2B3	TCC2B2	TCC2B1	TCC2B0	Description
0	0	0	0	TX TBT 1 Slot 1
0	0	0	1	TX TBT 1 Slot 2
0	0	1	0	TX TBT 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	TX TBT 2 Slot 1
0	1	0	1	TX TBT 2 Slot 2
0	1	1	0	TX TBT 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	TX TBT 3 Slot 1
1	0	0	1	TX TBT 3 Slot 2
1	0	1	0	TX TBT 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	TX TBT 4 Slot 1
1	1	0	1	TX TBT 4 Slot 2
1	1	1	0	TX TBT 4 Slot 3
1	1	1	1	Not used.

TCC3 Register (0006H)

Bit Name	Bit Number	Default	Description
TCC2A3	3	0	
TCC2A2	2	0	
TCC2A1	1	0	
TCC2A0	0	0	

Source of Slot 2 Data for TX Telecom Bus 1

TCC2A3	TCC2A2	TCC2A1	TCC2A0	Description
0	0	0	0	TX TBT 1 Slot 1
0	0	0	1	TX TBT 1 Slot 2
0	0	1	0	TX TBT 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	TX TBT 2 Slot 1
0	1	0	1	TX TBT 2 Slot 2
0	1	1	0	TX TBT 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	TX TBT 3 Slot 1
1	0	0	1	TX TBT 3 Slot 2
1	0	1	0	TX TBT 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	TX TBT 4 Slot 1
1	1	0	1	TX TBT 4 Slot 2
1	1	1	0	TX TBT 4 Slot 3
1	1	1	1	Not used.

TCC4 Register (0007H)

Bit Name	Bit Number	Default	Description
TCC2D3 TCC2D2 TCC2D1 TCC2D0	7 6 5 4	0 0 0 0	**Source of Slot 2 Data for TX Telecom Bus 4**
TCC2C3 TCC2C2 TCC2C1 TCC2C0	3 2 1 0	0 0 0 0	**Source of Slot 2 Data for TX Telecom Bus 3**

Source of Slot 2 Data for TX Telecom Bus 4

TCC2D3	TCC2D2	TCC2D1	TCC2S0	Description
0	0	0	0	TX TBT 1 Slot 1
0	0	0	1	TX TBT 1 Slot 2
0	0	1	0	TX TBT 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	TX TBT 2 Slot 1
0	1	0	1	TX TBT 2 Slot 2
0	1	1	0	TX TBT 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	TX TBT 3 Slot 1
1	0	0	1	TX TBT 3 Slot 2
1	0	1	0	TX TBT 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	TX TBT 4 Slot 1
1	1	0	1	TX TBT 4 Slot 2
1	1	1	0	TX TBT 4 Slot 3
1	1	1	1	Not used.

Source of Slot 2 Data for TX Telecom Bus 3

TCC2C3	TCC2C2	TCC2C1	TCC2C0	Description
0	0	0	0	TX TBT 1 Slot 1
0	0	0	1	TX TBT 1 Slot 2
0	0	1	0	TX TBT 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	TX TBT 2 Slot 1
0	1	0	1	TX TBT 2 Slot 2
0	1	1	0	TX TBT 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	TX TBT 3 Slot 1
1	0	0	1	TX TBT 3 Slot 2
1	0	1	0	TX TBT 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	TX TBT 4 Slot 1
1	1	0	1	TX TBT 4 Slot 2
1	1	1	0	TX TBT 4 Slot 3
1	1	1	1	Not used.

TCC5 Register (0008H)

Bit Name	Bit Number	Default	Description
TCC3B3 TCC3B2 TCC3B1 TCC3B0	7 6 5 4	0 0 0 0	**Source of Slot 3 Data for TX Telecom Bus 2**
TCC3A3 TCC3A2 TCC3A1 TCC3A0	3 2 1 0	0 0 0 0	**Source of Slot 3 Data for TX Telecom Bus 1**

Source of Slot 3 Data for TX Telecom Bus 2

TCC3B3	TCC3B2	TCC3B1	TCC3B0	Description
0	0	0	0	TX TBT 1 Slot 1
0	0	0	1	TX TBT 1 Slot 2
0	0	1	0	TX TBT 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	TX TBT 2 Slot 1
0	1	0	1	TX TBT 2 Slot 2
0	1	1	0	TX TBT 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	TX TBT 3 Slot 1
1	0	0	1	TX TBT 3 Slot 2
1	0	1	0	TX TBT 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	TX TBT 4 Slot 1
1	1	0	1	TX TBT 4 Slot 2
1	1	1	0	TX TBT 4 Slot 3
1	1	1	1	Not used.

Source of Slot 3 Data for TX Telecom Bus 1

TCC3A3	TCC3A2	TCC3A1	TCC3A0	Description
0	0	0	0	TX TBT 1 Slot 1
0	0	0	1	TX TBT 1 Slot 2
0	0	1	0	TX TBT 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	TX TBT 2 Slot 1
0	1	0	1	TX TBT 2 Slot 2
0	1	1	0	TX TBT 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	TX TBT 3 Slot 1
1	0	0	1	TX TBT 3 Slot 2
1	0	1	0	TX TBT 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	TX TBT 4 Slot 1
1	1	0	1	TX TBT 4 Slot 2
1	1	1	0	TX TBT 4 Slot 3
1	1	1	1	Not used.

TCC6 Register (0009H)

<table>
<tr><th>Bit Name</th><th>Bit Number</th><th>Default</th><th>Description</th></tr>
<tr><td>TCC3D3
TCC3D2
TCC3D1
TCC3D0</td><td>7
6
5
4</td><td>0
0
0
0</td><td>
Source of Slot 3 Data for TX Telecom Bus 4
<table>
<tr><th>TCC3D3</th><th>TCC3D2</th><th>TCC3D1</th><th>TCC3S0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>TX TBT 1 Slot 1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>TX TBT 1 Slot 2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>TX TBT 1 Slot 3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Not used.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>TX TBT 2 Slot 1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>TX TBT 2 Slot 2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>TX TBT 2 Slot 3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Not used.</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>TX TBT 3 Slot 1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>TX TBT 3 Slot 2</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>TX TBT 3 Slot 3</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>Not used.</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>TX TBT 4 Slot 1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>TX TBT 4 Slot 2</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>TX TBT 4 Slot 3</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Not used.</td></tr>
</table>
</td></tr>
<tr><td>TCC3C3
TCC3C2
TCC3C1
TCC3C0</td><td>3
2
1
0</td><td>0
0
0
0</td><td>
Source of Slot 3 Data for TX Telecom Bus 3
<table>
<tr><th>TCC3C3</th><th>TCC3C2</th><th>TCC3C1</th><th>TCC3C0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>TX TBT 1 Slot 1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>TX TBT 1 Slot 2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>TX TBT 1 Slot 3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Not used.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>TX TBT 2 Slot 1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>TX TBT 2 Slot 2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>TX TBT 2 Slot 3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Not used.</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>TX TBT 3 Slot 1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>TX TBT 3 Slot 2</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>TX TBT 3 Slot 3</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>Not used.</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>TX TBT 4 Slot 1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>TX TBT 4 Slot 2</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>TX TBT 4 Slot 3</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Not used.</td></tr>
</table>
</td></tr>
</table>

RCC1 Register (000AH)

Bit Name	Bit Number	Default	Description
RCC1B3 RCC1B2 RCC1B1 RCC1B0	7 6 5 4	0 0 0 0	**Source of Slot 1 Data for RX Telecom Bus 2**
RCC1A3 RCC1A2 RCC1A1 RCC1A0	3 2 1 0	0 0 0 0	**Source of Slot 1 Data for RX Telecom Bus 1**

Source of Slot 1 Data for RX Telecom Bus 2

RCC1B3	RCC1B2	RCC1B1	RCC1B0	Description
0	0	0	0	RX TBCC 1 Slot 1
0	0	0	1	RX TBCC 1 Slot 2
0	0	1	0	RX TBCC 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	RX TBCC 2 Slot 1
0	1	0	1	RX TBCC 2 Slot 2
0	1	1	0	RX TBCC 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	RX TBCC 3 Slot 1
1	0	0	1	RX TBCC 3 Slot 2
1	0	1	0	RX TBCC 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	RX TBCC 4 Slot 1
1	1	0	1	RX TBCC 4 Slot 2
1	1	1	0	RX TBCC 4 Slot 3
1	1	1	1	Not used.

Source of Slot 1 Data for RX Telecom Bus 1

RCC1A3	RCC1A2	RCC1A1	RCC1A0	Description
0	0	0	0	RX TBCC 1 Slot 1
0	0	0	1	RX TBCC 1 Slot 2
0	0	1	0	RX TBCC 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	RX TBCC 2 Slot 1
0	1	0	1	RX TBCC 2 Slot 2
0	1	1	0	RX TBCC 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	RX TBCC 3 Slot 1
1	0	0	1	RX TBCC 3 Slot 2
1	0	1	0	RX TBCC 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	RX TBCC 4 Slot 1
1	1	0	1	RX TBCC 4 Slot 2
1	1	1	0	RX TBCC 4 Slot 3
1	1	1	1	Not used.

RCC2 Register (000BH)

<table>
<tr><th>Bit Name</th><th>Bit Number</th><th>Default</th><th>Description</th></tr>
<tr><td>RCC1D3
RCC1D2
RCC1D1
RCC1D0</td><td>7
6
5
4</td><td>0
0
0
0</td><td>
Source of Slot 1 Data for RX Telecom Bus 4
<table>
<tr><th>RCC1D3</th><th>RCC1D2</th><th>RCC1D1</th><th>RCC1S0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>RX TBCC 1 Slot 1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>RX TBCC 1 Slot 2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>RX TBCC 1 Slot 3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Not used.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>RX TBCC 2 Slot 1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>RX TBCC 2 Slot 2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>RX TBCC 2 Slot 3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Not used.</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>RX TBCC 3 Slot 1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>RX TBCC 3 Slot 2</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>RX TBCC 3 Slot 3</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>Not used.</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>RX TBCC 4 Slot 1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>RX TBCC 4 Slot 2</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>RX TBCC 4 Slot 3</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Not used.</td></tr>
</table>
</td></tr>
<tr><td>RCC1C3
RCC1C2
RCC1C1
RCC1C0</td><td>3
2
1
0</td><td>0
0
0
0</td><td>
Source of Slot 1 Data for RX Telecom Bus 3
<table>
<tr><th>RCC1C3</th><th>RCC1C2</th><th>RCC1C1</th><th>RCC1C0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>RX TBCC 1 Slot 1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>RX TBCC 1 Slot 2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>RX TBCC 1 Slot 3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Not used.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>RX TBCC 2 Slot 1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>RX TBCC 2 Slot 2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>RX TBCC 2 Slot 3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Not used.</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>RX TBCC 3 Slot 1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>RX TBCC 3 Slot 2</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>RX TBCC 3 Slot 3</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>Not used.</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>RX TBCC 4 Slot 1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>RX TBCC 4 Slot 2</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>RX TBCC 4 Slot 3</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Not used.</td></tr>
</table>
</td></tr>
</table>

RCC3 Register (000CH)

Bit Name	Bit Number	Default	Description
RCC2B3 RCC2B2 RCC2B1 RCC2B0	7 6 5 4	0 0 0 0	**Source of Slot 2 Data for RX Telecom Bus 2**
RCC2A3 RCC2A2 RCC2A1 RCC2A0	3 2 1 0	0 0 0 0	**Source of Slot 2 Data for RX Telecom Bus 1**

Source of Slot 2 Data for RX Telecom Bus 2

RCC2B3	RCC2B2	RCC2B1	RCC2B0	Description
0	0	0	0	RX TBCC 1 Slot 1
0	0	0	1	RX TBCC 1 Slot 2
0	0	1	0	RX TBCC 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	RX TBCC 2 Slot 1
0	1	0	1	RX TBCC 2 Slot 2
0	1	1	0	RX TBCC 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	RX TBCC 3 Slot 1
1	0	0	1	RX TBCC 3 Slot 2
1	0	1	0	RX TBCC 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	RX TBCC 4 Slot 1
1	1	0	1	RX TBCC 4 Slot 2
1	1	1	0	RX TBCC 4 Slot 3
1	1	1	1	Not used.

Source of Slot 2 Data for RX Telecom Bus 1

RCC2A3	RCC2A2	RCC2A1	RCC2A0	Description
0	0	0	0	RX TBCC 1 Slot 1
0	0	0	1	RX TBCC 1 Slot 2
0	0	1	0	RX TBCC 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	RX TBCC 2 Slot 1
0	1	0	1	RX TBCC 2 Slot 2
0	1	1	0	RX TBCC 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	RX TBCC 3 Slot 1
1	0	0	1	RX TBCC 3 Slot 2
1	0	1	0	RX TBCC 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	RX TBCC 4 Slot 1
1	1	0	1	RX TBCC 4 Slot 2
1	1	1	0	RX TBCC 4 Slot 3
1	1	1	1	Not used.

RCC4 Register (000DH)

Bit Name	Bit Number	Default	Description
RCC2D3 RCC2D2 RCC2D1 RCC2D0	7 6 5 4	0 0 0 0	**Source of Slot 2 Data for RX Telecom Bus 4**
RCC2C3 RCC2C2 RCC2C1 RCC2C0	3 2 1 0	0 0 0 0	**Source of Slot 2 Data for RX Telecom Bus 3**

Source of Slot 2 Data for RX Telecom Bus 4

RCC2D3	RCC2D2	RCC2D1	RCC2S0	Description
0	0	0	0	RX TBCC 1 Slot 1
0	0	0	1	RX TBCC 1 Slot 2
0	0	1	0	RX TBCC 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	RX TBCC 2 Slot 1
0	1	0	1	RX TBCC 2 Slot 2
0	1	1	0	RX TBCC 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	RX TBCC 3 Slot 1
1	0	0	1	RX TBCC 3 Slot 2
1	0	1	0	RX TBCC 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	RX TBCC 4 Slot 1
1	1	0	1	RX TBCC 4 Slot 2
1	1	1	0	RX TBCC 4 Slot 3
1	1	1	1	Not used.

Source of Slot 2 Data for RX Telecom Bus 3

RCC2C3	RCC2C2	RCC2C1	RCC2C0	Description
0	0	0	0	RX TBCC 1 Slot 1
0	0	0	1	RX TBCC 1 Slot 2
0	0	1	0	RX TBCC 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	RX TBCC 2 Slot 1
0	1	0	1	RX TBCC 2 Slot 2
0	1	1	0	RX TBCC 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	RX TBCC 3 Slot 1
1	0	0	1	RX TBCC 3 Slot 2
1	0	1	0	RX TBCC 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	RX TBCC 4 Slot 1
1	1	0	1	RX TBCC 4 Slot 2
1	1	1	0	RX TBCC 4 Slot 3
1	1	1	1	Not used.

RCC5 Register (000EH)

Bit Name	Bit Number	Default	Description
RCC3B3 RCC3B2 RCC3B1 RCC3B0	7 6 5 4	0 0 0 0	**Source of Slot 3 Data for RX Telecom Bus 2**
RCC3A3 RCC3A2 RCC3A1 RCC3A0	3 2 1 0	0 0 0 0	**Source of Slot 3 Data for RX Telecom Bus 1**

Source of Slot 3 Data for RX Telecom Bus 2

RCC3B3	RCC3B2	RCC3B1	RCC3B0	Description
0	0	0	0	RX TBCC 1 Slot 1
0	0	0	1	RX TBCC 1 Slot 2
0	0	1	0	RX TBCC 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	RX TBCC 2 Slot 1
0	1	0	1	RX TBCC 2 Slot 2
0	1	1	0	RX TBCC 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	RX TBCC 3 Slot 1
1	0	0	1	RX TBCC 3 Slot 2
1	0	1	0	RX TBCC 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	RX TBCC 4 Slot 1
1	1	0	1	RX TBCC 4 Slot 2
1	1	1	0	RX TBCC 4 Slot 3
1	1	1	1	Not used.

Source of Slot 3 Data for RX Telecom Bus 1

RCC3A3	RCC3A2	RCC3A1	RCC3A0	Description
0	0	0	0	RX TBCC 1 Slot 1
0	0	0	1	RX TBCC 1 Slot 2
0	0	1	0	RX TBCC 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	RX TBCC 2 Slot 1
0	1	0	1	RX TBCC 2 Slot 2
0	1	1	0	RX TBCC 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	RX TBCC 3 Slot 1
1	0	0	1	RX TBCC 3 Slot 2
1	0	1	0	RX TBCC 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	RX TBCC 4 Slot 1
1	1	0	1	RX TBCC 4 Slot 2
1	1	1	0	RX TBCC 4 Slot 3
1	1	1	1	Not used.

RCC6 Register (000FH)

Bit Name	Bit Number	Default	Description
RCC3D3 RCC3D2 RCC3D1 RCC3D0	7 6 5 4	0 0 0 0	**Source of Slot 3 Data for RX Telecom Bus 4**
RCC3C3 RCC3C2 RCC3C1 RCC3C0	3 2 1 0	0 0 0 0	**Source of Slot 3 Data for RX Telecom Bus 3**

Source of Slot 3 Data for RX Telecom Bus 4

RCC3D3	RCC3D2	RCC3D1	RCC3S0	Description
0	0	0	0	RX TBCC 1 Slot 1
0	0	0	1	RX TBCC 1 Slot 2
0	0	1	0	RX TBCC 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	RX TBCC 2 Slot 1
0	1	0	1	RX TBCC 2 Slot 2
0	1	1	0	RX TBCC 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	RX TBCC 3 Slot 1
1	0	0	1	RX TBCC 3 Slot 2
1	0	1	0	RX TBCC 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	RX TBCC 4 Slot 1
1	1	0	1	RX TBCC 4 Slot 2
1	1	1	0	RX TBCC 4 Slot 3
1	1	1	1	Not used.

Source of Slot 3 Data for RX Telecom Bus 3

RCC3C3	RCC3C2	RCC3C1	RCC3C0	Description
0	0	0	0	RX TBCC 1 Slot 1
0	0	0	1	RX TBCC 1 Slot 2
0	0	1	0	RX TBCC 1 Slot 3
0	0	1	1	Not used.
0	1	0	0	RX TBCC 2 Slot 1
0	1	0	1	RX TBCC 2 Slot 2
0	1	1	0	RX TBCC 2 Slot 3
0	1	1	1	Not used.
1	0	0	0	RX TBCC 3 Slot 1
1	0	0	1	RX TBCC 3 Slot 2
1	0	1	0	RX TBCC 3 Slot 3
1	0	1	1	Not used.
1	1	0	0	RX TBCC 4 Slot 1
1	1	0	1	RX TBCC 4 Slot 2
1	1	1	0	RX TBCC 4 Slot 3
1	1	1	1	Not used.

BP Register (0010H)

Bit Name	Bit Number	Default	Description
TB4 TB3 TB2 TB1	7 6 5 4	0 0 0 0	Transmit Retimer Bypass Control: 0= The Pointer Tracking State Machines in the corresponding TX Telecom Bus are used. A valid pointer byte and valid framing pulse are required. The SPE signal should be 0 during the frame pulse and high during the J1 pulses. The J1 pulses are ignored. 1= The Pointer Tracking State Machines in the corresponding TX Telecom Bus are bypassed. Valid pointer bytes are not needed. However, a valid SPE, and J0J1 are required.
RB4 RB3 RB2 RB1	3 2 1 0	0 0 0 0	Receive Retimer Bypass Control: 0= The Pointer Tracking State Machines in the corresponding RX Telecom Bus are used. A valid pointer byte and valid framing pulse are required. The SPE signal should be 0 during the frame pulse and high during the J1 pulses. The J1 pulses are ignored. 1= The Pointer Tracking State Machines in the corresponding RX Telecom Bus are bypassed. Valid pointer bytes are not needed. However, a valid SPE, and J0J1 are required.

ID Registers (00F0H - 00F4H)

Description
The manufacturers ID (MI), part number (PN), and revision number (RN) are included in these registers. The manufacturer's ID for TranSwitch is 06BH. The part number for the POP-12 is 06603 = 19CBH.

STAT1 Register (y000H)[a]

Bit Name	Bit Number	Default	Description
LOPR	7	--	The definition of this bit depends on the format selected through the format bits and which POP function is being read and the setting of the RCCxz(3:0) bits as follows: **Definition of LOPR bit** RCCxz3 / RCCxz2 / RCCxz1 / RCCxz0 / Definition 0 0 0 0 — **STS-3:** Loss of Pointer in STS-1 number 1 of the RX AURT in Telecom Bus A is routed to POP function x of Telecom Bus z. STS-1 1-3 are in Telecom Bus A, STS-1 4-6 are in Telecom Bus B, etc. **STM-1/STS-3C:** Loss of pointer in STS-3c from telecom bus A is routed to POP-function x of Telecom Bus Z. 0 0 0 1 — **STS-3:** Loss of Pointer in STS-1 number 2 of the RX AURT in Telecom Bus A is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Ignore this bit. 0 0 1 0 — **STS-3:** Loss of Pointer in STS-1 number 3 of the RX AURT in Telecom Bus A is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Ignore this bit. 0 1 0 0 — **STS-3:** Loss of Pointer in STS-1 number 1 of the RX AURT in Telecom Bus B is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Loss of pointer in STS-3c from telecom bus B is routed to POP-function x of Telecom Bus Z. 0 1 0 1 — **STS-3:** Loss of Pointer in STS-1 number 2 of the RX AURT in Telecom Bus B is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Ignore this bit. 0 1 1 0 — **STS-3:** Loss of Pointer in STS-1 number 3 of the RX AURT in Telecom Bus B is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Ignore this bit. 1 0 0 0 — **STS-3:** Loss of Pointer in STS-1 number 1 of the RX AURT in Telecom Bus C is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Loss of pointer in STS-3c from telecom bus C is routed to POP-function x of Telecom Bus Z. 1 0 0 1 — **STS-3:** Loss of Pointer in STS-1 number 2 of the RX AURT in Telecom Bus C is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Ignore this bit. 1 0 1 0 — **STS-3:** Loss of Pointer in STS-1 number 3 of the RX AURT in Telecom Bus C is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Ignore this bit. 1 1 0 0 — **STS-3:** Loss of Pointer in STS-1 number 1 of the RX AURT in Telecom Bus D is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Loss of pointer in STS-3c from telecom bus D is routed to POP-function x of Telecom Bus Z. 1 1 0 1 — **STS-3:** Loss of Pointer in STS-1 number 2 of the RX AURT in Telecom Bus D is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Ignore this bit. 1 1 1 0 — **STS-3:** Loss of Pointer in STS-1 number 3 of the RX AURT in Telecom Bus D is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Ignore this bit. X X 1 1 — Invalid setting, do not use. This bit should be ignored when the corresponding RX PTSM is bypassed. Note: y=1 if xz=1A, y=2 if xz=2A,.... y=B if xz=2D, y=C if xz=3D. This is because the LOPR and AISR alarms are routed through the RX AUCC to the corresponding POP Function.

STAT1 Register (y000H)[a]

Bit Name	Bit Number	Default	Description
PAISR	6	--	The definition of this bit depends on the format selected through the format bits and which POP function is being read and the setting of the RCCxz(3:0) bits as follows: **Definition of PAISR bit** This bit should be ignored when the corresponding RX PTSM is bypassed. Note: y=1 if xz=1A, y=2 if xz=2A,.... y=B if xz=2D, y=C if xz=3D. This is because the LOPR and AISR alarms are routed through the RX AUCC to the corresponding POP Function.

Definition of PAISR bit

RCCxz3	RCCxz2	RCCxz1	RCCxz0	Definition
0	0	0	0	**STS-3:** Path AIS in STS-1 number 1 of the RX AURT in Telecom Bus A is routed to POP function x of Telecom Bus z. STS-1 1-3 are in Telecom Bus A, STS-1 4-6 are in Telecom Bus B, etc. **STM-1/STS-3C:** Path AIS in STS-3c from telecom bus A is routed to POP-function x of Telecom Bus Z.
0	0	0	1	**STS-3:** Path AIS in STS-1 number 2 of the RX AURT in Telecom Bus A is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Ignore this bit.
0	0	1	0	**STS-3:** Path AIS in STS-1 number 3 of the RX AURT in Telecom Bus A is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Ignore this bit.
0	1	0	0	**STS-3:** Path AIS in STS-1 number 1 of the RX AURT in Telecom Bus B is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Path AIS in STS-3c from telecom bus B is routed to POP-function x of Telecom Bus Z.
0	1	0	1	**STS-3:** Path AIS in STS-1 number 2 of the RX AURT in Telecom Bus B is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Ignore this bit.
0	1	1	0	**STS-3:** Path AIS in STS-1 number 3 of the RX AURT in Telecom Bus B is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Ignore this bit.
1	0	0	0	**STS-3:** Path AIS in STS-1 number 1 of the RX AURT in Telecom Bus C is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Path AIS in STS-3c from telecom bus C is routed to POP-function x of Telecom Bus Z.
1	0	0	1	**STS-3:** Path AIS in STS-1 number 2 of the RX AURT in Telecom Bus C is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Ignore this bit.
1	0	1	0	**STS-3:** Path AIS in STS-1 number 3 of the RX AURT in Telecom Bus C is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Ignore this bit.
1	1	0	0	**STS-3:** Path AIS in STS-1 number 1 of the RX AURT in Telecom Bus D is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Path AIS in STS-3c from telecom bus D is routed to POP-function x of Telecom Bus Z.
1	1	0	1	**STS-3:** Path AIS in STS-1 number 2 of the RX AURT in Telecom Bus D is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Ignore this bit.
1	1	1	0	**STS-3:** Path AIS in STS-1 number 3 of the RX AURT in Telecom Bus D is routed to POP function x of Telecom Bus z. **STM-1/STS-3C:** Ignore this bit.
X	X	1	1	Invalid setting, do not use.

STAT1 Register (y000H)[a]

Bit Name	Bit Number	Default	Description
LOPT	5	--	The definition of this bit depends on the format selected through the format bits and which POP function is being read as follows: **Definition of LOPT bit** FORMATB(2:0) = STS-1-SPE: Loss of Pointer in STS-1 number y of the AURT T. STS-1 1-3 are in Telecom Bus A, STS-1 4-6 are in Telecom Bus B, etc. FORMATB(2:0) = STS-3C-SPE/VC-4: Loss of AU-4 Pointer detected in the AURT T. Valid only for y = 1, 4, 7, 10. This bit should be ignored when the corresponding TX PTSM is bypassed.
PAIST	4	--	The definition of this bit depends on the format selected through the format bits as follows: **Definition of PAIST bit** FORMATB(2:0) = STS-1-SPE: Path AIS in STS-1 number y of the AURT T. STS-1 1-3 are in Telecom Bus A, STS-1 4-6 are in Telecom Bus B, etc. FORMATB(2:0) = STS-3C-SPE/VC-4: Path AIS detected in the AURT T. Valid only for y = 1, 4, 7, 10. This bit should be ignored when the corresponding TX PTSM is bypassed.
PRDI	3	0	VC-4 Mode: 0= Bit 5 of the RX G1 byte is detected as 0, for 10 consecutive frames or LOP or Path AIS have been detected. 1= Bit 5 of the RX G1 byte is detected as 1, for 10 consecutive frames in the absence of LOP and Path AIS. STS-3c-SPE/STS-1-SPE Mode: 0= Bits 5-7 of the RX G1 byte is detected as 000, 001, or 011 for 10 consecutive frames or LOP or Path AIS have been detected. 1= Bits 5-7 of the RX G1 byte is detected as 010, 100, 101, 110, or 111 for 10 consecutive frames in the absence of LOP and Path AIS. For VC-4 or STS-3c modes this bit is only valid for the POH processors 1, 4, 7, and 10.
SLM	2	0	0= Either the **C2PEN** bit is set to 0, or the **C2PEN** bit is set to 1 and the RX C2 bytes match the contents of the EXC2 register or 01H for 5 consecutive frames. 1= The RX C2 bytes do not match the contents of the EXC2 register or 01H for 5 consecutive frames. For VC-4 or STS-3c modes this bit is only valid for the POH processors 1, 4, 7, and 10.
UNEQ	1	0	0= Either the **C2PEN** bit is set to 0, or the **C2PEN** bit is set to 1 and the RX C2 bytes are set to a value other than 00H for 5 consecutive frames. 1= The RX C2 bytes are received as 00H for 5 consecutive frames. For VC-4 or STS-3c modes this bit is only valid for the POH processors 1, 4, 7, and 10.
TIM	0	0	0= Either the **TIMEN** bit is set to 0 or the **TIMEN** bit is set to 1 and the RX J1 message has 1 or less errors out of 64 bytes, after 64 bytes with no errors have been received. 1= The RX J1 message has 2 or more bytes in error out of 64 bytes. For VC-4 or STS-3c modes this bit is only valid for the POH processors 1, 4, 7, and 10.

a. The bits in the STAT1 registers are latched bits and clear on read. If the alarm is still present the corresponding bit will become set again.

STAT1_M Register (y001H)

Bit Name	Bit Number	Default	Description
LOPR_M	7	0	Interrupt mask bit.
PAISR_M	6	0	0 = Interrupt signal not sent to the microprocessor if the corresponding bit in STAT1 register is 1.
LOPT_M	5	0	1 = Interrupt signal sent to the microprocessor if the corresponding bit in STAT1 register is 1.
PAIST_M	4	0	These bits are AND gated with the corresponding bit in the STAT1 register, the resulting signals are OR gated together, and the resulting signal is sent to the INT/IRQ lead with the appropriate polarity based upon the state of the MOTO lead.
PRDI_M	3	0	
SLM_M	2	0	
UNEQ_M	1	0	
TIM_M	0	0	

TEST (y002H)

Bit Name	Bit Number	Default	Description
--	7-0	--	These are test bits for internal TranSwitch use only.

B3 Error Counter (y200H)

Bit Name	Bit Number	Default	Description
B3CNT	7-0	--	When this register is read, the lower 8-bits of the 16-bit B3 Error Count is returned. The upper 8-bits can then be read from 0ffset y3FFH.

REI Error Counter (y201H)

Bit Name	Bit Number	Default	Description
REICNT	7-0	--	When this register is read, the lower 8-bits of the 16-bit of received REI Count is returned. The upper 8-bits can then be read from 0ffset y3FFH. This counter is enabled when the **REIEN** bit is set to a 1.

+PAT Counter (y202H)

Bit Name	Bit Number	Default	Description
PJTCNT	7-0	--	Count of positive pointer justifications input to the AURT T. This is an 8-bit counter. The value of this counter is not valid when the corresponding TX PTSM is bypassed.

-PAT Counter (y203H)

Bit Name	Bit Number	Default	Description
NJTCNT	7-0	--	Count of negative pointer justifications input to the AURT T. This is an 8-bit counter. The value of this counter is not valid when the corresponding TX PTSM is bypassed.

+PAR Counter (y204H)

Bit Name	Bit Number	Default	Description
PJRCNT	7-0	--	Count of positive pointer justifications input to the AURT R. This is an 8-bit counter. The value of this counter is not valid when the corresponding RX PTSM is bypassed.

-PAR Counter (y205H)

Bit Name	Bit Number	Default	Description
PJRCNT	7-0	--	Count of positive pointer justifications input to the AURT R. This is an 8-bit counter. The value of this counter is not valid when the corresponding RX PTSM is bypassed.

Common High Byte (y3FFH)

Bit Name	Bit Number	Default	Description
CHB	7-0	--	Upper 8-bits of 16-bit counters are stored in this register when their lower 8-bits are read.

TXJ1 (y400H-y43FH)

Bit Name	Bit Number	Default	Description
TX J1 Buffer	7-0	00	This 64-byte buffer is continuously transmitted in the J1 byte stream when the **J1EN** bit is set to 1. For applications requiring a repeating 16 byte message, the message can be repeated in this buffer four times.

TXC2 (y441H)

Bit Name	Bit Number	Default	Description
TXC2	7-0	00	The contents of this register is continuously transmitted in the C2 byte stream when the **C2EN** bit is set to 1; otherwise the C2 byte from the Telecom Bus is passed through.

TXF2 (y443H)

Bit Name	Bit Number	Default	Description
TXF2	7-0	00	The contents of this register is continuously transmitted in the F2 byte stream when the **F2EN** bit is set to 1; otherwise the F2 byte from the Telecom Bus is passed through.

TXH4 (y444H)

Bit Name	Bit Number	Default	Description
TXH4	7-0	00	The contents of this register is continuously transmitted in the H4 byte stream when the **H4M(1:0)** bits are set to 01. If the **H4M(1:0)** bits are set to 00 the H4 byte from the Telecom Bus is passed through. If the **H4M(1:0)** bits are set to 1X then the H4 is internally generated as a multiframe indicator and is synchronized to the V1 pulse on the TX Telecom Bus.

TXF3 (y445H)

Bit Name	Bit Number	Default	Description
TXF3	7-0	00	The contents of this register is continuously transmitted in the F3 byte stream when the **F3EN** bit is set to 1; otherwise the F3 byte from the Telecom Bus is passed through.

TXN1 (y446H)

Bit Name	Bit Number	Default	Description
TXN1	7-0	00	The contents of this register is continuously transmitted in the N1 byte stream when the **N1EN** bit is set to 1; otherwise the N1 byte from the Telecom Bus is passed through.

TXK3 (y447H)

Bit Name	Bit Number	Default	Description
TXK3	7-0	00	The contents of this register is continuously transmitted in the K3 byte stream when the **K3EN** bit is set to 1; otherwise the K3 byte from the Telecom Bus is passed through.

For STM-1 and STS-3c modes the TXCNTL1 bits for POH processors 2, 3, 5, 6, 8, 9, 11, and 12 should be set to FFH and the corresponding TX POH bytes set to 00H. Also, when TX path AIS is being generated due to the detection of TX LOP or TX Path AIS, and one of the bits in the TXCNTL1 register is set to a 1, then that POH byte will be overwritten with the POH RAM value or processed value and transmitted. The TX H1H2 bytes will still be all 1s. To be sure that the POH bytes are transmitted as FFH in that case, an FFH should be written at that time to the POH byte registers, and then returned back to their previous settings at the end of the alarm condition. The situations where this has to be done is rare since the PTSM is generally always bypassed in the TX direction.

TXCNTL1 (y448H)

Bit Name	Bit Number	Default	Description
J1EN	7	0	0=J1 from Telecom Bus is passed through. 1=J1 from TXJ1 buffer is transmitted.
B3EN	6	0	0=B3 from Telecom Bus is passed through. 1=B3 is calculated and inserted.
C2EN	5	0	0=C2 from Telecom Bus is passed through. 1=C2 from TXC2 register is transmitted.
G1EN	4	0	0=G1 from Telecom Bus is passed through. 1=G1 is derived from RX side alarms and errors. Bits 5-8 are transmitted as 0000 in SDH mode when no RX side alarms are detected. Bits 5-8 are transmitted as 0010 in SONET mode when no RX side alarms are detected.
F2EN	3	0	0=F2 from Telecom Bus is passed through. 1=F2 from TXF2 register is transmitted.
F3EN	2	0	0=F3 from Telecom Bus is passed through. 1=F3 from TXF3 register is transmitted.
K3EN	1	0	0=K3 from Telecom Bus is passed through. 1=K3 from TXK3 register is transmitted.
N1EN	0	0	0=N1 from Telecom Bus is passed through. 1=N1 from TXN1 register is transmitted.

For STM-1 and STS-3c modes the TXCNTL2 bits for POH processors 2, 3, 5, 6, 8, 9, 11, and 12 should be set to 01H and the corresponding TX H4 bytes set to 00H.

TXCNTL2 (y449H)

Bit Name	Bit Number	Default	Description
--	7-2	000000	Not used. These bits must always be written with 0s.

TXCNTL2 (y449H)

Bit Name	Bit Number	Default	Description
H4M1 H4M0	1 0	0 0	

H4M1	H4M0	Operation
0	0	H4 from Telecom Bus is passed through.
0	1	H4 from TXH4 register is transmitted.
1	X	H4 is synchronized to external V1 pulse on the Telecom Bus J0J1 signal and is internally generated and transmitted as a multiframe indicator.

RXJ1 (y600H-y63FH)

Bit Name	Bit Number	Default	Description
RX J1 Buffer	7-0	--	This 64 byte buffer contains the received J1 Path Trace bytes as received, in circular fashion when the corresponding **TIMEN** bit is set to 0. When the **TIMEN** bit is set to 1, and a match is found between the received J1 message and the corresponding RX Expected J1message, then the received J1 bytes are written into this buffer aligned to the RX Expected J1 message with a one byte shift. i.e. the first byte of the message is written into y601H, the 2nd is written into y602H, the last byte is written into y600H.

RXB3 (y640H)

Bit Name	Bit Number	Default	Description
RXB3	7-0	--	The contents of this register is the received B3 byte.

RXC2 (y641H)

Bit Name	Bit Number	Default	Description
RXC2	7-0	--	The contents of this register is the received C2 byte.

RXG1 (y642H)

Bit Name	Bit Number	Default	Description
RXG1	7-0	--	The contents of this register is the received G1 byte.

RXF2 (y643H)

Bit Name	Bit Number	Default	Description
RXF2	7-0	--	The contents of this register is the received F2 byte.

RXH4 (y644H)

Bit Name	Bit Number	Default	Description
RXH4	7-0	--	The contents of this register is the received H4 byte.

RXF3 (y645H)

Bit Name	Bit Number	Default	Description
RXF3	7-0	--	The contents of this register is the received F3 byte.

RXN1 (y646H)

Bit Name	Bit Number	Default	Description
RXN1	7-0	--	The contents of this register is the received N1 byte.

RXK3 (y647H)

Bit Name	Bit Number	Default	Description
RXK3	7-0	--	The contents of this register is the received K3 byte.

EXC2 (y690H)

Bit Name	Bit Number	Default	Description
Expected C2	7-0	00	This register contains the expected J1 Path Trace message. The incoming C2 byte is compared against this byte and an internal 01H value. If the **C2PEN** bit is set to a 1, and the received C2 byte does not match the byte in this register, or 01H, for 5 consecutive frames, then the **SLM** bit will become set. If the incoming C2 byte matches the value in this register, or 01H, then the **SLM** bit will clear, or stay cleared.

RXCNTL1 (y691H)

Bit Name	Bit Number	Default	Description
--	7-6	00	Not used. These bits should always be set to 0.

RXCNTL1 (y691H)

Bit Name	Bit Number	Default	Description
AZSPE	5	0	0=Normal Operation. 1= TX Telecom Bus Input Data is set to all 0s. This setting is used in conjunction with the bits in the TXCNTL1 and TXCNTL2 registers to force an unequipped or supervisory unequipped in the corresponding STS-1-SPE/VC-4/STS-3c-SPE of the TX Telecom Bus.
SLMEN	4	0	0=Inhibits **SLM** from generating TX path RDI. 1=Enables **SLM** to generate TX path RDI.
RV1EN	3	0	0= Only J0 and J1 pulses are output on the RX J0J1 line. 1= A V1 pulse and J0 and J1 pulses are output on the RX J0J1 line. The V1 pulse is synchronized to the received H4 byte.
REIEN	2	0	0= REI counter is disabled. REI transferred to TX G1 block is 0s. 1= REI counter is enabled. REI is transferred to TX G1 block based on received B3 Errors.
C2PEN	1	0	0=RX C2 processing is disabled. **UNEQ** and **SLM** bits are forced to 0. 1=RX C2 processing is enabled. **UNEQ** and **SLM** bits are set based on the RX C2 byte.
TIMEM	0	0	0=RX J1 processing is disabled. **TIM** is forced to 0. 1=RX J1 processing is enabled. **TIM** is set based on the RX J1 bytes.

J1EN	B3EN	C2EN	G1EN	F2EN	H4M1	H4M0	F3EN	K3EN	N1EN	TYPE OF TX UNEQUIPPED SIGNAL
0	1	0	0	0	0	0	0	0	0	Unequipped (Bellcore or ITU-T modes of operation)
1	1	0	1[a]	0	0	0	0	0	0	Supervisory (defined only for ITU-T)

a. The corresponding REIEN, C2PEN, and TIMEN should be set to 1 as appropriate to ensure that the path RDI and REI functions are operating.

EXJ1 (y6C0H-y6FFH)

Bit Name	Bit Number	Default	Description
Expected J1	7-0	00	This 64 byte buffer contains the expected J1 Path Trace message. The incoming J1 Path Trace is compared against this message when the **TIMEN** bit is se to a 1; if a mismatch occurs, the **TIM** bit is set to a 1. If the **TIMEN** is set to a 0, the **TIM** bit is set to 0 and the J1 path trace comparison message function is disabled.

BOUNDARY SCAN

BOUNDARY SCAN INTRODUCTION

The IEEE 1149.1 Standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface leads of the device. The Test Access Port block, which implements the boundary scan functions, consists of a Test Access Port (TAP) controller, instruction and test data registers, and a boundary scan register path bordering the input and output leads, as illustrated in Figure 17. The boundary scan test bus interface consists of four input signals (i.e., the Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{\text{TRS}}$) input signals) and a Test Data Output (TDO) output signal. A brief description of boundary scan operation is provided below; further information is available in the IEEE Standard document.

The TAP controller receives external control information via a Test Clock (TCK) signal, a Test Mode Select (TMS) signal, and a Test Reset ($\overline{\text{TRS}}$) signal, and it sends control signals to the internal scan paths. The scan path architecture consists of a sixteen-bit serial instruction register, a one-bit bypass register and a boundary scan register. The instruction and data registers are connected in parallel between the serial Test Data Input (TDI) and Test Data Output (TDO) signals. The TDI signal is routed to the instruction, bypass and boundary scan registers and is used to transfer serial data into a register during a scan operation. The data to the TDO signal is selected from either register during a scan operation. When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device leads to pass to and from the POP-12 device's internal logic, as illustrated in Figure 17. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. A timing diagram for the boundary scan feature is provided in Figure 11.

Boundary Scan Support

The maximum frequency the POP-12 device will support for boundary scan is 20 MHz. The POP-12 device performs the following boundary scan test instructions:

- EXTEST
- SAMPLE/PRELOAD
- BYPASS
- IDCODE

EXTEST Test Instruction:

One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the POP-12 device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external POP-12 input and output leads.

SAMPLE/PRELOAD Test Instruction:

When the SAMPLE/PRELOAD instruction is shifted in, the POP-12 device remains fully operational. While in this test mode, POP-12 input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.

BYPASS Test Instruction:

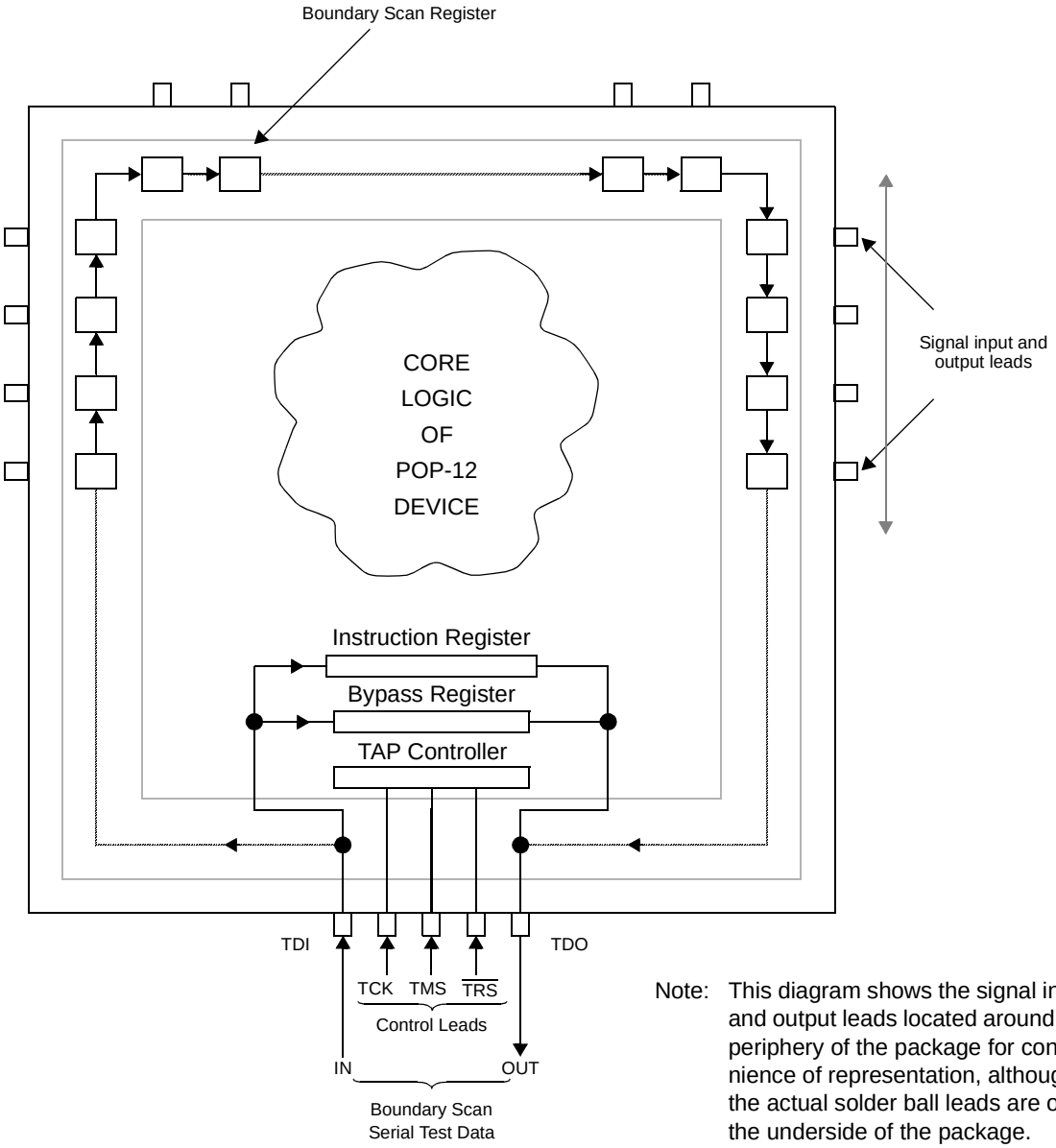
When the BYPASS instruction is shifted in, the POP-12 device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO lead. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.

IDCODE Test Instruction:

When the IDCODE instruction is shifted in, the contents of the IDCODE register can be read.

Boundary Scan Reset:

Specific control of the $\overline{\text{TRS}}$ lead is required in order to ensure that the boundary scan logic does not interfere with normal device operation. This lead should be held low whenever boundary scan operations are not being performed and also during power up.



Note: This diagram shows the signal input and output leads located around the periphery of the package for convenience of representation, although the actual solder ball leads are on the underside of the package.

Figure 17. Boundary Scan Schematic

BOUNDARY SCAN CHAIN

Bidirectional device leads have combined input/output scan cells. Additional scan cells are used for direction control as needed.

BSDL FILE

A BSDL file for use with the POP-12 is available from the TranSwitch Internet Web Site at www.transwitch.com.

APPLICATION EXAMPLES

A list of applications for the POP-12 are given below:

- Enabler for PHAST-12E.
- Interconnect between multiple or single SONET/SDH Overhead Terminators and mapper devices.
- IXC/ILEC Central Office Equipment
- OC-12/48 Add/Drop Mux
- Multiple STM-1/STS-3c/STS-3 Add/Drop Mux
- Grooming Switching for Metro Networks
- Transmux for DS-3 to VT mapping
- High density T3/E3 applications
- Protection applications

The following subsections graphically depict some POP-12 applications.

TRANSMUX

The Transmux is used to insert/extract T1 traffic into/from a DS-3 signal and de-map/map them directly from/into VT1.5 containers.

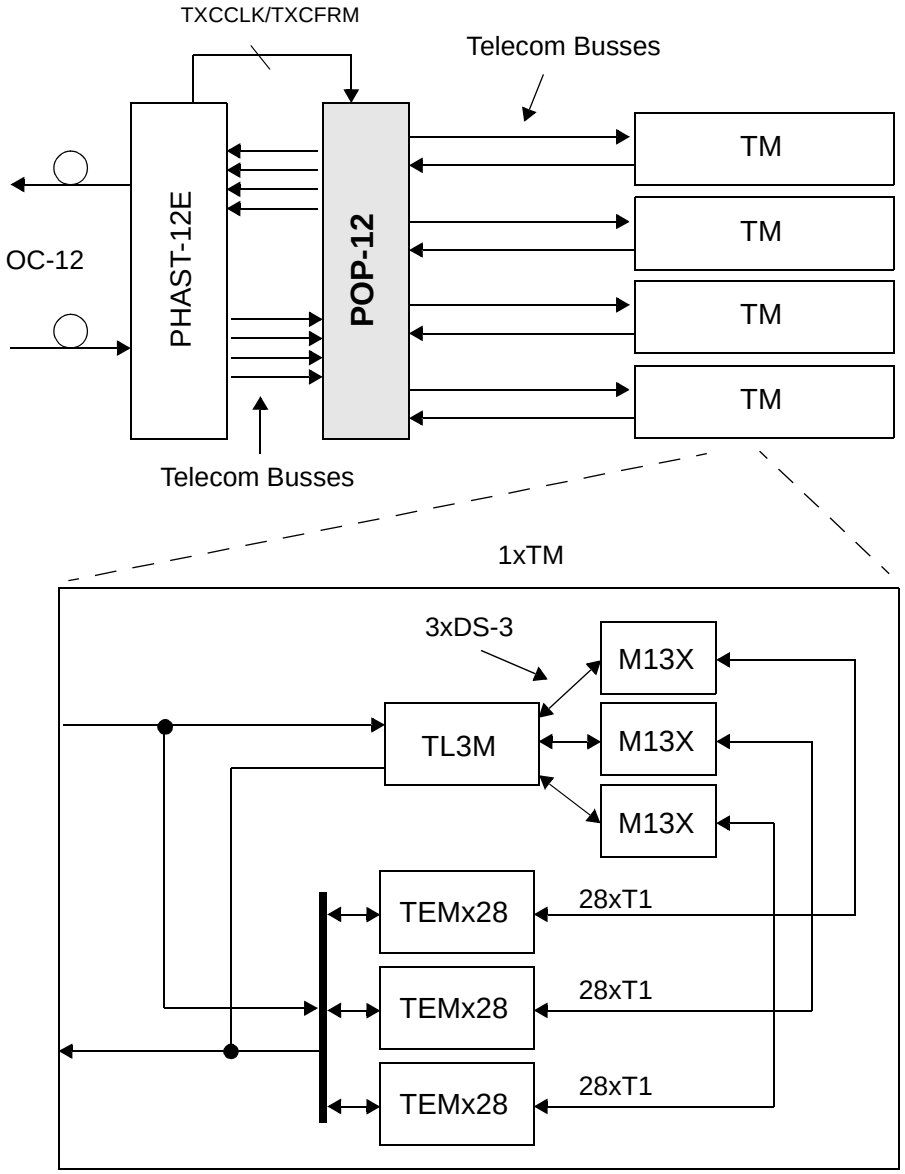


Figure 18. TransMux Application for the POP-12

TERMINAL MUX FOR HIGH DENSITY DS-3/E3 ACCESS

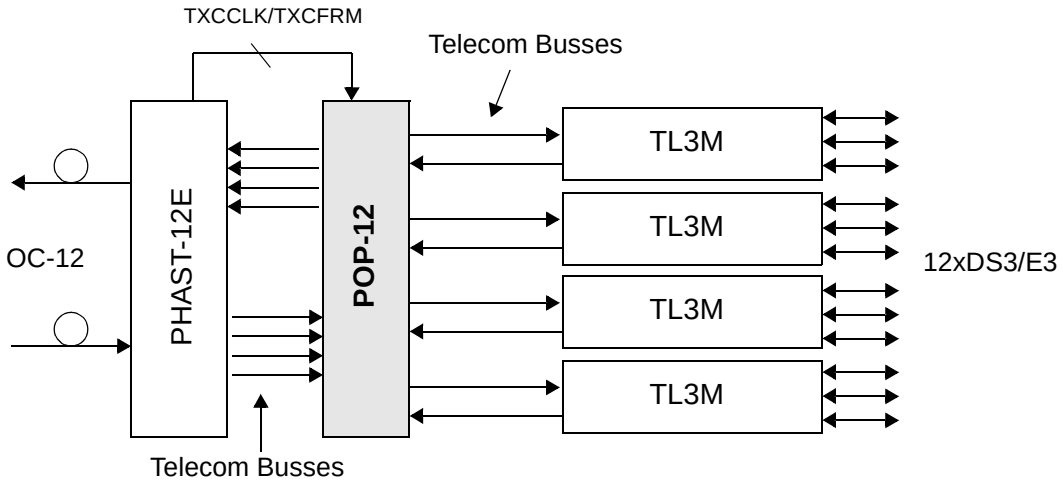


Figure 19. Terminal Mux Application for the POP-12

1+1 APS FOR OC-12/STM-4 MULTIPLEX SECTION/LINE PROTECTION

The two PHAST-12E devices terminate their respective Multiplex Section/Line. POP-12 B does the POH processing for the selected working PHAST-12E device. POP-12 A is simply used as an inexpensive retiming element so that the transmitted data is aligned also to PHAST-12E A's TX clock and frame.

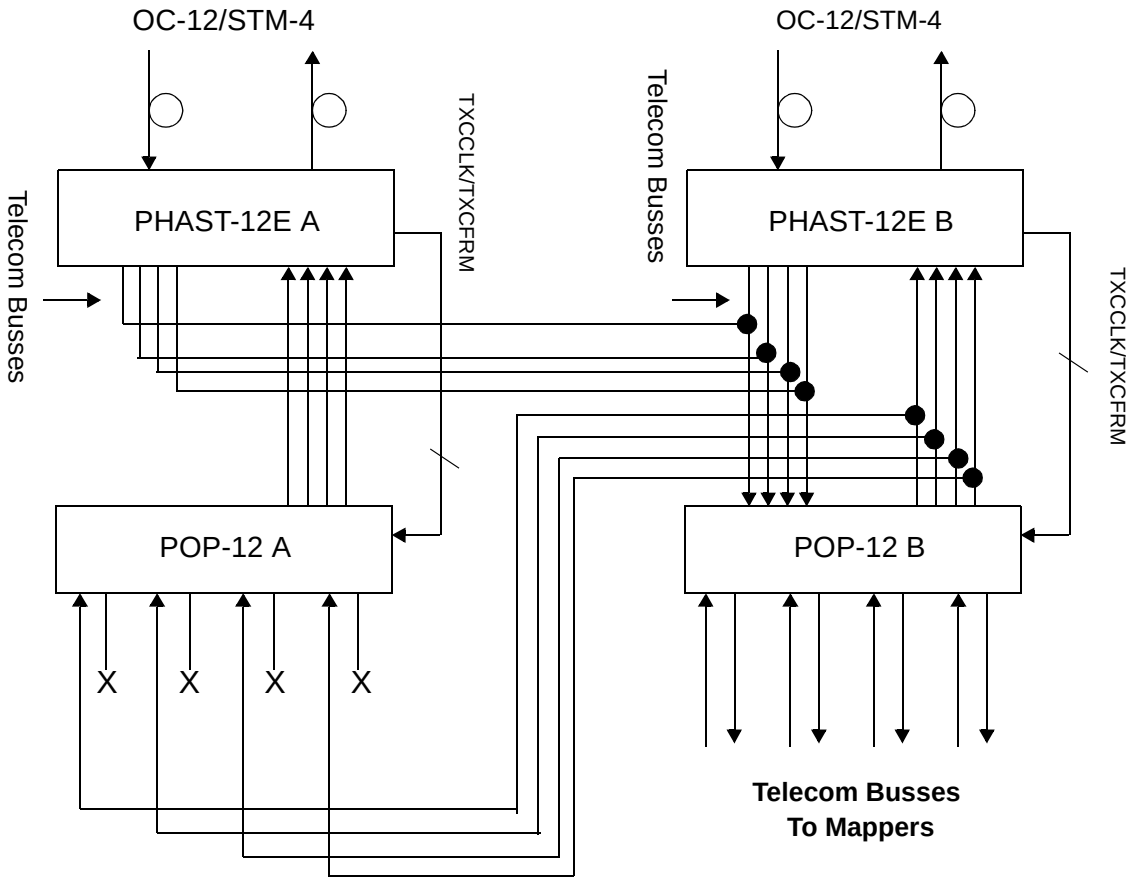


Figure 20. 1+1 APS Application for Multiplex Section/Line Protection

LINEAR ADD/DROP MUX

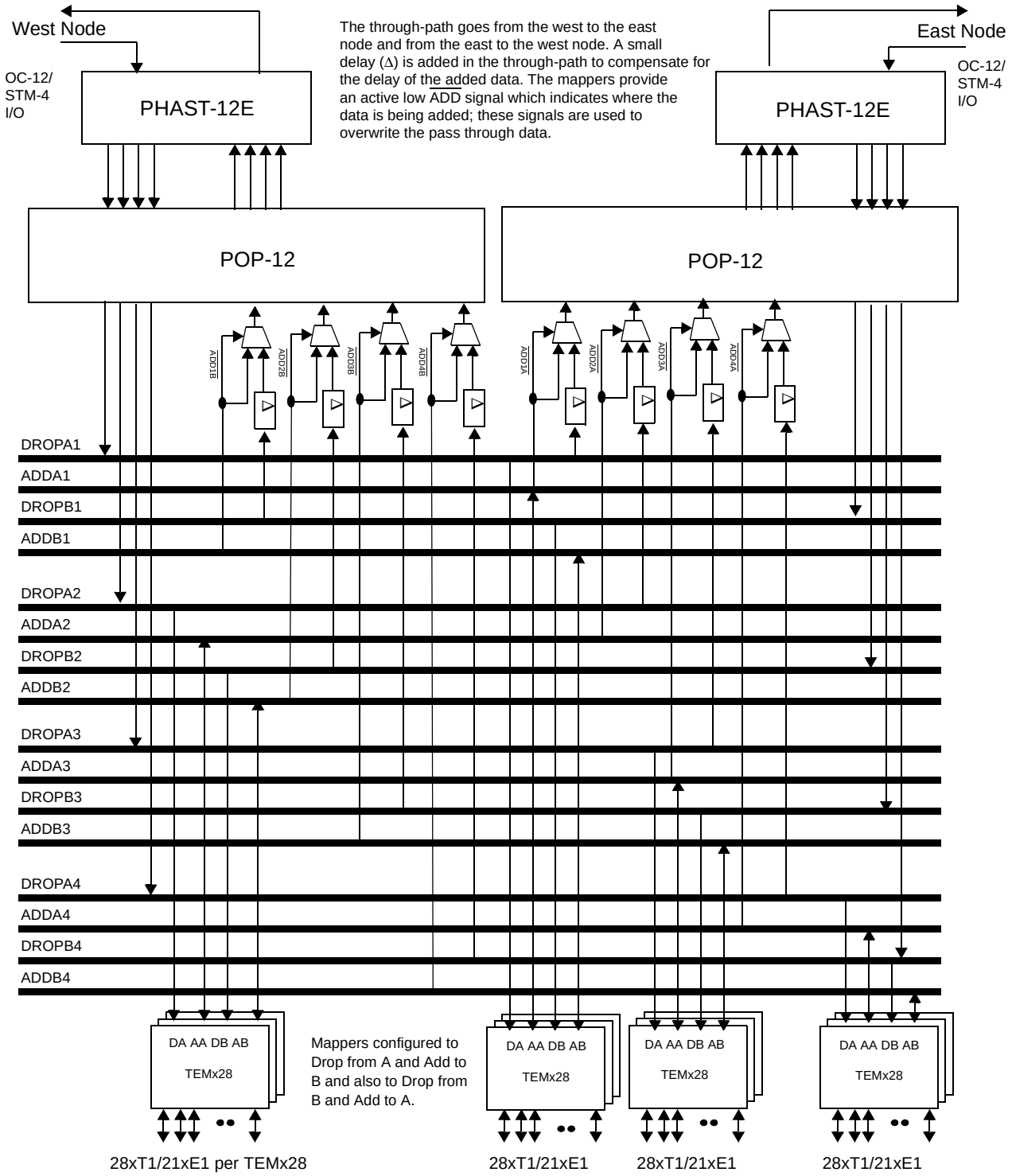


Figure 21. Linear Add/Drop Mux

DUAL RING ADD/DROP MUX

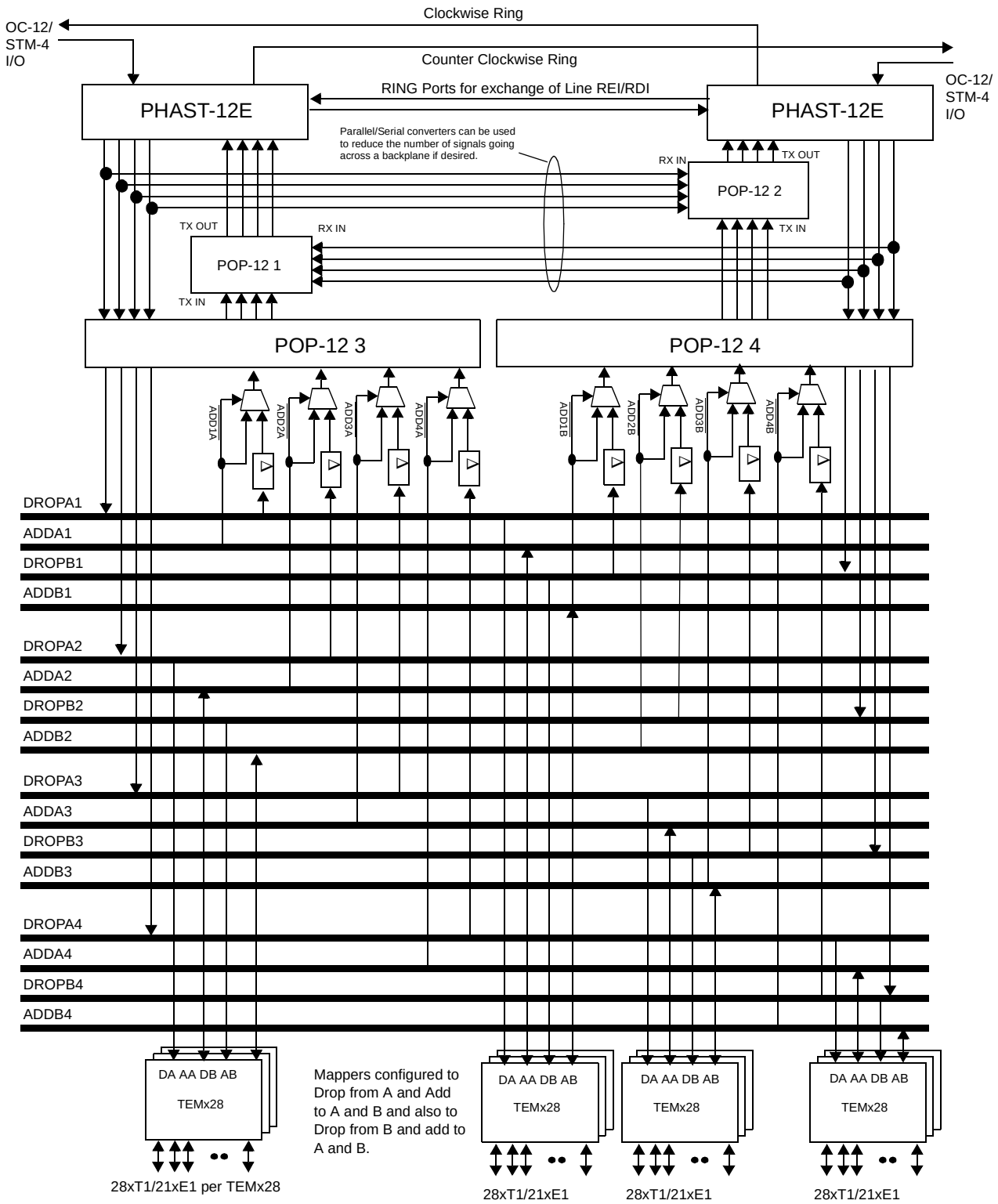


Figure 22. Dual-Ring Add/Drop Mux with Path Protection

POP-12s 1 and 2 in Figure 22 perform the function of sending the path layer alarms back to the source. In POP-12s 1 and 2, the Rx buses are only monitored.

Operation example:

a. Counter Clock Wise (CCW) ring is active.

b. Fiber cut occurs on incoming STM4

c. POP12 #3 sends path RDI forward to the CCW ring. POP12#1 is in pass trough.

d. also POP-12 #2 is monitoring the telecom buses from the CCW PHAST-12E (the one on the left), and is able to send path RDI to the Clock Wise (CW) PHAST-12E and therefore backwards, on the clockwise ring.

In other words, POP-12 #2 "mixes" i) the payload coming from the protection buses (the B buses in the picture) with ii) the path status calculated upon monitoring the active line (in this case the counter clockwise STM4).

ADM FOR SINGLE VC-4

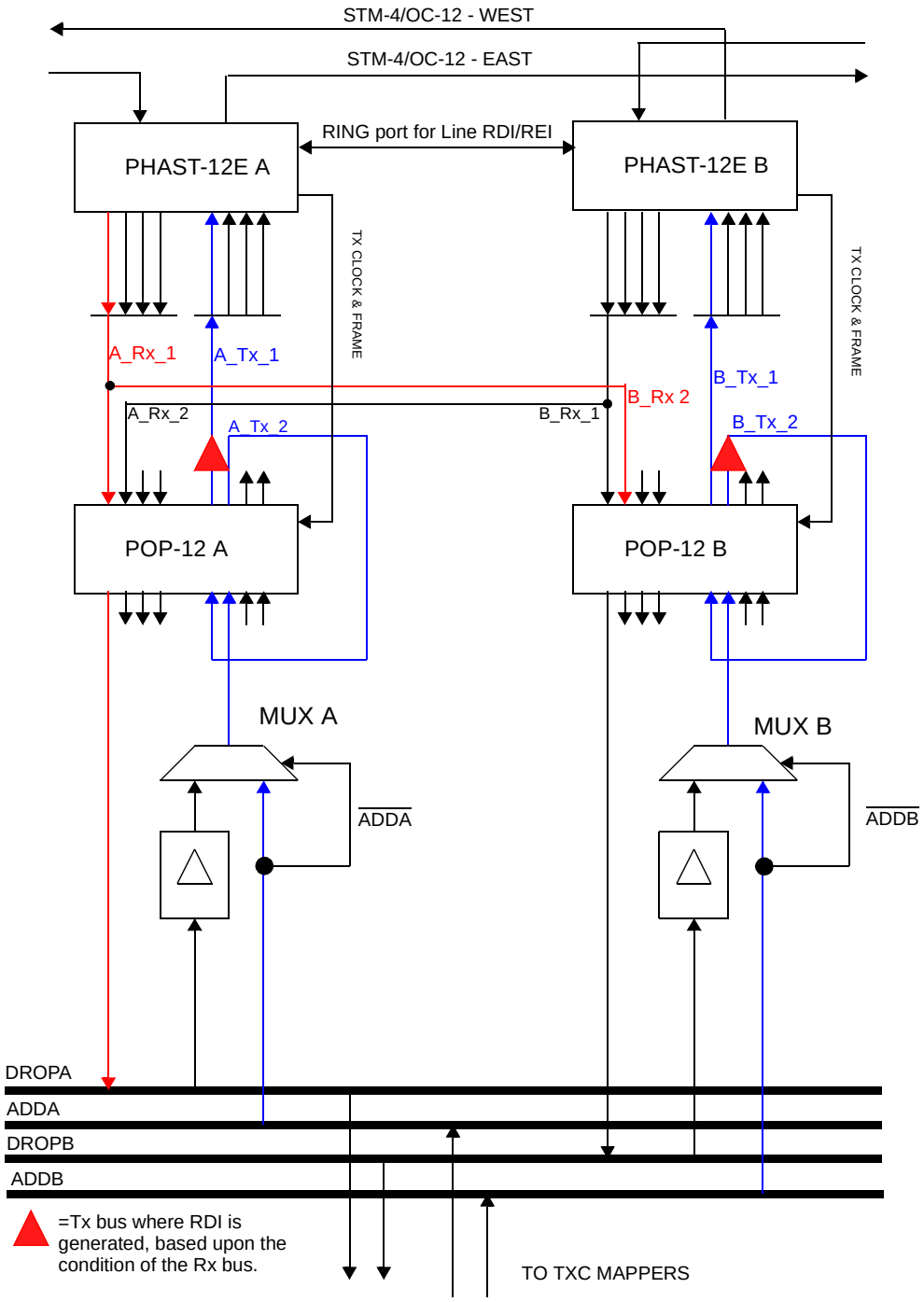


Figure 23. Path Protection for one VC-4 path

Figure 23 shows Path protection for one VC4 path, which will be called "VC4_X". It can be extended to two paths if desired without adding extra components. PHAST-12E A, POP-12 A, Telecom Bus A are working. PHAST-12E B, POP-12 B, Telecom Bus B are protecting. The same data is added to both ADDA and ADDB Telecom Busses via TDM mapper devices such as TranSwitch's TEMx28 or TL3M. This application makes use of the ability of the POP-12 to pass through traffic in its TX direction or to insert path REI and RDI based on received alarms and errors.

Normal operation: In the east direction, VC4_X is selected via tristate controls within PHAST-12E A to Telecom Bus A_Rx_1 and B_Rx2. The other three VC-4 that are not selected are passed through the PHAST-12E A's internal VC-4 cross connect. Lower Order (LO) tributaries from the mapper devices are added and dropped from DROPA and ADDA. A mux which uses the mappers ADDA signal and a delay element, are used to add the traffic from the ADDA bus and pass through unaffected LO tributaries from the DROPA bus. This traffic is sent to POP-12 A twice through two loops. The first loop (A_Tx_2) does not do anything to the data during normal operation, the POP-12 is programmed to just pass this data straight through. The 2nd time through the POP-12 (A_Tx_1), path RDI and REI are added to the signal based upon alarms and errors received at A_Rx_1. In the west direction a similar operation occurs, except that POP-12 B is programmed to insert path RDI and REI based on the alarms and errors it receives at B_Rx2 (i.e the 1st loop through POP-12 B). During the 2nd loop (B_Tx_1) through POP-12 B the data is just passed through. Thus, the same data and path alarms are provided to both the east and west directions of the RING. Additionally note that simultaneous monitoring of the paths of both directions is provided.

Switch: A similar operation exists when a switch takes place. The TX Telecom Busses in the POP-12s are programmed such that the channels that passed data through before, now add path RDI and REI, and channels that added path RDI and REI now do not. Also, note that the channels that add the path RDI and REI are adding them based on alarms and errors received from the west Ring. In such a case, the data from MUX A has path RDI and REI added based on alarms detected on A_Rx_2. This data is then passed through to A_Tx_2 which is looped around and passed through POP-12 A, unmodified, via A_Tx_1. The data from MUX B is passed through POP-12 B unmodified to B_Tx_2 which is then fed back to PHAST-12E B via B_Tx_1 which has Path RDI and REI added by POP-12 B based on alarms and errors received on B_Rx_1.

MULTISERVICE ADM WITH PASS THROUGH

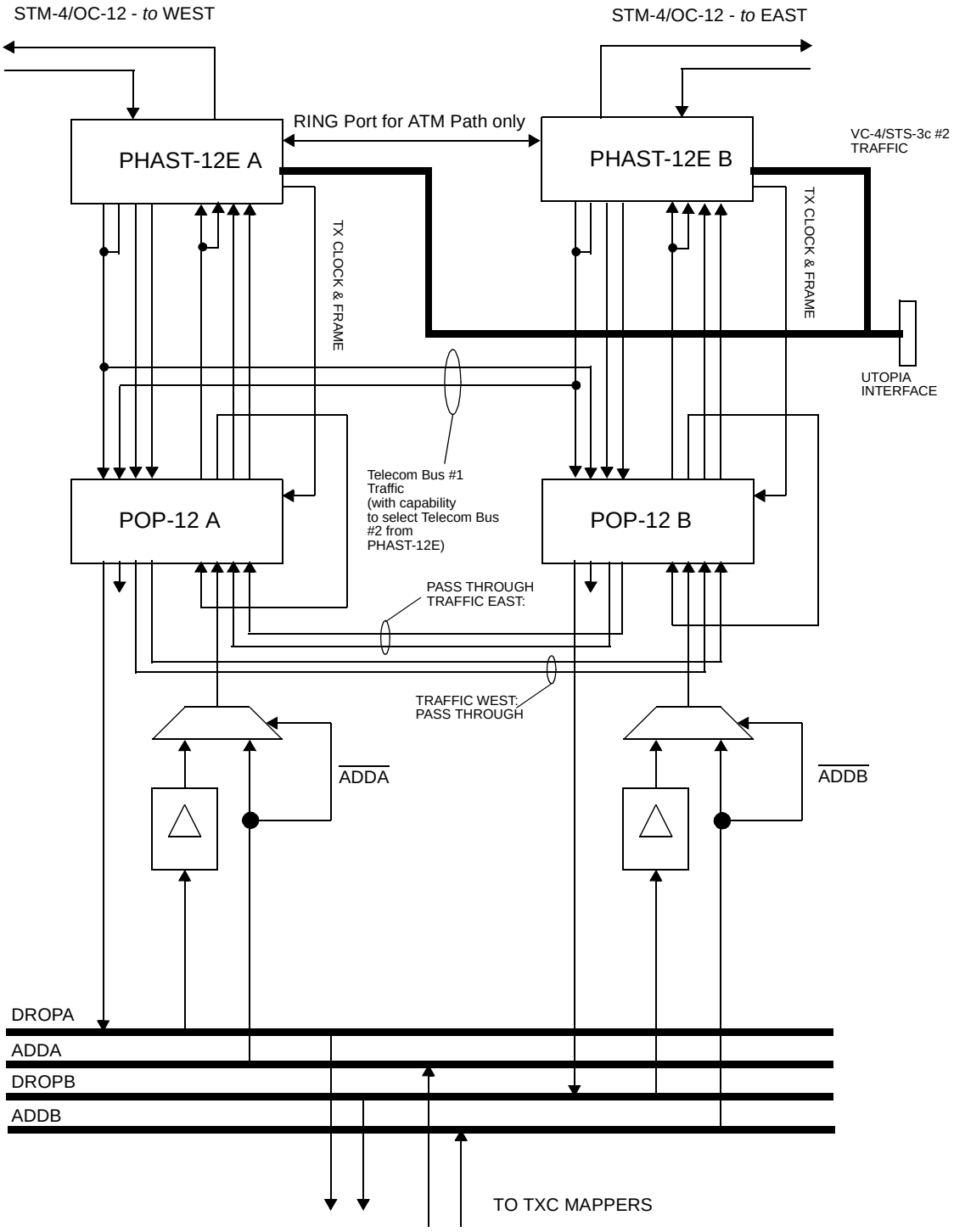


Figure 24. ADM with pass through of two Telecom Bus channels, ADD/DROP of one tributary, and termination of one VC-4/STS-3c into the UTOPIA Level 2 Bus

The application above in Figure 24 allows two Telecom Bus payloads to be passed through while terminating the other two payloads into a UTOPIA Level 2 Bus and a dual ADD/Drop Bus.

Payloads are terminated as follows:

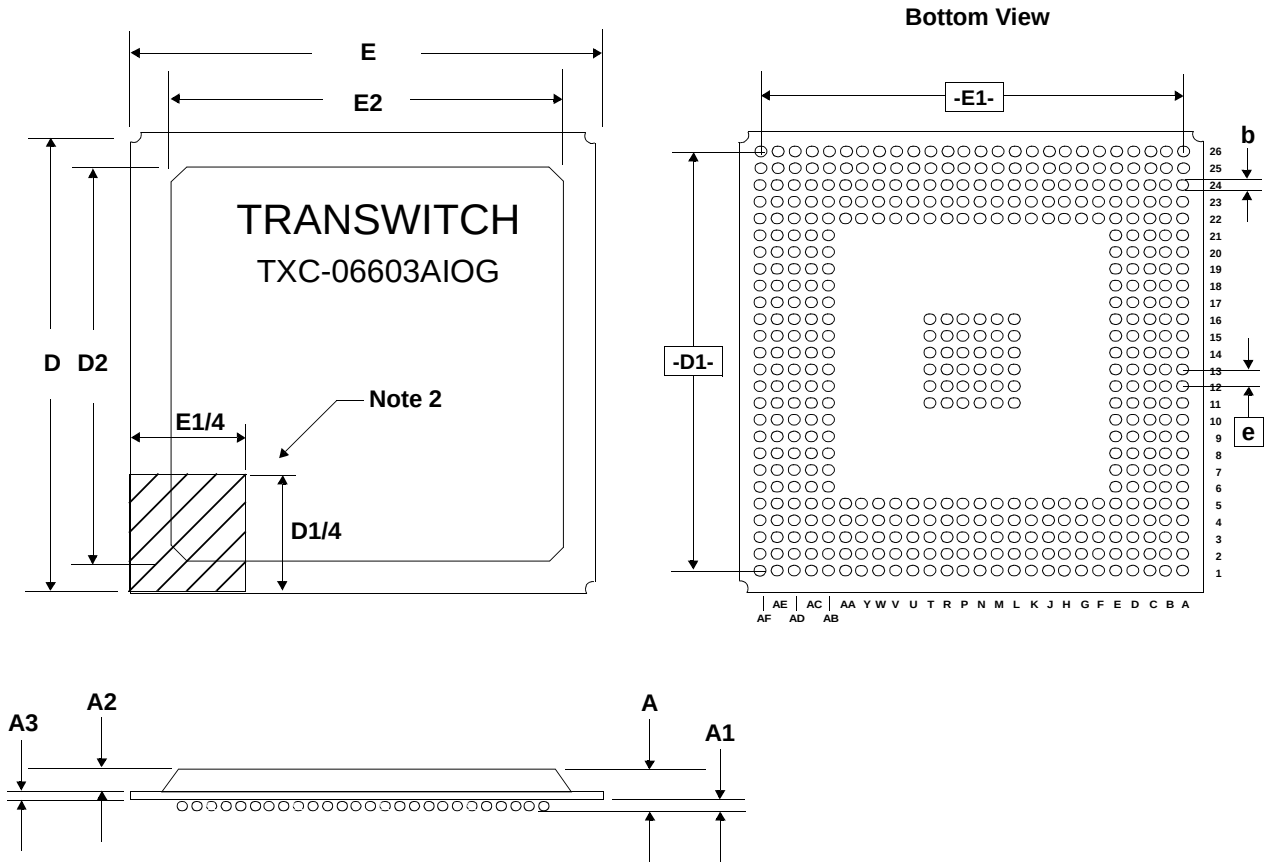
- #1 can have lower order VCs or STS-1 or VTs dropped or added via the dual ADD/DROP bus and TranSwitch Mapper Device's such as the TEMx28 and TL3M. The path layer is 1+1 protected, on the opposite ring. The POP-12 allows STS-3c-SPE, STS-1-SPE (via STS-3-SPE), or VC-4 to be processed. Either Telecom Bus 1 or 2 can be selected via the PHAST-12E depending upon which one is carrying ATM traffic and which one is carrying TDM traffic.

- #2 carries ATM traffic and goes on the UTOPIA Level 2 bus and does NOT go through POP-12. This path is also 1+1 protected on the opposite ring. The RING port of the PHAST-12E devices, with a mux (not shown), is used to communicate path ring data.

- #3 and #4 are passed through the POP-12 devices. In this application the pass-through traffic go through the POP-12 A and B, supposing that the NE must terminate, monitor and generate also the path layer. If the NE only must terminate, monitor and generate the RSOH and MSOH layer, PHAST-12E A and PHAST-12E B you can be connected directly (basically the drawing would have a shallower loop). The payload of the pass-through Telecom Busses can be either TDM or ATM; the granularity can go down to the AU-3 level and be cross connected as well because the traffic goes through the POP-12.

PACKAGE INFORMATION

The POP-12 device is packaged in a 456-lead, 27 mm x 27 mm, plastic ball grid array package suitable for surface mounting, as illustrated in Figure 25 below.



Dimension (Note 1)	Min	Max
A (Nom)	2.23	
A1	0.40	0.60
A2 (Nom)	1.12	1.22
A3 (Nom)	0.56	
b (Ref.)	0.63	
D	27.00	
D1 (Nom)	25.00	
D2	23.95	24.70
E	27.00	
E1 (Nom)	25.00	
E2	23.95	24.70
e (Ref.)	1.00	

Notes:
1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. Package corner may not be a 90° angle.

Figure 25. POP-12 TXC-06603 456-Lead Plastic Ball Grid Array Package

ORDERING INFORMATION

Part Number: TXC-06603AIOG 456-lead Plastic Ball Grid Array package (PBGA)

RELATED PRODUCTS

TXC-02020, ART VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter). ART performs the transmit and receive line interface functions required for transmission of STS-1 (51.840 Mbit/s) and DS3 (44.736 Mbit/s) signals across a coaxial interface.

TXC-02021, ARTE VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter). ARTE has the same functionality as ART, plus extended features.

TXC-02050, MRT Multi-Rate Line Interface VLSI Device. The MRT provides the functions for terminating ITU-specified 8448 kbit/s (E2) and 34368 kbit/s (E3) line rate signals, or 6312 kbit/s (JT2) line signals specified in the Japanese NTT Technical Reference for High Speed Digital Leased Circuits. An optional HDB3 codec is provided for the two ITU line rates.

TXC-03003B, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This is a dual-mode device, which can be configured either to emulate the TXC-03003 device or to provide additional capabilities.

TXC-03305, M13X VLSI Device (DS3/DS1 Mux/Demux). This single-chip device provides the functions needed to multiplex and demultiplex 28 independent DS1 signals to and from a DS3 signal with either an M13 or C-bit frame format. It includes some enhanced features relative to the M13E device.

TXC-03452B, L3M VLSI Device (Level 3 Mapper/Desynchronizer) - L3M maps a DS3 or E3 signal into an SDH/SONET signal formatted for STM-n (VC-3 via TU-3) or STS-n (via STS-1 SPE).

TXC-03453, TL3M VLSI Device (Triple Level 3 Mapper). Maps three 44.736 Mbit/s DS3 to an STM-1, TUG-3 or STS-3 STS-1 SPE SDH/SONET signal. An 34.368 Mbit/s E3 signal is mapped in to an STM-1 TUG-3. The TL3M's SDH/SONET interface format is COMBUS, byte wide parallel. The TL3M supports drop bus and add bus SDH/SONET timing modes. Drop bus timing provides timing signals for the add side while timing for both busses is independent for the add bus timing mode.

TXC-03456, L4M VLSI Device (Level 4 Mapper/Desynchronizer) - L4M Maps a 139.264 Mbit/s asynchronous line signal into an AU-4 VC-4/STS-3c SPE signal. The SONET/SDH signal is transmitted via the add bus with timing derived from the drop bus, add bus or an external source. The L4M provides test features such as line loopback, SONET/SDH loopback and on-chip test pattern generator and analyzer. The L4M meets strict jitter requirements to transport broadcast grade video signals.

TXC-04201B, DS1MX7 VLSI Device (DS1 Mapper 7-Channel). The DS1MX7 maps seven DS1 signals into any seven selected asynchronous or byte-synchronous mode VT1.5 or TU-11 tributaries in a SONET/SDH synchronous payload envelope.

TXC-04216, E1Mx16 VLSI Device (Sixteen channel E1 to AU-4/VT2 or TU-12 Async Mapper-Desync). Interconnects sixteen E1 signals with any sixteen asynchronous mode VT2 or TU-12 tributaries carried in SDH AU-4/AU-3 rate payload interface.

TXC-04222, TEMx28 VLSI Device (21/28 Channel Dual Bus High Density Mapper). An add/drop multiplexer, terminal multiplexer, and dual and single unidirectional ring applications. Up to 28 E1, DS1, or VT/TU payloads are mapped to and from VT1.5/TU-11s and VT2/TU-12s carried in an STM-1 VC-4 or STS-3 format.

TXC-04228, T1Mx28 VLSI Device (DS1 Mapper 28-CHannel Device). The DS1MX28 maps twenty eight DS1 signals into any seven selected asynchronous or byte-synchronous mode VT1.5 or TU-11 tributaries in a SONET/SDH synchronous payload envelope.

TXC-04251, QT1M VLSI Device (Quad DS1 to VT1.5 or TU-11 Async Mapper-Desync). Interconnects four DS1 signals with any four asynchronous mode VT1.5 or TU-11 tributaries carried in SONET STS-1 or SDH AU-3 rate payload interface.

TXC-04252, QE1M VLSI Device (Quad E1 to AU-4/VT2 or TU-12 Async Mapper-Desync). Interconnects four E1 signals with any four asynchronous mode VT2 or TU-12 tributaries carried in SDH AU-4/AU-3 rate payload interface.

TXC-05802B, CUBIT-*Pro* VLSI Device (ATM *CellBus* Switch). Implements cost effective ATM multiplexing and switching systems, based on the 32-bit *CellBus* architecture. A single-chip solution, the CUBIT-*Pro* has the ability to send and also receive cells for control purposes over the same *CellBus*. *CellBus* technology works at aggregate rates of up to 1 Gbit/s and provides header translation, multiplexing, concentration and switching functions for a wide variety of small-to-medium size ATM systems. This is a successor to the TXC-05802 device.

TXC-05804, CUBIT-3 is a single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus* architecture. Such systems are constructed from a number of CUBIT-3 devices, all interconnected by a 37-line common bus, the *CellBus*. CUBIT-3 supports unicast, broadcast and spatial multicast transfers, and has all necessary functions for implementing a switch: cell address translation, cell routing and outlet cell queuing. The CUBIT-3 is a VLSI product designed to interface directly on the terminal side with UTOPIA Level 1/2 8/16-bit compliant devices such as the CUBIT-*Pro* (TXC-05802B). The CUBIT-3 switch side interface is a *CellBus* interface which interfaces directly with *CellBus* devices such as the CUBIT-*Pro* (TXC-05802B).

TXC-06101, PHAST-1 VLSI Device (SONET STS-1 Overhead Terminator). This device performs section, line and path overhead processing for STS-1 SONET signals. It has programmable STS-1 or STS-N modes. It operates from a 3.3 volt supply and consumes less power than the SOT-1E TXC-03011 device with similar capability.

TXC-06103, PHAST-3N Device (STM-1/STS-3/STS-3c SDH/SONET Overhead Terminator). This device performs STM-1/STS-3/STS-3c termination into a Telecom Bus interface. Section, line, and path overhead byte processing is performed. A serial and byte parallel line interface is provided. TX and RX retiming and clock synthesis/recovery at 155.52 Mbit/s is provided on chip. Alarm and error processing is provided along with STS-1 loopback capability.

TXC-06203, PHAST-3P Device (STM-1/STS-3c SDH/SONET Overhead Terminator with CDB/PPP UTOPIA Interface). This device performs STM-1/STS-3c termination into a UTOPIA Level 2 for ATM cell data, or a UTOPIA Level 2P interface for PPP data. Single-PHY or Multi-PHY operation is supported. A serial and byte parallel line interface is provided. Section, line, and path overhead byte processing is performed. Clock synthesis/recovery at 155.52 Mbit/s, alarm and error processing, as well as TX and RX retiming is provided.

TXC-06212, PHAST-12E VLSI Device (Programmable, High-Performance ATM/Packet/Transmission SONET/SDH Terminator for Level 12). A highly integrated SONET/SDH terminator device designed for ATM cell, frame, higher-order multiplexing, and transmission applications. This PHAST-12 VLSI device provides a Telecom Bus interface for downstream devices and operates from a power supply of 3.3 volts.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
25 West 43rd Street
New York, New York 10036
Tel: (212) 642-4900
Fax: (212) 398-0023
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

404 Balboa Street
San Francisco, CA 94118
Tel: (415) 561-6275
Fax: (415) 561-6120
Web: www.atmforum.com

ATM Forum Europe Office

Kingsland House - 5th Floor
361-373 City Road
London EC1 1PQ, England
Tel: 20 7837 7882
Fax: 20 7417 7500

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan
Tel: 3 3438 3694
Fax: 3 3438 3698

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112
Tel: (800) 854-7179 (within U.S.A.)
Tel: (303) 397-7956 (outside U.S.A.)
Fax: (303) 397-2740
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia-Antipolis Cedex, France
Tel: 4 92 94 42 00
Fax: 4 93 65 47 16
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007
Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (903) 769-3818
Web: www.mvip.org

IEEE (Corporate Office):

American Institute of Electrical Engineers
3 Park Avenue, 17th Floor
New York, New York 10016-5997 U.S.A.

Tel: (212) 419-7900 (within U.S.A.)
Tel: (800) 678-4333 (Members only)
Fax: (212) 752-4929
Web: www.ieee.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5852
Fax: 22 730 5853
Web: www.itu.int

JEDEC (International):

Joint Electron Device Engineering Council
2500 Wilson Boulevard
Arlington, VA 22201-3834

Tel: (703) 907-7559
Fax: (703) 907-7583
Web: www.jedec.org

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
5440 SW Westgate Dr., #217
Portland, OR 97221

Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 291-2569 (outside U.S.A.)
Fax: (503) 297-1090
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place Rm 3A184
Piscataway, NJ 08854-4157

Tel: (800) 521-2673 (within U.S.A.)
Tel: (732) 699-2000 (outside U.S.A.)
Fax: (732) 336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunication Technology Committee
Hamamatsu-cho Suzuki Building
1-2-11, Hamamatsu-cho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated *PRELIMINARY* POP-12 Data Sheet that have significant differences relative to the previous and now superseded *PRODUCT PREVIEW* POP-12 Data Sheet:

Updated POP-12 Data Sheet: *PRELIMINARY* Ed. 5, October 2003

Previous POP-12 Data Sheet: *PRELIMINARY* Ed. 4, June 2002

The page numbers indicated below of this updated Data Sheet include changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
16	Modified Lead Description column for Lead Names TTBDATAOUTA(7-0), and TTBCLKOUTA.
17	Modified Lead Description column for Lead Names TTBDATAOUTB(7-0), TTBCLKOUTB, TTBDATAOUTC(7-0) and TTBCLKOUTC.
18	Modified Lead Description column for Lead Names TTBDATAOUTD(7-0), and TTBCLKOUTD.
19	Modified Lead Description column for Lead Names RXCCLK, RTBDATAOUTA(7-0) and RTBCLKOUTA.
20	Modified Lead Description column for Lead Names RTBDATAOUTB(7-0) and RTBCLKOUTB.
21	Modified Lead Description column for Lead Names RTBDATAOUTC(7-0), RTBCLKOUTC, RTBDATAOUTD(7-0) and RTBCLKOUTD.
40	Changed Min value for Symbols $t_{SU(2)}$ and $t_{H(4)}$.
44	Changed Min value for Symbol $t_{H(4)}$.
105	Added IEEE (Corporate Office) contact information.
106	Changed List of Data Sheet Changes section.

-NOTES-

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