Preliminary Data Sheet

PowerPC 440SPe Embedded Processor

Features

- PowerPC® 440 processor core operating up to 667 MHz with 32KB I- and D-caches (with parity checking)
- On-chip 256KB SRAM configurable as L2 Cache or Ethernet Packet/Code store memory
- Selectable Processor vs Bus clock ratios (Refer to the Clocking chapter in the *PPC440SPe Embedded Processor User's Manual* for details)
- Support up to 16 GB (4 Chip Selects) of 64-bit/32-bit SDRAM with ECC
  DDR I 266-333-400
  DDR II 400-533-667
- Three PCI-Express serial interfaces:
  one 8 lanes and two 4 lanes - 2.5Gb/s per lane
  Root and Endpoint support.
  Opaque bridge
- One 64-bit DDR PCI-X interfaces up to 133 MHz (DDR 266) with support for conventional PCI
- Optional: High throughput RAID 6 hardware acceleration, performs XOR and Galois Field P & Q parity computations, supports up to 255 drives
- Optional:16 Programmable Galois Field polynomials including 14d and 11d
- XOR Accelerator with DMA controller
- I2O messaging with two DMA controllers
- External Peripheral Bus (16-bit Data, 27-bit Address) for up to three devices; Bank0=16 MB, Bank1 and Bank2=128 MB each
- One Ethernet 10/100/1000Mbps half- or full-duplex interface. Operational modes supported are MII and GMII.
- Programmable Interrupt Controller supports interrupts from a variety of sources.
- Programmable General Purpose Timers (GPT)
- Three serial ports (16750 compatible UART)
- Two IIC interfaces
- General Purpose I/O (GPIO) interface available
- JTAG interface for board level testing
- Processor can boot from PCI memory

Description

Designed specifically to address high-end embedded applications for storage, the PowerPC 440SPe (PPC440SPe) provides a high-performance, low power solution that interfaces to a wide range of peripherals by incorporating on-chip power management features and lower power dissipation.

This chip contains a high-performance RISC processor core, a DDR1/DDR2 SDRAM controller, configurable 256KB SRAM to be used as L2 cache or software-controlled on-chip memory, three PCI-Express interfaces, one DDR PCI-X bus interface, a 1Gbps Ethernet interface, an I2O/DMA controller, control for external ROM and peripherals, optional RAID 6 acceleration, an XOR DMA unit, serial ports, IIC interfaces, and general purpose I/O.

Technology: CMOS Cu-11, 0.13mm

Package: 27mm, 675-ball, 1mm pitch, Flip Chip-Plastic Ball Grid Array (FC-PBGA)

Power (estimated): Less than 14W @533MHz

Supply voltages required: 3.3V, 2.5V, 1.8V, 1.5V

Contents

Figures

Tables

Ordering and PVR Information

For information about the availability of the following parts, contact your local sales office. The most current version of the 440SPe is Revision B. The part numbers for 440SPe Revision B are shown in the following figures.

Product Name	Order Part Number (see Notes 1-5)	Package	Rev Level	PVR Value	JTAG ID
PPC440SPe	PPC440SPe-xpBfffC	27mm, 675 FC-PBGA	B	0x53421891	0x14538049

Notes:

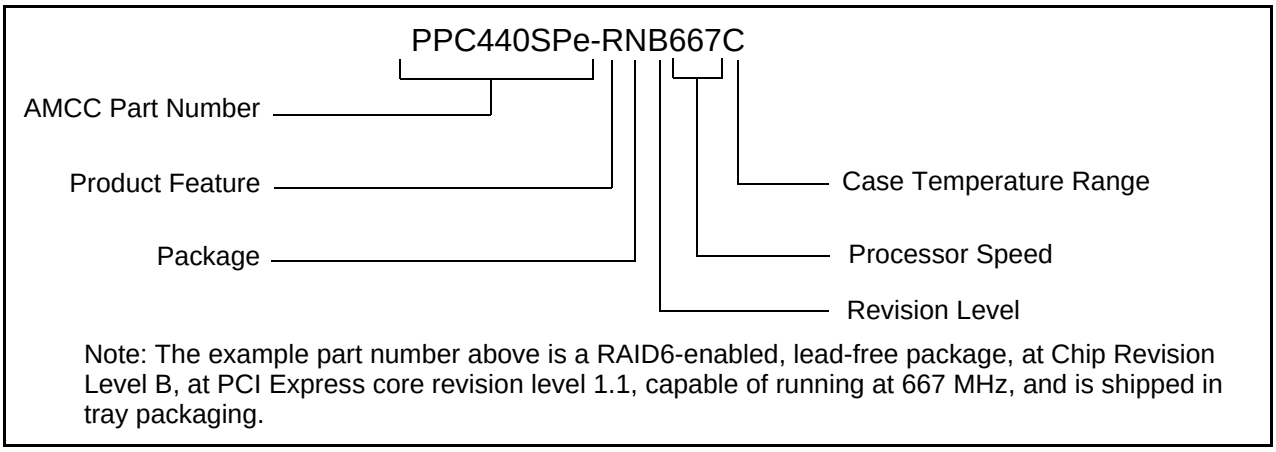
1. x = Product Feature
   A = RAID6 not enabled (Rev Level B only)
   R = RAID6 enabled (Rev Level B only)
2. p = Module Package Type
   G = leaded FC-PBGA
   N = lead free FC-PGBA (RoHS compliant)
3. B = Chip Revision Level B (2.0)
4. fff = Processor Frequency
   533 = 533MHz
   667 = 667MHz
5. C = Case Temperature Range of 0°C to +95°C

Each part number contains a revision code. This is the die mask revision number and is included in the part number for identification purposes only.

The PVR (Processor Version Register) and the JTAG ID register are software accessible (read-only) and contain information that uniquely identifies the part. See the *PPC440SPe Embedded Processor User's Manual* for details about accessing these registers.

Note: Raid-enabled versions (Product Feature = R) require a RAID key license.

Figure 1. Order Part Number Key



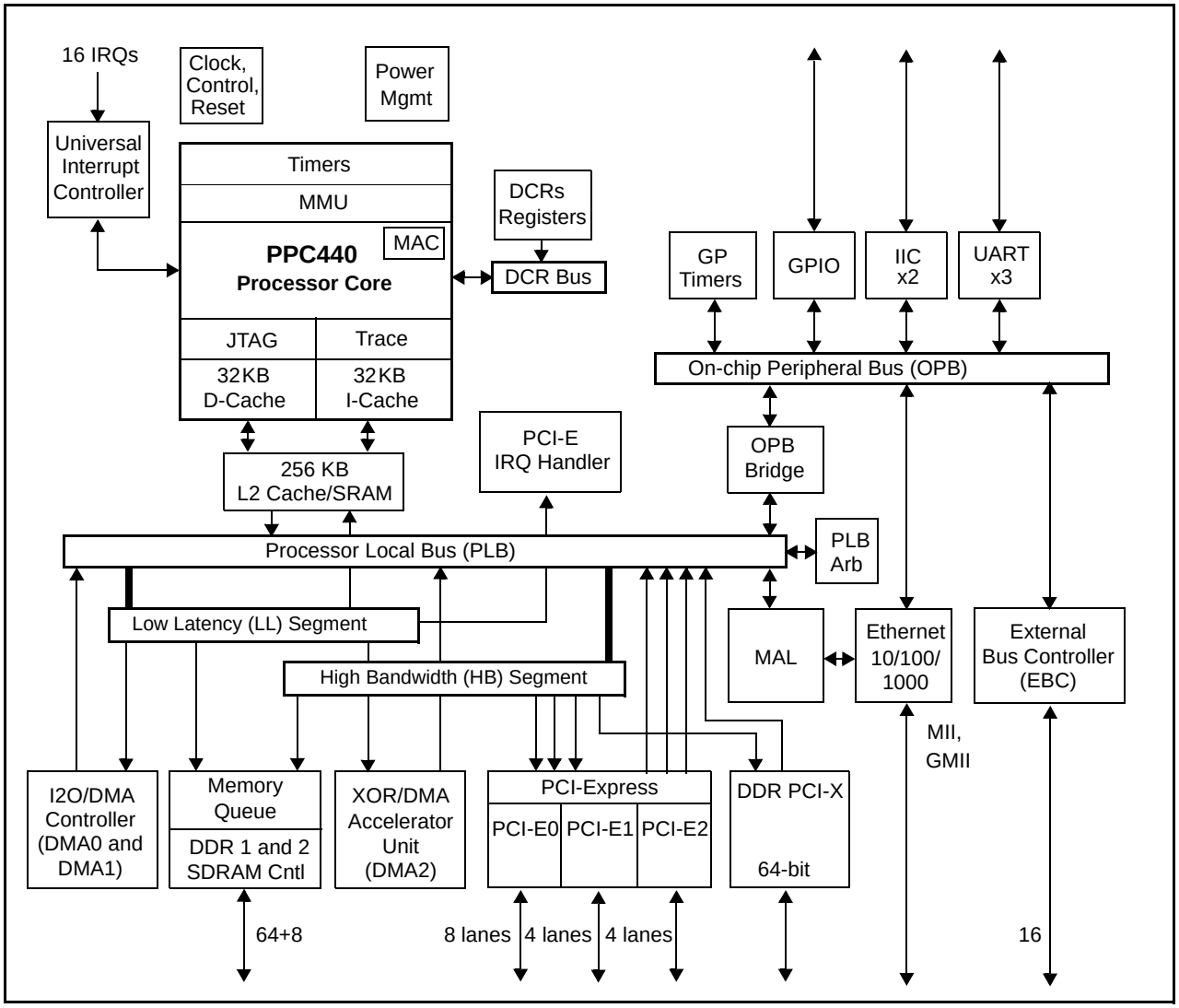
Note: The example part number above is a RAID6-enabled, lead-free package, at Chip Revision Level B, at PCI Express core revision level 1.1, capable of running at 667 MHz, and is shipped in tray packaging.

The part numbers for 440SPe Revision A are shown in the following figure.

Product Name	Order Part Number	Processor Frequency	Package	Rev Level	PVR Value	JTAG ID
PPC440SPe	PPC440SPe-3GA533C	533MHz	27mm, 675 FC-PBGA	A	0x53421890	0x14538049
PPC440SPe	PPC440SPe-3GA667C	667MHz	27mm, 675 FC-PBGA	A	0x53421890	0x14538049

PPC440SPe Functional Block Diagram

Figure 2. PPC440SPe Functional Block Diagram



The PPC440SPe is a System on a Chip (SOC) designed around the IBM CoreConnect Bus™ Architecture.

Implemented with the Crossbar option, the CoreConnect buses provide:

- Two Master PLB bus 128-bit Data 64-bit Address PLB interfaces up to 166.66 MHz, 2.6 GB/s on both the Read and Write data path (10.6 GB/s total)
- 32-bit OPB interfaces up to 83.33 MHz for a maximum throughput of 333 MB/s

Address Maps

The PPC440SPe incorporates two address maps. The first is a fixed processor system memory address map. This address map defines the possible contents of various processor accessible address regions. The second address map identifies the system Device Configuration Registers (DCRs). DCRs are accessed by software running on the PPC440SPe processor through the use of **mtdcr** and **mfdcr** instructions.

Table 1. System Memory Address Map (Sheet 1 of 2)

Function	Sub Function	Start Address	End Address	Size
Local Memory (LL)[1]	DDR SDRAM	0000 0000 0000 0000	0000 0003 FFFF FFFF	16GB
	SRAM	0000 0004 0000 0000	0000 0004 0003 FFFF	256KB
	Reserved	0000 0004 0004 0000	0000 0004 000F FFFF	
Internal PLB Interfaces (LL)	I2O Registers	0000 0004 0010 0000	0000 0004 0010 00FF	256B
	DMA 0 Registers	0000 0004 0010 0100	0000 0004 0010 01FF	256B
	DMA 1 Registers	0000 0004 0010 0200	0000 0004 0010 02FF	256B
	I20/DMA Buffers	0000 0004 0010 0300	0000 0004 0010 0FFF	3.25KB
	Reserved	0000 0004 0010 1000	0000 0004 001F FFFF	
	XOR/DMA2	0000 0004 0020 0000	0000 0004 0020 03FF	1KB
	Reserved	0000 0004 0020 0400	0000 0004 002F FFFF	
	PCI Express Interrupt Handler	0000 0004 0030 0000	0000 0004 0030 00FF	256B
	Reserved	0000 0004 0030 0100	0000 0004 DFFF FFFF	
Internal OPB Peripherals (LL)	EBC Memory[6]	0000 0004 E000 0000	0000 0004 EFFF FFFF	256MB
	Reserved	0000 0004 F000 0000	0000 0004 F000 01FF	
	UART0	0000 0004 F000 0200	0000 0004 F000 0207	8B
	Reserved	0000 0004 F000 0208	0000 0004 F000 02FF	
	UART1	0000 0004 F000 0300	0000 0004 F000 0307	8B
	Reserved	0000 0004 F000 0308	0000 0004 F000 03FF	
	IIC0	0000 0004 F000 0400	0000 0004 F000 041F	32B
	Reserved	0000 0004 F000 0420	0000 0004 F000 04FF	
	IIC1	0000 0004 F000 0500	0000 0004 F000 051F	32B
	Reserved	0000 0004 F000 0520	0000 0004 F000 05FF	
	UART2	0000 0004 F000 0600	0000 0004 F000 0607	8B
	Reserved	0000 0004 F000 0608	0000 0004 F000 06FF	248B
	GPIO Controller Registers	0000 0004 F000 0700	0000 0004 F000 077F	128B
	Reserved	0000 0004 F000 0780	0000 0004 F000 07FF	
	Ethernet Controller Registers	0000 0004 F000 0800	0000 0004 F000 08FF	256B
	Reserved	0000 0004 F000 0900	0000 0004 F000 09FF	

Table 1. System Memory Address Map (Sheet 2 of 2)

Function	Sub Function	Start Address	End Address	Size
	General Purpose Timers	0000 0004 F000 0A00	0000 0004 F000 0B3F	320B
	Reserved	0000 0004 F000 0B40	0000 0004 FEFF FFFF	
Boot ROM[2, 3]	EBC Bank0	0000 0004 FF00 0000	0000 0004 FFFF FFFF	16MB
Reserved		0000 0005 0000 0000	0000 0007 FFFF FFFF	
Local Memory Alias (HB)	Aliased DDR SDRAM	0000 0008 0000 0000	0000 000B FFFF FFFF	16GB
PCI Space (HB)	Reserved	0000 000C 0000 0000	0000 000C 07FF FFFF	
	PCIX0 I/O	0000 000C 0800 0000	0000 000C 0800 FFFF	64KB
	Reserved	0000 000C 0801 0000	0000 000C 0EBF FFFF	
	PCIX0 Addressing configuration Regs	0000 000C 0EC0 0000	0000 000C 0EC0 0007	8B
	Reserved	0000 000C 0EC0 0008	0000 000C 0EC7 FFFF	
	PCIX0 Core Configuration Regs	0000 000C 0EC8 0000	0000 000C 0EC8 0FFF	4KB
	Reserved	0000 000C 0EC8 1000	0000 000C 0EC8 10FF	
	PCIX0 Simple Message Passing	0000 000C 0EC8 1100	0000 000C 0EC8 11FF	256B
	Reserved	0000 000C 0EC8 1200	0000 000C 0ECF FFFF	
	PCIX0 Special Cycle	0000 000C 0ED0 0000	0000 000C 0EDF FFFF	1MB
	Reserved	0000 000C 0EE0 0000	0000 000C 0FFF FFFF	
	PCI Memory (PCI-Express & PCI-X)	0000 000C 1000 0000	0000 000C FEFF FFFF	3.8GB
	PCI-X DDR boot ROM (PCI memory	0000 000C FF00 0000	0000 000C FFFF FFFF	16MB
	PCI Memory (PCI-Express & PCI-X)	0000 000D 0000 0000	0000 000F FFFF FFFF	12GB
	Reserved[4]	0000 0010 0000 0000	0FFF FFFF FFFF FFFF	
	Reserved[5]	1000 0000 0000 0000	1FFF FFFF FFFF FFFF	
PCI Core Space (HB)	PCI Memory (PCI-Express & PCI-X)	2000 0000 0000 0000	FFFF FFFF FFFF FFFF	

Notes:

1. DDR SDRAM and on-chip SRAM can be located anywhere in the Local Memory area of the memory map.
2. The Boot ROM and Expansion ROM areas of the memory map are intended for use by ROM or Flash-type devices. While locating volatile DDR SDRAM and SRAM in this region is supported, use of these regions for this purpose is not recommended.
3. When the optional boot from PCI-X memory is selected, the PCI-X Boot ROM address space begins at C FF00 0000 (16 MB).
4. Never decoded.
5. Unpredictable results on Read and Write operations.
6. Accessed by means of EBC Peripheral Bank Configuration Registers.

Table 2. DCR Address Map (4KB of Device Configuration Registers)

Function	Start Address	End Address	Size
Total DCR Address Space[1]	000	3FF	1KW (4KB)[1]
By function:			
Reserved	000	00B	12W
Clocking Power On Reset	00C	00D	2W
System DCRs	00E	00F	2W
Memory Controller	010	011	2W
External Bus Controller	012	013	2W
Reserved	014	01F	12W
SRAM	020	02F	16W
L2 Controller	030	03F	16W
Memory Queue	040	05F	32W
I2O, DMA0 & DMA1	060	07F	32W
PLB	080	08F	16W
PLB to OPB Bridge Out	090	09F	16W
Reserved	0A0	0AF	16W
Reserved	0B2	0BF	14W
Interrupt Controller 0	0C0	0CF	16W
Interrupt Controller 1	0D0	0DF	16W
Interrupt Controller 2	0E0	0EF	16W
Interrupt Controller 3	0F0	0FF	16W
PCI-Express 0	100	11F	32W
PCI-Express 1	120	13F	32W
PCI-Express 2	140	15F	32W
Power Management	160	167	8W
Reserved	168	17F	24W
Ethernet MAL	180	1FF	128W
Reserved	200	3FF	512W

Notes:
1. DCR address space is addressable with up to 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register. One KW (1024W) equals 4KB (4096 bytes).

PowerPC 440 Processor Core

The PowerPC 440 processor core is designed for high-end applications such as RAID controllers, SAN, ISCSI, routers, switches, printers, set-top boxes, and so on. It is the first processor core to implement the Book E PowerPC embedded architecture and uses the 128-bit version of IBM's on-chip CoreConnect Bus Architecture.

Features include:

- Up to 800 MHz operation
- PowerPC Book E architecture
- 32KB I-cache, 32KB D-cache
  - parity on data and tag address - Checking of parity with error injection
- Three logical regions in D-cache: Locked, Transient, and Normal
- D-cache full-line flush capability
- 41-bit virtual address, 36-bit (64GB) physical address
- Superscalar, out-of-order execution
- Seven-stage pipeline
- Three execution pipelines
- Dynamic branch prediction
- Memory management unit
  - 64-entry, full associative, unified TLB with parity
  - Separate instruction and data micro-TLBs
  - Storage attributes for write-through, cache-inhibited, guarded, and big or little endian
- Debug facilities
  - Multiple instruction and data range breakpoints
  - Data value compare
  - Single step, branch, and trap events
  - Non-invasive real-time trace interface
- 24 DSP instructions
  - Single cycle multiply and multiply-accumulate
  - 32 x 32 integer multiply

Internal Buses

The PowerPC 440SPe features three IBM standard on-chip buses: the Processor Local Bus (PLB), the On-Chip Peripheral Bus (OPB), and the Device Control Register Bus (DCR). The high performance, high bandwidth cores such as the PowerPC 440 processor core, the DDR SDRAM memory controller, the PCI Express and the DDR PCI-X bridges connect to the PLB. The OPB hosts lower data rate peripherals. The daisy-chained DCR provides a lower bandwidth path for passing status and control information between the processor core and the other on-chip cores.

The PLB has a Crossbar arbiter that supports data transfer between the PLB master and two slave segments identified as the Low Latency (LL) and High Bandwidth (HB) segments. The LL segment allows PLB masters CPU and I2O, that are adversely affected by latency, to communicate with slave devices with minimal latency. The HB segment allows PLB masters DMA, XOR, PCI and PCI Express to exchange large blocks of data with SDRAM, PCI and PCI Express without interfering with the low latency PLB masters.

Bus features include:

- PLB
  - 128-bit implementation of the PLB architecture
  - Separate and simultaneous read and write data paths
  - 64-bit address
  - Simultaneous control, address, and data phases
  - Four levels of pipelining
  - Byte enable capability supporting unaligned transfers
  - 32- and 64-byte burst transfers

  - 166MHz, maximum 5.2GB/s (simultaneous read and write)
  - Processor vs Bus clock ratios of N:1 and N:2
- OPB
  - Dynamic bus sizing: 32, 16, and 8-bit data path
  - 32-bit address
  - 83.33MHz, maximum 333MB/s
- DCR
  - Register control bus
  - 32-bit data path
  - 10-bit address

On-Chip SRAM/L2 Cache

Features include:
- Four banks of 64KB each for a total of 256KB
- Configurable as either L2 cache or SRAM
- Memory cycles supported:
  - Single beat read and write, 1 to 16 bytes
  - Quadword Read and Write burst for 12-bit master
  - Guarded memory accesses on 4KB boundaries
- Sustainable 2.6GB/s peak bandwidth at 166MHz
- Use as an L2 cache improves processor performance and reduces the PLB load
  - Cache coherency maintained by a hardware snoop mechanism on the Low Latency (LL) PLB or by software
  - Data Array and Tag Array parity
  - Unified data and instruction cache
  - Four-way set associative
  - 36-bit addressing
  - Full LRU replacement algorithm
  - Write through, look aside
- Use as Ethernet packet store allows Ethernet packets to be held for processing by the Ethernet core

PCI Express

Features include:
- Three independent PCI Express interfaces
  - One 8 lanes
  - Two 4 lanes
  - 2.5 GB/sec full duplex per lane
- Compliant with PCI Express base specification 1.0a
- Each PCI Express port can be End Point or Root Complex. (Upstream & Downstream)
  - Applications compliant with MSI rules are limited to one End Point port per PPC440SPe
- PCI-Express to PCI-Express opaque (Non-Transparent) bridge
- Power Management
- Supports one virtual channel (VC0) no Traffic Class (TC) filtering
- Maximum Payload block size 512 Bytes
- Supports up to 1024 byte maximum Read request size
- Requests supported:
  - up to 4 posted outbound Write requests (memory and messages)
  - up to 4 posted inbound Write requests
  - up to 4 outbound Read requests outstanding on PCI Express
  - up to 4 inbound Read requests outstanding on PCI Express
  - Outbound I/O request as a PCI Express Root Port
  - Inbound I/O request as a PCI Express End Point

- Buffering in each PCI Express Port for the following transaction types:
  - 4K byte Replay buffer: up to 8 in flight transactions
  - 2K bytes for Outbound posted Writes
  - 8K bytes for Outbound Reads completion
    - 2K prefetch request from first I2O/DMA PLB Master
    - 1K prefetch request from 2nd I2O/DMA PLB Master
    - 1K prefetch request from first PCIE 4x links
    - 1K prefetch request from 2nd PCIE 4x links
    - 256 byte from the PPC440
  - 2K bytes for Inbound posted Writes
  - 2K bytes for Inbound Reads completion
- Parity checking on each buffer
- POM Programmable Outbound Memory Regions: 3 Memory, 1 I/O, 1 Message, 1 config, 1 Internal Regs
- PIM Programmable Inbound Memory Regions: 4 Memory, 1 I/O, 1 Expansion ROM
- INTx Interrupts support (PCI legacy):
  - up to 4 INTx Termination for Root Ports. A/B/C/D interrupts are wired to the UIC
  - A/B/C/D INTx types Generation for Endpoints
- MSI - Message Signaled Interrupts
  - MSI Generation for End Point
  - MSI Termination for Root Ports
  - MSI_X Termination for Root Ports

DDR PCI-X Interface

The DDR PCI-X interface allows connection of PCI and PCI-X devices to the PowerPC processor and local memory. The PCI-X interface supports 64-bit PCI-X bus in DDR mode 2. It can be configured for either host or adapter mode. PCI 32/64-bit legacy mode, compatible with PCI Version 2.3, is also supported.

Features include:

- PCI-X 2.0
  - Split transactions
  - Frequency to 266MHz
  - 32- and 64-bit address/data bus
  - ECC supported for 266MHz Mode 2 only
- PCI 2.3 backward compatibility
  - Frequency to 66MHz
  - 32- and 64-bit bus
- Can be the PCI Host Bus Bridge or an Adapter Device PCI interface
- Optional PCI arbitration function with PCI and PCI-X mode 1, supporting up to four external devices, that can be disabled for use with an external arbiter
- Support for PLB-based (external to PLB–PCI-X bridge) I2O
- Support for Message Signaled Interrupts (MSI) on both in- and out-bound interrupts
- Simple message passing capability
- Asynchronous to the PLB
- PCI Power Management Version 1.1
- PCI arbitration function with PCI-X Mode 2 support (optional)
- PCI register set addressable both from on-chip processor and PCI device sides
- Ability to boot from PCI-X bus memory
- Error tracking/status
- Supports initiation of transfer to the following address spaces:
  - Single beat I/O reads and writes
  - Single beat and burst memory reads and writes
  - Single beat configuration reads and writes (Type 0 and Type 1)
  - Single beat special cycles

- PCI-X initialization sequence support (frequency & mode determination)
- Support for unexpected split completions
- Outbound transaction split discard timers
- Vital Product Data (VPD) support
- PCI-X to PCI-Express opaque bridge

DDR1/DDR2 SDRAM Memory Controller

The DDR2 SDRAM memory controller supports industry standard 184-pin DIMMs, SO-DIMMs, and other discrete devices. Global memory timings, address and bank sizes, and memory addressing modes are programmable. The DDR2 SDRAM controller interfaces to the PLB through a Memory Queue (MQ) function that includes six high-speed 1KB FIFO buffers.

Features include:

- Registered and non-registered industry standard DIMMs
- DDR2 400/667 support
- 64-and 32-bit memory interfaces with optional 8-bit ECC (SEC/DED)
- 5.32GB/s peak bandwidth for the 64-bit interface
- 2.66GB/s peak bandwidth for the 32-bit interface
- Four chip (bank) select signals supporting 4 external banks
- CAS latencies of 2, 3, 4, 5, 6, and 7 supported
- Page mode accesses (up to 32 open pages) with configurable paging policy
- Look-ahead request queue with programmable depth of four commands.
- Optional optimized command scheduling (activate/precharge non-conflicting banks while accessing the current bank)
- Up to 16GB in four external banks
- Up to 6 MemClkout signals for high loading unbuffered DIMMS.
- Programmable address mapping and timing
- Hardware and software initiated self-refresh
- Sync DRAM configuration by means of mode register and extended mode register set commands
- Power management (self-refresh, suspend, sleep)
- Low Latency & High Bandwidth PLB ports
- Selectable PLB read response (immediate or deferred)
- Programmable Low Latency & High Bandwidth arbitration schemes
- High Bandwidth port has four 1KB read buffers and two 1KB write buffers
- Low Latency port has four 128B read buffers and two 128B write buffers

External Peripheral Bus Controller (EBC)

Features include:

- Support Boot ROM on Bank 0; programmable size 2, 4, 8,16 MB
- Up to three ROM, EPROM, SRAM, Flash memory, and slave peripherals supported
- Burst and non-burst devices
- 16 or 8-bit data bus
- 27-bit address, 128MB address space for Banks 1 & 2
- Peripheral Device pacing with external “Ready”
- Latch data on Ready, synchronous or asynchronous
- Programmable access timing per device
  - 256 Wait States for non-burst
  - 32 Burst Wait States for first access and up to 8 Wait States for subsequent accesses
  - Programmable CSon, CSoff relative to address
  - Programmable OEon, WEon, WEoff (1 to 4 clock cycles) relative to CS
- Programmable address mapping

Ethernet Controller Interface

The Ethernet support interfaces to the physical layer, but the PHY is not included on the chip.

Features include:
- One 10/100/1000 interface running in full- and half-duplex modes
  - One full Media Independent Interface (MII) with 4-bit parallel data transfer
  - One Gigabit Media Independent Interface (GMII)

I2O/DMA Controller

The I20/DMA controller provides support for I20 messaging and two DMA controllers (DMA0 and DMA1). I2O manages Message Frame Address (MFA) FIFOs or queues in memory in response to I2O register reads and writes and transfers message frames. The DMAs provide normal memory access support to ease the CPU burden.

I2O features include:
- I2O pull- and push-messaging methods
- Dynamic message frame size
- Programmable FIFO size (4096 64-bit MFAs maximum)
- 64-bit and 32-bit MFA sizes
- Three interrupt gathering methods
- Registered MFA prefetch and posting
- 32-bit inbound and outbound doorbell registers
- Four 32-bit scratch pad registers

DMA features include:
- Programmable Command Pointer FIFO and Completion FIFO size (up to 2048 DMA operations queued)
- 512-byte buffering
- Simultaneous fill and drain (PLB read/write pipelining)
- Any source PLB address to any destination address
- No memory alignment restrictions on source or destination
- 32-byte command descriptor block
- Maximum transfer size of 16MB
- 64-bit addressing
- 1KB buffering (DMA1 only)
- Prefetch indicators for PCI-X buffer management (DMA1 only)

Optional RAID 5 and RAID 6 Acceleration Hardware

The 440SPe provides integrated acceleration hardware that implements high throughput RAID 5 and RAID 6 algorithms to compute the single parity P for RAID 5, and dual parity P & Q for RAID 6. RAID 5 is used to recover data in the case of a single disk drive failure, and RAID 6 provides for data recovery if two disk drives fail.

The 440SPe offers a choice of two XOR engines for computing the P parity. The first choice is available with the XOR/DMA2 acceleration unit and is used for RAID 5. The second choice for XOR parity computation, along with the RAID 6 Galois Field GF(2^8)-based polynomial computations, resides inside the Memory Queue functional block of the Memory Controller unit. The Galois Field polynomial used with the 440SPe is programmable and can be one of sixteen available irreducible polynomials, including 14d and 11d.

The RAID 5 and RAID 6 parity computations performed in the Memory Queue are assisted by the two-channel DMA engine of the I2O/DMA controller unit, designated as DMA0 and DMA1. The RAID acceleration hardware also provides various alternatives for balancing load and performance, depending on customer-specific application firmware. The two-way crossbar bus architecture can perform data read and write operations simultaneously, resulting in extremely high throughput.

RAID 6 capability is available only with the RAID-enabled part numbers (PPC440SPe-RpBfffC) as indicated in the ordering information section of this data sheet.

For more information about the RAID 6 implementation, description, and configuration of the acceleration hardware, refer to the following AMCC documents:
- PowerPC 440SP/440SPe RAID Support Application Note
- PowerPC 440SPe RAID Addendum to the User's Manual

XOR/DMA2 Controller

The XOR/DMA2 controller performs the XOR functions needed to support RAID 5 applications including parity generation and check functions used across data stripes in a RAID 5 system.
- Computes a bit-wise XOR on up to 16 data streams with result stored in designated target
- Performs XOR check on up to 16 data streams
- Driven by a linked list Command Block structure specifying control information, source operands, target operand, status information, and link
- Source and target streams may reside anywhere in PLB address space.
- Provides completion status per Command Block to be handled by software at a later time
- 96-byte and 160-byte Command Block formats are supported
- No memory alignment restrictions on operands or target
- Internal register arrays and data buffers are parity protected
- Can be used as a DMA controller (DMA2) with single source and target addresses
- PLB Master interface
- PLB Slave port used as control interface for reading and writing control and status information

Serial Port

The serial port is compatible with the NS, 16570 UART interface.

Features include:
- One 8-pin, one 4-pin, and one 2-pin interfaces are provided
- Selectable internal or external serial clock to allow wide range of baud rates
- Register compatibility with 16750 register set
- Complete status reporting capability
- Fully programmable serial-interface characteristics

IIC Bus Interface

Features include:
- Two IIC interfaces provided
- Support for Philips, Semiconductors I^2C Specification, dated 1995
- Operation at 100kHz or 400kHz
- 8-bit data
- 10- or 7-bit address
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Supports fixed V_{DD} IIC interface
- Two independent 4 x 1 byte data buffers
- Twelve memory-mapped, fully programmable configuration registers
- One programmable interrupt request signal
- Full management of all IIC bus protocols
- Programmable error recovery
- Port 0 supports serial Bootstrap ROM with default override parameters at initialization

General Purpose Timers (GPT)

Provides a time base counter and system timers additional to those defined in the processor core.
- 32-bit time base counter driven by the OPB bus clock
- Seven 32-bit compare timers

General Purpose IO (GPIO) Controller

- Controller functions and GPIO registers are programmed and accessed by means of memory-mapped OPB bus master accesses.
- The 32 GPIOs are pin-shared with other functions. DCRs control whether a particular pin that has GPIO capabilities acts as a GPIO or is used for another purpose.
- Each GPIO output is a separately programmable tri-state driver (pull-up, pull-down, or open-drain).

Universal Interrupt Controller (UIC)

Four cascaded Universal Interrupt Controllers (UIC) process internal on-chip and external processor interrupts.

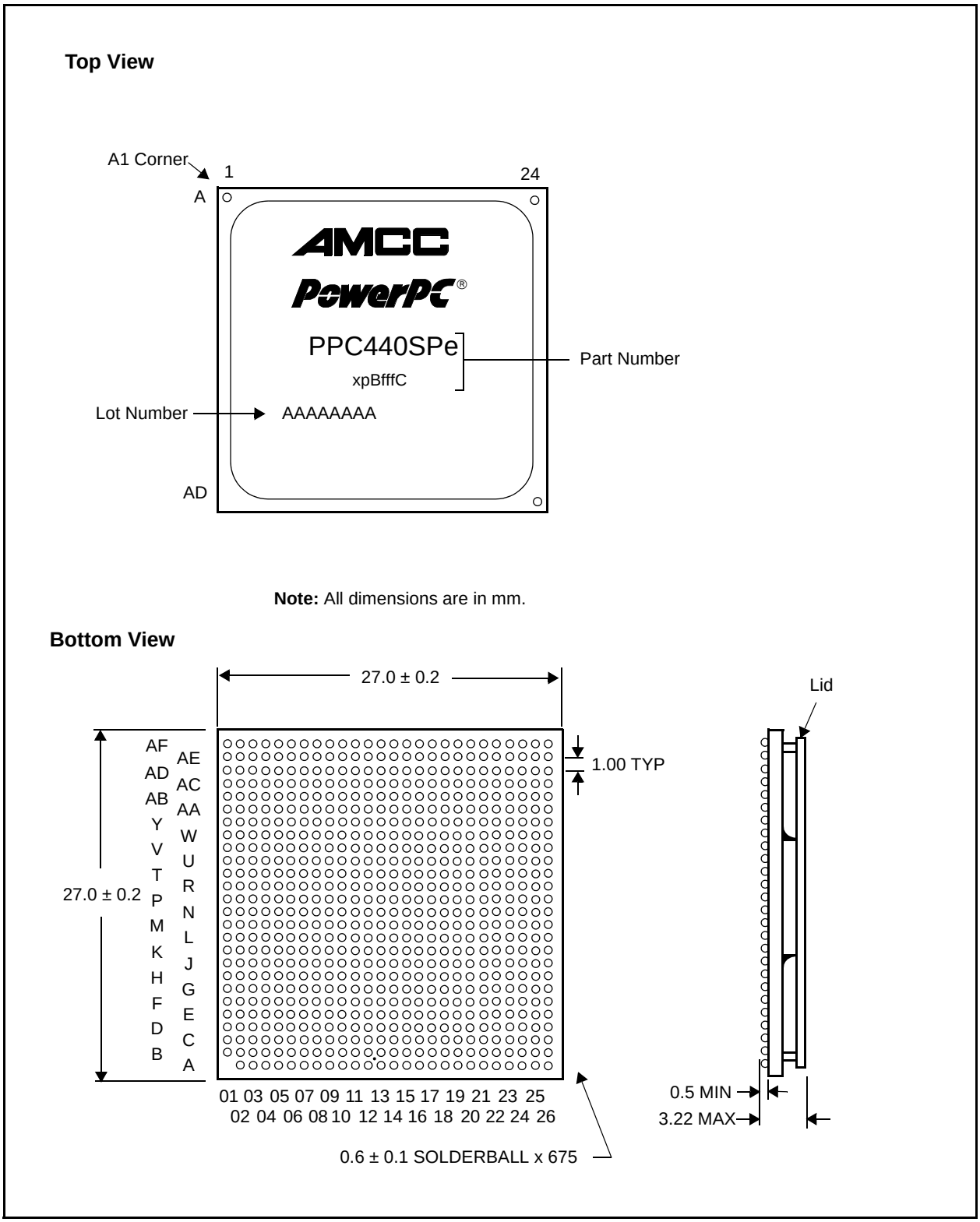
Note: Processor specific interrupts (for example, page faults) do not use UIC resources.

Features include:
- 16 external interrupts
- 101 internal interrupts
- Edge-triggered or level-sensitive
- Positive- or negative-active
- Non-critical or critical interrupt to the on-chip processor core
- Programmable interrupt priority ordering
- Programmable critical interrupt vector for faster vector processing

JTAG

Features include:
- IEEE 1149.1 Test Access Port
- IBM RISCWatch Debugger support
- JTAG Boundary Scan Description Language (BSDL)

Figure 3. 27mm, 675-Ball FC-PBGA Core Package



Signal Lists

This section contains two tables that list external signals.

Table 3 lists all the external signals in alphabetical order and shows the ball (pin) number on which the signal appears. Multiplexed signals are shown with the default signal (following reset) *not* in brackets and the alternate signal(s) in brackets.

In Table 3, multiplexed pins that have *no* internal signal connected after reset are marked High Z.

Multiplexed signals appear alphabetically multiple times in the list—once for each signal name on the ball. The page number listed gives the page in “Signal Functional Description” on page 50 where the signals in the indicated interface group begin.

Table 4 on page 42 lists all the external signals in order by ball (pin) number.

Signal List—Alphabetic Order

Table 3. Signals Listed Alphabetically (Sheet 1 of 25)

Signal Name	Ball	Interface Group	Page
BA0	AE22	DDR SDRAM	52
BA1	AD21		
BA2	AE21		
$\overline{\text{BankSel0}}$	AD20		
$\overline{\text{BankSel1}}$	Y18		
$\overline{\text{BankSel2}}$	Y19		
$\overline{\text{BankSel3}}$	W17		
$\overline{\text{CAS}}$	AB22		
ClkEn0	Y21		
ClkEn1	AA22		
ClkEn2	AE25		
ClkEn3	AF25		
DM0	AD25	DDR SDRAM	52
DM1	V20		
DM2	V25		
DM3	T25		
DM4	J26		
DM5	G22		
DM6	F24		
DM7	C23		
DM8	M19		

Table 3. Signals Listed Alphabetically (Sheet 2 of 25)

Signal Name	Ball	Interface Group	Page
$\overline{\text{DQS0}}$	AA23	DDR SDRAM	52
DQS0	AA24		
$\overline{\text{DQS1}}$	U21		
DQS1	T19		
$\overline{\text{DQS2}}$	W23		
DQS2	W24		
$\overline{\text{DQS3}}$	P24		
DQS3	P25		
$\overline{\text{DQS4}}$	M22		
DQS4	L22		
$\overline{\text{DQS5}}$	G25		
DQS5	H25		
$\overline{\text{DQS6}}$	E22		
DQS6	F22		
$\overline{\text{DQS7}}$	B25		
DQS7	C25		
$\overline{\text{DQS8}}$	P21		
DQS8	R21		
ECC0	R19		
ECC1	R20		
ECC2	M20		
ECC3	P18		
ECC4	P19		
ECC5	N19		
ECC6	N21		
ECC7	N18		

Table 3. Signals Listed Alphabetically (Sheet 3 of 25)

Signal Name	Ball	Interface Group	Page
EMCCD	H05	Ethernet	53
EMCCrS	D03		
EMCGTxClk	J08		
EMCMDClk	F03		
EMCMDIO	B02		
EMCRefClk	H07		
EMCRxClk	B01		
EMCRxD0	L06		
EMCRxD1	J02		
EMCRxD2	G03		
EMCRxD3	H02		
EMCRxD4	H03		
EMCRxD5	L04		
EMCRxD6	M07		
EMCRxD7	F05		
EMCRxDV	J06		
EMCRxErr	F04		
EMCTxClk	C02		
EMCTxD0	C03		
EMCTxD1	G06		
EMCTxD2	J07		
EMCTxD3	A05		
EMCTxD4	E03		
EMCTxD5	C05		
EMCTxD6	E01		
EMCTxD7	B10		
EMCTxEn	C01		
EMCTxErr	D02		
$\overline{\text{ExtReset}}$	B11	System	55
GND	A04	Power	56
GND	A10		
GND	A17		
GND	A23		
GND	D01		

Table 3. Signals Listed Alphabetically (Sheet 4 of 25)

Signal Name	Ball	Interface Group	Page
GND	D07		
GND	D13		
GND	D14		
GND	D20		
GND	D26		
GND	G04		
GND	G10		
GND	G17		
GND	G23		
GND	J09		
GND	J12		
GND	J15		
GND	J18		
GND	K01		
GND	K07		
GND	K10		
GND	K12		
GND	K15		
GND	K17		
GND	K20		
GND	K26		
GND	L11		
GND	L13		
GND	L14		
GND	L16		

Table 3. Signals Listed Alphabetically (Sheet 5 of 25)

Signal Name	Ball	Interface Group	Page
GND	M09	Power	56
GND	M10		
GND	M12		
GND	M15		
GND	M17		
GND	M18		
GND	N04		
GND	N11		
GND	N13		
GND	N14		
GND	N16		
GND	N23		
GND	P04		
GND	P11		
GND	P13		
GND	P14		
GND	P16		
GND	P23		
GND	R09		
GND	R10		
GND	R12		
GND	R15		
GND	R17		
GND	R18		
GND	T11		
GND	T13		
GND	T14		
GND	T16		
GND	U01		
GND	U07		

Table 3. Signals Listed Alphabetically (Sheet 6 of 25)

Signal Name	Ball	Interface Group	Page
GND	U12	Power	56
GND	U15		
GND	U17		
GND	U20		
GND	U26		
GND	V09		
GND	V12		
GND	V15		
GND	V18		
GND	Y04		
GND	Y10		
GND	Y17		
GND	Y23		
GND	AC01		
GND	AC07		
GND	AC13		
GND	AC14		
GND	AC20		
GND	AC26		
GND	AF04		
GND	AF10		
GND	AF17		
GND	AF23		
[GPIO00] [TRCCLK] High Z	L01	GPIO Peripherals Note: Trace can be enabled at reset by setting SDR0_SDSTP1[DBG] (bit 27) to 1 in the serial bootstrap ROM.	55
[GPIO01] [TRCBS0] High Z	H01		
[GPIO02] [TRCBS1] High Z	F01		
[GPIO03] [TRCBS2] High Z	L02		
[GPIO04] [TRCES0] High Z	K03		
[GPIO05] [TRCES1] High Z	G02		
[GPIO06] [TRCES2] High Z	M05		
[GPIO07] [TRCES3] High Z	F02		
[GPIO08] [TECES4] High Z	J03		
[GPIO09] [TRCTS0] High Z	H04		
[GPIO10] [TRCTS1] High Z	J05		

Table 3. Signals Listed Alphabetically (Sheet 7 of 25)

Signal Name	Ball	Interface Group	Page
[GPIO11] [TRCTS2] High Z	G05	GPIO Peripherals	55
[GPIO12] [TRCTS3] High Z	L05		
[GPIO13] [TRCTS4] High Z	J04		
[GPIO14] [TRCTS5] High Z	K06		
[GPIO15] [TRCTS6] High Z	H06		
[GPIO16] IRQ0	L08		
[GPIO17] IRQ1	M06		
[GPIO18] IRQ2	M08		
[GPIO19] IRQ3	E02		
[GPIO20] IRQ4	E04		
[GPIO21] IRQ5	H09		
[GPIO22] IRQ6	L07		
[GPIO23] IRQ7	F06		
[GPIO24] IRQ8	H08		
[GPIO25] IRQ9	A02		
[GPIO26] IRQ10	E26		
[GPIO27] IRQ11	E24		
[GPIO28] IRQ12	C22		
[GPIO29] IRQ13	L24		
[GPIO30] IRQ14	K25		
[GPIO31] IRQ15	K22		
$\overline{\text{Halt}}$	N22	System	55
HISRRst	AD17		
IIC0SClk	H17	IIC Peripheral	54
IIC0SDA	J16		
IIC1SClk	H18		
IIC1SDA	H15		

Table 3. Signals Listed Alphabetically (Sheet 8 of 25)

Signal Name	Ball	Interface Group	Page
IRQ0 [GPIO16]	L08	Interrupts	55
IRQ1 [GPIO17]	M06		
IRQ2 [GPIO18]	M08		
IRQ3 [GPIO19]	E02		
IRQ4 [GPIO20]	E04		
IRQ5 [GPIO21]	H09		
IRQ6 [GPIO22]	L07		
IRQ7 [GPIO23]	F06		
IRQ8 [GPIO24]	H08		
IRQ9 [GPIO25]	A02		
IRQ10 [GPIO26]	E26		
IRQ11 [GPIO27]	E24		
IRQ12 [GPIO28]	C22		
IRQ13 [GPIO29]	L24		
IRQ14 [GPIO30]	K25		
IRQ15 [GPIO31]	K22		
MemAddr00	AF22	DDR SDRAM	52
MemAddr01	AF19		
MemAddr02	AD22		
MemAddr03	T24		
MemAddr04	AF18		
MemAddr05	AB24		
MemAddr06	AF21		
MemAddr07	AE18		
MemAddr08	R25		
MemAddr09	AE20		
MemAddr10	AD19		
MemAddr11	AB26		
MemAddr12	R23		
MemAddr13	AB17		
MemAddr14	AE19		

Table 3. Signals Listed Alphabetically (Sheet 9 of 25)

Signal Name	Ball	Interface Group	Page
MemClkOut0	AA21	DDR SDRAM	52
$\overline{\text{MemClkOut0}}$	AA20		
MemClkOut1	AB21		
$\overline{\text{MemClkOut1}}$	AC21		
MemClkOut2	AB19		
$\overline{\text{MemClkOut2}}$	AC19		
MemClkOut3	AA19		
$\overline{\text{MemClkOut3}}$	AB20		
MemClkOut4	AA18		
$\overline{\text{MemClkOut4}}$	AB18		
MemClkOut5	AC18		
$\overline{\text{MemClkOut5}}$	AD18		
MemData00	AC25		
MemData01	AA26		
MemData02	AC24		
MemData03	AA25		
MemData04	AD24		
MemData05	AD23		
MemData06	AB25		
MemData07	AB23		
MemData08	U19		
MemData09	T21		
MemData10	V19		
MemData11	T20		
MemData12	V21		
MemData13	V22		
MemData14	T18		
MemData15	W22		
MemData16	U24		
MemData17	W25		
MemData18	V23		
MemData19	V24		

Table 3. Signals Listed Alphabetically (Sheet 10 of 25)

Signal Name	Ball	Interface Group	Page
MemData20	Y24		
MemData21	V26		
MemData22	Y25		
MemData23	W26		
MemData24	T22		
MemData25	R24		
MemData26	T23		
MemData27	R22		
MemData28	T26		
MemData29	N25		
MemData30	R26		
MemData31	N24		
MemData32	M26		
MemData33	K24		
MemData34	L26	DDR SDRAM	52
MemData35	L23		
MemData36	L25		
MemData37	J25		
MemData38	M21		
MemData39	M24		
MemData40	J23		
MemData41	H26		
MemData42	H23		
MemData43	G24		
MemData44	H24		
MemData45	H22		
MemData46	J24		
MemData47	J22		
MemData48	F26		

Table 3. Signals Listed Alphabetically (Sheet 11 of 25)

Signal Name	Ball	Interface Group	Page
MemData49	F23	DDR SDRAM	52
MemData50	F25		
MemData51	E23		
MemData52	E25		
MemData53	D25		
MemData54	D22		
MemData55	D24		
MemData56	C24		
MemData57	C26		
MemData58	B24		
MemData59	A24		
MemData60	B26		
MemData61	B23		
MemData62	A25		
MemData63	B22		
MemDCFdbkD	AE24		
MemDCFdbkR	AF24		
MemODT0	W21		
MemODT1	Y22		
MemODT2	W20		
MemODT3	W19		
MemVRef0	W18		
MemVRef1	V16		
No ball	A01		

Table 3. Signals Listed Alphabetically (Sheet 12 of 25)

Signal Name	Ball	Interface Group	Page
OV_{DD}	A07		
OV_{DD}	A13		
OV_{DD}	A14		
OV_{DD}	A20		
OV_{DD}	A26		
OV_{DD}	G01		
OV_{DD}	G07		
OV_{DD}	G13		
OV_{DD}	G14		
OV_{DD}	G20		
OV_{DD}	G26		
OV_{DD}	K11		
OV_{DD}	K13		
OV_{DD}	K14	Power	56
OV_{DD}	K16		
OV_{DD}	L10		
OV_{DD}	L17		
OV_{DD}	M13		
OV_{DD}	M14		
OV_{DD}	N01		
OV_{DD}	N07		
OV_{DD}	N10		
OV_{DD}	N12		
OV_{DD}	N15		
OV_{DD}	N17		
OV_{DD}	N20		
OV_{DD}	N26		

Table 3. Signals Listed Alphabetically (Sheet 13 of 25)

Signal Name	Ball	Interface Group	Page
PCIE_PLLGNDA	P02	Power	56
PCIE_PLLGNDB	N02		
PCIE_PLLVDD2	P09		
PCIE_PLLVDDA	P03		
PCIE_PLLVDDB	N03		
PCIE_REFCLK	P05	PCI-Express 0:2	50
$\overline{\text{PCIE\_REFCLK}}$	P06		
PCIE0_RX0	V11		
$\overline{\text{PCIE0\_RX0}}$	W11		
PCIE0_RX1	AB11		
$\overline{\text{PCIE0\_RX1}}$	AC11		
PCIE0_RX2	W12		
$\overline{\text{PCIE0\_RX2}}$	Y12		
PCIE0_RX3	AD12		
$\overline{\text{PCIE0\_RX3}}$	AD13		
PCIE0_RX4	AF15		
$\overline{\text{PCIE0\_RX4}}$	AF16		
PCIE0_RX5	AE16		
$\overline{\text{PCIE0\_RX5}}$	AD15		
PCIE0_RX6	V14		
$\overline{\text{PCIE0\_RX6}}$	W14		
PCIE0_RX7	W15		
$\overline{\text{PCIE0\_RX7}}$	W16		
PCIE0_TX0	Y11		
$\overline{\text{PCIE0\_TX0}}$	AA11		
PCIE0_TX1	AF11		
$\overline{\text{PCIE0\_TX1}}$	AE11		
PCIE0_TX2	AB12		
$\overline{\text{PCIE0\_TX2}}$	AA12		
PCIE0_TX3	AE13		
$\overline{\text{PCIE0\_TX3}}$	AF12		

Table 3. Signals Listed Alphabetically (Sheet 14 of 25)

Signal Name	Ball	Interface Group	Page
PCIE0_TX4	AE14	PCI-Express 0:2	50
$\overline{\text{PCIE0\_TX4}}$	AD14		
PCIE0_TX5	AB16		
$\overline{\text{PCIE0\_TX5}}$	AC16		
PCIE0_TX6	Y15		
$\overline{\text{PCIE0\_TX6}}$	AA15		
PCIE0_TX7	Y16		
$\overline{\text{PCIE0\_TX7}}$	AA16		
PCIE0AV25	V13		
PCIE0AVREG	W13		
PCIE1_RX0	E20		
$\overline{\text{PCIE1\_RX0}}$	E21		
PCIE1_RX1	B21		
$\overline{\text{PCIE1\_RX1}}$	C20		
PCIE1_RX2	C19		
$\overline{\text{PCIE1\_RX2}}$	D19		
PCIE1_RX3	A19		
$\overline{\text{PCIE1\_RX3}}$	B19		
PCIE1_TX0	C21		
$\overline{\text{PCIE1\_TX0}}$	D21		
PCIE1_TX1	A21		
$\overline{\text{PCIE1\_TX1}}$	B20		
PCIE1_TX2	C18		
$\overline{\text{PCIE1\_TX2}}$	D18		
PCIE1_TX3	A18		
$\overline{\text{PCIE1\_TX3}}$	B18		
PCIE1AV25	E19		
PCIE1AVREG	E18		

Table 3. Signals Listed Alphabetically (Sheet 15 of 25)

Signal Name	Ball	Interface Group	Page
PCIE2_RX0	J21	PCI-Express 0:2	50
$\overline{\text{PCIE2\_RX0}}$	K21		
PCIE2_RX1	J19		
$\overline{\text{PCIE2\_RX1}}$	K19		
PCIE2_RX2	F20		
$\overline{\text{PCIE2\_RX2}}$	F21		
PCIE2_RX3	F18		
$\overline{\text{PCIE2\_RX3}}$	F19		
PCIE2_TX0	L21		
$\overline{\text{PCIE2\_TX0}}$	L20		
PCIE2_TX1	J20		
$\overline{\text{PCIE2\_TX1}}$	H20		
$\overline{\text{PCIE2\_TX2}}$	G21		
PCIE2_TX2	H21		
$\overline{\text{PCIE2\_TX3}}$	G19		
PCIE2_TX3	H19		
PCIE2AV25	L18		
PCIE2AVREG	L19		
PCIECalRN	T08		
PCIECalRP	R08		
PCIEPLLTSTON	J01		

Table 3. Signals Listed Alphabetically (Sheet 16 of 25)

Signal Name	Ball	Interface Group	Page
PCIX0Ack64	AD02	PCI-X0	50
PCIX0AD0	AB04		
PCIX0AD1	AA05		
PCIX0AD10	AB02		
PCIX0AD11	AA03		
PCIX0AD12	W05		
PCIX0AD13	V06		
PCIX0AD14	AA02		
PCIX0AD15	AA01		
PCIX0AD16	W03		
PCIX0AD17	W04		
PCIX0AD18	V05		
PCIX0AD19	V04		
PCIX0AD2	Y06		
PCIX0AD20	V03		
PCIX0AD21	V02		
PCIX0AD22	V01		
PCIX0AD23	U06		
PCIX0AD24	T07		
PCIX0AD25	T06		
PCIX0AD26	T05		
PCIX0AD27	T04		
PCIX0AD28	T02		
PCIX0AD29	T01		
PCIX0AD3	V08		
PCIX0AD30	R07		
PCIX0AD31	R06		
PCIX0AD32	AD10		

Table 3. Signals Listed Alphabetically (Sheet 17 of 25)

Signal Name	Ball	Interface Group	Page
PCIX0AD33	AA10		
PCIX0AD34	W10		
PCIX0AD35	AF09		
PCIX0AD36	AF08		
PCIX0AD37	AD09		
PCIX0AD38	AF06		
PCIX0AD39	AD08		
PCIX0AD4	W07		
PCIX0AD40	AC09		
PCIX0AD41	AE06		
PCIX0AD42	AD07		
PCIX0AD43	AC08		
PCIX0AD44	AB09		
PCIX0AD45	AE05		
PCIX0AD46	AD06		
PCIX0AD47	AB08	PCI-X0	50
PCIX0AD48	AA09		
PCIX0AD49	Y09		
PCIX0AD5	AC02		
PCIX0AD50	AF03		
PCIX0AD51	AE04		
PCIX0AD52	AA08		
PCIX0AD53	W08		
PCIX0AD54	AB07		
PCIX0AD55	AF02		
PCIX0AD56	AE03		
PCIX0AD57	AD04		
PCIX0AD58	AC05		
PCIX0AD59	AE07		
PCIX0AD6	AA04		
PCIX0AD60	W09		

Table 3. Signals Listed Alphabetically (Sheet 18 of 25)

Signal Name	Ball	Interface Group	Page
PCIX0AD61	U08		
PCIX0AD62	AA07		
PCIX0AD63	AE02		
PCIX0AD7	Y05		
PCIX0AD8	W06		
PCIX0AD9	V07		
$\overline{\text{PCIX0BE0}}$	Y03		
$\overline{\text{PCIX0BE1}}$	Y02		
$\overline{\text{PCIX0BE2}}$	W02		
$\overline{\text{PCIX0BE3}}$	U03		
$\overline{\text{PCIX0BE4}}$	AB05		
$\overline{\text{PCIX0BE5}}$	AA06		
$\overline{\text{PCIX0BE6}}$	AC06		
$\overline{\text{PCIX0BE7}}$	AB06		
PCIX0CalG0	AE09	PCI-X0	50
PCIX0CalR0	AE08		
PCIX0Cap	M03		
PCIX0Clk	N05		
$\overline{\text{PCIX0DevSel}}$	N08		
PCIX0ECC2	R05		
PCIX0ECC3	R03		
PCIX0ECC4	R01		
PCIX0ECC5	P08		
$\overline{\text{PCIX0Frame}}$	N06		
$\overline{\text{PCIX0Gnt0}}$	T03		
$\overline{\text{PCIX0Gnt1}}$	E10		
$\overline{\text{PCIX0Gnt2}}$	M04		
$\overline{\text{PCIX0Gnt3}}$	R04		
PCIX0IDSel	U05		

Table 3. Signals Listed Alphabetically (Sheet 19 of 25)

Signal Name	Ball	Interface Group	Page
PCIX0INTA	U02	PCI-X0	50
PCIX0IRDY	AB01		
PCIX0M66En	A09		
PCIX0Par	W01		
PCIX0Par64	AD03		
PCIX0PErr	N09		
PCIX0PLLG	AE01		
PCIX0PLLV	AD01		
PCIX0Req0	R02		
PCIX0Req1	K02		
PCIX0Req2	K05		
PCIX0Req3	M02		
PCIX0Req64	AC03		
PCIX0Reset	L03		
PCIX0Serr	AF05		
PCIX0Stop	AD05		
PCIX0TRDY	AB03		
PCIX0VC	M01		
PCIX0VRef0	Y08		
PCIX0VRef1	T09		
PerAddr0	E13	External Slave Peripheral (EBC)	54
PerAddr1	E14		
PerAddr10	B16		
PerAddr11	E15		
PerAddr12	F11		
PerAddr13	D11		
PerAddr14	C10		
PerAddr15	B09		

Table 3. Signals Listed Alphabetically (Sheet 20 of 25)

Signal Name	Ball	Interface Group	Page
PerAddr16	C09	External Slave Peripheral (EBC)	54
PerAddr17	A08		
PerAddr18	B07		
PerAddr19	E11		
PerAddr2	B15		
PerAddr20	E09		
PerAddr21	C08		
PerAddr22	A06		
PerAddr23	D08		
PerAddr24	A22		
PerAddr25	E17		
PerAddr26	B17		
PerAddr3	D15		
PerAddr4	H16		
PerAddr5	H14		
PerAddr6	J14		
PerAddr7	J13		
PerAddr8	A15		
PerAddr9	F14		
$\overline{\text{PerBE0}}$	C07		
$\overline{\text{PerBE1}}$	B04		
$\overline{\text{PerBLast}}$	D16		
PerClk	C17		
$\overline{\text{PerCS0}}$	C15		
$\overline{\text{PerCS1}}$	C11		
$\overline{\text{PerCS2}}$	G12		
PerData00	G08		
PerData01	H10		
PerData02	B05		
PerData03	H11		
PerData04	C06		

Table 3. Signals Listed Alphabetically (Sheet 21 of 25)

Signal Name	Ball	Interface Group	Page
PerData05	J11	External Slave Peripheral (EBC)	54
PerData06	E08		
PerData07	F07		
PerData08	F09		
PerData09	E06		
PerData10	D05		
PerData11	C04		
PerData12	F08		
PerData13	B03		
PerData14	E07		
PerData15	D06		
PerErr	G15		
$\overline{\text{PerOE}}$	E05		
PerPar0	B06		
PerPar1	A03		
PerR/$\overline{\text{W}}$	F15		
PerReady	E16		
$\overline{\text{PerWE}}$	A16		
PSRO1	U10	Miscellaneous	57
PxVDD	P01	Power	56
PxVDD	P07		
PxVDD	P10		
PxVDD	P12		
PxVDD	R13		
PxVDD	T10		
PxVDD	U11		
PxVDD	U13		
PxVDD	Y01		
PxVDD	Y07		
PxVDD	Y13		

Table 3. Signals Listed Alphabetically (Sheet 22 of 25)

Signal Name	Ball	Interface Group	Page
PxVDD	AF01	Power	56
PxVDD	AF07		
PxVDD	AF13		
$\overline{\text{RAS}}$	AE23	DDR SDRAM	52
SCANOUT00	U25	Tests	56
SCANOUT07	U22		
SCANOUT08	P22		
SCANOUT14	AB10		
SCANOUT15	AE10		
SCANOUT16	AD11		
SCANOUT17	AC12		
SCANOUT18	AE12		
SCANOUT19	AB13		
SCANOUT20	AB14		
SCANOUT21	AE15		
SCANOUT25	M23		
SVDD	P15	Power	56
SVDD	P17		
SVDD	P20		
SVDD	P26		
SVDD	R14		
SVDD	T17		
SVDD	U14		
SVDD	U16		
SVDD	Y14		
SVDD	Y20		
SVDD	Y26		
SVDD	AF14		
SVDD	AF20		
SVDD	AF26		

Table 3. Signals Listed Alphabetically (Sheet 23 of 25)

Signal Name	Ball	Interface Group	Page
SYS2PLLG	AD26	Power	56
SYS2PLLV	AE26		
SYSClk	C16		
SYSErr	M25		
SysPartSel	A11		
SYSPLLG	B14		
SYSPLLV	B13		
$\overline{\text{SysReset}}$	L09	System	55
TCK	AA17	JTAG	56
TDI	AB15		
TDO	AD16		
TESTEN	E12		
THERMALDA	AA13	Miscellaneous	57
THERMALDB	AA14		
TMR_CLK	K08	System	55
TMS	AC15	JTAG	56
[TRCCLK] [GPIO00] High Z	L01	Trace Note: Trace can be enabled at reset by setting SDR0_SDSTP1[DBG] (bit 27) to 1 in the serial bootstrap ROM.	56
[TRCBS0] [GPIO01] High Z	H01		
[TRCBS1] [GPIO02] High Z	F01		
[TRCBS2] [GPIO03] High Z	L02		
[TRCES0] [GPIO04] High Z	K03		
[TRCES1] [GPIO05] High Z	G02		
[TRCES2] [GPIO06] High Z	M05		
[TRCES3] [GPIO07] High Z	F02		
[TRCES4] [GPIO08] High Z	J03		
[TRCTS0] [GPIO09] High Z	H04		
[TRCTS1] [GPIO10] High Z	J05		
[TRCTS2] [GPIO11] High Z	G05		
[TRCTS3] [GPIO12] High Z	L05		
[TRCTS4] [GPIO13] High Z	J04		
[TRCTS5] [GPIO14] High Z	K06		
[TRCTS6] [GPIO15] High Z	H06		
$\overline{\text{TRST}}$	AE17	JTAG	56

Table 3. Signals Listed Alphabetically (Sheet 24 of 25)

Signal Name	Ball	Interface Group	Page
UARTSerClk	H12		
$\overline{\text{UART0\_CTS}}$	B08		
$\overline{\text{UART0\_DCD}}$	H13		
$\overline{\text{UART0\_DSR}}$	C12		
$\overline{\text{UART0\_DTR}}$	C13		
$\overline{\text{UART0\_RI}}$	C14		
$\overline{\text{UART0\_RTS}}$	G09		
UART0_Rx	D12	UART Peripheral	55
UART0_Tx	D09		
$\overline{\text{UART1\_DSR/CTS}}$	F10		
$\overline{\text{UART1\_DTR/RTS}}$	G11		
UART1_Rx	A12		
UART1_Tx	B12		
UART2_Rx	F13		
UART2_Tx	F12		

Table 3. Signals Listed Alphabetically (Sheet 25 of 25)

Signal Name	Ball	Interface Group	Page
VDD	D04	Power	56
VDD	D10		
VDD	D17		
VDD	D23		
VDD	J10		
VDD	J17		
VDD	K04		
VDD	K09		
VDD	K18		
VDD	K23		
VDD	L12		
VDD	L15		
VDD	M11		
VDD	M16		
VDD	R11		
VDD	R16		
VDD	T12		
VDD	T15		
VDD	U04		
VDD	U09		
VDD	U18		
VDD	U23		
VDD	V10		
VDD	V17		
VDD	AC04		
VDD	AC10		
VDD	AC17		
VDD	AC23		
$\overline{WE}$	AC22	DDR SDRAM	52

Signal List—Ball Assignment Order

In the following table, only the primary (default) signal name is shown for each pin.

Multiplexed pins are marked with an asterisk (*). To determine the other signals that share a pin, look up the primary signal name in Table 3 on page 17.

Table 4. Signals Listed by Ball Assignment (Sheet 1 of 7)

Ball	Signal name	Ball	Signal name	Ball	Signal name	Ball	Signal name
A01	No ball	B01	EMCRxClk	C01	EMCTxEn	D01	GND
A02	IRQ9*	B02	EMCMDIO	C02	EMCTxClk	D02	EMCTxErr
A03	PerPar1	B03	PerData13	C03	EMCTxD0	D03	EMCCrS
A04	GND	B04	$\overline{\text{PerBE1}}$	C04	PerData11	D04	VDD
A05	EMCTxD3	B05	PerData02	C05	EMCTxD5	D05	PerData10
A06	PerAddr22	B06	PerPar0	C06	PerData04	D06	PerData15
A07	OV_{DD}	B07	PerAddr18	C07	$\overline{\text{PerBE0}}$	D07	GND
A08	PerAddr17	B08	$\overline{\text{UART0\_CTS}}$	C08	PerAddr21	D08	PerAddr23
A09	PCIX0M66En	B09	PerAddr15	C09	PerAddr16	D09	UART0_Tx
A10	GND	B10	EMCTxD7	C10	PerAddr14	D10	VDD
A11	SysPartSel	B11	$\overline{\text{ExtReset}}$	C11	$\overline{\text{PerCS1}}$	D11	PerAddr13
A12	UART1_Rx	B12	UART1_Tx	C12	$\overline{\text{UART0\_DSR}}$	D12	UART0_Rx
A13	OV_{DD}	B13	SYSPLLV	C13	$\overline{\text{UART0\_DTR}}$	D13	GND
A14	OV_{DD}	B14	SYSPLLG	C14	$\overline{\text{UART0\_RI}}$	D14	GND
A15	PerAddr8	B15	PerAddr2	C15	$\overline{\text{PerCS0}}$	D15	PerAddr3
A16	$\overline{\text{PerWE}}$	B16	PerAddr10	C16	SYSCLK	D16	$\overline{\text{PerBLast}}$
A17	GND	B17	PerAddr26	C17	PerClk	D17	VDD
A18	PCIE1_TX3	B18	$\overline{\text{PCIE1\_TX3}}$	C18	PCIE1_TX2	D18	$\overline{\text{PCIE1\_TX2}}$
A19	PCIE1_RX3	B19	$\overline{\text{PCIE1\_RX3}}$	C19	PCIE1_RX2	D19	$\overline{\text{PCIE1\_RX2}}$
A20	OV_{DD}	B20	$\overline{\text{PCIE1\_TX1}}$	C20	$\overline{\text{PCIE1\_RX1}}$	D20	GND
A21	PCIE1_TX1	B21	PCIE1_RX1	C21	PCIE1_TX0	D21	$\overline{\text{PCIE1\_TX0}}$
A22	PerAddr24	B22	MemData63	C22	GPIO28_IRQ12	D22	MemData54
A23	GND	B23	MemData61	C23	DM7	D23	VDD
A24	MemData59	B24	MemData58	C24	MemData56	D24	MemData55
A25	MemData62	B25	$\overline{\text{DQS7}}$	C25	DQS7	D25	MemData53
A26	OV_{DD}	B26	MemData60	C26	MemData57	D26	GND

Table 4. Signals Listed by Ball Assignment (Sheet 2 of 7)

Ball	Signal name	Ball	Signal name	Ball	Signal name	Ball	Signal name
E01	EMCTxD6	F01	TRCBS1*	G01	OV_{DD}	H01	TRCBS0*
E02	GPIO19_IRQ3	F02	TRCES3*	G02	TRCES1*	H02	EMCRxD3
E03	EMCTxD4	F03	EMCMDClk	G03	EMCRxD2	H03	EMCRxD4
E04	IRQ4*	F04	EMCRxErr	G04	GND	H04	TRCTS0*
E05	$\overline{\text{PerOE}}$	F05	EMCRxD7	G05	TRCTS2*	H05	EMCCD
E06	PerData09	F06	IRQ7*	G06	EMCTxD1	H06	TRCTS6*
E07	PerData14	F07	PerData07	G07	OV_{DD}	H07	EMCRefClk
E08	PerData06	F08	PerData12	G08	PerData00	H08	IRQ8*
E09	PerAddr20	F09	PerData08	G09	$\overline{\text{UART0\_RTS}}$	H09	IRQ5*
E10	$\overline{\text{PCIX0Gnt1}}$	F10	$\overline{\text{UART1\_DSR/CTS}}$	G10	GND	H10	PerData01
E11	PerAddr19	F11	PerAddr12	G11	$\overline{\text{UART1\_DTR/RTS}}$	H11	PerData03
E12	TESTEN	F12	UART2_Tx	G12	$\overline{\text{PerCS2}}$	H12	UARTSerClk
E13	PerAddr0	F13	UART2_Rx	G13	OV_{DD}	H13	$\overline{\text{UART0\_DCD}}$
E14	PerAddr1	F14	PerAddr9	G14	OV_{DD}	H14	PerAddr5
E15	PerAddr11	F15	PerR/$\overline{\text{W}}$	G15	PerErr	H15	IIC1SDA
E16	PerReady	F16	Reserved	G16	Reserved	H16	PerAddr4
E17	PerAddr25	F17	Reserved	G17	GND	H17	IIC0SClk
E18	PCIE1AVREG	F18	PCIE2_RX3	G18	Reserved	H18	IIC1SClk
E19	PCIE1AV25	F19	$\overline{\text{PCIE2\_RX3}}$	G19	$\overline{\text{PCIE2\_TX3}}$	H19	PCIE2_TX3
E20	PCIE1_RX0	F20	PCIE2_RX2	G20	OV_{DD}	H20	$\overline{\text{PCIE2\_TX1}}$
E21	$\overline{\text{PCIE1\_RX0}}$	F21	$\overline{\text{PCIE2\_RX2}}$	G21	$\overline{\text{PCIE2\_TX2}}$	H21	PCIE2_TX2
E22	$\overline{\text{DQS6}}$	F22	DQS6	G22	DM5	H22	MemData45
E23	MemData51	F23	MemData49	G23	GND	H23	MemData42
E24	IRQ11*	F24	DM6	G24	MemData43	H24	MemData44
E25	MemData52	F25	MemData50	G25	$\overline{\text{DQS5}}$	H25	DQS5
E26	IRQ10*	F26	MemData48	G26	OV_{DD}	H26	MemData41

Table 4. Signals Listed by Ball Assignment (Sheet 3 of 7)

Ball	Signal name	Ball	Signal name	Ball	Signal name	Ball	Signal name
J01	PCIEPLLTSTON	K01	GND	L01	TRCCLK*	M01	PCIX0VC
J02	EMCRxD1	K02	$\overline{\text{PCIX0Req1}}$	L02	TRCBS2*	M02	$\overline{\text{PCIX0Req3}}$
J03	TRCES4*	K03	TRCES0*	L03	$\overline{\text{PCIX0Reset}}$	M03	PCIX0Cap
J04	TRCTS4*	K04	VDD	L04	EMCRxD5	M04	$\overline{\text{PCIX0Gnt2}}$
J05	TRCTS1*	K05	$\overline{\text{PCIX0Req2}}$	L05	TRCTS3*	M05	TRCES2*
J06	EMCRxDV	K06	TRCTS5*	L06	EMCRxD0	M06	IRQ1*
J07	EMCTxD2	K07	GND	L07	IRQ6*	M07	EMCRxD6
J08	EMCGTxClk	K08	TMR_CLK	L08	IRQ0*	M08	IRQ2*
J09	GND	K09	VDD	L09	$\overline{\text{SysReset}}$	M09	GND
J10	VDD	K10	GND	L10	OV_{DD}	M10	GND
J11	PerData05	K11	OV_{DD}	L11	GND	M11	VDD
J12	GND	K12	GND	L12	VDD	M12	GND
J13	PerAddr7	K13	OV_{DD}	L13	GND	M13	OV_{DD}
J14	PerAddr6	K14	OV_{DD}	L14	GND	M14	OV_{DD}
J15	GND	K15	GND	L15	VDD	M15	GND
J16	IIC0SDA	K16	OV_{DD}	L16	GND	M16	VDD
J17	VDD	K17	GND	L17	OV_{DD}	M17	GND
J18	GND	K18	VDD	L18	PCIE2AV25	M18	GND
J19	PCIE2_RX1	K19	$\overline{\text{PCIE2\_RX1}}$	L19	PCIE2AVREG	M19	DM8
J20	PCIE2_TX1	K20	GND	L20	$\overline{\text{PCIE2\_TX0}}$	M20	ECC2
J21	PCIE2_RX0	K21	$\overline{\text{PCIE2\_RX0}}$	L21	PCIE2_TX0	M21	MemData38
J22	MemData47	K22	IRQ15*	L22	DQS4	M22	$\overline{\text{DQS4}}$
J23	MemData40	K23	VDD	L23	MemData35	M23	SCANOUT25
J24	MemData46	K24	MemData33	L24	IRQ13*	M24	MemData39
J25	MemData37	K25	IRQ14*	L25	MemData36	M25	SYSERR
J26	DM4	K26	GND	L26	MemData34	M26	MemData32

Table 4. Signals Listed by Ball Assignment (Sheet 4 of 7)

Ball	Signal name	Ball	Signal name	Ball	Signal name	Ball	Signal name
N01	OV_{DD}	P01	PxV_{DD}	R01	PCIX0ECC4	T01	PCIX0AD29
N02	PCIE_PLLGNDB	P02	PCIE_PLLGNDA	R02	$\overline{\text{PCIX0Req0}}$	T02	PCIX0AD28
N03	PCIE_PLLVDDB	P03	PCIE_PLLVDDA	R03	PCIX0ECC3	T03	$\overline{\text{PCIX0Gnt0}}$
N04	GND	P04	GND	R04	$\overline{\text{PCIX0Gnt3}}$	T04	PCIX0AD27
N05	PCIX0Clk	P05	PCIE_REFCLK	R05	PCIX0ECC2	T05	PCIX0AD26
N06	$\overline{\text{PCIX0Frame}}$	P06	$\overline{\text{PCIE\_REFCLK}}$	R06	PCIX0AD31	T06	PCIX0AD25
N07	OV_{DD}	P07	PxV_{DD}	R07	PCIX0AD30	T07	PCIX0AD24
N08	$\overline{\text{PCIX0DevSel}}$	P08	PCIX0ECC5	R08	PCIECalRP	T08	PCIECalRN
N09	$\overline{\text{PCIX0PErr}}$	P09	PCIE_PLLVDD2	R09	GND	T09	PCIX0VRef1
N10	OV_{DD}	P10	PxV_{DD}	R10	GND	T10	PxV_{DD}
N11	GND	P11	GND	R11	VDD	T11	GND
N12	OV_{DD}	P12	PxV_{DD}	R12	GND	T12	VDD
N13	GND	P13	GND	R13	PxV_{DD}	T13	GND
N14	GND	P14	GND	R14	SV_{DD}	T14	GND
N15	OV_{DD}	P15	SV_{DD}	R15	GND	T15	VDD
N16	GND	P16	GND	R16	VDD	T16	GND
N17	OV_{DD}	P17	SV_{DD}	R17	GND	T17	SV_{DD}
N18	ECC7	P18	ECC3	R18	GND	T18	MemData14
N19	ECC5	P19	ECC4	R19	ECC0	T19	DQS1
N20	OV_{DD}	P20	SV_{DD}	R20	ECC1	T20	MemData11
N21	ECC6	P21	$\overline{\text{DQS8}}$	R21	DQS8	T21	MemData09
N22	$\overline{\text{Halt}}$	P22	SCANOUT08	R22	MemData27	T22	MemData24
N23	GND	P23	GND	R23	MemAddr12	T23	MemData26
N24	MemData31	P24	$\overline{\text{DQS3}}$	R24	MemData25	T24	MemAddr03
N25	MemData29	P25	DQS3	R25	MemAddr08	T25	DM3
N26	OV_{DD}	P26	SV_{DD}	R26	MemData30	T26	MemData28

Table 4. Signals Listed by Ball Assignment (Sheet 5 of 7)

Ball	Signal name	Ball	Signal name	Ball	Signal name	Ball	Signal name
U01	GND	V01	PCIX0AD22	W01	PCIX0Par	Y01	PxV_{DD}
U02	$\overline{\text{PCIX0INTA}}$	V02	PCIX0AD21	W02	$\overline{\text{PCIX0BE2}}$	Y02	$\overline{\text{PCIX0BE1}}$
U03	$\overline{\text{PCIX0BE3}}$	V03	PCIX0AD20	W03	PCIX0AD16	Y03	$\overline{\text{PCIX0BE0}}$
U04	VDD	V04	PCIX0AD19	W04	PCIX0AD17	Y04	GND
U05	PCIX0IDSel	V05	PCIX0AD18	W05	PCIX0AD12	Y05	PCIX0AD7
U06	PCIX0AD23	V06	PCIX0AD13	W06	PCIX0AD8	Y06	PCIX0AD2
U07	GND	V07	PCIX0AD9	W07	PCIX0AD4	Y07	PxV_{DD}
U08	PCIX0AD61	V08	PCIX0AD3	W08	PCIX0AD53	Y08	PCIX0VRef0
U09	VDD	V09	GND	W09	PCIX0AD60	Y09	PCIX0AD49
U10	PSRO1	V10	VDD	W10	PCIX0AD34	Y10	GND
U11	PxV_{DD}	V11	PCIE0_RX0	W11	$\overline{\text{PCIE0\_RX0}}$	Y11	PCIE0_TX0
U12	GND	V12	GND	W12	PCIE0_RX2	Y12	$\overline{\text{PCIE0\_RX2}}$
U13	PxV_{DD}	V13	PCIE0AV25	W13	PCIE0AVREG	Y13	PxV_{DD}
U14	SV_{DD}	V14	PCIE0_RX6	W14	$\overline{\text{PCIE0\_RX6}}$	Y14	SV_{DD}
U15	GND	V15	GND	W15	PCIE0_RX7	Y15	PCIE0_TX6
U16	SV_{DD}	V16	MemVRef1	W16	$\overline{\text{PCIE0\_RX7}}$	Y16	PCIE0_TX7
U17	GND	V17	VDD	W17	$\overline{\text{BankSel3}}$	Y17	GND
U18	VDD	V18	GND	W18	MemVRef0	Y18	$\overline{\text{BankSel1}}$
U19	MemData08	V19	MemData10	W19	MemODT3	Y19	$\overline{\text{BankSel2}}$
U20	GND	V20	DM1	W20	MemODT2	Y20	SV_{DD}
U21	$\overline{\text{DQS1}}$	V21	MemData12	W21	MemODT0	Y21	ClkEn0
U22	SCANOUT07	V22	MemData13	W22	MemData15	Y22	MemODT1
U23	VDD	V23	MemData18	W23	$\overline{\text{DQS2}}$	Y23	GND
U24	MemData16	V24	MemData19	W24	DQS2	Y24	MemData20
U25	SCANOUT00	V25	DM2	W25	MemData17	Y25	MemData22
U26	GND	V26	MemData21	W26	MemData23	Y26	SV_{DD}

Table 4. Signals Listed by Ball Assignment (Sheet 6 of 7)

Ball	Signal name	Ball	Signal name	Ball	Signal name	Ball	Signal name
AA01	PCIX0AD15	AB01	PCIX0IRDY	AC01	GND	AD01	PCIX0PLLV
AA02	PCIX0AD14	AB02	PCIX0AD10	AC02	PCIX0AD5	AD02	PCIX0Ack64
AA03	PCIX0AD11	AB03	PCIX0TRDY	AC03	PCIX0Req64	AD03	PCIX0Par64
AA04	PCIX0AD6	AB04	PCIX0AD0	AC04	VDD	AD04	PCIX0AD57
AA05	PCIX0AD1	AB05	PCIX0BE4	AC05	PCIX0AD58	AD05	PCIX0Stop
AA06	PCIX0BE5	AB06	PCIX0BE7	AC06	PCIX0BE6	AD06	PCIX0AD46
AA07	PCIX0AD62	AB07	PCIX0AD54	AC07	GND	AD07	PCIX0AD42
AA08	PCIX0AD52	AB08	PCIX0AD47	AC08	PCIX0AD43	AD08	PCIX0AD39
AA09	PCIX0AD48	AB09	PCIX0AD44	AC09	PCIX0AD40	AD09	PCIX0AD37
AA10	PCIX0AD33	AB10	SCANOUT14	AC10	VDD	AD10	PCIX0AD32
AA11	PCIE0_TX0	AB11	PCIE0_RX1	AC11	PCIE0_RX1	AD11	SCANOUT16
AA12	PCIE0_TX2	AB12	PCIE0_TX2	AC12	SCANOUT17	AD12	PCIE0_RX3
AA13	THERMALDA	AB13	SCANOUT19	AC13	GND	AD13	PCIE0_RX3
AA14	THERMALDB	AB14	SCANOUT20	AC14	GND	AD14	PCIE0_TX4
AA15	PCIE0_TX6	AB15	TDI	AC15	TMS	AD15	PCIE0_RX5
AA16	PCIE0_TX7	AB16	PCIE0_TX5	AC16	PCIE0_TX5	AD16	TDO
AA17	TCK	AB17	MemAddr13	AC17	VDD	AD17	HISRRst
AA18	MemClkOut4	AB18	MemClkOut4	AC18	MemClkOut5	AD18	MemClkOut5
AA19	MemClkOut3	AB19	MemClkOut2	AC19	MemClkOut2	AD19	MemAddr10
AA20	MemClkOut0	AB20	MemClkOut3	AC20	GND	AD20	BankSel0
AA21	MemClkOut0	AB21	MemClkOut1	AC21	MemClkOut1	AD21	BA1
AA22	ClkEn1	AB22	CAS	AC22	WE	AD22	MemAddr02
AA23	DQS0	AB23	MemData07	AC23	VDD	AD23	MemData05
AA24	DQS0	AB24	MemAddr05	AC24	MemData02	AD24	MemData04
AA25	MemData03	AB25	MemData06	AC25	MemData00	AD25	DM0
AA26	MemData01	AB26	MemAddr11	AC26	GND	AD26	SYS2PLLG

Table 4. Signals Listed by Ball Assignment (Sheet 7 of 7)

Ball	Signal name	Ball	Signal name	Ball	Signal name	Ball	Signal name
AE01	PCIX0PLLG	AF01	PxV_{DD}				
AE02	PCIX0AD63	AF02	PCIX0AD55				
AE03	PCIX0AD56	AF03	PCIX0AD50				
AE04	PCIX0AD51	AF04	GND				
AE05	PCIX0AD45	AF05	$\overline{\text{PCIX0Serr}}$				
AE06	PCIX0AD41	AF06	PCIX0AD38				
AE07	PCIX0AD59	AF07	PxV_{DD}				
AE08	PCIX0CalR0	AF08	PCIX0AD36				
AE09	PCIX0CalG0	AF09	PCIX0AD35				
AE10	SCANOUT15	AF10	GND				
AE11	$\overline{\text{PCIE0\_TX1}}$	AF11	PCIE0_TX1				
AE12	SCANOUT18	AF12	$\overline{\text{PCIE0\_TX3}}$				
AE13	PCIE0_TX3	AF13	PxV_{DD}				
AE14	PCIE0_TX4	AF14	SV_{DD}				
AE15	SCANOUT21	AF15	PCIE0_RX4				
AE16	PCIE0_RX5	AF16	$\overline{\text{PCIE0\_RX4}}$				
AE17	$\overline{\text{TRST}}$	AF17	GND				
AE18	MemAddr07	AF18	MemAddr04				
AE19	MemAddr14	AF19	MemAddr01				
AE20	MemAddr09	AF20	SV_{DD}				
AE21	BA2	AF21	MemAddr06				
AE22	BA0	AF22	MemAddr00				
AE23	$\overline{\text{RAS}}$	AF23	GND				
AE24	MemDCFdbkD	AF24	MemDCFdbkR				
AE25	ClkEn2	AF25	ClkEn3				
AE26	SYS2PLLV	AF26	SV_{DD}				

Signal Description

The PPC440SPe embedded controller is packaged in a 27mm Flip-Chip Plastic Ball Grid Array (FC-PBGA). The following tables describe the package level pinout.

Table 5. Pin Summary

Group	No. of Pins
Total Signal Pins	**495**
AxV_{DD} (1.5V)	3
AxV_{DD} (2.5V HSS)	6
AxGND	5
OV_{DD} (3.3V I/Os)	23
PxV_{DD} (3.3/1.5V PCI)	14
SV_{DD} (2.5/1.8V SDRAM)	14
V_{DD} (1.5V logic)	28
GND	83
Total Power Pins	
Reserved	4
Total Pins	675

In the table “Signal Functional Description” on page 50, each I/O signal is listed along with a short description of its function. Active-low signals (for example, $\overline{RAS}$) are marked with an overline. See “Signals Listed Alphabetically” on page 17 for the pin (ball) number to which each signal is assigned.

Multiplexed Signals

Some signals are multiplexed on the same pin so that the pin can be used for different functions. The signal names shown in Table 6 on page 50 are not accompanied by signal names that might be multiplexed on the same pin. It is expected that in any single application a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

Strapping Pins

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Strapping” on page 77). Note that these are *not multiplexed* pins since the function of the pins is not programmable.

Multipurpose Signals

In addition to multiplexing, some pins are also multi-purpose. For example, the PCIX0Ack can function instead as PCIX0ECC1 depending on the PCI interface mode of operation.

Table 6. Signal Functional Description (Sheet 1 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
PCI-Express 0:2 Interfaces				
$\overline{\text{PCIE\_REFCLK}}$ PCIE_REFCLK	PCI Express Reference Clock: 100 MHz differential clock pair. Input type is controlled by bit 3 of the PESDR0_PLLLCT1[MCENT] register. 0 2.5V CMOS or LVDS 1 2.5V LVPECL (recommended)	I	Diff PECL	
PCIE0Tx[7:0] PCIE0Tx[7:0] PCIE1:2Tx[3:0] PCIE1:2Tx[3:0]	PCI Express Serial Data Transmit differential signals LSB is 0. X8 Mode: All $\overline{\text{PCIE0Tx[7:0]}}$/PCIE0Tx[7:0] are used. X4 Mode: Only $\overline{\text{PCIE0Tx[3:0]}}$/PCIE0Tx[3:0] are used.	O	Diff PECL	
PCIE0Rx[7:0] PCIE0Rx[7:0] PCIE1:2Rx[3:0] PCIE1:2Rx[3:0]	PCI Express Serial Data Receive differential signals LSB is 0. X8 Mode: All $\overline{\text{PCIE0Rx[7:0]}}$/PCIE0Rx[7:0] are used. X4 Mode: Only $\overline{\text{PCIE0Rx[3:0]}}$/PCIE0Rx[3:0] are used	I	Diff PECL	
PCIE0:2AVREG	PCI Express Analog Observation point for internal voltage regulator	O		
PCIECalRP PCIECalRN	Positive and negative inputs for a 1 Kohm ±1% PCI Express External calibration resistor	I		
PCIEPLLTSTON	Enable PCI Express PLL test modes.	I		
PCI-X0 Interfaces				
$\overline{\text{PCIX0Ack64}}$/PCIX0ECC1	Ack64 or ECC1. Normally used as Ack64 indicating that the target can transfer data using 64 bits. or Used as ECC1 for PCIX mode 2.	I/O	3.3V PCI or 1.5V PCI for mode 2	4
PCIX0AD63:00	Address/Data bus (bidirectional) for PCI-X0	I/O	3.3V PCI or 1.5V PCI for mode 2	
$\overline{\text{PCIX0BE7:0}}$	PCI-X Byte Enables for PCI-X0	I/O	3.3V PCI or 1.5V PCI for mode 2	
PCIX0CalG0 PCIX0CalR0	Balls G and R for a 114 Ohm External calibration resistor. Used to control PCI-X I/O Impedance at 57 Ohm.	I	NA	
PCIX0Cap	Capable of PCI-X operation. This analog input is sampled to configure PCI and determine the state of the PCIX0VC output signal: $0.00V_{DD}$ (0.0V) = Conventional PCI & PCIX0VC = 0 $0.49V_{DD}$ (1.0V) = PCI-X DDR 266 Mode 2 & PCIX0VC = 1 $0.75V_{DD}$ (2.5V) = PCI-X 66 & PCIX0VC = 0 $1.00V_{DD}$ (3.3V) = PCI-X 133 & PCIX0VC = 0	I	NA	

Table 6. Signal Functional Description (Sheet 2 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
PCIX0Clk	Input PCI & PCI-X Clock. **Note:** If the PCI-X interface is not being used, drive this pin with a 3.3V clock signal at a frequency between 1 and 66MHz	I	3.3V PCI	
$\overline{\text{PCIX0DevSel}}$	Indicates the driving device has decoded its address as the target of the current access.	I/O	3.3V PCI	4
PCIX0ECC5:2	ECC check bits 5–2. All ECC bits are valid only for PCIX DDR mode 2. **Note:** See PCIXPar for ECC0. See PCIXAck64 for ECC1. See PCIXReq64 for ECC6. See PCIXPar64 for ECC7.	I/O	3.3V PCI or 1.5V PCI for mode 2	
$\overline{\text{PCIX0Frame}}$	Driven by the current master to indicate beginning and duration of an access.	I/O	3.3V PCI	4
$\overline{\text{PCIX0Gnt0}}$ $\overline{\text{PCIX0Gnt1:3}}$	Indicates that the specified agent is granted access to the PCI-X bus. When Arbitration is internal to the PPC440SPe, all GRANTS Gnt0:3 are outputs. When arbitration is external, only Gnt 0 is used as an Input.	I/O O	3.3V PCI	4
PCIX0IDSel	Used as a chip select during configuration read and write transactions. If the PCI-X is a Host, during Configuration the ISDSEL is an Output that duplicates the AD17. The ISDSEL is always 3.3V even in Mode 2 DDR	I/O	3.3V PCI	5
$\overline{\text{PCIX0INTA}}$	Level sensitive PCI interrupt.	O	3.3V PCI	
$\overline{\text{PCIX0IRDY}}$	Indicates initiating agent's ability to complete the current data phase of the transaction.	I/O	3.3V PCI	4
PCIX0M66En	Capable of 66MHz operation.	I	3.3V PCI or 1.5V PCI for mode 2	
PCIX0Par/PCIX0ECC0	Even parity indicator or ECC0. Normally used to indicate even parity across PCIAD31:00 and BE3:0. Used as ECC0 for PCIX0 mode 2.	I/O	3.3V PCI or 1.5V PCI for mode 2	
PCIX0Par64/PCIX0ECC7	Even parity indicator or ECC7. Normally used to indicate even parity across PCIXAD63:32 and BE7:4 for PCIX0 or Used as ECC7 for PCIX0 mode 2.	I/O	3.3V PCI or 1.5V PCI for mode 2	
$\overline{\text{PCIX0PErr}}$	Reports data parity errors during all PCI transactions except a Special Cycle.	I/O	3.3V PCI	4
$\overline{\text{PCIX0Req0}}$ $\overline{\text{PCIX0Req1:3}}$	An indication to the PCI-X arbiter that the specified agent wishes to use the bus. When Arbitration is internal to the PPC440SPe, all REQS Req0:3 are Inputs. When arbitration is external, only Req 0 is used as an output.	I/O I	3.3V PCI	4

Table 6. Signal Functional Description (Sheet 3 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
$\overline{\text{PCIX0Req64/PCIX0ECC6}}$	Request 64-bit transfer or ECC6. Normally used by the current bus master to indicate a 64-bit transfer. Used as ECC6 for PCIX0 mode 2.	I/O	3.3V PCI or 1.5V PCI for mode 2	4
$\overline{\text{PCIX0Reset}}$	Sets PCI device registers and logic to a consistent state.	O	3.3V PCI	
$\overline{\text{PCIX0SErr}}$	Reports address parity errors, data parity errors on the Special Cycle command, or other catastrophic system errors.	I/O	3.3V PCI	4
$\overline{\text{PCIX0Stop}}$	Indicates the current target is requesting the master to stop the current transaction.	I/O	3.3V PCI	4
$\overline{\text{PCIX0TRDY}}$	Indicates the target agent's ability to complete the current data phase of the transaction.	I/O	3.3V PCI	4
PCIX0VC	Voltage control output. Used to control the voltage regulator supplying the PCI I/O voltage. See PCIX0Cap signal. 0 = 3.3V (PCI I/O) 1 =1.5V (PCI-X DDR)	O	3.3(1.5)V PCI	
PCIX0VRef0:1	Voltage reference input for PCI-X mode 2/DDR (1.5V) I/O. Not used for PCI or PCI-X mode 1.	I	VPCIXDDR	5
DDR SDRAM Interface				
BA0:2	Bank Address supporting up to 8 internal banks.	O	2.5(1.8)V DDR SDRAM	
$\overline{\text{BankSel0:3}}$	Selects up to four external DDR SDRAM banks.	O	2.5(1.8)V DDR SDRAM	
$\overline{\text{CAS}}$	Column Address Strobe.	O	2.5(1.8)V DDR SDRAM	
ClkEn0:3	Clock Enable. One for each external bank.	O	2.5(1.8)V DDR SDRAM	
DM0:8	Memory write data byte lane masks. MEMDM8 is the byte lane mask for the ECC byte lane.	O	2.5(1.8)V DDR SDRAM	
DQS0:8 $\overline{\text{DQS0:8}}$	Byte lane data strobe. DQS8 is the data strobe for the ECC byte lane. These signals are differential pairs.	I/O	2.5(1.8)V DDR SDRAM DIFF	
ECC0:7	ECC check bits 0:7.	I/O	2.5(1.8)V DDR SDRAM	
MemAddr14:00	Memory address bus. **Note:** MemAddr14 is the most significant bit (msb).	O	2.5(1.8)V DDR SDRAM	
MemClkOut0:5 $\overline{\text{MemClkOut0:5}}$	Subsystem clocks. The Clock signal (differential pair) is duplicated six times to support high loading: Six clocks can be used for two unbuffered DIMMS. Each individual clock signal can be enabled by programming the SDR0_DDRCLKSET register.	O	2.5(1.8)V DDR SDRAM DIFF	
MemData63:00	Memory data bus. **Note:** MemData63 is the most significant bit (msb).	I/O	2.5(1.8)V DDR SDRAM	

Table 6. Signal Functional Description (Sheet 4 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
MemDCFdbkD	Feedback driver, for I/O timing measurements.	O	2.5(1.8)V DDR SDRAM	
MemDCFdbkR	Feedback receiver. Connect externally to MemDCFdbkD.	I	2.5(1.8)V DDR SDRAM	
MemODT0:3	Memory on-die termination control	O	2.5(1.8)V DDR SDRAM	
MemVRef0	Memory reference voltage (SV_{REF}) input.	I	2.5(1.8)V DDR SDRAM Volt Ref Rcv	
MemVRef1	Memory reference voltage (SV_{REF}) supplemental input.	I	2.5(1.8)V DDR SDRAM Volt Ref Sup	
$\overline{RAS}$	Row Address Strobe.	O	2.5(1.8)V DDR SDRAM	
$\overline{WE}$	Write Enable.	O	2.5(1.8)V DDR SDRAM	
Ethernet Interface				
EMCCD	Collision detection.	I	3.3V LVTTL	
EMCCrS	Carrier sense.	I	3.3V LVTTL	
EMCMDClk	Management data clock.	O	3.3V LVTTL	
EMCMDIO	Transfer command and status information between MII and PHY.	I/O	3.3V LVTTL	
EMCRxD0:7	Receive data.	I	3.3V LVTTL	
EMCRxDV	Receive data valid.	I	3.3V LVTTL	
EMCRxErr	Receive error.	I	3.3V LVTTL	
EMCRxClk	Receive clock.	I	3.3V LVTTL	
EMCRefClk	Reference clock.Typical use: GMII Gigabit interface	I	3.3V LVTTL	
EMCTxClk	Transmit clock for 10/100 Mb/s.	I	3.3V LVTTL	
EMCGTxClk	Ethernet gigabit transmit clock. 125MHz to PHY	O	3.3V LVTTL	
EMCTxD0:7	Transmit data.	O	3.3V LVTTL	
EMCTxEn	Transmit data enabled.	O	3.3V LVTTL	
EMCTxErr	Transmit error.	O	3.3V LVTTL	

Table 6. Signal Functional Description (Sheet 5 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
External Slave Peripheral Interface - EBC				
PerAddr00:26	Peripheral address bus. **Note:** PerAddr00 is the most significant bit (msb).	O	3.3V LVTTL	1
$\overline{\text{PerBE0:1}}$	External peripheral data bus byte enable.	O	3.3V LVTTL	1
$\overline{\text{PerBLast}}$	Used by the peripheral controller to indicates the last transfer of a memory access.	O	3.3V LVTTL	
$\overline{\text{PerCS0:2}}$	External peripheral device select.	O	3.3V LVTTL	
PerData00:15	Peripheral data bus. **Note:** PerData0 is the most significant bit (msb).	I/O	3.3V LVTTL	1
$\overline{\text{PerOE}}$	Used by peripheral controller or DMA controller depending upon the type of transfer involved. When the PPC440SPe is the bus master, it enables the selected device to drive the bus.	O	3.3V LVTTL	
PerPar0:1	External peripheral data bus byte parity.	I/O	3.3V LVTTL	1
PerReady	Used by a peripheral slave to indicate it is ready to transfer data.	I	3.3V LVTTL	
PerR/$\overline{\text{W}}$	The peripheral controller set this signal to High for a Read from external memory, and to Low for a Write.	O	3.3V LVTTL	1
$\overline{\text{PerWE}}$	Write Enable.	O	3.3V LVTTL	
PerClk	Peripheral clock used by synchronous peripheral slaves.	O	3.3V LVTTL	
PerErr	External error used as an input to record external slave peripheral errors.	I	3.3V LVTTL	1, 5
IIC Peripheral Interface				
IIC0SClk	IIC0 Serial Clock.	I/O	3.3V IIC	1, 2
IIC0SDA	IIC0 Serial Data.	I/O	3.3V IIC	1, 2
IIC1SClk	IIC1 Serial Clock.	I/O	3.3V IIC	1, 2
IIC1SDA	IIC1 Serial Data.	I/O	3.3V IIC	1, 2

Table 6. Signal Functional Description (Sheet 6 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
UART Peripheral Interface				
UARTSerClk	Serial clock input that provides an alternative to the internally generated serial clock. Used in cases where the allowable internally generated clock rates are not satisfactory.	I	3.3V LVTTL	1, 4
UART0_Rx	UART0 Receive data.	I	3.3V LVTTL	1, 4
UART0_Tx	UART0 Transmit data.	O	3.3V LVTTL	4
$\overline{\text{UART0\_DCD}}$	UART0 Data Carrier Detect.	I	3.3V LVTTL	6
$\overline{\text{UART0\_DSR}}$	UART0 Data Set Ready.	I	3.3V LVTTL	6
$\overline{\text{UART0\_CTS}}$	UART0 Clear To Send.	I	3.3V LVTTL	1, 4, 6
$\overline{\text{UART0\_DTR}}$	UART0 Data Terminal Ready.	O	3.3V LVTTL	4
$\overline{\text{UART0\_RTS}}$	UART0 Request To Send.	O	3.3V LVTTL	4
$\overline{\text{UART0\_RI}}$	UART0 Ring Indicator.	I	3.3V LVTTL w/pull-up	1, 4
UART1_Rx	UART1 Receive data.	I	3.3V LVTTL	1, 4
UART1_Tx	UART1 Transmit data.	O	3.3V LVTTL	1, 4
$\overline{\text{UART1\_DSR}}$/$\overline{\text{CTS}}$	UART1 Data Set Ready or Clear To Send. The choice is determined by a DCR register bit setting.	I	3.3V LVTTL	1, 4
$\overline{\text{UART1\_DTR/RTS}}$	UART1 Request To Send or Data Terminal Ready. The choice is determined by a DCR register bit setting.	O	3.3V LVTTL	1, 4
UART2_Rx	UART2 Receive data.	I	3.3V LVTTL	1, 4
UART2_Tx	UART2 Transmit data.	O	3.3V LVTTL	1, 4
Interrupts Interface				
IRQ0:15	External interrupt Requests 0 through 15. These pins are multiplexed with GPIO16:31	I	3.3V LVTTL	1, 5
System Interface				
$\overline{\text{Halt}}$	Halt from external debugger.	I	3.3V LVTTL	1, 4
GPIO00:31	General purpose I/O 0 through 31. The GPIOs are multiplexed with IRQs, and Trace signal IO. Setting is done with the DCR register bits.	I/O	3.3V LVTTL	
SysClk	Main system clock input.	I	3.3V LVTTL	
SysErr	Set to 1 when a machine check is generated.	O	3.3V LVTTL	
SysPartSel	Not used.	I	NA	3
$\overline{\text{SysReset}}$	Main system reset. External logic can drive this pin low (minimum of 16 cycles) to initiate a system reset. A reset of the PPC440SPe can also be initiated by software.	I	3.3V LVTTL	1, 2
$\overline{\text{ExtReset}}$	External Reset. During the PPC440SPe's reset phase this signal is at down level.	O	3.3V LVTTL	

Table 6. Signal Functional Description (Sheet 7 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
$\overline{\text{HISRRst}}$	Hardware initiated system reset with an initial SDRAM self-refresh phase to save data in Memory.	I	3.3V LVTTL	1, 2
TESTEN	Test Enable.	I	3.3V LVTTL	3
TMR_CLK	Processor timer external input clock.	I	3.3V LVTTL	
JTAG Interface				
TCK	Test Clock.	I	3.3V LVTTL	1
TDI	Test Data In.	I	3.3V LVTTL w/pull-down	4
TDO	Test Data Out.	O	3.3V LVTTL	
TMS	Test Mode Select.	I	3.3V LVTTL with pull-up	1
$\overline{\text{TRST}}$	Test Reset. During chip power-up, this signal must be low from the start of VDD ramp-up until at least 16 SysClk cycles after VDD is stable in order to initialize the JTAG controller.	I	3.3V LVTTL with pull-up	5
Trace Interface				
TrcClk	Trace data capture clock, runs at 1/4 the frequency of the processor.	O	3.3V LVTTL	
TRCBS0:2	Trace branch execution status.	O	3.3V LVTTL	
TrcES0:4	Trace Execution Status is presented every fourth processor clock cycle.	O	3.3V LVTTL	
TrcTS0:6	Additional information on trace execution and branch status.	O	3.3V LVTTL	
Tests				
SCANOUT[00][07:08] [14:21] [25]	Test scan out Manufacturing test signals: No need for termination	n/a		
Power				
PCIE0:2AV25	2.5V supply voltage for the serial link of the PCI Express	I		
PCIE_PLLVDD2	2.5V supply voltage for the PCI Express Reference clock Input receiver in front of the PLL	I		
PCIE_PLLVDDA	Analog 2.5V filtered supply voltage A for the PLL of the PCI Express	I		
PCIE_PLLVDDB	Analog 2.5V filtered supply voltage B for the PLL of the PCI Express	I		
PCIE_PLLGNDA	GNDA for the PLL of the PCI Express	I		
PCIE_PLLGNDB	GNDB for the PLL of the PCI Express	I		
PCIX0PLLG	Ground for the PCI-X0 PLL	n/a	n/a	
PCIX0PLLV	Analog 1.5V Filtered Supply voltages input for PCI-X0 A separate filter for all analog voltages is recommended.	I	n/a	

Table 6. Signal Functional Description (Sheet 8 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
SYSPLLG	Ground for the SYS_PLL	n/a	n/a	
SYSPLLV	Analog 1.5V Filtered Supply voltages input for the SYS_PLL A separate filter for all analog voltages is recommended.	I	n/a	
SYS2PLLG	Ground for the DDR_PLL (SDRAM)	n/a	n/a	
SYS2PLLV	Analog 1.5V Filtered Supply voltages input for the DDR_PLL (SDRAM) A separate filter for all analog voltages is recommended.	I	n/a	
GND	Logic and I/O voltage ground.	n/a	n/a	
OV_{DD}	3.3V I/O supply (except DDR SDRAM and PCI-X).	n/a	n/a	
PxV_{DD}	PCI-X I/O voltage supply. 3.3 V for PCI and PCI-X 1.5 V for PCI-X 266 DDR Mode 2	n/a	n/a	
SV_{DD}	DDR SDRAM I/O voltage supply. 2.5V for DDR1 SDRAM 1.8V for DDR2 SDRAM	n/a	n/a	
V_{DD}	1.5V Logic voltage supply.	n/a	n/a	
Miscellaneous				
PSRO1	Performance Screen Ring Oscillator.	n/a	n/a	5
THERMALDA THERMALDB	On chip Diode for thermal monitoring. P diffusion on Pad A (In), and N on pad B (out)	I O		
Reserved	Do not connect voltage, ground, or any signals to these pins.	n/a	n/a	

Device Characteristics

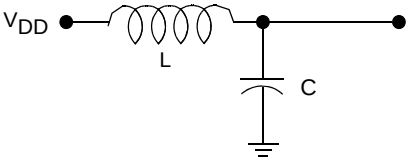
Table 7. Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. *Operation at or beyond these maximum ratings can cause permanent damage to the device. None of the performance specification contained in this document are guaranteed when operating at these maximum ratings.*

Characteristic	Symbol	Value	Unit	Notes
Supply Voltage (Internal logic)	V_{DD}	0 to +1.6	V	
Supply Voltage (I/O interface, except DDR SDRAM)	OV_{DD}	0 to +3.6	V	
Supply Voltage (PCI-X I/O)	PxV_{DD}	0 to +3.6	V	
Supply Voltage (PCI-X DDR I/O)	PxV_{DD}	0 to +1.6	V	
Supply Voltages (System PLLs)	AxV_{DD}	0 to +1.6	V	1
Supply Voltages (PCI-X PLLs)	$APxV_{DD}$	0 to +1.6	V	1
Supply Voltage (DDR SDRAM logic)	SV_{DD}	0 to +2.7	V	
Supply Voltage (DDR2 SDRAM logic)	SV_{DD}	0 to +1.95	V	
Input Voltage (3.3V LVTTL receivers)	V_{IN}	0 to +3.6	V	
Storage temperature range	T_{STG}	-55 to +150	°C	
Case temperature under bias	T_C	-40 to +120	°C	2

Notes:

1. The analog voltages used for the on-chip PLLs can be derived from the logic voltage, but must be filtered before entering the PPC440SPe. A separate filter, as shown below, is recommended for each voltage:



AxV_{DD}, $APxV_{DD}$	PCIE_PLLVDDA & B PCI Express
L – SMT ferrite bead chip, Murata BLM31A700S	Murata BLM15AG102SN1
C – 0.1µF ceramic	C – 1µF ceramic

2. This value is not a specification of the operational temperature range, it is a stress rating only.

Table 8. Package Thermal Specifications

Thermal resistance values for the PPC440SPe package in a convection environment are as follows:

Parameter	Symbol	Airflow ft/min (m/sec)			Unit	Notes
		0 (0)	100 (0.51)	200 (1.02)		
Junction-to-case thermal resistance	θ_{JC}	0.8	0.8	0.8	°C/W	1
Case-to-ambient thermal resistance (w/o heat sink)	θ_{CA}	15.5	13.1	11.9	°C/W	2
		Range				
		Minimum		Maximum		
Junction-to-ball (typical)	θ_{JB}	6.5		6.5	°C/W	3

Notes:

1. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board. For this part the junction temperature and the case temperature are essentially identical.
2. The case-to-ambient thermal resistance is measured in a JEDEC JESD51-6 standard environment; and may not accurately predict thermal performance in production equipment environments. The operational case temperature must be maintained.
3. 6.5 °C/W is the theoretical θ_{JB} using an infinite heat sink. The larger number applies to the module mounted on a 1.8mm thick, 2P card using 1oz. copper power planes, with an effective heat transfer area of 75mm^2.

Table 9. Recommended DC Operating Conditions (Sheet 1 of 3)

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage	V_{DD}	+1.425	+1.5	+1.575	V	4
I/O Supply Voltage	OV_{DD}	+3.0	+3.3	+3.6	V	4
PCI & PCI-X I/O Supply Voltage PCI-X DDR mode 2	PxV_{DD}	+3.0 +1.425	+3.3 +1.5	+3.6 +1.575	V	4
Voltage Reference Input for PCI-X DDR Mode 2	PCIX0VRef0:1	+1.425	+1.5	+1.575	V	4
DDR1 SDRAM Supply Voltage (DDR400) DDR2 SDRAM	SV_{DD}	+2.3 +1.7	+2.5 (2.6) +1.8	+2.7 +1.9	V	4
Analog System and DDR PLL Supply Voltages	AxV_{DD}	+1.4	+1.5	+1.6	V	3
Analog PCI Express PLL Supply voltage	$APExV_{DD}$	+ 1.65	+2.5	+2.75	V	
Analog PCI-X PLL Supply Voltages	$APxV_{DD}$	+1.4	+1.5	+1.6	V	3
DDR1 SDRAM Reference Voltage	SV_{REF}	+1.15	+1.25	+1.35	V	3
DDR2 SDRAM Reference Voltage	SV_{REF}	0.49 x SV_{DD}	0.50 x SV_{DD}	0.51 x SV_{DD}	V	

Table 9. Recommended DC Operating Conditions (Sheet 2 of 3)

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Input Logic High (2.5V DDR SDRAM)	V_{IH}	SV_{REF}+0.18		SV_{DD}+0.3	V	2
Input Logic High (1.8V DDR2 SDRAM)		SV_{REF}+0.125		SV_{DD}+0.3	V	
Input Logic High (2.5V CMOS, 3.3V tolerant receiver)		1.7			V	
Input Logic High (3.3V PCI-X)		0.5OV_{DD}		OV_{DD}+0.5	V	1
Input Logic High (1.5V PCI-X DDR)		-		-	V	1
Input Logic High (3.3V LVTTL)		+2.0		+3.6	V	
Input Logic Low (2.5V DDR SDRAM)	V_{IL}	-0.3		SV_{REF}-0.18	V	
Input Logic Low (1.8V DDR2 SDRAM)		-0.3		SV_{REF}-0.125	V	
Input Logic Low (2.5V CMOS, 3.3V tolerant receiver)				0.7	V	
Input Logic Low (3.3V PCI-X)		-0.5		0.35OV_{DD}	V	1
Input Logic Low (1.5V PCI-X DDR)		-		-	V	1
Input Logic Low (3.3V LVTTL)		0		+0.8	V	
Output Logic High (2.5V DDR SDRAM)	V_{OH}	+1.95		SV_{DD}	V	
Output Logic High (1.8V DDR2 SDRAM)		SV_{DD}-0.45		SV_{DD}	V	
Output Logic High (2.5V CMOS, 3.3V tolerant receiver)		2.0			V	
Output Logic High (3.3V PCI-X)		0.9OV_{DD}		OV_{DD}	V	1
Output Logic High (1.5V PCI-X DDR)		-		-	V	1
Output Logic High (3.3V LVTTL)		+2.4		OV_{DD}	V	
Output Logic Low (2.5V DDR SDRAM)	V_{OL}	0		0.45	V	
Output Logic Low (1.8V DDR2 SDRAM)		0		0.45	V	
Output Logic Low (2.5V CMOS, 3.3V tolerant receiver)				0.4	V	
Output Logic Low (3.3V PCI-X)				0.1OV_{DD}	V	1
Output Logic Low (1.5V PCI-X DDR)		-		-	V	1
Output Logic Low (3.3V LVTTL)		0		+0.4	V	
Input Leakage Current (with no internal pull-up or pull-down)	I_{IL1}	0		1	µA	
Input Leakage Current (with internal pull-down)	I_{IL2}	0 (LPDL)		200 (MPUL)	µA	5
Input Leakage Current (with internal pull-up)	I_{IL3}	-150 (LPDL)		0 (MPUL)	µA	5

Table 9. Recommended DC Operating Conditions (Sheet 3 of 3)

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Input Max Allowable Overshoot (3.3V LVTTL)	V_{IMAO}			+3.9	V	
Input Max Allowable Undershoot (3.3V LVTTL)	V_{IMAU}	-0.6			V	
Output Max Allowable Overshoot (3.3V LVTTL)	V_{OMAO}			+3.9	V	
Output Max Allowable Undershoot (3.3V LVTTL)	V_{OMAU3}	-0.6			V	
Case Temperature	T_C	0		+95	°C	6

Notes:

1. PCI-X drivers meet PCI-X specifications.
2. $SV_{REF} = SV_{DD}/2$
3. The analog voltages used for the on-chip PLLs can be derived from the logic voltage, but must be filtered before entering the PPC440SPe. See “Absolute Maximum Ratings” on page 58.
4. During chip power-up, OV_{DD} should begin to ramp before VDD. External voltage should not be applied to the chip I/O pins before OV_{DD} is applied to the chip. A power-down cycle should complete (OV_{DD} and VDD should both be below 0.4V) before a new power up cycle is started.
5. LPDL is least positive down level; MPUL is most positive up level.
6. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.

Table 10. Input Capacitance

Parameter	Symbol	Maximum	Unit	Notes
Group 1 (2.5V SSTL I/O)	C_{IN1}	5.7	pF	
Group 2 (3.3V LVTTL I/O)	C_{IN2}	6.8	pF	
Group 3 (PCI-X I/O)	C_{IN3}	5.1	pF	
Group 4 (Receivers)	C_{IN4}	6.7	pF	
Group 5 (3.3V tolerant CMOS I/O)	C_{IN5}	2.6	pF	

Table 11. DC Power Supply Loads

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
V_{DD} (1.5V) active operating current	I_{DD}			3000	mA	2
OV_{DD} (3.3V) active operating current	I_{ODD}			30	mA	2
PxV_{DD} (3.3V) active operating current	I_{PDD}	-	-	-	mA	2
PxV_{DD} (1.5V) active operating current	I_{PDD}	-	-	1200	mA	
SV_{DD} (2.5V) active operating current	I_{SDD}			285	mA	2
SV_{DD} (1.8V) active operating current	I_{SDD}			580	mA	2
AxV_{DD} (1.5V) input current	I_{ADD}		33		mA	1, 2
$APxV_{DD}$ (1.5V) input current	I_{APDD}		33		mA	1, 2
Notes: 1. See “Absolute Maximum Ratings” on page 58 for filter recommendations. 2. Valid only for CPU/PLB/OPB = 533.33/133.33/66.66 MHz.						

Clock Test Conditions

Clock timing and switching characteristics are specified in accordance with operating conditions shown in the table “Recommended DC Operating Conditions.” AC specifications are characterized with V_{DD} = 1.5V, T_C = +95 °C and a 10pF test load as shown in the figure to the right.

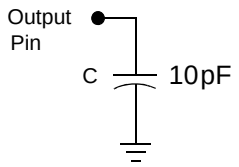


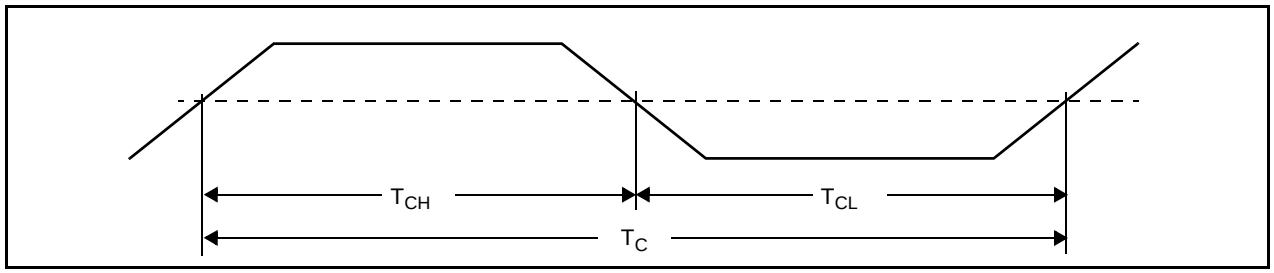
Table 12. Clocking Specifications

Symbol	Parameter	Min	Max	Units
SysClk Input				
F_C	Frequency	33.33	83.33	MHz
T_C	Period	12	30	ns
T_{CS}	Edge stability (cycle-to-cycle jitter)	–	±0.15	ns
T_{CH}	High time	40% of nominal period	60% of nominal period	ns
T_{CL}	Low time	40% of nominal period	60% of nominal period	ns
Note: Input slew rate ≥ 1V/ns				
PLL VCO				
F_C	Frequency	600	1333.33	MHz
T_C	Period	0.75	1.66	ns

Table 12. Clocking Specifications

Symbol	Parameter	Min	Max	Units
Processor Clock (CPU Clock)				
F_C	Frequency	400	666.66	MHz
T_C	Period	1.5	2.5	ns
MemClkOut				
F_C	Frequency	200	333.33	MHz
T_C	Period	3	5	ns
T_{CH}	High time	45% of nominal period	55% of nominal period	ns
OPB Clock and PerClk				
F_C	Frequency	–	83.33	MHz
T_C	Period	12	–	ns
MAL Clock				
F_C	Frequency	45	83.33	MHz
T_C	Period	12	22.2	ns

Figure 4. Clock Timing Waveform



Spread Spectrum Clocking

Care must be taken when using a spread spectrum clock generator (SSCG) with the PPC440SPe. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is referred to as tracking skew. The PLL bandwidth and phase angle determine how much tracking skew there is between the SSCG and the PLL for a given frequency deviation and modulation frequency. When using an SSCG with the PPC440SPe the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the PPC440SPe with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation cannot exceed -1%, and the modulation frequency cannot exceed 40kHz. In some cases, on-board PPC440SPe peripherals impose more stringent requirements.
- Use the Peripheral Bus Clock for logic that is synchronous to the peripheral bus since this clock tracks the modulation.
- Use the DDR SDRAM MemClkOut since it also tracks the modulation.

- For PCI-X and PCI 66 the maximum spread spectrum is -1% modulated between 30kHz and 33kHz.
- For PCI Express, the maximum spread spectrum is **-0.5%,** modulated between 30kHz and 33kHz. The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/- 300 ppm tolerance.

Notes:

1. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur. The 1.5% tolerance assumes that the connected device is running at precise baud rates.
2. Ethernet operation is unaffected.
3. IIC operation is unaffected.

Important: It is up to the system designer to ensure that any SSCG used with the PPC440SPe meets the above requirements and does not adversely affect other aspects of the system.

I/O Specifications

Table 13. Peripheral Interface Clock Timings

Parameter	Min	Max	Units	Notes
PCIX0Clk input frequency (asynchronous mode)	–	133.33	MHz	2
PCIX0Clk period (asynchronous mode)	7.5	–	ns	
PCIX0Clk input high time	40% of nominal period	60% of nominal period	ns	
PCIX0Clk input low time	40% of nominal period	60% of nominal period	ns	
EMCMDClk output frequency	–	2.5	MHz	
EMCMDClk period	400	–	ns	
EMCMDClk output high time	160	–	ns	
EMCMDClk output low time	160	–	ns	
EMCTxClk input frequency	2.5	25	MHz	
EMCTxClk period	40	400	ns	
EMCTxClk input high time	35% of nominal period	–	ns	
EMCTxClk input low time	35% of nominal period	–	ns	
EMCRxClk input frequency	2.5	25	MHz	
EMCRxClk period	40	400	ns	
EMCRxClk input high time	35% of nominal period	–	ns	
EMCRxClk input low time	35% of nominal period	–	ns	
PerClk output frequency (for sync. slaves)	–	83.33	MHz	
PerClk period	12	–	ns	
PerClk output high time	50% of nominal period	66% of nominal period	ns	
PerClk output low time	33% of nominal period	50% of nominal period	ns	
UARTSerClk input frequency	–	$1000/(2T_{OPB}^{1}+2ns)$	MHz	1
UARTSerClk period	$^{2}T_{OPB}+2$	–	ns	1
UARTSerClk input high time	$T_{OPB}+1$	–	ns	1
UARTSerClk input low time	$T_{OPB}+1$	–	ns	1
TmrClk input frequency	–	100	MHz	
TmrClk period	10	–	ns	
TmrClk input high time	40% of nominal period	60% of nominal period	ns	
TmrClk input low time	40% of nominal period	60% of nominal period	ns	

Notes:

1. T_{OPB} is the period in ns of the OPB clock. The internal OPB clock runs at an integral divisor ratio of the frequency of the PLB clock. The maximum OPB clock frequency is 83.33 MHz. Refer to the Clocking chapter of the *PPC440SPe Embedded Processor User's Manual* for details.
2. When the PCI-X interface is used to support a legacy PCI interface, the maximum PCIXClk frequency is 66.66MHz.

Input/Output Timing

These timing diagrams illustrate the relationship of the timing parameters defined in the I/O Specification tables that follow.

Figure 5. Input Setup and Hold Waveform

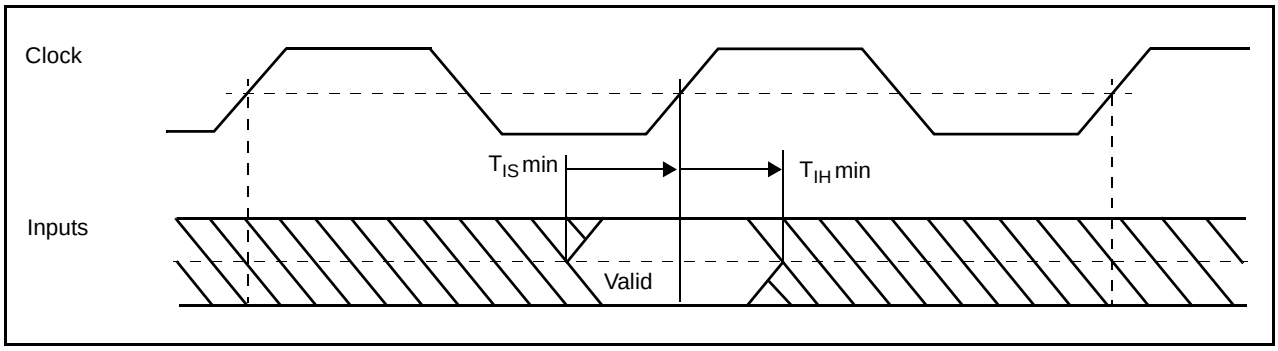


Figure 6. Output Delay and Hold Timing Waveform

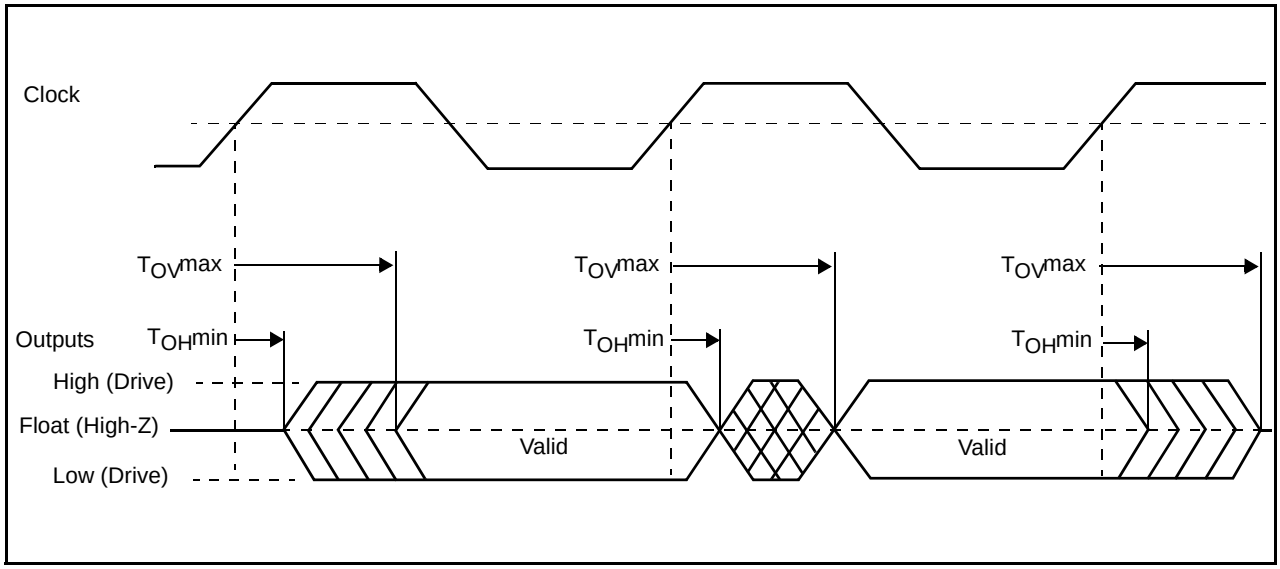


Table 14. I/O Specifications—All Speeds (Sheet 1 of 2)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PCI-X timings are for asynchronous operation up to 133.33MHz. PCI-X input setup time requirement is 1.2ns for 133.33MHz and 1.7ns for 66.66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66.66MHz. PCI output hold time requirement is 1ns for 66.66MHz and 2ns for 33.33MHz.
3. These are DDR signals that can change on both the positive and negative clock transitions.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
PCI-X Interface								
PCIX0Ack64	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIX0AD63:00	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIX0BE7:0	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIX0CalG0:1	Note 2 (2)	0.5(0)	n/a	n/a	n/a	n/a	PCIX0Clk	2
PCIX0CalR0:1	dc	dc	n/a	n/a	n/a	n/a		async
PCIX0Cap	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIX0Clk	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIX0DevSel	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIX0ECC5:2	n/a	n/a	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIX0Frame	n/a	n/a	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIX0Gnt0	n/a	n/a	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIX0Gnt1	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIX0Gnt2:3	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIX0IDSel	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIX0INTA	Note 2 (2)	0.5(0)	n/a	n/a	n/a	n/a	PCIX0Clk	2
PCIX0IRDY	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIX0M66En	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIXPar	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIXPar64	Note 2 (2)	0.5(0)	n/a	n/a	n/a	n/a	PCIX0Clk	2
PCIX0PErr	Note 2 (2)	0.5(0)	n/a	n/a	n/a	n/a	PCIX0Clk	2
PCIX0Req0	Note 2 (2)	0.5(0)	n/a	n/a	n/a	n/a	PCIX0Clk	2
PCIX0Req1:3	n/a	n/a	n/a	n/a	n/a	n/a	PCIX0Clk	2
PCIX0Req64	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIX0Reset	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIX0SErr	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIX0Stop	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIX0TRDY	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
PCIX0VC	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0Clk	2
Ethernet Interface								
EMCCD	-	-	na	na	19.1	8.7		1, async
EMCCrS	-	-	na	na	19.1	8.7		1, async
EMCMDClk	na	na	na	na	19.1	8.7		1, async
EMCMDIO	-	-	-	-	19.1	8.7	EMCMDClk	
EMCRxD0:7	4	1	na	na	19.1	8.7	EMCRxClk	
EMCRxDV	4	1	na	na	19.1	8.7	EMCRxClk	
EMCRxErr	-	-	na	na	19.1	8.7	EMCRxClk	
EMCRxClk	-	-	na	na	19.1	8.7		1, async
EMCRefClk	-	-	na	na	19.1	8.7		
EMCTxClk	na	na	na	na	19.1	8.7		1, async
EMCGTxClk	na	na	na	na	19.1	8.7		1, async
EMCTxD0:7	na	na	15	2	19.1	8.7	EMCTxClk	

Table 14. I/O Specifications—All Speeds (Sheet 2 of 2)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PCI-X timings are for asynchronous operation up to 133.33MHz. PCI-X input setup time requirement is 1.2ns for 133.33MHz and 1.7ns for 66.66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66.66MHz. PCI output hold time requirement is 1ns for 66.66MHz and 2ns for 33.33MHz.
3. These are DDR signals that can change on both the positive and negative clock transitions.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
EMCTxEn	na	na	15	2	19.1	8.7	EMCTxClk	
EMCTxErr	na	na	15	2	19.1	8.7	EMCTxClk	
Internal Peripheral Interface								
IIC0SClk	n/a	n/a	n/a	n/a	15.3	10.2		
IIC0SDA	-	-	-	-	15.3	10.2	IIC0SClk	
IIC1SClk	n/a	n/a	n/a	n/a	15.3	10.2		
IIC1SDA	-	-	-	-	15.3	10.2	IIC0SClk	
UARTSerClk	n/a	n/a	n/a	n/a	19.1	8.7		
UART0_Rx	-	-	n/a	n/a	-	-	UARTSerClk	
UART0_Tx	n/a	n/a	-	-	19.1	8.7	UARTSerClk	
UART0_DCD	-	-	n/a	n/a	19.1	8.7	async	
UART0_DSR	-	-	n/a	n/a	19.1	8.7	async	
UART0_CTS	-	-	n/a	n/a	19.1	8.7	async	
UART0_DTR	n/a	n/a			19.1	8.7	async	
UART0_RI	-	-	n/a	n/a	-	-	async	
UART0_RTS	n/a	n/a			19.1	8.7	async	
UART1_Rx			n/a	n/a	19.1	8.7	UARTSerClk	
UART1_Tx	n/a	n/a	-	-	19.1	8.7	UARTSerClk	
UART1_DSR/CTS	-	-	n/a	n/a	19.1	8.7	async	
UART1_DTR/RTS	n/a	n/a			19.1	8.7	async	
UART2_Rx	-	-	n/a	n/a	19.1	8.7	UARTSerClk	
UART2_Tx	n/a	n/a	-	-	19.1	8.7	UARTSerClk	
Interrupts Interface								
IRQ0:15	-	-	-	-	n/a	n/a	async	
JTAG Interface								
TDI	-	-	na	na	na	na	async	
TMS	-	-	na	na	na	na	async	
TDO	na	na	-	-	19.1	8.7	async	
TCK	-	-	na	na	na	na	async	
TRST	-	-	na	na	na	na	async	
System Interface								
Halt	-	-	n/a	n/a	n/a	n/a	async	
GPIO00:31	-	-	-	-	19.1	8.7	async	
SysClk	-	-	n/a	n/a	n/a	n/a	na	
SysErr	n/a	n/a	-	-	19.1	8.7	async	
SysReset	-	-	-	-	n/a	n/a	async	
HISRRst	-	-	-	-	19.1	8.7	async	
TESTEN	-	-	n/a	n/a	n/a	n/a	async	
TmrClk	-	-	n/a	n/a	n/a	n/a	na	
Trace Interface								
TrcClk	n/a	n/a	-	-	19.1	8.7		
TRCBS0:2	-	-	-	-	19.1	8.7		
TrcES0:4	-	-	-	-	19.1	8.7		
TrcTS0:6	-	-	-	-	19.1	8.7		

Table 15. I/O Specifications—667MHz

Notes:
1. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 1.3ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
External Slave Peripheral Interface								
PerAddr00:26	n/a	1	6.2	0	19.1	8.7	PerClk	
PerBE0:1	-	-	-	-	27.7	12.8	PerClk	
PerBLast	n/a	1	5.7	n/a	19.1	8.7	PerClk	
PerCS0:2	n/a	n/a	5.9	0	19.1	8.7	PerClk	
PerData0:15	1.2	1	6	0	19.1	8.7	PerClk	
PerOE	n/a	n/a	5.8	0	19.1	8.7	PerClk	
PerPar0:1	1.7	1	5.7	n/a	19.1	8.7	PerClk	
PerReady	3.6	1	n/a	n/a	19.1	8.7	PerClk	
PerR/W	n/a	1	5.7	n/a	19.1	8.7	PerClk	
PerWE	n/a	n/a	5.7	0	19.1	8.7	na	
ExtReset	n/a	n/a	n/a	n/a	19.1	8.7	PerClk	
PerClk	n/a	n/a	n/a	n/a	19.1	8.7	PLB clk	
PerErr	1.2		n/a	n/a	19.1	8.7	PerClk	

DDR SDRAM I/O Specifications

The DDR SDRAM controller times its operation with internal PLB clock signals and generates MemClkOut0 from the PLB clock. The PLB clock is an internal signal that cannot be directly observed. However MemClkOut0 is the same frequency as the PLB clock signal and is in phase with the PLB clock signal.

Note: MemClkOut0 can be advanced with respect to the PLB clock by means of the SDRAM0_CLKTR programming register. In a typical system, users advance MemClkOut by 90°. This depends on the specific application and requires a thorough understanding of the memory system in general (refer to the DDR SDRAM controller chapter in the *PPC440SPe Embedded Processor User's Manual*).

In the following sections, the label MemClkOut0(0) refers to MemClkOut0 when it has not been phase-shifted, and MemClkOut0(90) refers to MemClkOut0 when it has been phase-advanced 90°. Advancing MemClkOut0 by 90° creates a 3/4 cycle setup time and 1/4 cycle hold time for the address and control signals in relation to MemClkOut0(90). The rising edge of MemClkOut0(90) aligns with the first rising edge of the DQS signal.

The following DDR data is generated by means of *simulation* and includes logic, driver, package RLC, and lengths. It is *not* to be used as a circuit design recommendation. Values are calculated over best case and worst case processes with speed, temperature, and voltage as follows:

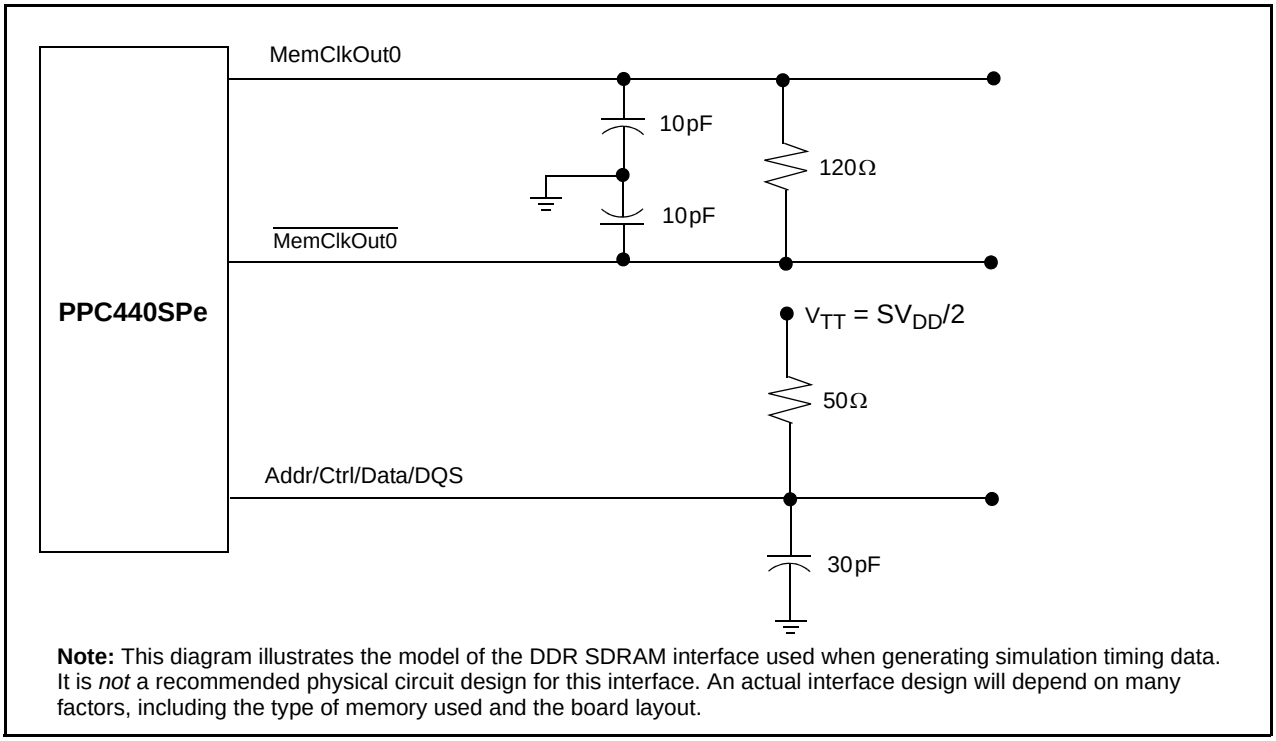
Best Case = Fast process, 0°C, +1.6V

Worst Case = Slow process, +95°C, +1.4V

Note: In all the following DDR tables and timing diagrams, *minimum* values are measured under *best* case conditions and *maximum* values are measured under *worst* case conditions.

The signals are terminated as indicated in the figure below for the DDR timing data in the following sections.

Figure 7. DDR SDRAM Signal Termination



Note: This diagram illustrates the model of the DDR SDRAM interface used when generating simulation timing data. It is *not* a recommended physical circuit design for this interface. An actual interface design will depend on many factors, including the type of memory used and the board layout.

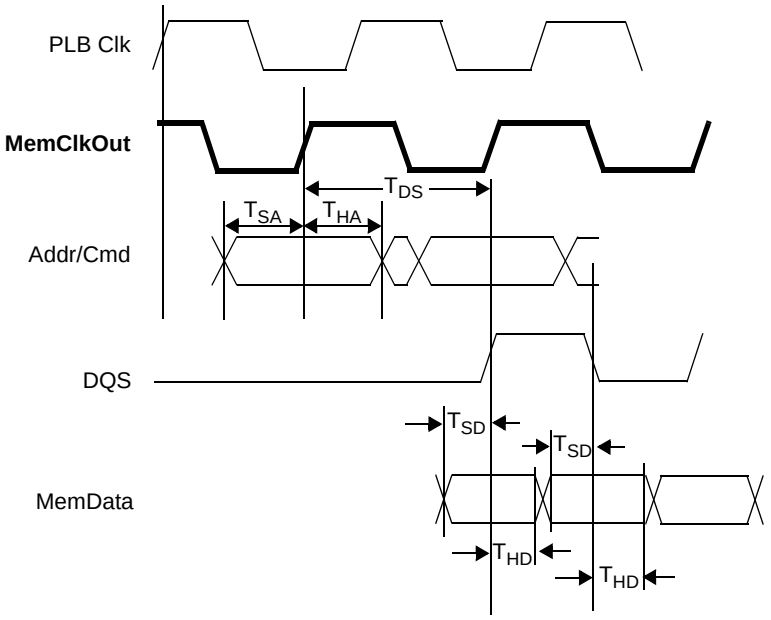
Table 16. DDR SDRAM Output Driver Specifications

Signal Path	Output Current (mA)	
	I/O H (maximum)	I/O L (minimum)
Write Data		
MemData00:07	15.2	15.2
MemData08:15	15.2	15.2
MemData16:23	15.2	15.2
MemData24:31	15.2	15.2
MemData32:39	15.2	15.2
MemData40:47	15.2	15.2
MemData48:55	15.2	15.2
MemData56:63	15.2	15.2
ECC0:7	15.2	15.2
DM0:8	15.2	15.2
MemClkOut0	15.2	15.2
MemAddr00:12	15.2	15.2
BA0:1	15.2	15.2
$\overline{\text{RAS}}$	15.2	15.2
$\overline{\text{CAS}}$	15.2	15.2
$\overline{\text{WE}}$	15.2	15.2
$\overline{\text{BankSel0:3}}$	15.2	15.2
ClkEn0:3	15.2	15.2
DQS0:8	15.2	15.2

DDR SDRAM Write Operation

The following timing chart shows the relationship between the signals involved in a DDR write operation.

Figure 8. DDR SDRAM Write Cycle Timing



T_{SA} = Setup time for address and command signals to MemClkOut
T_{HA} = Hold time for address and command signals from MemClkOut
T_{SD} = Setup time for data signals (minimum time data is valid *before* rising/falling edge of DSQ)
T_{HD} = Hold time for data signals (minimum time data is valid *after* rising/falling edge of DSQ)
T_{DS} = Delay from rising/falling edge of clock to the rising/falling edge of DQS

DDR SDRAM Read and Write I/O Timing—T_{SA} and T_{HA}

Note 1: Clock speed is 333 MHz. T_{SA} and T_{HA} are referenced to MemClkOut.

Note 2: Memory clock signal is shifted by 90° from the internal clock.

Table 17. DDR SDRAM Read and Write I/O Timing—T_{SA} and T_{HA}

Signal Name	T_{SA} (ns)	T_{HA} (ns)
	Minimum	Minimum
MemAddr00:12	1.32	1.2
BA0:1	1.15	1.49
BankSel0:3	1.12	1.52
ClkEn0:3	1.29	1.45
$\overline{CAS}$	1.24	1.14
$\overline{RAS}$	1.29	1.48
$\overline{WE}$	1.35	1.43

DDR SDRAM Clock to Write DQS Timing—T_{DS}

Note 1: All of the DQS signals are referenced to MemClkOut.

Note 2: Clock speed is 333 MHz.

Note 3: The TDS values in the table include 1.5 × 3ns cycle at 333 MHz (3 ns × 1.5 = 4.5 ns).

Note 4: To obtain adjusted values for lower clock frequencies, subtract 4 ns from the values in the following table and add × 1.5 of the cycle time for the lower clock frequency (T_{DS} - 4.5 + 1.5 T_{CYC}).

Table 18. DDR SDRAM Clock to Write DQS Timing—T_{DS}

Signal Name	T_{DS} (ns)	
	Minimum	Maximum
DQS0	4.76	5.07
DQS1	4.78	5.09
DQS2	4.78	5.10
DQS3	4.76	5.07
DQS4	4.79	5.11
DQS5	4.80	5.13
DQS6	4.81	5.11
DQS7	4.79	5.11
DQS8	4.77	5.07

DDR SDRAM Write Data to DQS Timing—T_{SD} and T_{HD}

Note 1: T_{SD} and T_{HD} are measured under worst-case conditions.

Note 2: Clock speed for the values in the following table is 333 MHz.

Table 19. DDR SDRAM Write Data to DQS Timing—T_{SD} and T_{HD}

Signal Name	Reference Signal	T_{SD} (ns)	T_{HD} (ns)
MemData00:07, DM0	DQS0	0.58	0.64
MemData08:15, DM1	DQS1	0.62	0.55
MemData16:23, DM2	DQS2	0.62	0.60
MemData24:31, DM3	DQS3	0.63	0.57
MemData32:39, DM4	DQS4	0.68	0.54
MemData40:47, DM5	DQS5	0.67	0.52
MemData48:55, DM6	DQS6	0.62	0.61
MemData56:63, DM7	DQS7	0.65	0.55
ECC0:7, DM8	DQS8	0.63	0.61

DDR SDRAM Read Operation

The Read of the incoming Data from the SDRAM is done on the rising and falling edges of the differential DQS signal. The Data must be centered to these edges for correct operation.

The PPC440SPe can delay with very fine granularity the DQS through the programming of the MCIF0_RODC[RQFD] register field.

DDR SDRAM MemClkOut0 and Read Clock Delay

In order to accommodate timing variations introduced by the system designs using this chip, the three-stage data path shown below is used to eliminate metastability and allow data sampling to be adjusted for minimum latency. The data are stored in the 8 Flip Flops of the Stage 1, such that it can be transferred later within a 8X period.

Figure 9. DDR SDRAM Read Data Path

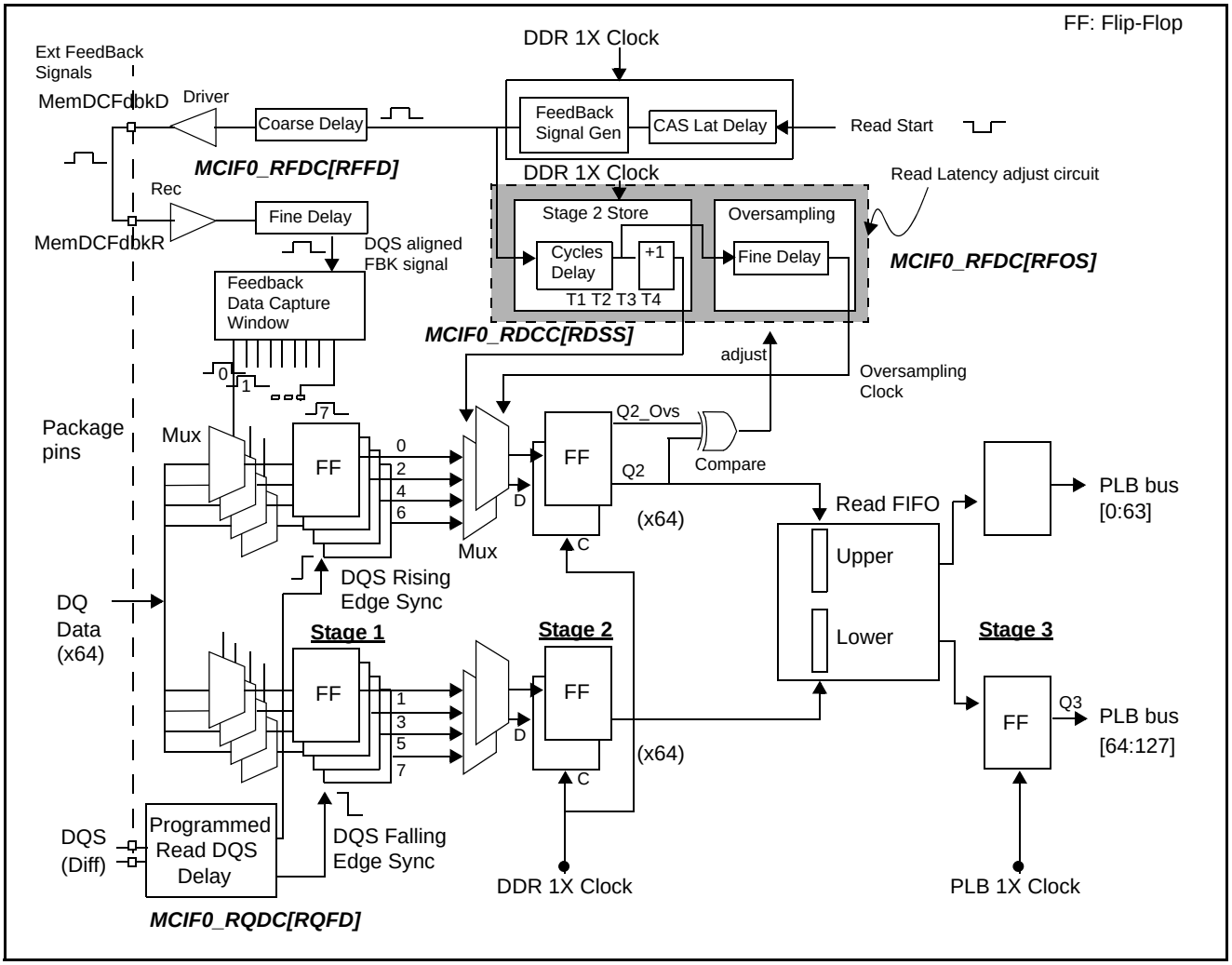


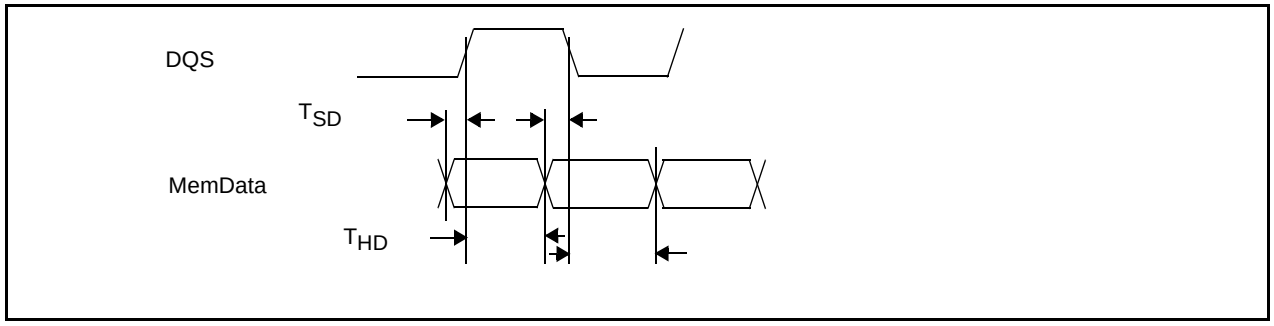
Table 20. DDR SDRAM I/O Read Timing—T_{SD} and T_{HD}

Notes:
1. T_{SD} and T_{HD} are measured under worst case conditions.
2. Clock speed for the values in the table is 333.33 MHz.
3. The time values in the table include 1/4 of a cycle at 166 MHz (3 ns x 0.25 = 0.75 ns).
4. To obtain adjusted T_{SD} and T_{HD} values for lower clock frequencies, subtract 0.75 ns from the values in the table and add 1/4 of the cycle time for the lower clock frequency (e.g., T_{SD} - 0.75 + 0.25T_{CYC}).

Signal Names	Reference Signal	Read Data vs DQS Set up T_{SD} (ns)	Read Data vs DQS Hold T_{HD} (ns)
MemData00:07	DQS0	0.00	1.00
MemData08:15	DQS1	0.00	1.00
MemData16:23	DQS2	0.00	1.00
MemData24:31	DQS3	0.00	1.00
MemData32:39	DQS4	0.00	1.00
MemData40:47	DQS5	0.00	1.00
MemData48:55	DQS6	0.00	1.00
MemData56:63	DQS7	0.00	1.00
ECC0:7	DQS8	0.00	1.00

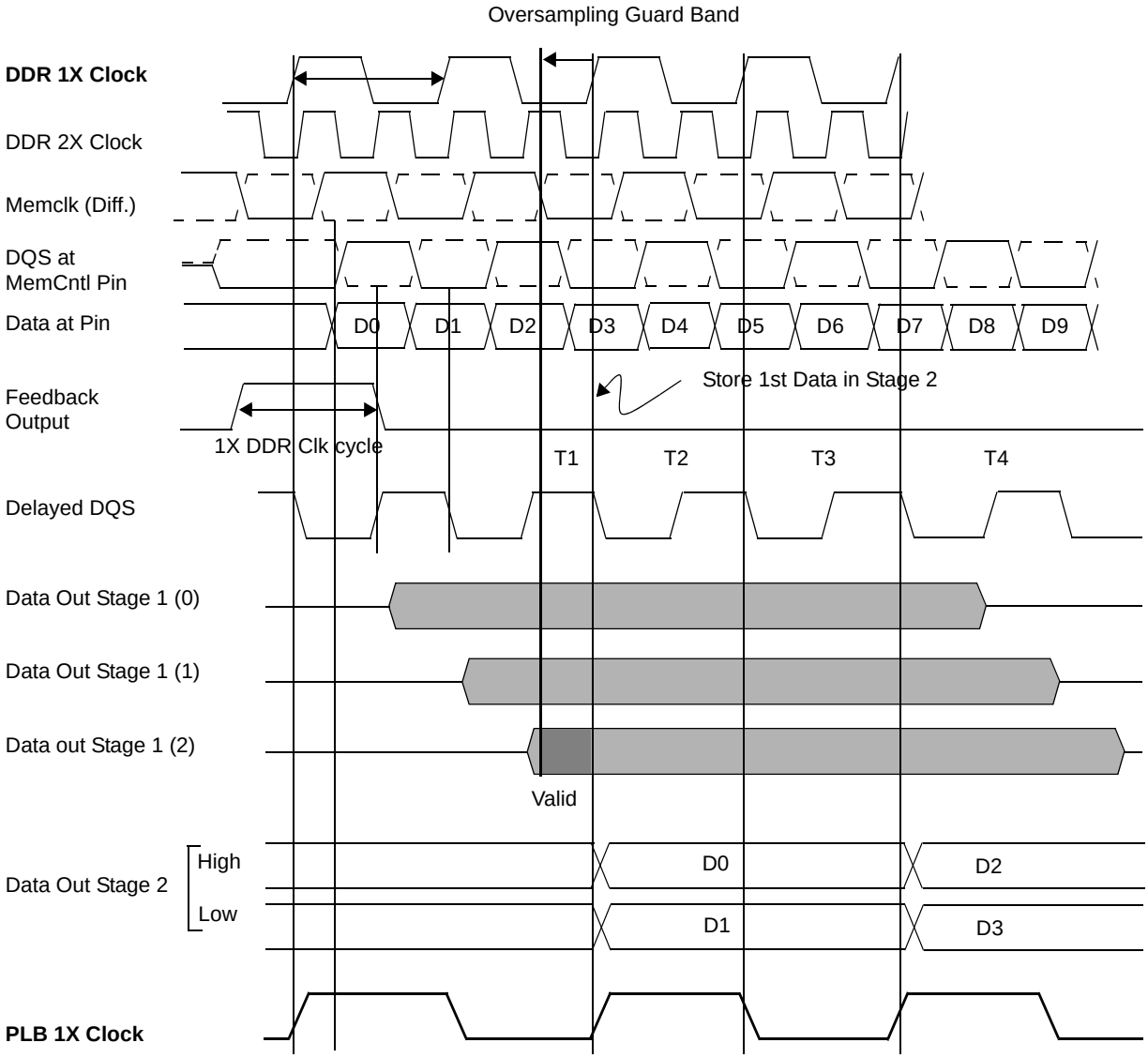
In the following examples, the data strobes (DQS) and the data are shown to be coincident. There is actually a slight skew as specified by the SDRAM specifications, and there can be additional skew due to loading and signal routing. It is recommended that the signal length for all of the eight DQS signals be matched.

Figure 10. DDR SDRAM Memory Data and DQS



The following example shows the timing relationship between SDRAM DDR Data at the input pin and the store of the Data in stage 1.

Figure 11. DDR SDRAM Read Cycle Timing—Example



Initialization

The PPC440SPe provides the option for setting initial parameters based on default values or by reading them from a serial “bootstrap” ROM attached to the IIC0 bus. These options are defined by strapping on three external pins (see “Strapping” below).

Strapping

While the SysReset input pin is low (system reset), the state of certain I/O pins is read to enable certain default initial conditions prior to PPC440SPe start-up. The actual capture instant is the nearest SysClk edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. They are used for strap functions only during reset. Following reset they are used for normal functions.

The following table lists the strapping pins along with their functions and strapping options:

Table 21. Strapping Pin Assignments

Function	Option	Pin Strapping		
		Bit 0 **H13** (UART0_DCD)	**Bit 1** **C12** (UART0_DSR)	**Bit2** **B08** (UART0_CTS)
Serial Bootstrap ROM is disabled (Bit 0 off). Refer to the IIC Bootstrap Controller chapter in the *PPC440SPe Embedded Processor User’s Manual* for details.	Boot from EBC	0	0	
	Boot from PCI	0	1	
Serial Bootstrap ROM is enabled (Bit 0 on). The options being selected are the IIC0 slave address that responds with strapping data and reading *128 bits* from the Bootstrap ROM.	0x54	1	0	0
	0x50	1	1	0
Serial Bootstrap ROM is enabled (Bit 0 on). The options being selected are the IIC0 slave address that responds with strapping data and reading *256 bits* from the Bootstrap ROM.	0x54	1	0	1
	0x50	1	1	1

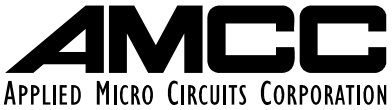
Serial Bootstrap ROM

During reset, if the serial device is enabled, initial conditions can be read from a ROM connected to the IIC0 port. In this case, at the de-assertion of SysReset, the PPC440SPe sequentially reads up to 32 bytes from the ROM device on the IIC0 port and sets the SDR0_SDSTP0 - SDR0_SDSTP7 registers accordingly.

The initialization settings and their default values are covered in detail in the *PPC440SPe Embedded Processor User’s Manual*.

Document Revision History

Revision	Date	Description
1.23	Sept 21, 2006	Updated Recommended DC Operating Conditions table.
1.22	Sept 12, 2006	Updated Processor Clock values in Clocking Specifications table.
1.21	June 27, 2006	Updated Recommended DC Op Conditions and Signal Functional Description tables for PCI-X DDR mode 2.
1.20	June 14, 2006	Updated signal lists. Corrected reference to PCIX0Cap in Signal Functional Description table. Added reference to Note 6 for UART0_CTS register in Signal Functional Description table.
1.19	May 23, 2006	Fixed doc issue for PEROE signal in Signal Functional Description table. Fixed doc issue for UARTSerClk signal throughout document. Fixed doc issue for PSRO1 signal in Signal Functional Description table. Updated Clocking Specifications table and Serial Bootstrap ROM paragraph.
1.18	May 1, 2006	Updated ordering and PVR information, and core package graphic in Figure 3. Added RAID acceleration section to Features, Description, and functional details sections.
1.17	April 6, 2006	Additional update to ordering and PVR information. GJG
1.16	March 8, 2006	Updated ordering and PVR information, part number list, and package diagram. GJG
1.15	March 7, 2006	Removed DMA statement from Serial Port feature statement. Removed reference to notes from PERBLAST entry in signal functional description table. GJG
1.14	March 6, 2006	Updated description of On-Chip SRAM/L2 Cache in Introduction. GJG
1.13	January 9, 2006	Updated Signal Function Description table per JB, updated mailing address and copyright date in disclaimer. GJG
1.12	November 15, 2005	Clarified information about DDR SDRAM I/O specifications. GJG
1.11	October 26, 2005	Corrected upper limit of allowable case temperature, documented reserved signal pins, added bookmarks for signal lists. GJG
1.10	October 17, 2005	Restored multiplexed signal information to the “Signals Listed Alphabetically” table. Applied corrections to the table from GB. GJG
1.09	July 12, 2005	Updated leakage current info, case temp range, DDR SDRAM Signal Termination graphic. GJG
1.08	May 23, 2005	Update Write timing diagrams. GJG
1.07	May 20, 2005	Updated system memory address map. Corrected functional block diagram. GJG
1.06	Mar 10, 2005	Removed text for unsupported COLA component. GJG
1.05	Feb 15, 2005	Removed references to unsupported COLA serial interface. Reformatted LOF, LOT to comply with AMCC style. GJG
1.04	Dec 21, 2004	Update max case temp in Recommended DC Op Conditions table to match Ordering and PVR Information table. GJG
1.03	Dec 20, 2004	Update Ordering and PVR info, PCI Express features info, DDR SDRAM read data path and read cycle timing example, memory map. GJG
1.02	Sept 21, 2004	PCI-Express Rx Tx pin assignment changes. GJG
1.01	Sept 13, 2004	Converted to AMCC format, corrected tables, graphics as needed. GJG
0.5	Sept 10, 2004	Renamed 440SPe, added Mux table, VDDA 2.5V (IN PROGRESS)
0.4	Aug 02, 2004	Miscellaneous technical additions, PN and corrections from Support.
0.3	July 18, 2004	Correct TOC, LOF, LOT, broken cross-references.
0.2	June 25, 2004	Add alphabetic list, update Sys Mem address map.
0.1	June 18, 2004	Create initial data sheet.



Applied Micro Circuits Corporation

215 Moffett Park Dr., Sunnyvale, CA 94089

Phone: (858) 450-9333 — (800) 755-2622 — Fax: (858) 450-9885

http://www.amcc.com