Winbond

# PROGRAMMABLE MANCHESTER CODE ENCODER/DECODER

## GENERAL DESCRIPTION

The WE9215 Series is a Manchester code Encoder/Decoder chip for remote control. Each chip contains the transmitter and receiver circuit. Therefore it can operate in transmit mode or receive mode depending on the Tx/$\overline{Rx}$ pin. In the transmit (encoder) mode it will generate 1 of 32768 codes depending on the A1-A15 inputs. In the receive (decoder) mode the circuit will receive the serial data in Manchester code format and make a comparison to the local data word A1-A15.

The circuit contains an on chip inexpensive RC oscillator circuit. The chip operating voltage is recommended at the 3.0V-5.0V. If the $V_{DD}$ supply voltage is great than 5.5V then the limiting resistor and Zener diode are needed.
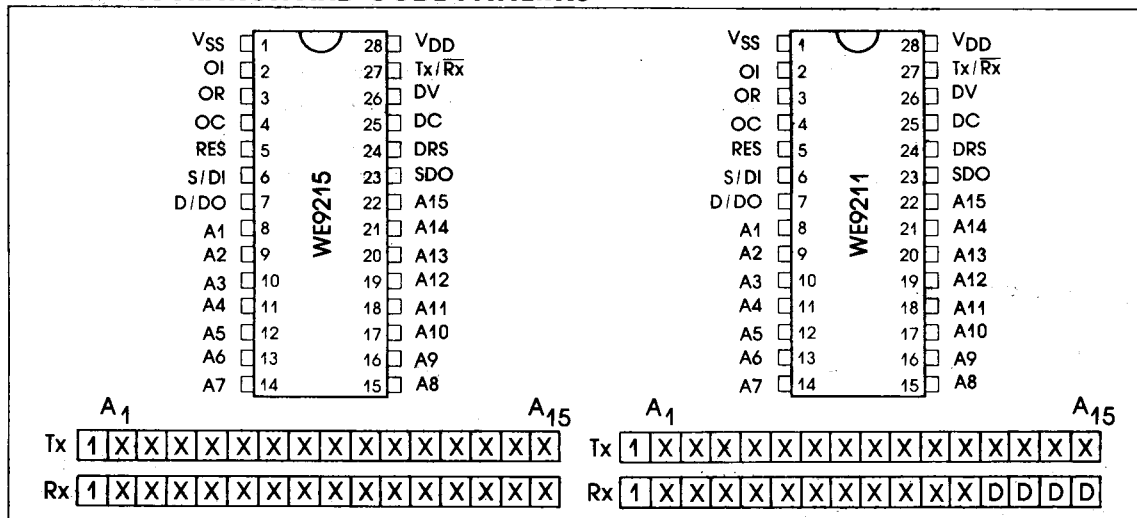
## FEATURES

- Operating voltage range 3.0V-5.0V. Low stand-by current.
- On chip oscillator using inexpensive RC components.
- Manchester code encoder/decoder on one chip.
- Automatic preamble generation.
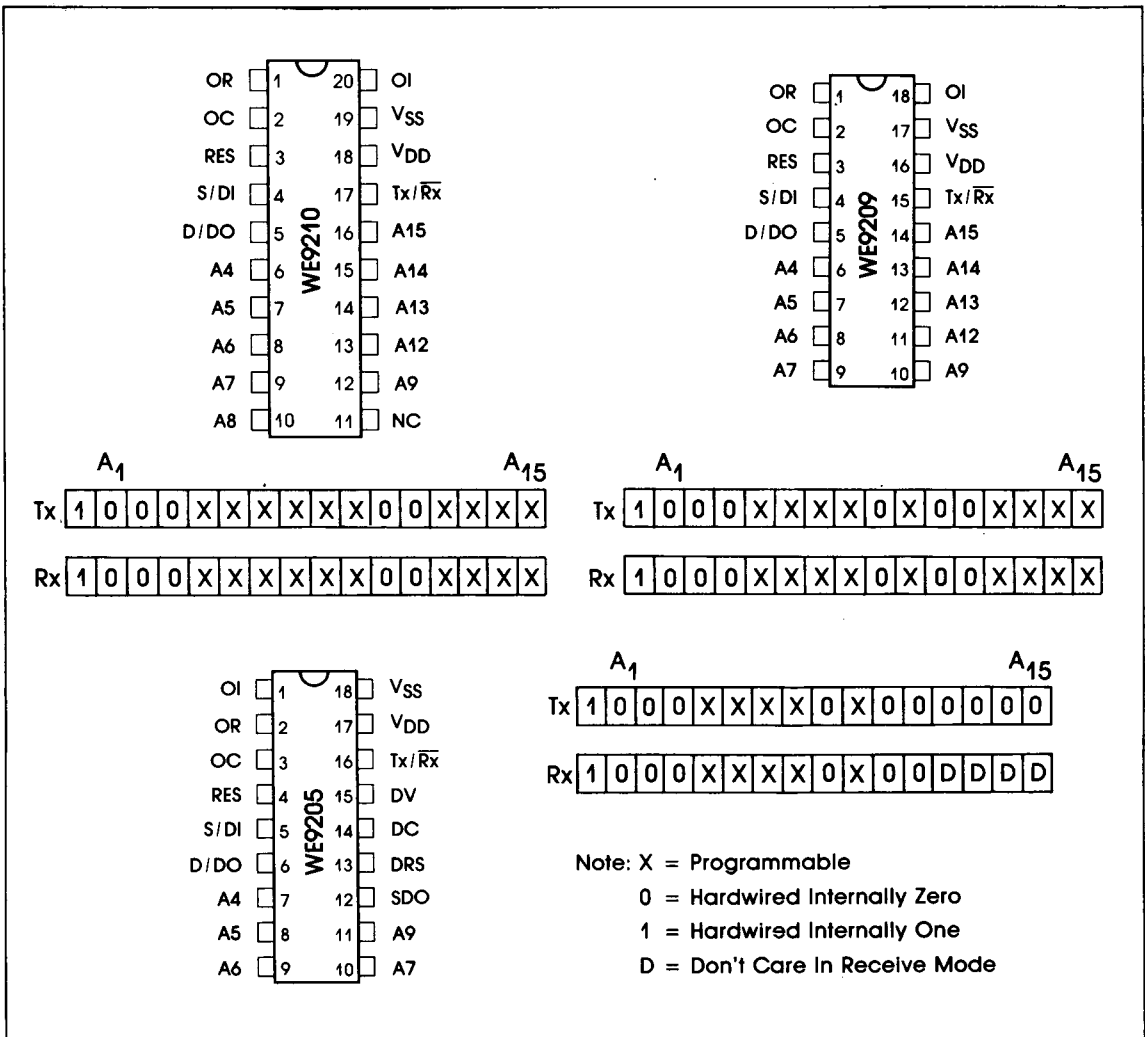- Schmitt trigger for data input.

## APPLICATIONS

- Alarm control system.
- Security system.
- Cordless telephone.
- Digital locks.
- Remote control.
- Paging system.

## PIN CONFIGURATION AND CODE PATTERNS



SO 28pin is available for WE9215S

417

**WE9210**

| | | | |
|---|---|---|---|
| OR | 1 | 20 | OI |
| OC | 2 | 19 | $V_{SS}$ |
| RES | 3 | 18 | $V_{DD}$ |
| S/DI | 4 | 17 | $Tx/\overline{Rx}$ |
| D/DO | 5 | 16 | A15 |
| A4 | 6 | 15 | A14 |
| A5 | 7 | 14 | A13 |
| A6 | 8 | 13 | A12 |
| A7 | 9 | 12 | A9 |
| A8 | 10 | 11 | NC |

$A_1$ ............ $A_{15}$

| Tx | 1 | 0 | 0 | 0 | X | X | X | X | X | X | X | 0 | 0 | X | X | X |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

| Rx | 1 | 0 | 0 | 0 | X | X | X | X | X | X | X | 0 | 0 | X | X | X |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**WE9209**

| | | | |
|---|---|---|---|
| OR | 1 | 18 | OI |
| OC | 2 | 17 | $V_{SS}$ |
| RES | 3 | 16 | $V_{DD}$ |
| S/DI | 4 | 15 | $Tx/\overline{Rx}$ |
| D/DO | 5 | 14 | A15 |
| A4 | 6 | 13 | A14 |
| A5 | 7 | 12 | A13 |
| A6 | 8 | 11 | A12 |
| A7 | 9 | 10 | A9 |

$A_1$ ............ $A_{15}$

| Tx | 1 | 0 | 0 | 0 | X | X | X | X | 0 | X | 0 | 0 | X | X | X | X |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

| Rx | 1 | 0 | 0 | 0 | X | X | X | X | 0 | X | 0 | 0 | X | X | X | X |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**WE9205**

| | | | |
|---|---|---|---|
| OI | 1 | 18 | $V_{SS}$ |
| OR | 2 | 17 | $V_{DD}$ |
| OC | 3 | 16 | $Tx/\overline{Rx}$ |
| RES | 4 | 15 | DV |
| S/DI | 5 | 14 | DC |
| D/DO | 6 | 13 | DRS |
| A4 | 7 | 12 | SDO |
| A5 | 8 | 11 | A9 |
| A6 | 9 | 10 | A7 |

$A_1$ ............ $A_{15}$

| Tx | 1 | 0 | 0 | 0 | X | X | X | X | 0 | X | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

| Rx | 1 | 0 | 0 | 0 | X | X | X | X | 0 | X | 0 | 0 | D | D | D | D |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Note: X = Programmable
0 = Hardwired Internally Zero
1 = Hardwired Internally One
D = Don't Care In Receive Mode

## PIN DESCRIPTION

**A. $V_{SS}$ $V_{DD}$**

Negative and Positive Power Supply

**B. OI (Oscillator Input)**

This input is to drive the oscillator and is the tie point of the timing resistor (R) and the timing capacitor (C).

**C. OR (Oscillator Resistor)**

Provides phase feedback to the RC timing circuit through the connected timing resistor.

**D. OC** (Oscillator Capacitor)

Capacitor connection of RC timing circuit Provides phased feedback from the oscillator.

**E. R E S** (Reset)

This pin be used to override the data transmission cycle or inhibiting a S/DI input. It clears the D/DO to a low state and reset the internal oscillator and data comparison circuits.

**F. S/DI** (Start/Date)

S/DI input is a dual function Pin. In the transmit Input mode, it is used to start the oscillator which enables the transmission of the encoded word and in the receive mode this input receives the serial coded information for processing and comparison.

**G. D/DO** (Date/Decode)

In transmit mode, this Pin is the encoded sequence data output Pin. In receive mode, It indicates the result of the comparison.

**H. A1-A15** (Data bit Inputs)

In transmit mode, these inputs provide parallel input data to be sequentially transmitted. In the receive mode these inputs become the parallel local data code for comparison with the incoming data.

**I. SDO** (Serial Data Output)

This output signal is buffered S/DI signal and is the same polarity as the S/DI. Can be us-

ed to chain a number of receivers together. This output can be connected to the input of a 16bit shift register (clocked by the DC Pin) in a receiver system where data is to be recovered regardless of its comparison to a pre-set address word.

**J. DRS** (Data Reset Output)

Be used in the receive mode to reset an external data shift register since this signal pulse indicated that a new word has just begun processing.

**K. DC** (Data Clock Output)

The data clock output may be used in a receive system since it is the recovered data sync pulses. Also this output can be used to clock an external shift register where data is to be recovered.

**L. DV** (Data Valid Output)

This output is triggered low at the start of any input and will remain low until a complete word has been processed. Note that this output simply signals that a valid word has been received and not that the code received has matched the local address code.
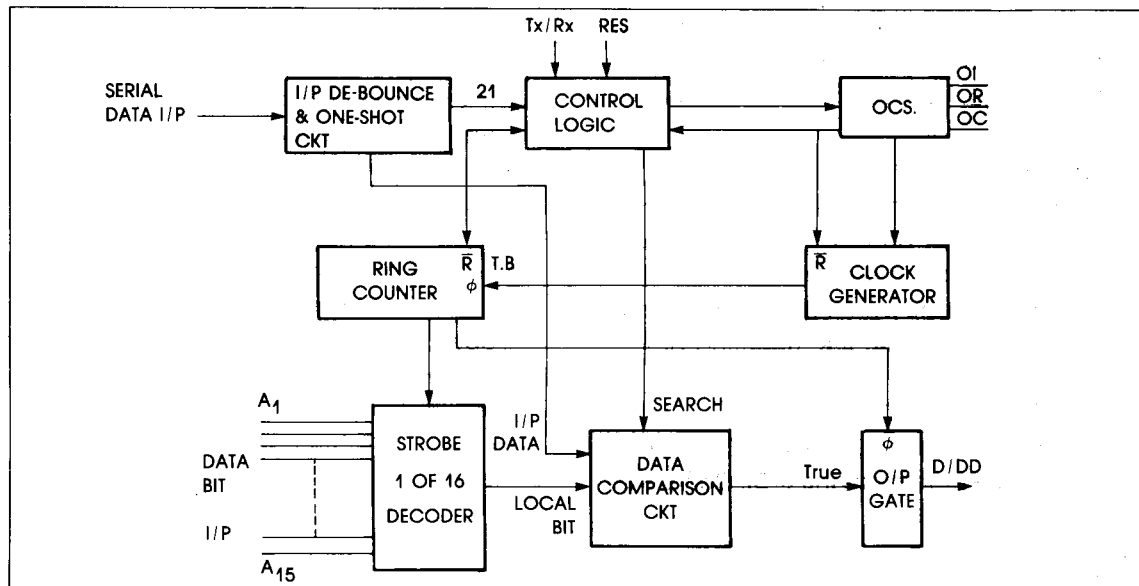
**M. Tx/$\overline{\text{Rx}}$** (Transmit/Receive)

This is a control input to determine the operating mode. The Hi puts it in the transmit mode. The Low puts it in the receive mode.

*ENCODER/*
*DECODER*

## BLOCK DIAGRAM
### A. Transmit (Encoder) Mode
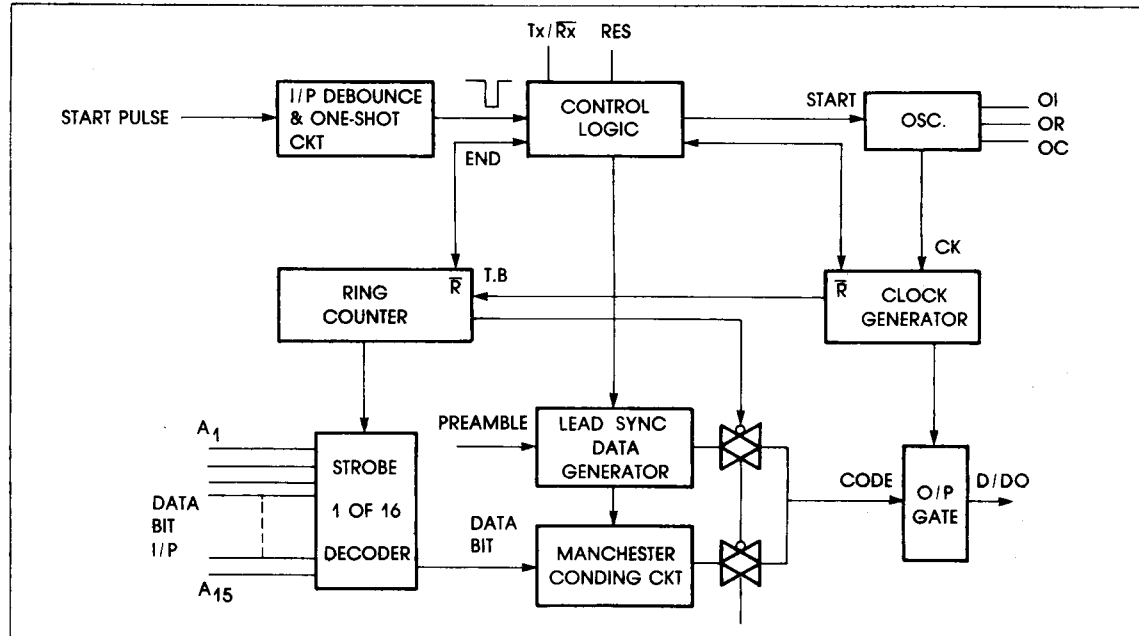


### B. Receive (decoder) Mode:

## OPERATION DESCRIPTION

### A. GENERAL

The WE9215 series mode of operation is controlled by the transmit/Receive control input(Tx/$\overline{Rx}$) when switch the Tx/$\overline{Rx}$ pin from $V_{SS}$ to $V_{DD}$, the circuit will automatically change the oscillator, start/Data Input, and Data/Decode Output from receive mode to transmit mode.

The WE9215 output drivers are capable of sinking or sourcing 0.7mA minimum at 1.0 volts $V_{DS}$. All inputs are gate-protected to both power supplies by internal diodes. The data inputs each have pull down resistors to ground so that only a "1" will have to be programmed. This allows the inputs to be programmed by using "SPST" switches or jumpers to $V_{DD}$ only. The Tx/Rx input does not have a pull up or pull down resistor, but is applied to a Schmitt trigge input circuit to improve noise rejection.

### B. ENCODER FUNCTION

Encoder function is selected by connecting the Tx/$\overline{Rx}$ control input to $V_{DD}$. This enables the transmit mode and the circuit will function as an encoder-sampling the 15 data inputs and encoding this parallel data in "NRZ" format, combining it with the clock in Manchester code and presented to the D/DO pin for transmission. The encoder will transmit the serial data each time the S/DI is activated. This encoded data word is transmitted in 2 Parts. The first part is the preamble information which is a series of 12 "1"s then a space indicating that the encoded data is to follow. This preamble information is intended to be used to synchronize a phase locked loop at the receiver or used as a settling time for receivers that have automatic gain control. The second part contains the 15 bits of addresses and/or controls.

### C. DECODER FUNCTION

The receive mode is selected by connecting the Transmit/Receive control input to ground. In this mode the circuit will works as a decoder, receiving the serial data in Manchester coded format and recover the clock. The incoming data is converted to a 15-bit serial word. Compare it with the local data word by sampling the address inputs (15-bits). These bits are usually programmed to expected data that will be decoded. If the two data words match, the decoded output will become logic "1" state, but if the two words do not match the decoded output will stay low. Also if the words do not match but the bit stream was valid (i.e. 15-bits of proper timing) then only the output valid signal will go high. If at any time the bit sequence has the wrong timing, the local oscillator and internal comparison circuits will be reset and any new input pulses will be recognized as a new bit stream. Therefore, as with the receiver processing of the preamble information the 12 bits will be recognized but during the 13th interval where no bit transition occurs, the circuit times-out and awaits the start bit of the data sequence.

*ENCODER/*
*DECODER*

## D. WE9211 OPTION

The WE9211 differs from the WE9215 in that in the receive mode the WE9211 will only compare the 11 bits and ignore the state of the last 4 bits–that is 2048 distinct address codes with 4 bits of that may be used for control data transmission.

## E. WE9210/WE9209 OPTION

The WE9210/WE9209 is essentially an 20 Pin/18 Pin packaging of the WE9215 die. The operation and function of this circuit is the same as the WE9215 the only difference being in the available pins. In the transmit mode the circuit is only capable of encoding 10 bits/9 bits of data, the other 5 bits/6 bits are not programmable and remain zero's. The Pin configuration also drops DV, DC, DRS, and SDO such that the circuit can now only respond to a data match condition on the only output D/DO. In the rceive mode the circuit can decode the same 10 bits/9 bits of data, enabling up to 1024/512 possible addresses.

## F. WE9205 OPTION

The 18 Pin packaging option of the WE9211 die is called the WE9205. In the transmit mode it is only capable of 5 bits of programmable code. All the other bits are held at zero. But in the receive mode, the circuit has five (32) unlock code bits plus the last four transparent bits of the WE9211. The WE9205 also supplies the necessary output signals to process the 4 bits of control data.

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
|---|---|---|
| DC Supply Voltage | 5.5 | V |
| Input Voltage Range | $V_{SS}-0.3 \sim V_{DD}+0.3$ | V |
| Power Dissipation (WE9210, 9209, 9205) | 500 | mS |
| Power Dissipation (WE9215, 9211) | 1.0 | mW |
| Operating Temperature | $0 \sim +70$ | °C |
| Storage Temperature | $-25 \sim +125$ | °C |

## D.C. CHARACTERISTICS

($V_{DD}=5.0V$, $V_{SS}=0.0V$, $T_A=25°C$)

| PARAMETER | SYM. | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | "1" Input | $0.7V_{DD}$ | $V_{DD}$ | $V_{DD}+0.3$ | V |
| Input Low Voltage | $V_{IL}$ | "0" Output | $V_{SS}-0.3$ | $V_{SS}$ | $0.3V_{SS}$ | V |

| PARAMETER | SYM. | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{LKG}$ | $V_{IN}=5.0V$ for Pin Tx/$\overline{Rx}$, S/DI | — | 0 | ±5 | $\mu A$ |
| Input Load Current | $I_{LD}$ | $V_{IN}=5.0V$ for Pin RES, A1-A15 | 2.0 | 10.0 | 25.0 | $\mu A$ |
| Output High | $V_{OH}$ | $I_{Load}=-100\mu A$ | $V_{DD}-0.3$ | $V_{DD}$ | $V_{DD}$ | V |
| Output Low | $V_{DL}$ | $I_{Load}=-100\mu A$ | — | $V_{SS}$ | $V_{SS}+0.3$ | V |
| Input Capacitance | $C_{IN}$ | | — | — | $-10.0$ | pF |
| Output Capacitance | $C_{OUT}$ | | — | — | 10.0 | pF |
| Output High Current | $I_{OH}$ | $V_{OH}=V_{DD}-1.0V$ | $-0.7$ | $-0.8$ | — | mA |
| Output Low Current | $I_{OL}$ | $V_{OL}=V_{SS}+1.0V$ | 1.5 | 2.0 | — | mA |
| Stand-by Current | $I_{STB}$ | $V_{DD}=5.0V$, input=GND Oscillator is halt | — | 2.0 | 10.0 | $\mu A$ |
| Operating Current | $I_{OPR}$ | $V_{DD}=5.0V$, Input=GND output=OPEN | — | 20.0 | 100.0 | $\mu A$ |

## A.C. CHARACTERISTICS

| PARAMETER | SYM. | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Operating Clock frequency | $F_C$ | $F_C=\dfrac{1}{2.5RC}$ | 0.1 | — | 5.0 | KHz |
| Start Pulse Width | $I_{SDI}$ | | 500 | — | — | nS |
| D/DD Delay from S/DI | $T_{DDO}$ | | — | 5 | — | $\mu S$ |
| Data Clock Pulse Width | $T_{DC}$ | $T_C=\dfrac{1}{F_C}$ | — | $0.5T_C$ | — | Sec. |
| Full Cycle Word Length | $T_{WORD}$ | | — | $103T_C$ | — | Sec. |
| Receiver Oscillator Resistor Tolerance from Transmitter Oscillator Resistor | $R_R$ | | — | — | ±5 | % |
| Receiver Oscillator Capacitor Tolerance from Transmitter Oscillator Capacitor | $C_R$ | | — | — | ±10 | % |
| Operating Clock Frequency Deviation Rate | $F_R$ | $F_R=\dfrac{\triangle F/Fc}{\triangle V}$ $3.0V\le V_{DD}\le5.0V$ | — | — | 5 | %/V |

*ENCODER/ DECODER*
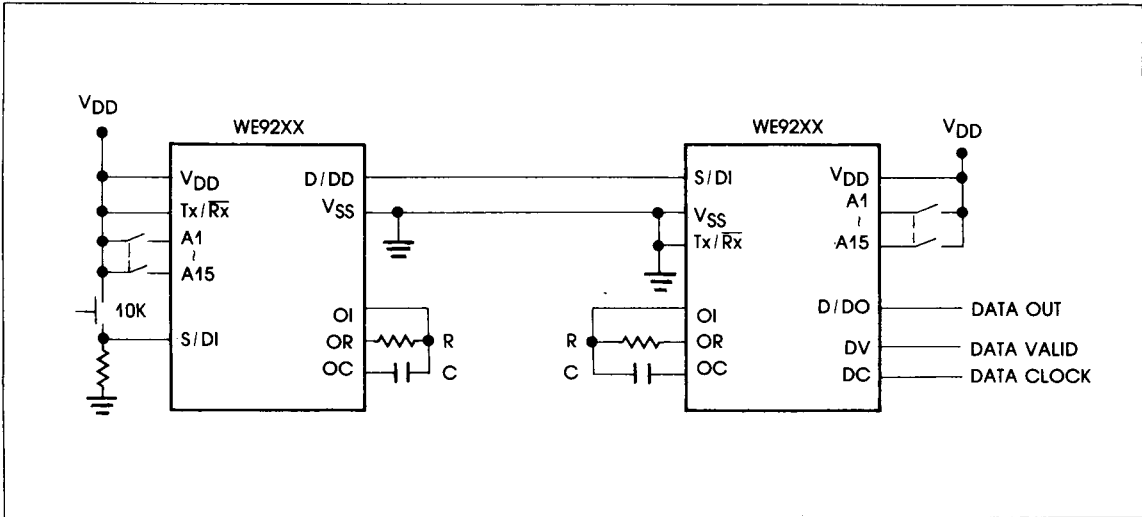
## TIMING WAVEFORM

### A. TRANSMIT MODE
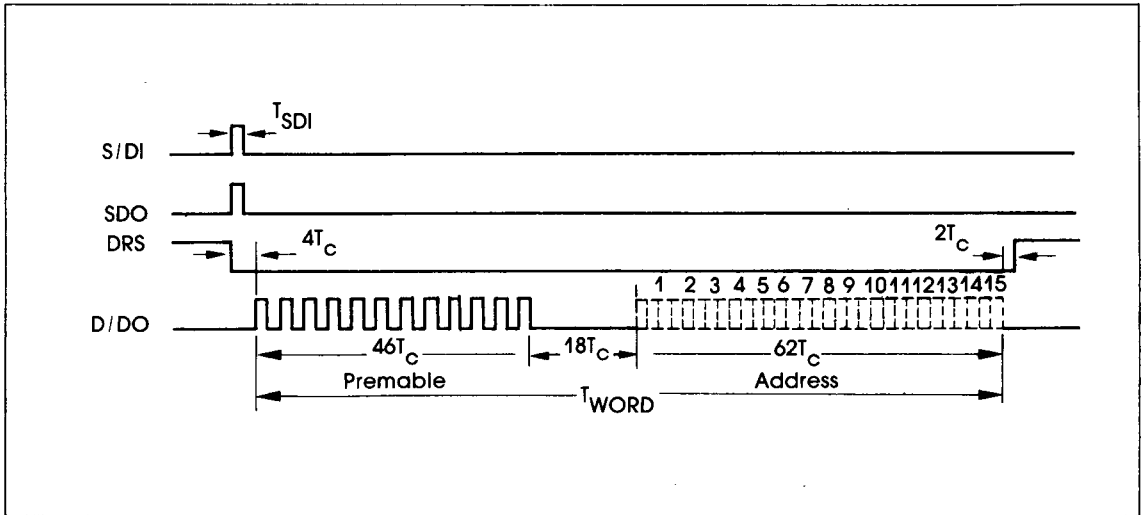


### B. RECEIVE MODE
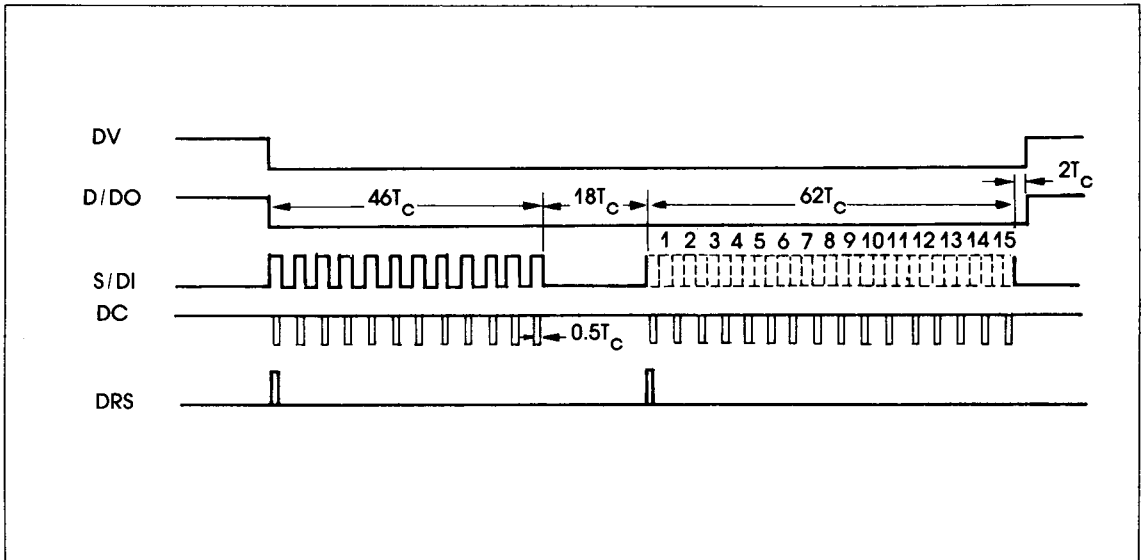
## APPLICATION AND TEST CIRCUIT

### A. BASIC TWO-WIRE SYSTEM AND TEST CIRCUIT



### B. WITH CONTROL DATA OUTPUT
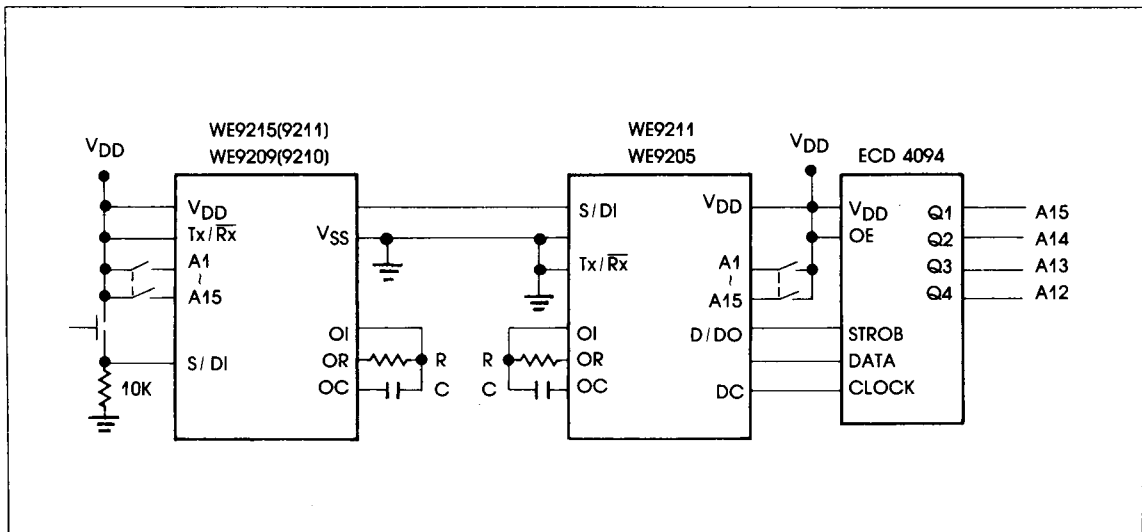


| COMPONENT | VALUE |
|-----------|-------|
| R | 4.7K ~ 1.0M |
| C | 30pF ~ 0.2$\mu$F |

ENCODER/
DECODER