MX23C1010

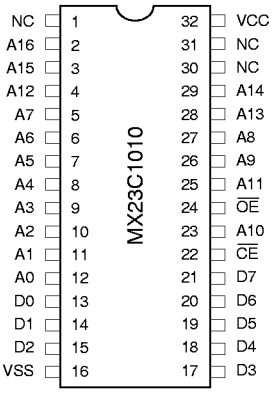
1M-BIT MASK ROM (8 BIT OUTPUT)

FEATURES

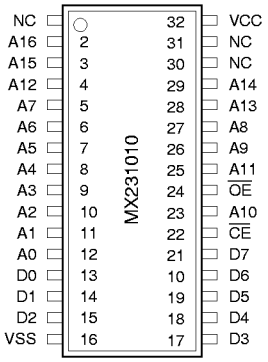
- Bit organization
  - 128K x 8 (byte mode)
- Fast access time
  - Random access: 45ns (max.)
- Current
  - Operating: 40mA
  - Standby: 100uA
- Supply voltage
  - 5V±10% for 70ns(max.)
  - 5V±5% for 45ns(max.)
- Package
  - 32 pin PDIP/SOP/PLCC/TSOP

PIN CONFIGURATION

32 PDIP



32 SOP



ORDER INFORMATION

Part No.	Access Time	Package
MX23C1010PC-45	45ns	32 pin PDIP
MX23C1010PC-70	70ns	32 pin PDIP
MX23C1010PC-90	90ns	32 pin PDIP
MX23C1010PC-10	100ns	32 pin PDIP
MX23C1010PC-12	120ns	32 pin PDIP
MX23C1010PC-15	150ns	32 pin PDIP
MX23C1010MC-45	45ns	32 pin SOP
MX23C1010MC-70	70ns	32 pin SOP
MX23C1010MC-90	90ns	32 pin SOP
MX23C1010MC-10	100ns	32 pin SOP
MX23C1010MC-12	120ns	32 pin SOP
MX23C1010MC-15	150ns	32 pin SOP
MX23C1010QC-45	45ns	32 pin PLCC
MX23C1010QC-70	70ns	32 pin PLCC
MX23C1010QC-90	90ns	32 pin PLCC
MX23C1010QC-10	100ns	32 pin PLCC
MX23C1010QC-12	120ns	32 pin PLCC
MX23C1010QC-15	150ns	32 pin PLCC
MX23C1010TC-45	45ns	32 pin TSOP
MX23C1010TC-70	70ns	32 pin TSOP
MX23C1010TC-90	90ns	32 pin TSOP
MX23C1010TC-10	100ns	32 pin TSOP
MX23C1010TC-12	120ns	32 pin TSOP
MX23C1010TC-15	150ns	32 pin TSOP
MX23C1010QI-12(*)	120ns	32 pin PLCC
MX23C1010QI-15(*)	150ns	32 pin PLCC
MX23C1010TI-90(*)	90ns	32 pin TSOP

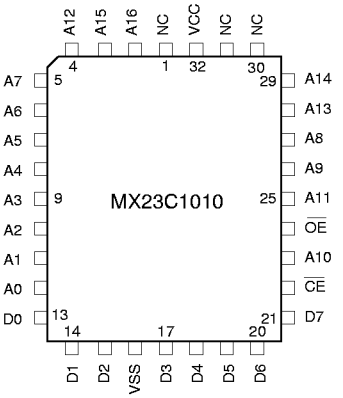
(*): industrial grade, TA= -40°C ~ 85°C

PIN DESCRIPTION

Symbol	Pin Function
A0~A16	Address Inputs
D0~D7	Data Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

32 TSOP(I)

32 PLCC



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATINGS
Voltage on any Pin Relative to VSS	VIN	-0.5V to 7.0V
Ambient Operating Temperature	Topr	-40℃ to 85℃
Storage Temperature	Tstg	-65℃ to 125℃

DC CHARACTERISTICS (Ta = -40℃ ~ 85℃, VCC = 5V±10% for 70ns max., 5V±5% for 45ns max.)

ITEM	SYMBOL	MIN.	MAX.	CONDITIONS
Output High Voltage	VOH	2.4V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 2.1mA
Input High Voltage	VIH	2.0V	VCC+0.5V	
Input Low Voltage	VIL	-0.3V(Note)	0.8V	
Input Leakage Current	ILI	-10	10uA	VIN=0 to 5.5V
Output Leakage Current	ILO	-10	10uA	VOUT=0 to 5.5V
Operating Current	ICC1	-	40mA	CE = VIL, f = 5MHz, Iout = 0mA
Standby Current (TTL)	ISTB1	-	1.5mA	CE = VIH
Standby Current (CMOS)	ISTB2	-	100uA	CE = VCC +/- 0.3V
Input Capacitance	CIN	-	12pF	VIN=0V
Output Capacitance	COUT	-	12pF	VOUT=OV

Note:
VIL min.=-1.0V for pulse width ≤ 50ns
VIL min.=-2.0V for pulse width ≤ 20ns

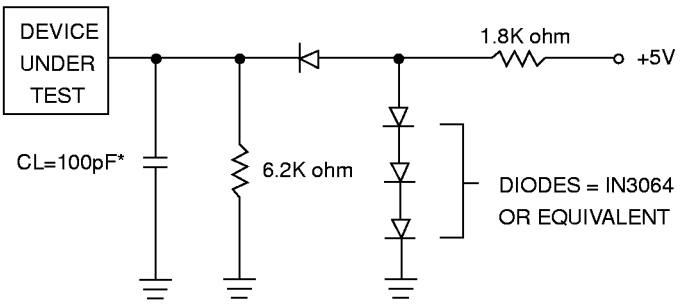
AC CHARACTERISTICS (Ta = -40℃ ~ 85℃, VCC = 5V±10% for 70ns max., 5V±5% for 45ns max.)

ITEM	SYMBOL	23C1010-45*		23C1010-70*		23C1010-90		23C1010-10		23C1010-12		23C1010-15	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN	MAX	MIN	MAX
Read Cycle Time	tRC	45ns	-	70ns	-	90ns	-	100ns	-	120ns	-	150ns	-
Address Access Time	tAA	-	45ns	-	70ns	-	90ns	-	100ns	-	120ns	-	150ns
Chip Enable Access Time	tACE	-	45ns	-	70ns	-	90ns	-	100ns	-	120ns	-	150ns
Output Enable Time	tOE	-	25ns	-	35ns	-	40ns	-	45ns	-	50ns	-	60ns
Output Hold After Address	tOH	0ns	-	0ns	-	0ns	-	0ns	-	0ns	-	0ns	-
Output High Z Delay	tHZ	-	17ns	-	20ns	-	25ns	-	30ns	-	35ns	-	50ns

Note :Output high-impedance delay (tHZ) is measured from $\overline{OE}$ or $\overline{CE}$ going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.
*45ns&70ns speed grades are under development.

AC Test Conditions

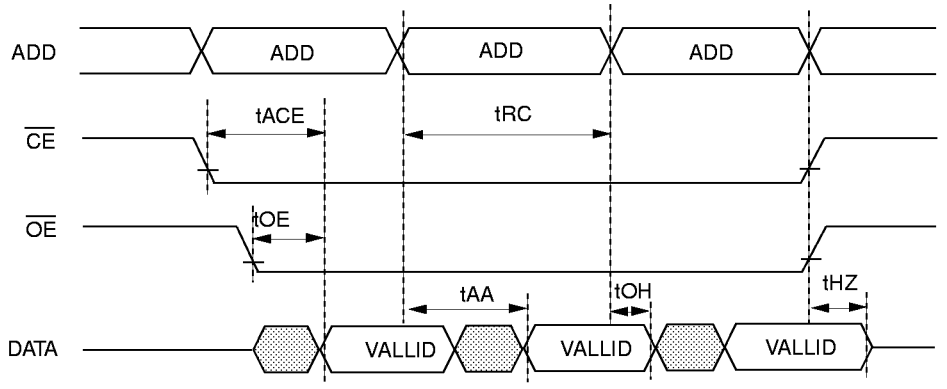
Input Pulse Levels	0.4V~2.4V 0V~3v (for 45ns&70ns)
Input Rise and Fall Times	10ns
Input Timing Level	0.8V~2.0V 1.5V (for 45ns&70ns)
Output Timing Level	0.8V and 2.0V 1.5V (for 45ns&70ns)
Output Load	See Figure



*CL=30pF for 45ns&70ns

TIMING DIAGRAM

RANDOM READ



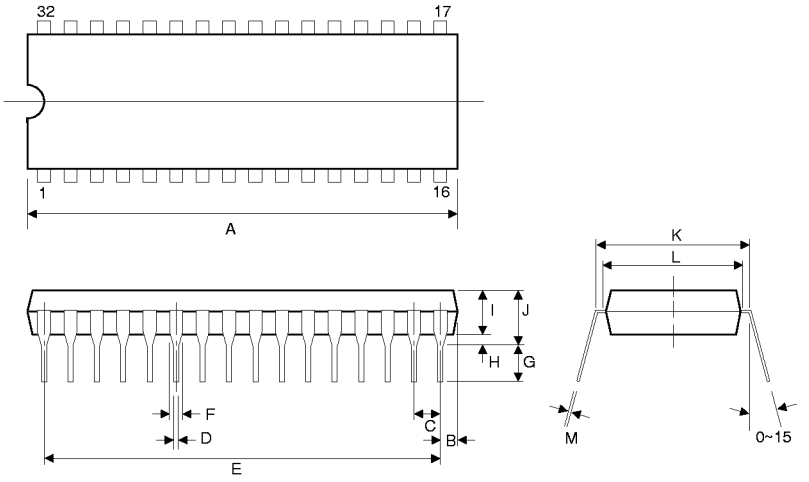
Note : $\overline{CE}$, $\overline{OE}$ are enable.

PACKAGE INFORMATION

32-PIN PLASTIC DIP (600 mil)

ITEM	MILLIMETERS	INCHES
A	42.13 max.	1.660 max.
B	1.90 [REF]	.075 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	38.07	1.500
F	1.27 [Typ.]	.050 [Typ.]
G	3.30±.25	.130±.010
H	.51 [REF]	.020 [REF]
I	3.94±.25	.155±.010
J	5.33 max.	.210 max.
K	15.22±.25	.600±.010
L	13.97±.25	.550±.010
M	.25 [Typ.]	.010 [Typ.]

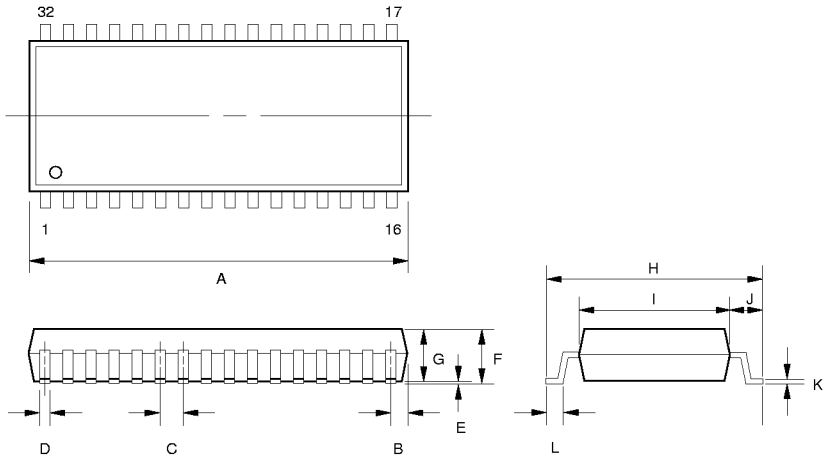
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



32-PIN PLASTIC SOP (450 mil)

ITEM	MILLIMETERS	INCHES
A	20.95 max.	.825 max.
B	1.00 [REF]	.039 [REF]
C	1.27 [TP]	.050 [TP]
D	.40 [Typ.]	.016 [Typ.]
E	.05 min.	.002 min.
F	3.05 max.	.120 max.
G	2.69±.13	.106±.005
H	14.12±.25	.556±.010
I	11.30±.13	.445±.005
J	1.42	.056
K	.20 [Typ.]	.008 [Typ.]
L	.79	.031

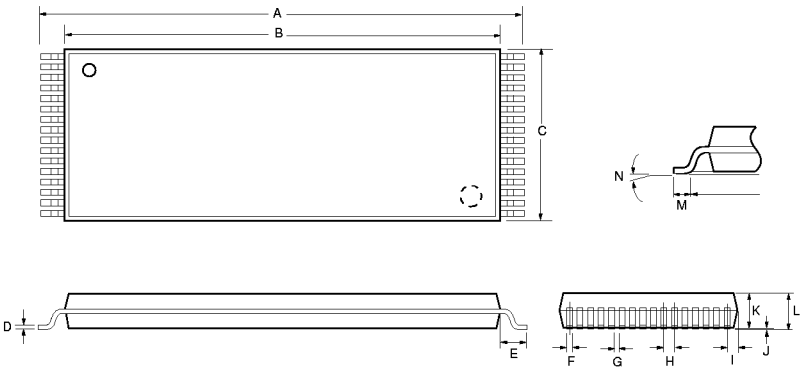
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



32-PIN PLASTICTSOP

ITEM	MILLIMETERS	INCHES
A	20.0±.20	.078±.006
B	18.40±.10	.724±.004
C	8.20 max.	.323 max.
D	.15 [Typ.]	.006 [Typ.]
E	.80 [Typ.]	.031 [Typ.]
F	.20±.10	.008±.004
G	.30±.10	.012±.004
H	.50 [Typ.]	.020 [Typ.]
I	.45 max.	.018 max.
J	0 ~ .20	0 ~ .008
K	1.00±.10	.039±.004
L	1.27 max.	.050 max.
M	.50	.020
N	0 ~ 5°	.500

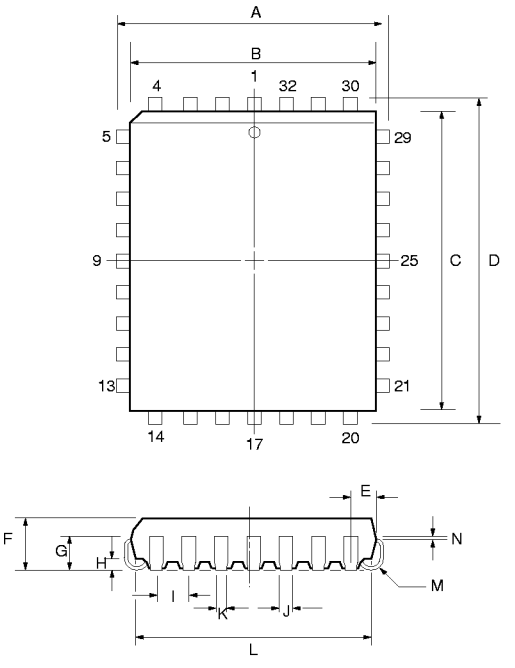
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



32-PIN PLASTIC LEADED CHIP CHARRIER (PLCC)

ITEM	MILLIMETERS	INCHES
A	12.44±.13	.490±.005
B	11.50±.13	.453±.005
C	14.04±.13	.553±.13
D	14.98±.13	.590±.13
E	1.93	.076
F	3.30±.25	.130±.010
G	2.03±.13	.080±.005
H	.51±.13	.020±.005
I	1.27 [Typ.]	.050 [Typ.]
J	.71 [REF]	.028 [REF]
K	.46 [REF]	.018 [REF]
L	10.40/12.94	.410/.510
	(W) (L)	(W) (L)
M	.89 R	.035 R
N	.25 [TYP.]	.010 [TYP.]

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



REVISION HISTORY

REVISION	DESCRIPTION	PAGE	DATE
3.9	To add 70ns speed grade	P2	NOV/23/1998
4.0	To add 45ns speed grade	P2	DEC/10/1998
4.1	To add Note:VIL min.	P2	JUN/16/1999