FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27204-3E

ASSP

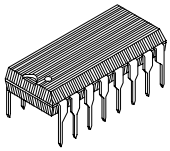
SWITCHING REGULATOR CONTROLLER

MB3775

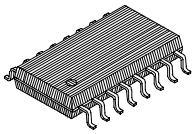
LOW VOLTAGE DUAL PWM SWITCHING REGULATOR CONTROLLER

The MB3775 is a dual pulse-width-modulation control circuit. It contains the basic circuits required for two PWM control circuits. Complete synchronization is obtained by using the same oscillator output waveform.
This IC can provide following types of output voltage: step down, step up, and inverter. Power consumption is low, thus the MB3775 is ideal for use in high-efficiency portable equipment.

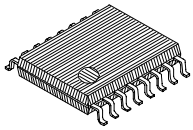
- Wide supply voltage range: 3.6 V to 18 V
- Low current consumption: 1.3 mA typical
- Wide oscillation frequency range: 1 kHz to 500 kHz
- On-chip timer latch short protection circuit
- On-chip under voltage lockout protection
- On-chip reference voltage: 1.28 V
- Variable dead time provides control over total operating range.



(DIP-16P-M04)



(FPT-16P-M06)



(FPT-16P-M05)

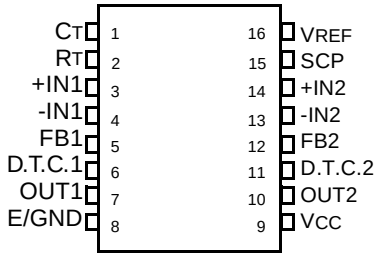
ABSOLUTE MAXIMUM RATINGS (see NOTE) (T_a = 25°C)

Rating	Symbol	Condition	Value	Unit
Power Supply Voltage	V_{CC}		20	V
Error Amp. Input Voltage	V_I		-0.3 to +10	V
Collector Output Voltage	V_O		20	V
Collector Output Current	I_O		75	mA
Power Dissipation	P_D	$T_a \leq$ 25 °C(SOP)	*620	mW
		$T_a \leq$ 25 °C(DIP)	1000	mW
		$T_a \leq$ 25°C(VSOP)	*430	mW
Operating Temperature	T_{OP}		-30 to +85	°C
Storage temperature	T_{stg}		-55 to+125	°C

***:** The packages are mounted on the epoxy board (4 cm x 4 cm x 1.5 mm)

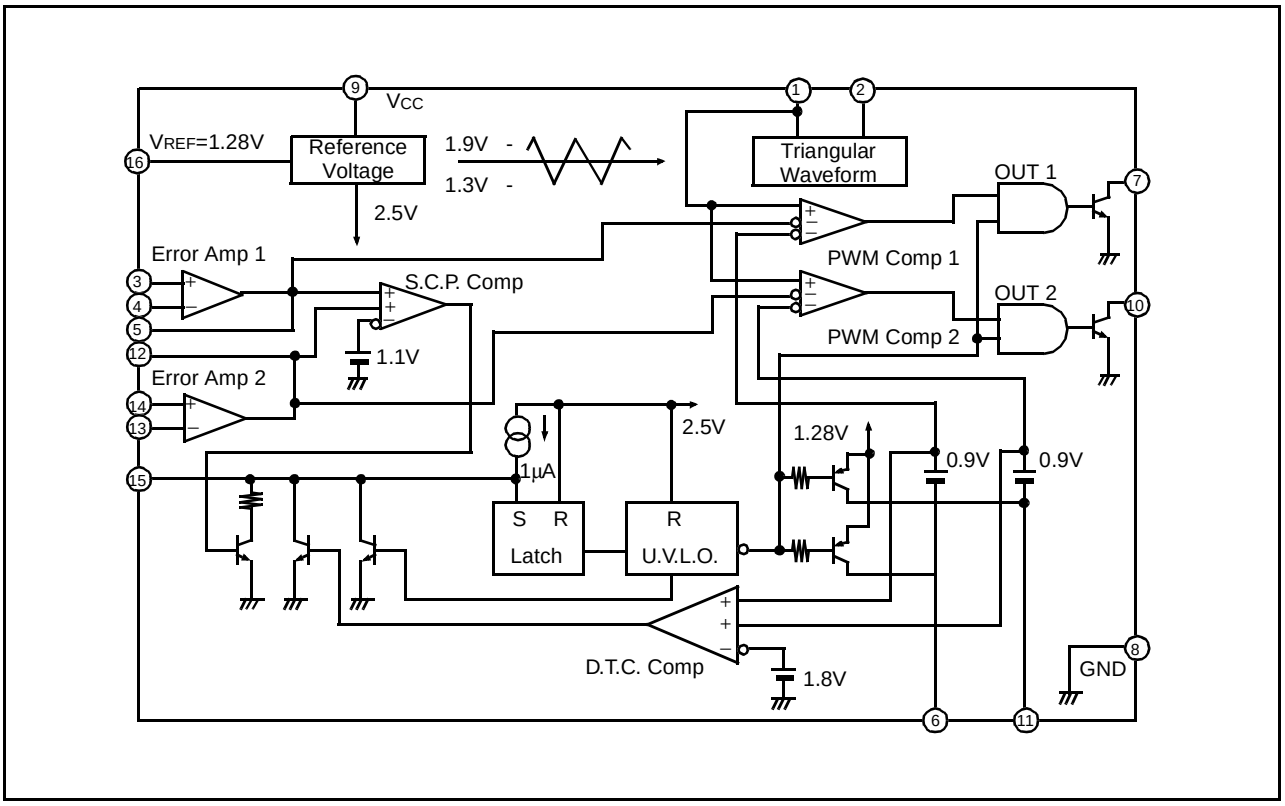
NOTE : Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT
(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

■ BLOCK DIAGRAM



■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	3.6	6.0	18	V
Error Amp. Input Voltage	V_I	-0.2	–	1.45	V
Collector Output Voltage	V_O	–	–	18	V
Collector Output Current	I_O	0.3	–	50	mA
Phase Compensation Capacitor	C_P	–	0.1	–	μF
Timing Capacitor	C_T	150	–	15000	pF
Timing Resistor	R_T	5.1	–	100	kΩ
Oscillator Frequency	f_{OSC}	1	–	500	kHz
Reference Voltage Output Current	I_{REF}	-3	-1	–	mA
Operating Temperature	T_{OP}	-30	25	85	°C

■ OPERATION DESCRIPTION

1. Reference voltage

The reference voltage circuit generates a stable, temperature-compensated 2.5 V reference from Vcc (pin 9) for use by internal circuits.
A reference voltage of temperature compensated 1/2 Vref can be obtained to external circuit by Vref terminal (pin 16).

2. Oscillator

A triangular waveform of any frequency is obtained by connecting an external capacitor and resistor to the C_T (pin 1) and R_T terminals (pin 2).
The amplitude of this waveform is from 1.3 V to 1.9 V. The oscillator is internally connected to the non-inverting inputs of the PWM comparators. The oscillator waveform is available at the C_T terminal.

3. Error amplifiers

The error amplifier detects the output voltage of the switching regulator.
The common-mode input voltage range is -0.2 V to 1.45 V, so the input reference voltage can be set the V_{REF} and GND levels. Error amplifiers can be used as either inverting and non-inverting amplifiers.
The voltage gain is fixed. Phase compensation is possible by connecting a capacitor to the FB terminals (pins 5 and 12) of the error amplifiers.
The error amplifier output are internally connected to the inverting inputs of the PWM comparators and also to the short protection circuit.

4. Timer latch short protection circuit

The timer latch short protection circuit detects the output levels of the error amplifiers. If one or both error amplifier outputs are 1.1 V or lower, the timer circuit begins charging the externally connected protection enable capacitor.
If the output level of the error amplifier does not drop below the normal voltage range before the capacitor voltage reaches the transistor base-emitter voltage V_{BE} ($\fallingdotseq$ 0.65 V), the latch circuit turns the output drive transistor off and sets the dead time to 100 %.

5. Under voltage lockout protection circuit

An ambiguous transition state at power-on or a momentary fluctuation in the supply line may result in loss of control and may adversely affect or even destroy the system. The under voltage lockout protection circuit compares the internal reference voltage level with the supply voltage level. If the supply voltage level falls below the reference level the latch circuit is reset the output drive transistor is turned off and the dead time is set to 100 %. The protection enable terminal (pin 15) is pulled “Low”.

6. PWM comparator

Each PWM comparator has two inverting inputs and one non-inverting input. This voltage-to-pulse-width converter controls the output pulse width according to the input voltage.
The PWM comparator turns the output drive transistor on when the oscillator triangular waveform is higher than the error amplifier output and the dead time control terminal voltage.

7. Output drive transistor

The open-collector output-drive transistors provide common-emitter output of 18 V dielectric capability. The output drive transistors can source up to 50 mA of drive current to the switching power transistor.

■ ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=6V)

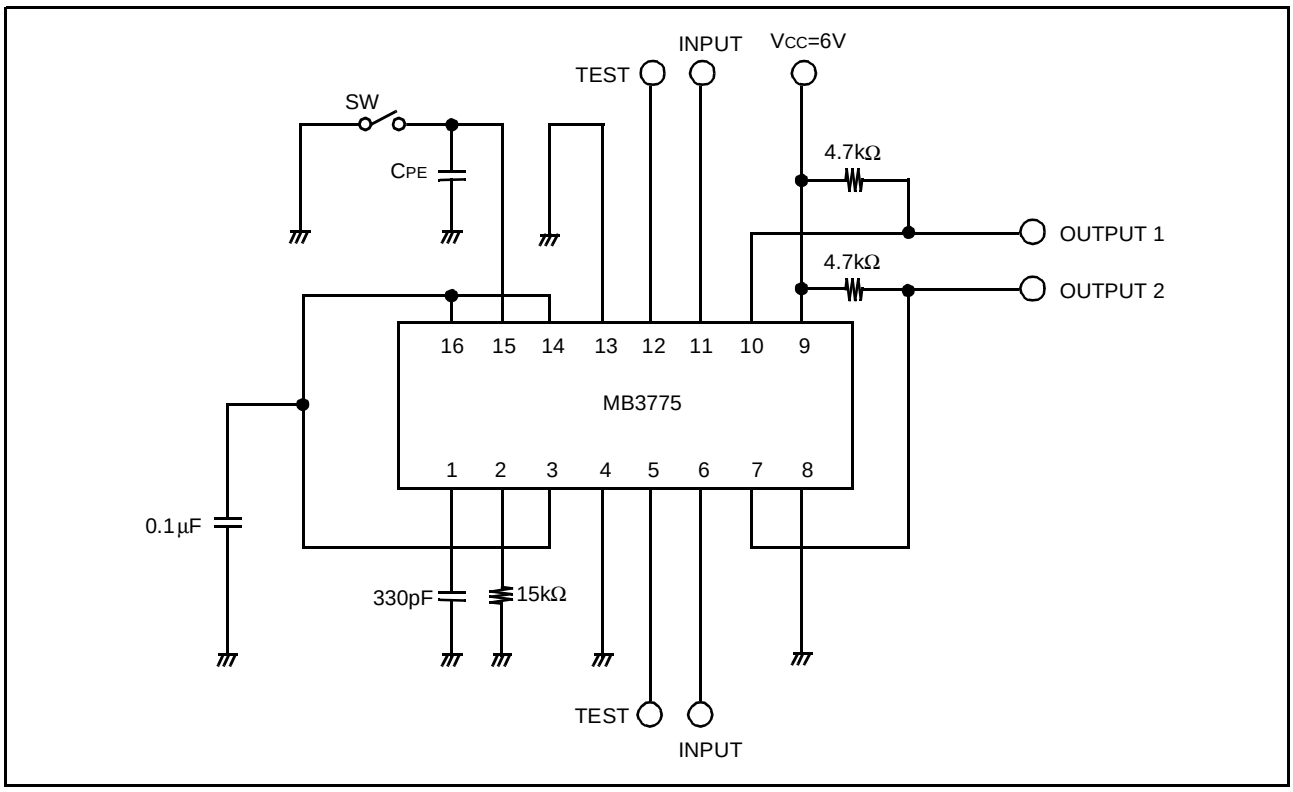
Parameter	condition	Symbol	Value			Unit
			Min	Typ	Max	
Reference Section						
Output Voltage	I_{OR} =-1 mA	V_{REF}	1.26	1.28	1.30	V
Output Temp. Stability	T_a = -30 °C to +85 °C	V_{RTC}	-2	±0.2	2	%
Input Stability	V_{CC} = 3.6 V to 18 V	Line	–	2	10	mV
Load Stability	I_{OR} = -0.1 mA to -1 mA	Load	–	1	7.5	mV
Short Circuit Output Current	V_{REF} = 0 V	I_{OS}	–	–30	–10	mA
Under Voltage Lockout Protection Section						
Threshold Voltage	I_{OR} = -0.1 mA	V_{tH}	–	2.72	–	V
	I_{OR} = -0.1 mA	V_{tL}	–	2.60	–	V
Hysteresis Width	I_{OR} = -0.1 mA	V_{HYS}	80	120	–	mV
Reset Voltage (V_{CC})		V_R	1.5	1.9	–	V
Protection Circuit Section						
Input Threshold Voltage		V_{tPC}	0.60	0.65	0.7	V
Input Stand by Voltage	No pull up	V_{STB}	–	50	100	mV
Input Latch Voltage	No pull up	V_I	–	50	100	mV
Input Source Current		I_{bpc}	-1.4	-1.0	-0.6	µA
Comparator Threshold Voltage	Pin 5, Pin 12	V_{tC}	–	1.1	–	V
Triangular Waveform Oscillator Section						
Ocillator Frequency	C_T = 330 pF, R_T = 15 kΩ	f_{OSC}	–	200	–	kHz
Frequency Deviation	C_T = 330 pF, R_T = 15 kΩ	f_{dev}	–	10	–	%
Frequency Stability (V_{CC})	V_{CC} = 3.6 V to 18 V	f_{dV}	–	1	–	%
Frequency Stability (T_a)	T_a = -30 °C to +85 °C	f_{dT}	-4	–	4	%
Dead-Time Control Section						
Input Threshold Voltage (f_{OSC} = 10 kHz)	Duty Cycle = 0 %	V_{t0}	–	1.0	V_{REF} -0.15	V
	Duty Cycle = 100 %	V_{t100}	0.2	0.4	–	V
Input Bias Current		I_{bdt}	–	-0.2	–1	µA
Latch Mode Source Current	V_{dt} = 0.7 V	I_{dt}	–	-150	-80	µA
Latch Input Voltage	Idt=-40 µA	V_{dt}	V_{REF} -0.1	–	–	V

■ ELECTRICAL CHARACTERISTICS (Continued)

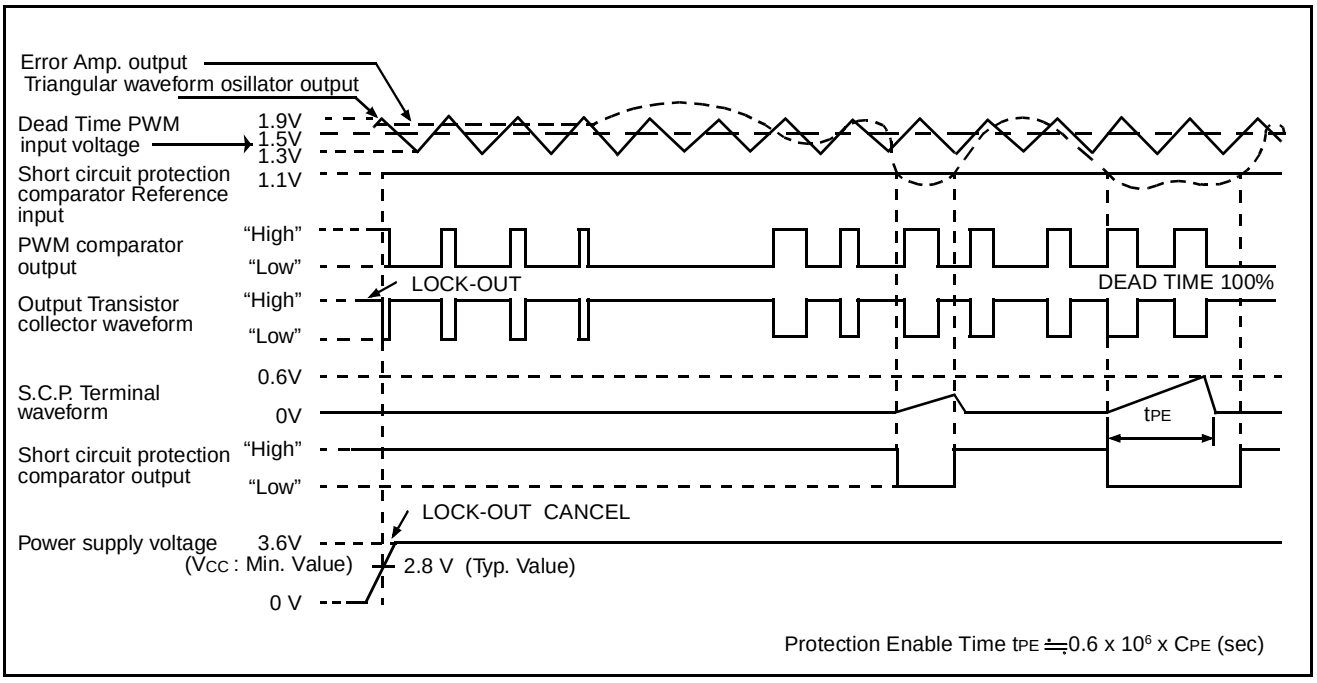
(T_a=25°C, V_{CC}=6V)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
Error Amp. Section						
Input Offset Voltage	V_O = 1.6 V	V_{IO}	-10	–	+10	mV
Input Offset Current	V_O = 1.6 V	I_{IO}	-100	–	+100	nA
Input Bias Current	V_O = 1.6 V	I_B	-500	-100	–	nA
Common Mode Input Voltage Range	V_{CC}=3.6V to 18V	V_{ICR}	-0.2	–	+1.45	V
Voltage Gain		A_V	84	120	–	V/V
Frequency Band Width	A_V = -3 dB	BW	–	3	–	MHz
Common Mode Rejection Ratio		CMRR	60	80	–	dB
Max. Output Voltage Width		V_{OM+}	2.2	2.4	–	V
		V_{OM-}	–	0.7	0.9	V
Output Sink Current	V_O = 1.6 V	I_{OM+}	24	50	–	µA
Output Source Current	V_O = 1.6 V	I_{OM-}	–	-1.2	-0.7	mA
PWM Comparator Section						
Input Threshold Voltage (f_{OSC}=10 kHz)	Duty Cycle = 0 %	V_{t0}	–	1.9	2.1	V
	Duty Cycle = 100 %	V_{t100}	1.05	1.3	–	V
Input Sink Current	Pin 5, Pin 12 = 1.6 V	I_{IN+}	24	50	–	µA
Input Source Current	Pin 5, Pin 12 = 1.6 V	I_{IN-}	–	-1.2	-0.7	mA
Output Section						
Output Leak Current	V_O=18V	Leak	–	–	10	µA
Output Saturation Voltage	I_O=50 mA	V_{SAT}	–	1.1	1.4	V
Stand by Current	Output “OFF”	I_{CCS}	–	1.3	1.8	mA
Average Supply Current	R_T=15kΩ	I_{CCa}	–	1.7	2.4	mA

■ TEST CIRCUIT



■ TIMING CHART (Internal Waveform)



■ APPLICATION CIRCUIT

Fig. 1 - Chopper Type Step Down/Inverting

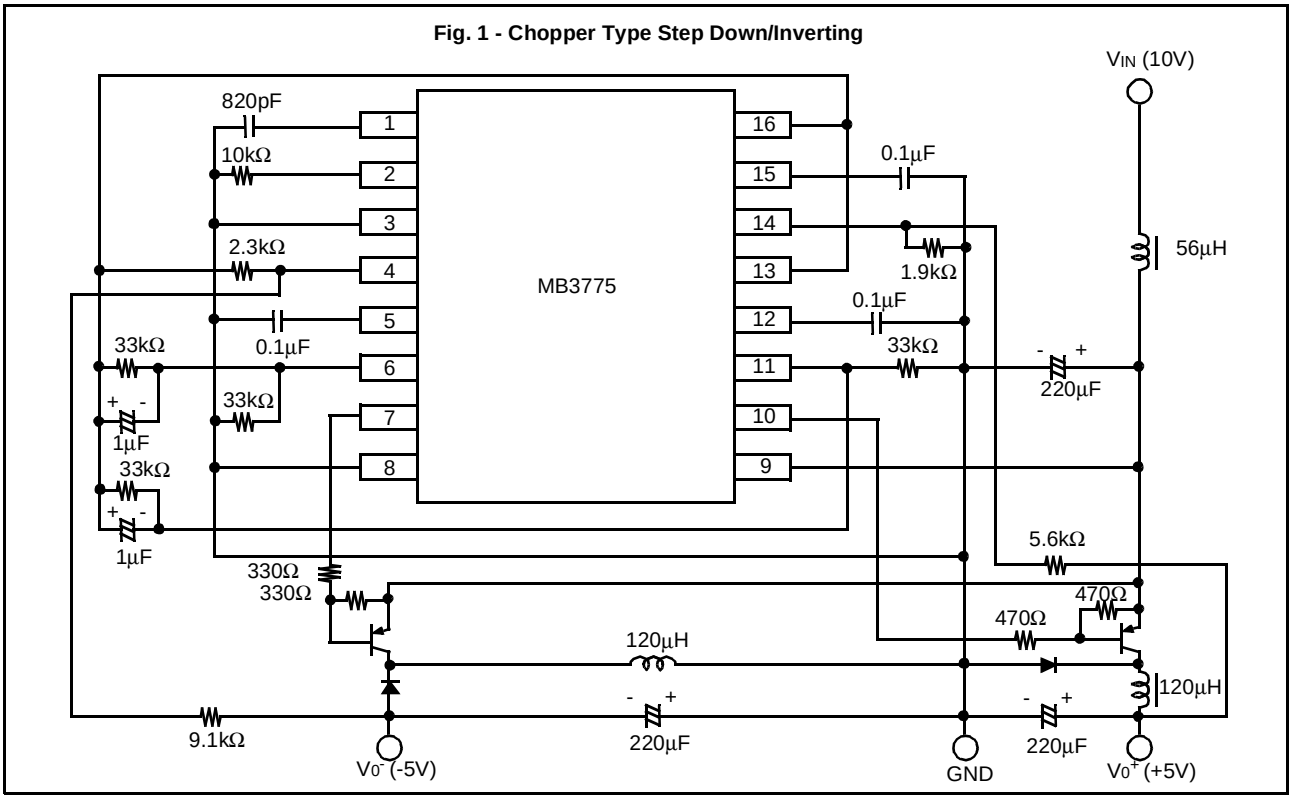
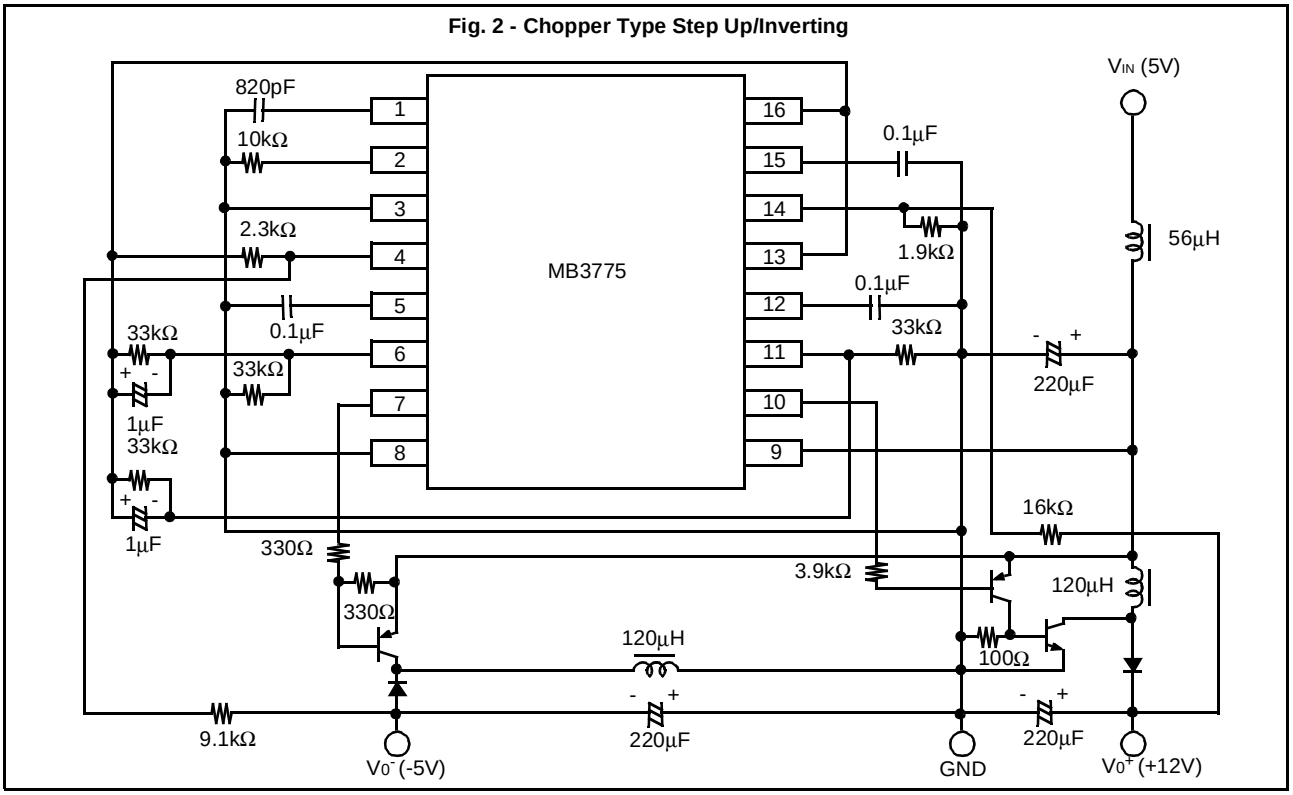


Fig. 2 - Chopper Type Step Up/Inverting



■ APPLICATION CIRCUIT (Continued)

Fig. 3 - Chopper Type Step Up/Inverting (For High Speed)

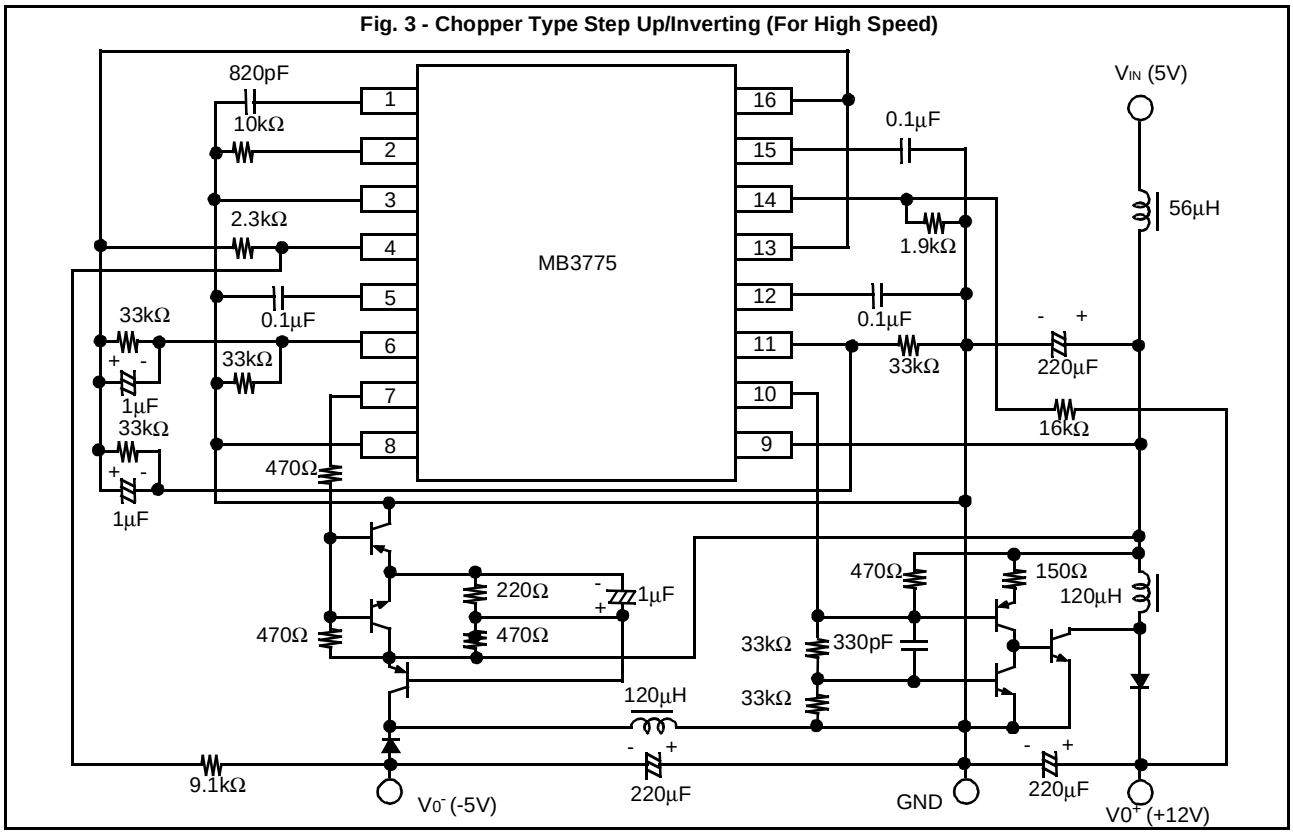
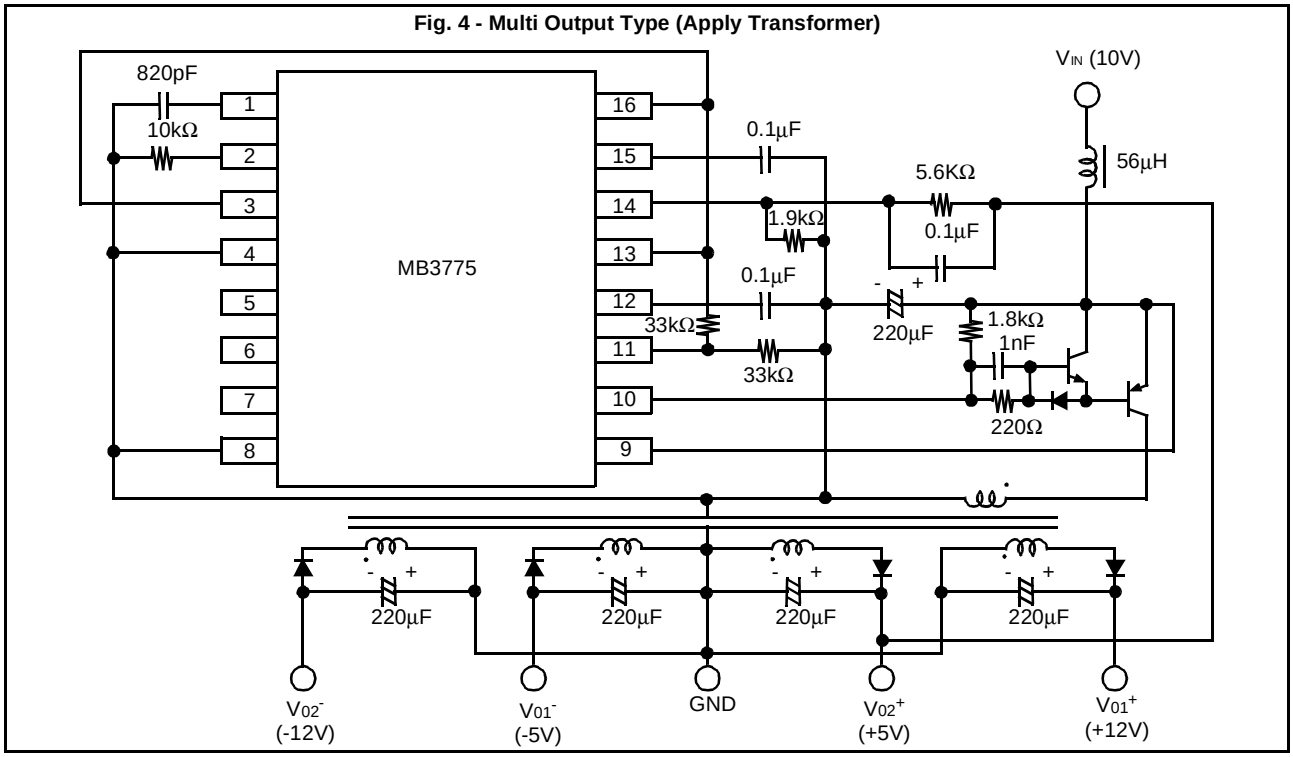


Fig. 4 - Multi Output Type (Apply Transformer)



■ HOW TO SET OUTPUT VOLTAGE

The output voltage is set using the connection shown in Fig. 5 and 6.
The error amplifiers are supplied to the internal reference voltage circuit as are the other internal circuits. The common-mode input voltage range is from -0.2 V to +1.45 V.

When the amplifiers are operated non-inverting, tie the inverting terminal to V_{REF} (≒1.28 V). When the amplifiers are operated inverting, tie the non-inverting terminal to ground.

Fig. 5 -Connection of Error Amp.
Output Voltage V_0 is plus

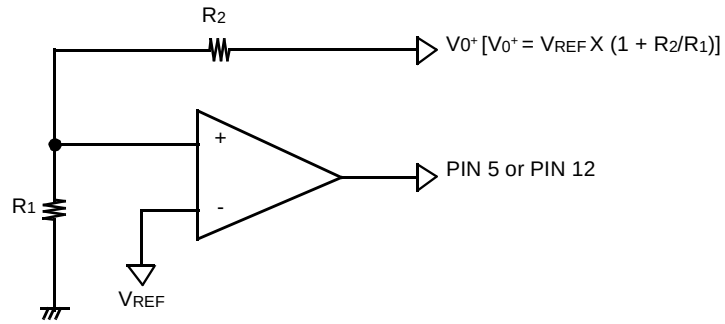
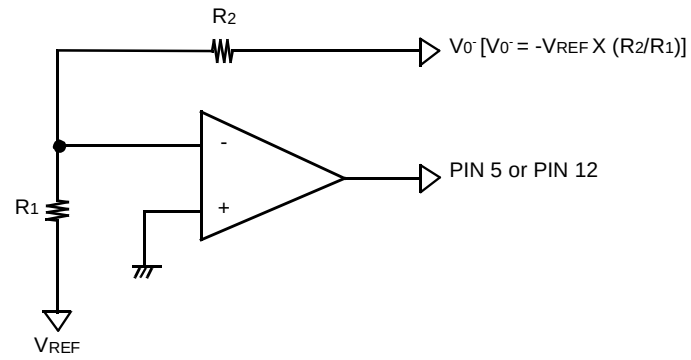


Fig. 6 -Connection of Error Amp.
Output Voltage V_0 is minus



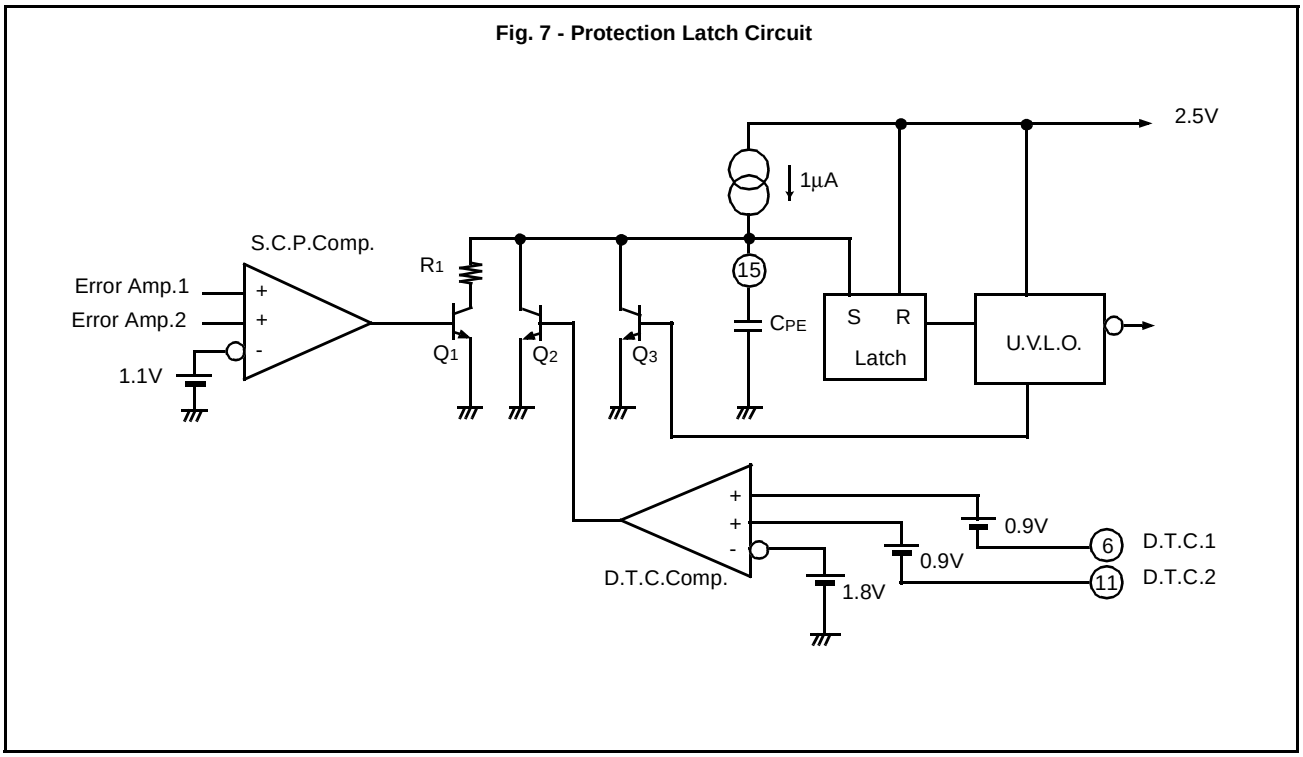
■ HOW TO SET TIME CONSTANT FOR TIMER LATCH SHORT PROTECTION CIRCUIT

TIMING CHART shows the configuration of the protection latch circuit.
Error amplifier outputs, are internally connected to the non-inverting inputs of the short-circuit protection comparator and are compared with the reference voltage (1.1 V) connected to the inverting input.
When the load condition of the switching regulator is stable, the error amplifier has no output fluctuation. Thus, short-circuit protection control is also kept in balance, and the protection enable terminal (pin 15) voltage is kept at about 50 mV.
If the load condition drastically changes due to a load short-circuit and if low-level signals (1.1 V or lower) are input to the non-inverting inputs of the short-circuit protection comparator from the error amplifiers, the short-circuit protection comparator outputs a “Low” level to turn transistor Q_1 off. The protection enable terminal voltage is discharged, and then the short-circuit protection comparator charges the externally connected protection enable capacitor C_{PE} according to the following formula:

$$V_{PE} = 50\ mV + t_{PE} \times 10^{-6}/C_{PE}$$
$$0.65 = 50\ mV + t_{PE} \times 10^{-6}/C_{PE}$$
$$C_{PE} = t_{PE}/0.6\ (\mu F)$$

When the protection enable capacitor charges to about 0.65 V, the protection latch is set to enable the under voltage lockout protection circuit and to turn the output drive transistor off. The dead time is set to 100 %.
Once the under voltage lockout protection circuit is enabled, the protection enable is released; however, the protection latch is not reset if the power is not turned off.
The non-inverting inputs of the D.T.C. comparator are connected to the D.T.C. terminals (pins 6 and 11) through the power supply (about 0.9 V) and are compared with a reference voltage (about 1.8 V) connected to the inverting input.
To prevent malfunction of the short protection circuit in soft-start mode (using D.T.C. terminals), the D.T.C. comparator outputs a “High” level to turn Q_2 on until the D.T.C. terminal voltage drops to about 0.9 V.

Fig. 7 - Protection Latch Circuit



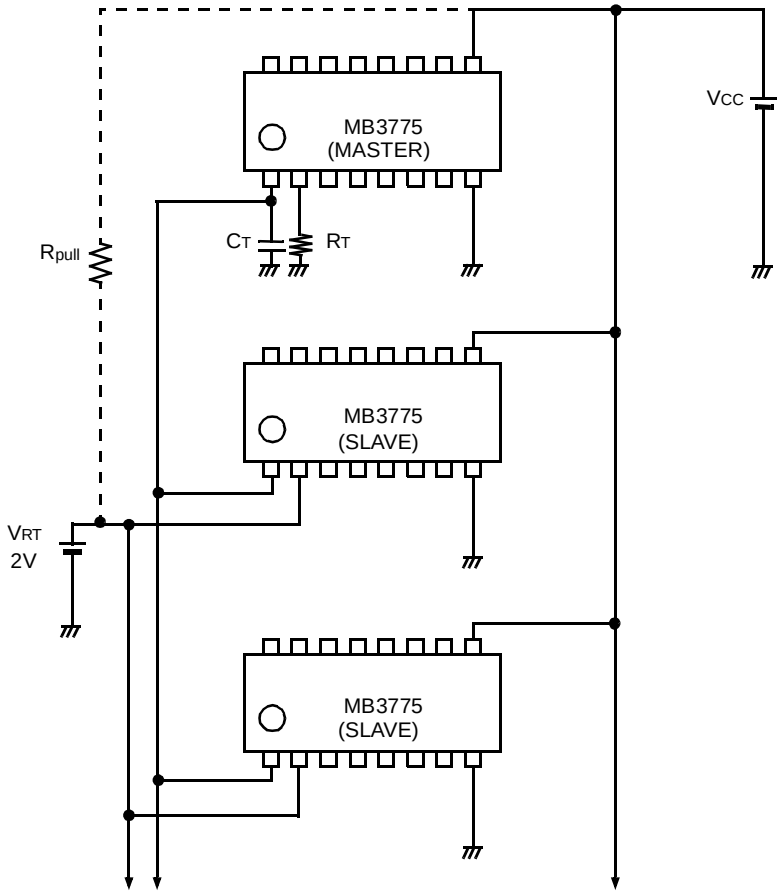
■ SYNCHRONIZATION OF ICs

To synchronize MB3775 ICs, first, the specified capacitor and resistor are connected to the C_T and R_T terminals of the master IC to start self oscillation. Next, 2 V is applied to the R_T terminals of the slave ICs to disable the charge/discharge circuit for triangular wave oscillation. Finally, the C_T terminals of the master and slave ICs are connected.
Instead of applying V_{RT} to the R_T terminals, these terminals can be pulled up by a resistor (see resistance indicated by the dashed line in Fig. 8). Select the pull-up resistance R_{pull} from the formula given below.

$$\frac{V_{CC}}{0.5 \times N} \leq R_{pull}$$

R_{pull}: Pull up Resistor (kΩ)
V_{CC}: Power Supply Voltage (V)
N: Number of Slave ICs

Fig. 8 - Connection of Master, Slave



■ TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 9 - Power supply voltage vs. Reference voltage

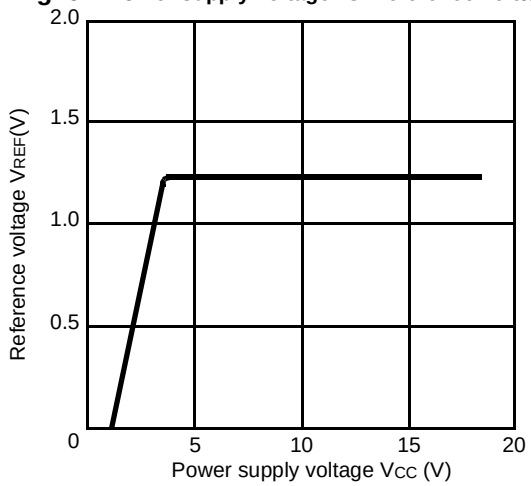


Fig. 10 - Power supply voltage vs. Average supply current

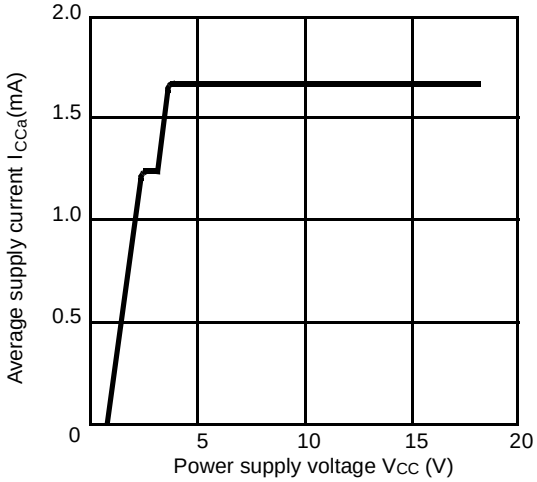


Fig. 11 - Power supply voltage vs. Stand by current

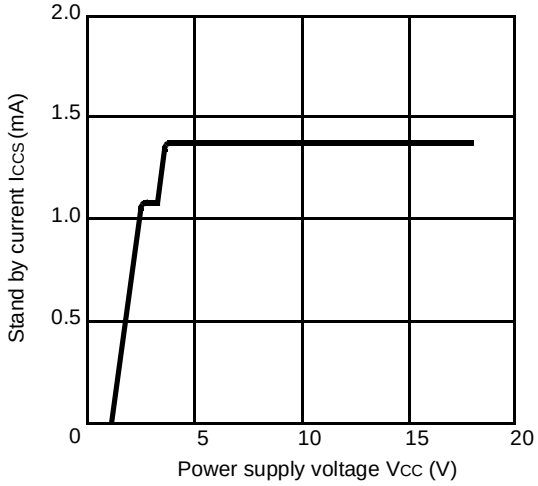


Fig. 12 - Reference voltage vs. Temp.

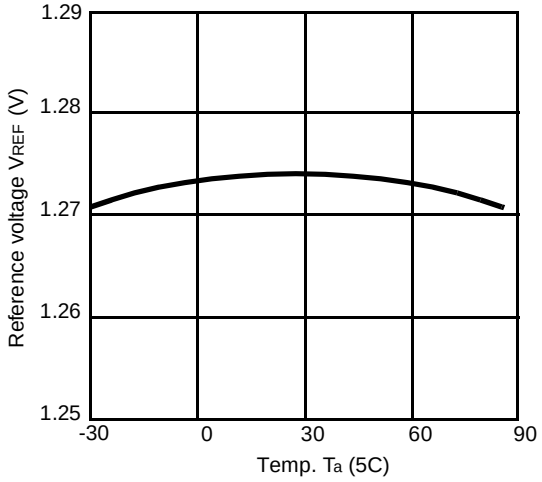


Fig. 13 - Collector saturation voltage vs. Sink current

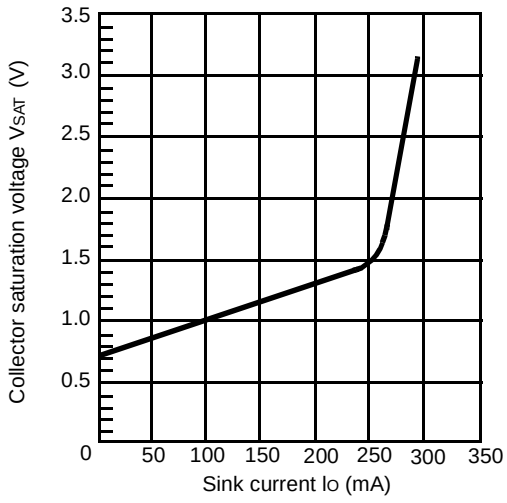
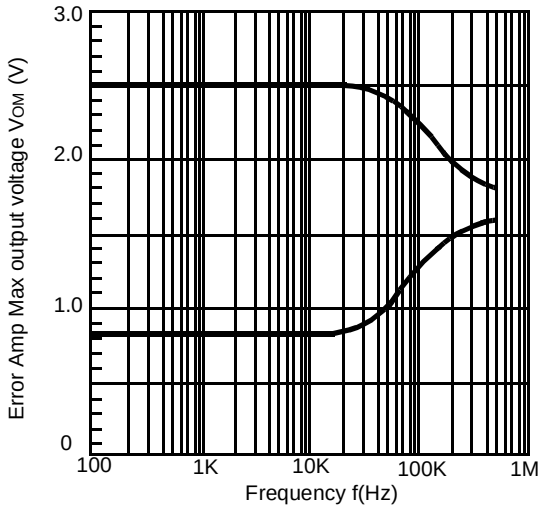


Fig. 14 - Error Amp. Max. output voltage vs. Frequency



■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 15 - Timing resistor vs. Oscillation Frequency

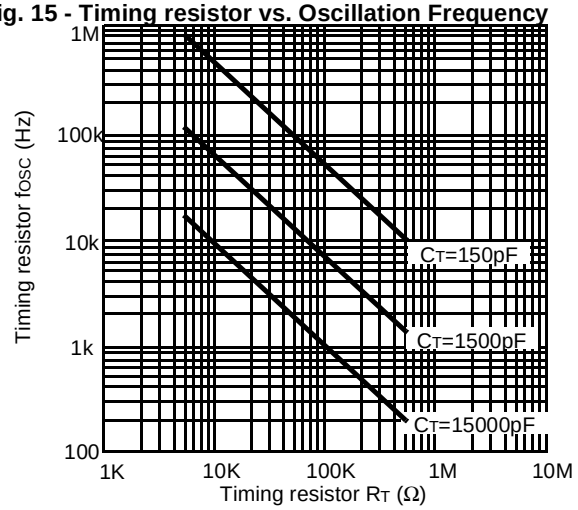


Fig. 16 - Triangular waveform cycle vs. Timing capacitor

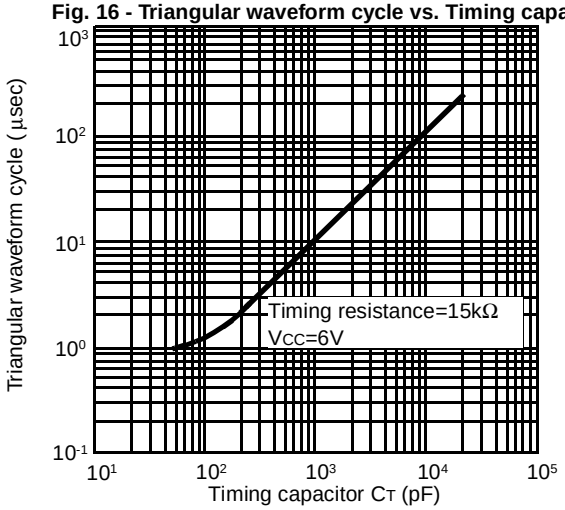


Fig. 17 - Timing capacitor vs. Triangular waveform Max. Amplitude voltage

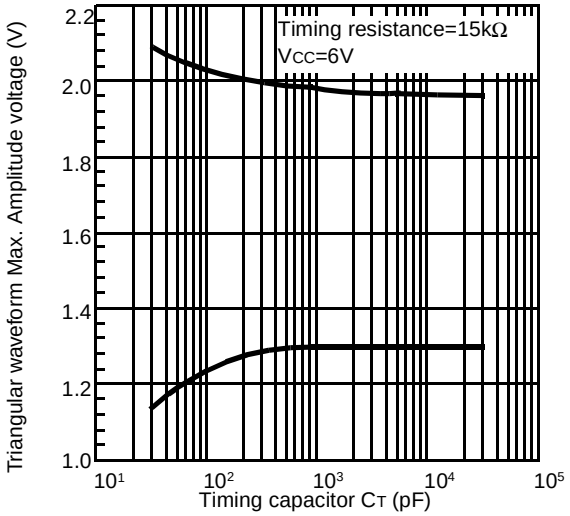


Fig. 18 - Frequency vs. Gain/Phase

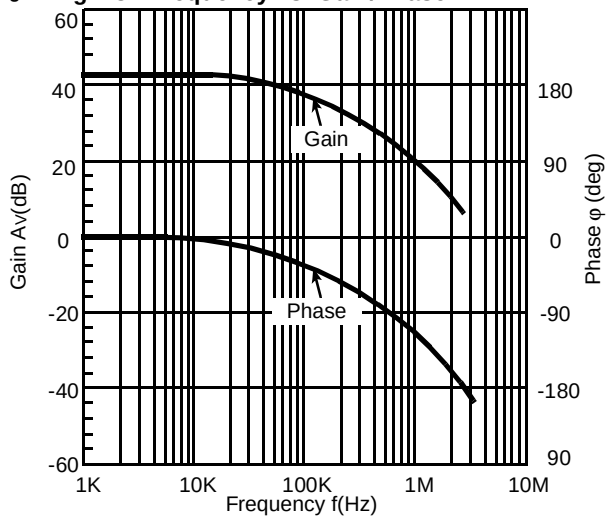


Fig. 19 - Frequency vs. Gain/Phase (Actual Data)

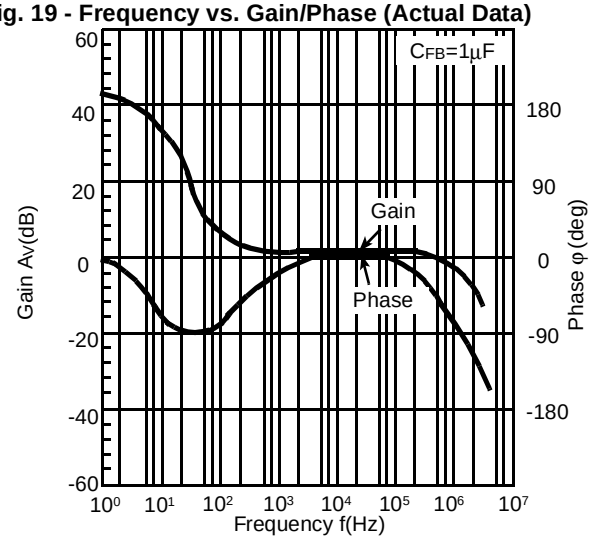
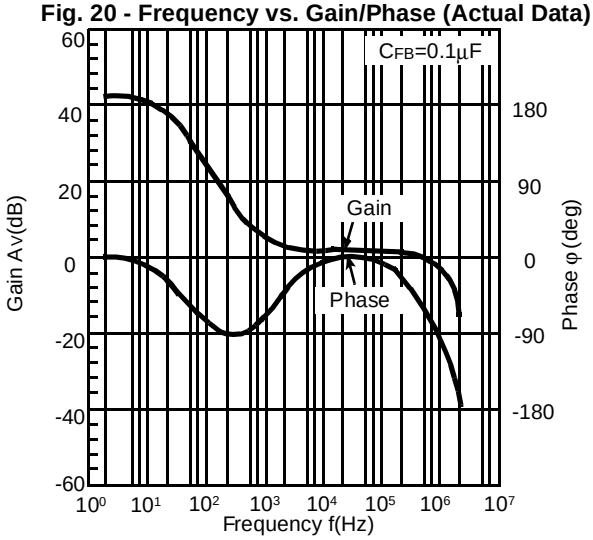
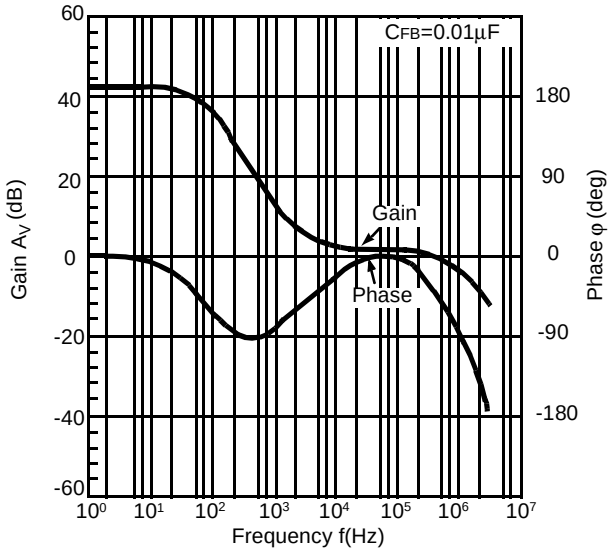


Fig. 20 - Frequency vs. Gain/Phase (Actual Data)



■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 21 - Frequency vs. Gain/Phase (Actual Data)



■ APPLICATION

1. How to set the error amplifier frequency characteristic

Figure 22 shows the equivalent circuit of the error amplifier.

The frequency characteristic of the error amplifier is set by R_1, R_2, and C_P. The high-frequency gain is set by the ratio of resistors R_1 and R_2 in the IC (set value ≒ 0 dB).

When C_P = 0.1 µF, the gain at 20 kHz ≤ f ≤ 5 MHz is about 0 dB. The roll-off frequency is adjusted by changing external phase compensating capacitor C_P (see Fig. 24).

When high frequency gain is needed or the phase must be advanced at a low frequency, connect a resistor R_P between the FB terminal and C_P as shown in Figure 23 (see Fig. 25).

Fig. 22 - Error Amp. Equivalent Circuit

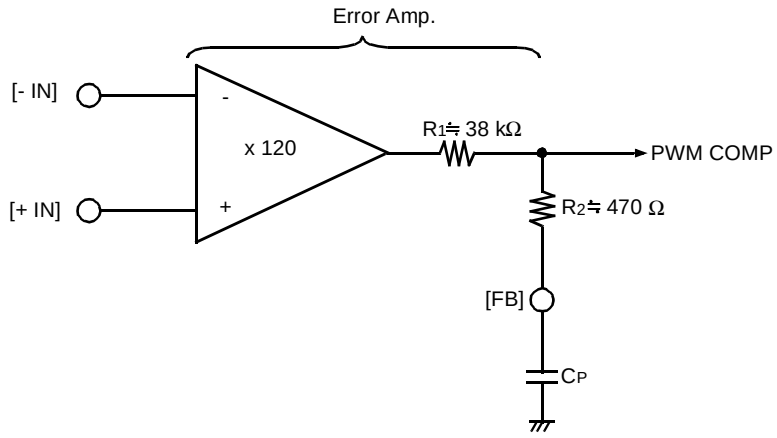
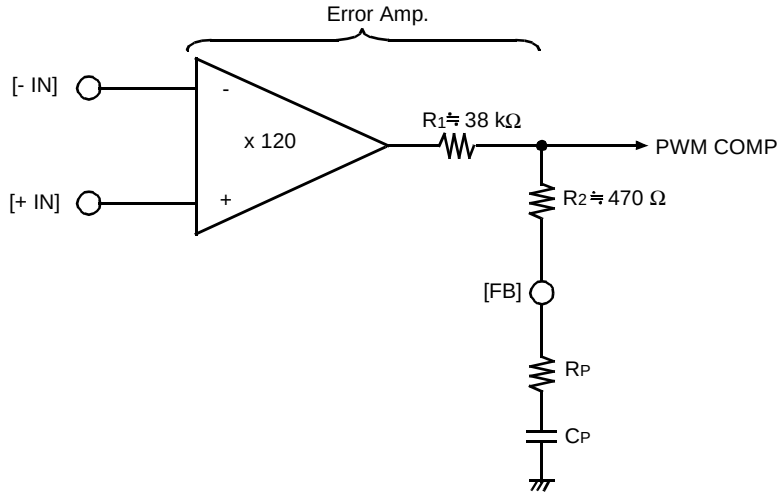


Fig. 23 - Error Amp. Equivalent Circuit (Insert R_P)



NOTE: As shown above, the frequency characteristic of the error amplifier is set by the external phase compensating capacitor CP.
When a ceramic chip capacitor must be used to meet the requirements of a small system, be careful of its temperature characteristic. (-30 °C≒1/5 and 80 °C≒1/3 for the frequency characteristic, so a sufficient phase margin must be allowed for at room temperature.) Ceramic chip capacitors with a low temperature characteristic (B characteristic) or film capacitors are recommended (see Fig. 26 to 28).

Fig. 24 - Error Amp. Frequency characteristics

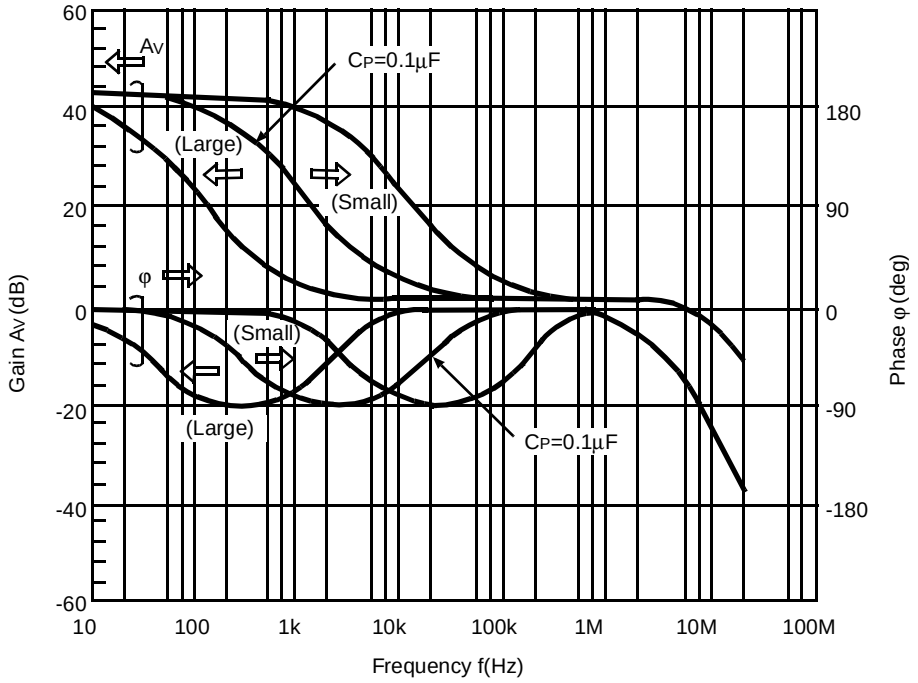


Fig. 25 - Error Amp. Frequency characteristics

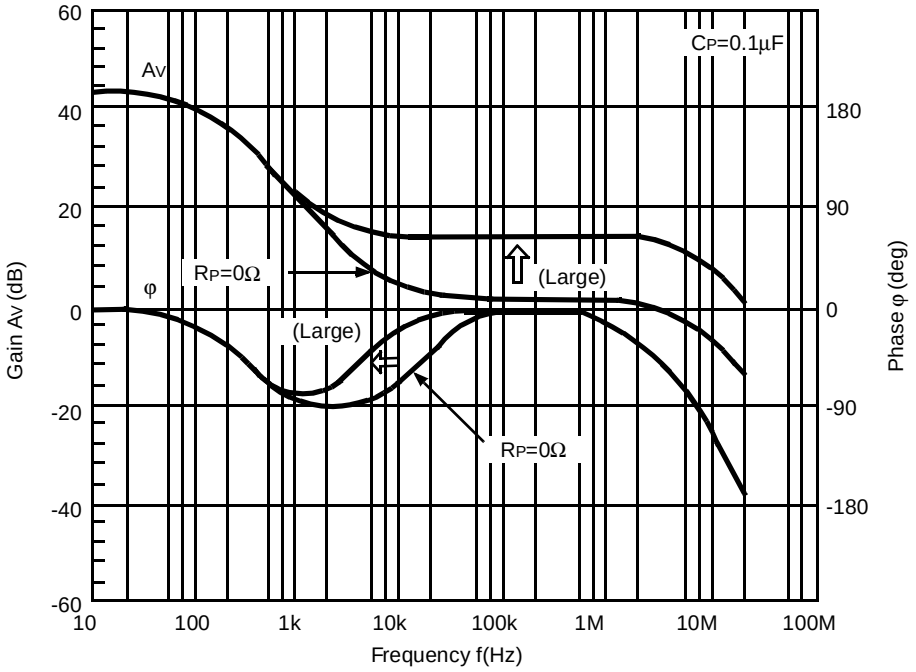


Fig. 26 - Ceramic Chip Capacitor (0.1 μF)

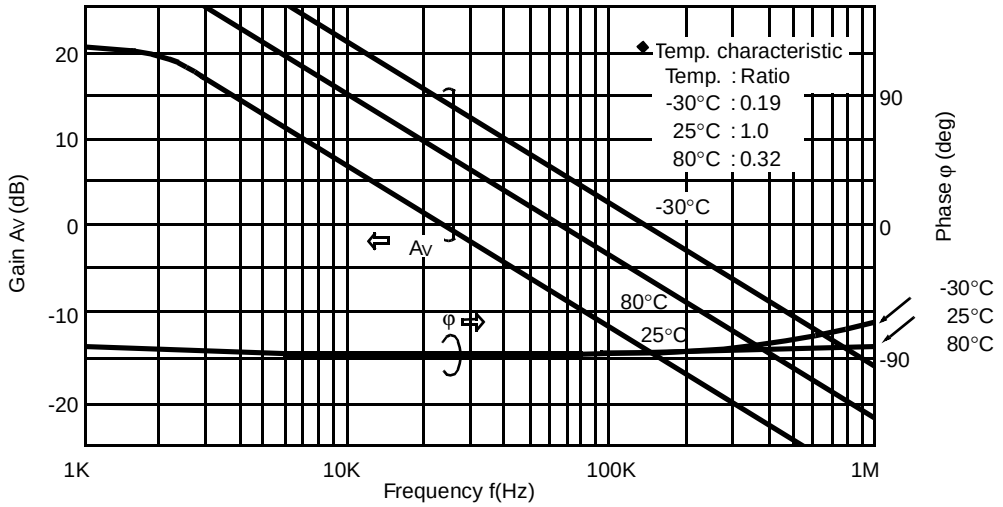


Fig. 27 - Tantal Capacitor (0.33 μF)

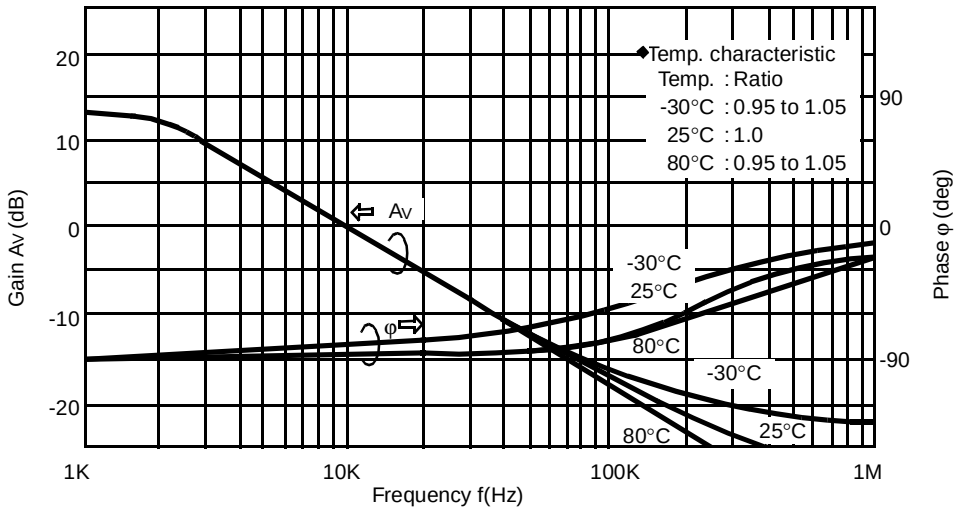
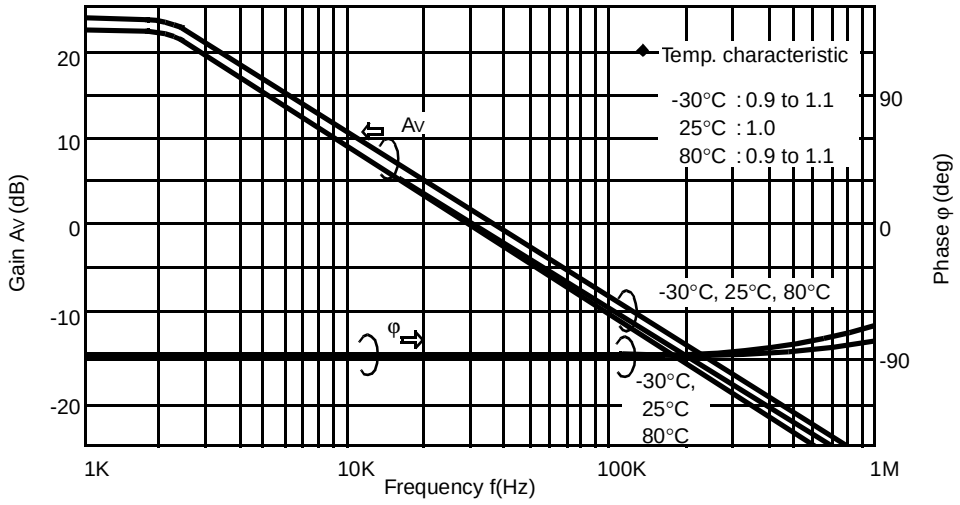


Fig. 28 - Film Capacitor (0.1 μF)



2. Effect of equivalent series resistance of smoothing capacitor

The equivalent series resistance (ESR) of the smoothing capacitor in the DC/DC converter greatly affects the loop phase characteristic. A smoothing capacitor with a low ESR reduces system stability by increasing the phase shift in the high-frequency region (see Fig. 30). Therefore, a smoothing capacitor with a high ESR will improve system stability. Be careful when using low ESR semiconductor electrolytic capacitors (OS-CON) and tantalum capacitors.

Fig. 29 - Step Down DC/DC Converter Basic Circuit

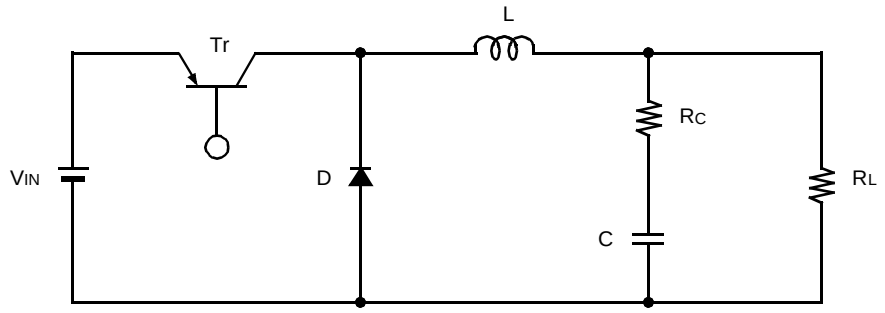


Fig. 30 - Gain vs. Frequency

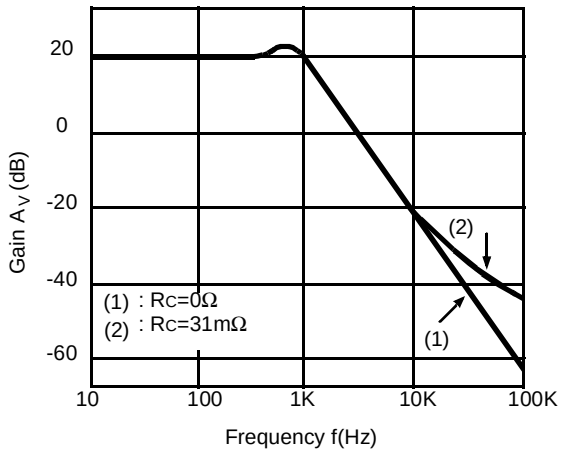
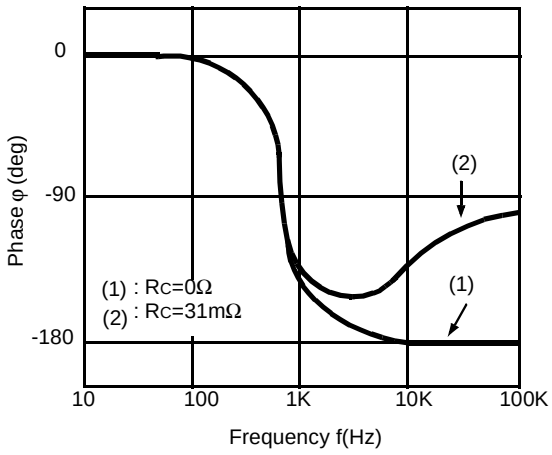


Fig. 31 - Phase vs. Frequency



Reference data

If an aluminum electrolytic smoothing capacitor ($R_C \fallingdotseq 1.0\Omega$) is replaced with a low ESR semiconductor electrolytic capacitor (OS-CON: $R_C \fallingdotseq 0.2\ \Omega$), the phase shift is reduced by half (see Fig. 33 and 34).

Fig. 32 - DC/DC Converter A_V vs. φ characteristic Test Circuit

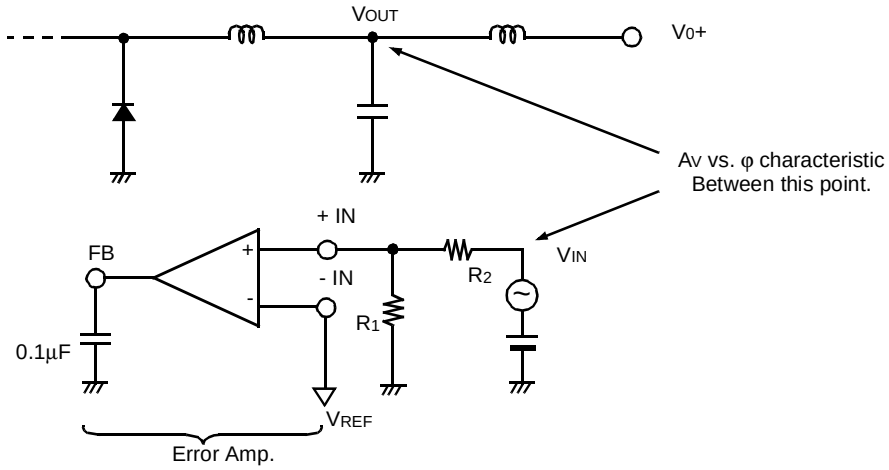


Fig. 33 - DC/DC Converter +5 V output

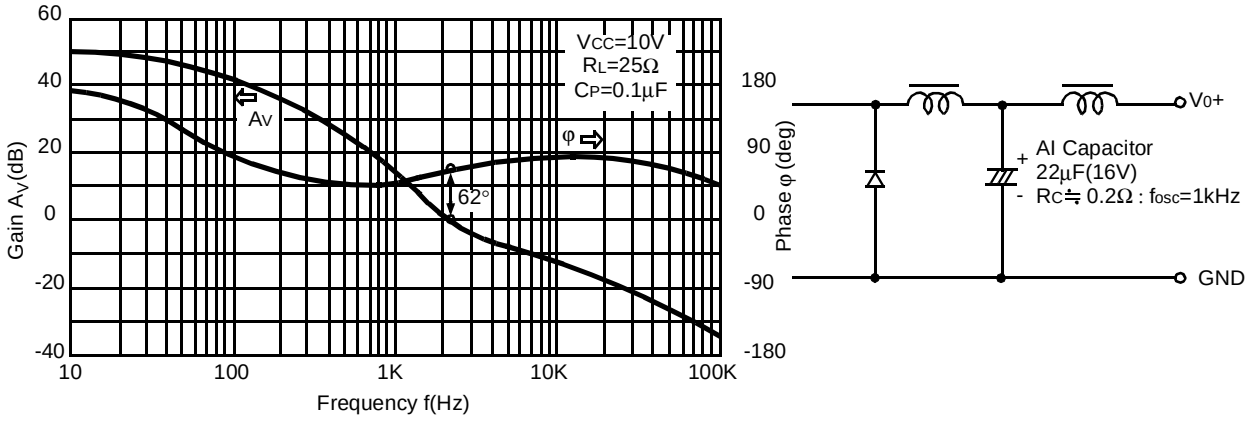
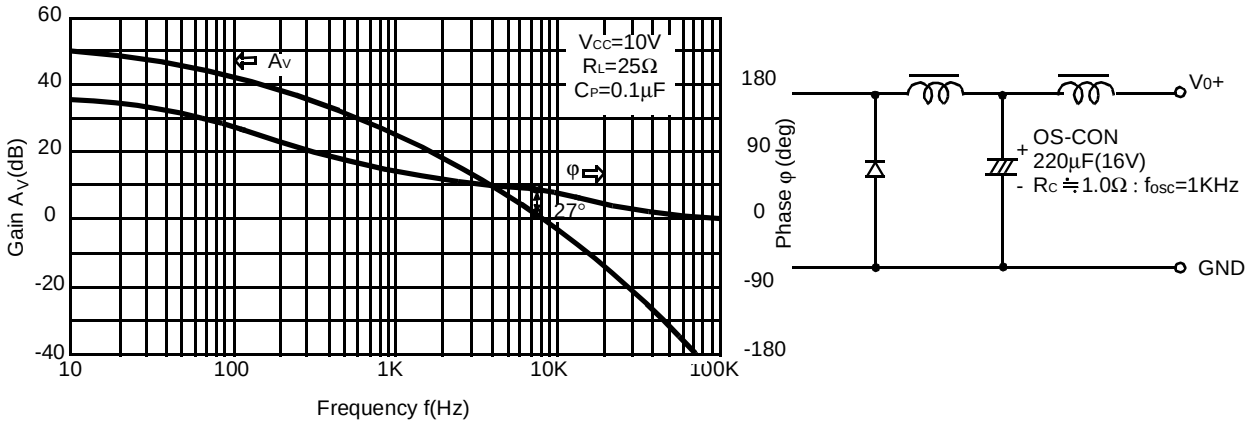


Fig. 34 - DC/DC Converter +5 V output



3. Measures for ensuring system stability when a low ESR smoothing capacitor is used

When a low ESR smoothing capacitor is used in the DC/DC converter, only the L and C are apparent even in the high-frequency region, and the phase is delayed by almost 180°. Consequently, the system phase margin and stability are reduced. On the other hand, a low ESR capacitor is needed to reduce the amount of output ripple. This is contrary to the system stability explained above.
To solve this problem, phase compensation can be used. This method increases the phase margin by advancing the phase when the phase margin is reduced by a low ESR capacitor.
The three suggestions listed below are recommended for DC/DC converters using the MB3775.

(1) As shown in Fig. 35, a capacitor is connected in parallel with the output feedback resistor to advance the phase. Use the formula below as a guideline for the capacitance.

$$C_1 \fallingdotseq \frac{1}{2\pi f R_2}$$

f: Unstable Frequency (See Fig. 32)

Fig. 35 - External circuit example1 to advance the phase

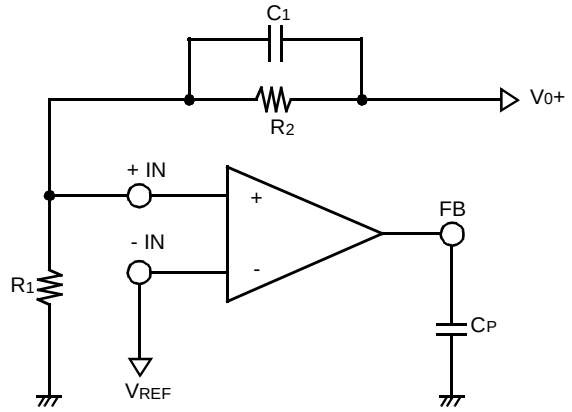
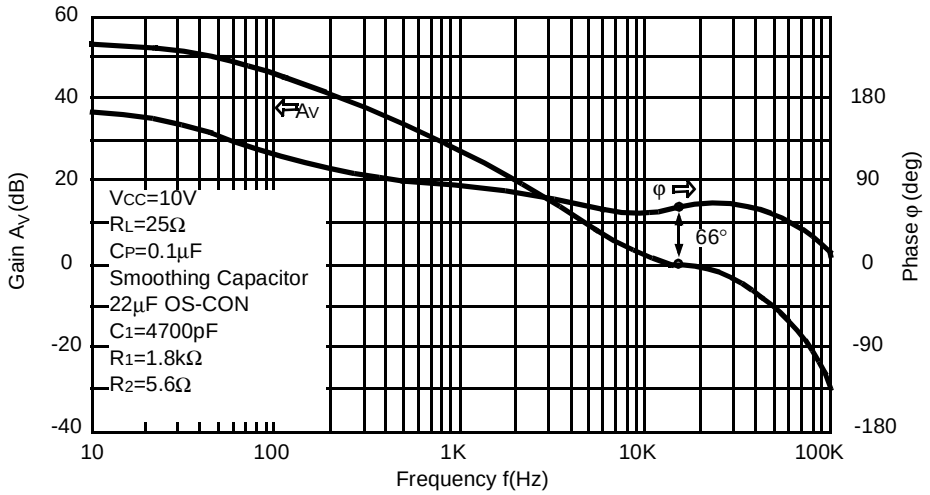


Fig. 36 - DC/DC Converter +5 V output



3. Measures for ensuring system stability when a low ESR smoothing capacitor is used (Continued)

(2) As shown in Figure 37, a resistor (R_P) is connected between the FB terminal and C_P of the error amplifier to advance the phase. The more R_P is increased, the more the phase is advanced. However, the gain in the high-frequency range is also increased, which causes instability. Therefore, select the optimum resistance (see Fig. 38).

Fig. 37 - External circuit example 2 to advance the phase

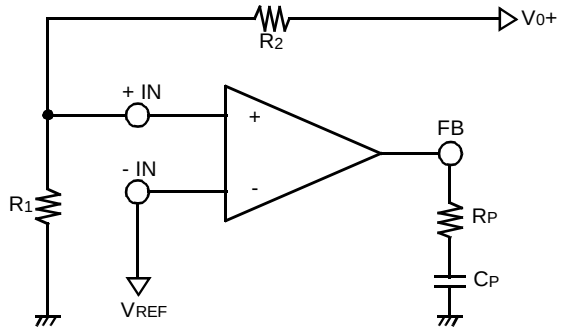
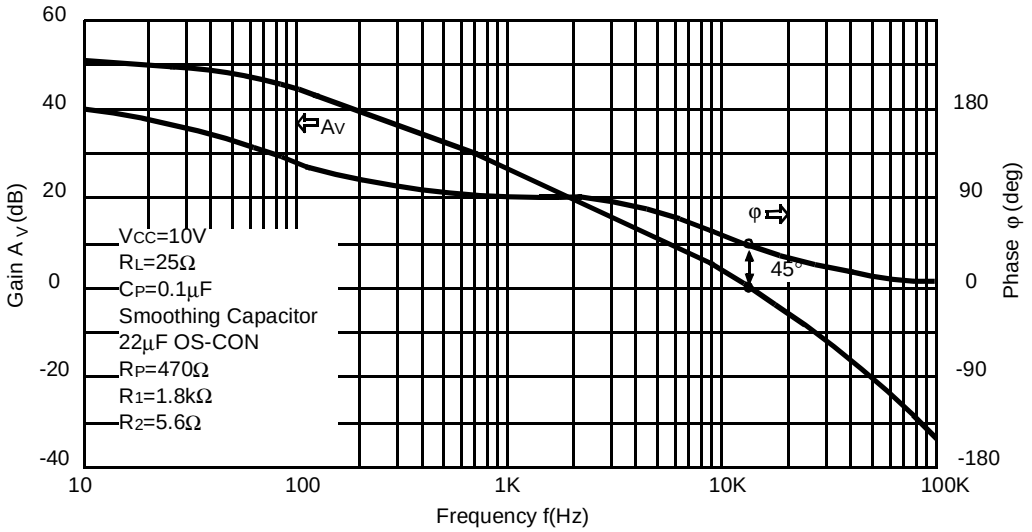
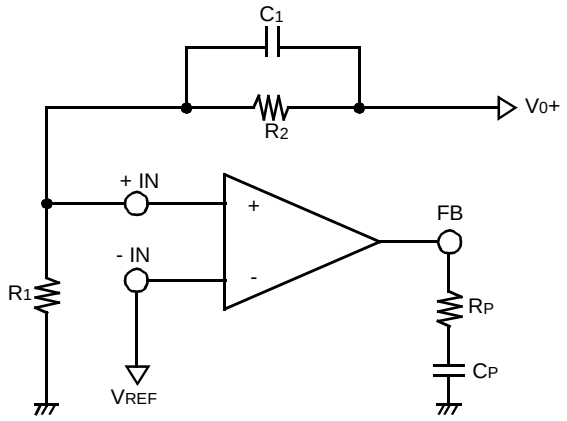


Fig. 38 - DC/DC Converter +5 V output



(3) As shown in Fig. 39, the phase is advanced by using both example 1 and 2 (Fig. 35 and 37).

Fig. 39 - External circuit example 3 to advance the phase

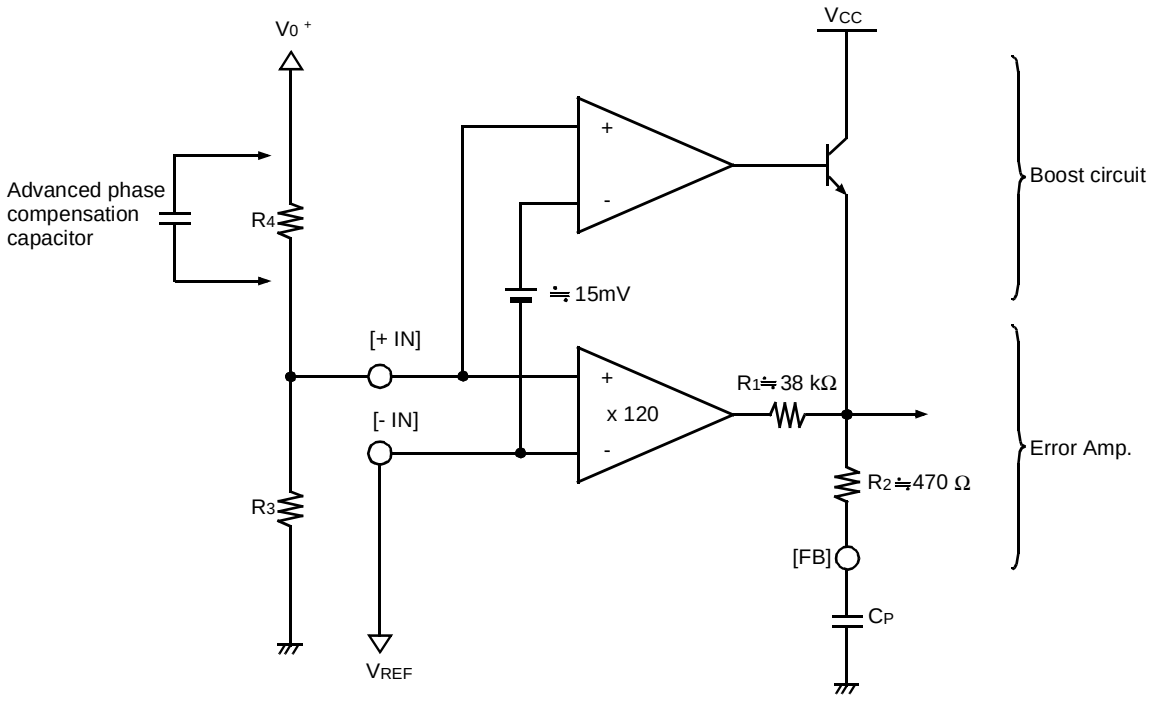


4. Error amplifier input ripple voltage

The boost circuit for charging the phase compensating capacitor C_P is connected to the error amplifier as shown in Figure 40 to protect against output voltage overload at power-on.

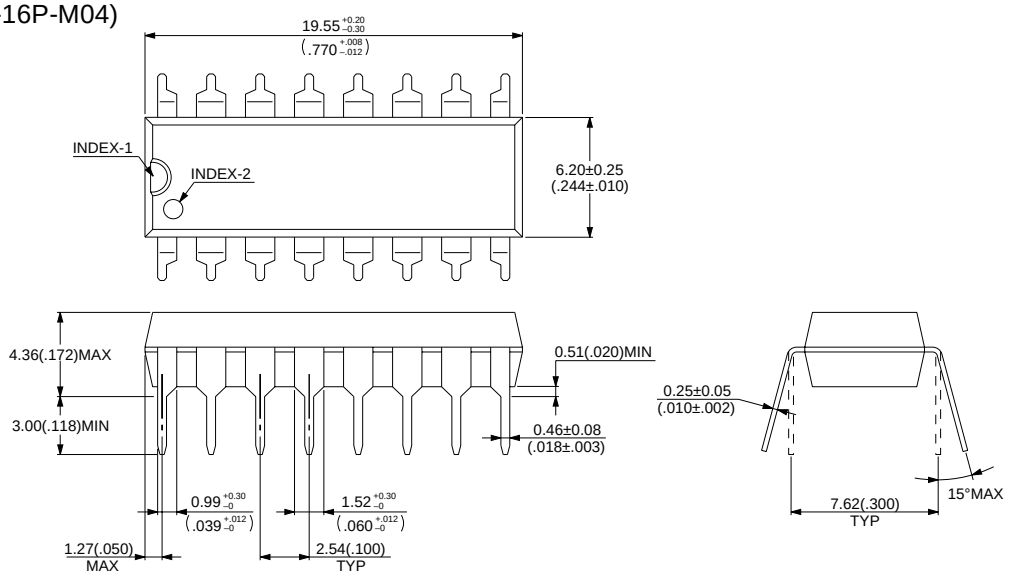
A 15 mV offset voltage is provided for the negative input side so that the boost circuit only operates at power-on. When a capacitor is connected in parallel with the output feedback resistor, because the output ripple is too large or for advanced phase compensation, the boost circuit starts operating, which may degrade regulation if the differential input voltage of the error amplifier exceeds 15 mV. Be careful with the differential input voltage of the error amplifier.

Fig. 40 - Error Amp. /Boost Equivalent circuit



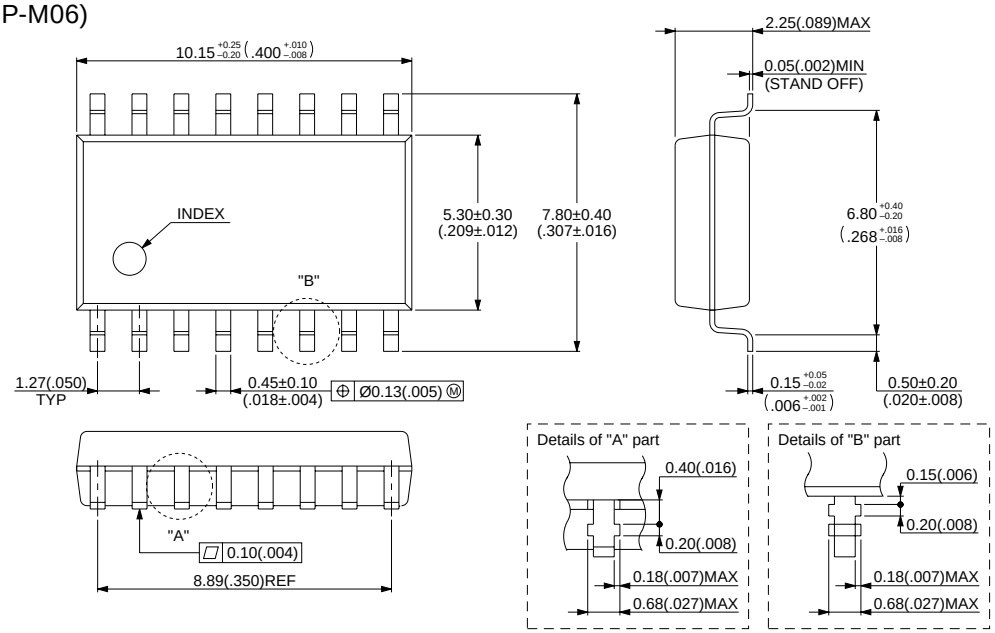
■ PACKAGE DIMENSIONS

16 pins, Plastic DIP
(DIP-16P-M04)



Dimensions in mm (inches).

16 pins, Plastic SOP
(FPT-16P-M06)



Dimensions in mm (inches).

16 pins, Plastic SOP
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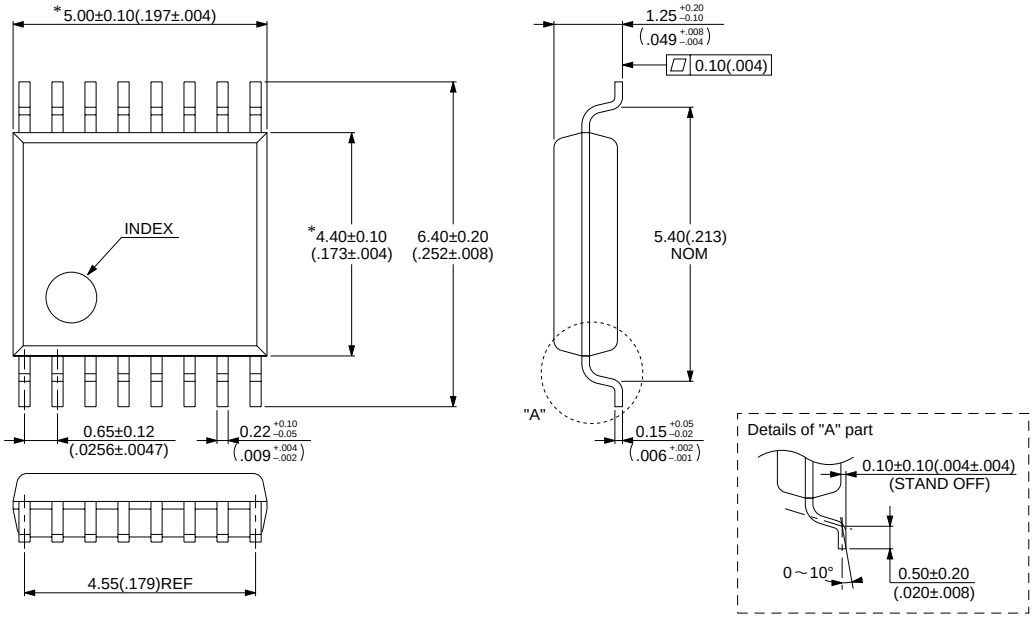

Dimensions in mm (inches).

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