HT81R30

5.6 Sec Speech Chip with EPROM

Features

- Operating voltage: 3.5V~5.0V
- 5.6-second voice capacity at about 6kHz sampling rate
- Functions compatible with the HT811XX, HT812XX and HT813XX series speech products
- Internal EPROM for one time programming (OTP)
- Directly driving the external transistor
- Low standby current (1μA Typ.)
- Supported by development system with recording & programming capabilities
- Programmable options for
  - Retrigger/non-retrigger keys
  - 0/4/8/16 sections for sequence group size (KEY1 only)
  - 700μs/22ms/180ms key debounce time
  - 200kΩ/100kΩ/50kΩ/20kΩ key pull-high resistance
  - 3Hz/busy/end-pulse flag output

Applications

- Toys
- Alarm clocks
- Public address system
- Alert & warning system
- Sound effect generators
- Products with a speech interface

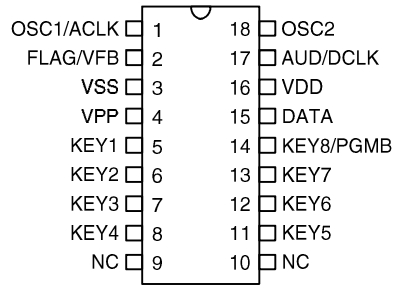
General Description

The HT81R30 is a PCM voice synthesis LSI with a built-in EPROM which provides 5.6-second voice capacity. Blocks within the chip include a timing generator, programming circuitry, a D/A converter and control circuitry for the key options.

The HT81R30 can be programmed one time only for simulating the mask ROM type bodies. In addition, the customer's voice data can be recorded and programmed into the internal EPROM array without changing any mask. Comparing to the masked products chip, it provides fast throughput and a small quality alterative for the instant-personalized products.

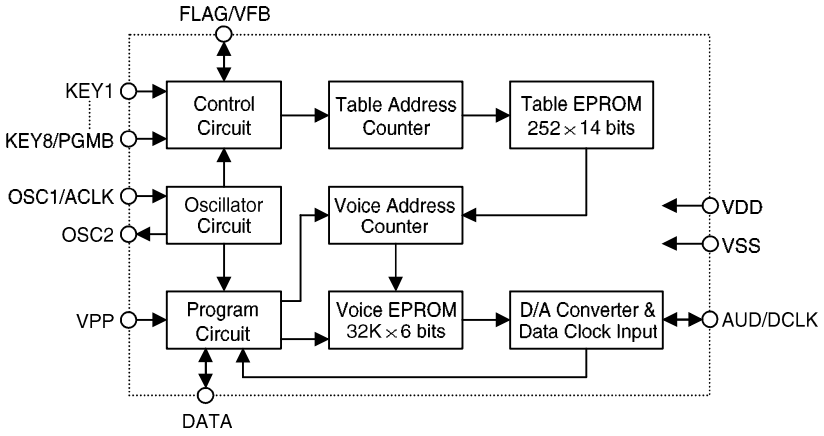
The HT81R30 is supported by a development system with recording & programming, and is functionally compatible with the HT811XX, HT812XX and HT813XX series speech products.

Pin Assignment

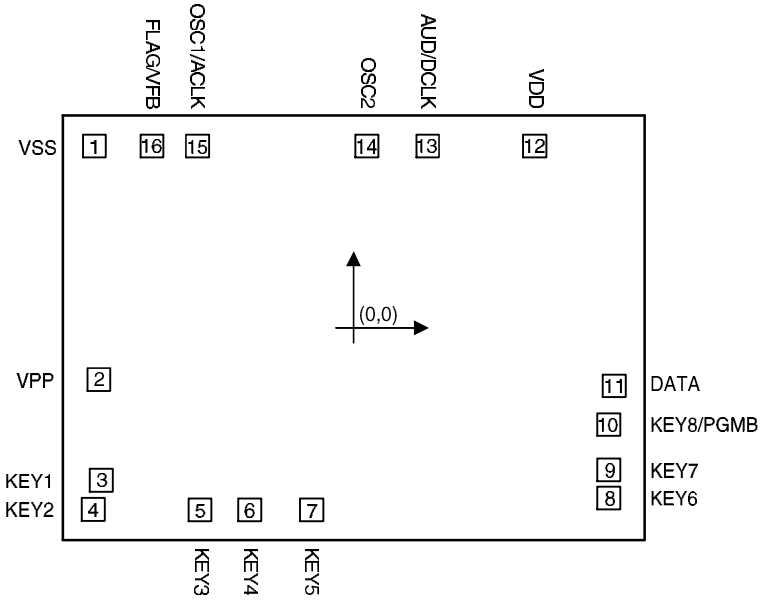


HT81R30
– 18 DIP

Block Diagram



Pad Assignment



Chip size: 3790×2820 (μm)^2

∗ The IC substrate should be connected to VSS in the PCB layout artwork.

Pad Coordinates

Unit: μm

Pad No.	X	Y	Pad No.	X	Y
1	–1694.65	1193.95	9	1678.15	–931.95
2	–1666.65	–337.95	10	1678.15	–634.95
3	–1650.65	–1000.95	11	1715.15	–382.15
4	–1703.65	–1190.95	12	1193.85	1193.85
5	–1002.65	–1193.95	13	493.65	1193.85
6	–676.35	–1193.95	14	93.45	1193.95
7	–270.95	–1193.95	15	–1020.65	1193.95
8	1678.15	–1116.95	16	–1316.35	1193.95

Pin Description

Pin No.	Pin Name	I/O	Internal Connection	Description	
				Read Mode	Program Mode
1	OSC1/ACLK	I	—	Oscillator input pin	Clock input for the internal address counter
2	FLAG/VFB	O/I	NMOS Open Drain	End-pulse, 3Hz flash or busy output by option	Input for the verify enable signal
3	VSS	—	—	Negative power supply (GND)	Negative power supply (GND)
4	VPP	—	—	No used.	Positive power supply (12.5V) and programming mode enable signal
5~8	KEY1~KEY4	I	Pull-High	Trigger key, low active. Programmable for retrigger or non-retrigger	No used.
11~13	KEY5~KEY7	I			
9,10	NC	—	—	No connection	No connection
12	KEY8/PGMB	I	Pull-High	Trigger key, low active. Programmable for retrigger or non-retrigger	Input for the programming enable signal, active low
13	DATA	I/O	—	No used.	Programming and verifying data I/O pin
14	VDD	—	—	Positive power supply	System positive power supply (5V)
15	AUD/DCLK	I/O	PMOS Open Drain	Voice output for driving the external transistor	Clock input for the serial data input/output
16	OSC2	O	—	Oscillator output pin	No used.

Absolute Maximum Ratings*

Supply Voltage ..... –0.3V to 6V

Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3

Storage Temperature ..... –50°C to 125°C

Operating Temperature ..... –25°C to 70°C

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extened periods may affect device reliability.

Electrical Characteristics

D.C. electrical characteristics

(Ta=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	3.5	—	5.0	V
V_{pp}	Programming Operation Voltage	—	—	12.2	12.5	12.8	V
I_{OP}	Operating Current	5V	F_{OSC}=96kHz No load, play mode	—	500	800	μA
I_{STB}	Standby Current	5V	—	—	1	5	μA
I_O	Max. AUD Output Current	5V	V_{OH}=0.6V	–2	–4	—	mA
I_{OL}	FLAG Sink Current	5V	V_{OL}=0.5V	2	4	—	mA
V_{IH}	"H" Input Voltage	—	—	$0.8V_{DD}$	—	—	V
V_{IL}	"L" Input Voltage	—	—	—	—	$0.2V_{DD}$	V
F_{OSC}	System Frequency	5V	R_{OSC}=480kΩ	76	96	116	kHz
F_{SR}	Sampling Rate	5V	F_{OSC}=96kHz	—	6	—	kHz

A.C. electrical characteristics

(Ta=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Type
		V_{DD}	Conditions				
t_{VPS}	VPP Setup Time	5V	—	2	—	—	μs
t_{DS}	Data Setup Time	5V	—	2	—	—	μs
t_{CLK}	Address Clock Pulse Width	5V	—	10	—	—	μs
t_{DH}	Data Hold Time	5V	—	2	—	—	μs
t_{PW}	Program Pulse Width	5V	—	500	700	—	μs
t_{AS}	ACLK Setup Time	5V	—	2	—	—	μs
t_{VFS}	VFB Setup Time	5V	—	2	—	—	μs
t_{VF}	VFB to Output Delay	5V	—	—	—	2	μs
t_{CS}	Address Clock Setup Time	5V	—	2	—	—	μs
t_{DCLK}	Data Clock Pulse Width	5V	—	2	—	—	μs
t_{VFD}	Delay between VFB & DCLK	5V	—	2	—	—	μs
t_{CH}	Output Hold from DCLK Change	5V	—	20	—	—	ns
t_{HZ}	VFB to Output High Z Time	5V	—	—	—	50	ns

Functional Description

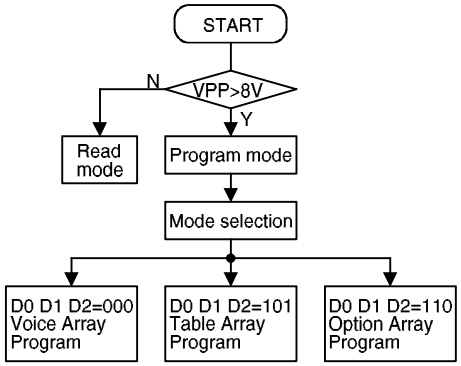
The HT81R30 is a voice synthesis LSI with a built-in EPROM. The customer's voice data can be recorded and programmed through HOLTEK's development system. The programmed voice data and option code can be written into the HT81R30 through the HOLTEK EPROM writer. The option code includes the trigger function, key debounce time, key pull-high resistor and FLAG output.

Program mode

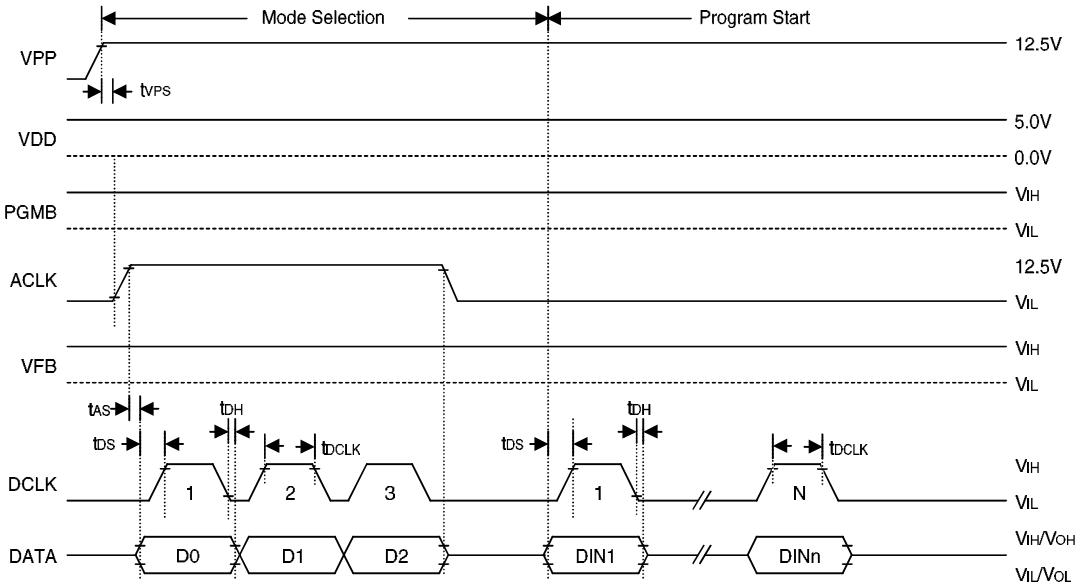
- Program flowchart

  When the input voltage of V_{PP} is greater than 8V, the HT81R30 goes into the program mode immediately. For a complete programming, the three group of codes, namely Voice Array, Table Array and Option Array, are required to be written into the internal EPROM of the HT81R30. A check word should be issued before entering an Array. The Voice Array is the default array. Following is a table for the check word of each Array.

Array	Check Word		
	D0	D1	D2
Voice Array	0	0	0
Table Array	1	0	1
Option Array	1	1	0



As for the Timing of the Write Check Word, it is listed below:

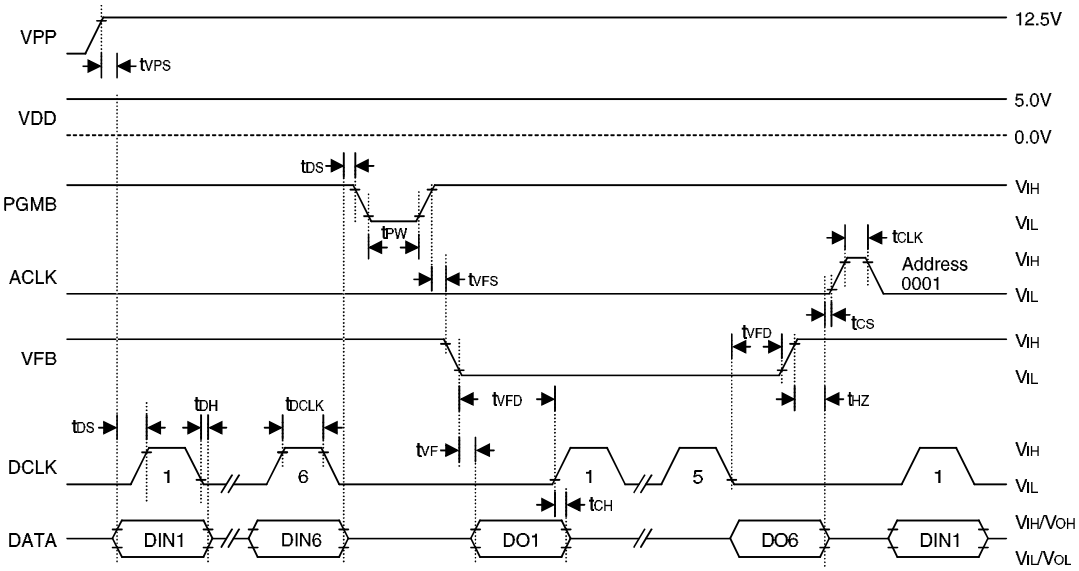


Program flowchart

- Voice Array program

  Voice Array is the place where voice codes are saved. The available length of the array varies with the simulated body of the Mask ROM type. Each voice code is of 6 bits in length. The first code begins with the initial address (0000H) of Voice Array. For the first code, no Address Clock (ACLK) is required. In addition, the address will be automatically increased with the ACLK pulse and the voice data will be programmed with the DCLK. The voice data is clocked into the device buffer serially at the fallening edge of the DCLK signal when the VFB is high. The 6 bits voice code will be writen in the voice array at the fallening edge of the PGMB signal.

  The writen-in data is clocked out of the device serially at the fallening edge of the DCLK signal when the VFB is low. The first bit is output at the VFB fallening edge without the DCLK pulse.



Voice array program

- Table Array program

  Table Array is the starting address of each section in the key groups. The starting address points out the position of Voice Array. The Timing is illustrated below.

- Option Array program

  Option Array is the position for saving the key definition, such as trigger mode, debounce time, pull-high, the FLAG output, etc., and for saving the corresponding address of Table Array of each key. The key definition includes the following, all of which must be set up before code writing:

  - Key trigger mode: Retrigger/Non-retrigger
  - Key debounce time: 700μs/22ms/180ms
  - KEY1 group size: 0/4/8/16 sections
  - Key pull-high resistor: 200kΩ/100kΩ/ 50kΩ/20kΩ
  - FLAG output: 3Hz flash/End-pulse/Busy

  As for the timing of Option Array, it is shown in the following.

Read Mode

All of the functions, except the value of oscillation resistor, are compatible with the IC of the Mask ROM type the moment the HT81R30 finishes writing.

The HT81R30 returns to the Read mode when

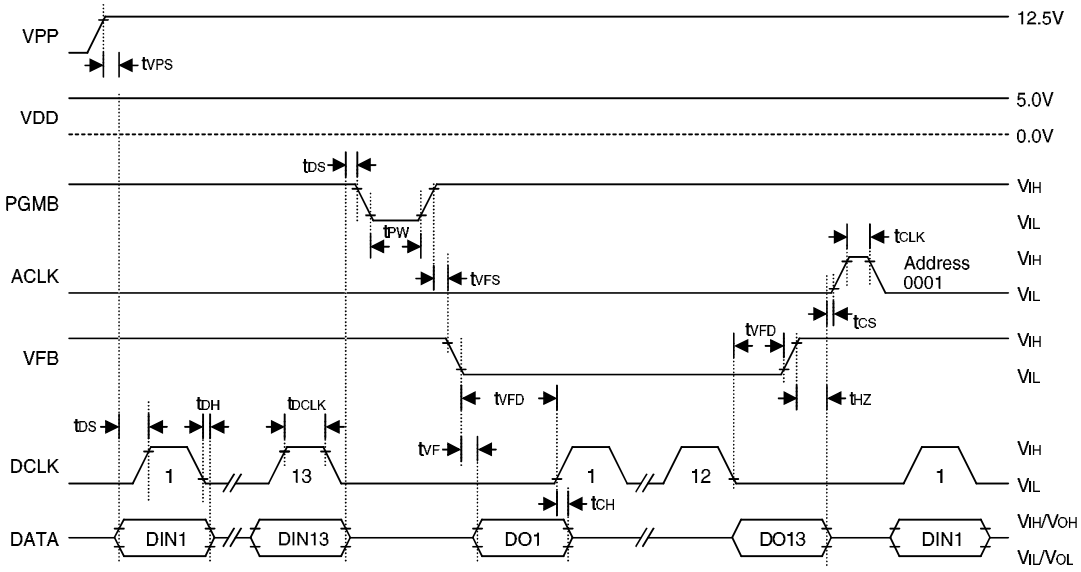
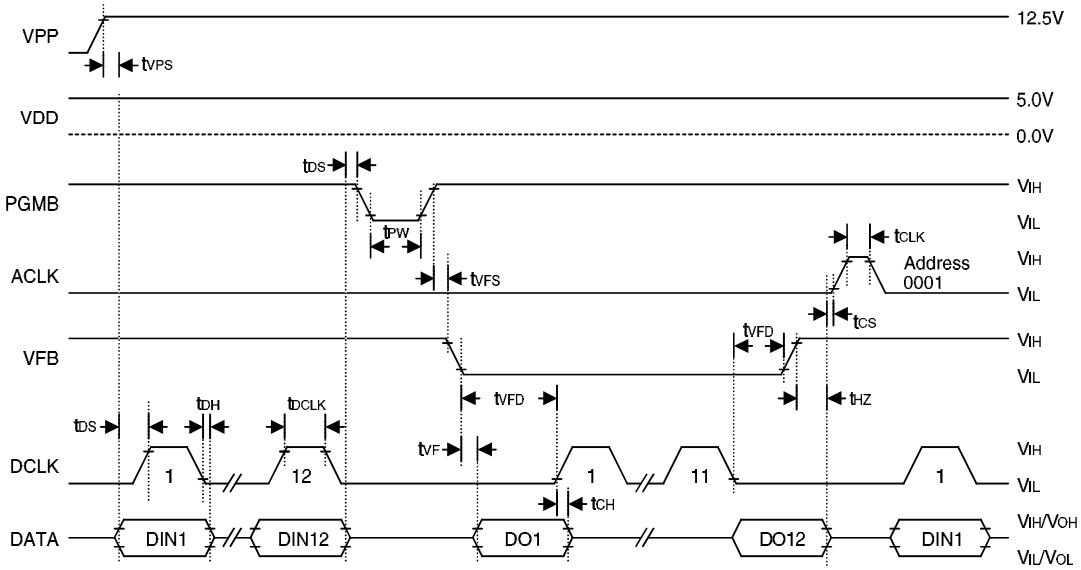


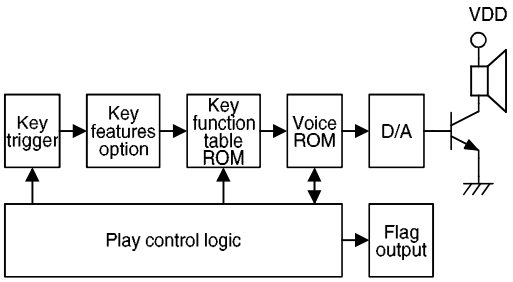
Table array program



Option array program

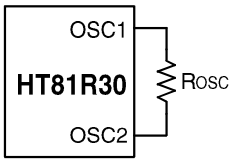
the input voltage of V_{PP} is lower than 8V. At this time, the HT81R30 is equal to an IC of the Mask ROM type. However, the HT81R30, after being written, can be used as the optioned Body without changing any mask layer.

Play function block diagram



System oscillator

The HT81R30 is built with an RC oscillator which requires only an exteranl resistor for normal applications. The oscillator frequency is typically 96kHz for an exteranl resistor of 480KΩ. Nonetheless, the value of the oscillator frequency may vary with different sampling rates in voice programmming. As a result, the values of the oscillator resistance may also be altered for different items.



The oscillator is turned on when triggered by a key input. It after playing is turned off and the chip goes into the standby state.

Voice ROM

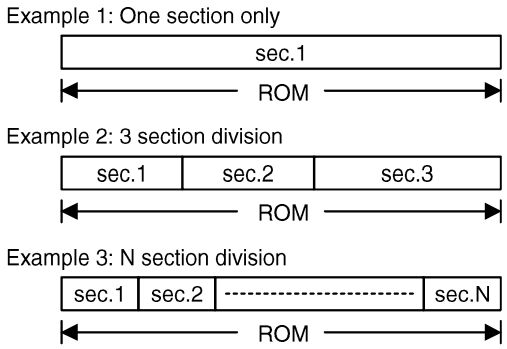
The voice ROM is designed originally for continuously recording the 5.6-second voice capacity at about 6kHz sampling rate. A higher sampling rate generates good voice play back quality but shortens the total recording time. On the other hand, a lower sampling rate will result in longer recording time but sacrifies the voice quality.

By taking the advantages such as coding efficiency, silence play, section repeat and section cascade, the play back time can be significantly extented.

Section

Section is the basic element of the contents of the voice ROM. During programming, the customer's voice sources can be divided into as many sections as required. A section can be composed of a voice or an interval of silence. However, the silene length will not be counted in the voice ROM. The entire number of sections included should be less than 252 due to the space limitation of the function table ROM. As for the total length of sections contained, it is limited by the voice ROM.

A section when triggered by a key input can be played one time, repeated or cascaded with other sections according to the instructions of the key function table. Following is some examples of the section division:



Group

The HT81R30 plays groups according to the key input. Each group can be made up of one or more sections. When a key is triggered, the corresponding group comes into play. For example, triggering KEY2 plays group 2, and so forth. The same section is allowed to appear in different groups. KEY1 can be made up of multiple groups when it is optioned as a sequential or random key. Otherwise, each key is comprised by one group exclusively.

Key function table

The sections included in the voice ROM are

played according to the instructions of the key funciton table. The function table contains group information and the playing order of sections contained in the groups. Notice that the entire number of the sections included in groups should be less than 252 due to the space limitation of the function table ROM.

- KEY1 as a direct key

  Each key is mapped to a group in the function table. If a certain key is not used, the group mapped to that key is a piece of silence. Following is an example illustrating the composition of the function table:

group 1	sec.1 + sec.2 + sec.3 + sec.5
group 2	sec.3
group 3	sec.2 + sec.2 + sec.3 + sec.4
group 4	sec.5 + sec.3

  The above example shows that the voice ROM is composed of 5 sections and the function table ROM of 11 sections. If KEY1 is momentarily triggered, section 1, section 2, section 3 and section 5 are played in sequence and then stopped. Triggering KEY2 plays section 3, and so forth.

- KEY1 as a sequential (random) key

  KEY1 is allowed to have multiple groups (subgropus) in the function table when it is optioned as a sequential or random key. The remaining 7 keys (KEY2~KEY8) are used as direct keys exclusively and are comprised by only one group in the funciton table. Below is such an example:

group 1-1	sec.4 + sec.2
group 1-2	sec.1 + sec.3
group 1-n	sec.2 + sec.3
group 2	sec.2 + sec.3
group 3	sec.3 + sec.5
group 4	sec.1 + sec.5 + sec.2

  KEY1 is composed of sub-groups. The according sub-groups come into play in sequence each time KEY1 is triggered.

  - The playing sequence of sequential KEY1

    group 1-1 → group 1-2 → group 1-3 ..... → group 1-N (the last group) → group 1-1 .....

  - The playing sequence of random KEY1

    group 1-3 → group 1-5 ..... → group 1- M (the last group) → group 1-3 → group 1-5 .....

    The random key is actually a special case of the sequential key with a particular arrangement of the sub-group playing sequence.

  - Reset of the KEY1 playing sequence

    KEY2~KEY7 function as a reset key when any subgroup of KEY1 is played. For example, if a certain subgroup of KEY1 is played and one of KEY2~KEY7 is triggered the KEY1 subgroups will return to the first subgroup. At this time, the first subgroup of KEY1 will start playing if KEY1 is retriggered (refer to Figure 1).

  - Sub-group selection

    A sub-group of the KEY1 group can be selected to play by directly controlling the pulse number of KEY1 when the features of KEY1 are set in the following way:

    - sequential or random
    - retriggerable
    - minimum key debounce time
      (≅700μs, f_{OSC}=96kHz)

    For instance, if sub-group 1-3 is the previous playing group, sub-group 1-5 will start playing when 2 pulses are input to KEY1, and so on.

    Nevertheless, if the total number of the subgroups included is only 4 (for example), subgroup 1-1 will be played under the same input condition.

    To make the selection of the KEY1 sub-groups more easily, a key of KEY2~KEY7 can be programmed as silence, and this silence key should be triggered prior to the KEY1 trigger pulses. By so doing, the sub-group to be played is directly specified by the pulse number of KEY1 (refer to Figure 2).

- KEY1 as a repeat key

  When KEY1 is optioned as a repeat key, the

same group will be played repeatedly till other triggers are input. The retriggerable function is recommended when KEY1 is set as a repeat key.

Key features

- Key priority

  The key priority is set as follows:

  KEY1>KEY2>.....KEY7>KEY8

  If two or more keys are triggered at the same time, the output is decided by the key priority.

- Key debounce

  There are 3 kinds of key-in debounce time selectable by mask option: 700μs, 22ms and 110ms

- Pull-high resistance

  There are four kinds of key input pin pull-high resistance selectable by mask option: 20kΩ, 50kΩ, 100kΩ, 200kΩ

- Trigger mode

  All of the 8 keys are set as one shot trigger mode internally.

- Trigger function

  Non-retriggerable/retriggerable options

  - Non-retriggerable

    Any new trigger input is ignored until the currently playing group is finished playing.

  - Retriggerable

    The currently playing group is stopped immediately when a new key trigger is input.

FLAG

When playing voices, the FLAG pin is activated to output one of the following signals through code option:

- End pulse output

  The FLAG pin outputs an active low pulse when a voice output is completed. The pulse width is programmable depending on the customer's requirements (default: 2ms, 90ms, 360ms). The minimal pulse width is 330μs when the sampling rate is 6kHz.

- 3Hz flash

  The FLAG pin outputs a 3Hz signal to drive an LED when voices are playing. The signal is active low, 25% duty. Once the voice output is terminated, the FLAG pin is set to floating.

- Busy output

  The FLAG output is turned low to indicate that the chip is busy when voices are playing.

  On the other hand, the FLAG pin is set to floating when the chip is in the standby state.

AUD

The AUD pin is a PMOS open drain structure. It outputs voice signals to drive the speaker through an external NPN transistor when the chip is active. However, the AUD pin is floating when the chip is in the standby state.

The 8050 type transistor with $h_{FE} \cong 150$ is recommended as an output driver.

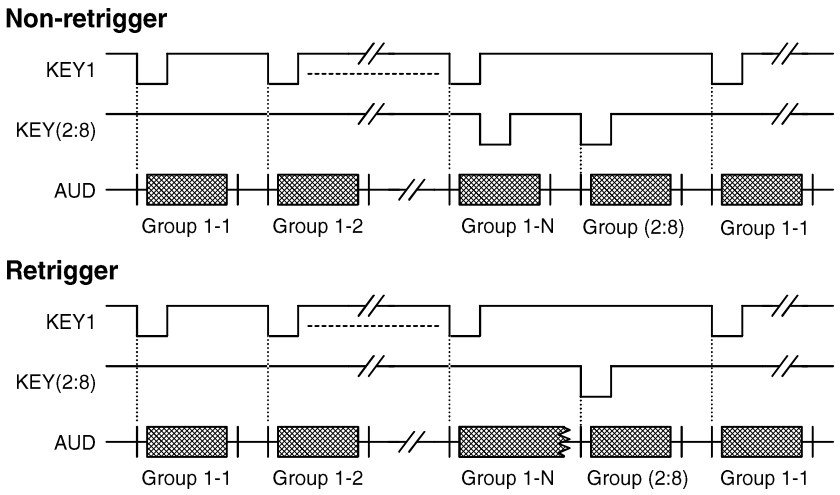


Figure 1

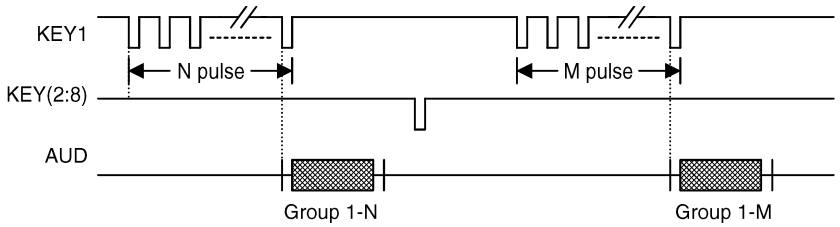
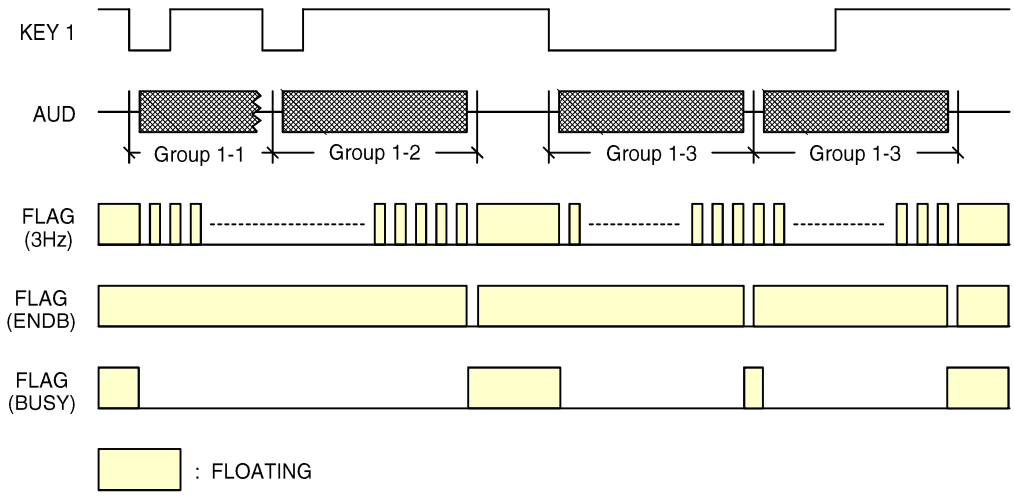


Figure 2

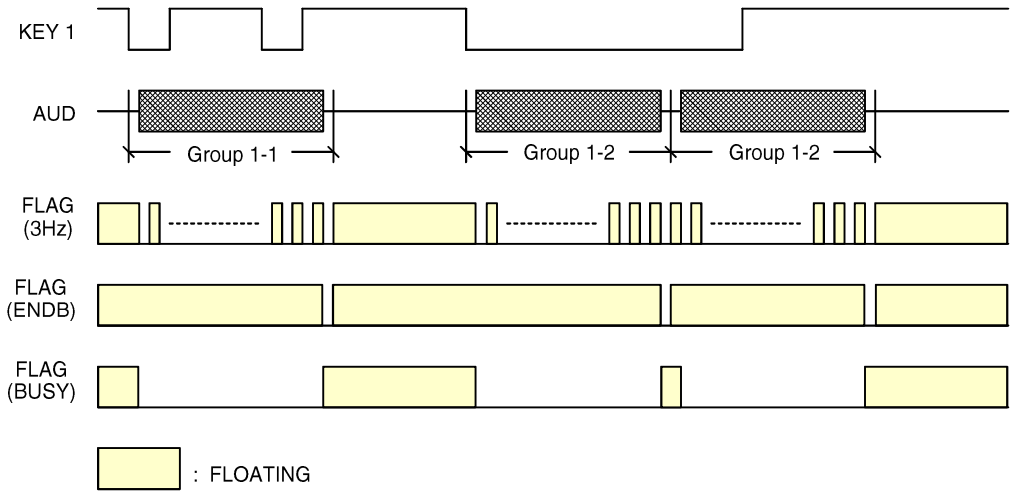
Timing Diagram

One key operation

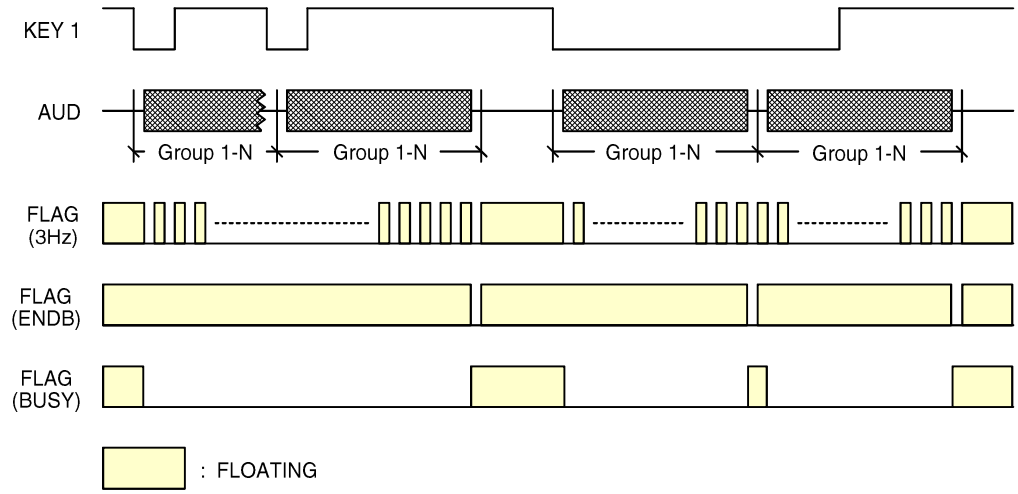
- Sequential-retriggerable



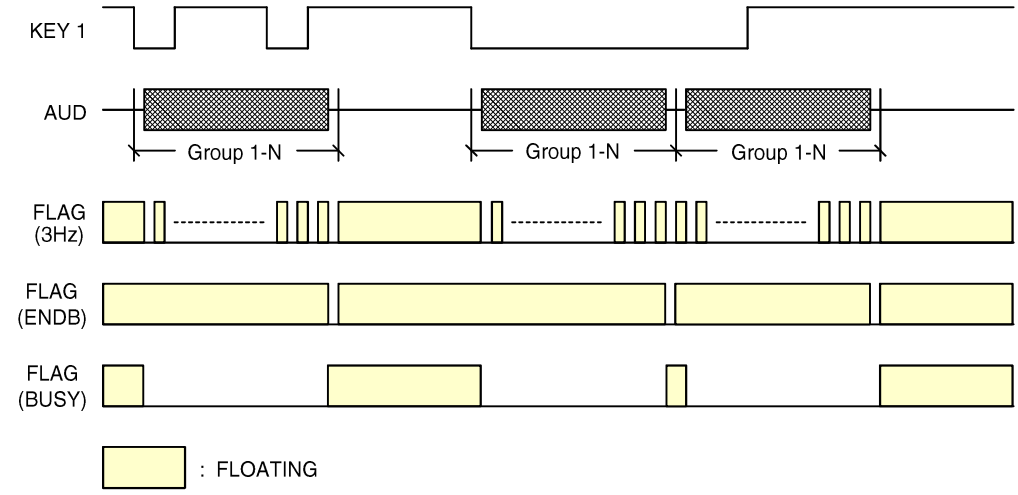
- Sequential-nonretriggerable



• Random-retriggerable



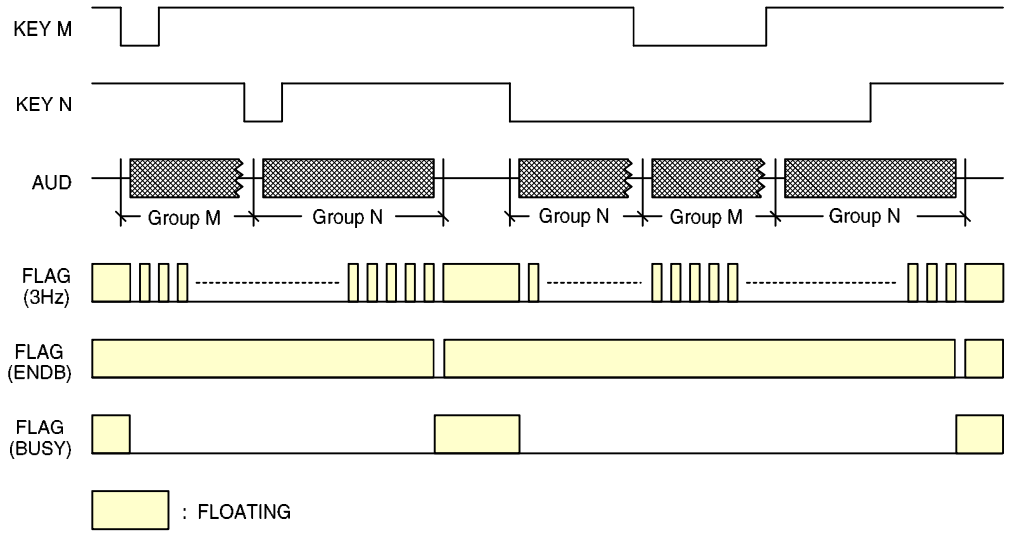
• Random-nonretriggerable



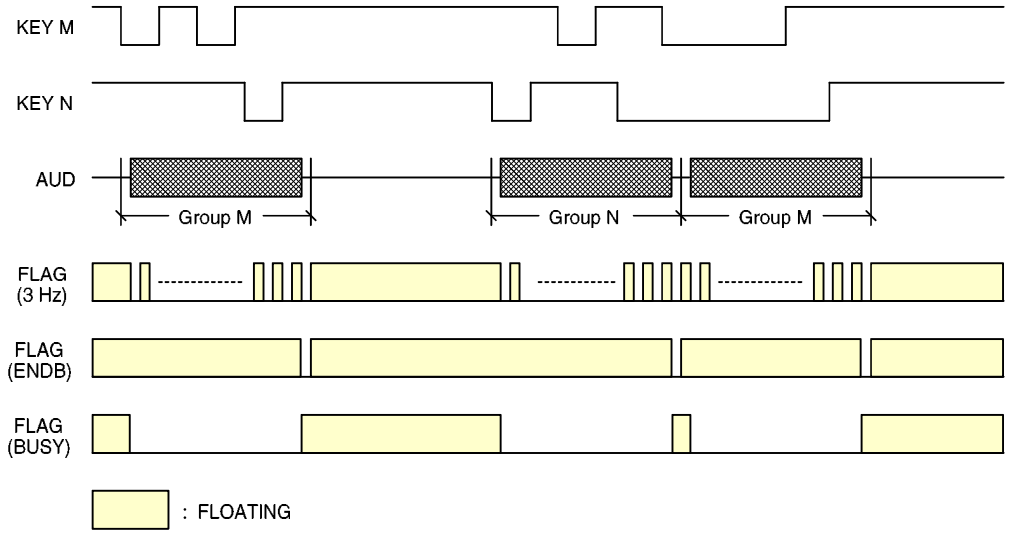
Note: Group 1-N may be any one of the groups.

Multi key operation

- Retriggerable

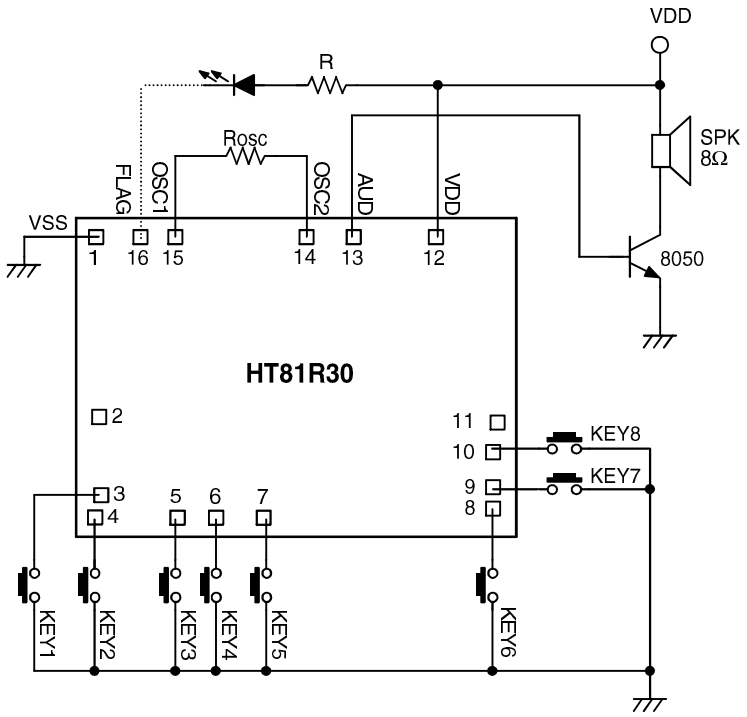


- Nonretriggerable



Note: The key priority: Key M > Key N.

Application Circuit



* The IC substrate should be connected to VSS in the PCB layout artwork.