4 Signals and DC Characteristics

4.1 Terminology

The input and output types have all been abbreviated with a letter code. For example, the VDATA31-00 signals are shown as input type CTTL (which are CMOS inputs with normal TTL voltage thresholds) and output type TS (which are tri-stateable outputs). The following is a list of abbreviations:

CMOS	CMOS input with CMOS thresholds
CMOS SCH	Schmitt trigger input with CMOS thresholds
CTTL SCH	Schmitt trigger input with TTL thresholds
CTTL	CMOS input with TTL thresholds
I	Input
I/O	Input/Output
O	Output
OD	Open drain output
TP	Totem pole output
TS	Tri-state totem pole output
VOD	VMEbus specification open drain output
VTS	VMEbus specification tri-state totem pole output

4.2 DC Characteristics

Table 4.1 : DC Electrical Characteristics

Symbol	Parameter	Signal Type	Test Conditions	Tested at -40°C, 25°C, 85°C V_{DD} = 5V±5%		Tested at -55°C, 125°C V_{DD} = 5V±10%	
				Min	Max	Min	Max
V_{IH}	Min. high-level input	CTTL	V_{OUT} = 0.1V or V_{DD} - 0.1V; $\lvert I_{OUT}\rvert$ = 20 µA	2.0 V	-	2.0 V	-
		CMOS	V_{OUT} = 0.1V or V_{DD} - 0.1V; $\lvert I_{OUT}\rvert$ = 20 µA	$0.7V_{DD}$	-	$0.7V_{DD}$	-
V_{IL}	Max. low-level input	CTTL	V_{OUT} = 0.1V or V_{DD} - 0.1V; $\lvert I_{OUT}\rvert$ = 20 µA	-	0.8V	-	0.8V
		CMOS	V_{OUT} = 0.1V or V_{DD} - 0.1V; $\lvert I_{OUT}\rvert$ = 20 µA	-	$0.3V_{DD}$	-	$0.3V_{DD}$
V_{T+}	Positive going Schmitt trigger voltage	CTTL/SCH	V_{OUT} = 0.1V or V_{DD} - 0.1V; $\lvert I_{OUT}\rvert$ = 20 µA	1.2 V	2.4 V	1.2 V	2.4 V
		CMOS/SCH	V_{OUT} = 0.1V or V_{DD} - 0.1V; $\lvert I_{OUT}\rvert$ = 20 µA	$0.42V_{DD}$	$0.94V_{DD}$	$0.4V_{DD}$	$1.03V_{DD}$
V_{T-}	Negative going Schmitt trigger voltage	CTTL/SCH	V_{OUT} = 0.1V or V_{DD} - 0.1V; $\lvert I_{OUT}\rvert$ = 20 µA	0.8 V	2.0 V	0.8 V	2.0 V
		CMOS/SCH	V_{OUT} = 0.1V or V_{DD} - 0.1V; $\lvert I_{OUT}\rvert$ = 20 µA	$0.31V_{DD}$	$0.69V_{DD}$	$0.29\ V_{DD}$	$0.76\ V_{DD}$
$V_{Hysteresis}$	Schmitt trigger hysteresis voltage	CTTL/SCH	V_{T+} to V_{T-}	$0.06V_{DD}$	$0.12V_{DD}$	$0.05\ V_{DD}$	$0.14\ V_{DD}$
		CMOS/SCH	V_{T+} to V_{T-}	$0.11V_{DD}$	$0.25V_{DD}$	$0.11\ V_{DD}$	$0.27\ V_{DD}$
I_{IN}	Maximum input leakage current	CMOS and CTTL	With no pull-up resistor (V_{IN} = V_{SS} or V_{DD})	-5.0 µA	5.0 µA	-5.0 µA	5.0 µA
I_{OZ}	Maximum output leakage current	TS	(V_{OUT} = V_{SS} or V_{DD})	-10.0 µA	10.0 µA	-10.0 µA	10.0 µA
		OD	(V_{OUT} = V_{DD})	-10.0 µA	10.0 µA	-10.0 µA	10.0 µA

Table 4.2 : Pin List and DC Characteristics for SCV64 Signals (-55°C to 125°C)

Signal Name	Type	Pin Number		In Type	Out Type	I_{OL} (mA) V_{OL}=0.4, * 0.6 V Min	I_{OH} (mA) V_{OH}=3.5V Min	Signal Description
		CPGA	PQFP					
BAUDCLK	O	E4	88	-	TP	10	-10	Baud clock
BBSY*	I/O	C20	295	CTTL/ SCH	V0D	48*	-	VMEbus BBSY* signal
BCLR*	I/O	N17	252	CTTL/ SCH	VTS	64*	-50	VMEbus BCLR* signal
BERR*	I/O	E19	291	CTTL/ SCH	VOD	48*	-	VMEbus error
BG0IN*	I	P19	251	CTTL	-	-	-	VMEbus bus grant in
BG1IN*	I	N19	253	CTTL	-	-	-	VMEbus bus grant in
BG2IN*	I	L19	262	CTTL	-	-	-	VMEbus bus grant in
BG3IN*	I	L17	264	CTTL	-	-	-	VMEbus bus grant in
BG0OUT*	O	U9	182	-	TP	10	-10	VMEbus bus grant out
BG1OUT*	O	T9	183	-	TP	10	-10	VMEbus bus grant out
BG2OUT*	O	V9	184	-	TP	10	-10	VMEbus bus grant out
BG3OUT*	O	W10	186	-	TP	10	-10	VMEbus bus grant out
BIMODE	O	D2	87	-	TP	10	-10	Bi-Mode output
$\overline{\text{BIREL}}$	I	A13	25	CTTL/ SCH	-	-	-	Bi-Mode release
$\overline{\text{BITRIG}}$	I	D11	36	CTTL/ SCH	-	-	-	Bi-Mode trigger
BR0*	I/O	D13	24	CTTL/ SCH	VOD	48*	-	VMEbus bus request
BR1*	I/O	B12	35	CTTL/ SCH	VOD	48*	-	VMEbus bus request
BR2*	I/O	D8	54	CTTL/ SCH	VOD	48*	-	VMEbus bus request
BR3*	I/O	B17	11	CTTL/ SCH	VOD	48*	-	VMEbus bus request
C14US	O	D7	58	-	TP	10	-10	Clock out - 14us period
C32MHZ	I	L3	114	CMOS	-	-	-	32MHz clock input
C8MHZ	O	L4	116	-	TP	10	-10	Clock output - 8MHz
DTACK*	I/O	N20	255	CTTL/ SCH	VOD	48*	-	VMEbus DTACK* signal
$\overline{\text{EXTRST}}$	I	D6	64	CTTL/ SCH	-	-	-	External reset
IACK*	I/O	U19	239	CTTL	VTS	48*	-40	VMEbus IACK* signal
IACKI*	I	N18	254	CTTL	-	-	-	VMEbus IACKIN* signal
IACKO*	O	W19	233	-	TP	10	-10	VMEbus IACKOUT* signal

Table 4.2 : Pin List and DC Characteristics for SCV64 Signals (-55°C to 125°C) (Continued)

Signal Name	Type	Pin Number		In Type	Out Type	I_{OL} (mA) V_{OL}=0.4, * 0.6 V Min	I_{OH} (mA) V_{OH}=3.5V Min	Signal Description
		CPGA	PQFP					
IRQ1*	I/O	W4	163	CTTL/ SCH	VOD	48*	-	VMEbus interrupt request
IRQ2*	I/O	W6	167	CTTL/ SCH	VOD	48*	-	VMEbus interrupt request
IRQ3*	I/O	U8	176	CTTL/ SCH	VOD	48*	-	VMEbus interrupt request
IRQ4*	I/O	W11	195	CTTL/ SCH	VOD	48*	-	VMEbus interrupt request
IRQ5*	I/O	V14	206	CTTL/ SCH	VOD	48*	-	VMEbus interrupt request
IRQ6*	I/O	W15	215	CTTL/ SCH	VOD	48*	-	VMEbus interrupt request
IRQ7*	I/O	Y18	219	CTTL/ SCH	VOD	48*	-	VMEbus interrupt request
JTCLK	I	J1	119	CTTL	-	-	-	JTAG test clock
JTDI	I	K4	110	CTTL	-	-	-	JTAG test data
JTDO	O	J5	111	-	TS	10	-10	JTAG test data
JTMS	I	M3	120	CTTL	-	-	-	JTAG test mode select
KADDR (31:0)	I/O	See Table 4.4	See Table 4.4	CTTL	TS	5	-5	CPU address bus
$\overline{\text{KAS}}$	I/O	K2	112	CTTL	TS	10	-10	CPU address strobe
$\overline{\text{KAVEC}}$	O	C5	70	-	TP	5	-5	AVEC interrupt termination
$\overline{\text{KBERR}}$	I/O	A3	69	CTTL	TS	10	-10	CPU bus error
$\overline{\text{KBGACK}}$	I/O	B4	67	CTTL/ SCH	OD	10	-	CPU bus grant acknowledge
$\overline{\text{KBGR}}$	I	B8	55	CTTL	-	-	-	CPU bus grant
$\overline{\text{KBRQ}}$	O	B9	53	-	TP	5	-5	CPU bus request
KCLK	I	K3	108	CMOS	-	-	-	CPU clock
KDATA (31:0)	I/O	See Table 4.4	See Table 4.4	CTTL	TS	5	-5	CPU data bus
$\overline{\text{KDS}}$	I/O	C8	52	CTTL	TS	5	-5	CPU data strobe
$\overline{\text{KDSACK0}}$	I/O	E10	47	CTTL	TS	10	-10	CPU data transfer and size acknowledge
$\overline{\text{KDSACK1}}$	I/O	D9	48	CTTL	TS	10	-10	CPU data transfer and size acknowledge
KFC0	I/O	C10	40	CTTL	TS	5	-5	CPU function code
KFC1	I/O	A11	41	CTTL	TS	5	-5	CPU function code
KFC2	I/O	D10	42	CTTL	TS	5	-5	CPU function code
$\overline{\text{KHALT}}$	I/O	A10	43	CTTL	TS	10	-10	CPU halt

Table 4.2 : Pin List and DC Characteristics for SCV64 Signals (-55°C to 125°C) (Continued)

Signal Name	Type	Pin Number		In Type	Out Type	I_{OL} (mA) V_{OL}=0.4, * 0.6 V Min	I_{OH} (mA) V_{OH}=3.5V Min	Signal Description
		CPGA	PQFP					
$\overline{\text{LIRQ2}}$ / $\overline{\text{KIACK}}$	I	W8	175	CTTL	-	-	-	Local interrupt acknowledge
$\overline{\text{KIPL0}}$	O	R2	139	-	TP	5	-5	CPU interrupt priority level
$\overline{\text{KIPL1}}$	O	R4	140	-	TP	5	-5	CPU interrupt priority level
$\overline{\text{KIPL2}}$	O	T2	141	-	TP	5	-5	CPU interrupt priority level
$\overline{\text{KRMC}}$	I/O	B10	44	CTTL	TS	2	-2	CPU RMC
KSIZE0	I/O	A12	37	CTTL	TS	5	-5	CPU transfer size code
KSIZE1	I/O	C11	38	CTTL	TS	5	-5	CPU transfer size code
$\overline{\text{KWR}}$	I/O	C9	46	CTTL	TS	10	-10	CPU write
$\overline{\text{L7IACF}}$	I	F17	292	CTTL	-	-	-	Level 7 interrupt (ACFAIL)
$\overline{\text{L7IMEM}}$	I	E18	294	CTTL	-	-	-	Level 7 interrupt (Memory error)
$\overline{\text{L7INMI}}$	I	C16	12	CTTL	-	-	-	Level 7 interrupt (non-maskable)
$\overline{\text{LBGR1}}$	O	B11	34	-	TP	5	-5	Local bus grant (external DMA)
$\overline{\text{LBRQ1}}$	I	V16	218	CTTL	-	-	-	Local bus request (external DMA)
$\overline{\text{LIACK4}}$	O	V7	174	-	TP	5	-5	Local interrupt acknowledge 4
$\overline{\text{LIACK5}}$	O	V8	178	-	TP	5	-5	Local interrupt acknowledge 5
$\overline{\text{LIRQ0}}$	I	V5	164	CTTL	-	-	-	Local interrupt
$\overline{\text{LIRQ1}}$	I	U6	166	CTTL	-	-	-	Local interrupt
$\overline{\text{LIRQ2}}$ / $\overline{\text{KIACK}}$	I	W8	175	CTTL	-	-	-	Local interrupt
$\overline{\text{LIRQ3}}$	I	U11	194	CTTL	-	-	-	Local interrupt
$\overline{\text{LIRQ4}}$	I	W12	205	CTTL	-	-	-	Local interrupt
$\overline{\text{LIRQ5}}$	I	U15	216	CTTL	-	-	-	Local interrupt
$\overline{\text{LMINT}}$	O	Y8	177	-	TP	2	-2	Location monitor interrupt
$\overline{\text{LRST}}$	O	U7	172	-	TP	20	-20	Local reset
$\overline{\text{PWRRST}}$	I	R17	240	CTTL/ SCH	-	-	-	Power-up reset
$\overline{\text{RAMSEL}}$	O	C13	26	-	TP	5	-5	Local memory select
RETRY*/ $\overline{\text{VRMC}}$	I/O	B6	63	CTTL/ SCH	TS	2	-2	VMEbus RETRY* (I), or VMEbus RMC signal (I/O)
$\overline{\text{SCV64SEL}}$	I	G19	283	CTTL	-	-	-	SCV64 chip select
SYSCLK	I/O	K16	263	CTTL	VTS	64*	-50	VMEbus SYSCLK

Table 4.2 : Pin List and DC Characteristics for SCV64 Signals (-55°C to 125°C) (Continued)

Signal Name	Type	Pin Number		In Type	Out Type	I_{OL} (mA) V_{OL}=0.4, * 0.6 V Min	I_{OH} (mA) V_{OH}=3.5V Min	Signal Description
		CPGA	PQFP					
SYSFAIL*	I/O	R18	242	CTTL/ SCH	VOD	48*	-	VMEbus SYSFAIL
$\overline{\text{SYSFLED}}$	O	C12	32	-	OD	24*	-	SYSFAIL LED driver
SYSRST*	I/O	H17	282	CTTL/ SCH	VOD	48*	-	VMEbus SYSRESET
$\overline{\text{TICK}}$	O	D12	30	-	TP	5	-5	Tick clock
TMODE0	I	J2	117	CMOS /SCH	-	-	-	Test mode enable connect to ground
TMODE1	I	L5	118	CMOS /SCH	-	-	-	Test mode enable connect to ground
VADDR (31:1)	I/O	See Table 4.3	See Table 4.3	CTTL	TS	2	-2	VMEbus address bus
VADDROUT	O	C14	22	-	TP	10	-10	VMEbus address direction control
VAM0	I/O	M17	258	CTTL	TS	2	-2	VMEbus address modifier 0
VAM1	I/O	M19	259	CTTL	TS	2	-2	VMEbus address modifier 1
VAM2	I/O	M18	260	CTTL	TS	2	-2	VMEbus address modifier 2
VAM3	I/O	L18	266	CTTL	TS	2	-2	VMEbus address modifier 3
VAM4	I/O	K18	268	CTTL	TS	2	-2	VMEbus address modifier 4
VAM5	I/O	L20	269	CTTL	TS	2	-2	VMEbus address modifier 5
$\overline{\text{VAS}}$	I/O	U18	235	CTTL/ SCH	TS	5	-5	VMEbus address strobe
VDATA (31:0)	I/O	See Table 4.3	See Table 4.3	CTTL	TS	2	-2	VMEbus data bus
VDATAOUT	O	D14	20	-	TP	10	-10	VMEbus data direction
$\overline{\text{VDS0}}$	I/O	V18	231	CTTL	TS	5	-5	VMEbus data strobe
$\overline{\text{VDS1}}$	I/O	U17	232	CTTL	TS	5	-5	VMEbus data strobe
$\overline{\text{VLWORD}}$	I/O	W9	187	CTTL	TS	2	-2	VMEbus LWORD* signal
$\overline{\text{VMEINT}}$	O	C15	18	-	TP	2	-2	VMEbus activity interrupt
$\overline{\text{VMEOUT}}$	I	V20	241	CTTL	-	-	-	VMEbus select
RETRY*/ $\overline{\text{VRMC}}$	I/O	B6	63	CTTL/ SCH	TS	2	-2	VMEbus RETRY* (I), or VMEbus RMC signal (I/O)
$\overline{\text{VSBSEL}}$	O	B13	23	-	TP	5	-5	VSBbus select
VSTRBOUT	O	B14	21	-	TP	5	-5	VMEbus strobe direction
$\overline{\text{VWR}}$	I/O	T17	234	CTTL	TS	2	-2	VMEbus WRITE* signal
$\overline{\text{WDOG}}$	O	E12	31	-	TP	5	-5	Watchdog interrupt output

Table 4.3 : VMEbus Address and Data Input and Output Signal Bits

Signal	CPGA Pin	PQFP Pin	Signal	CPGA Pin	PQFP Pin
VADDR1	U10	188	VDATA0	K17	270
VADDR2	Y10	189	VDATA1	K19	271
VADDR3	V10	190	VDATA2	J18	272
VADDR4	V11	192	VDATA3	J17	274
VADDR5	Y11	193	VDATA4	K20	275
VADDR6	V12	196	VDATA5	J16	276
VADDR7	U12	198	VDATA6	J19	279
VADDR8	T11	199	VDATA7	H18	280
VADDR9	V13	200	VDATA8	H19	281
VADDR10	U13	204	VDATA9	G18	284
VADDR11	W13	207	VDATA10	F20	285
VADDR12	T13	208	VDATA11	G17	286
VADDR13	W14	209	VDATA12	F18	288
VADDR14	U14	210	VDATA13	F19	289
VADDR15	V15	212	VDATA14	D19	293
VADDR16	Y15	213	VDATA15	C19	297
VADDR17	W16	217	VDATA16	F16	298
VADDR18	W17	221	VDATA17	D18	299
VADDR19	T15	222	VDATA18	E17	300
VADDR20	W18	223	VDATA19	C18	301
VADDR21	U16	224	VDATA20	E16	302
VADDR22	V17	225	VDATA21	B19	3
VADDR23	T16	226	VDATA22	D17	4
VADDR24	T18	236	VDATA23	B18	5
VADDR25	V19	237	VDATA24	E15	6
VADDR26	T19	243	VDATA25	C17	7
VADDR27	R19	245	VDATA26	D16	8
VADDR28	P17	246	VDATA27	A18	9
VADDR29	N16	248	VDATA28	B16	13
VADDR30	R20	249	VDATA29	D15	14
VADDR31	P18	250	VDATA30	B15	15
			VDATA31	A15	17

Table 4.4 : Local Bus Address and Data Input and Output Signal Bits

Signal	CPGA Pin	PQFP Pin	Signal	CPGA Pin	PQFP Pin
KADDR0	C7	56	KDATA0	M4	122
KADDR1	B7	57	KDATA1	L2	123
KADDR2	C6	60	KDATA2	N3	124
KADDR3	A6	61	KDATA3	L1	127
KADDR4	B5	65	KDATA4	N4	128
KADDR5	E7	66	KDATA5	M2	129
KADDR6	C4	71	KDATA6	P3	130
KADDR7	D5	72	KDATA7	N2	131
KADDR8	B3	73	KDATA8	N5	132
KADDR9	C3	74	KDATA9	P2	133
KADDR10	B2	79	KDATA10	P4	134
KADDR11	E5	80	KDATA11	R3	136
KADDR12	C2	81	KDATA12	R1	137
KADDR13	D4	82	KDATA13	T3	142
KADDR14	D3	83	KDATA14	U2	143
KADDR15	F5	84	KDATA15	V1	145
KADDR16	C1	85	KDATA16	T4	146
KADDR17	E3	89	KDATA17	V2	147
KADDR18	F4	90	KDATA18	U3	148
KADDR19	E2	91	KDATA19	W2	149
KADDR20	F3	93	KDATA20	T5	150
KADDR21	G4	94	KDATA21	V3	155
KADDR22	G3	96	KDATA22	U4	156
KADDR23	F2	97	KDATA23	W3	157
KADDR24	H4	98	KDATA24	T6	158
KADDR25	F1	99	KDATA25	V4	159
KADDR26	H3	100	KDATA26	U5	160
KADDR27	G2	101	KDATA27	Y3	161
KADDR28	J4	102	KDATA28	W5	165
KADDR29	H2	103	KDATA29	Y6	169
KADDR30	J3	106	KDATA30	V6	170
KADDR31	H1	107	KDATA 31	W7	173

Table 4.5 : Pin Assignments for Ground

V_{SS} Pins					
CPGA			PQFP		
A2	A4	A7	76	68	59
A9	A14	A17	50	45	39
A19	B1	B20	33	28	19
D1	D20	E8	10	1	304
E11	E14	G1	296	287	278
G5	G16	G20	273	267	261
J20	K1	K5	256	247	238
L16	M1	P1	229	228	220
P5	P16	P20	211	202	197
T7	T10	T14	191	185	180
U1	U20	W1	171	162	153
W20	Y2	Y4	152	144	135
Y7	Y12	Y14	126	121	115
Y17	Y19		109	104	95
			86	77	

Table 4.6 : Pin Assignments for Power

V_{DD} Pins					
CPGA			PQFP		
A1	A5	A8	75	62	51
A16	A20	E1	49	29	27
E9	E13	E20	16	2	303
H5	H16	H20	290	277	265
M5	M16	M20	257	244	230
N1	R5	R16	227	214	203
T1	T8	T12	201	181	179
T20	Y1	Y5	168	154	151
Y9	Y13	Y16	138	125	113
Y20			105	92	78

4.3 Capacitive Loading

Table 4.7 : Input Capacitive Loading

Signal Type	Signal Name	Input Capacitance (pF)
Input	BGIN[3:0], BIREL, BITRIG, C32MHZ, EXTRST, JTCLK, JTDI, JTMS, KBGR, KCLK, L7IACF, L7IMEM, L7INMI, LBRQ, LIRQ[5:0], PWRRST, TMODE[1:0], IACKIN, VMEOUT	18
Input/Output	IACK, KADDR[31:0], KAS, KBERR, KDATA[31:0], KDS, KDSACK[1:0], KFC[2:0], KHALT, KSIZE[1:0], KWR, KRMC, $\overline{\text{SCV64SEL}}$, VADDR[31:1], VAM[5:0], VAS, VDATA[31:0], VDS[1:0], VLWORD, VRETRY, VWR	18
	BBSY, BR[3:0], BERR, DTACK, IRQ[7:1], SYSFAIL, SYSRST	24
	BCLR, SYSCLK	30
Output	JTDO	18

4.4 Pin Configuration

The 299-pin CPGA configuration is shown here in Figure 4.1 while the 304 pin PQFP package is illustrated in Figure 4.2.

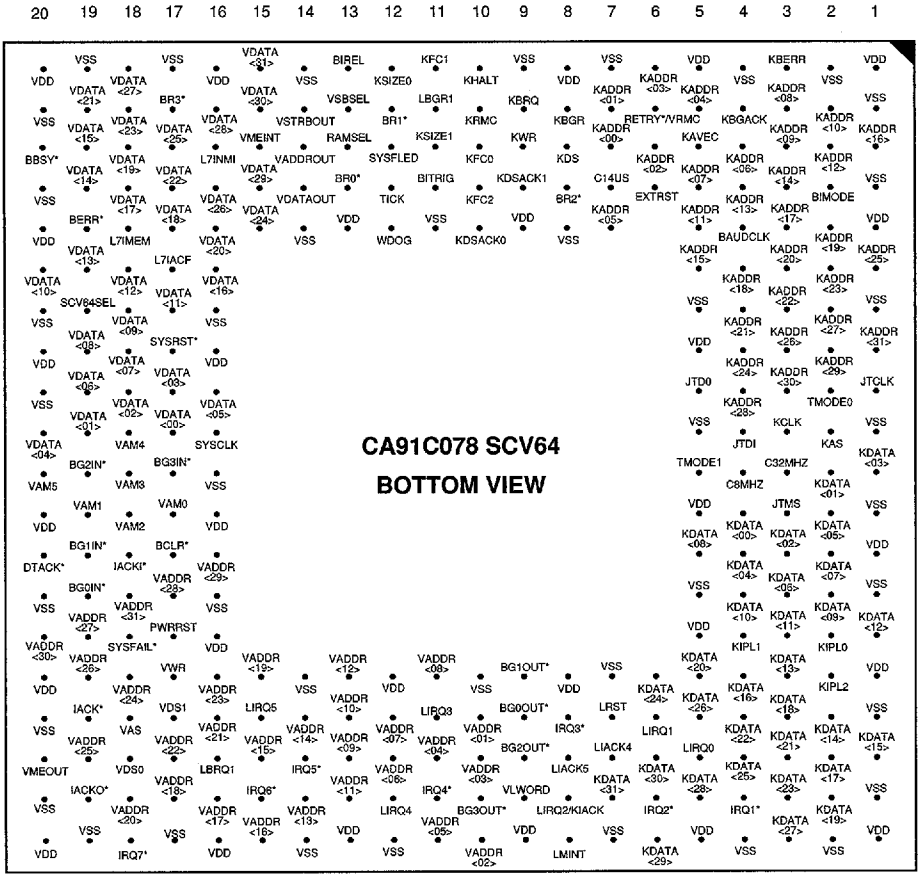


Figure 4.1 : Pin Configuration for 299-Pin CPGA Package

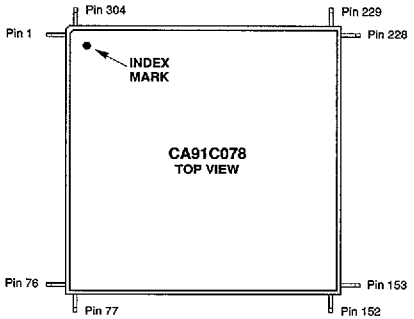


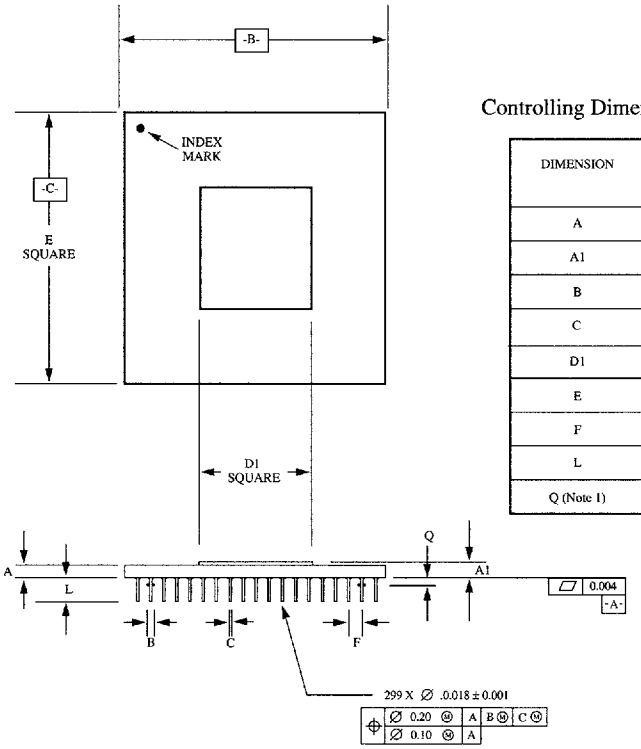
Figure 4.2 : Pin Configuration for 304-Pin PQFP Package

304 PIN PLASTIC QFP

1. V_{SS}	39. V_{SS}	77. V_{SS}	115. V_{SS}	153. V_{SS}	191. V_{SS}	229. V_{SS}	267. V_{SS}
2. V_{DD}	40. KFC0	78. V_{DD}	116. C8MHZ	154. V_{DD}	192. VADDR4	230. V_{DD}	268. VAM4
3. VDATA21	41. KFC1	79. KADDR10	117. TMODE0	155. KDATA21	193. VADDR5	231. $\overline{VDS0}$	269. VAM5
4. VDATA22	42. KFC2	80. KADDR11	118. TMODE1	156. KDATA22	194. $\overline{LIRQ3}$	232. $\overline{VDS1}$	270. VDATA0
5. VDATA23	43. $\overline{KHALT}$	81. KADDR12	119. JTCLK	157. KDATA23	195. IRQ4*	233. IACKO*	271. VDATA1
6. VDATA24	44. $\overline{KRMC}$	82. KADDR13	120. JTMS	158. KDATA24	196. VADDR6	234. $\overline{VWR}$	272. VDATA2
7. VDATA25	45. V_{SS}	83. KADDR14	121. V_{SS}	159. KDATA25	197. V_{SS}	235. $\overline{VAS}$	273. V_{SS}
8. VDATA26	46. $\overline{KWR}$	84. KADDR15	122. KDATA0	160. KDATA26	198. VADDR7	236. VADDR24	274. VDATA3
9. VDATA27	47. $\overline{KDSACK0}$	85. KADDR16	123. KDATA1	161. KDATA27	199. VADDR8	237. VADDR25	275. VDATA4
10. V_{SS}	48. $\overline{KDSACK1}$	86. V_{SS}	124. KDATA2	162. V_{SS}	200. VADDR9	238. V_{SS}	276. VDATA5
11. BR3*	49. V_{DD}	87. BIMODE	125. V_{DD}	163. IRQ1*	201. V_{DD}	239. IACK*	277. V_{DD}
12. $\overline{L7INMI}$	50. Vss	88. BAUDCLK	126. V_{SS}	164. $\overline{LIRQ0}$	202. V_{SS}	240. $\overline{PWRRST}$	278. V_{SS}
13. VDATA28	51. V_{DD}	89. KADDR17	127. KDATA3	165. KDATA28	203. V_{DD}	241. $\overline{VMEOUT}$	279. VDATA6
14. VDATA29	52. $\overline{KDS}$	90. KADDR18	128. KDATA4	166. $\overline{LIRQ1}$	204. VADDR10	242. SYSFAIL*	280. VDATA7
15. VDATA30	53. $\overline{KBRQ}$	91. KADDR19	129. KDATA5	167. IRQ2*	205. $\overline{LIRQ4}$	243. VADDR26	281. VDATA8
16. V_{DD}	54. BR2*	92. V_{DD}	130. KDATA6	168. V_{DD}	206. IRQ5*	244. V_{DD}	282. SYSRST*
17. VDATA31	55. $\overline{KBGR}$	93. KADDR20	131. KDATA7	169. KDATA29	207. VADDR11	245. VADDR27	283. $\overline{SCV64SEL}$
18. $\overline{VMEINT}$	56. KADDR0	94. KADDR21	132. KDATA8	170. KDATA30	208. VADDR12	246. VADDR28	284. VDATA9
19. V_{SS}	57. KADDR1	95. V_{SS}	133. KDATA9	171. V_{SS}	209. VADDR13	247. V_{SS}	285. VDATA10
20. VDATAOUT	58. C14US	96. KADDR22	134. KDATA10	172. $\overline{LRST}$	210. VADDR14	248. VADDR29	286. VDATA11
21. VSTRBOUT	59. V_{SS}	97. KADDR23	135. V_{SS}	173. KDATA31	211. V_{SS}	249. VADDR30	287. V_{SS}
22. VADDROUT	60. KADDR2	98. KADDR24	136. KDATA11	174. $\overline{LIACK4}$	212. VADDR15	250. VADDR31	288. VDATA12
23. $\overline{VSBSEL}$	61. KADDR3	99. KADDR25	137. KDATA12	175. $\overline{LIRQ2}$ /$\overline{KIACK}$	213. VADDR16	251. BG0IN*	289. VDATA13
24. BR0*	62. V_{DD}	100. KADDR26	138. V_{DD}	176. IRQ3*	214. V_{DD}	252. BCLR*	290. V_{DD}
25. $\overline{BIREL}$	63. RETRY*/$\overline{VRMC}$	101. KADDR27	139. $\overline{KIPL0}$	177. $\overline{LMINT}$	215. IRQ6*	253. BG1IN*	291. BERR*
26. $\overline{RAMSEL}$	64. $\overline{EXTRST}$	102. KADDR28	140. $\overline{KIPL1}$	178. $\overline{LIACK5}$	216. $\overline{LIRQ5}$	254. IACKI*	292. $\overline{L7IACF}$
27. V_{DD}	65. KADDR4	103. KADDR29	141. $\overline{KIPL2}$	179. V_{DD}	217. VADDR17	255. DTACK*	293. VDATA14
28. V_{SS}	66. KADDR5	104. V_{SS}	142. KDATA13	180. V_{SS}	218. $\overline{LBRQ1}$	256. V_{SS}	294. $\overline{L7IMEM}$
29. V_{DD}	67. $\overline{KBGACK}$	105. VDD	143. KDATA14	181. V_{DD}	219. IRQ7*	257. V_{DD}	295. BBSY*
30. $\overline{TICK}$	68. V_{SS}	106. KADDR30	144. V_{SS}	182. BG0OUT*	220. V_{SS}	258. VAM0	296. V_{SS}
31. $\overline{WDOG}$	69. $\overline{KBERR}$	107. KADDR31	145. KDATA15	183. BG1OUT*	221. VADDR18	259. VAM1	297. VDATA15
32. $\overline{SYSFLED}$	70. KAVEC	108. KCLK	146. KDATA16	184. BG2OUT*	222. VADDR19	260. VAM2	298. VDATA16
33. V_{SS}	71. KADDR6	109. V_{SS}	147. KDATA17	185. V_{SS}	223. VADDR20	261. VSS	299. VDATA17
34. $\overline{LBGR1}$	72. KADDR7	110. JTDI	148. KDATA18	186. BG3OUT*	224. VADDR21	262. BG2IN*	300. VDATA18
35. BR1*	73. KADDR8	111. JTDO	149. KDATA19	187. $\overline{VLWORD}$	225. VADDR22	263. SYSCLK	301. VDATA19
36. $\overline{BITRIG}$	74. KADDR9	112. $\overline{KAS}$	150. KDATA20	188. VADDR1	226. VADDR23	264. BG3IN*	302. VDATA20
37. KSIZE0	75. V_{DD}	113. V_{DD}	151. V_{DD}	189. VADDR2	227. V_{DD}	265. V_{DD}	303. V_{DD}
38. KSIZE1	76. V_{SS}	114. C32MHZ	152. V_{SS}	190. VADDR3	228. V_{SS}	266. VAM3	304. V_{SS}

Appendix J Mechanical and Ordering Information

J.1 Mechanical Information



Controlling Dimensions in Inches

DIMENSION	PGA 299 CERAMIC	
	Min.	Max.
A	0.090 in.	0.110 in.
A1	0.112 in.	0.144 in.
B	0.045 in.	0.055 in.
C	0.017 in.	0.019 in.
D1	0.895 in.	0.905 in.
E	2.040 in.	2.080 in.
F	0.095 in.	0.105 in.
L	0.175 in.	0.185 in.
Q (Note 1)	0.045 in.	0.055 in.

Note 1. This dimension applies to the 4 ceramic disks on pins B2, B19, W2, and W19, which are used to hold the device above the printed circuit board.

Figure J.1 : 299-pin Cavity-down CPGA Package

Controlling dimensions in millimetres

DIMENSION	304 PQFP	
	Min.	Max.
A	3.95 mm	4.5 mm
A1	0.25 mm	
A2	3.60 mm	4.00 mm
B	0.14 mm	0.30 mm
e	0.50 mm	
E	43.00 mm	43.40 mm
E1	39.90 mm	40.10 mm
E3	37.5 mm	
G	0.10 mm	
L	0.70 mm	.090 mm
M	1.25 mm	
P	0.09 mm	0.20 mm

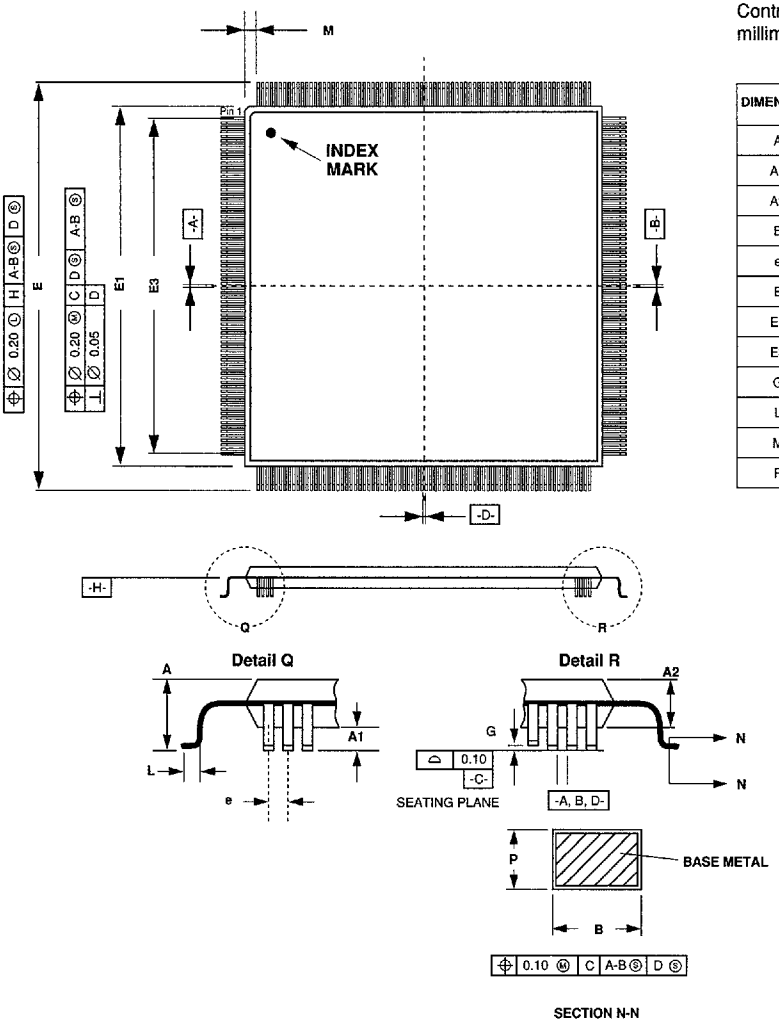
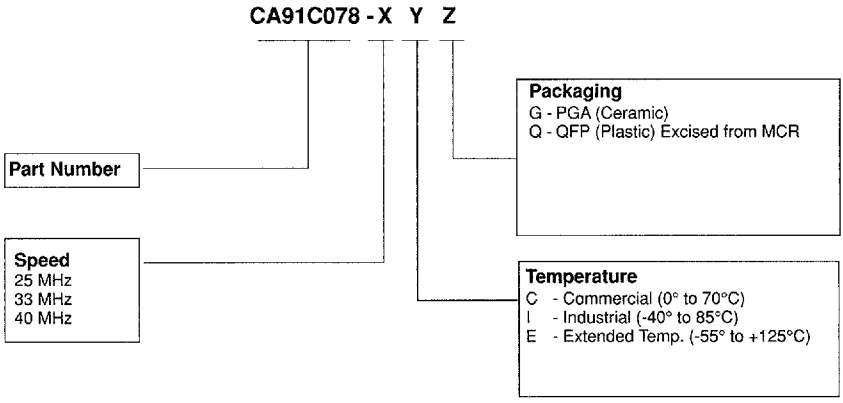


Figure J.2 : Mechanical Drawing for 304-Pin PQFP Package

J.2 Ordering Information

Tundra products are designated by a Product Code. When ordering, refer to products by their full code. For detailed mechanical drawings or alternative packaging requirements, please contact our factory directly.



Valid Suffixes for CA91C078

X	Y	Z
25	I	Q
25	E	G
33	C	G, Q
33	I	Q
33	E	G
40	C	G, Q