élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2006/EL2006A

High Gain Fast FET Input Op Amp

T-79-15

ELANTEC INC

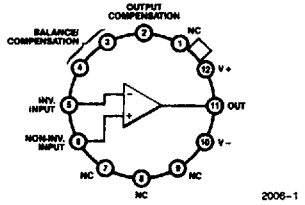
Features

- 90 dB open loop gain
- 450 V/μs slew rate
- 40 MHz bandwidth
- No thermal tail
- 3 mV max input offset voltage
- Offset nulls with single pot
- No compensation required for gains above 50
- Peak output current to 200 mA
- Pin compatible with LH0032
- 80 dB common mode rejection

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2006CG	−25°C to +85°C	TO-8	MDP0002
EL2006G	−55°C to +125°C	TO-8	MDP0002
EL2006G/883B	−55°C to +125°C	TO-8	MDP0002
EL2006ACG	−25°C to +85°C	TO-8	MDP0002
EL2006AG	−55°C to +125°C	TO-8	MDP0002
EL2006AG/883G	−55°C to +125°C	TO-8	MDP0002
EL2006L	−55°C to +125°C	52-Pad LCC	MDP0013

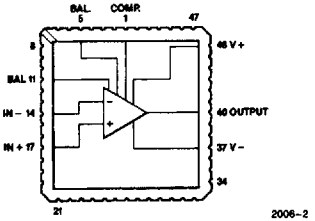
Connection Diagrams



2006-1

Top View

L Package



2006-2

Top View

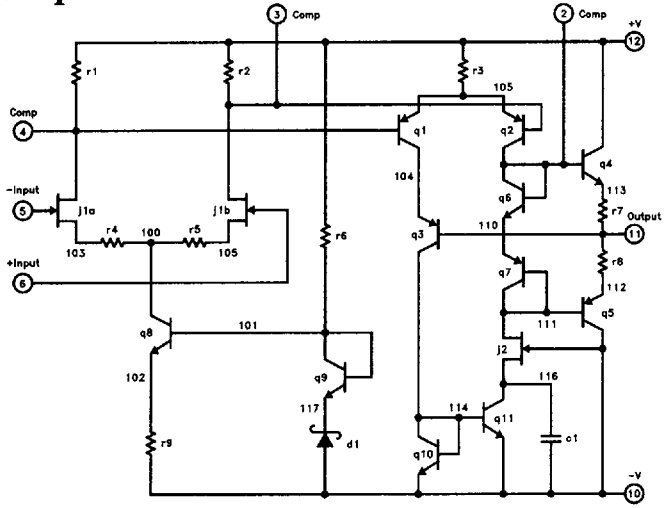
General Description

The EL2006/EL2006A are high slew rate, wide bandwidth, high input impedance, high gain and fully differential input operational amplifiers. They exhibit excellent open loop gain characteristics making them suitable for a broad range of high speed signal processing applications. These patented devices have open loop gains in excess of 86 dB making the EL2006/EL2006A ideal choices for current mode video bandwidth digital to analog converters of 10 bits or higher resolution. The EL2006's FET input structure, high slew rate, and high output drive capability allow use in applications such as buffers for flash converter inputs. In general, the EL2006/EL2006A allow the user to take relatively high closed loop gains without compromising gain accuracy or bandwidth.

The EL2006/EL2006A are pin compatible with the popular industry standard ELH0032/ELH0032A offering comparable bandwidth and slew rate, while offering significant improvements in open loop gain, common mode rejection and power supply rejection.

Elantec facilities comply with MIL-I-45208A and are MIL-STD-1772 certified. Elantec's Military devices comply with MIL-STD-883 Class B Revision C and are manufactured in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance Policy and procedures request brochure QRA-1.

Simplified Schematic



2006-3

Manufactured under U.S. Patent No. 4,746,877

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage	±15V		EL2006, EL2006A	−55°C to +125°C
	Differential Input Voltage	30V		EL2006C, EL2006AC	−25°C to +85°C
I_{OUT}	Peak Output Current (Note 1)	±200 mA	T_J	Operating Junction Temperature	175°C
P_D	Power Dissipation		T_{ST}	Storage Temperature	−65°C to +150°C
	T_A = 25°C 1.5W, derate 100°C/W to +125°C			Lead Temperature	
	T_C = 25°C 2.2W, derate 70°C/W to +125°C			(Soldering 10 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, $T_{MIN} < T_A < T_{MAX}$

Parameter	Description	Test Conditions	EL2006				EL2006C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	T_J = 25°C			5	I			5	I	mV
					10	I			10	III	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift			15		V		15		V	µV/°C
I_B	Bias Current	T_J = 25°C			100	I			500	I	pA
				1	10	I		1	10	III	nA
I_{OS}	Offset Current	T_J = 25°C			25	I			50	I	pA
				0.2	2.5	I		0.2	2.5	III	nA
V_{CM}	Common Mode Range		±10			I	±10			II	V
CMRR	Common Mode Rejection Ratio	ΔV_{IN} = ±10V	70	80		I	70	80		II	dB
PSRR	Power Supply Rejection Ratio	±5V ≤ V_S ≤ ±15V	70	88		I	70	88		II	dB
A_{VOL}	Large Signal Voltage Gain	R_L = 1 kΩ, V_{OUT} = ±10V, T_J = 25°C	74	90		I	74	90		I	dB
		R_L = 1 kΩ, V_{OUT} = ±10V	80			I	74			III	dB
V_O	Output Voltage Swing	R_L = 1 kΩ	±12			I	±12			II	V
I_{OUT}	Output Current	V_{OUT} = ±10V, T_J = 25°C, (Note 1)	±100			I	±100			I	mA
I_{CC}	Supply Current			20	23	I		20	23	II	mA

EL2006/EL2006A
High Gain Fast FET Input Op Amp

DC Electrical Characteristics — Contd.

$V_S = \pm 15V$, $T_{MIN} < T_A < T_{MAX}$ (Note: These tests are in addition to those listed above.)

Parameter	Description	Test Conditions	EL2006A				EL2006AC				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	$T_J = 25°C$			3	I			3	I	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift			15	25	I		15	25	I	µV/°C
A_{VOL}	Large Signal Voltage Gain	$T_J = 25°C$, $R_L = 1 k\Omega$, $V_{OUT} = \pm 10V$	74	90		I	74	90		II	dB
		$R_L = 1 k\Omega$, $V_{OUT} = \pm 10V$	74			I	74			III	dB

AC Electrical Characteristics

$V_S = \pm 15V$, $R_L = 1 k\Omega$, $T_J = 25°C$ (See AC Test Circuits)

Parameter	Description	Test Conditions	EL2006, EL2006A				EL2006C, EL2006AC				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
t_r	Rise Time	$A_V = 10V$, $V_{OUT} = 1 V_{P-P}$		18		V		18		V	ns
		$A_V = 1V$, $V_{OUT} = 1 V_{P-P}$		12	15	I		12	15	I	ns
SR	Slew Rate (Note 2)	$A_V = 1V$, $V_{OUT} = 20 V_{P-P}$	350	450		I	350	450		I	V/µs
t_s	Settling Time to 1.0%	$A_V = -1V$, $V_{OUT} = 10 V_{P-P}$		90		V		90		V	ns
t_s	Settling Time to 0.1%	$A_V = -1V$, $V_{OUT} = 10 V_{P-P}$		160		V		160		V	ns
t_s	Settling Time to 0.01%	$A_V = -1V$, $V_{OUT} = 10 V_{P-P}$		250		V		250		V	ns
GBW	Gain Bandwidth Product	$A_V \geq 20V$		500		V		500		V	MHz
	Pull Power Bandwidth (Note 3)	$V_{OUT} = \pm 10V$	5.5	7		I	5.5	7		I	MHz
	Unity Gain Bandwidth	$C_A = 8 pF$, $C_B = 100 pF$		40		V		40		V	MHz
e_N	Noise Voltage	1 kHz to 1 MHz		20		V		20		V	nV/√Hz
t_D	Small Signal Delay	$A_V = 1V$		13	15	I		13	15	I	ns
C_{IN}	Input Capacitance			2		V		2		V	pF

Note 1: $T_J = 25°C$, duty cycle < 1%, pulse width < 10 µs.
Note 2: Slew rate is measured at the 25% and 75% points.
Note 3: The Full Power bandwidth is guaranteed by testing slew rate.

EL2006 Recommended Compensation

(See Figure 1)

A_{VOL}	C_A	C_B	R_{S+}	R_{S-}	R_F
+1	5–8 pF	100 pF	2k	Open Circuit	100
−1 to +5	5 pF	68 pF	0	< 1k	1k
±10	5 pF	10 pF	< 1k	1k	> 10k
> ±20	3 pF	10 pF	< 1k	1k	> 20k

Note: Use a small capacitor of about 1 pF in parallel with R_F to compensate for stray input capacitance.

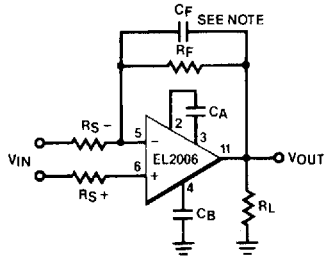
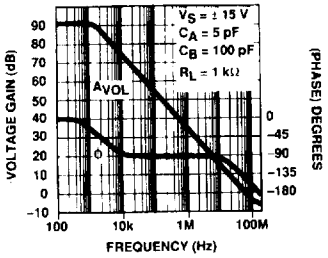


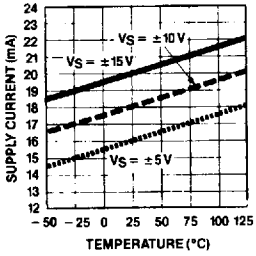
Figure 1

Typical Performance Curves

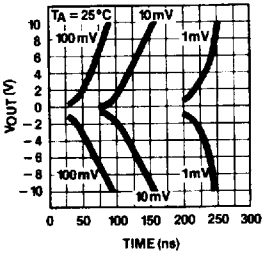
Bode Plot, Unity Gain Compensation



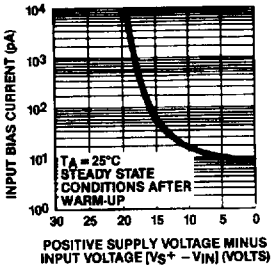
Supply Current vs Temperature



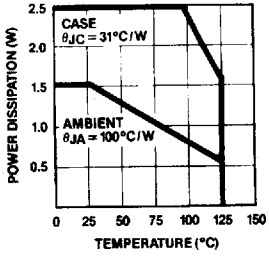
Inverting Gain of −1 Settling Time



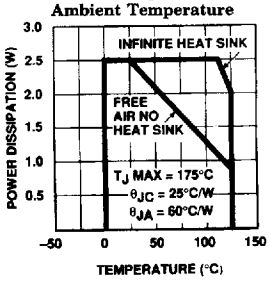
Input Bias Currents as a Function of Input Voltage



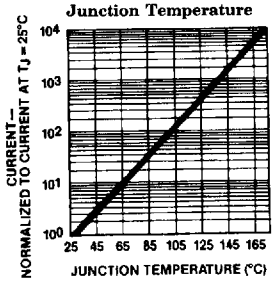
TO-8 Maximum Power Dissipation



52-Pad LCC Maximum Power Dissipation vs Ambient Temperature



Normalized Input Bias and Offset Current vs Junction Temperature



2006-5

Applications Information

General

The EL2006 was designed to overcome the gain and stability limitations of prior high speed FET input operational amplifiers like the LH0032. Open loop gain is typically 90 dB allowing gain setting to 12-bit accuracy. This new design also eliminates "thermal tail", which is the tendency for the gain to diminish at very low frequencies to DC due to thermal feedback. The EL2006 is also easier to stabilize than earlier designs, thanks to an Elantec proprietary internal compensation technique which eliminates the "second stage bump." The EL2006 open loop gain

EL2006/EL2006A
High Gain Fast FET Input Op Amp

Applications Information — Contd.

characteristic is well behaved well beyond the unity gain frequency so that spurious ringing or oscillation in the 100 MHZ–200 MHz region is avoided. Finally, we have provided temperature compensation so that gain and stability are relatively constant over temperature.

These improvements are provided in a configuration which is plug compatible with LH0032 and similar products so that designers can easily upgrade their system performance without extensive re-design. In most cases, the EL2006 can be used to replace LH0032 with no change in external compensation.

Video DAC Amplifiers

A typical application for the EL2006 is to provide gain for video signals. In the example shown, the EL2006 provides a gain of 2 with settling time around 35 ns to 10 mV.

Power Supply Decoupling

The EL2006/EL2006A, like most high-speed circuits, is sensitive to layout and stray capacitance. Power supplies should be bypassed as near to pins 10 and 12 as possible with low inductance capacitors such as 0.01 μF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

Input Current

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power, thus raising the FET junction temperature 40°C–60°C above the free-air ambient temperature when supplies are ±15V. The device temperature will stabilize within 5–10 minutes after application of power, and the input bias currents measured at the time will be indicative of normal operating currents. An additional rise will occur as power is delivered to a load due to additional internal power dissipation.

Power Dissipation

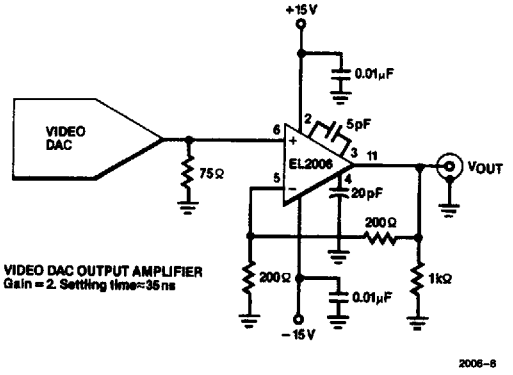
There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalanche-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value, depending on FET geometry and doping levels. This effect will be noted as the input voltage of the EL2006 is taken below ground potential when the supplies are ±15V. All of the effects described here may be minimized by operating the device with $V_S \leq \pm 15V$.

These effects are indicated in the typical performance curves.

Input Capacitance

The input capacitance to the EL2006/EL2006A is typically 2 pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a 1 pF.



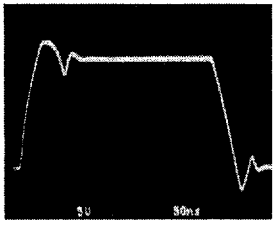
VIDEO DAC OUTPUT AMPLIFIER
Gain = 2. Settling time=35 ns

Applications Information — Contd.

Heatsinking

While the EL2006/EL2006A are specified for operation without any explicit heatsink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

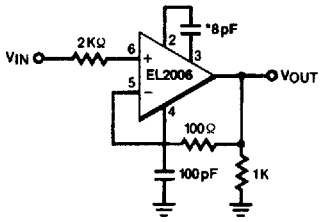
Voltage Follower (A_V = +1)
Large Signal Pulse Response



2006-12

V_S = ±15V, V_{IN} = +10V to −10V and −10V to +10V

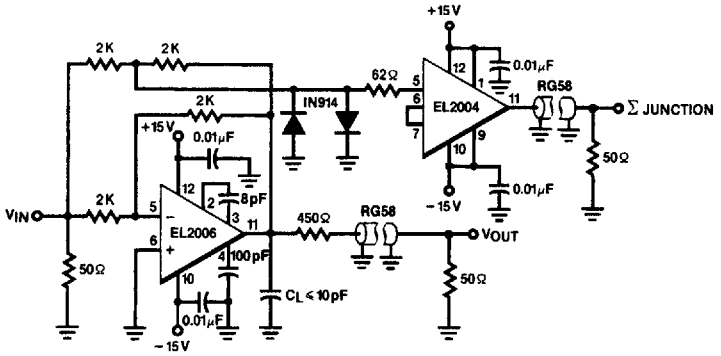
Large Signal Pulse Response Test Circuit



*INCLUDES STRAYS

2006-7

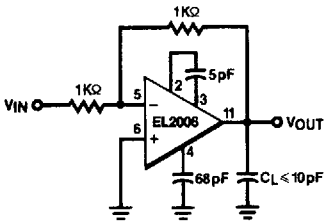
EL2006 Settling Time Test Circuit



R_L = 2KΩ // 2KΩ // 500Ω = 333Ω

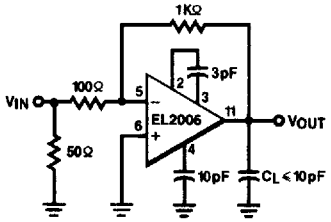
2006-8

Inverting Unity Gain



2006-9

Inverting Gain of 10

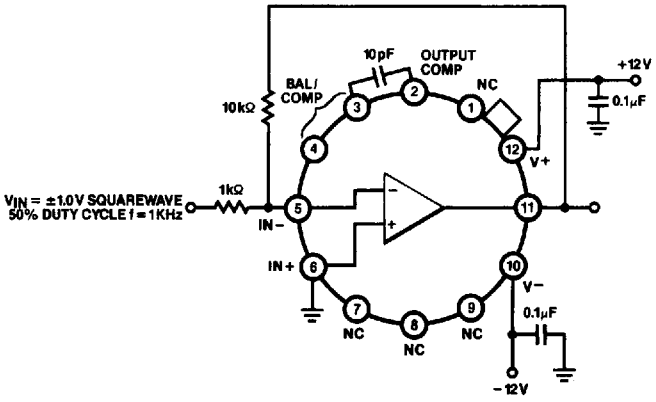


2006-10

EL2006/EL2006A

High Gain Fast FET Input Op Amp

Burn-In Circuit



Pin Numbers are for TO-8 package. LCC uses the same schematic.

EL2006 Macromodel

```
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     Comp 3
*                   |     |     |     |     |     Comp 4
*                   |     |     |     |     |     |     Comp 2
*                   |     |     |     |     |     |     |     Output
*                   |     |     |     |     |     |     |     |
.subckt M2006       6     5     12    10    3     4     2     11
* Models
.model qfa njf (vto = -2.5V beta = 1.11e-3 cgd = 2pF cgs = 5pF m = 0.3744)
.model qp pnp (is = 5E-14 bf = 150 vaf = 100 ikf = 100mA tf = .53nS vtf = 0 ise = 1 nA,
+ cjc = 4pF cje = 5.7pF tr = 170nS rb = 3 br = 5 mje = .32 mjc = .43 xtb = 2.1 ne = 4
+ isc = 1nA nc = 4 itf = .4 vtf = 4 xtf = 6)
.model qn npn (is = 5e-14 bf = 150 vaf = 800 ikf = 200mA tf = .54nS vtf = 0
+ cjc = 4pF cje = 5pF rb = 3 br = 5 mje = .42 mjc = .23 tr = 200nS xtb = 2.1
+ ise = 4nA ne = 4 isc = 4nA nc = 4 itf = .4 vtf = 4 xtf = 2)
.model qfb njf (vto = -2.8V beta = 4e-3 cgd = 7pF cgs = 8pF lambda = 4e-3)
.model zener d (bv = 2.49V ibv = 1mA)
* Resistors and Capacitors
r1 12 4 700
r2 12 3 700
r3 12 105 160
r4 103 100 10
r5 108 100 10
r6 12 101 22K
r7 113 11 10
r8 11 112 10
r9 102 10 407
cs2 10 116 100pF
* Transistors and Diodes
j1a 4 5 103 qfa
j1b 3 6 108 qfa
j2 111 10 116 qfb
q1 104 4 105 qp
q2 2 3 105 qp
q3 114 11 104 qp
q4 12 2 113 qn
q5 10 111 112 qp
q6 2 2 110 qn
q7 111 111 110 qp
q8 100 101 102 qn
d1 10 117 zener
q9 101 101 117 qn
q10 114 114 10 qn
q11 116 114 10 qn
.ends
```

EL2006 Macromodel — Contd.