



# MX23L6411

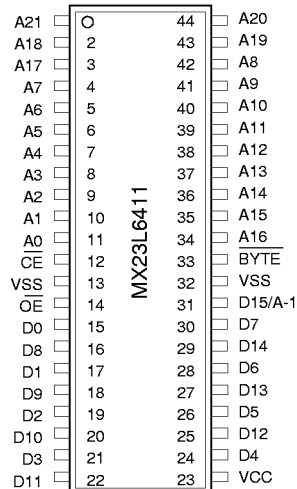
## 64M-BIT Mask ROM (8/16 Bit Output)

### FEATURES

- Bit organization
  - 8M x 8 (byte mode)
  - 4M x 16 (word mode)
- Fast access time
  - Random access: 120ns (max.)
  - Page access: 50ns (max.)
- Page Size
  - 8 words per page
- Current
  - Operating: 60mA (max.)
  - Standby: 15uA (max.)
- Supply voltage
  - 2.9V~3.6V
- Package
  - 44 pin SOP (500 mil)
  - 48 pin TSOP (20mm x 12mm)

### PIN CONFIGURATION

#### 44 SOP



### ORDER INFORMATION

Part No.	Access Time	Page Access Time	Package
MX23L6411MC-12	120ns	50ns	44 pin SOP
MX23L6411TC-12	120ns	50ns	48 pin TSOP
MX23L6411RC-12	120ns	50ns	48 pin TSOP (Reverse type)

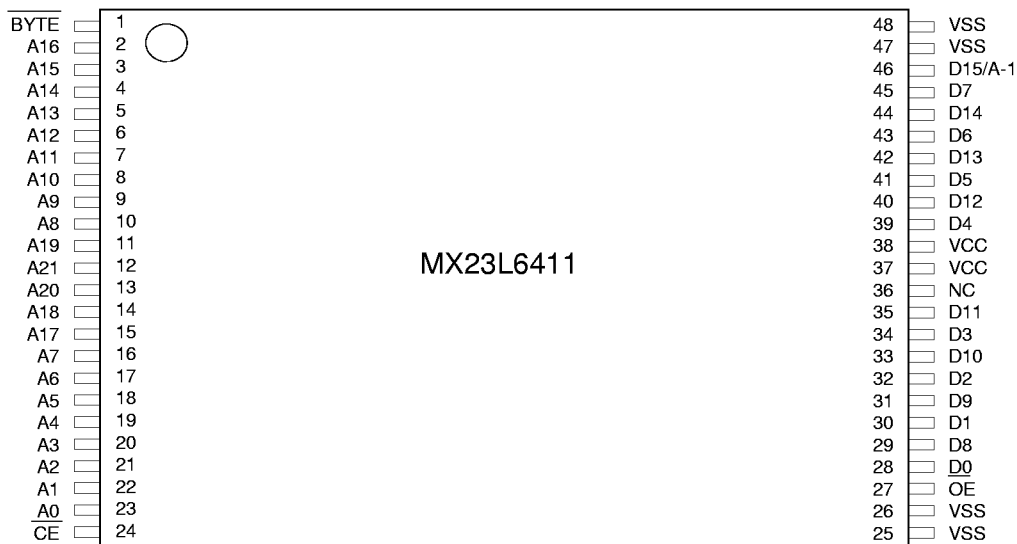
### PIN DESCRIPTION

Symbol	Pin Function
A0~A21	Address Inputs
D0~D14	Data Outputs
D15/A-1	D15 (Word Mode) / LSB Address (Byte Mode)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
Byte	Word / Byte Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

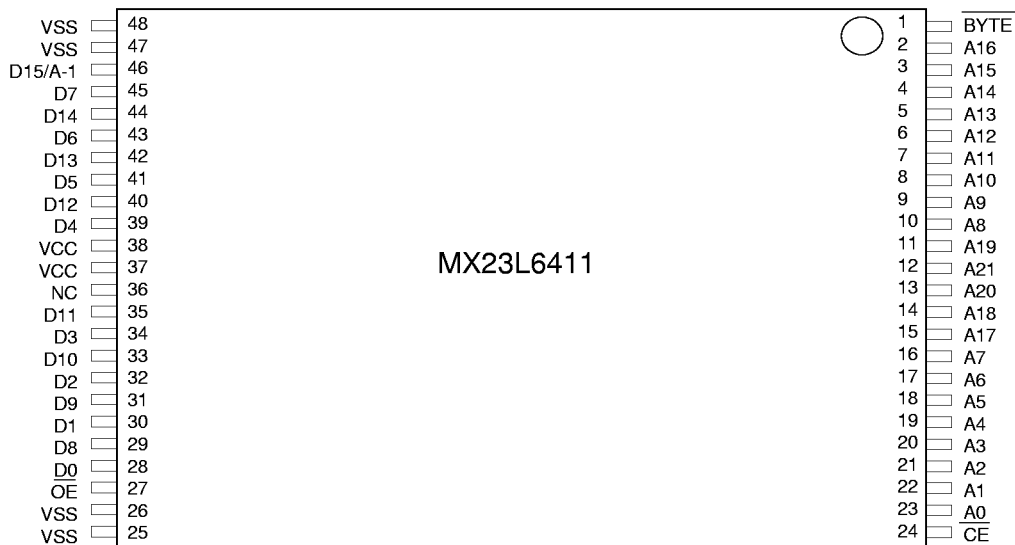
### MODE SELECTION

$\overline{CE}$	$\overline{OE}$	Byte	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

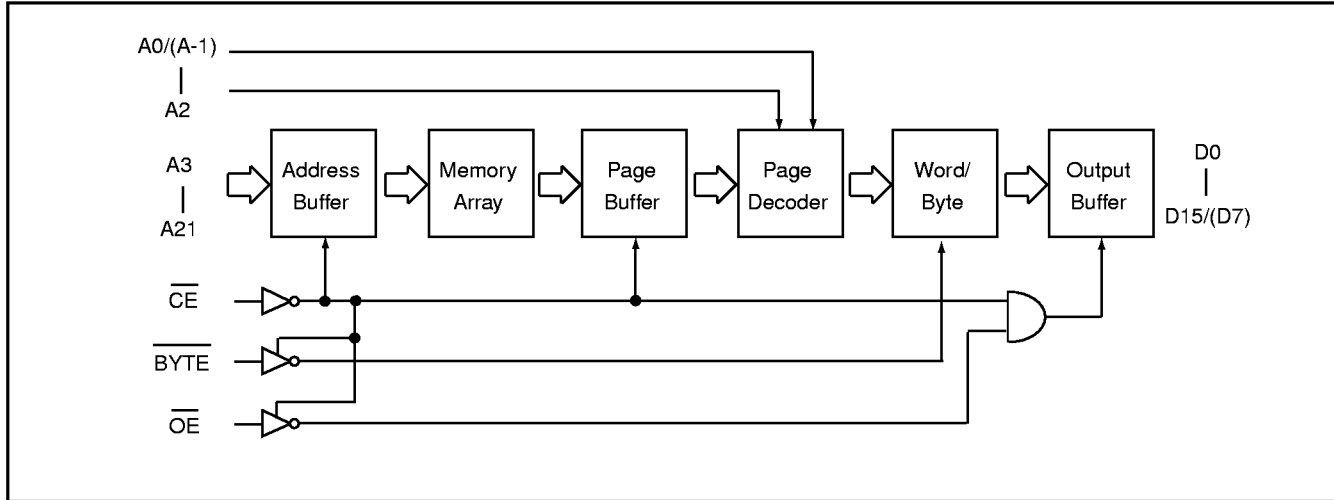
## 48TSOP (NORMAL TYPE)



## 48TSOP (REVERSE TYPE)



## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	V <sub>IN</sub>	-1.3V to 2.0V
Ambient Operating Temperature	T <sub>opr</sub>	0°C to 70°C
Storage Temperature	T <sub>stg</sub>	-65°C to 125°C

Note: Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -1.3V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.



## DC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 2.9V~3.6V)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC1	-	60mA	tRC = 120ns, all output open
	ICC2	-	30mA	tRC=1us
Standby Current (TTL)	ISTB1	-	1mA	$\overline{CE} = V_{IH}$
Standby Current (CMOS)	ISTB2	-	15uA	$\overline{CE} > V_{CC} - 0.2V$
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHZ

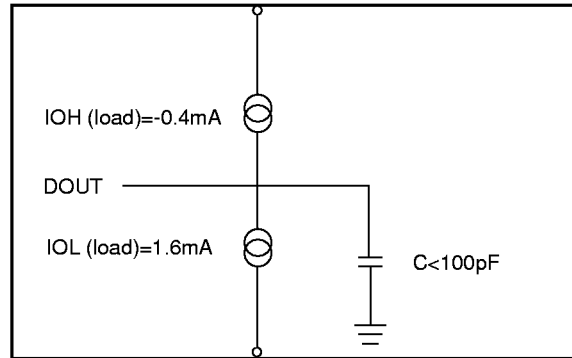
## AC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 3.0V~3.6V)

Item	Symbol	23L6411-12	
		MIN.	MAX.
Read Cycle Time	tRC	120ns	-
Address Access Time	tAA	-	120ns
Chip Enable Access Time	tACE	-	120ns
Page Mode Access Time	tPA	-	50ns
Output Enable Time	tOE	-	50ns
Output Hold After Address	tOH	0ns	-
Output High Z Delay	tHZ	-	20ns

Note: Output high-impedance delay (tHZ) is measured from  $\overline{OE}$  or  $\overline{CE}$  going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

## AC Test Conditions

Input Pulse Levels	0.4V~ 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure



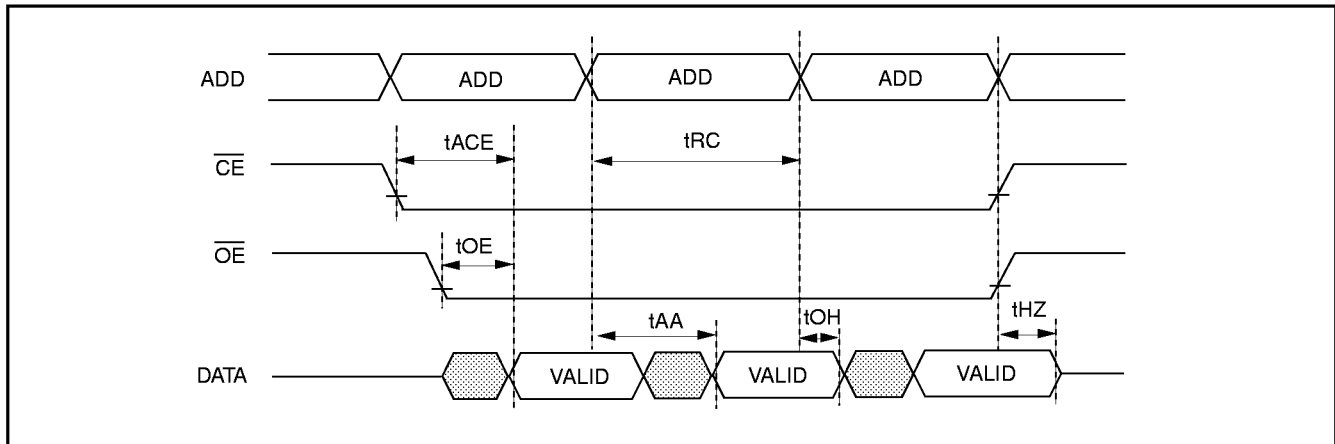
Note: No output loading is present in tester load board.

Active loading is used and under software programming control.

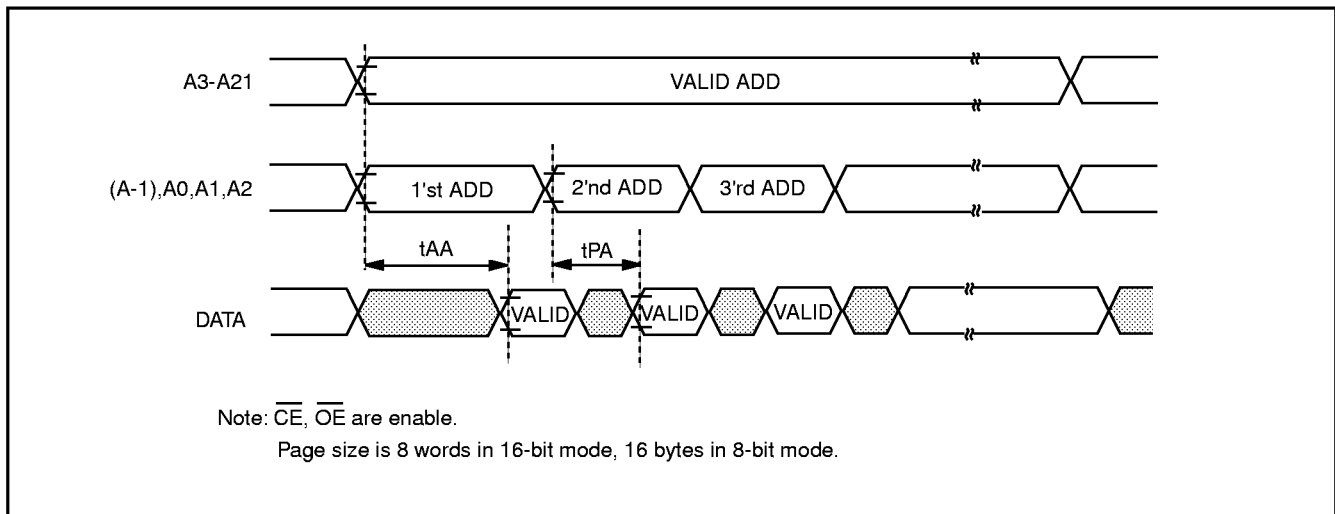
Output loading capacitance includes load board's and all stray capacitance.

## TIMING DIAGRAM

### RANDOM READ



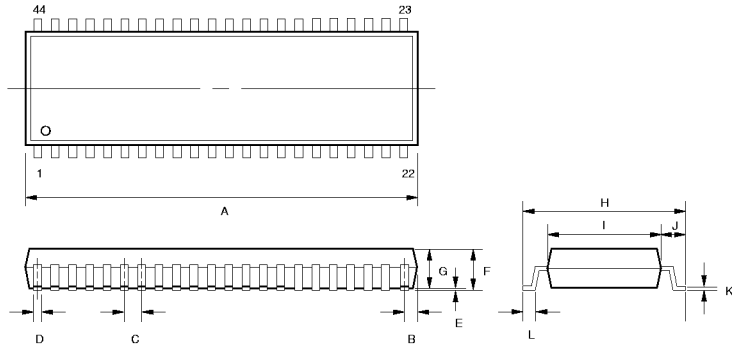
### PAGE READ



## PACKAGE INFORMATION

### 44-PIN PLASTIC SOP

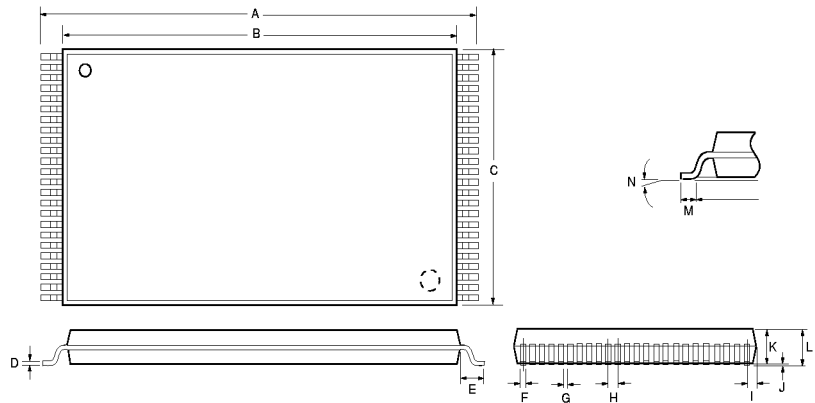
ITEM	MILLIMETERS	INCHES
A	28.70 max.	1.130 max.
B	1.10 [REF]	.043 [REF]
C	1.27 [TP]	.050 [TP]
D	.40 ± .10 [Typ.]	.016 ± .004 [Typ.]
E	.010 min.	.004 min.
F	3.00 max.	.118 max.
G	2.80 ± .13	.110 ± .005
H	16.04 ± .30	.631 ± .012
I	12.60	.496
J	1.72	.068
K	.15 ± .10 [Typ.]	.006 ± .004 [Typ.]
L	.80 ± .20	.031 ± .008



**NOTE:** Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.

### 48-PIN PLASTIC TSOP

ITEM	MILLIMETERS	INCHES
A	20.0 ± .20	.787 ± .008
B	18.40 ± .10	.724 ± .004
C	12.20 max.	.480 max.
D	0.15 [Typ.]	.006 [Typ.]
E	.80 [Typ.]	.031 [Typ.]
F	.20 ± .10	.008 ± .004
G	.30 ± .10	.012 ± .004
H	.50 [Typ.]	.020 [Typ.]
I	.45 max.	.018 max.
J	0 ~ .20	0 ~ .008
K	1.00 ± .10	.039 ± .004
L	1.27 max.	.050 max.
M	.50	.020
N	0 ~ 5°	.500



**NOTE:** Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.



**REVISION HISTORY**

REVISION	DESCRIPTION	PAGE	DATE
2.1	AC CHARACTERISTICS tOH 10ns-->0ns	P4	JAN/29/1999
2.2	DC CHARACTERISTICS ISTB2 5uA-->15uA	P4	SEP/03/1999