



Data Sheet

SST 29EE512
5.0V-only 512 Kilobit
Page Mode EEPROM

July 1996



SST 29EE512

5.0V-only 512 Kilobit

Page Mode EEPROM

Features:

Single 5.0-Volt Read and Write Operations CMOS SuperFlash EEPROM Technology

Endurance: 100,000 Cycles (typical)
Greater than 100 years Data Retention

Low Power Consumption:

Active Current: 20 mA (typical)
Standby Current: 10 μ A (typical)

Fast Page-Write Operation

128 Bytes per Page, 512 Pages
Page-Write Cycle: 5 ms (typical)
Complete Memory Rewrite: 2.5 sec (typical)
Effective Byte-write Cycle Time: 39 μ s (typical)

Fast Access Time: 90 and 120 ns

Latched Address and Data

Automatic Write Timing with Internal V_{pp} Generation

End of Write Detection

Toggle Bit
Data# Polling

Hardware and Software Data Protection

TTL I/O Compatibility

JEDEC Standard Byte-wide EEPROM

Pinouts

Packages Available

32-Pin TSOP
32-Lead PLCC
32 Pin Plastic DIP

Product Description

The 29EE512 is a 64K x 8 CMOS page mode EEPROM manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The 29EE512 writes with a 5.0-volt-only power supply. Internal erase/program is transparent to the user. The 29EE512 conforms to JEDEC standard pinouts for byte-wide memories.

Featuring high performance page write, the 29EE512 provides a typical byte-write time of 39 μ sec. The entire memory, i.e., 64K bytes, can be written page by page in as little as 2.5 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of a write cycle. To protect against inadvertent write, the 29EE512 has on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the 29EE512 is offered with a guaranteed page-write endurance of 10^4 or 10^3 cycles. Data retention is rated at greater than 100 years.

The 29EE512 is suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the 29EE512 significantly improves performance and reliability, while lowering power consumption, when compared with floppy disk or EPROM approaches. The 29EE512 improves

flexibility while lowering the cost for program, data, and configuration storage applications.

To meet high density, surface mount requirements, the 29EE512 is offered in 32-pin TSOP and 32-lead PLCC packages. A 600-mil, 32-pin PDIP package is also available. See Figures 2A and 2B for pinouts.

Device Operation

The SST page mode EEPROM offers in-circuit electrical write capability. The 29EE512 does not require separate erase and program operations. The internally timed write cycle executes both erase and program transparently to the user. The 29EE512 has industry standard optional Software Data Protection, which SST recommends always to be enabled. The 29EE512 is compatible with industry standard EEPROM pinouts and functionality.

Read

The read operation of the 29EE512 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the read cycle timing diagram for further details (Figure 3).

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Write

The write operation consists of three steps. The first step is the optional three byte load sequence for Software Data Protection. This is an optional first step in the write operation, but highly recommended to ensure proper data integrity. Step 2 is the byte-load cycle to a page buffer of the 29EE512. Step 3 is an internally controlled write cycle for writing the data loaded in the page buffer into the memory array for nonvolatile storage. During the byte-load cycle, the addresses are latched by the falling edge of either CE# or WE#, whichever occurs last. The data is latched by the rising edge of either CE# or WE#, whichever occurs first. The internal write cycle is initiated by a timer after the rising edge of WE# or CE#, whichever occurs first. The write cycle, once initiated, will continue to completion, typically within 5 ms. See Figures 4 and 5 for WE# and CE# controlled page write cycle timing diagrams and Figures 15 and 17 for flowcharts.

The write operation has three functional cycles: the optional Software Data Protection load sequence, the page load cycle and the internal write cycle. The Software Data Protection consists of a specific three byte load sequence that will leave the 29EE512 protected at the end of the page write. The page load cycle consists of loading 1 to 128 bytes of data into the page buffer. The internal write cycle consists of the T_{BLCO} time-out and the write timer operation. During the write operation, the only valid reads are Data# Polling and Toggle Bit.

The page-write operation allows the loading of up to 128 bytes of data into the page buffer of the 29EE512 before the initiation of the internal write cycle. During the internal write cycle, all the data in the page buffer is written simultaneously into the memory array. Hence, the page-write feature of 29EE512 allows the entire memory to be written in as little as 2.5 seconds. During the internal write cycle, the host is free to perform additional tasks, such as to fetch data from other locations in the system to set up the write to the next page. In each page-write operation, all the bytes that are loaded into the page buffer must have the same page address, i.e., A_7 through A_{15} . Any byte not loaded with user data will be written to FF.

See Figures 4, 5, and 8 for the page-write cycle timing diagrams. If after the initial byte-load cycle, the host loads a second byte into the page buffer within a byte-load cycle time (T_{BLC}) of 100 μ s, the 29EE512 will stay in the page load cycle. Additional bytes are then loaded consecutively. The page load cycle will be terminated if no additional byte is loaded into the page buffer within 200 μ s (T_{BLCO}) from the last byte-load cycle, i.e., no subsequent WE# or CE# high-to-low transition after the last rising edge of WE# or CE#. Data in the page buffer can be changed by a subsequent byte-load cycle. The page load period can continue indefinitely, as long as the host continues to load the device within the byte-load cycle time of 100 μ s. The page to be loaded is determined by the page address of the last byte loaded.

Software Chip-Erase

The 29EE512 provides a chip-erase operation, which allows the user to simultaneously clear the entire memory array to the "1" state. This is useful when the entire device must be quickly erased.

The Software Chip-Erase operation is initiated by using a specific six byte-load sequence. After the load sequence, the device enters into an internally timed cycle similar to the write cycle. During the erase operation, the only valid read is Toggle Bit. See Table 4 for the load sequence, Figure 10 for timing diagram, and Figure 19 for the flowchart.

Write Operation Status Detection

The 29EE512 provides two software means to detect the completion of a write cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The end of write detection mode is enabled after the rising WE# or CE# whichever occurs first, which initiates the internal write cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6 . In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If



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both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ₇)

When the 29EE512 is in the internal write cycle, any attempt to read DQ₇ of the last byte loaded during the byte-load cycle will receive the complement of the true data. Once the write cycle is completed, DQ₇ will show true data. The device is then ready for the next operation. See Figure 6 for Data# Polling timing diagram and Figure 16 for a flowchart.

Toggle Bit (DQ₆)

During the internal write cycle, any consecutive attempts to read DQ₆ will produce alternating 0's and 1's, i.e., toggling between 0 and 1. When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 7 for Toggle Bit timing diagram and Figure 16 for a flowchart. The initial read of the Toggle Bit will be a "1".

Data Protection

The 29EE512 provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The 29EE512 provides the JEDEC approved optional software data protection scheme for all data alteration operations, i.e., write and chip erase. With this scheme, any write operation requires the inclusion of a series of three byte-load operations to precede the data loading operation. The three byte-load sequence is used to initiate the write cycle, providing optimal protection from inadvertent write operations, e.g., during the system power-up or power-down. The 29EE512 is shipped with the software data protection disabled.

The software protection scheme can be enabled by applying a three-byte sequence to the device, during a page-load cycle (Figure 8). The device will then be automatically set into the data protect mode. Any subsequent write operation will require the preceding three-byte sequence. See Table 4 for the specific software command codes and Figure 8 for the timing diagram. To set the device into the unprotected mode, a six-byte sequence is required. See Table 4 for the specific codes and Figure 9 for the timing diagram. If a write is attempted while SDP is enabled the device will be in a non-accessible state for ~ 300 μs. SST recommends Software Data Protection always be enabled. See Figure 17 for flowcharts.

The 29EE512 Software Data Protection is a global command, protecting (or unprotecting) all pages in the entire memory array once enabled (or disabled). Therefore using SDP for a single page write will enable SDP for the entire array. Single pages by themselves cannot be SDP enabled or disabled.

Single power supply reprogrammable nonvolatile memories may be unintentionally altered. SST strongly recommends that Software Data Protection (SDP) always be enabled. The 29EE512 should be programmed using the SDP command sequence. SST recommends the SDP Disable Command Sequence not be issued to the device prior to writing.

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Product Identification

The product identification mode identifies the device as the 29EE512 and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by a programmer to identify the correct algorithm for the SST 29EE512. Users may wish to use the software product identification operation to identify the part (i.e., using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 11 for the software ID entry and read timing diagram and Figure 18 for the ID entry command sequence flowchart. The manufacturer and device codes are the same for both operations.

Table 1: Product Identification Table

	Byte	Data
Manufacturers Code	0000 H	BF H
Device Code	0001 H	5D H

Product Identification Mode Exit

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Software ID Exit (reset) operation, which returns the device to the read operation. The reset operation may also be used to reset the device to the read mode after an inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. See Table 4 for software command codes, Figure 12 for timing waveform and Figure 18 for a flowchart.

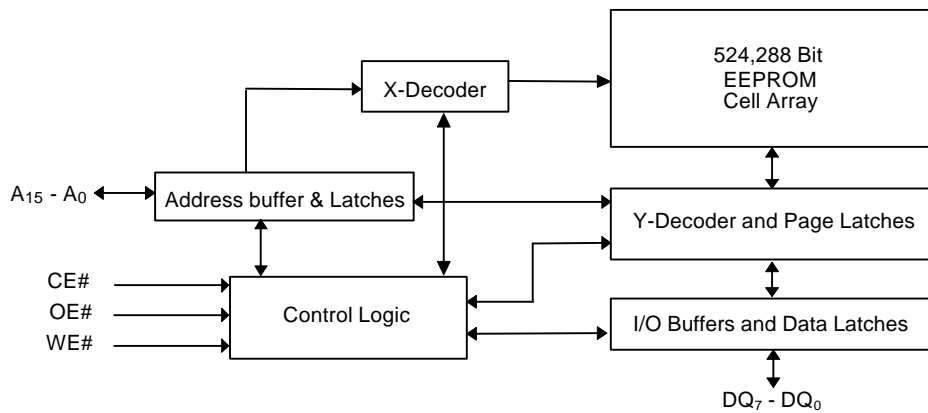


Figure 1: Functional Block Diagram of SST 29EE512



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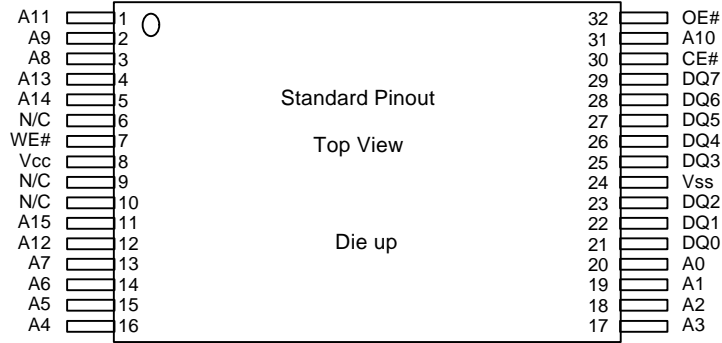


Figure 2A: Pin Assignments for 32-pin TSOP Packages

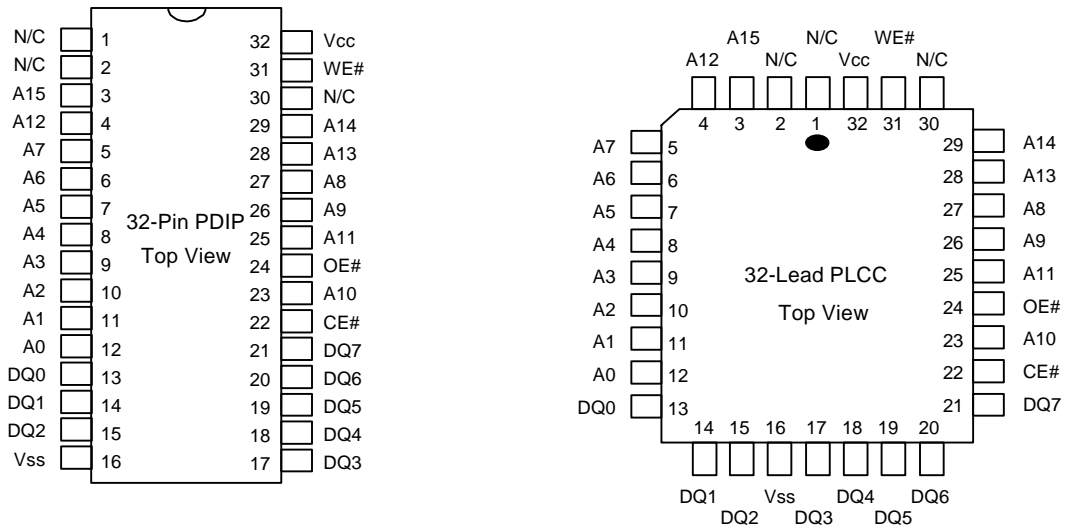


Figure 2B: Pin Assignments for 32-pin Plastic DIPs and 32-lead PLCCs

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Table 2: Pin Description

Symbol	Pin Name	Functions
A ₁₅ -A ₇	Row Address Inputs	To provide memory addresses. Row addresses define a page for a write cycle.
A ₆ -A ₀	Column Address Inputs	Column Addresses are toggled to load page data.
DQ ₇ -DQ ₀	Data Input/output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the write operations
V _{cc}	Power Supply	To provide 5-volt supply ($\pm 10\%$)
V _{ss}	Ground	
NC	No Connection	Unconnected pins.

Table 3: Operation Modes Selection

Mode	CE#	OE#	WE#	DQ	Address
Read	V _{IL}	V _{IL}	V _{IH}	D _{OUT}	A _{IN}
Page Write	V _{IL}	V _{IH}	V _{IL}	D _{IN}	A _{IN}
Standby	V _{IH}	X	X	High Z	X
Write Inhibit	X	V _{IL}	X	High Z/ D _{OUT}	X
Write Inhibit	X	X	V _{IH}	High Z/ D _{OUT}	X
Software Chip Erase	V _{IL}	V _{IH}	V _{IL}	D _{IN}	A _{IN} , See Table 4
Product Identification					
Hardware Mode	V _{IL}	V _{IL}	V _{IH}	Manufacturer Code (BF)	A ₁₅ - A ₁ = V _{IL} , A ₉ = V _H , A ₀ = V _{IL}
				Device Code (5D)	A ₁₅ - A ₁ = V _{IL} , A ₉ = V _H , A ₀ = V _{IH}
Software Mode	V _{IL}	V _{IH}	V _{IL}		See Table 4
SDP Enable Mode	V _{IL}	V _{IH}	V _{IL}		See Table 4
SDP Disable Mode	V _{IL}	V _{IH}	V _{IL}		See Table 4



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Table 4: Software Command Codes

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr ⁽¹⁾	Data	Addr ⁽¹⁾	Data	Addr ⁽¹⁾	Data	Addr ⁽¹⁾	Data	Addr ⁽¹⁾	Data	Addr ⁽¹⁾	Data
Software Data Protect Enable & Page Write	5555H	AAH	2AAAH	55H	5555H	A0H	Addr ⁽²⁾	Data				
Software Data Protect Disable	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	20H
Software Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						
Alternate Software ID Entry ⁽³⁾	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	60H

Notes: ⁽¹⁾ Address format A₁₄-A₀ (Hex), Address A₁₅ is a "Don't Care".

⁽²⁾ Page Write consists of loading up to 128 bytes (A₈ - A₀).

⁽³⁾ Alternate 6 byte Software Product ID Command Code

Notes for Software Product ID Command Code:

1. With A₁₄-A₁=0; SST Manufacturer Code = BFH, is read with A₈ = 0,
29EE512 Device Code = 5DH, is read with A₈ = 1.
2. The device does not remain in Software Product ID Mode if powered down.
3. This product supports both the JEDEC standard 3 byte command code sequence and SST's original 6 byte command code sequence. For new designs, SST recommends that the 3 byte command code sequence be used.

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Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential	-0.5V to $V_{CC} + 0.5V$
Transient Voltage (<20 ns) on Any Pin to Ground Potential	-1.0V to $V_{CC} + 1.0V$
Voltage on A_9 Pin to Ground Potential	-0.5V to 14.0V
Package Power Dissipation Capability ($T_a = 25^\circ C$)	1.0W
Through Hole Lead Soldering Temperature (10 Seconds)	300°C
Surface Mount Lead Soldering Temperature (3 Seconds)	240°C
Output Short Circuit Current ⁽¹⁾	100 mA

Note: ⁽¹⁾ Outputs shorted for no more than one second. No more than one output shorted at a time.

Operating Range

Range	Ambient Temp	V_{CC}
Commercial	0 °C to +70 °C	5V±10%
Industrial	-40 °C to +85 °C	5V±10%

AC Conditions of Test

Input Rise/Fall Time.....	10 ns
Output Load.....	1 TTL Gate and $C_L = 100$ pF
See Figures 13 and 14	

Table 5: DC Operating Characteristics

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{CC}	Power Supply Current Read		30	mA	$CE\#=OE\#=V_{IL}, WE\#=V_{IH}$, all I/Os open, Address input = V_{IL}/V_{IH} , at $f=1/T_{RC}$ Min., $V_{CC}=V_{CC}$ Max
	Write		50	mA	$CE\#=WE\#=V_{IL}, OE\#=V_{IH}, V_{CC}=V_{CC}$ Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		3	mA	$CE\#=OE\#=WE\#=V_{IH}, V_{CC}=V_{CC}$ Max.
I_{SB2}	Standby V_{CC} Current (CMOS input)		50	μA	$CE\#=OE\#=WE\#=V_{CC} - 0.3V$. $V_{CC} = V_{CC}$ Max.
I_{LI}	Input Leakage Current		1	μA	$V_{IN} = GND$ to $V_{CC}, V_{CC} = V_{CC}$ Max.
I_{LO}	Output Leakage Current		10	μA	$V_{OUT} = GND$ to $V_{CC}, V_{CC} = V_{CC}$ Max.
V_{IL}	Input Low Voltage		0.8	V	$V_{CC} = V_{CC}$ Max.
V_{IH}	Input High Voltage	2.0		V	$V_{CC} = V_{CC}$ Max.
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = 2.1$ mA, $V_{CC} = V_{CC}$ Min.
V_{OH}	Output High Voltage			V	$I_{OH} = -400\mu A, V_{CC} = V_{CC}$ Min.
V_H	Supervoltage for A_9	11.6	12.4	V	$CE\# = OE\# = V_{IL}, WE\# = V_{IH}$
I_H	Supervoltage Current for A_9		200	μA	$CE\# = OE\# = V_{IL}, WE\# = V_{IH},$ $A_9 = V_H$ Max.



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Table 6: Power-up Timings

Symbol	Parameter	Maximum	Units
$T_{PU-READ}^{(1)}$	Power-up to Read Operation	100	μ s
$T_{PU-WRITE}^{(1)}$	Power-up to Write Operation	5	ms

Table 7: Capacitance ($T_a = 25\text{ }^\circ\text{C}$, $f=1\text{ Mhz}$, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}^{(1)}$	I/O Pin Capacitance	$V_{I/O} = 0V$	12 pF
$C_{IN}^{(1)}$	Input Capacitance	$V_{IN} = 0v$	6 pF

Note: ⁽¹⁾This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 8: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	1,000 & 10,000 ⁽²⁾	Cycles	MIL-STD-883, Method 1033
$T_{DR}^{(1)}$	Data Retention	100	Years	MIL-STD-883, Method 1008
$V_{ZAP_HBM}^{(1)}$	ESD Susceptibility Human Body Model	1000	Volts	JEDEC Standard A114
$V_{ZAP_MM}^{(1)}$	ESD Susceptibility Machine Model	200	Volts	JEDEC
$I_{LTH}^{(1)}$	Latch Up	100	mA	JEDEC Standard 17

Note: ⁽¹⁾This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

⁽²⁾See Ordering Information for desired type.

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AC Characteristics

Table 9: Read Cycle Timing Parameters

Symbol	Parameter	29EE512-90		29EE512-120		Units
		Min	Max	Min	Max	
T _{RC}	Read Cycle Time	90		120		ns
T _{CE}	Chip Enable Access Time		90		120	ns
T _{AA}	Address Access Time		90		120	ns
T _{OE}	Output Enable Access Time		40		50	ns
T _{CLZ} ⁽¹⁾	CE# Low to Active Output	0		0		ns
T _{OLZ} ⁽¹⁾	OE# Low to Active Output	0		0		ns
T _{CHZ} ⁽¹⁾	CE# High to High-Z Output		30		30	ns
T _{OHZ} ⁽¹⁾	OE# High to High-Z Output		30		30	ns
T _{OH} ⁽¹⁾	Output Hold from Address Change	0		0		ns

Table 10: Page-Write Cycle Timing Parameters

Symbol	Parameter	Min	Max	Units
T _{WC}	Write Cycle (erase and program)		10	ms
T _{AS}	Address Setup Time	0		ns
T _{AH}	Address Hold Time	50		ns
T _{CS}	WE# and CE# Setup Time	0		ns
T _{CH}	WE# and CE# Hold Time	0		ns
T _{OES}	OE# High Setup Time	0		ns
T _{OEH}	OE# High Hold Time	0		ns
T _{CP}	CE# Pulse Width	70		ns
T _{WP}	WE# Pulse Width	70		ns
T _{DS}	Data Setup Time	35		ns
T _{DH}	Data Hold Time	0		ns
T _{BLC} ⁽¹⁾	Byte Load Cycle Time	0.05	100	μs
T _{BLCO} ⁽¹⁾	Byte Load Cycle Time	200		μs
T _{IDA}	Software ID Access and Exit Time		10	μs
T _{SCE}	Software Chip Erase		20	ms

Note: ⁽¹⁾This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.



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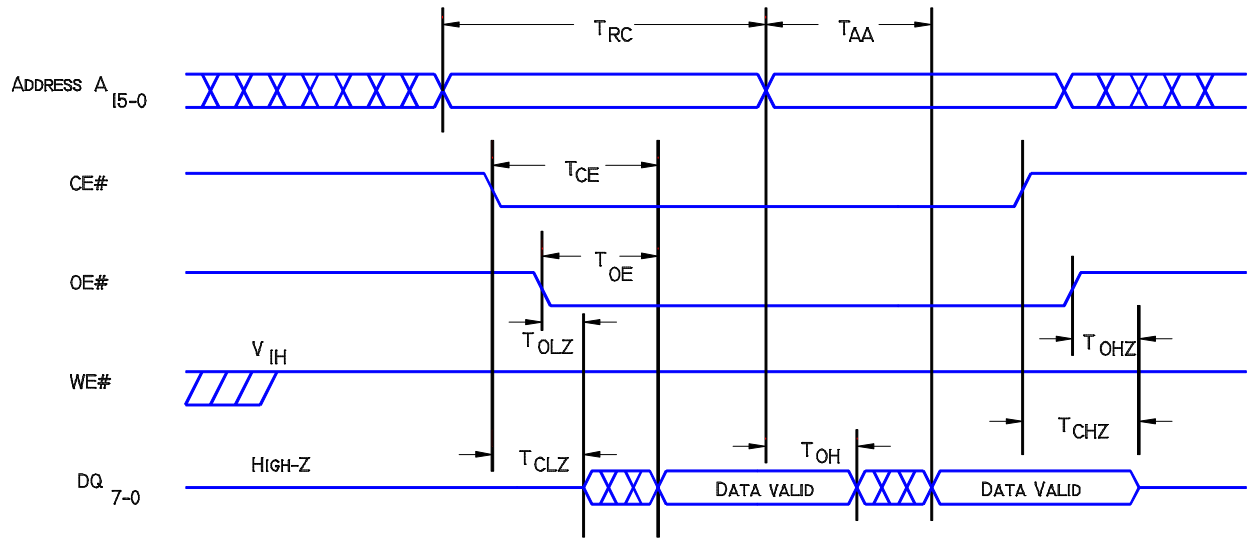


Figure 3: Read Cycle Timing Diagram

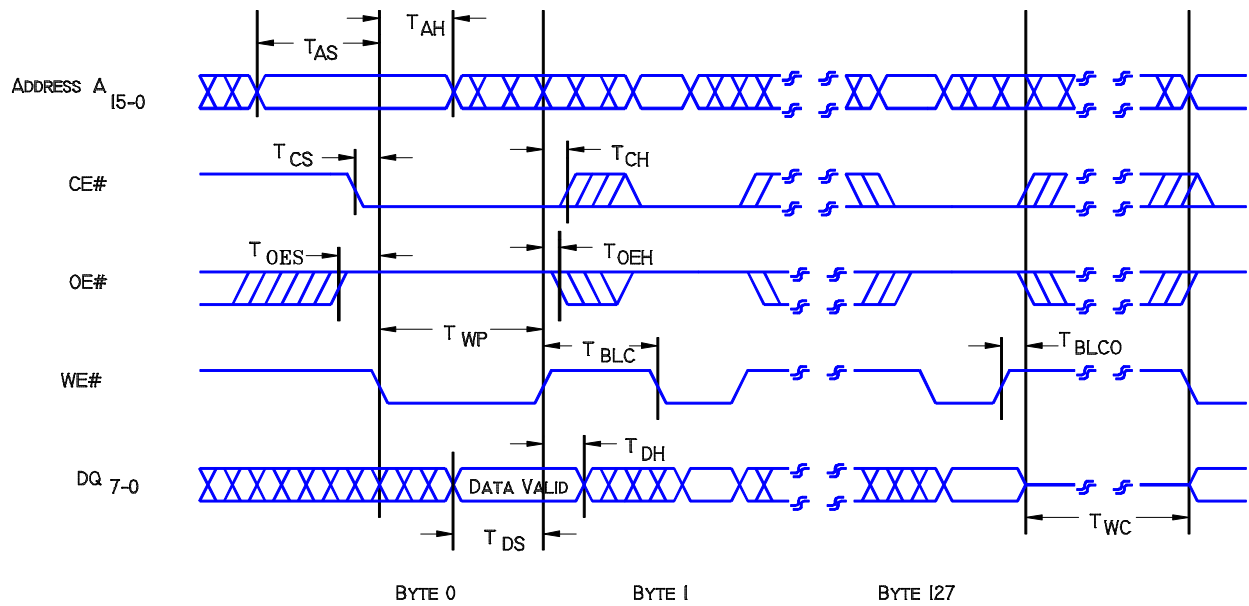


Figure 4: WE# Controlled Page Write Cycle Timing Diagram

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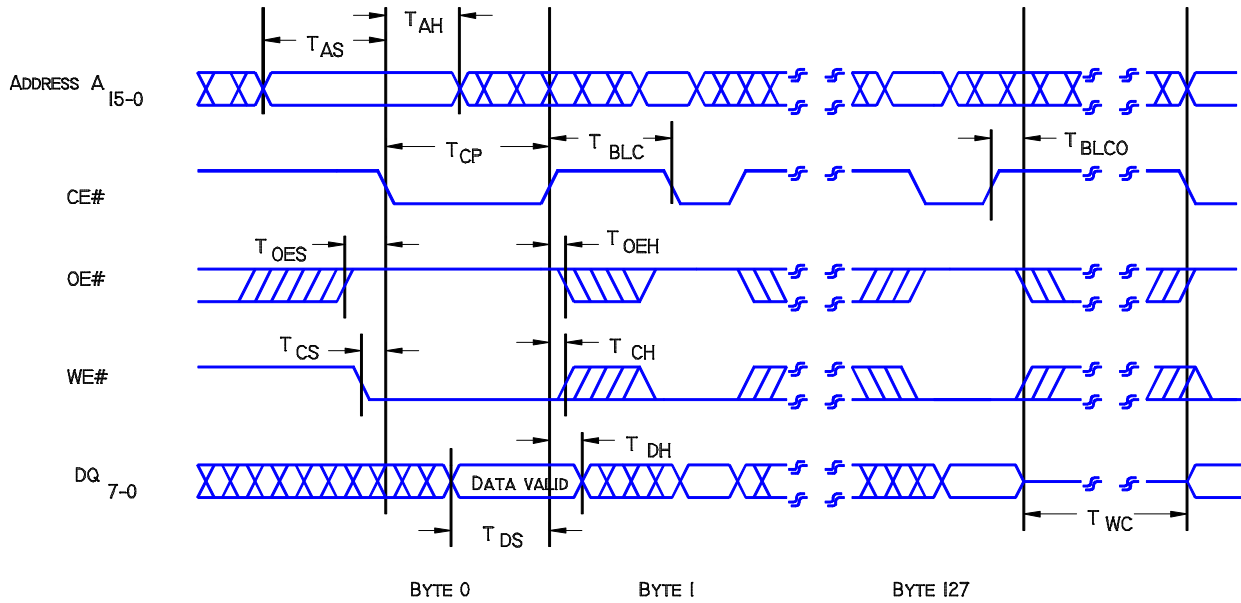


Figure 5: CE# Controlled Page Write Cycle Timing Diagram

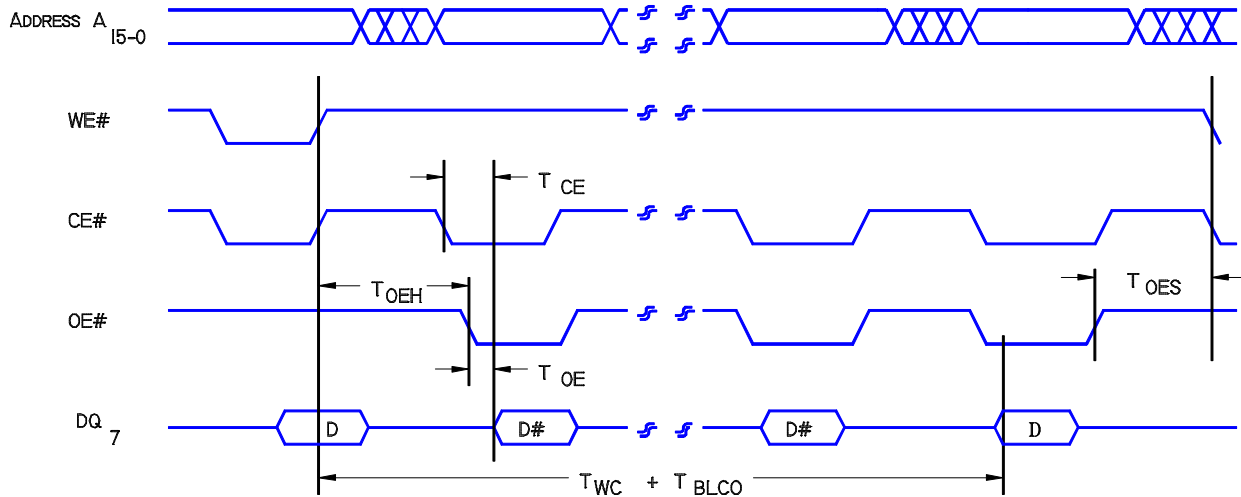


Figure 6: Data# Polling Timing Diagram



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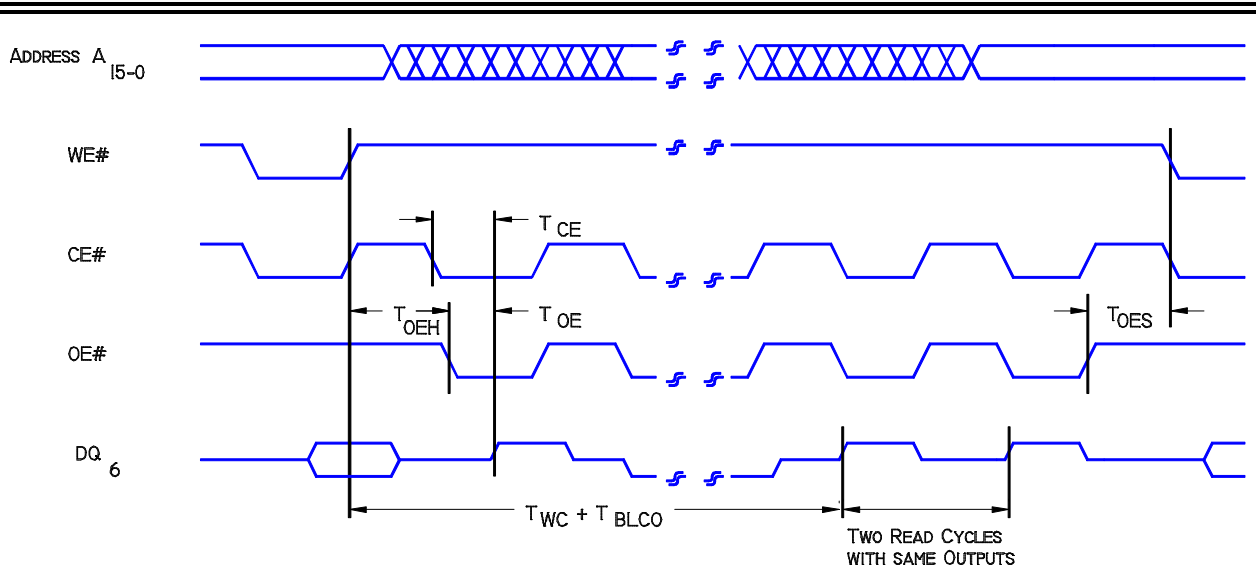


Figure 7: Toggle Bit Timing Diagram

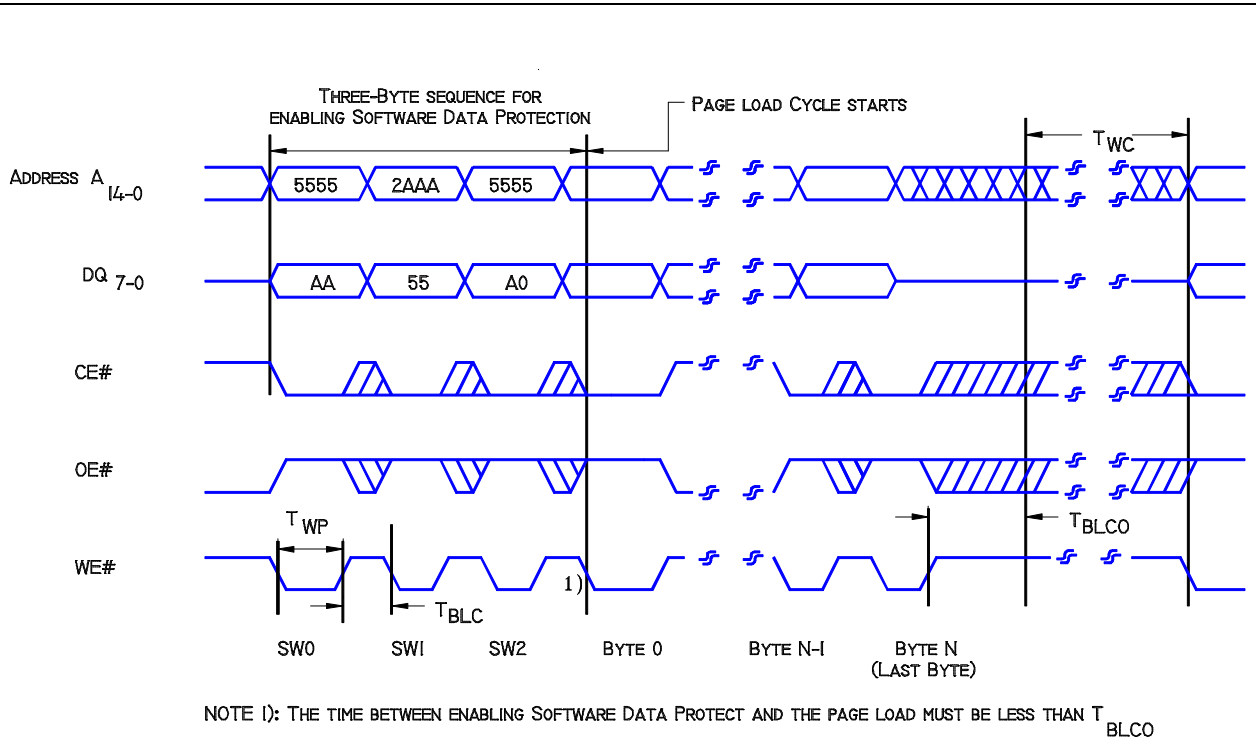


Figure 8: Software Data Protection Page Write Timing Diagram

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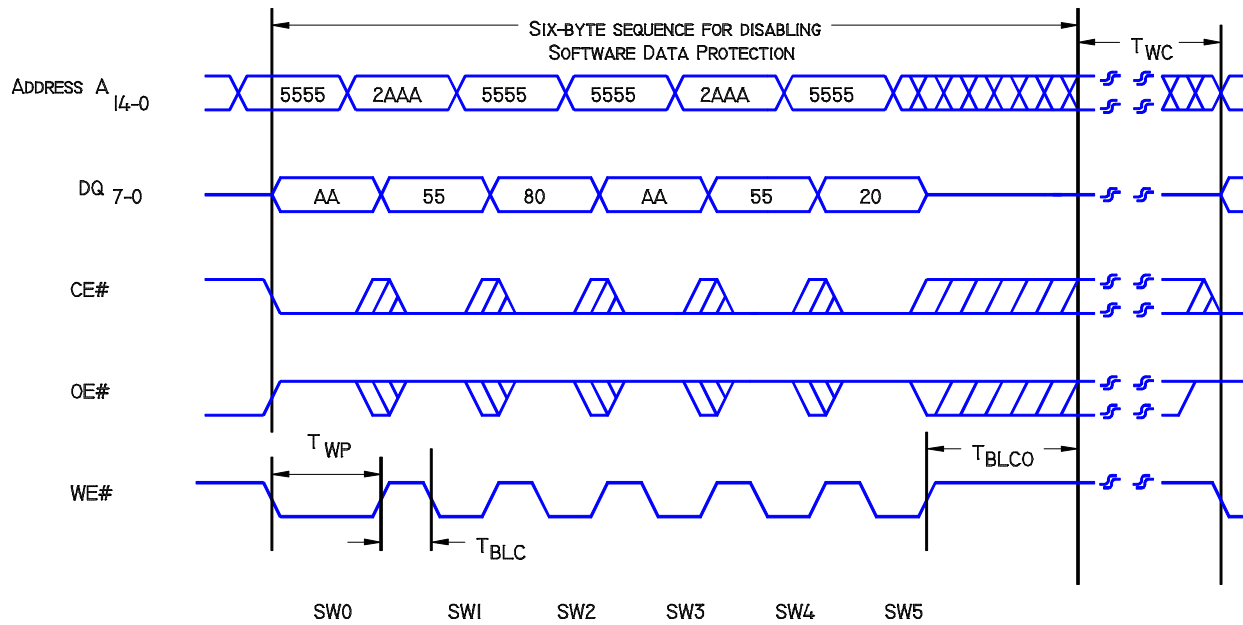


Figure 9: Software Data Protect Disable Timing Diagram

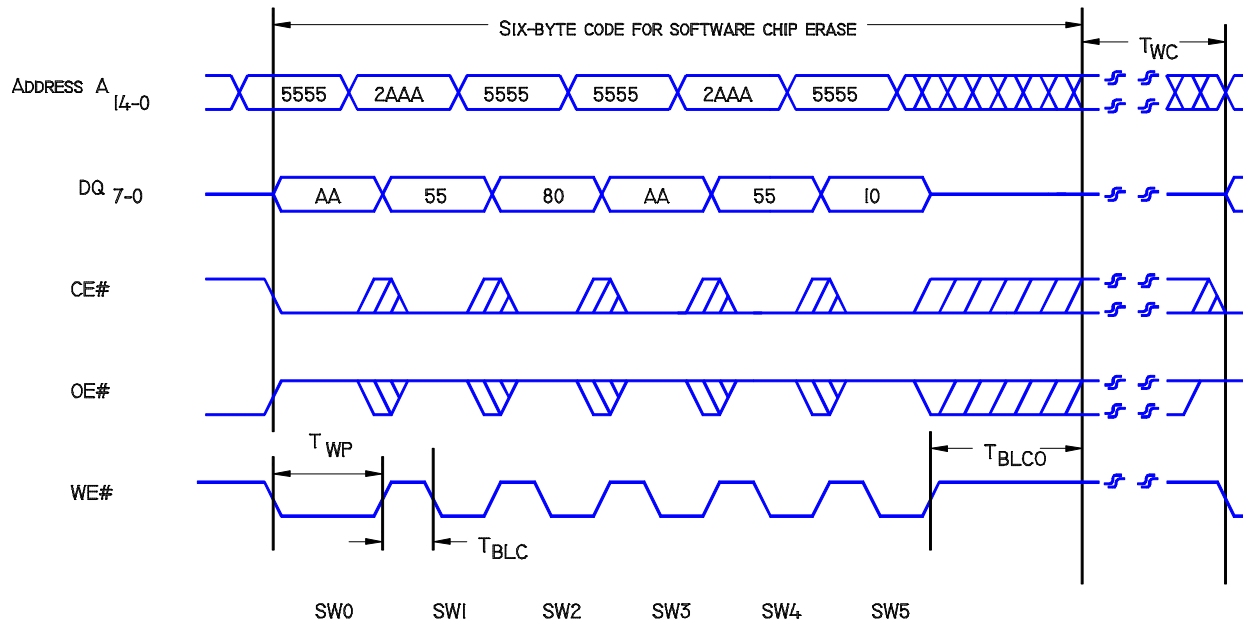


Figure 10: Software Chip Erase Timing Diagram



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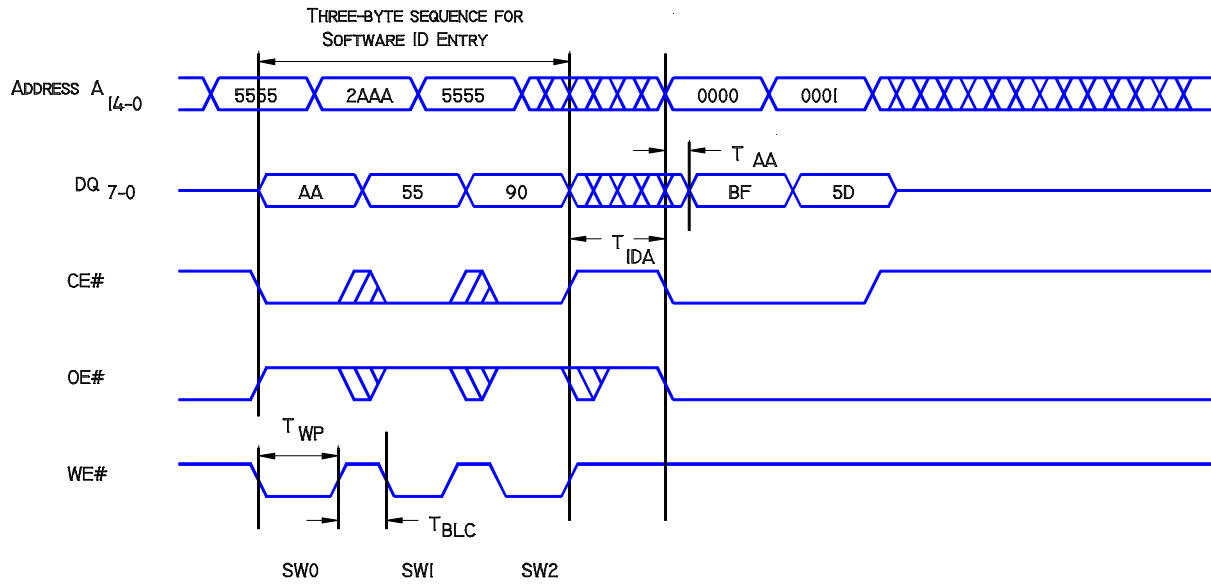


Figure 11: Software ID Entry and Read

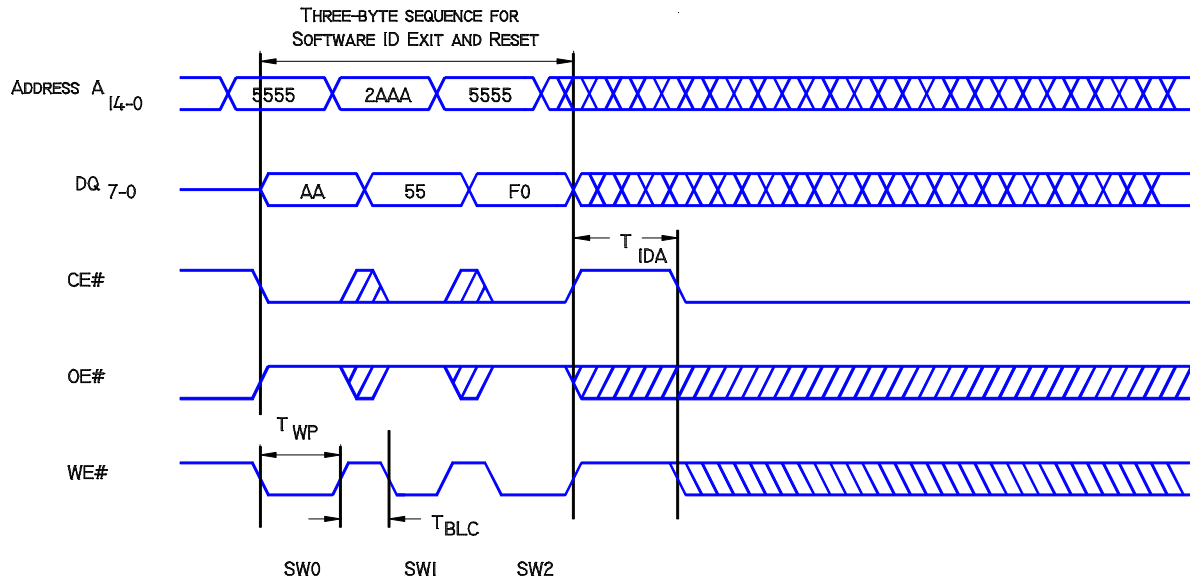
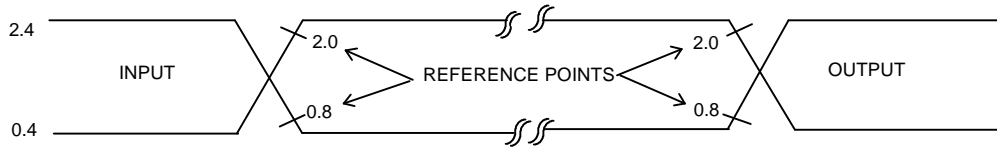


Figure 12: Software ID Exit and Reset

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AC test inputs are driven at V_{OH} ($2.4 V_{TTL}$) for a logic "1" and V_{OL} ($0.4 V_{TTL}$) for a logic "0". Measurement reference points for inputs and outputs are V_H ($2.0 V_{TTL}$) and V_{IL} ($0.8 V_{TTL}$). Inputs rise and fall times (10% \leftrightarrow 90%) are <10 ns.

Figure 13: AC Input/Output Reference Waveforms

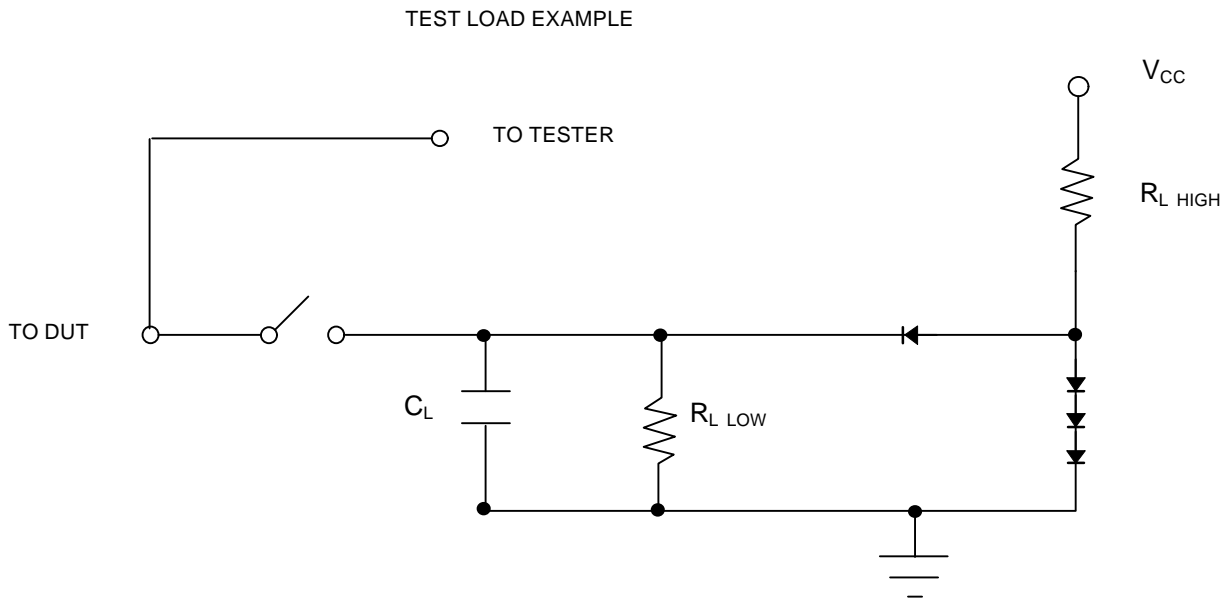


Figure 14: Test Load Example



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See Figure 17

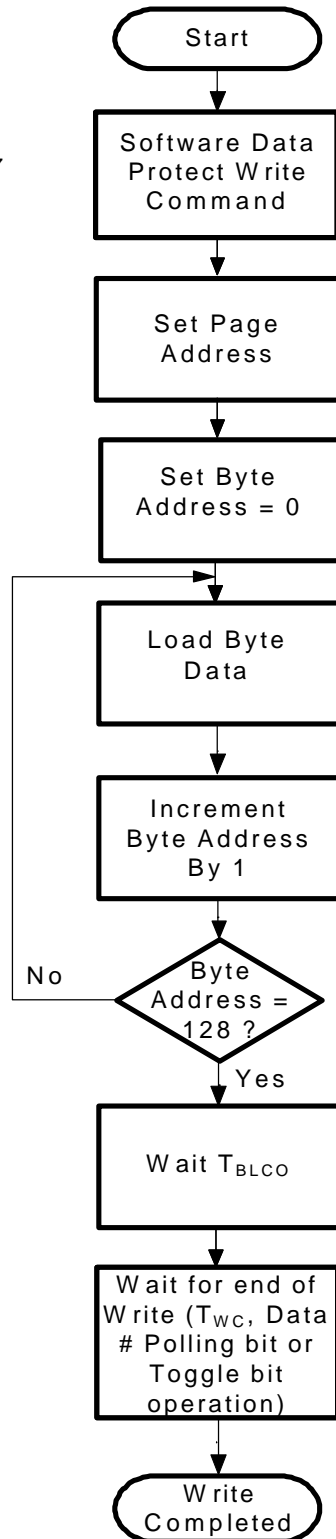


Figure 15: Write Algorithm

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5.0V-only 512 Kilobit
Page Mode EEPROM

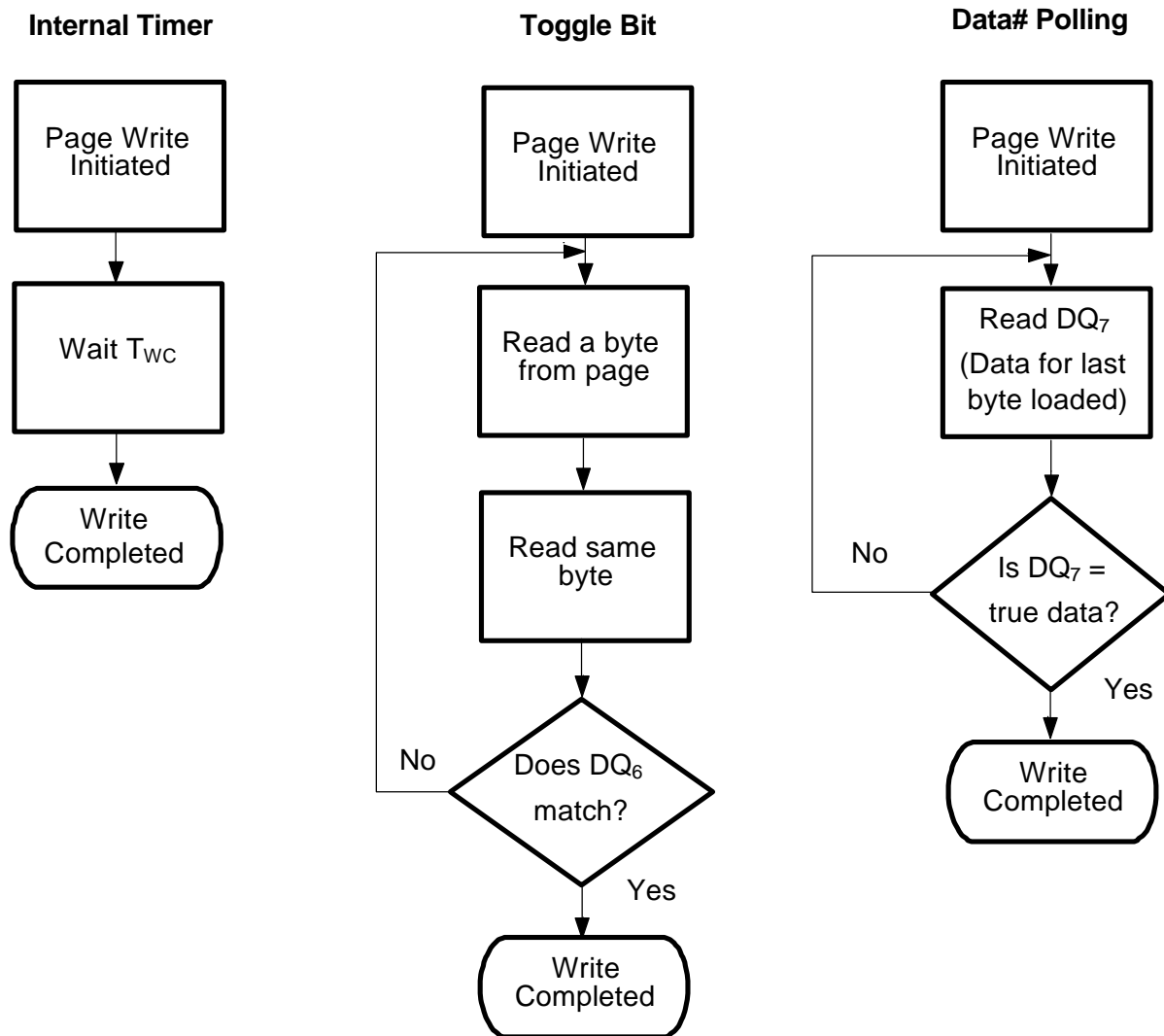


Figure 16: Wait Options



SST 29EE512

5.0V-only 512 Kilobit

Page Mode EEPROM

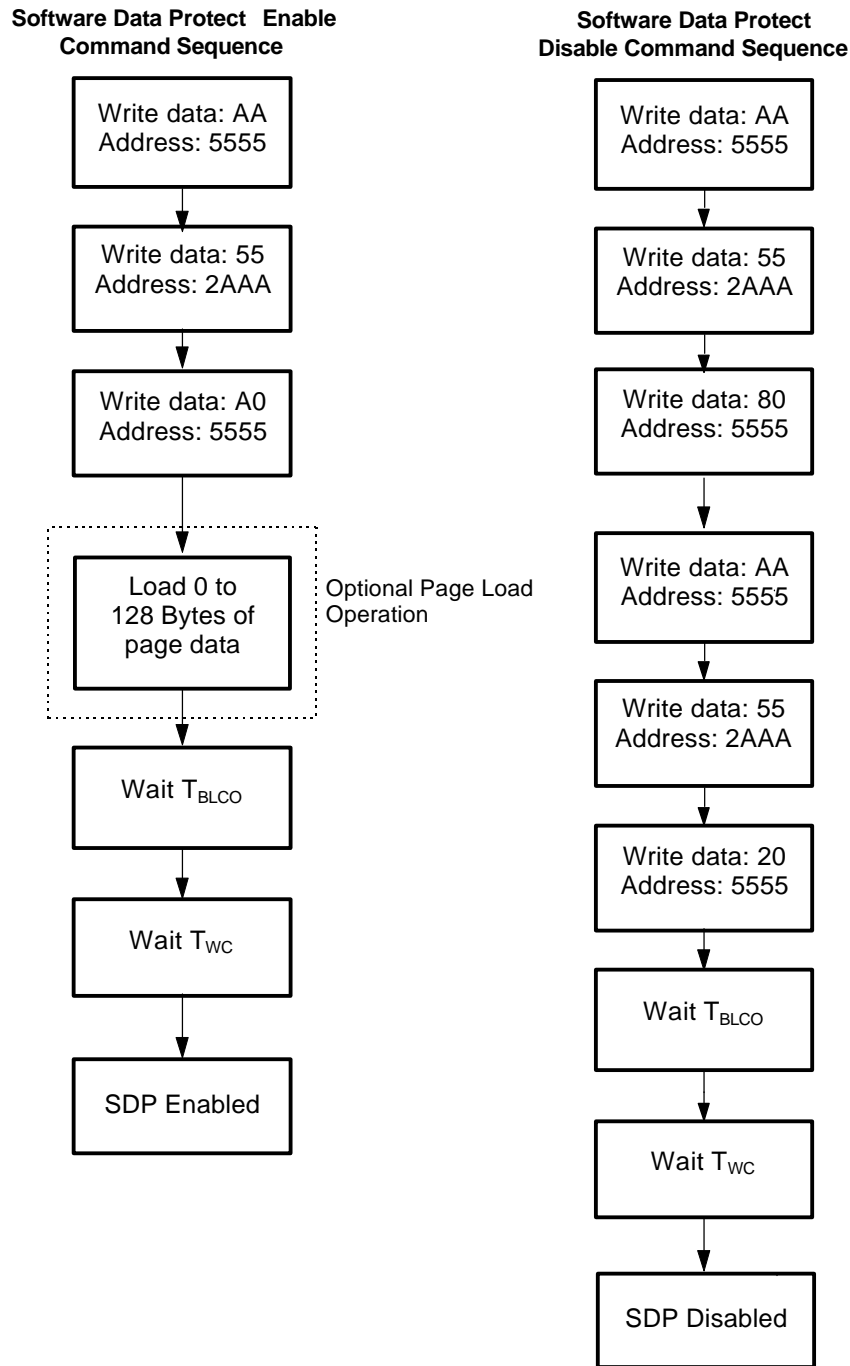
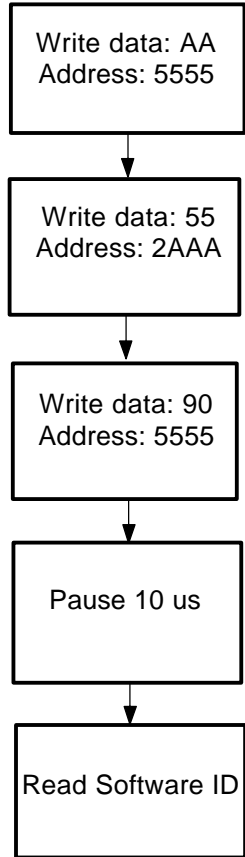


Figure 17: Software Data Protection Flowcharts

SST 29EE512
5.0V-only 512 Kilobit
Page Mode EEPROM



**Software Product ID Entry
Command Sequence**



**Software Product ID Exit &
Reset Command Sequence**

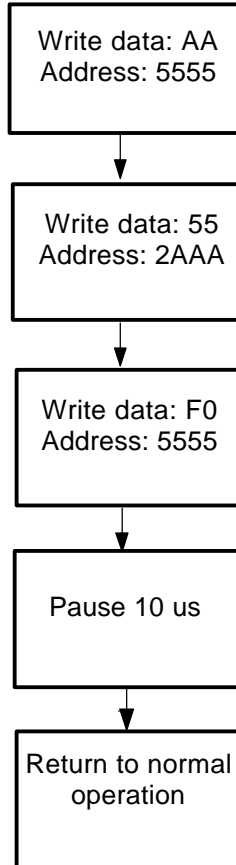


Figure 18: Software Product Command Flowcharts



SST 29EE512

5.0V-only 512 Kilobit

Page Mode EEPROM

Software Chip-Erase Command Sequence

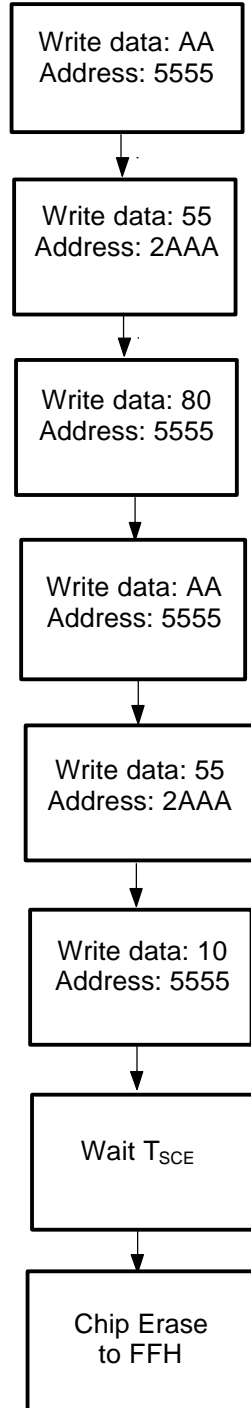


Figure 19: Software Chip Erase Command Codes

SST 29EE512

5.0V-only 512 Kilobit

Page Mode EEPROM



Product Ordering Information

Device	Speed	Suffix1	Suffix2	
SST29EE512	- XXX	- XX	- XX	
				<p>Package Modifier H = 32 leads Numeric = Die modifier</p> <p>Package Type P = PDIP N = PLCC E = TSOP (die up) U = Unencapsulated die</p> <p>Operating Temperature C = Commercial = 0° to 70°C I = Industrial = -40° to 85°C</p> <p>Minimum Endurance 3 = 1000 cycles 4 = 10,000 cycles</p> <p>Read Access Speed 120 = 120 ns 90 = 90 ns</p>



SST 29EE512 5.0V-only 512 Kilobit Page Mode EEPROM

Valid combinations

SST29EE512- 90-4C- EH	SST29EE512- 90-4C- NH	SST29EE512- 90-4C- PH
SST29EE512-120-4C- EH	SST29EE512-120-4C- NH	SST29EE512-120-4C- PH
SST29EE512- 90-3C- EH	SST29EE512- 90-3C- NH	SST29EE512- 90-3C- PH
SST29EE512-120-3C- EH	SST29EE512-120-3C- NH	SST29EE512-120-3C- PH
SST29EE512- 90-4I-EH	SST29EE512- 90-4I-NH	
SST29EE512-120-4I-EH	SST29EE512-120-4I-NH	SST29EE512-120-4C-U1
SST29EE512- 90-3I-EH	SST29EE512- 90-3I-NH	
SST29EE512-120-3I-EH	SST29EE512-120-3I-NH	SST29EE512-120-3C-U1

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.