SIEMENS

ICs for Communications

S/T Bus Interface Circuit Extended
SBCX

PEB 2081 Version 3.4

User's Manual 11.96

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Introduction

The PEB 2081 S/T Bus Interface Circuit Extended (SBCX) implements the four-wire S/T-interface used to link voice/data ISDN terminals, network terminators and PABX trunk lines to a Central Office.

The SBCX provides the electrical and functional link between the analog S/T-interface according to ITU recommendation I.430, ETS 300 012 and T1.605 Basic User Network Interface Specification respectively, and the ISDN Oriented Modular interface Rev. 2 (IOM-2).

This manual is divided into 6 major sections. Compared to previous data sheets for the S transceiver, the organization of the data sheet for version 3.4 has been modified in order to make information more readily available to the user.

Section 1 gives the user an introduction to the PEB 2081 Vers. 3.4. It contains information about the functional blocks, features and pinning of the SBCX.

Section 2 provides an overview of typical ISDN applications and demonstrates how these applications can be realized with the PEB 2081 Vers. 3.4.

Sections 3 and **4** are identical in structure. Both cover the major S transceiver topics “Interfaces”, “Control Procedures” and “Maintenance Functions”. **Section 3** gives the user an overview on the discussed topics without going into technical details. It is intended as an application guide where the user can quickly look up how the registers of ICC, EPIC and SBCX Vers. 3.4 need to be programmed in order to initiate the desired action.

Section 4 is dedicated to detailed technical information. Status diagrams, state descriptions, algorithms, dynamic characteristics are to be found here. **Section 4** thus is intended for the user who seeks specific technical information.

Section 5 summarizes all electrical, **section 6** all environmental characteristics.

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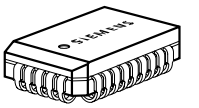
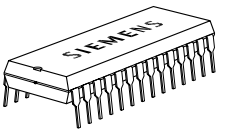
S/T Bus Interface Circuit Extended — PEB 2081

1 Features

- Full duplex 2B+D S/T-interface transceiver according to the following specifications:
  - ITU Recommendation I.430
  - ETS 300 012
  - ANSI T1.605
- 192 kbit/s transmission rate
- Pseudo-ternary coding with 100 % pulse width
- Activation and deactivation procedures
- Extended loop-length up to 2 km



P-LCC-28-1



P-DIP-28-3

IOM®-2 Interface

- Optimized for operation in conjunction with IEC-Q, IBC, ICC, EPIC and IDEC telecom ICs
- Handling of commands and indications contained in the IOM-2 C/I channel for activation, deactivation and testing
- Switching of test-loops

Modes

- TE : Terminal Mode
- NT : Network termination connected to IEC-Q
- LT-T : Trunk mode in private exchange
- LT-S : Line termination in public or private exchanges

Special Features

- Fully compliant NT2 trunk mode including multipoint operation
- Frame alignment with absorption of phase wander in NT2 network side applications
- D channel access control, also in trunk application
- Access to S and Q bits of S/T-interface (S1, S2 and Q channel)
- Software controlled maintenance interface (I/O ports)
- Switching of test loops
- Advanced CMOS technology with low power consumption:
  power down max. 4 mW
  operational max. 60 mW

Type	Ordering Code	Package
PEB 2081P	Q67100-H6581	P-DIP-28-3
PEB 2081N	Q67100-H6580	P-LCC-28-1

1.1 Pin Configuration

(top view)

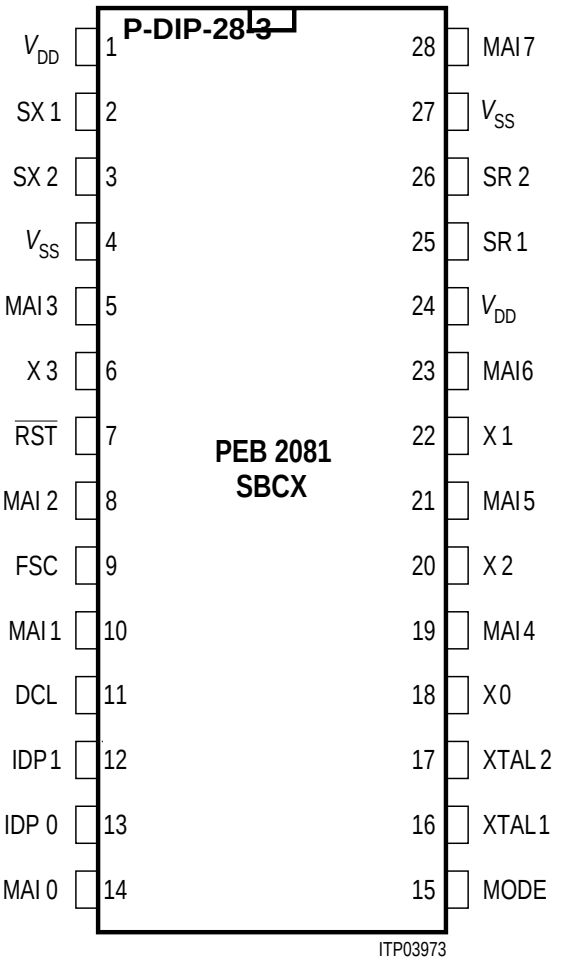


Figure 1
PEB 2081 SBCX in P-DIP-28-3 and P-LCC-28-1 Packages

1.2 Pin Definition and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
11	DCL	I/O	Data Clock The frequency is equal to twice the data rate on the IOM-2 interface. **LT-S, LT-T, NT:** clock input 512 kHz to 8192 kHz **TE:** clock output 1536 kHz
9	FSC	I/O	Frame Synchronization Clock **LT-S, LT-T, NT:** clock input 8 kHz **TE:** clock output 8 kHz
13	IDP0	I/O	IOM-2 data port 0; open drain with an external pull up resistor, otherwise push/pull
12	IDP1	I/O	IOM-2 data port 1; open drain (if external pull up resistor at IDP0), otherwise push/pull
25	SR1	I	Differential S/T-interface receiver signal input
26	SR2	I	Differential S/T-interface receiver signal input
2	SX1	O	Differential S/T-interface positive transmitter output
3	SX2	O	Differential S/T-interface negative transmitter output
15	MODE	I	Setting of either LT modes or NT and TE mode
6 20 22 18	X3 X2 X1 X0	I/O I I I/O	Specific function pins dependent from the selected operating mode
28, 23, 21, 19	MAI (7:4)	O	Maintenance Auxiliary Interface; output pins
5	MAI 3	I	Maintenance Auxiliary Interface; input pin
8, 10, 14	MAI (2:0)	I/O	Maintenance Auxiliary Interface; input/output pins
24	V_{DD}	I	Power supply + 5 V $\pm$ 5 %
1	V_{DD}	I	Power supply + 5 V $\pm$ 5 %
4	V_{SS}	I	Ground
27	V_{SS}	I	Ground
7	$\overline{\text{RST}}$	I	Reset, low active
16	XTAL1	I	Connection for external crystal, or input for external clock generator
17	XTAL2	O	Connection for external crystal, not connected, when an external clock generator is used

1.3 Logic Symbol

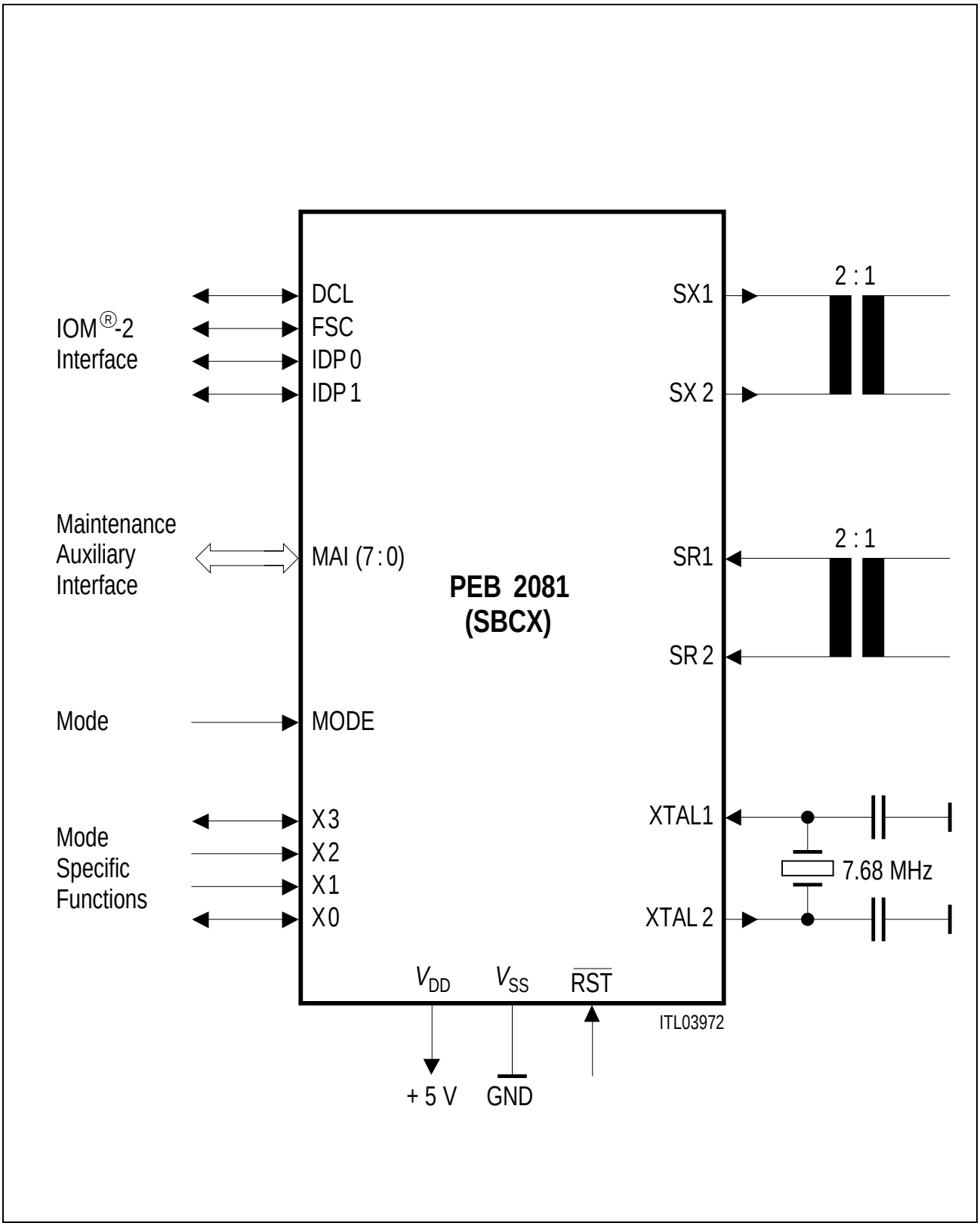


Figure 2
Logic Symbol of the SBCX

1.4 Functional Block Diagram

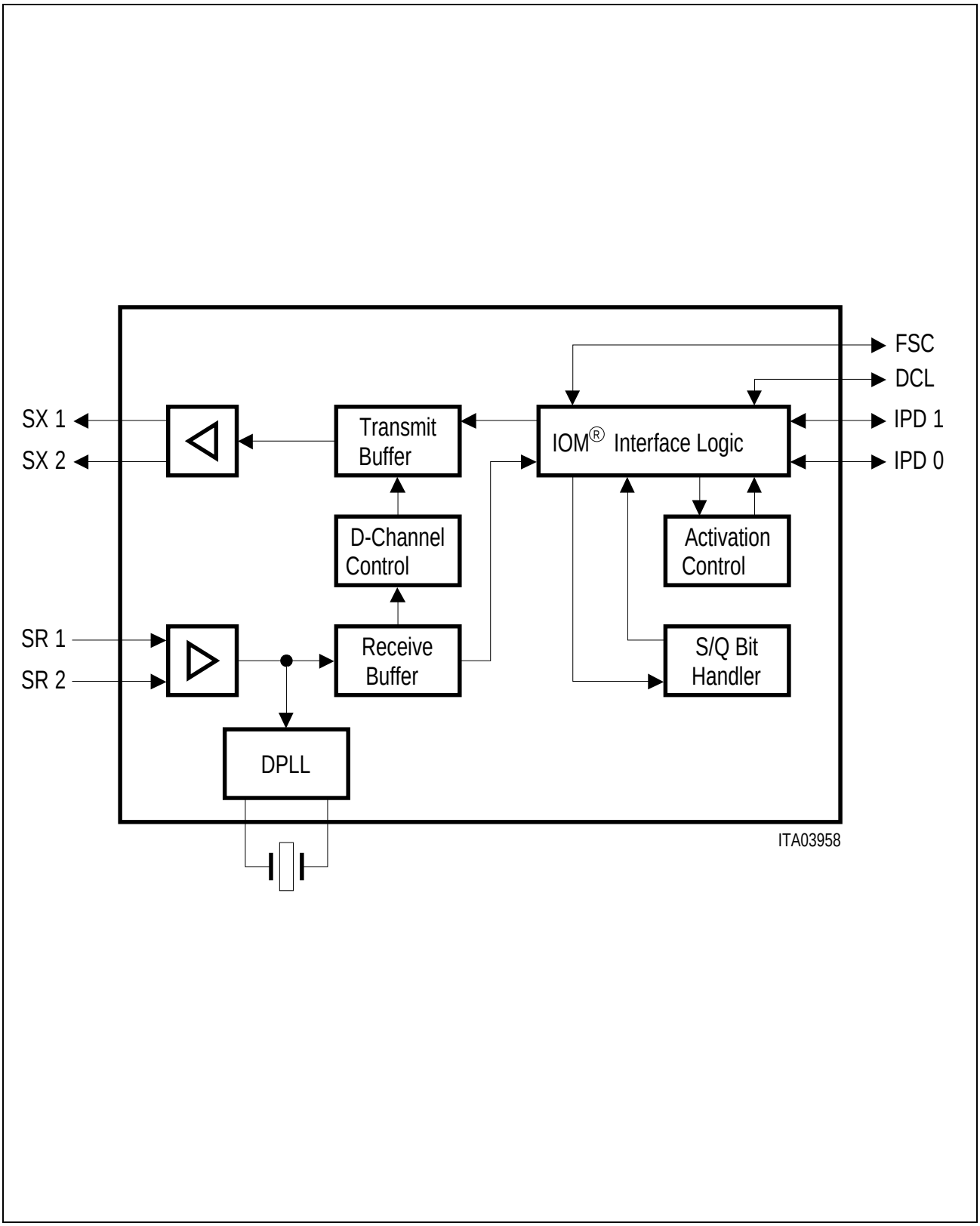


Figure 3
Block Diagram of the SBCX

2 System Integration and Applications

The SBCX implements the four-wire S- and T-interfaces used in the ISDN basic access. By programming the corresponding operating mode it may be used at both ends of these interfaces.

The operating modes are:

- ISDN terminals (TE)
- ISDN network termination (NT) for a link between the four-wire S/T-interface and the two-wire U-interface
- ISDN subscriber line termination (LT-S)
- ISDN trunk line termination (LT-T); (PBX connection to Central Office).

The basic use of these modes is shown in the following figure, where the usual nomenclature as defined by the ITU for the basic access functional blocks and reference points, is used.

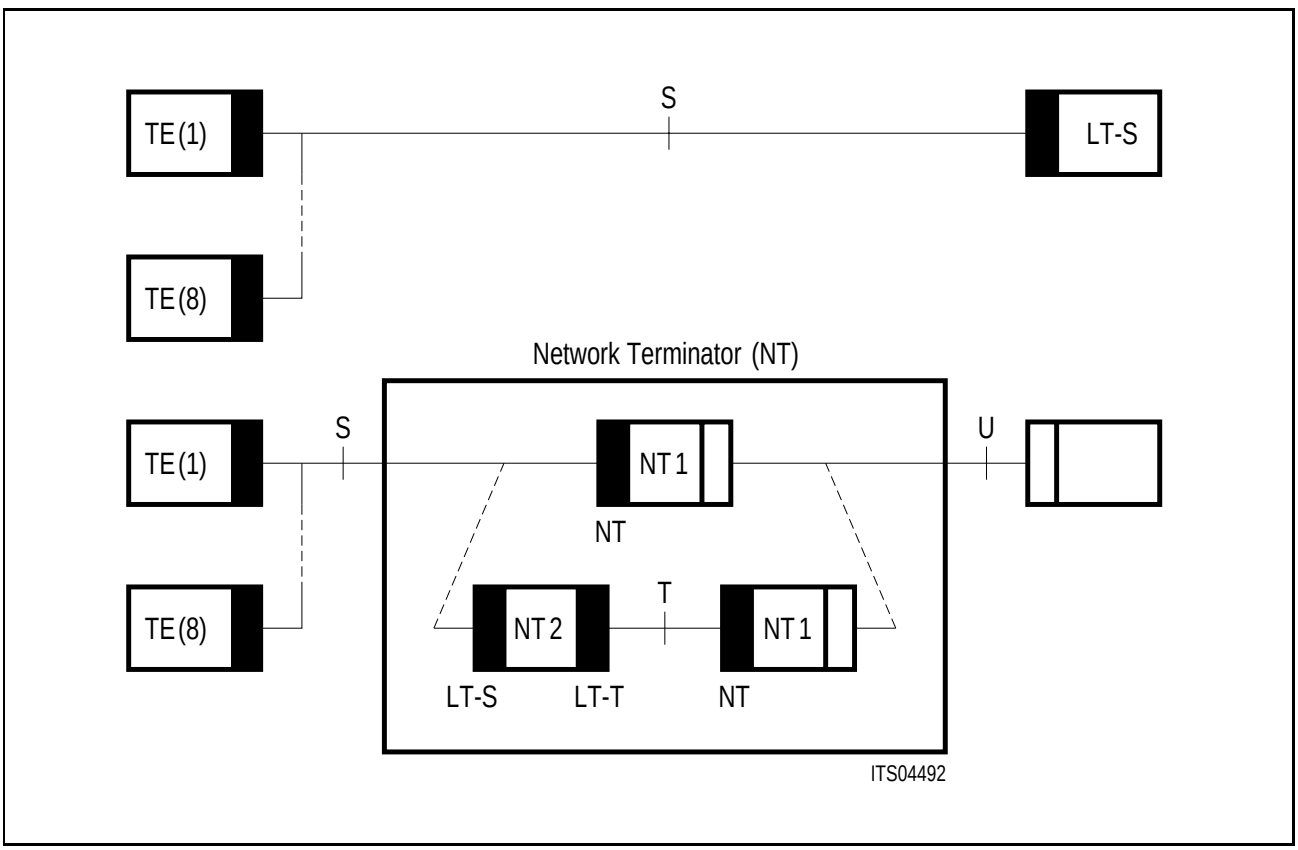


Figure 4
Operating Modes of the SBCX in the ISDN Basic Access Architecture

The NT equipment serves as a converter between the U-interface at the exchange and the S-interface at the user premises. The NT may consist of either an NT1 or an NT1 together with an NT2 connected via the T-interface which is physically identical to the S-interface. The NT1 is a direct transformation between layer 1 of S and layer 1 of U. NT2 may include higher level functions like multiplexing and switching as in a PBX.

2.1 Operational Modes and System Integration

2.1.1 TE Application

In the terminal several IOM-2 compatible devices can be connected to the IOM-2 bus structure (e.g. PEB 2070 ISDN Communications Controller (ICC), PSB 2161 Audio Ringing Codec Filter (ARCOFI®), PSB 2163 Audio Ringing Codec Filter (ARCOFI®SP) and PSB 2110 ISDN Terminal Adapter Circuit (ITAC®)). The ICC allows access to IOM-2 bus by the microcontroller. The SBCX is controlled via MON0 channel, the other devices via MON1 channel of the IOM-2 bus.

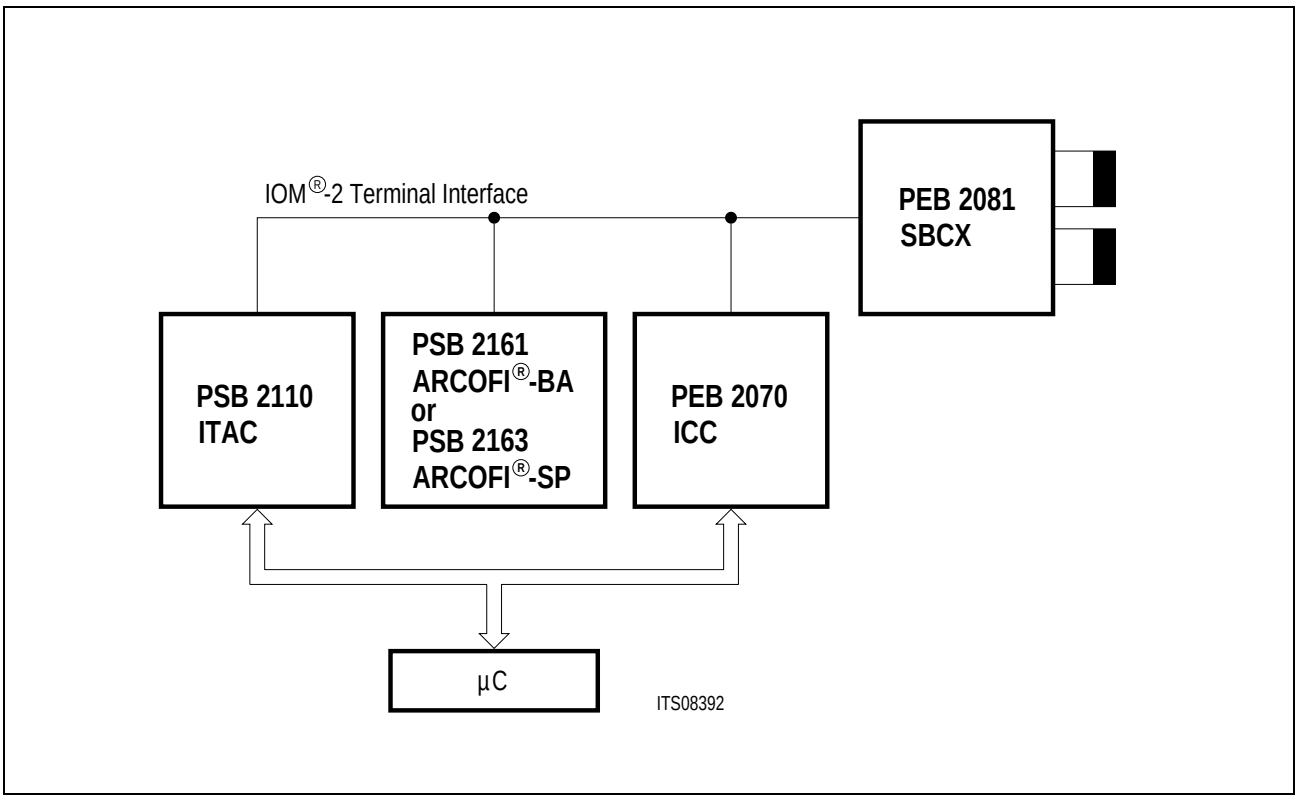


Figure 5
ISDN Voice/Data Terminal using the IOM®-2 Terminal Architecture (TE)

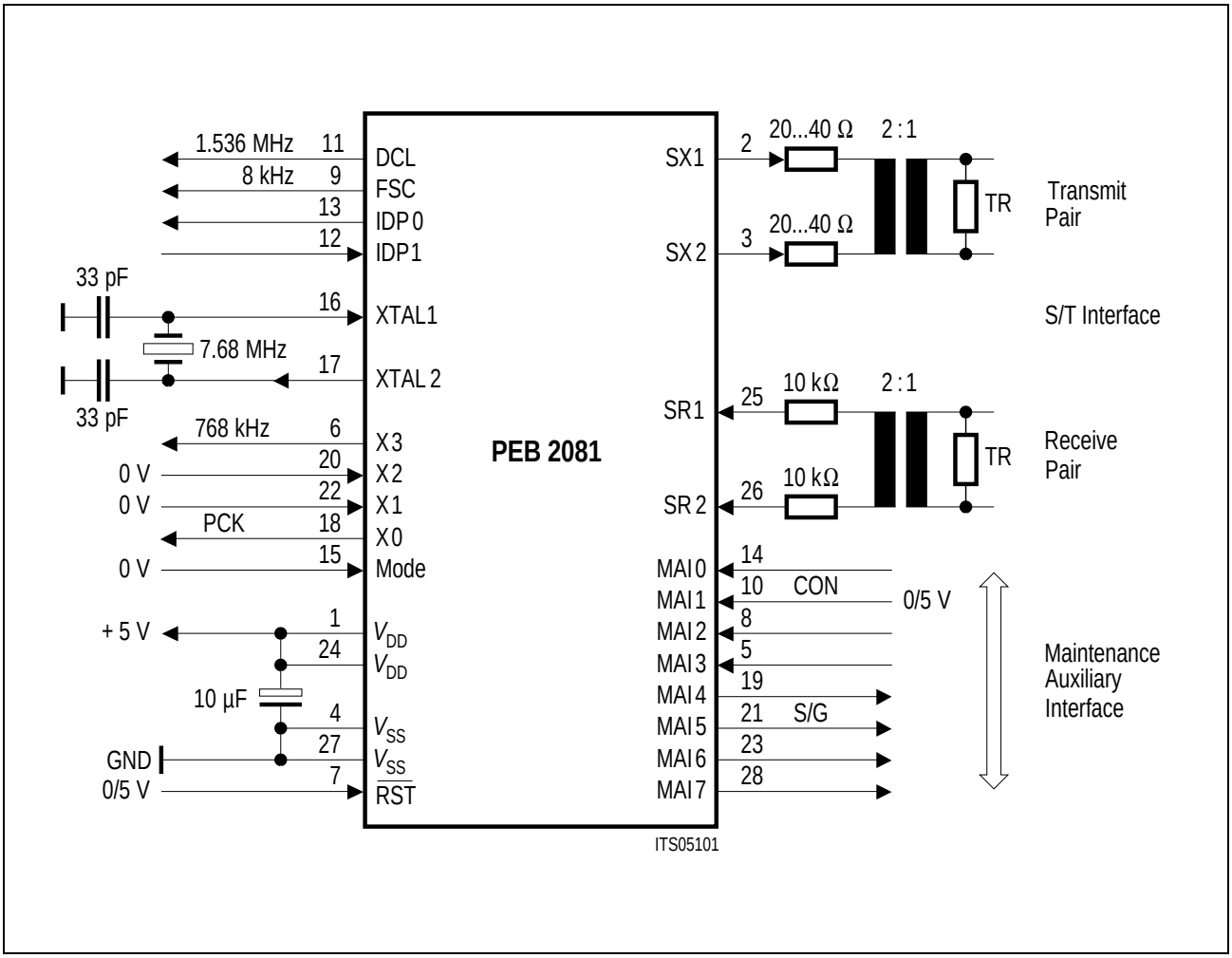


Figure 6
SBCX in TE Mode

2.1.2 ISDN Network Termination (NT1)

The S-interface is a four-wire interface for connecting ISDN Terminal Equipment (TE) and Terminal Adapter (TA) to the Network Termination (NT). From here a twisted pair interfaces to the exchange. The Network Terminator interfaces the four-wire to the two-wire interface.

A basic Network Terminator (NT1) can be built using the SBCX together with the PEB 2091 ISDN Echo-Cancellation Circuit (IEC-Q1) or in case of a private exchange the PEB 2095 ISDN Burst Transceiver Circuit (IBC). All information between S- and U-interface is handled automatically between the layer-1 devices IEC-Q (or IBC) and the SBCX.

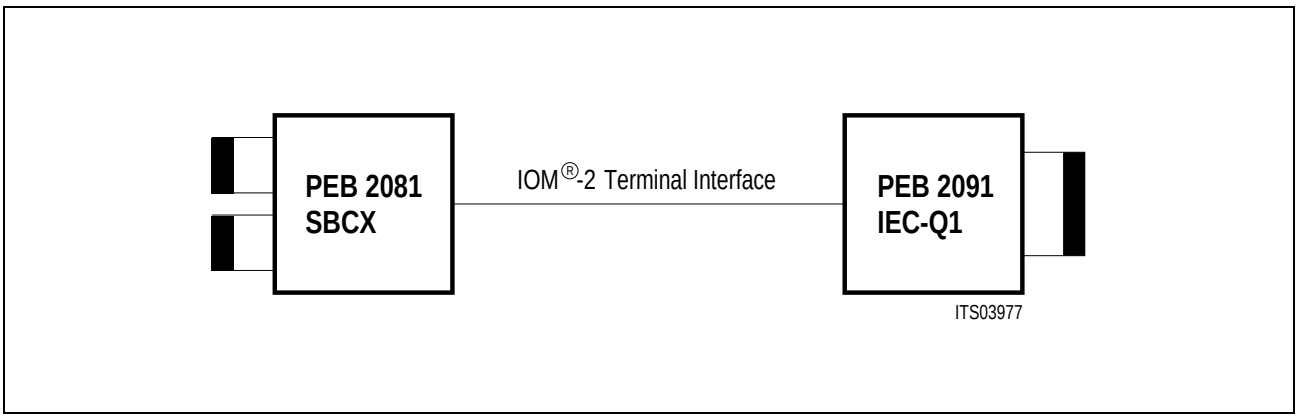


Figure 7
Basic Network Terminator (NT1)

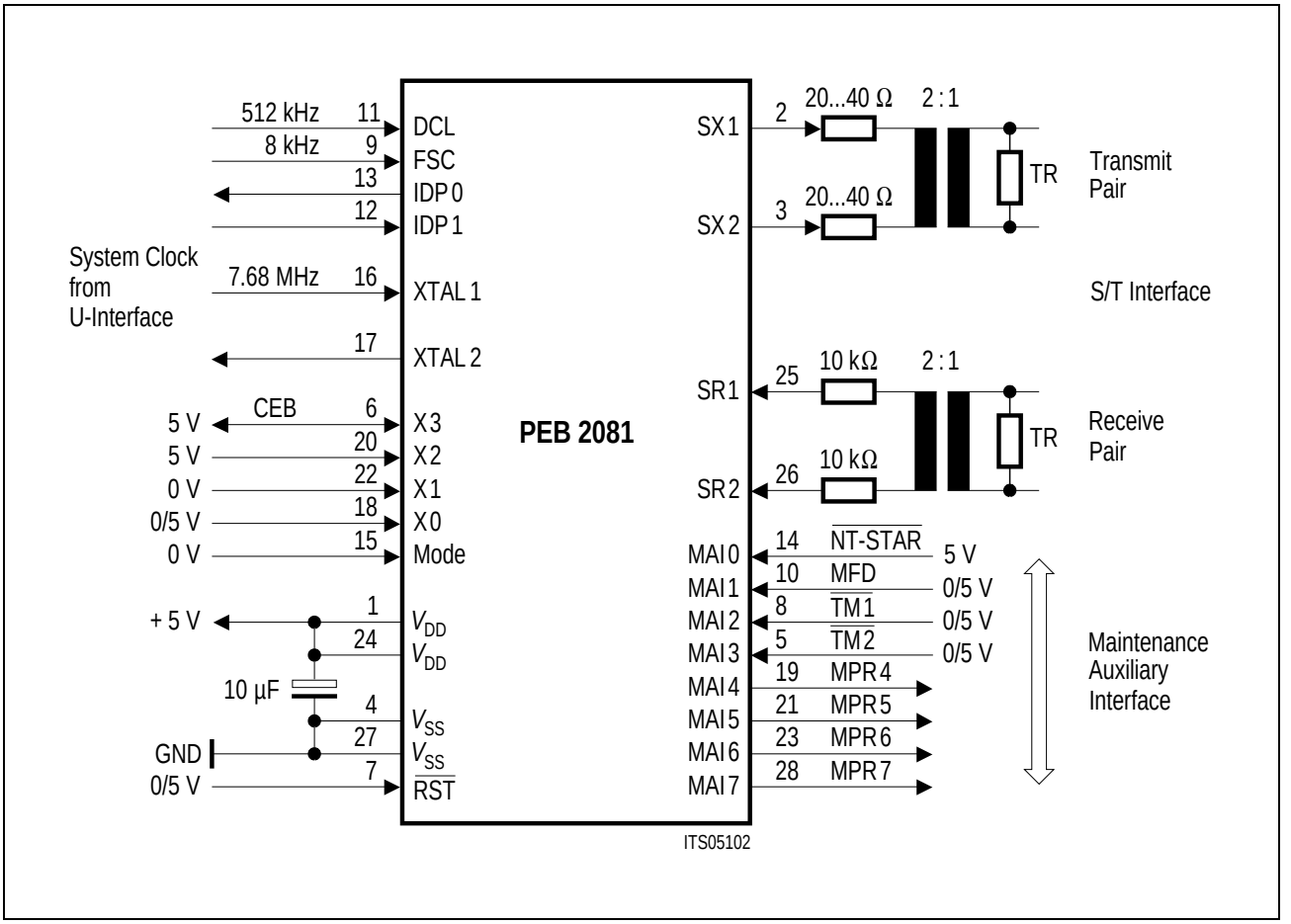


Figure 8
SBCX in NT-Mode

2.1.3 ISDN Network Terminator (NT1) in Star Configuration

A NT-star configuration is used when it is not possible to connect all terminals with a short or extended passive bus configuration. This may be the case if the terminal locations are too far apart to comply to the restrictions specified for short or extended passive bus systems. In this application the IOM-2 interface operates with a DCL frequency of 512 kHz. Downstream data will be transmitted to all connected TEs. The upstream data from all TE's will be wired-ANDed on the IOM-2 interface.

The NT-star mode ensures under these circumstances, the correct D-channel collision detection as well as the correct activation behavior (see also **section 3.3**).

Both point-to-point or passive bus configurations are allowed. A combination of these two configurations is also possible, **see figure 9** and **10**.

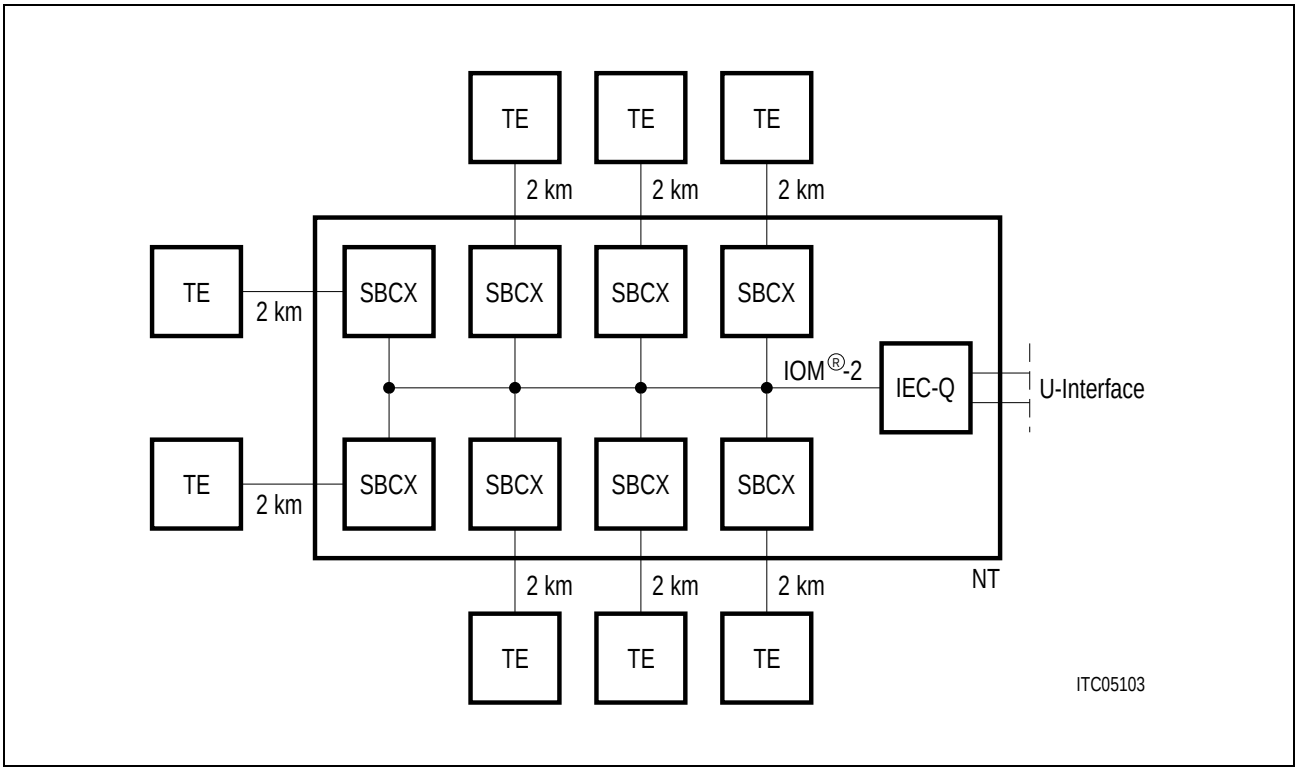


Figure 9
NT-Star Configuration with 8 TEs Connected Point-to-Point

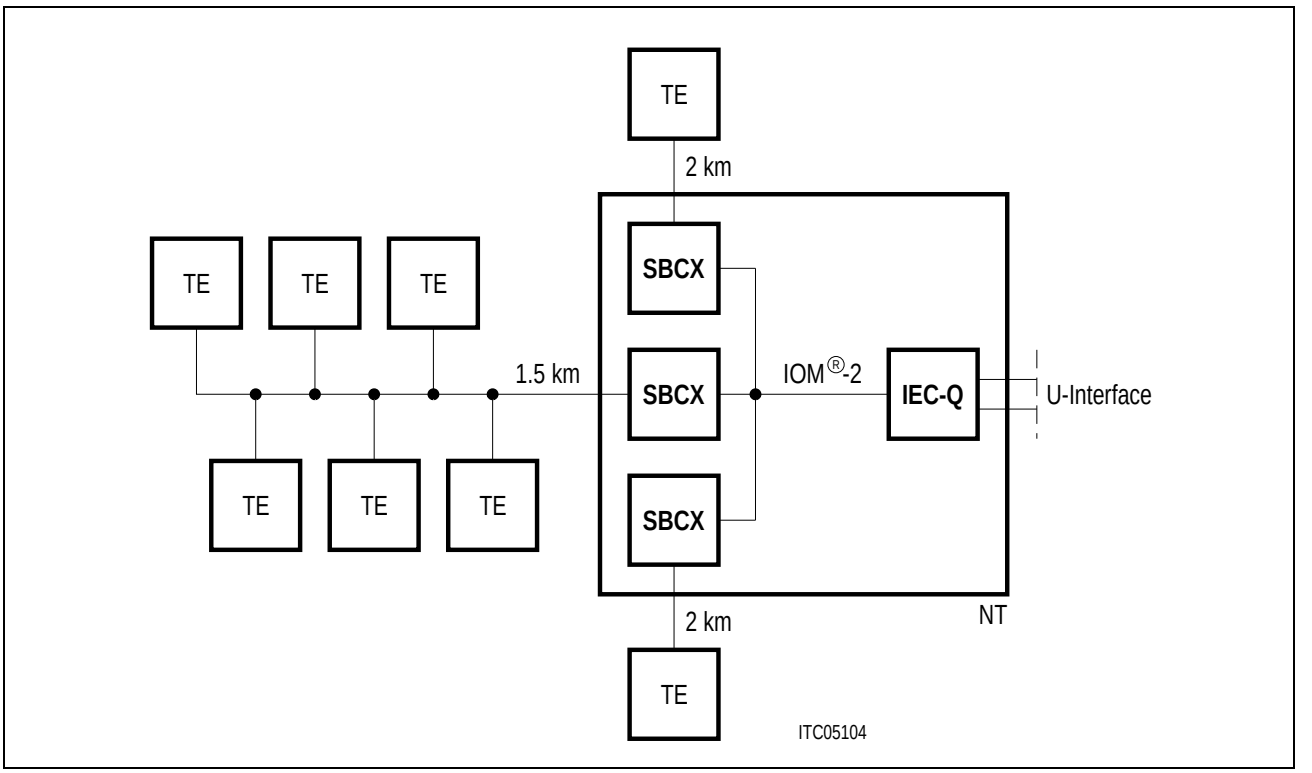


Figure 10
NT-Star Configuration with 2 TEs Connected Point-to-Point and 6 TEs Connected via an Extended Passive Bus

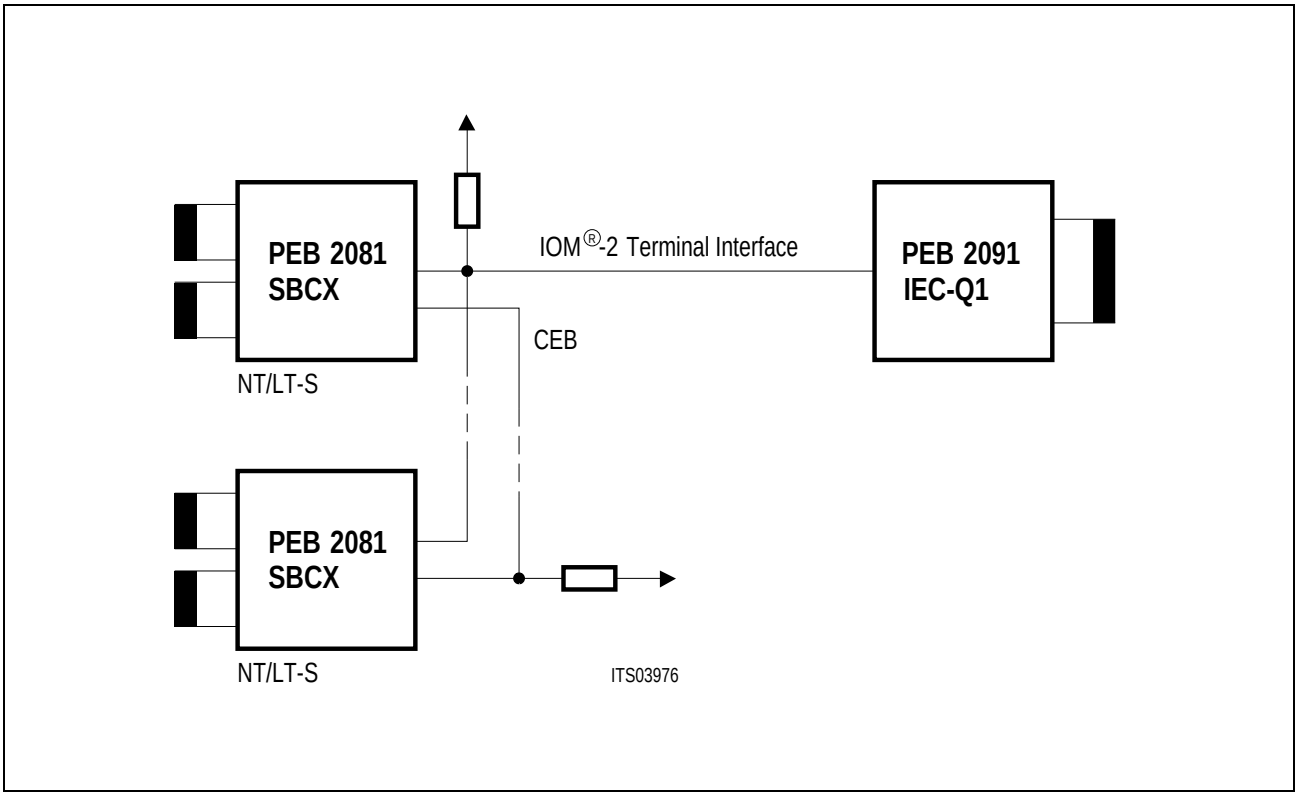


Figure 11
NT-Star Configuration

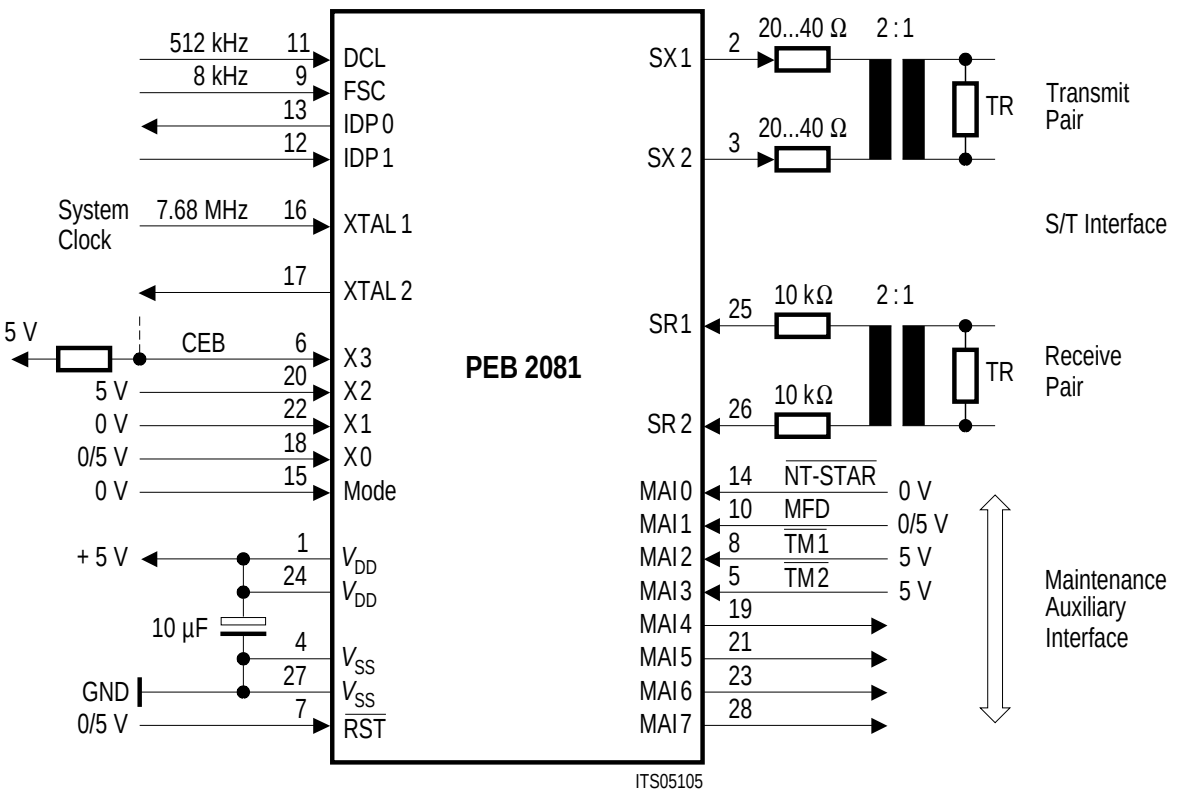


Figure 12
SBCX in NT-Star Mode

2.1.4 ISDN Network Terminator Using IOM®-2 Architecture (Intelligent NT)

The IOM-2 architecture allows to build a **micro controlled NT** using additionally the ICC and operating the IEC-Q (or IBC) in the IOM-2 terminal mode. The ICC provides software controlled layer-1 maintenance function such as programming the SBCX via the monitor channel.

The SBCX is set to LT-S mode and is operated in the IOM-2 channel 1 of the IOM-2 terminal architecture. For that purpose the SBCX offers the possibility of changing the state machine from LT-S mode to NT mode (refer to FSMM-bit of the configuration register) in order to behave like a Network Termination with only two devices (NT1).

The SBCX provides the required IOM-2 channel switching functions (B1, B2, D and C/I) for this application. To ensure a proper wake up procedure of a micro controlled NT being in power down (case of a deactivated line) the asynchronous timing bit (AST-bit of the loop-back register) should be set.

The U- and S/T-interface maintenance data is conveyed via the IOM-2 interface's monitor channel to the ICC.

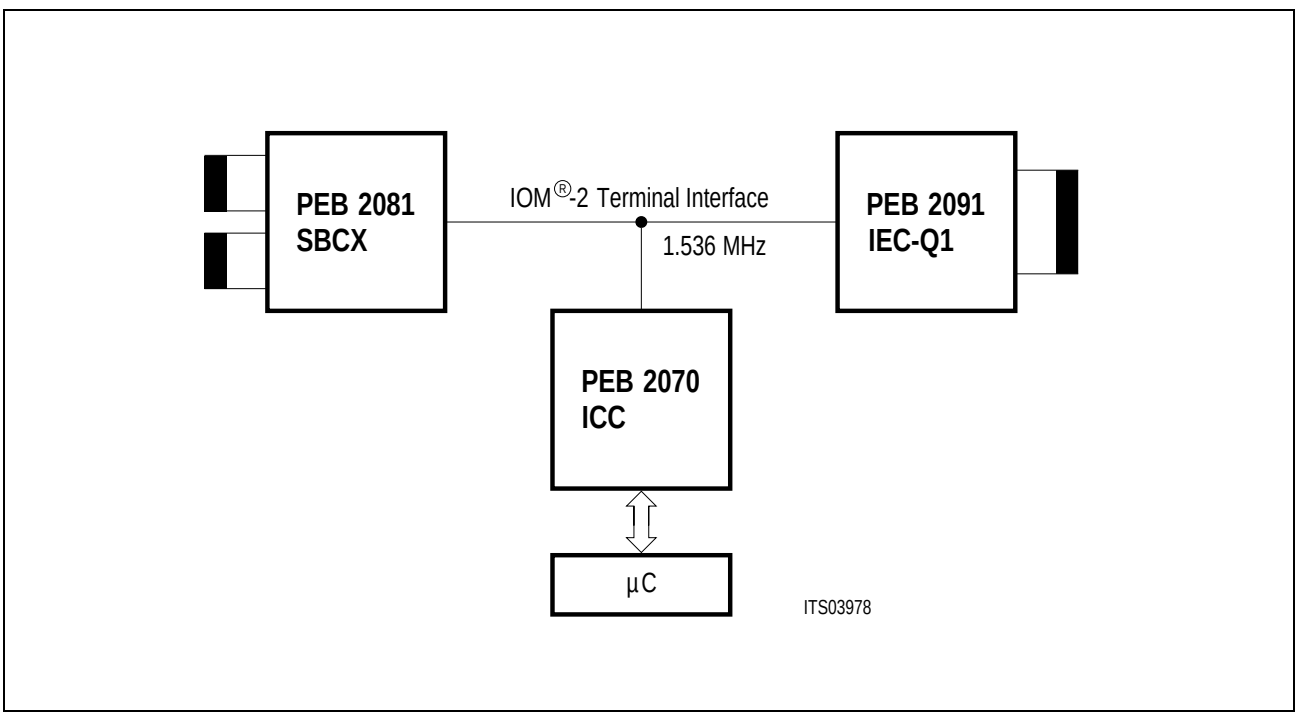


Figure 13
Micro Controlled NT Configuration

The S-interface is the standard ISDN subscriber interface, but in a PBX environment also an U-interface (e.g. IBC or IEC-Q) may be used for the connection of a subscriber resulting in an U-interface terminal with an S/T-extension (**Intelligent NT**). The Intelligent NT can be seen as an enhancement of the micro controlled NT.

In this case the SBCX is treated as an additional IOM-2 device. The ICC accesses the IBC or IEC-Q via MON0 channel, the other devices via MON1 channel.

The functionality of such a configuration includes D-channel collision resolution in upstream direction (TIC bus) and IOM-2 channel switching functions for internal communication.

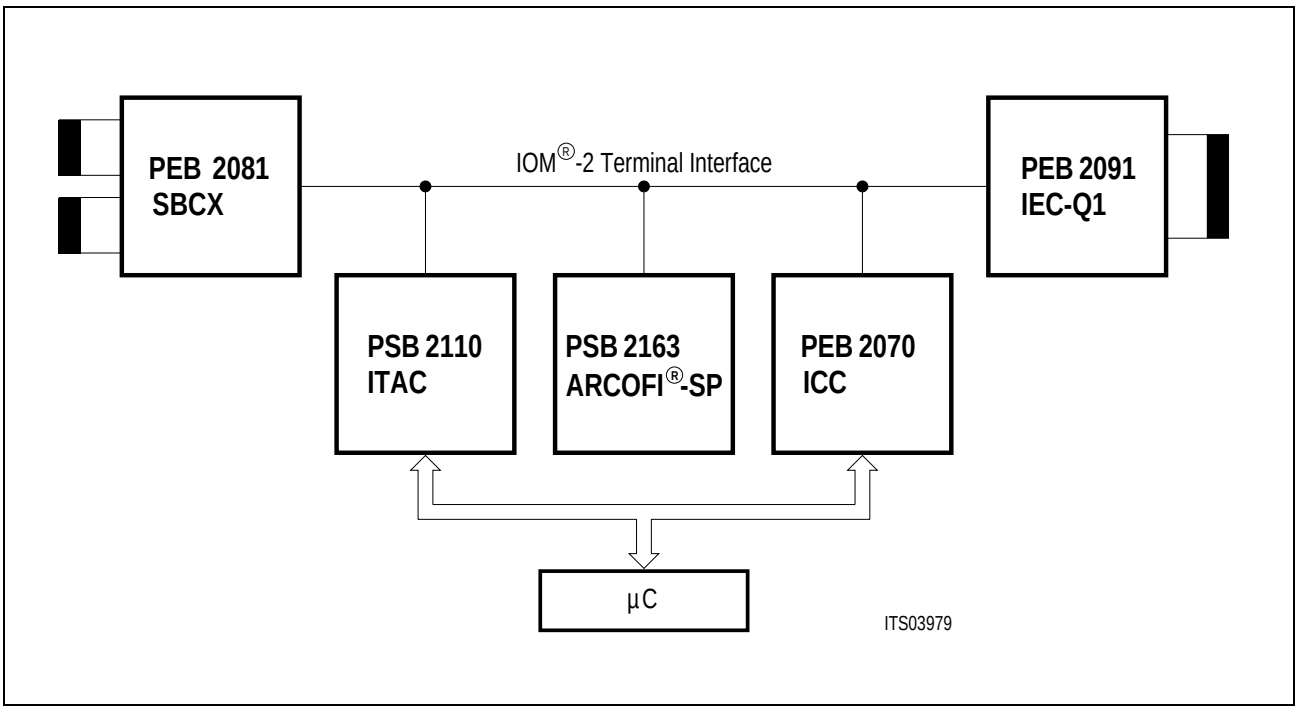


Figure 14
Intelligent NT Providing both Terminal (voice/data) and Network Terminating Functions (S/T-interface)

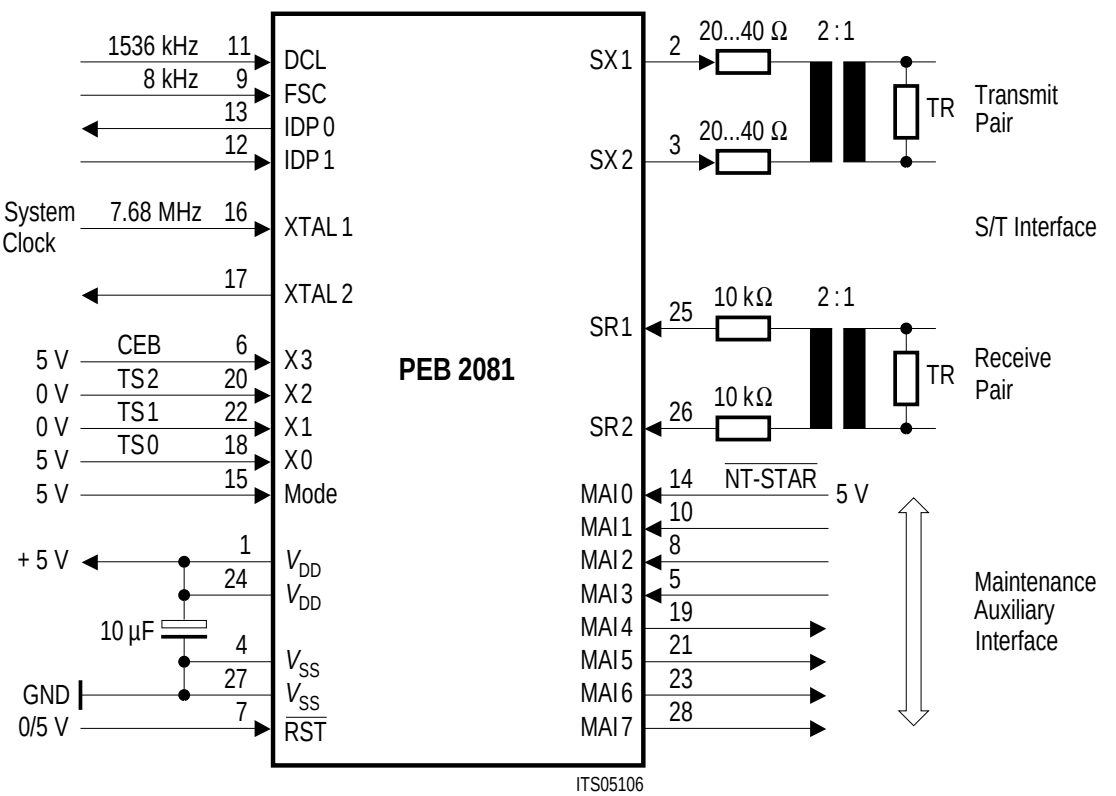


Figure 15
SBCX in LT-S Mode for Intelligent NT Configurations

2.1.5 Line Card Application (one D-channel controller per line)

The SBCX supports a line card implementation both in an ISDN Subscriber Line Termination LT-S) and in an ISDN Trunk Line Termination (LT-T) using e.g. the PEB 2055 Extended PCM Interface Controller (EPIC®-1). Up to eight devices can be connected to the IOM-2 interface. This application requires a data clock of 4.096 MHz. The standard implementation of a S/T-interface line card includes one D-channel controller, e.g. PEB 2075 ISDN D-Channel Exchange Controller (IDEC®), per line for decentralized D-channel handling. **Figure 16** illustrates this configuration for line cards on the exchange side.

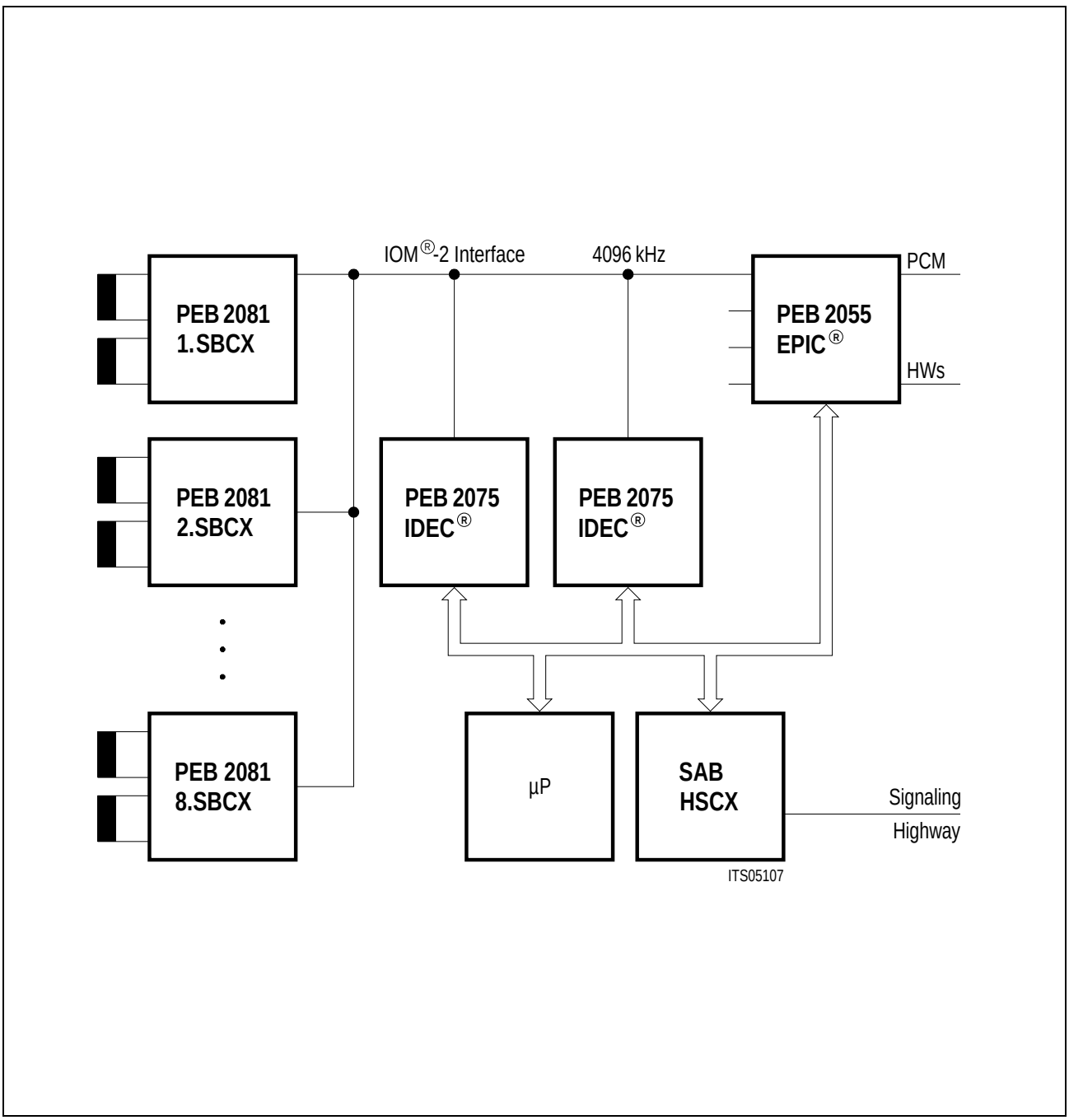


Figure 16
IOM®-2 Line Card Architecture (LT-S) with One D-Channel Controller per Line

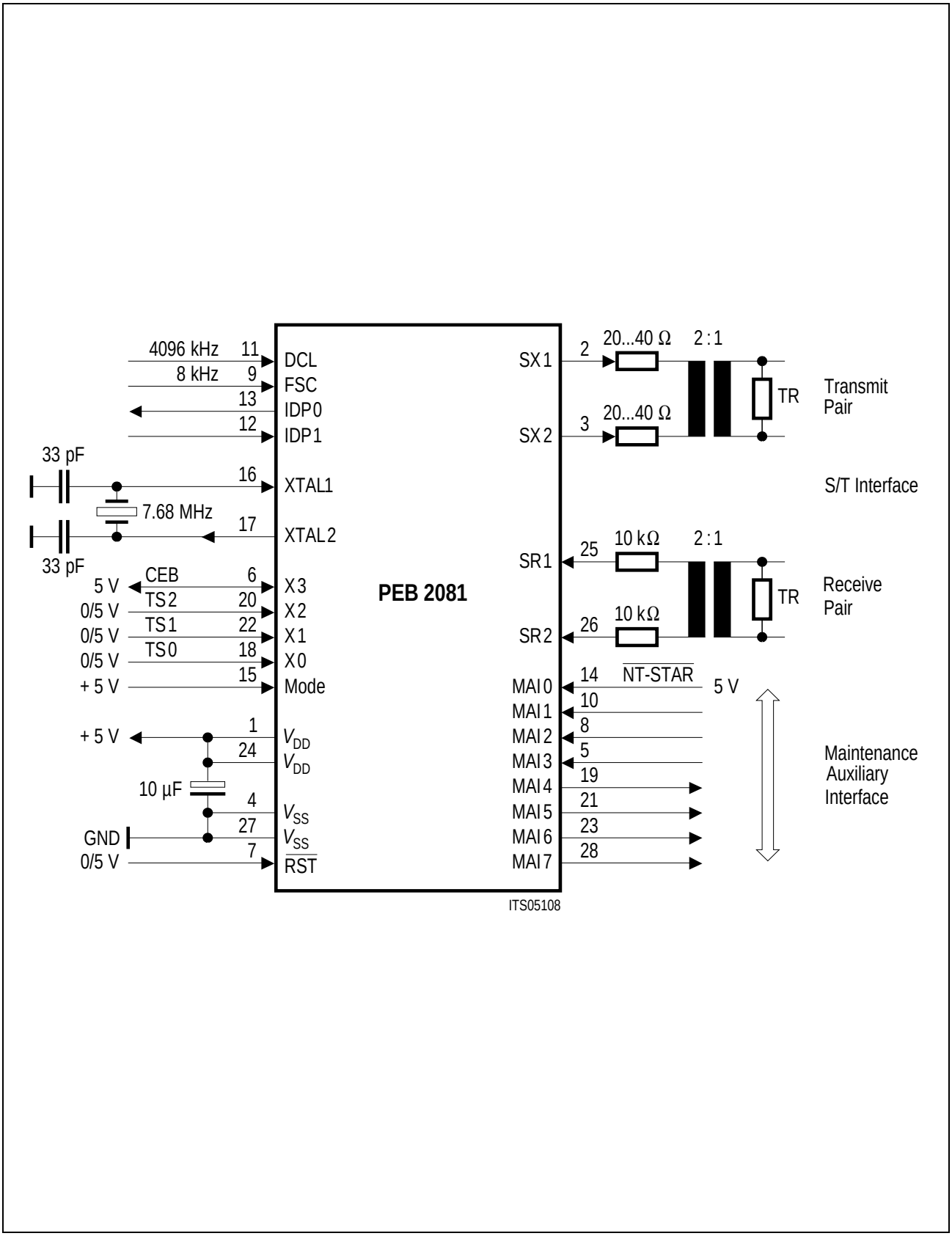


Figure 17
SBCX in LT-S Mode for Basic Line Card Configuration

2.1.6 Line Card Application (one D-channel controller for eight lines)

This configuration is used under the same circumstances as described in **section 2.1.3** “NT1 Star Configuration”. Refer to this section for additional information.

Figure 18 and figure 19 illustrate the principle and its realization in line card applications.

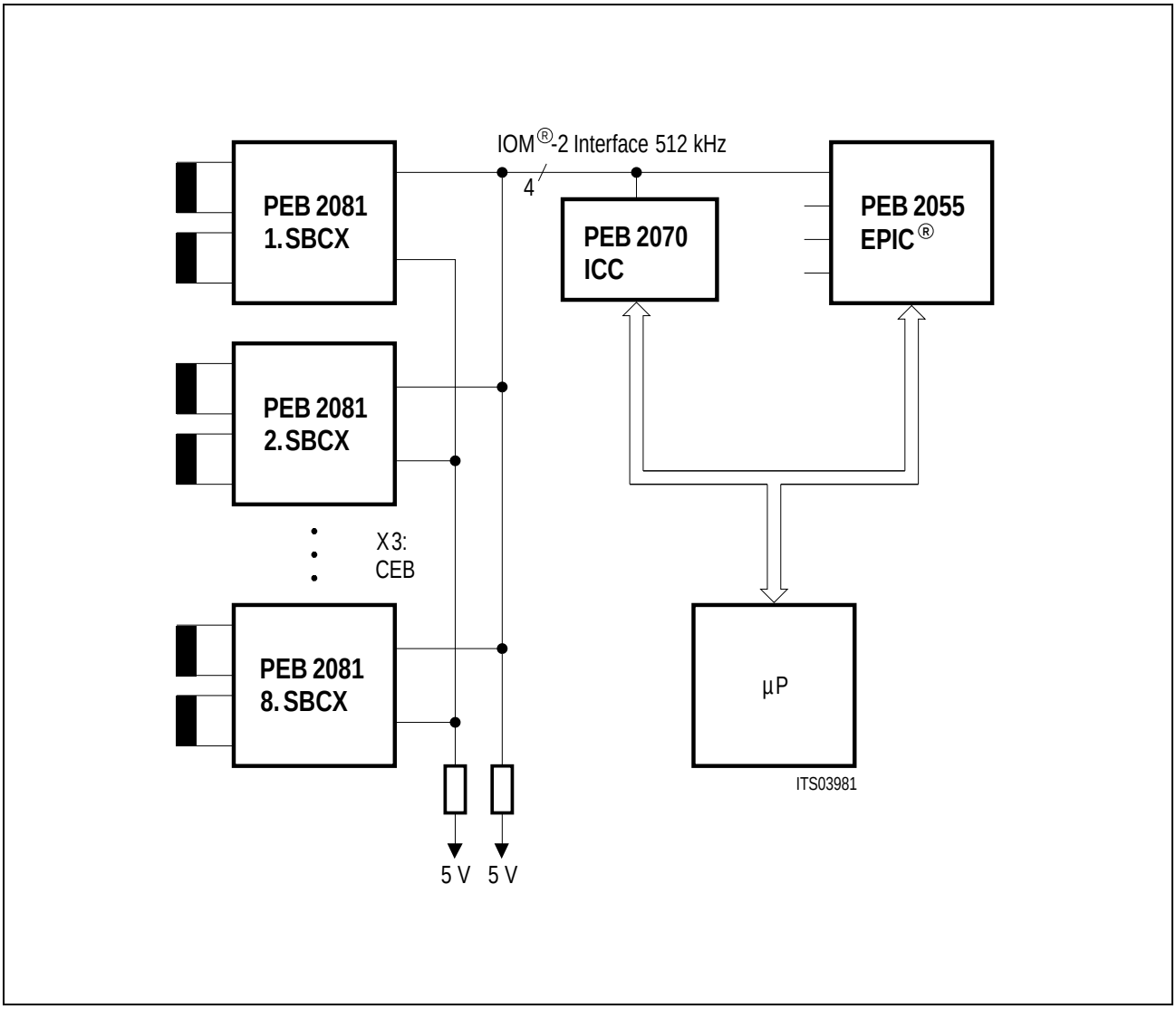
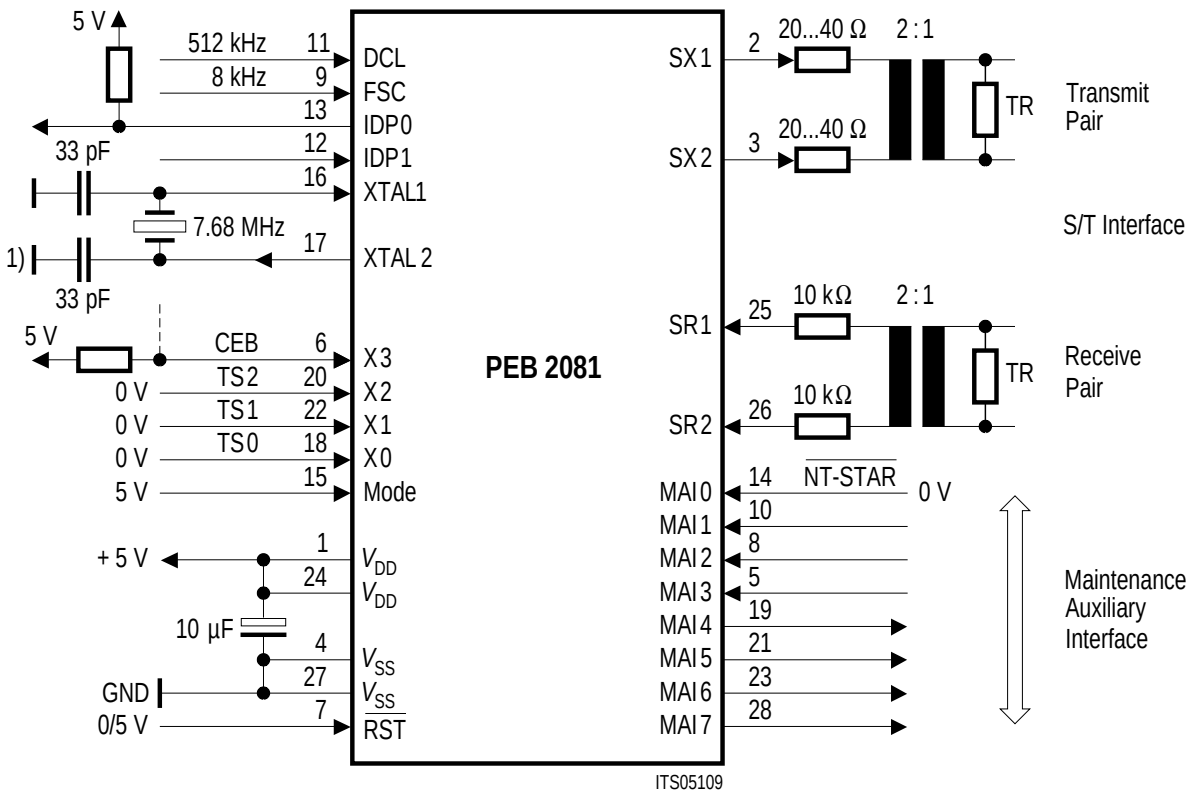


Figure 18
IOM®-2 Line Card Architecture (LT-S only) with One D-Channel Controller per up to Eight Lines



1) Optionally system clock may be used

Figure 19
SBCX in LT-S Mode for Star Configuration

2.1.7 Private-Branch-Exchange Application (one D-channel controller per line)

The SBCX also supports ISDN-PBX configurations in its LT-T (Line Termination-Trunk) mode. By providing internal buffers in this mode, the device is able to compensate phase deviations between the two clock systems on the S-interface and the IOM-2 interface (in PBX system the PEB 2081 is slave with respect to these two clock systems). Specific requirements regarding the clock generation in a PBX system are described in **section 2.3** “Clock Generation”.

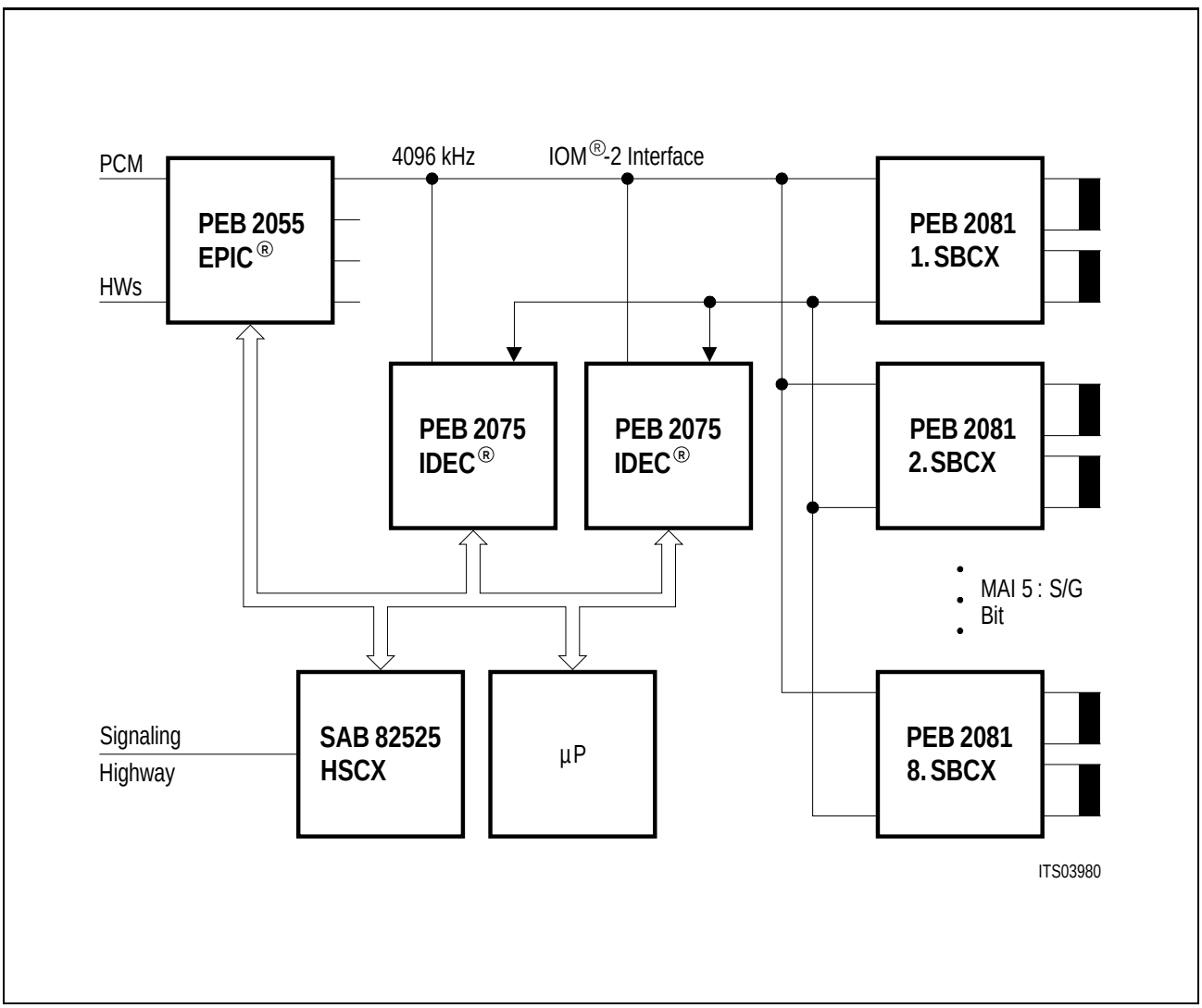


Figure 20
PBX Architecture (LT-T) with One D-Channel Controller per Line

D-channel processing is handled by a separate controller for each line as was the case for line card applications. In order to guarantee correct D-channel access on the S-interface when additional terminals are connected to the same S-bus, an external “D-channel access monitor bit” (≙ S/G bit) is provided in this mode. A system where this bit must be evaluated for correct D-channel access is shown in the following figure. In this configuration the D-channel controller of PBX No. 1 is informed via the S/G bit when the terminal occupies the D-channel on the S-interface. In case a point-to-point configuration is used to connect a single PBX to an exchange the S/G line is not required. Please refer to **section 3.2.3.1** for additional information regarding the use of the S/G bit.

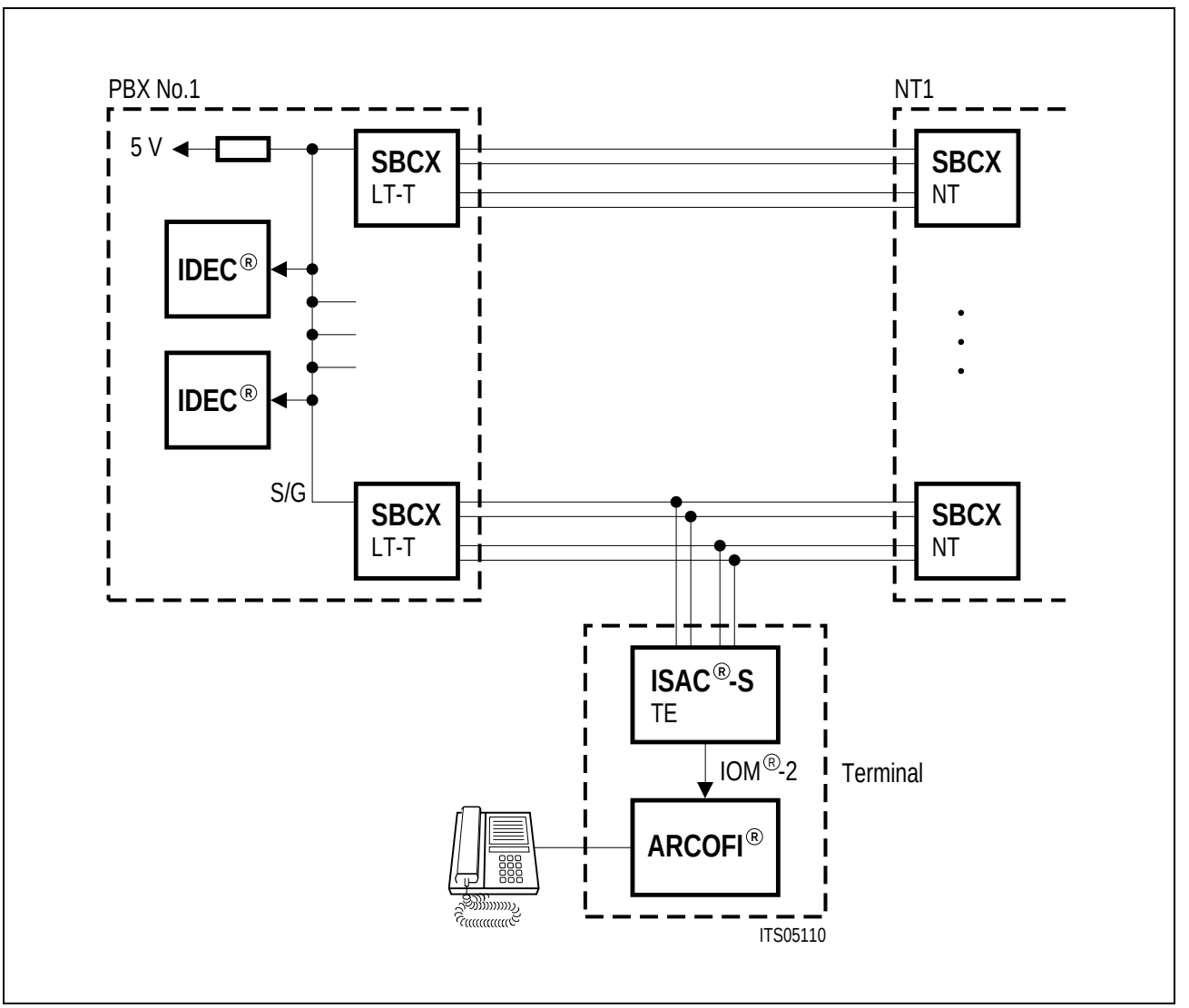


Figure 21
PBX-Configuration Requiring S/G Bit Evaluation

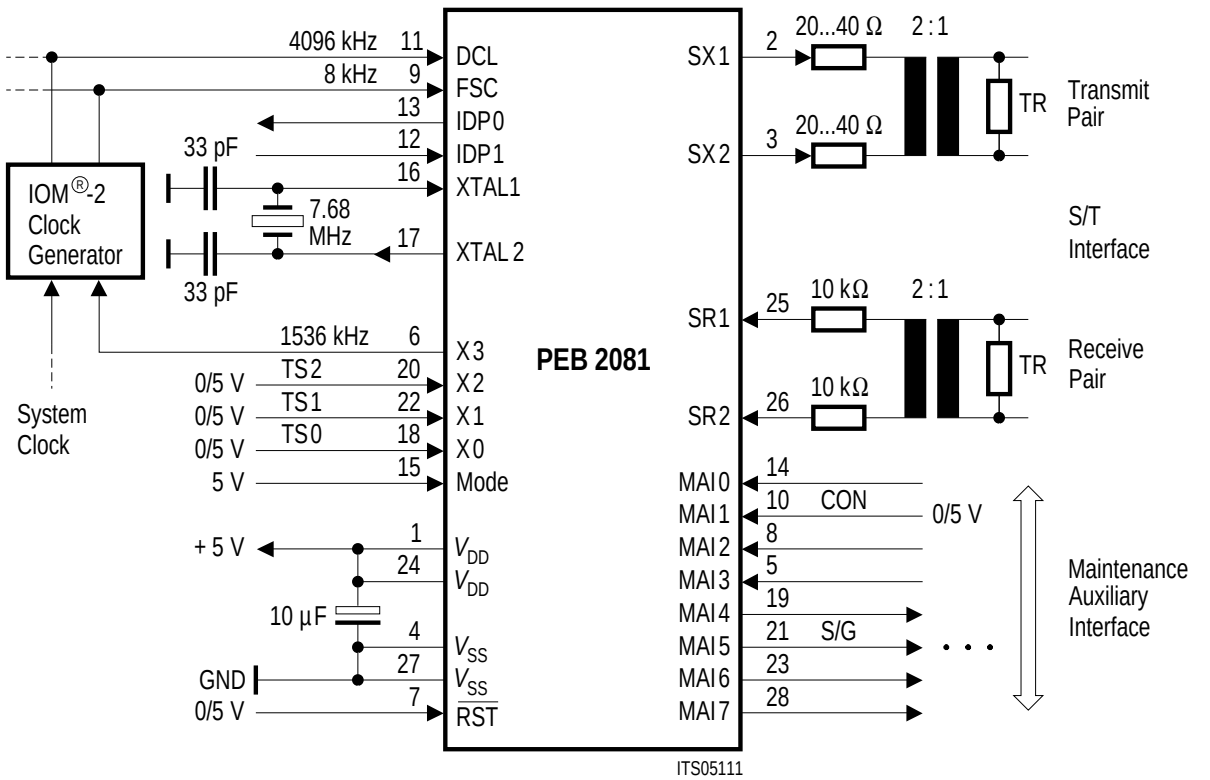


Figure 22
SBCX in LT-T Mode

2.2 Setting Operating Modes

Tables 1-2 illustrate which modes are supported by the PEP 2081 version 3.4 and how they can be configured by the user. **Table 1** gives an overview of pin signals and the register configuration. For the description of MAI pins it was assumed, that for the initial mode, the “I/O specific” mode was selected. Refer to **chapter 4.1.4** for details on the MAI interface options.

It is possible to change the mode of a device during operation by pin strapping (e.g. for test purposes) if the mode change is followed by a hardware reset. A hardware reset sets all registers to their initial value.

Table 1
Modes of Operation

Configuration	**LT-S** Point-Point/Bus	**NT** Point-Point/Bus	**LT-T**	**TE**
Pin				
Mode	1	0	1	0
X0	i:TS0	i:0/i:1 [1)]	i:TS0	o:32/16 kHz (1:1)
X1	i:TS1	i:0	i:TS1	i:0
X2	i:TS2	i:1	i:TS2	i:0
X3	i/o:CEB	i/o:CEB	o:1536 kHz (3:2)	o:768 kHz (1:1)
MAI0	i:$\overline{\text{NT-STAR}}$	i:$\overline{\text{NT-STAR}}$	i:MPR0	i:MPR0
MAI1	i:MPR1	i:MFD	i:CON[2)]	i:CON[3)]
MAI2	i:MPR2	i:$\overline{\text{TM1}}$	i:MPR2	i:MPR2
MAI3	i:MPR3	i:$\overline{\text{TM2}}$	i:MPR3	i:MPR3
MAI4	o:MPR4	o:MPR4	o:MPR4	o:MPR4
MAI5	o:MPR5	o:MPR5	o:S/G	o:S/G if SGE = “1”
MAI6	o:MPR6	o:MPR6	o:MPR6	o:MPR6
MAI7	o:MPR7	o:MPR7	o:MPR7	o:MPR7
FSC	i:8 kHz	i:8 kHz	i:8 kHz	o:8 kHz (1:2)
DCL	i:512-8192 kHz	i:512-8192 kHz	i:512-8192 kHz	o:1536 kHz (1:1)

(cont’d)

Note:
1) Choice for bus configuration (1 = bus). In LT-S mode only programmable. In NT mode programmable or pin strapping. Pin strapping has the higher priority.
2) CON-pin functionality is enabled if DH = “1” in the IOM-2 Channel register in LT-T mode.
3) CON-pin functionality is enabled if DH = “0” in the IOM-2 Channel register in TE mode.

Table 1
Modes of Operation (cont'd)

Configuration	**LT-S** Point-Point/Bus	**NT** Point-Point/Bus	**LT-T**	**TE**
Register				
Configuration Bit 0 (Mode) [0]	0	0/1[7)]	1	0/1[7)]
Configuration Bit 1 (C/W/P) [0]	0/1[1)]	0/1[1)]	0/1[2)]	0/1[3)]
Configuration Bit 5 (FSMM) [0]	0/1	0/1	0	0
Configuration Bit 6 (MAIM) [0]	0	0	0	0
SM/CI Bit 0 (MIO) [0]	0	0	0	0
SM/CI Bit 2 (SGE) [0]	0	0	0	0/1[8)]
IOM-2 Channel Bit 2 (DH) [0]	0/1[4)]	0/1[4)]	0/1[5)]	0/1[6)]

Notes:
1) Choice for bus configuration (1 = bus). In LT-S Mode only programmable. In NT mode programmable or pin strapping. Pin strapping has the higher priority.
2) Slip warning control. C/W/P = 0 will issue C/I "Slip" code warning after 50 µs wander. C/W/P = 1 will issue the "Slip" code warning after 25 µs.
3) PCK (pin X0) frequency select. C/W/P = 0 will issue a power converter clock frequency of 32 kHz, C/W/P = 1 will issue 16 kHz.
4) Select "1" for intelligent NT applications to ensure partial TIC Bus evaluation (**see section 3.3.5.5)**.
5) Select "1" for point-to-multipoint configurations to ensure D-channel collision resolution according to ITU I.430 (**see section 2.1.7 and 3.3.5.4**).
6) For normal D-channel collision procedure program DH = "0".
7) 0: MAI pins I/O specific; 1: MAI pins only I/O.
8) In TE Mode pin MAI5 outputs a D-channel enable signal, which may be used by a general purpose HDLC controller for LAP D handling. The signal contiuously monitors the D-E channel status and provides a stop/ go information.

[0] Initial register bit value after hard- or software reset.

Table 2
IOM®-2 Channel Assignment *)

IOM®-2 Channel No.	TS2	TS1	TS0	Bit No.	Min. Freq. of DCL (kHz)
CH 0	0	0	0	0 … 31	512
CH 1	0	0	1	32 … 63	1024
CH 2	0	1	0	64 … 95	1536
CH 3	0	1	1	96 … 127	2048
CH 4	1	0	0	128 … 159	2560
CH 5	1	0	1	160 … 191	3072
CH 6	1	1	0	192 … 223	3584
CH 7	1	1	1	224 … 255	4096

Note:
*) TS pins are read continuously (non-latching) after the supply voltage has reached its nominal value.

2.3 Clock Generation

Clock generation varies with the application. The following diagrams show what timing signals need to be generated for each SBCX mode and how system synchronization is obtained.

2.3.1 TE Mode

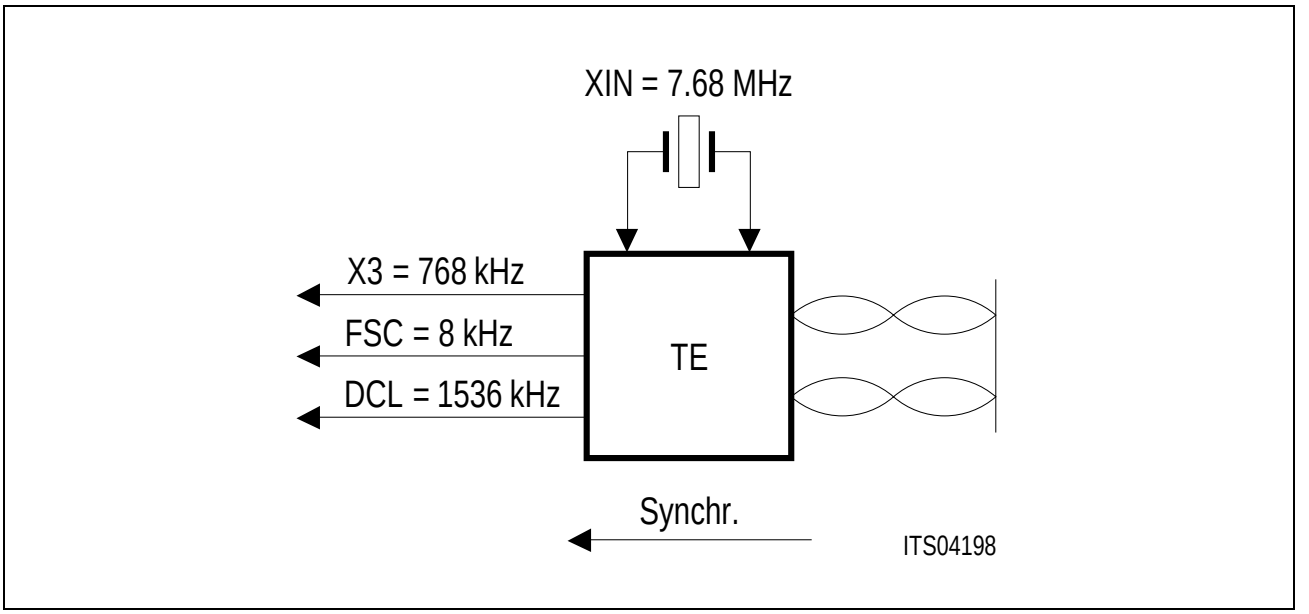


Figure 23
Clock Generation for TE Mode

In TE mode the PEB 2081 recovers the timing directly from the S-interface. A free running crystal or other clock source provides a 7.68 MHz base clock. The device synchronizes in TE Mode with a Receive PLL (RPLL) onto the S-interface by including 65 ns correction steps. Thus the issued IOM clocks and the clock signal on pin X3 are synchronous to the PTT master clock.

2.3.2 NT Mode

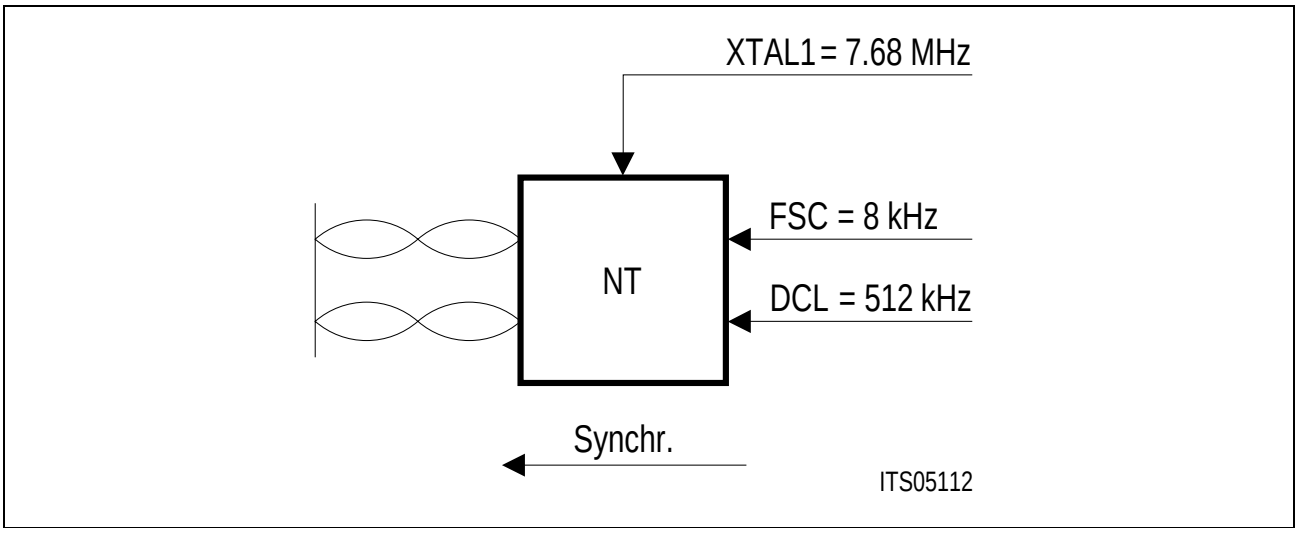


Figure 24
Clocks Generation in NT Mode

In NT Mode the SBCX is supplied with synchronous IOM clocks and a synchronous base clock signal. These signals typically are generated by the upstream U-interface device (PEB 2091 or PEB 2095).

In case no 7.68 MHz base clock signal is available, a 7.68 MHz crystal may be connected to XTAL1 and XTAL2. In this configuration the internal Transmit PLL (XPLL) synchronizes the freerunning crystal clock onto the FSC signal.

If required DCL clock rates up to 8192 kHz may be used. However the PEB 2081 will operate in IOM channel 0 independently of the DCL frequency applied.

2.3.3 LT-T Mode

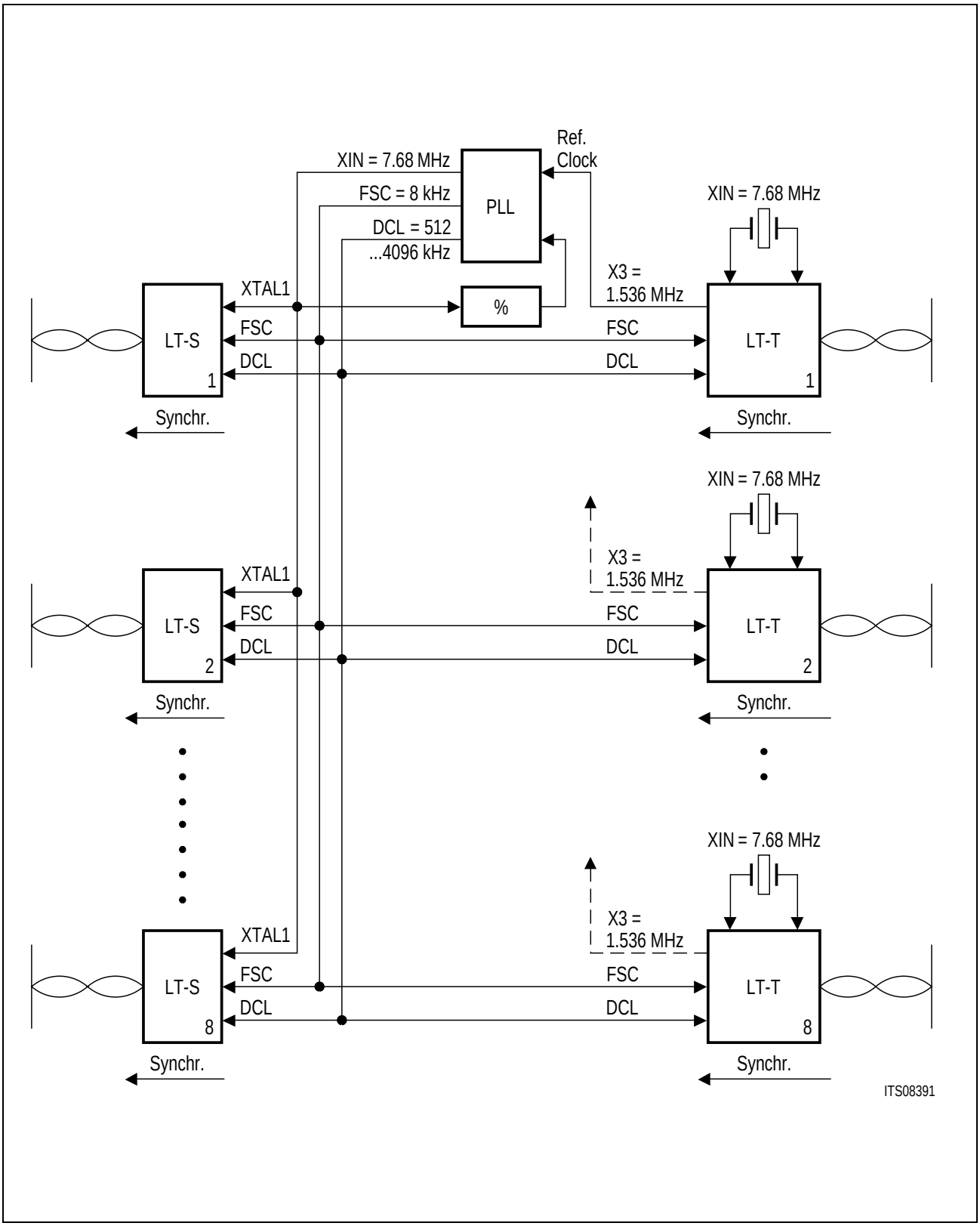


Figure 25
Clock Generation in LT-T Mode

In LT-T mode IOM-clock signals are not issued by the device but need to be generated externally. In order to ensure synchronous timing to the PTT-master clock, a PLL is used for generation of FSC and DCL (supplied to LT-T and LT-S devices) as well as of the 7.68-MHz system clock (LT-S only). Reference clock for the PLL is the PTT synchronous 1536-kHz signal from pin X3.

Note:

It may be necessary to use a multiplexer for the PLL reference clock because the X3 clock signal is synchronous to the PTT clock only if the corresponding line is activated. Otherwise the PLL reference must be supplied by the X3 clock from a different activated line.

2.3.4 LT-S Mode

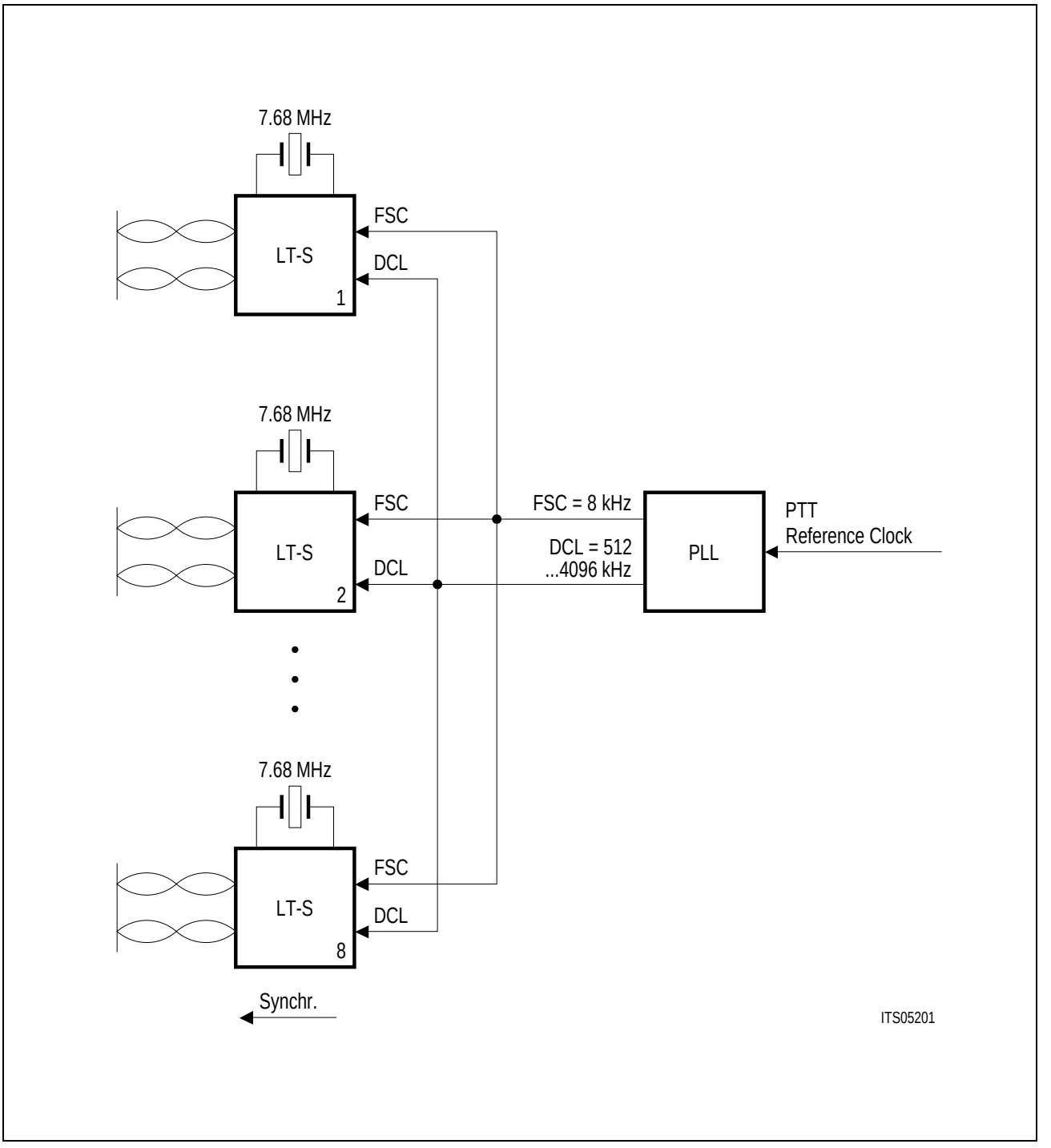


Figure 26
Clock Generation in LT-S Mode

In LT-S mode the device synchronizes with the internal Transmit PLL (XPLL) the freerunning crystal clock onto the FSC signal. This ensures that transmission on the S-interface will be synchronous to the PTT clock.

2.4 S/T-Interface Configurations

The receiver of the SBCX exceeds the electrical requirements of the S/T-interface. An overview of the different wiring configurations is given in the following figures.

The maximum length of a point-to-point configuration depends on the kind of cable installed. The maximum allowable line attenuation is 13 dB. However, the following figures give an idea of the performance of the SBCX.

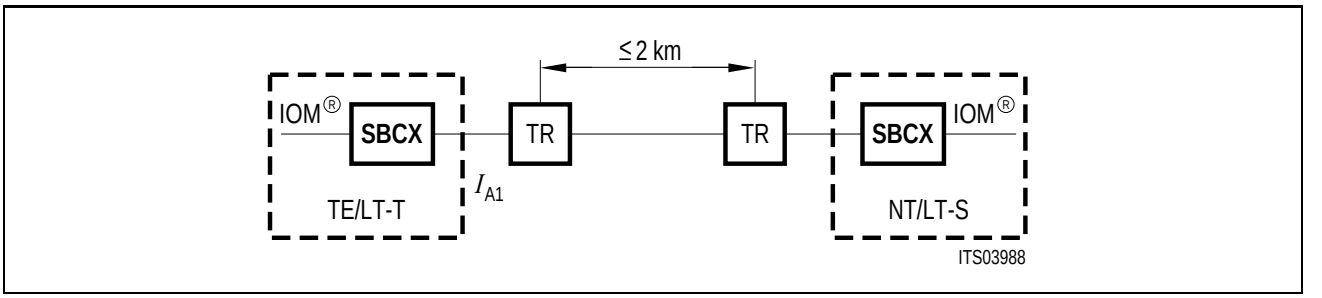


Figure 27
S/T-Interface Point-to-Point Configuration ("TR" stands for the 100 Ω Terminating Resistor)

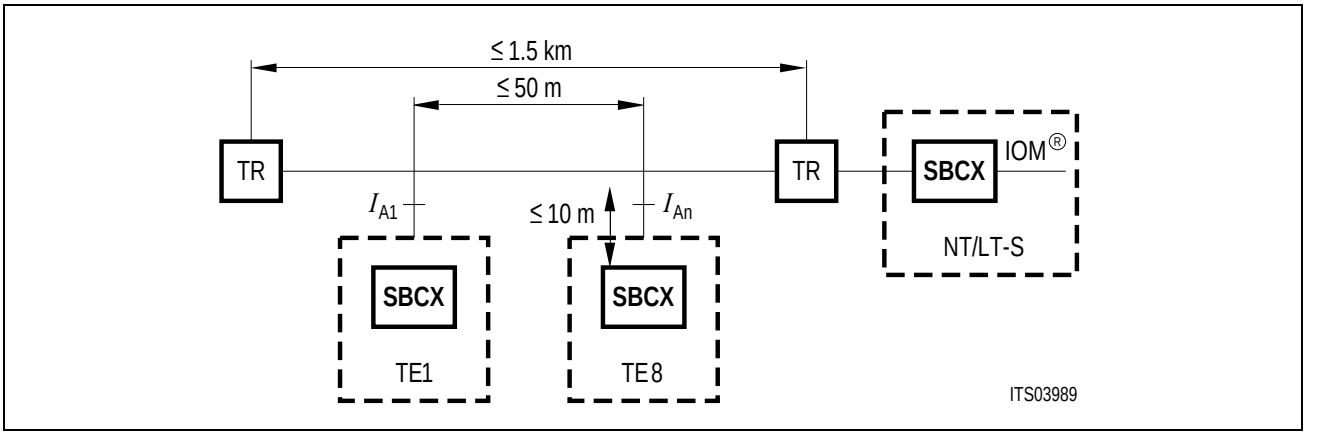


Figure 28
S/T-Interface Extended Passive Bus Configuration ("TR" stands for the 100 Ω Terminating Resistor)

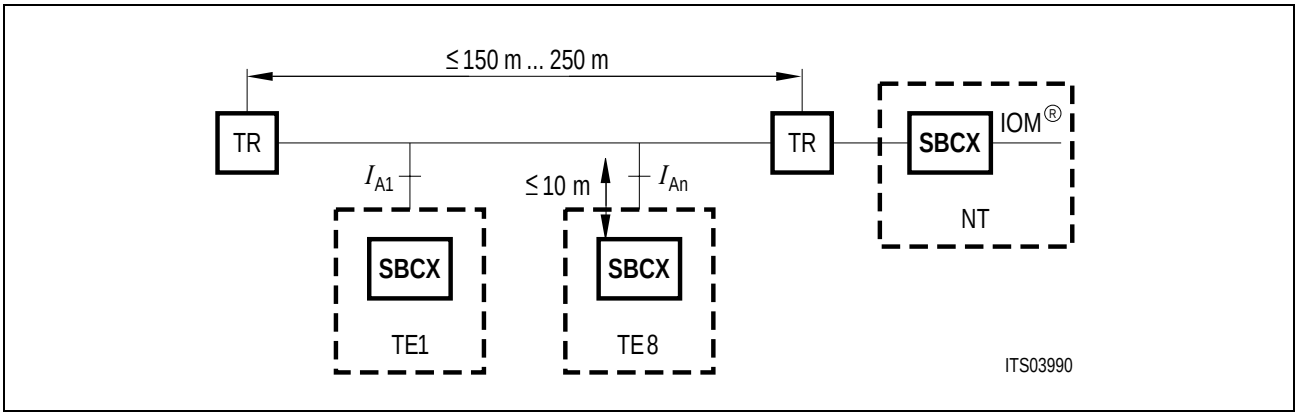


Figure 29
S/T-Interface Short Passive Bus Configuration ("TR" stands for the 100 Ω Terminating Resistor)

3 Application Guide

3.1 SBCX Device Architecture and General Functions

The SBCX performs the layer-1 functions of the S/T-interface according to ITU recommendation I.430, ETS 300 012 and T1.605 Basic User Network Interface Specification, respectively. It can be used at all ends of the S/T-interface. The following figure depicts the device architecture.

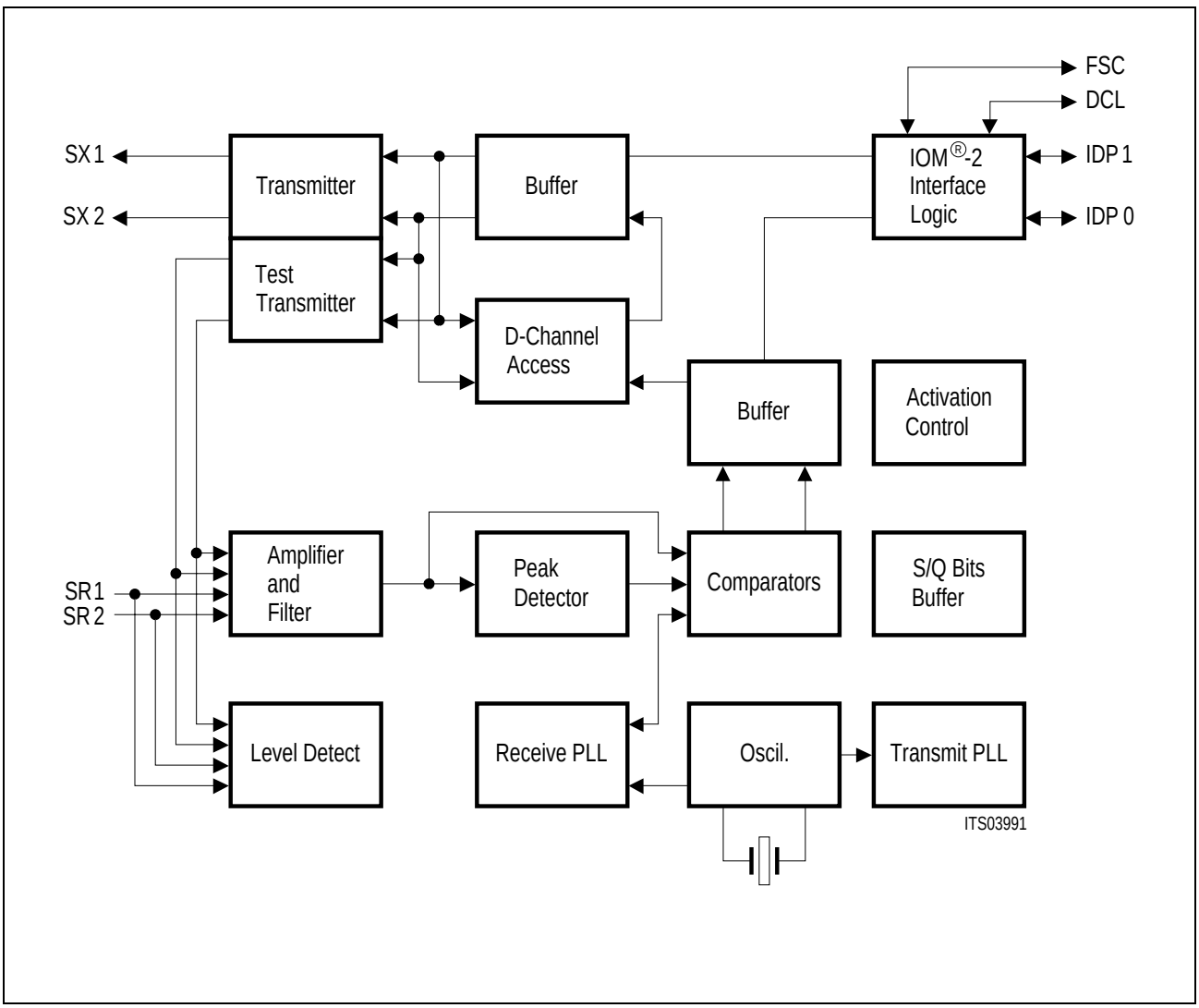


Figure 30
SBCX Device Architecture

The Common Functions for all Operating Modes are:

- line transceiver functions for the S/T-interface according to the electrical specifications of ITU I.430
- The pseudo-ternary pulse shaping which meets the I.430 pulse templates, is achieved with the integrated transmitter.
- The integrated receiver is designed to cope with all wiring configurations of the S/T-interface (point-to-point, passive bus, and extended passive bus). The maximum allowable line attenuation is 13 dB.
- conversion of the frame structure between the IOM-2 interface and S/T-interface
- conversion from/to binary to/from pseudo-ternary code
- access to S and Q bits
- The level detect block monitors the receive line and therefore initiates switching into power down or power up state.

Mode Specific Functions are:

- receive timing recovery for point-to-point, passive bus and extended passive bus configuration
- S/T timing generation using IOM-2 timing synchronous to system, or vice versa
- D-channel access control and priority handling
- D-channel echo bit generation by handling of the common echo bit
- activation/deactivation procedures, triggered by primitives received over the IOM-2 interface or by INFOs received from the line
- frame alignment in trunk application with maximum wander of $\pm 50\ \mu s$
- execution of test loops

3.2 Interfaces

Section 3.2 describes the interfaces supplied by the SBCX. Three interfaces are implemented:

- IOM-2 Interface
- S-Interface
- Maintenance Auxiliary Interface

3.2.1 IOM®-2 Interface

The IOM-2 interface is primarily used to interconnect telecommunication ICs. It provides a symmetrical full-duplex communication link, containing user data, control/programming and status channels. The SBCX communicates with other ISDN devices to realize OSI layer-1 functions (such as a U Transceiver) or upper layer functions (such as ICC, EPIC, ARCOFI and ITAC).

The structure used follows the 2B + 1D-channel structure of ISDN. The ISDN user data rate of 144 kbit/s (B1 + B2 + D) on the S/T-interface is transmitted transparently in both directions over the interface. The D-channel switching may also be subject to the D-channel access procedure and collision detection and therefore is not fully transparent.

The IOM-2 interface is a generalization and enhancement of the IOM®-1 interface.

3.2.1.1 IOM®-2 Frame Structure/Timing Modes

The IOM-2 interface comprises two clock lines for synchronization and two data lines.

Data is carried over Data Upstream (DU) and Data Downstream (DD) signals. The downstream and upstream direction are always defined with respect to the exchange. Downstream refers to information flow from the exchange to the subscriber and upstream vice versa respectively. The IOM-2 Interface Specification describes open drain data lines with external pull-up resistors. However, if operation is logically point-to-point, tristate operation is possible as well.

The data is clocked by a Data Clock (DCL) that operates at twice the data rate. Frames are delimited by an 8-kHz Frame Synchronization Clock (FSC).

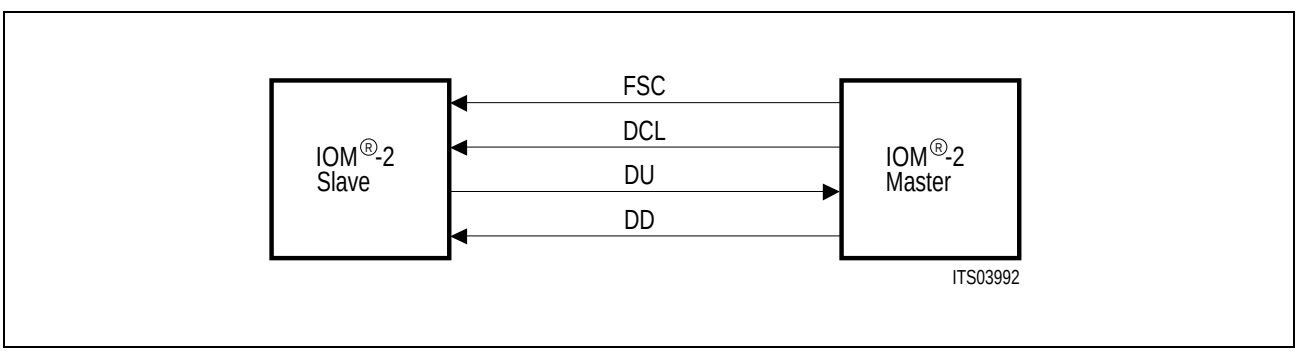


Figure 31
IOM®-2 Interface Structure

Within one FSC period 32 bit to 512 bit are transmitted, corresponding to DCL frequencies from 512 kHz to 8.192 MHz. The SBCX needs no pin strapping to indicate the actual bit rate, because each rising edge of FSC resets the internal bit counter.

Two optimized IOM-2 timing modes exist for:

– Line card Applications
– Terminal Applications

Both the line card and terminal applications utilize the same basic frame and clocking structure, but differ in the number and usage of the individual channels.

frame	B1	B2	Monitor	D	Command/Indication	MR	MX
bits	8	8	8	2	4	1	1

Figure 32
Basic Channel Structure of IOM®-2

Each frame consists of

- two 64 kbit/s channels B1 and B2
- the monitor channel for transferring maintenance information between the layer-1 functional blocks (SBCX, IEC-Q, etc.) and the layer-2 controller (ICC, EPIC)
- two bits for the 16 kbit/s D-channel
- four command/indication (C/I) bits for controlling of layer-1 functions (activation/deactivation and additional control functions) by the layer-2 controller (ICC, EPIC). For a list of the C/I codes and their use refer to **chapter 4**.
- two bits MR and MX for handling the monitor channel

3.2.1.1.1 IOM®-2 Interface Line Card Frame Structure

The SBCX in line card applications (LT-S and LT-T) supports bit rates from 256 kbit/s to 4096 kbit/s corresponding to DCL frequencies from 512 kHz to 8.192 MHz.

The typical IOM-2 line card applications comprises a DCL frequency of 4096 kHz with a nominal bit rate of 2048 kbit/s. Therefore eight channels are available, each consisting of the basic frame with a nominal data rate of 256 kbit/s. The length of the FSC high phase usually covers IOM-2 channel 0 (minimum FSC length is 2 DCL) unless synchronization of the S/T-interface multi-frame is desired.

The SBCX is assigned to an individual channel by pin strapping.

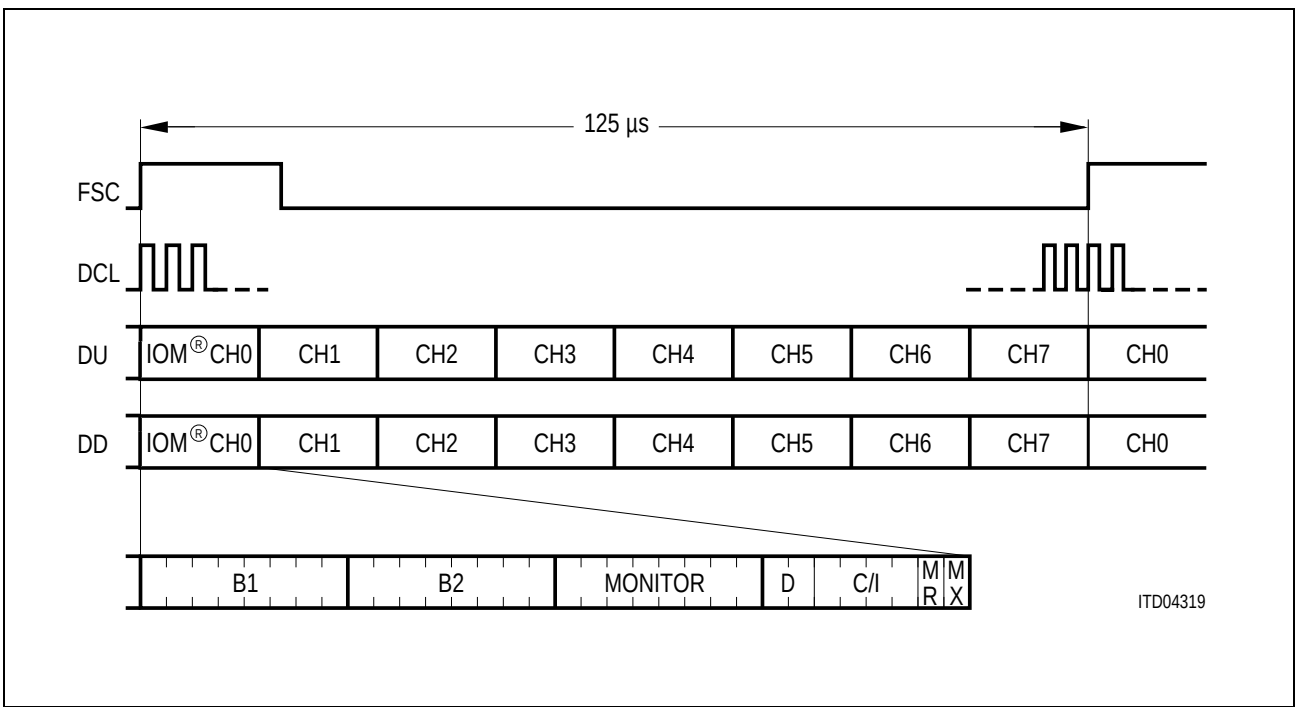


Figure 33
Multiplexed Frame Structure of the IOM®-2 Interface

3.2.1.1.2 IOM®-2 Interface Terminal Frame Structure

In TE mode the SBCX provides a data clock DCL with a frequency of 1536 kHz. As a consequence the IOM-2 interface provides three channels each with a nominal data rate of 256 kbit/s.

The SBXC only uses IOM-2 channel 0, and, for D-channel access control, the C/I field of IOM-2 channel 2. The downstream data (DD) are transferred on pin IDP0, the upstream data (DU) on pin IDP1.

The remaining two IOM-2 channels are for the use of other devices (ARCOFI, ITAC) within the TE.

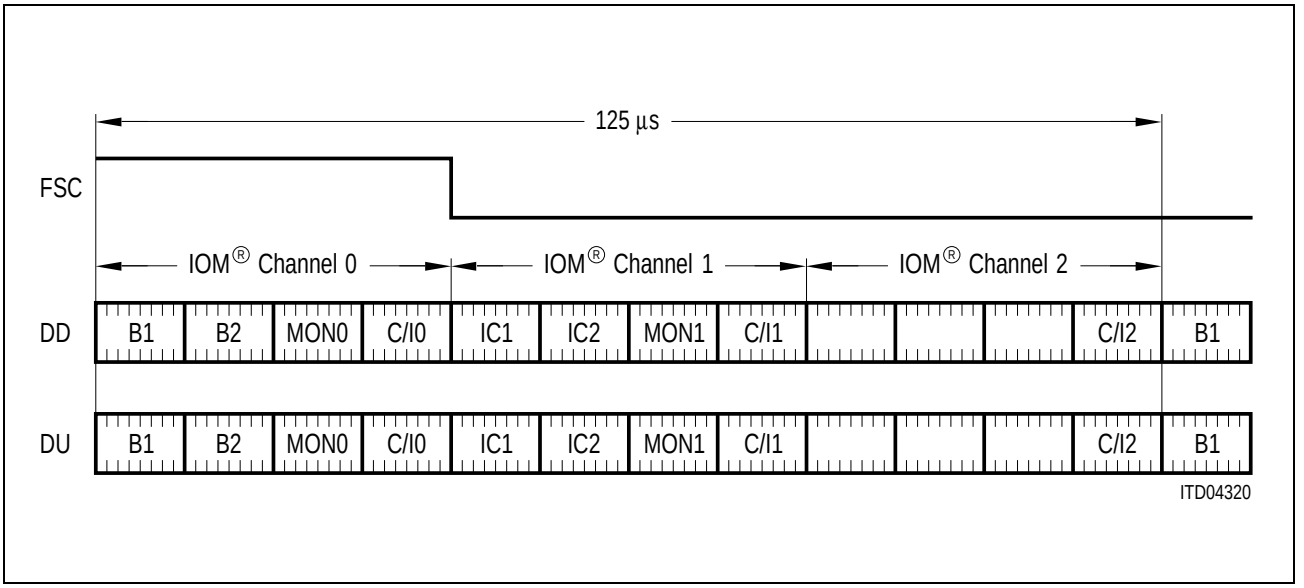


Figure 34
Definition of the IOM®-2 Channels in a Terminal

– C/I0 in IOM® Channel 0:

DU / DD	D	D	C/I4	C/I3	C/I2	C/I1	MR	MX

D: two bits for the 16 kbit/s D-channel

C/I: The four command/indication (C/I) bits are used for controlling of the layer-1 functions (activation/deactivation and additional control functions) by the layer-2 controller (ICC, EPIC).

MR, **MX:** two bits MR and MX for handling the monitor channel 0

– C/I1 in IOM® Channel 1:

DU / DD	C/I6	C/I5	C/I4	C/I3	C/I2	C/I1	MR	MX

C/I1 to C/I6 are used to convey real status information between a layer-2 device (ICC) and various non layer-1 devices e.g. ARCOFI.

MR, **MX:** two bits MR and MX for handling the monitor channel 1

– C/I2 in IOM® Channel 2:

DU	1	1	BAC	TBA2	TBA1	TBA0	1	1
DD	E	E	S/G	A/B	1	1	1	1

E: D-echo bits

BAC-bit (Bus ACcessed), used by the layer-2 device (e.g. ICC). When the TIC bus is occupied the BAC-bit is low.

S/G-bit (Stop/Go), available to the layer-2 devices (e.g. ICC) to determine if they can access the S bus D-channel (S/G = 1: stop, S/G = 0: go).

A/B-bit (available/blocked), supplementary bit for D-channel control.
(A/B = 1: D-channel available, A/B = 0: D-channel blocked).

For more information also refer to the chapters TIC Bus Access and D-channel access control.

3.2.1.2 IOM®-2 Interface Command / Indicate Channel

The Command/Indicate channel (C/I channel) is used to control the operational status of the SBCX and to issue corresponding indications. C/I channel codes serve as the main link between the SBCX and other external intelligence (layer-1 or layer-2 devices). In **chapter 4.3** status diagrams for all selectable modes give information on the commands with which the current operational status may be left, and on indications issued in all states.

The codes originating from the control devices are called “commands”, those originating from the SBCX are referred to as “indications”. Commands have to be applied continuously by the controller until the command is validated by the SBCX and the desired action has been initiated. Afterwards the command may be changed.

An indication is issued permanently by the SBCX until a new indication needs to be forwarded. Because a number of states issue identical indications it is not possible to identify each state individually.

The interpretation of C/I codes depends on the mode selected. **Table 3** shows the abbreviations used for C/I commands and indications.

The C/I channel can be disabled (Intelligent NT) by setting the CIH-bit in the IOM channel register. The C/I channel would then be accessible via the monitor channel (SM/CI register).

In TE mode a second C/I channel can be used to convey real status information between by a layer 2 device (ICC) and various non layer-1 devices e.g. ARCOFI. The channel consists of six bits in each direction.

For a list of the C/I codes and their use, refer to **chapter 4**.

Table 3
C/I Abbreviations

Code	Description
AI	Activation Indication
AI8	Activation Indication with priority 8
AI10	Activation Indication with priority 10
AIL	Activation Indication Loop
AR	Activation Request
AR8	Activation Request with priority 8
AR10	Activation Request with priority 10
ARL	Activation Request Loop
CVR	Code Violation Received (far end)
DC	Deactivation Confirmation
DI	Deactivation Indication
DR	Deactivation Request
MAIC	Maintenance Auxiliary Interface Change
PU	Power Up
RES	Reset
RSY	Resynchronizing
SLIP	Slip of Frame (frame jump)
TIM	Timing Request
TM1	Test Mode 1 (2-kHz test signal)
TM2	Test Mode 2 (96-kHz test signal)

The following examples illustrate the use of the C/I channel in combination with the PEB 2070 and the PEB 2055. Both examples assume that the device has been correctly initialized prior to starting the C/I code transfer.

PEB 2070 and C/I-Channel Programming

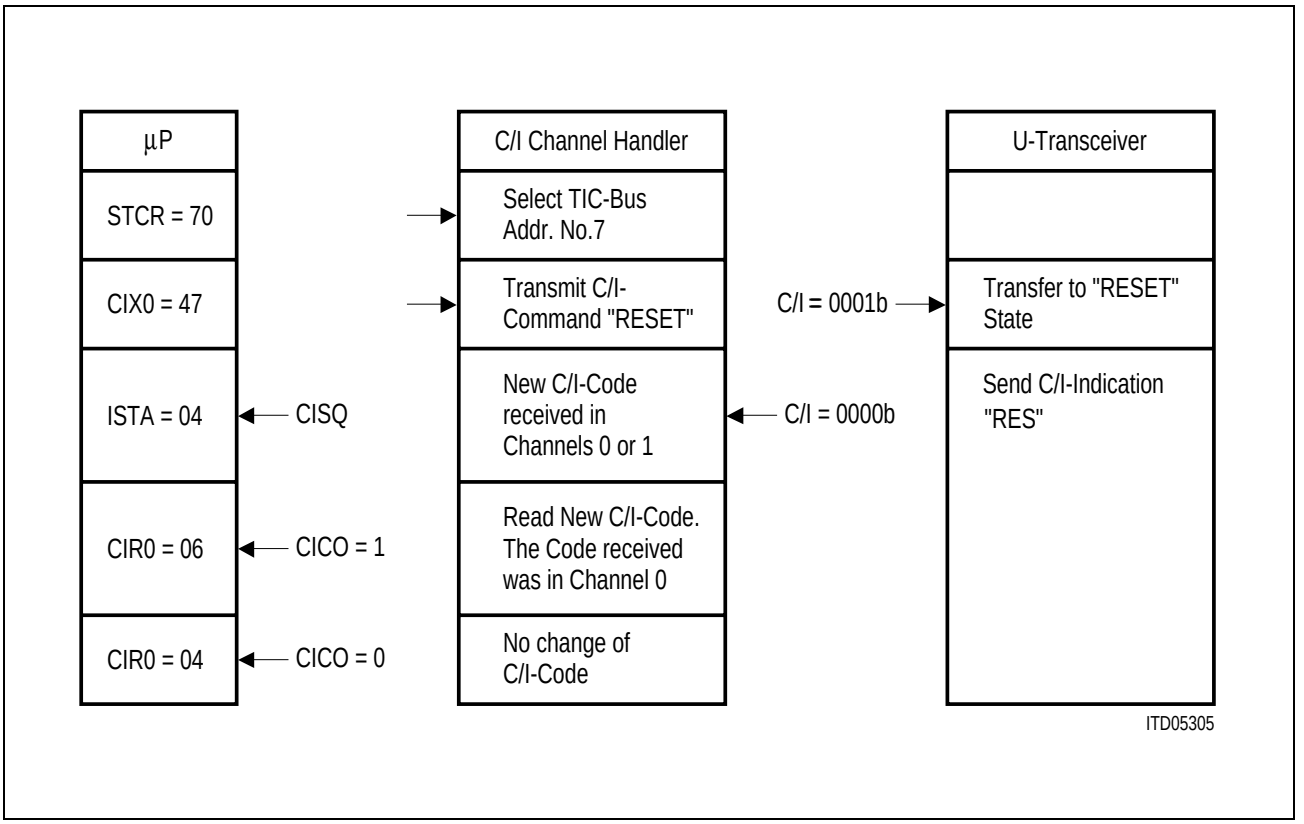


Figure 35
C/I-Channel Use with the ICC (all data values hexadecimal)

The STCR-register is programmed to allocate TIC-bus address 7 to the ICC. The C/I-command is transmitted with the CIX0-register (structure: 0 1 C/I C/I C/I C/I 1 1, bus access bit enabled). After the new C/I-command is loaded it is transmitted immediately.

A change in the C/I-channel is indicated by an ISTA-interrupt (CISQ-bit). The new C/I-message can be read from register CIR0 (structure: 0 0 C/I C/I C/I CIC0 0 1). Bit CIC0 indicates that the new C/I-message was received in channel 0 for at least two consecutive frames. It is reset after the read operation.

PEB 2055 and C/I-Channel Programming

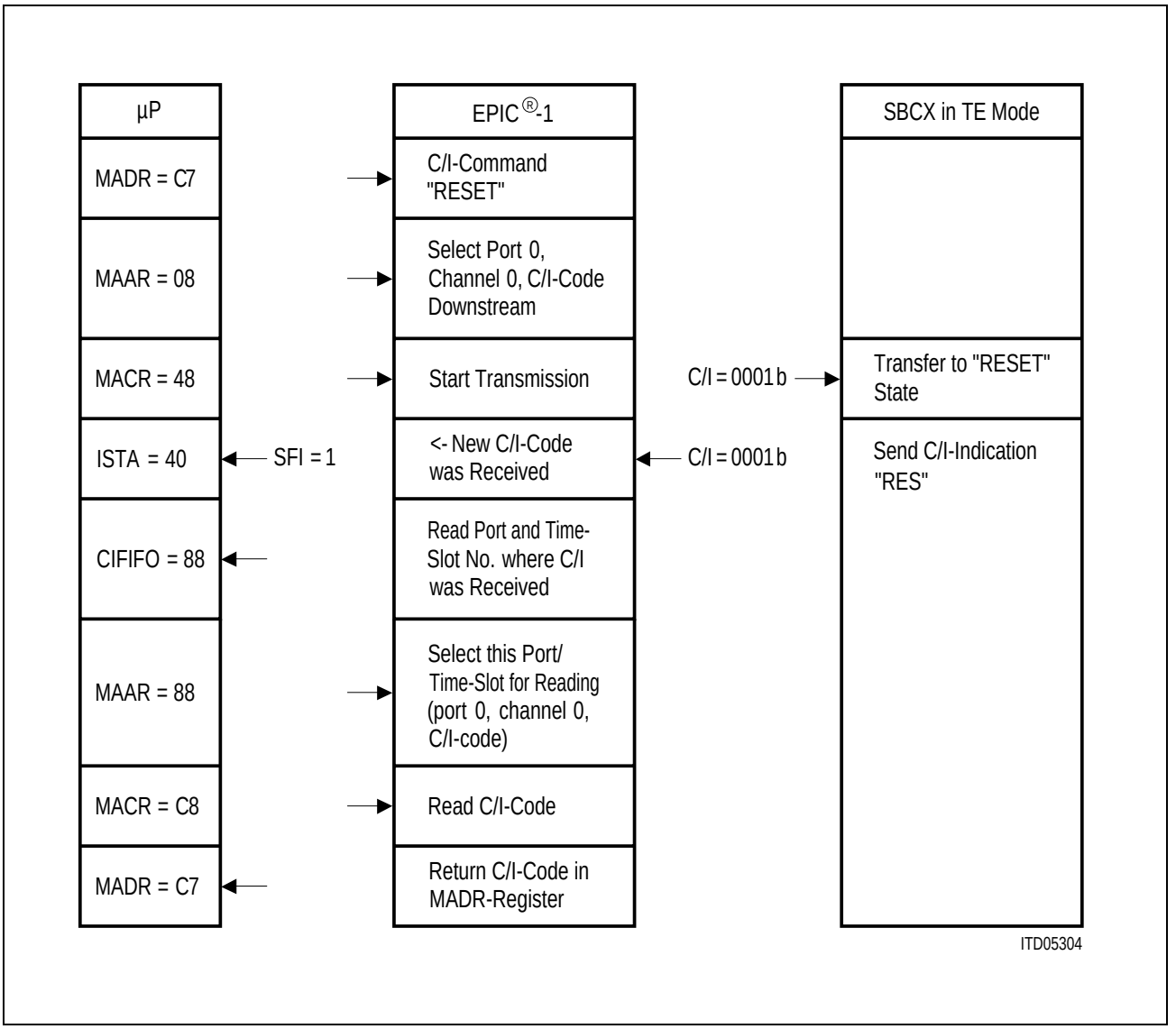


Figure 36
C/I-Channel Use with the EPIC® (all data values hexadecimal)

After the correct initialization of the EPIC, the C/I-code which is to be transmitted to the SBCX is written into the MADR-register (structure 1 1 C/I C/I C/I C/I 1 1). With the MAAR-register the EPIC is informed where to send this C/I-code (transmission direction, port number and time-slot number). For a description of this register please refer to the EPIC-manual, the example above sends the C/I-command to port 0, IOM-2 channel 0. MACR = 48_H starts the transmission of the command.

If a change in one of the C/I-channels was observed, and ISTA-interrupt (bit SFI) is generated. Because the user does not know in which channel the change occurred, the location needs to be read from the CIFIFO-register. This address is copied via software into address register MAAR. After having started the read operation with MACR = $C8_H$ the C/I-message can be read from MADR (structure as described earlier).

3.2.1.3 IOM®-2 Interface Monitor Channel

The monitor channel represents a second method to access SBCX specific features. Features of the monitor channel are supplementary to the C/I-channel. The SBCX uses the monitor channel for both, local programming and local functions (register access, e.g. MAI status) and S/Q maintenance bit information transfer. Monitor commands supported by the PEB 2081 divide into three categories. Each category derives its name from the first nibble (4 bits) of the one or two byte long message. All monitor messages representing similar functions are grouped together.

Monitor functions of the SBCX can only be accessed by a control device (ICC, EPIC) in IOM-2 mode. The following chapters describe the principle of monitor handshake in IOM-2, internal safeguards against a blocking of the monitor channel as well as features supported.

In case the IOM-2 Terminal structure is used, monitor channel 1 may be used by a codec device (e.g. ARCOFI).

3.2.1.3.1 Handshake Procedure

IOM-2 provides a sophisticated handshake procedure for the transfer of monitor messages. For handshake control two bits are assigned to each IOM-frame (on IDP0 and IDP1).

The monitor transmit bit (MX) indicates when a new byte has been issued in the monitor channel (active low). The transmitter postpones the next information until the correct reception has been confirmed. A correct reception will be confirmed by setting the monitor read bit (MR) to low.

In order to send a monitor message from the control unit to the SBCX, the MX-bit on IDP1 and the MR-bit on IDP0 are used. In the opposite direction the SBCX handles the MX-bit of the IDP0-pin and watches the MR-bit of the IDP1-signal.

Figure 37 illustrates monitor channel handling with the PEB 2070 (ICC), **figure 38** demonstrates it with the PEB 2055 (EPIC-1). A two-byte message is sent from the control unit to the SBCX who acknowledges the receipt by returning a two-byte long message in the monitor channel.

ICC and Monitor Channel Programming

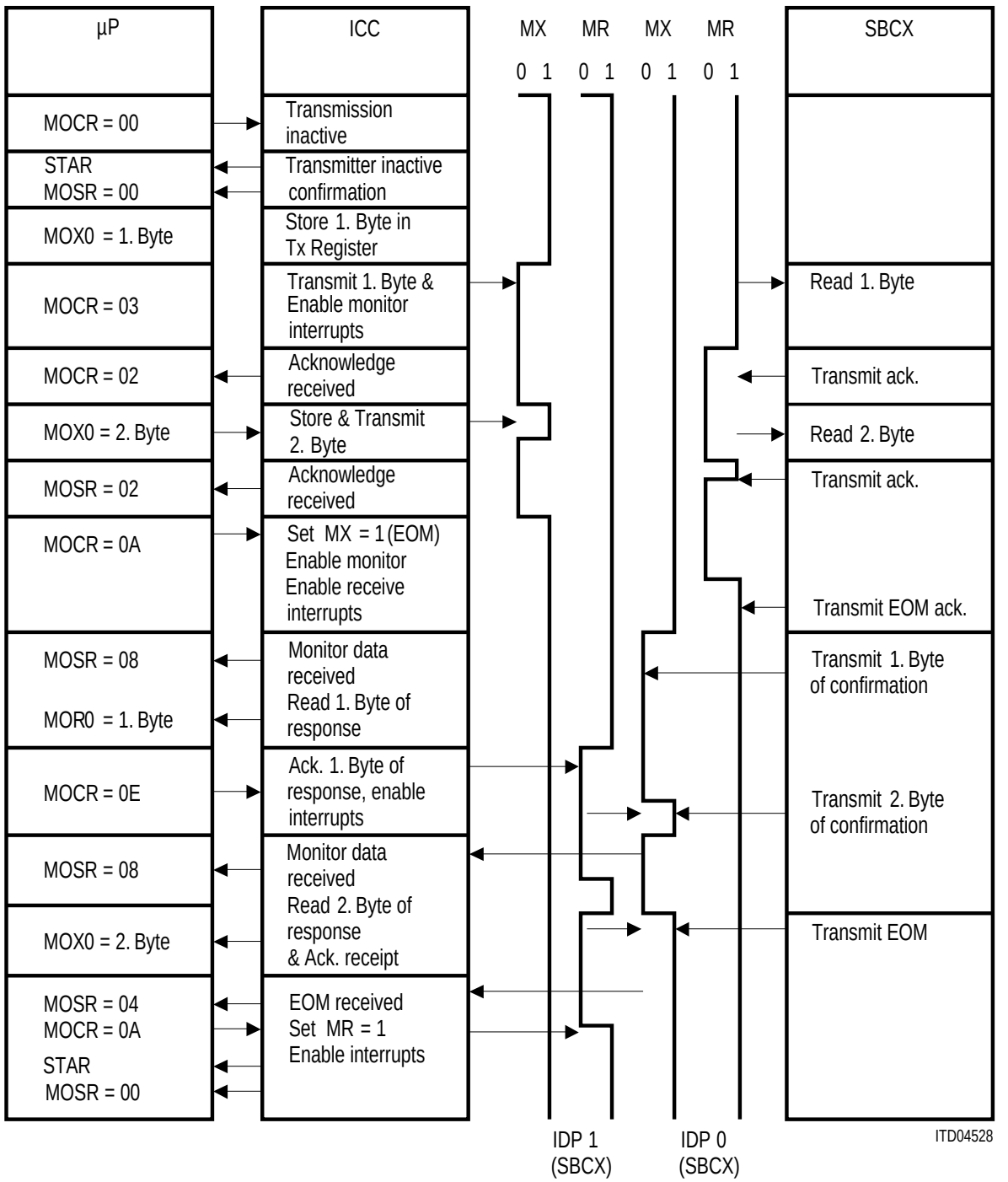


Figure 37
Monitor Channel Handling with ICC (all data values hexadecimal)

The µP starts the transfer procedure after having confirmed the monitor channel being inactive. The first byte of monitor data is loaded into the transmit register. Via the Monitor Control Register MOCR-monitor interrupts are enabled and control of the MX-bit is handed over to the ICC. Then transmission of the first byte begins. The SBCX reacts to a low level of the MX-bit on IDP1 by reading and acknowledging the monitor channel byte automatically. On detection of the confirmation, the ICC issues a monitor interrupt to inform the µP that the next byte may be sent. Loading the second byte into the transmit register results in an immediate transmission (timing is controlled by ICC). The SBCX receives the second byte in the same manner as before. When transmission is completed, the ICC sends “End of Message” (MX-bit high).

It is assumed that a monitor command was sent that needs to be confirmed by the SBCX (e.g. EOC commands). Therefore the PEB 2081 commences to issue a two-byte confirmation after an End-of-Message indication from the ICC has been detected. The handshake protocol is identical to that of the ICC. The ICC notifies the µP via interrupt when new monitor data has been received. The processor may then read and acknowledge the byte at a convenient instant. When confirmation has been completed, the SBCX sends “EOM”. This generates a corresponding interrupt in the ICC. By setting the MR-bit to high, the monitor channel is inactive, the transmission is finished.

PEB 2055 and Monitor Channel Programming:

The EPIC-1 supports monitor transfers on a higher level than the ICC. Several modes are offered to support different types of monitor transfer. For communication with the SBCX, three are of special interest.

- Transmit Only. This mode is required when the EPIC sends monitor messages but no confirmation is returned by the SBCX (e.g. MON8 “Configuration Register”).
- Transmit and Receive. The EPIC transmits first and receives afterwards. Confirmations sent by the SBCX can be read (e.g. MON8 “Identification Register”).
- Searching for Active Monitor Channels. Listens to the IOM-monitor channel and reads information issued by the SBCX autonomously (e.g. MON1 S/Q-messages). Nothing is transmitted by the EPIC.

Unlike the ICC which had to respond to each change of the MR- and MX-bits individually (interrupt driven), the EPIC uses a FIFO for transmission and reception. The user therefore does not have to provide routines for the handshake protocol.

The example of **figure 37** demonstrates the use of EPIC-1 in the transmit-and-receive mode. As for the ICC it is assumed that the transferred monitor message will be followed by a two byte confirmation issued by the SBCX.

Before programming the FIFO, it is verified that the FIFO is empty and write access is possible. All monitor data is loaded into the FIFO (two bytes), the transmission channel and mode are selected. Writing “CMDR = 08” starts transmission of the FIFO contents and enables monitor data reception. After both bytes have been transmitted, the confirmation from the SBCX is read into the FIFO. After completion of the transfer an interrupt is generated. If the operation was successful, “STAR = 26” will indicate that data is loaded and the read access is enabled (in addition it is indicated that the PCM-synchronization status is correct). Following the readout of the confirmation bytes, the FIFO is cleared and the write access is selected again with the CMDR-register (“CMDR = 01”).
The handshake timing for byte transfer is identical to that described for the ICC. Both devices (EPIC and SBCX) handle it automatically.

EPIC® and Monitor Channel Programming

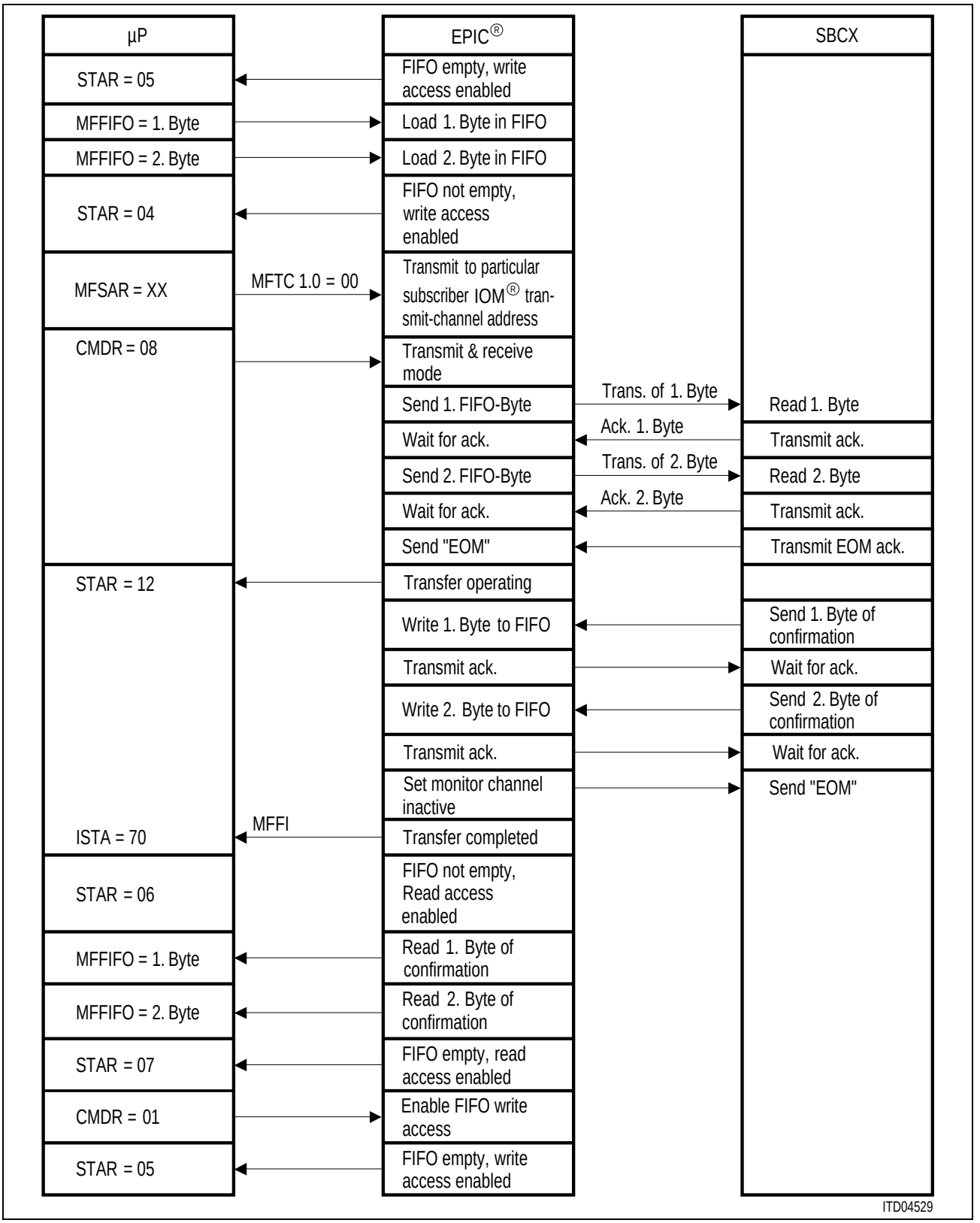


Figure 38
Monitor Channel Handling with EPIC® (all data values hexadecimal)

3.2.1.3.2 Monitor Procedure “Timeout” (TOD)

The SBCX offers an internal reset (monitor procedure “Timeout”) for the monitor routine. This reset function transfers the monitor channel into the idle state (MR and MX set to high) by issuing “EOM” (End of Message). Thereby possible lock-up situations will be resolved. It therefore is recommended to enable the internal timeout feature in all systems when no µP is capable of detecting and resolving hang-up situations in the monitor procedure (e.g. in a standard NT1).

The device checks for lock-up situation every 5 ms. In case a hang-up has been detected “EOM” will be issued on IDP0. Afterwards the original monitor message will be sent in the monitor channel again. The information thus is not lost after a monitor procedure timeout occurred.

In applications where a µP controls the system this internal reset function may be disabled by programming the TOD bit (timeout disable) in the SM/CI Register to ONE. In this mode no restrictions regarding the time for completing a monitor transfer exists.

3.2.1.3.3 MON-1, MON-2 Commands (S/Q Channel Access)

Monitor commands supported by the PEB 2081 divide into three categories. Each category derives its name from the first nibble (4 bits). The first two categories (MON-1 and MON-2) serve a similar function. They are therefore grouped together and will be described in more detail in this section. MON-8 commands are described in the next section.

Both MON-1 and MON-2 messages are also referred to as S/Q messages because they are used to read and write the registers containing the information of the S channel (direction NT → TE) or the Q channel (direction TE → NT) on the S-interface. Via the S-interface S/Q channel it is possible to exchange service or signalling information between the terminal and the network termination/exchange side. The S/Q channel is only available if multiframing was selected in the MFD bit of the MON-8 Configuration register. It is important to note that MON1/2 message provide only access to the device internal S/Q registers. Insertion and extraction of a message on the S-interface is handled automatically by the PEB 2081.

Currently no MON-1 and MON-2 commands are defined. The S/Q channel thus operates as a transparent channel only. In the direction NT → TE two channels are available. They are named S1 and S2 channel, each of them containing 4 bits of information. In the opposite direction one channel is provided (Q channel, also 4 bit wide).

The structure of a MON-1 message is shown below.

Table 4
MON-1 Structure

1 Byte							
0	0	0	1	S1/Q	S1/Q	S1/Q	S1/Q
MON-1				S1 or Q data			

The structure of a MON-2 message is similar:

Table 5
MON-2 Structure

1 Byte							
0	0	1	0	S2	S2	S2	S2
MON-2				S2 data			

The following table gives an overview of the S/Q messages available:

Table 6
MON-1, MON-2 Functions

TE		LT		Function
DD	DU	DD	DU	
S1-MON-1		S1-MON-1		Transmit and Receive in the S1 channel via MON-1 commands
S2-MON-2		S2-MON-2		Transmit and Receive in the S2 channel via MON-2 command
	Q-MON-1		Q-MON-1	Transmit and receive in the Q channel via MON-1 command

Non-Auto Mode / Transparent Mode

The use of the S/Q channel depends on the S/Q processing mode. The user can choose between the non-auto mode and the transparent mode. These two alternatives are independent of the operational mode the SBCX works in.

The non-auto mode is restricted to transfers in the S1 and Q channel. Channel S2 is not available in non-auto mode operation.

In non-auto mode a message in the IOM-2 monitor channel is generated only if the Q or S1 data has changed on the S-interface.

In transparent mode all three channels, Q, S1, and S2 can be accessed. IOM-2 monitor messages are generated everytime a complete S-interface multiframe has been received (i.e. every 5 ms). The generation of monitor messages thus is completely independent of the received S/Q data.

3.2.1.3.4 MON-8 Commands (Internal Register Access)

The PEB 2081 V 3.4 contains six internal registers. Access to these registers is only possible via the IOM-2 monitor channel. The following registers are implemented in the SBCX V 3.4:

- Identification Register
- Configuration Register
- Loop-back Register
- IOM-2 Channel Register
- SM/CI Register
- MAI Pin Register

The identification register is a read only register, all remaining registers are read/write registers.

The structure of MON-8 write and read request/response commands are shown in the three tables below:

Table 7
MON-8 “Write to Register” Structure

1. Byte								2. Byte							
1	0	0	0	r	r	r	r	D7	D6	D5	D4	D3	D2	D1	D0
MON-8				Reg. Address				Register Data Write							

In case this function is used in conjunction with multiple µP read command (see MAI pin register) a 5 byte long response message will result.

Table 8
MON-8 “Read Register Request” Structure

1. Byte								2. Byte							
1	0	0	0	0	0	0	0	0	0	0	0	r	r	r	r
MON-8												Reg. Address			

The response issued by the SBCX after having received a “Read Register Request” has the following structure.

Table 9
MON-8 “Read Response” Structure

1. Byte								2. Byte							
1	0	0	0	r	r	r	r	D7	D6	D5	D4	D3	D2	D1	D0
MON-8				Reg. Adr. Confirmation				Register Data Read							

The following sections describe the register features. For bit locations within a register, its initial value after reset and its address please refer to **chapter 4**.

3.2.1.3.5 MON-8 Identification Register

The contents of the identification register differs with the SBCX version. PEB 2081 V3.3 and 3.4 is identified with the code 42_{Hex}.

Former PEB 2081 versions identify themselves with the following codes:

PEB 2081	Identification
Version A1 … A3	40_{HEX}
Version B1, 2.2	41_{HEX}

3.2.1.3.6 MON-8 Configuration Register

In the configuration register the user programs the SBCX for different operational modes, selects required S-bus features and controls the function of the MAI interface.

The following paragraphs describe the application relevance of all individual configuration register bits.

MODE With this bit the user chooses between LT-S and LT-T operational mode. Default selection is LT-S mode. The setting of the MODE bit is only evaluated when pin MODE (No. 15 DIP) is set to ONE.

C/W/P This bit has three different meanings depending on the operational mode of the SBCX:
In **LT-S** and **NT** modes the S/T bus configuration is programmed. For point-to-point or extended passive bus configurations an adaptive timing recovery must be chosen. This allows the SBCX to adapt to cable length dependent round trip delays.
In **LT-T** mode the user selects the amount of permissible wander before a C/I code warning will be issued by the SBCX. The warning may be sent after 25 µs or 50 µs.
Note:
The C/I indication SLIP which will be issued if the specified wander has been exceeded, is only a warning. Data has not been lost at this stage.
In **TE** mode the frequency of the power converter clock at pin X0 (No. 18 DIP) is selected. The user has the choice between a 32 kHz (default) and a 16-kHz signal.

SQM Selects the SQ channel handling mode. In non-auto mode operation, the SBCX issues S1 and Q messages in the IOM-2 monitor channel only after a change has been detected. The S2 channel is not available in non-auto mode.
In transparent mode monitor messages containing the S1, S2 and Q data are forwarded to IOM-2 once per multiframe (5 ms), regardless of the data content. Programming the SQM bit is only relevant if multiframing on S/T is selected (bit MFD configuration register). See also MON-1 and MON-2 monitor messages.

RCVE Receive Code Violation Errors. The user has the option to issue a C/I error code (CVR) everytime an illegal code violation has been detected. The implementation is realized according to ANSI T1.605.

LP Loop Transparency. In case analog loop-backs are closed with C/I = ARL or bit SC in the loop-back register, the user may determine with this bit, whether the data is forwarded to the S/T-interface outputs (transparent) or not. The default setting depends on the operational mode. In LT-S and NT by default transparency is selected, for LT-T and TE non-transparency is standard.

FSMM Finite State Machine Mode. By programming this bit the user has the possibility to exchange the state machines of LT-S and NT, i.e. a SBCX pin strapped for LT-S operates with a NT state machine and vice versa. All other operation mode specific characteristics are retained (MAI interface, etc.).
This function is used in intelligent NT configurations where the SBCX needs to be pin-strapped to LT-S mode but the state machine of a NT is desirable.

MAIM MAI interface Mode. Selects between µP interface and I/O mode. The operation of the I/O mode is determined with the MIO bit in the SM/CI register (see MAI interface).

MFD Multi-Frame-Disable. Selects whether multiframe generation (LT-S, NT) or synchronization (TE, LT-T) is prohibited or allowed. Enable multiframing if S/Q channel data transfer is desired.
When reading this register the bit indicates whether multiframe synchronization has been established or not.

3.2.1.3.7 MON-8 Loop-Back Register

The loop-back register controls all analog (S/T-interface) and digital (IOM-2 interface) loop-backs. Additionally the wake-up mode can be programmed.

AST Asynchronous Timing.
Defines the length of the Timing signal (IDP0 = 0) on IOM-2. If synchronous timing is selected the SBCX in NT or LT-S mode will issue the timing request only in the C/I channel of the selected timeslot (C/I = 0000b). This mode is useful for applications where IOM-2 clock signals are not switched off. Here the SBCX can pass the TE initiated activation via C/I = 0000b in IOM-2 cannel 0 upstream to the U-interface device. In case IOM-2 clocks can be turned off during power-down or the LT-S SBCX is pin-strapped to a different timeslot than the U-interface device, synchronous timing signals will not succeed in waking the U-interface device. Under these circumstances asynchronous timing needs to be programmed. Here the line IDP0 is set to ZERO for a period long enough to wake any U-interface device, independent of timeslot or clocks. Typically asynchronous timing is programmed for intelligent NT applications (SBCX pin-strapped to LT-S with NT state machine).

Note:
The asynchronous timing option is restricted to configurations with the SBCX operating with NT state machine (i.e., LT-S pin-strap & FSMM bit programmed, or NT pin-strap & FSMM bit not programmed).

SB1 Closes the loop-back for B1 channel data close to the activated S/T-interface (i.e., loop-back IOM-2 data) in LT-S and NT mode.

SB2 Closes the loop-back for B2 channel data close to the activated S/T-interface (i.e., loop-back IOM-2 data) in LT-S and NT mode.

SC Close complete analog loop-back (2B+D) close to the S/T-interface. Corresponds to C/I = ARL. Transparency is optional. Operational in LT-S and NT mode.

IB1 Close the loop-back for B1 channel close to the IOM-2 interface (i.e. loop-back S/T data). Transparent. IB1 and IB2 may be closed simultaneously.

IB2 Close the loop-back for B2 channel close to the IOM-2 interface (i.e. loop-back S/T data). Transparent. IB1 and IB2 may be closed simultaneously.

IB12 Exchange B1 and B2 channels. IB1 and IB2 need to be programmed. Loops back data received from S/T and interchanges it, i.e. B1 input (S/T) → B2 output (S/T) and vice versa.

3.2.1.3.8 MON-8 IOM®-2 Channel Register

The features accessible via the IOM-2 Channel register allow to implement simple switching functions. These make the SBCX the ideal device for intelligent NT applications. Please refer also to the section “IOM-2 channel switching” later in this application guide. Two types of manipulation are possible: the transfer from the pin-strapped IOM-2 channel (0 … 7) into IOM-2 channel 0 and a change of the B1, B2 and D data source.

B1L Transfers the B1 channel from its pin-strapped location into IOM-2 channel 0.

B2L Transfers the B2 channel from its pin-strapped location into IOM-2 channel 0.

DL Transfers the D-channel from its pin-strapped location into IOM-2 channel 0.

B1D Direction of the B1 channel. Normally pin IDP1 is the data source (input) for all data channels and IDP0 the output. By programming this bit, input and output are interchanged for the B1 data channel, i.e. B1 (IDP0) is input and IDP1 is output.

B2D Direction of the B2 channel. Normally pin IDP1 is the data source (input) for all data channels and IDP0 the output. By programming this bit input and output are interchanged for the B2 data channel, i.e. B2 (IDP0) is input and IDP1 is output.

CIH C/I Channel handling: Normally the C/I commands are read from the pin-strapped IOM-2 channel. With this bit programmed C/I channel access is only possible via the SM/CI register.

DH D-Channel handling. Selects the protocol for D-channel access. Three alternatives exist:

- Transparent D data transmission
- D-channel collision resolution according to ITU I.430
- D-channel bus access procedure for intelligent NT applications or configurations involving the “new line card” concept.

An entire chapter is dedicated to D-channel access procedures later in this application guide. Details on all three methods including typical applications are described there.

3.2.1.3.9 MON-8 SM/CI Register

This multifeature register allows access to the C/I channel, sets the MAI interface mode and controls the monitor time-out and S/G bit function.

C/I — Allows the user to access the C/I channel if the CIH bit is the IOM-2 register has been previously set. If the CIH bit was not programmed the content of the CI bits will be ignored and the SBCX will access the IOM-2 C/I channel. When reading the SM/CI register these bits will always return the current C/I indication (independent of CIH bit).

TOD — Time Out Disable. Allows the user to disable the monitor time-out function. Refer to section “Monitor Timeout” earlier in this chapter for details.

SGE — S/G Enable. This bit is only relevant in TE mode. By programming it, the stop/go bit issued in the IOM-2 channel 2 will also be available at MAI pin No. 5 (pin No. 21, DIP). If this function is required the MAI interface must be programmed for “I/O specific” operation.

MIO — Maintenance Input Output. Provided bit MAIM was programmed for I/O operation of the MAI interface, bit MIO allows the choice between a standard I/O and I/O specific usage of the MAI interface. Refer to section “Maintenance Auxiliary Interface (MAI)” for details.

3.2.1.4 MAI Pin Register

In both I/O specific and standard I/O mode pin levels can be set and read with the MAI pin register. In case the I/O specific mode is implemented, only pins not used for I/O specific purposes may be read or written.

In case the µP mode is selected (MAIM bit) the MAI pins are redefined as follows to provide a complete µP interface.

$\overline{WR}$ — Write bit. The user sets the $\overline{WR}$ bit to low if data needs to be written to a specified address of the µP interface. The desired address and data must be written simultaneously with the $\overline{WR}$ bit into the MAI pin register.

$\overline{RD}$ — Read bit. Allows the user to read data from the specified address of the µP interface. Note that a read request must be sent to the SBCX with the “MON-8 Write to Register” structure. The distinction between write and read operation on the µP interface is only performed with the $\overline{WR}$ and $\overline{RD}$ bits.
With bit $\overline{INT}$ set to ONE an address needs to be specified. With $\overline{INT}$ set to ZERO all four µP addresses are read and returned in a single 5 byte long monitor message.

$\overline{INT}$ — Interrupt. Any change of the level on the $\overline{INT}$ pin of the µP interface will result in the C/I code MAIC to be issued on IOM-2 (for four frames). Additionally the $\overline{INT}$ bit is used to distinguish between a single address and multiple address reading (see $\overline{RD}$ bit or MAI interface).

A0, A1 — Address bits for µP interface.

D0, D1, D2 — Data bits for µP interface.

3.2.2 S/T-Interface

The S-interface establishes a direct link between terminals and the exchange or NT. It consists of two pairs of copper wires: one for the transmit and one for the receive direction.

The PEB 2081 inputs and outputs are coupled via matching resistors and transformers to the S-interface.

Direct access to the S-interface is not possible. 2B+D user data as well as S/Q channel information can be inserted and extracted via IOM-2 interface.

Framing and balancing bits are generated and transmitted automatically by the SBCX.

Because chapter 3 is application oriented and the user has no direct access possibility to the S-interface, the following sections give only an overview. For details please refer to the technical description in **chapter 4**.

S/T Frame Structure

Transmission over the S-interface is performed at a rate of 192 kbaud. For both directions of transmission a pseudo-ternary code is used.

Data is grouped together into S-frames containing 48 bits each, 36 bits contain 2B+D user data (i.e. user data from two IOM-2 frames packed into one S-frame). The remaining 12 bits are reserved for framing, S/Q and service bits.

In case multiframing is selected (optional) 20 S-frames are combined to one S-interface multiframe. The start of a new multiframe is marked by a special framing bit (see **chapter 4** for details).

Figures 39 and **40** illustrate the S-bus framing structure.

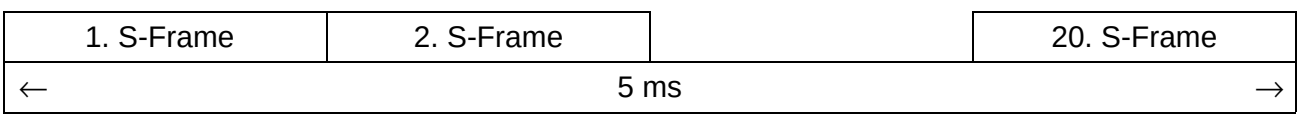


Figure 39
S Multiframe Structure

2 Bit F	8 Bit B1	5 Bit F+S+D	8 Bit B2	3 Bit F+D	8 Bit B1	3 Bit F+D	8 Bit B2	3 Bit F+D
←	250 µs							→

Figure 40
S-Frame Structure

3.2.3 Maintenance Auxiliary Interface (MAI)

The SBCX provides eight pins, MAI (7:0), for maintenance aids and general interface purposes. Two major operational modes are supported:

MAI Interface:

- I/O Mode
- µP Mode

The I/O mode offers two additional alternatives:

- I/O Specific Mode
- Standard I/O Mode.

To select between these three alternatives the “Configuration” and “SM/CI” registers are programmed. The following table illustrates the register settings:

Table 10

Configuration Reg. MAIM	SM/CI Register MIO	MAI Interface Mode
0	0	I/O Specific Mode
0	1	Standard I/O Mode
1	0	µP Mode
1	1	not applicable

The following sections describe the features of the different MAI modes and gives application examples.

3.2.3.1 I/O Specific Mode

The I/O specific function mode is selected automatically after a reset. Four pins (MAI 3:0) operate as inputs, four as outputs (MAI 4:7). Depending on the operational mode some of these MAI pins are used to transfer mode specific signals. Pins not required to convey these special signals are used as standard input or output pins.

All MAI pins are tristate during $\overline{RST}$ = ‘0’ or when the SBCX is in the state ‘reset’ unless MAIM is programmed to ‘1’. After reset all MAI pins are logically ‘0’ and work push/pull. The MAI pins are accessed via the MAI pin register MPR (address 5_H) using the monitor channel.

All input pins not allocated to I/O specific functions are monitored continuously. After a change was detected the input values are latched and the C/I indication MAIC will be issued. The input values remain latched until the MAI pin register was read via MON-8 command.

I/O specific input pin changes cause no C/I MAIC indication. The pin levels are nevertheless latched correctly everytime a MAIC indication was generated.

The following table illustrates the I/O specific pin allocation for all operating modes.

Table 11
I/O Specific MAI Interface

	LT-S	NT	LT-T	TE
MAI 0	i:$\overline{\text{NT-STAR}}$	i:$\overline{\text{NT-STAR}}$	i:MPR0	i:MPR0
MAI 1	i:MPR1	i:MFD	i:CON	i:CON
MAI 2	i:MPR2	i:$\overline{\text{TM1}}$	i:MPR2	i:MPR2
MAI 3	i:MPR3	i:$\overline{\text{TM2}}$	i:MPR3	i:MPR3
MAI 4	o:MPR4	o:MPR4	o:MPR4	o:MPR4
MAI 5	o:MPR5	o:MPR5	o:S/G	o:S/G
MAI 6	o:MPR6	o:MPR6	o:MPR6	o:MPR6
MAI 7	o:MPR7	o:MPR7	o:MPR7	o:MPR7

$\overline{\text{NT-STAR}}$: In NT or LT-S configurations optionally the NT-STAR mode may be used (see **sections 2.1.3** and **2.1.6**). In these configurations the IOM-2 bus is operated at a DCL rate of 512 kHz. All SBCX thus write onto the same IOM-2 channel. Because their outputs are logically ANDed “0”s win on the bus.

In the opposite direction all SBCXs receive identical information from the controller.

If an activation attempt is initiated from the upstream controller, the activation normally (i.e. without NT-STAR mode) can only be completed successfully when all terminals are connected. In case a single terminal was not connected the corresponding NT/LT-S SBCX would stop the activation process in the state “G2 pend. act.” because no INFO3 is received. In this state the C/I indication AR, binary code 1000b, is issued. The 3rd ZERO would overwrite the AI indications, binary code 1100b, from the remaining, correctly activated, SBCXs.

Programming the NT-STAR mode by setting this pin to ZERO avoids this conflict. A NT-STAR configuration can therefore be correctly activated even if not all terminals are connected.

Furthermore, transitions from the states “wait for AID” or “G3 activated” to “lost framing on S” under the condition of not receiving INFO3 is disabled.

MFD: Multi Frame Disable
In NT mode the transmission of the 5 ms multiframe signalling bits is disabled (M and S bits high) with a HIGH at this pin.

A LOW level enables the multiframe generation provided the MFD bit in the configuration register was not programmed to disable it.

The pin strapping has higher priority than the register setting.

CON: This input pin can be used to prevent a TE/LT-T from initiating an activation under emergency conditions. For this purpose it must be connected to a signal indicating the reverse polarity of a phantom power supply (e.g. pin $\overline{\text{EME}}$ of the PSB 2120).

A LOW level at this input (D-channel collision must be programmed via DH bit in IOM channel register) prevents transmission of INFO1 after AR (activation-request) has been received on the C/I channel.

An activation initiated by the network side (reception of INFO2/INFO4) is possible independently of the CON pin level.

In LT-T mode bit DH in the IOM-2-Channel register must be set to “1” to enable the CON pin functionality.

$\overline{TM1}$: Test Mode 1
A LOW at this input transfers the NT SBCX into test mode 1. In this test mode pseudo-ternary pulses are transmitted at a rate of 2 kHz.

$\overline{TM2}$: Test Mode 2
A LOW at this input transfers the NT SBCX into test mode 2. In this test mode pseudo-ternary pulses are transmitted at a rate of 96 kHz.

S/G: Stop/Go
This pin can be used to inform the D-channel controller in TEs and LT-Ts when the S-bus D-channel is occupied by another S-interface device (see **section 2.1.7**).
LT-T mode:
In LT-T mode this feature is only available after setting the DH bit in the IOM-2 register to ONE.
In case the S-interface D-channel is busy, the S/G pin is set to ZERO. This must be interpreted by the D-channel controller (e.g. IDEC) as a “stop D-channel transmission” indication.
In LT-T mode the S/G bit is set synchronously to the D-channel, i.e. the stop/go information is transmitted in the same time-slot as the corresponding SBCX is pin-strapped to. This mechanism allows the D-channel controller to distinguish between up to eight SBCX S/G pins (S/G = ‘0’ means ‘stop’, S/G = ‘1’ means ‘go’).
In mixed configurations with LT-T and LT-S mode devices connected together at pin MAI5, these MAI5 outputs have to be decoupled by using diodes. Otherwise the asynchronous push/pull outputs of the LT-S mode devices could disturb the synchronous (D-channel oriented) outputs of the LT-T mode devices.
TE mode:
In TE mode this feature is only available after setting the SGE bit in the SM/CI register to HIGH. In both operational modes the D and E bits on the S-interface are monitored continuously to issue always the correct S/G status. Requires the same pull-up resistor as IDP0.
In TE mode the S/G pin has the same polarity as the S/G-bit on IOM-2. S/G = ‘1’ stands for ‘stop’ and S/G = ‘0’ means ‘go’. As opposed to the LT-T mode pin S/G keeps its value between the D-channel time-slots on IOM-2.

Applications

I/O specific MAI pins are under control of the SBCX. The user therefore can only influence the standard I/O pins. Examples demonstrating the use of standard I/O pins are presented in the following section.

3.2.3.2 Standard I/O Mode

In standard I/O mode no pins are reserved for special signals. Thus four input and four output lines are available to the user for general purpose interface applications. Do not use this mode however when in need of special features like STAR operation, collision detection in LT-T/TE point-multipoint configurations etc. MAI0 and MAI3 are used for inputs. A change at any input pin will cause a MAIC C/I indication to be issued and the data to be latched. Data will remain latched until read out from the MAI pin register with a MON-8 command.

MAI4 and MAI7 serve as outputs. The pin level is determined by the corresponding bit level in the MAI pin register. The value specified for the lower four bits (inputs) does not matter.

Application

The following example illustrates the use of the standard I/O MAI interface. The same procedures apply to the I/O specific MAI mode for all pins not reserved for special signals.

IOM®-2			**SBCX**	
MON-8 Config: MAIM = 0	(8100_H)	→	–	; Select standard I/O
MON-8 SM/CI: MIO = 1	(8301_H)	→	–	
MON-8 MAI:	($85F0_H$)	→	MAI4 = (1) MAI5 = (1) MAI6 = (1) MAI7 = (1)	; Set all outputs to HIGH
C/I MAIC:	(0101)	←	(1) = MAI0 (0) = MAI1 (1) = MAI2 (0) = MAI3	; Change input levels
MON-8 MAI:	(8005_H)	→		; Read MAI register request
MON-8 MAI:	($85X5_H$)	←		; Return value MAI inputs

3.2.3.3 µP MAI Mode

The interface structure is adapted to the register structure of the IEPC. It consists of three data bits MAI0 … 2, two address bits MAI4,5, read and write signals MAI6 and MAI7 respectively as well as an interrupt facility MAI3.

The address bits are latched, they may therefore in general interface applications be used as output lines. For general interface inputs each of the three data bits is suitable. Read and write operations are performed via MON-8 commands. Three inputs and two outputs are thus available to connect external circuitry.

The interrupt pin is edge sensitive. Each change of level at the pin MAI3 will initiate a C/I code “MAIC” (0101) lasting for four IOM frames. Interpretation of the interrupt cause and resultant actions need to be performed by the control unit.

Usage of the µP interface differs from the standard I/O or I/O specific interface. As for these two interface types the µP interface makes use of the MAI pin register. However only MON-8 commands with the “write to register” structure may be used. The “read register request” structure is not interpreted if the MAI pin register is accessed in combination with the µP mode. The differentiation between a µP interface write operation and a µP interface read operation is performed only by activating either the $\overline{RD}$ or the $\overline{WR}$ bits within the MAI pin register. In both cases the “write to register” structure is used.

Depending on the $\overline{INT}$ bit specified together with a read µP interface request either the data from a single, specified address is read ($\overline{INT}$ = ONE) or all addresses are read ($\overline{INT}$ = ZERO).

In case only a single address is to be read, the SBCX returns the value in a 2-byte MON-8 message (structure: 85_H, MAI pin register). If all four addresses were read the response is a single 5 byte long (85_H, MAI Reg. (Adr0), … , MAI Reg. (Adr. 3)) MON-8 monitor message.

In this function the data from the following address will be read from the µP interface as soon as the previous MON-8 byte has been acknowledged on the IOM-2 bus by the controller.

Application

The following three examples illustrate a write operation as well as a single address and full address read operation. It is assumed that no power controller is connected. The data lines are clamped to the values specified in the examples, the address lines are unconnected.

1. Write to µP Interface:

	IOM®-2		**SBCX**	
→	MON-8 Config: MAIM	(8140_H)	–	; Program µP interface
→	MON-8 MAI:	($855E_H$)	MAI4 pin = (1)	; Activate $\overline{WR}$ signal, set
			MAI5 pin = (0)	; address 1 (latched)
			MAI2 pin = (1)	; Set data to value 6
			MAI1 pin = (1)	
			MAI0 pin = (0)	; (non-latched)

2. Read from µP Interface (single address):

	IOM®-2		SBCX	
			MAI2 pin = (1) MAI1 pin = (0) MAI0 pin = (1)	; Constant values on ; data lines
→	MON-8 Config: MAIM	(8140_H)	–	; Program µP interface
→	MON-8 MAI:	($85B8_H$)		; Activate $\overline{RD}$, $\overline{INT}$ = (1)
			MAI5 pin = (1) MAI4 pin = (1)	; read from address 3
←	MON-8 MAI:	($85BD_H$)		; 2 byte response incl. ; data lines from adr. 3

3. Read from µP Interface (complete address scan):

The following example assumes that a device capable of decoding addresses is connected to the µP interface. The data values to be returned from the addresses are:

Adr. 0: Data = 7
Adr. 1: Data = 6
Adr. 2: Data = 5
Adr. 3: Data = 4

	IOM®-2		SBCX	
→	MON-8 Config: MAIM	(8140_H)	–	; Program µP interface
→	MON-8 MAI:	(8580_H)		; Set $\overline{INT}$ = (0), activate $\overline{RD}$; read all addresses
←	MON-8 MAI:	(85 87 96 A5 $B4_H$)		; 5 byte response incl. ; data from adr. 0 … 3

3.3 Control Procedures

Control procedures describe the commands and messages required to control the PEB 2081 in different modes and situations. This chapter shows the user how to activate and deactivate the device under various circumstances. In order to keep this chapter as application oriented as possible only actions and reactions the user needs to initiate or may observe are mentioned. Technical details on transmitted status bits and signals are described in **chapter 4** of this manual.

For transfer of the C/I commands to and from the ICC or EPIC proceed as described in **section 3.2.1.2**.

3.3.1 Activation Initiated by Exchange (LT-S)

	TE/LT-T IOM®-2			**LT-S IOM®-2**				
←	C/I	DC	(1111b)	C/I	DC	(1111b)	←	; Initial state is G1 deactivated
→	C/I	DI	(1111b)	C/I	DI	(1111b)	→	; and F3 Power Down
←	C/I	RSY	(0100b)	**C/I**	**AR**	**(1000b)**	**←**	; Start activation
←	C/I	AR	(1000b)	C/I	AR	(1000)	→	
←	C/I	AI	(1100b)	C/I	AI	(1100)	→	; Activation completed
→	C/I	AR8/AR10	(1000b/1001b)					

3.3.2 Activation Initiated by Exchange (NT)

In case the counter station of the TE of LT-T is in NT mode the C/I “AI” command needs to be issued at the end. The first section of the activation procedure is identical to the activation with SBCX in LT-S mode.

	TE/LT-T IOM®-2			**NT IOM®-2**				
←	C/I	DC	(1111b)	C/I	DC	(1111b)	←	; Initial state is G1
→	C/I	DI	(1111b)	C/I	DI	(1111b)	→	; Deactivated and F3 ; Power Down
←	C/I	RSY	(0100b)	**C/I**	**AR**	**(1000b)**	**←**	; Activation starts
←	C/I	AR	(1000b)	C/I	AR	(1000)	→	
←	C/I	AI	(1100b)	C/I	AI	(1100)	→	
				C/I	**AI**	**(1100)**	**←**	; Transfer to G3 Activated
→	C/I	AR8/AR10	(1000b/1001b)					

3.3.3 Activation Initiated by Terminal (TE/LT-T)

The following scheme illustrates how a terminal initiates an activation. As described in the previous section the command C/I “AI” needs to be sent at the end if the device is operating in NT mode.

	TE/LT-T IOM®-2			LT-S (NT) IOM®-2				
←	C/I	DC	(1111b)	C/I	DC	(1111b)	←	; Initial state is G1 Deactivated
→	C/I	DI	(1111b)	C/I	DI	(1111b)	→	; and F3 Power Down
→	**C/I**	**TIM**	**(0000b)** [1]					; Request timing (IOM clocks)
←	C/I	PU	(0111b)					
→	**C/I**	**AR8**	**(1000b)**					
→	**TIM Release** [2]							; Start Activation
←	C/I	RSY	(0100b)					; Transfer to G3 Activated
←	C/I	AR	(1000b)	C/I	AR	(1000b)	→	;
←	C/I	AI	(1100b)	C/I	AI	(1100b)	→	;
				(C/I	AI	(1100b)	←	; Transfer to G3 Activated ; in NT mode)

Notes:
1) For PEB 2070 TIM is requested with register SPCR = 80_H
2) For PEB 2070 TIM is released with register SPCR = 00_H

3.3.4 Deactivation

A deactivation of the S-interface can only be initiated by the exchange side (SBCX in NT or LT-S mode). It is possible to begin a deactivation process from all interim activation states, i.e. not only from the fully activated state. The following example nevertheless assumes that the line is fully activated when the deactivation is initialized.

	TE/LT-T IOM®-2			NT/LT-S IOM®-2				
←	C/I	AI8	(1100b)	C/I	AI	(1100b)	→	; Initial state
←	C/I	DR	(0000b)	**C/I**	**DR**	**(0000b)**	**←**	; start deactivation
→	**C/I**	**DI**	**(1111b)**	C/I	TIM	(0000b)	→	;
←	C/I	DC	(1111b)	C/I	DI	(1111b)	→	; “G1 Deactivated”
				C/I	**DC**	**(1111b)**	**←**	; Transfer to “F3 Power Down”

3.3.5 D-Channel Access Control

D-channel access control was defined to guarantee all connected TEs and HDLC controllers a fair chance to transmit data in the D-channel. **Figure 41** illustrates that collisions are possible on the TIC- and the S-bus.

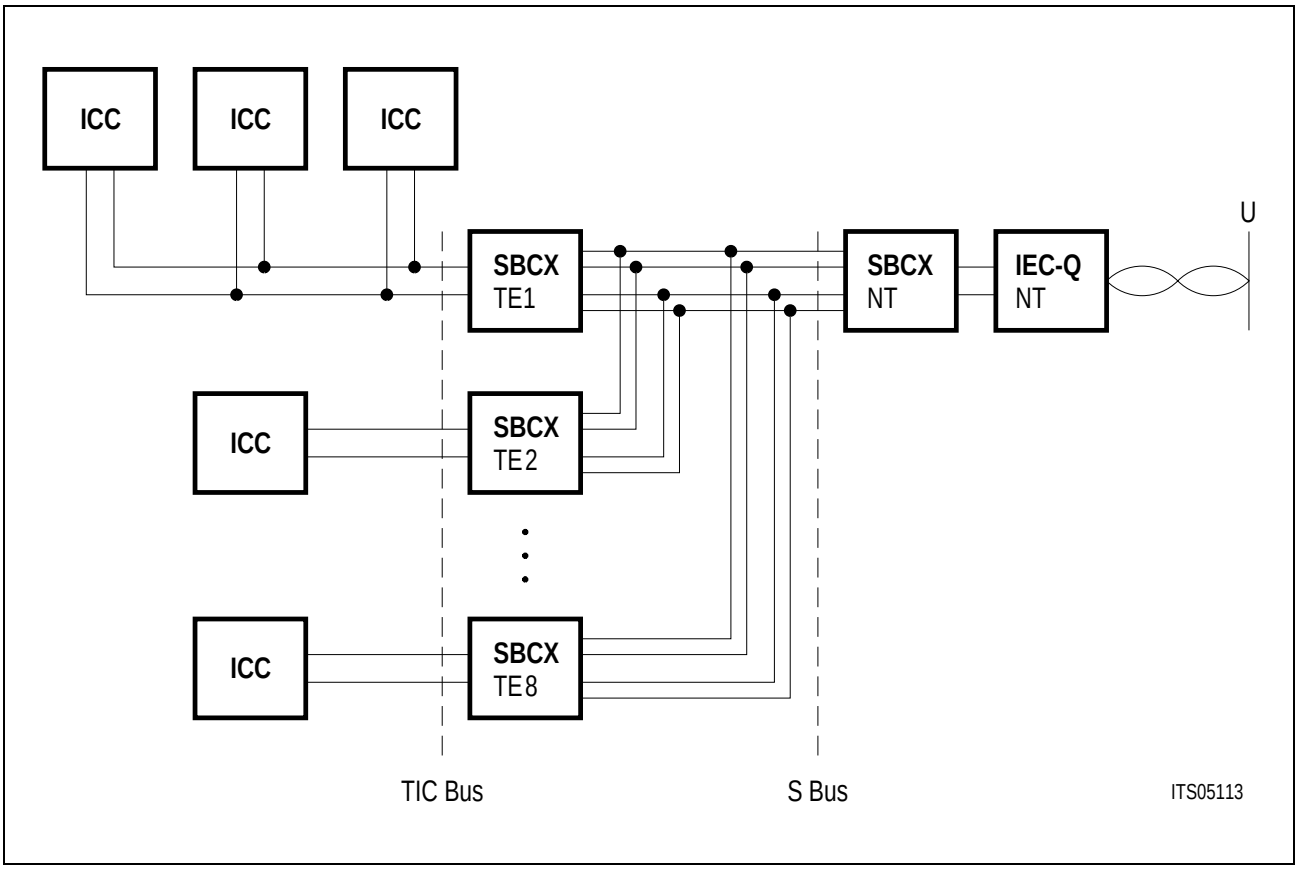


Figure 41
D-Channel Access Control on TIC Bus and S Bus

The TIC bus is used to control D-channel access on the IOM interface when more than one HDLC controller is connected. This configuration is illustrated in the above figure for TE1 where three ICCs are connected to one IOM-2 bus.

On the S bus the D-channel control is handled according to the ITU recommendation I.430. This control mechanism is required everytime a point to multipoint configuration is implemented (NT → TE1 … TE8).

While the S-bus collision detection is handled by the SBCX itself, TIC bus access is mainly controlled by the HDLC controller (e.g. ICC).

The following sections describe both control mechanisms because the TIC bus, although largely handled by the HDLC controller, represents an important part of D-channel access.

3.3.5.1 TIC Bus D-Channel Control in TE

The TIC bus was defined to organize D- and C/I channel access when two or more D- and C/I channel controllers can access the same IOM-2 timeslot. Bus access is controlled by five bits in IOM-2 channel No. 2 (see **section 3.2.1.1**):

Upstream:	BAC	Bus access control bit
	TBA0 … 2	TIC bus address bits 0 … 2
Downstream:	S/G	Stop/Go bit

When a controller wants to write to the D or C/I channel the following procedure is executed:

1. Controller checks whether BAC bit is set to ONE. If this is not the case access currently is not allowed: the controller has to postpone transmission. Only if BAC = 1 the controller may continue with the access procedure.
2. The controller transmits its TIC bus address (TBA0…2). This is done in the same frame in which BAC = “1” was recognized. On the TIC bus binary “ZERO”s overwrite binary “ONE”s. Thus low TIC bus addresses have higher priority.
3. After transmitting a TIC bus address bit, the value is read back (with the falling edge) to check whether its own address has been overwritten by a controller with higher priority. This procedure will continue until all three address bits are sent and confirmed.
   In case a bit is overwritten by an external controller with higher priority, the controller asking for bus access has to withdraw immediately from the bus by setting all TIC bus address bits to ONE.
4. If access was granted, the controller will put the D-channel data onto the IOM-2 bus in the following frame provided by the S/G bit is set to ZERO (i.e. S-bus free to transmit). The BAC bit will be set to ZERO by the controller to block all remaining controllers.
   In case the S/G bit is ONE this prevents only the D-channel data to be switched through to the IOM-2 bus. The TIC bus request remains unaffected (i.e. if access was granted the TIC address and BAC bit are activated). As soon as the S-bus D-channel is clear and the S/G bit was set back to “GO” the controller will commence with data transmission.
   The S/G Bit generation in IOM-2 channel 2 is handled automatically by the SBCX operating in TE mode. Additionally the Stop/Go information may be issued at the MAI5 pin by setting the SGE bit in the SM/CI register to ONE.
5. After the transmission of an HDLC frame has been completed the ICC controller withdraws from the TIC bus for one IOM-2 frame. This also applies when a new HDLC frame is to be transmitted in immediate succession. With this mechanism it is ensured that all connected controls receive an equally fair chance to access the TIC bus.

3.3.5.2 S-Bus Priority Mechanism for D-Channel

The S-bus access procedure specified in ITU I.430 was defined to organize D-channel access with multiple TEs connected to a single S-bus.

To implement collision detection the D (channel) and E (echo) bits are used. The D-channel S-bus condition is indicated towards the IOM-2 interface with the S/G bit (see previous section).

The access to the D-channel is controlled by a priority mechanism which ensures that to all competing TEs is given a fair access chance. This priority mechanism discriminates among the kind of information exchanged and information exchange history: Layer-2 frames are transmitted in such a way that signalling information is given priority (priority class 1) over all other types of information exchange (priority class 2). Furthermore, once a TE having successfully completed the transmission of a frame, it is assigned a lower level of priority of that class. The TE is given back its normal level within a priority class when all TEs have had an opportunity to transmit information at the normal level of that priority class.

The priority mechanism is based on a rather simple method: A TE not transmitting layer-2 frames sends binary 1s on the D-channel. As layer-2 frames are delimited by flags consisting of the binary pattern “01111110” and zero bit insertion is used to prevent flag imitation, the D-channel may be considered idle if more than seven consecutive 1s are detected on the D-channel. Hence by monitoring the D echo channel, the TE may determine if the D-channel is currently used by another TE or not.

A TE may start transmission of a layer-2 frame first when a certain number of consecutive 1s has been received on the echo channel. This number is fixed to 8 in priority class 1 and to 10 in priority class 2 for the normal level of priority; for the lower level of priority the number is increased by 1 in each priority class, i.e. 9 for class 1 and 11 for class 2.

A TE, when in the active condition, is monitoring the D echo channel, counting the number of consecutive binary 1s. If a 0 bit is detected, the TE restarts counting the number of consecutive binary 1s. If the required number of 1s according to the actual level of priority has been detected, the TE may start transmission of an HDLC frame. If a collision occurs, the TE immediately shall cease transmission, return to the D-channel monitoring state, and send 1s over the D-channel.

3.3.5.3 S-Bus D-Channel Control in TEs

The SBCX in TE mode continuously compares the D data bits with the received E-echo bits. Depending on the priority class selected, 8 or 10 consecutive ONEs need to be detected before setting the S/G bit to ZERO. With bit SGE in the SM/CI register the S/G bit may optionally be issued on pin MAI5.

The priority class (priority 8 or priority 10) is selected by transferring the appropriate activation command via the Command/Indication (C/I) channel of the IOM-2 interface to the SBCX. If the activation is initiated by a TE, the priority class is selected implicitly by the choice of the activation command. If the S-interface is activated from the NT, an activation command selecting the desired priority class should be programmed at the TE on reception of the activation indication (AI8). In the activated state the priority class may be changed whenever required by simply programming the desired activation request command (AR8 or AR10).

Application

1. Priority Class 8/10 Selection with NT Initiated Activation

	TE IOM®-2			LT-S (NT) IOM®-2				
←	C/I	DC	(1111b)	C/I	DC	(1111b)	←	
→	C/I	DI	(1111b)	C/I	DI	(1111b)	→	
←	C/I	RSY	(0100b)	C/I	**AR**	**(1000b)**	**←**	; Start activation from
←	C/I	AR	(1000b)	C/I	AR	(1000b)	→	; NT side
←	C/I	AI	(1100b)	C/I	AI	(1100b)	→	;
→	**C/I**	**AR8**	**(1000b)**	C/I	**AI**	**(1100b)**	**←**	; Allocate highest priority
	D: transfer HDLC frame							; (e.g. for signaling data)
→	**C/I**	**AR10**	**(1001b)**					; Allocate lower priority
	D: transfer packet data							; for packet data
←	C/I	AI10	(1101b)					

2. Priority Class 8/10 Selection with TE Initiated Activation

	TE IOM®-2			NT IOM®-2				
←	C/I	DC	(1111b)	C/I	DC	(1111b)	←	
→	C/I	DI	(1111b)	C/I	DI	(1111b)	→	
→	**C/I**	**TIM**[1]	**(0000b)**					; Request timing (IOM clocks)
←	C/I	PU	(0111b)					
→	**C/I**	**AR10**	**(1001b)**					; Activation with second
→	**C/I**	**TIM Release**[2]		C/I	AR	(1000b)	→	; priority (e.g. for packet data)
←	C/I	RSY	(0100b)	**C/I**	**AR**	**(1000b)**	**←**	
←	C/I	AR	(1000b)	C/I	AI	(1100b)	→	
←	C/I	AI10	(1101b)	**C/I**	**AI**	**(1100b)**	**←**	;
	D: transfer packet data							
→	**C/I**	**AR8**	**(1000b)**					; Allocate highest priority
	D: transfer HDLC frame							
←	C/I	AI8	(1100b)					

Note:
1) For PEB 2070 TIM is requested with register SPCR = 80_H
2) For PEB 2070 TIM is released with register SPCR = 00_H

3.3.5.4 S-Bus D-Channel Control in LT-T

In LT-T mode the SBCX is primarily considered to be in a point-to-point configuration. In these configurations no S-bus D-channel collision can occur, therefore the default setting after resetting the SBCX is transparent (IOM-2 $\rightarrow$ S-bus) D-channel transmission.

In case a point to multipoint configuration is implemented D-channel collision resolution according to ITU I.430 needs to be programmed in the “IOM channel register” [bit DH set to ONE]. In this mode the SBCX will issue a strobe signal at pin MAI5 (S/G bit) to control the LAPD controller IDEC.

This strobe signal is issued synchronously to the D-channel, i.e. in case more SBCXs operate in different IOM-2 channels (selection with pin strapping) each SBCX sends its S/G signal in its own IOM-2 channel. This allows the IDEC to distinguish between multiple S/G signals on a single S/G control line (see **section 2.1.7**).

Priority allocation is identical to that described for the TE mode. For application example refer also to the last section [DH bit must be set in addition].

3.3.5.5 D-Channel Control in the Intelligent NT (TIC-and S-Bus)

In intelligent NT applications both the SBCX and one or more D-channel controllers have to share a single upstream D-channel. For this purpose the SBCX must be programmed in the IOM channel register to perform a partial TIC bus evaluation [DH = “1”].

The intelligent NT configuration involves a layer-1 device (IBC, ISAC-P TE, IEC-Q) operating in TE mode (1.536 MHz DCL rate), one or more D-channel controllers and a SBCX in LT-S mode (D-channel transmitting in IOM-2 channel 0).

With the DH bit set to ONE, the SBCX V 3.4 in LT-S mode interprets the A/B, BAC bit and monitors the S-bus D-channel activity. Both S/G and BAC bit, the S-bus echo channel and the upstream IOM-2 D-channel data are controlled by these inputs according to the following procedure:

1. NT D-Channel Controller Transmits Upstream

In the initial state neither the intelligent NT D-channel controller nor any of the terminals connected to the S-bus transmit in the D-channel. The exchange indicates via the A/B bit (controlled by layer 1) that D-channel transmission on this line currently is permitted (A/B = “1”). Data transmission could temporarily be prohibited by the exchange when only a single D-channel controller handles more lines (A/B = “0”, ELIC-concept).

The SBCX thus receives A/B = “1”, BAC = “1” and transmits S/G = “0”. The access will then be established according to the following procedure:

- D-channel controller verifies that BAC bit is set to ONE.
- D-channel controller issues TIC bus address and verifies that no controller with higher priority requests transmission.
- D-channel controller issues BAC = “0”.
- SBCX reacts to BAC=”0” by transmitting the S/G bit with inverse polarity of the A/B bit $\Rightarrow$ S/G = “0”= $\overline{\text{A/B}}$.
- SBCX transmits inverted echo channel (E bits) on the S-bus to block all connected S-bus terminals (E = $\overline{\text{D}}$).
- D-channel controller commences with D data transmission on IOM-2 as soon as it receives S/G = “0”.

- After D-channel data transmission is completed the controller sets the BAC bit to ONE. [1)]
- SBCX pulls S/G bit to ZERO.
- SBCX transmits non-inverted echo (E = D).

Note:

1. Although the D-channel controller releases the TIC bus for one IOM-2 frame even if a new HDLC frame needs to be transmitted in immediate succession, this one frame period is not sufficient to allow a S-bus terminal to request the D-channel successfully. The reason is that at least 8 ONEs need to be recognized by a terminal in the echo-channel before it can start with D-channel transmission (in the meantime the intelligent NT D-channel controller would have aquired D-channel transmit permission again).
   To ensure equal access chances for the S-bus terminals, the intelligent NT controller software must delay any new TIC bus access request for at least 5 IOM-2 frames.

Figure 42 illustrates the signal flow in an intelligent NT and the algorithm implemented in the SBCX.

2. Terminal Transmits D-Channel Data Upstream

The initial state is identical to that described in the last paragraph. When one of the connected S-bus terminals needs to transmit in the D-channel, access is established according to the following procedure:

- SBCX (in intelligent NT) recognizes that the D-channel on the S-bus is active.
- SBCX sets S/G = 1 to block NT D-channel controller
- SBCX transfers S-bus D-channel data transparently through to the upstream IOM-2 bus (IOM-2 channel 0).
- After D-channel transmission has been completed by the terminal and the SBCX in the intelligent NT recognizes the idle condition on the S-bus D-channel, the S/G bit is set to ZERO.

In case the exchange prohibits D data transmission on this line the A/B bit is set to ZERO (block). This forces the intelligent NT SBCX to transmit an inverted echo channel on the S-bus, thus disabling all terminal requests, and switches S/G to $\overline{A/B}$, which blocks the HDLC controller in the intelligent NT.

Note:

1. Although the SBCX operates in LT-S mode and is pinstrapped to IOM-2 channel 0 or 1 it will write into IOM-2 channel 2 at the S/G bit position.

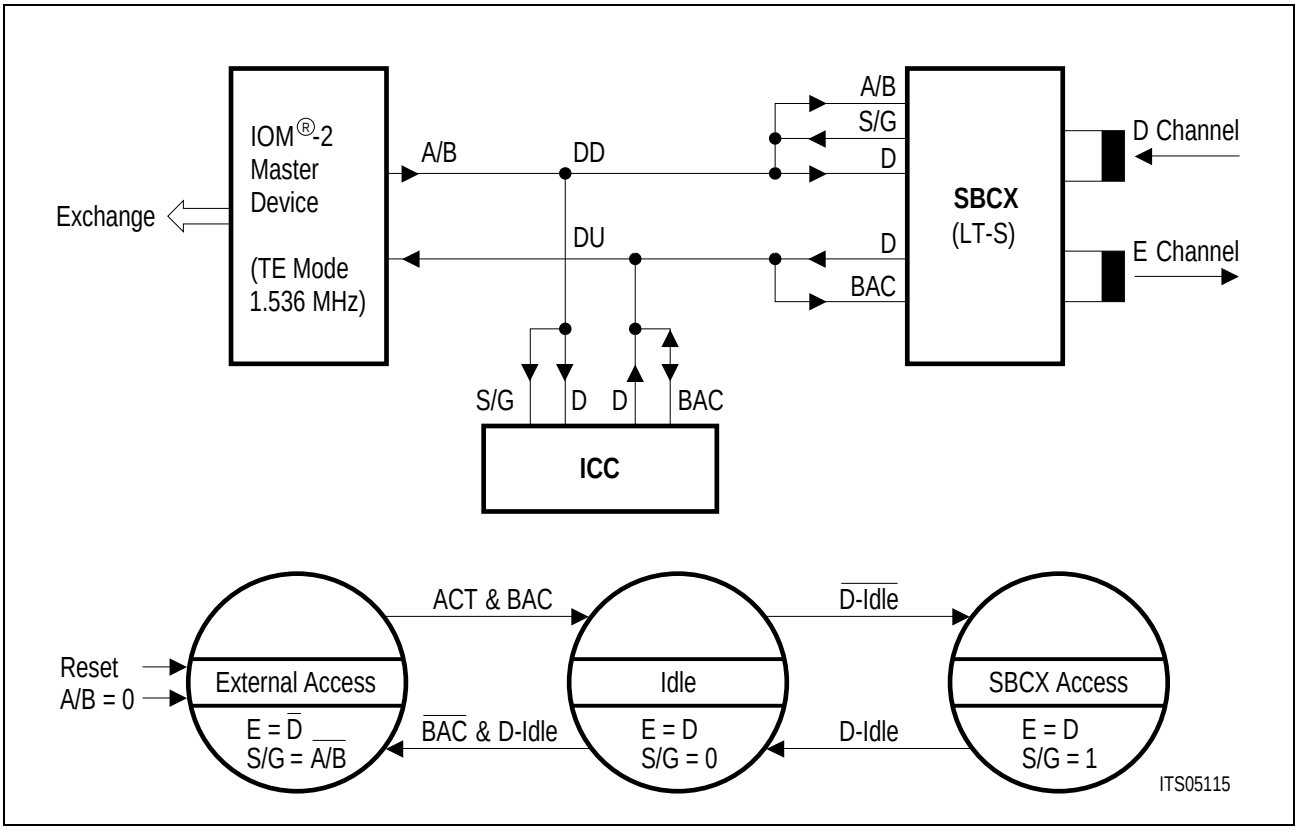


Figure 42
Data Flow for Collision Resolution Procedure in Intelligent NT

The SBCX uses the Echo-bit of the S-interface to control the transfer of D-channel information from the terminals at the S-interface. It also controls the state of the Stop/Go bit (S/G) and evaluates the A/B bit.

The state machine for D-channel access uses three states:

External access	The D-channel is occupied by another source indicated by the BAC-bit (BAC=0). The S/G bit corresponds to the invers of the A/B bit. The Echo-bits are set to '$\overline{D}$'.
Idle	The D-channel is transparent and no other device occupies the D-channel (BAC=1). The S/G bit is set to '0'. The Echo-bits correspond to the received D-bits of the S-interface.
SBCX Access	The D-channel is transparent and occupied by the SBCX. The S/G bit is set to '1'.

'D-Idle' is '1' if the received D-channel information from the S/T interface is idle (8 x '1'). 'D-Idle' changes to '0' after a '0' bit has been received from the S-interface D-channel.

'ACT' is set to '1' if the S-interface is in the activated state.

3.3.6 IOM®-2 Interface Channel Switching

In order to realize intelligent NT configurations the SBCX provides basic switching functions. These include:

- Individual channel transfer from IOM-2 channel 1 to IOM-2 channel 0.
- Individual channel reversion on input and output lines.

All switching functions are controlled via the MON-8 “IOM-2 channel” register (see MON-8 description). The following sections illustrate a variety of possible switching combinations typical for the intelligent NT. To facilitate the description of the switching function **figure 43** illustrates a typical intelligent NT with the speech CODEC ARCOFI combined with several terminals. Monitor programming for both ARCOFI and SBCX can only be performed in monitor channel 1.

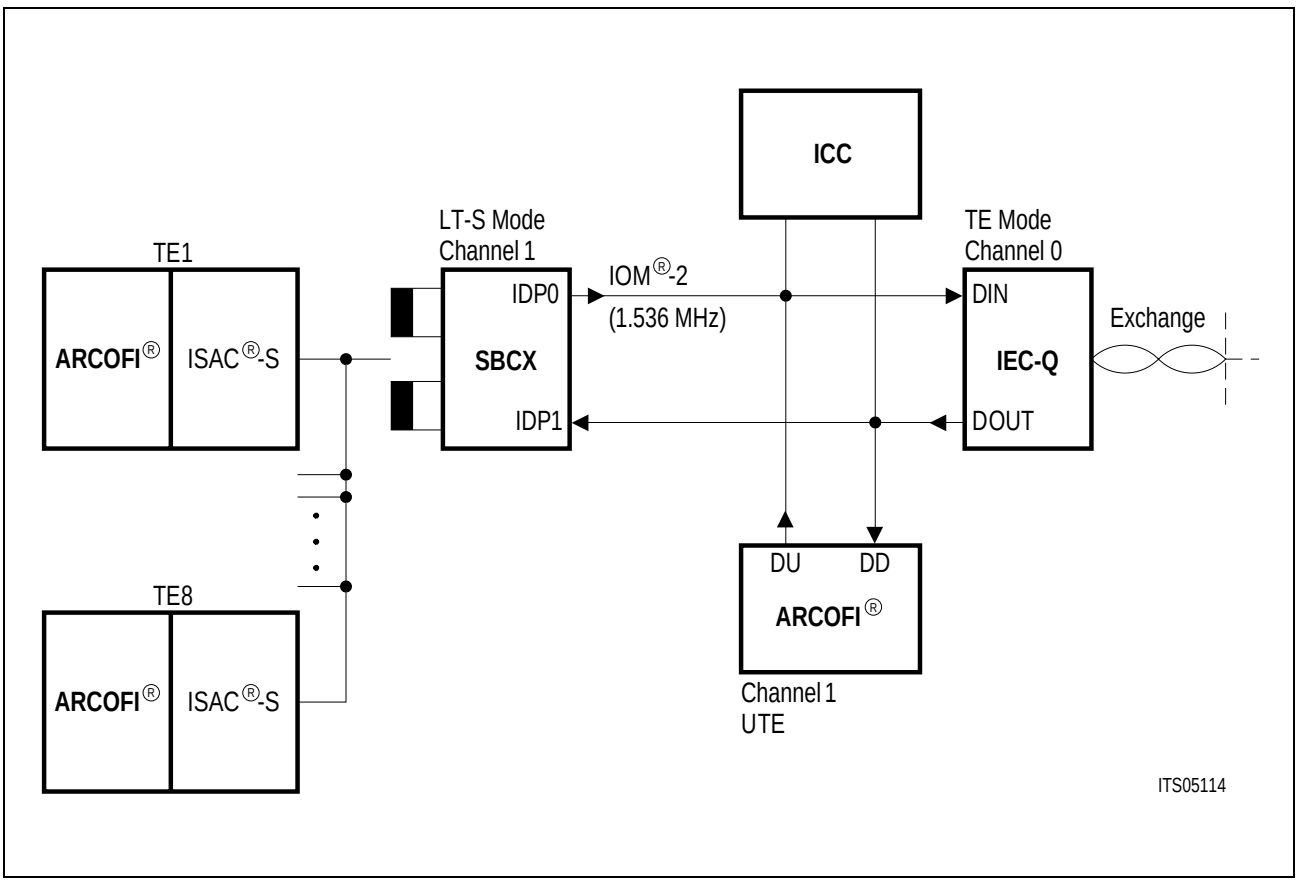
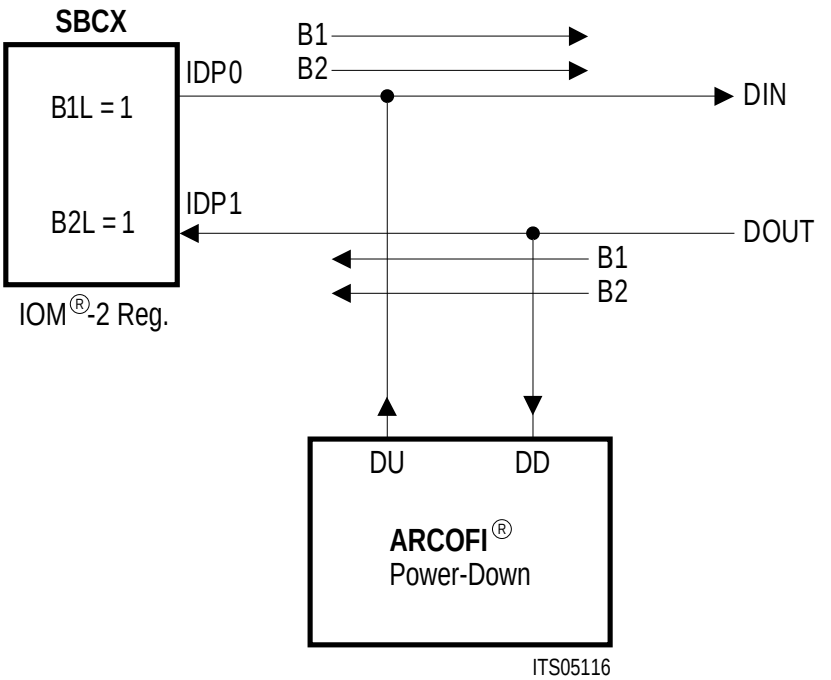


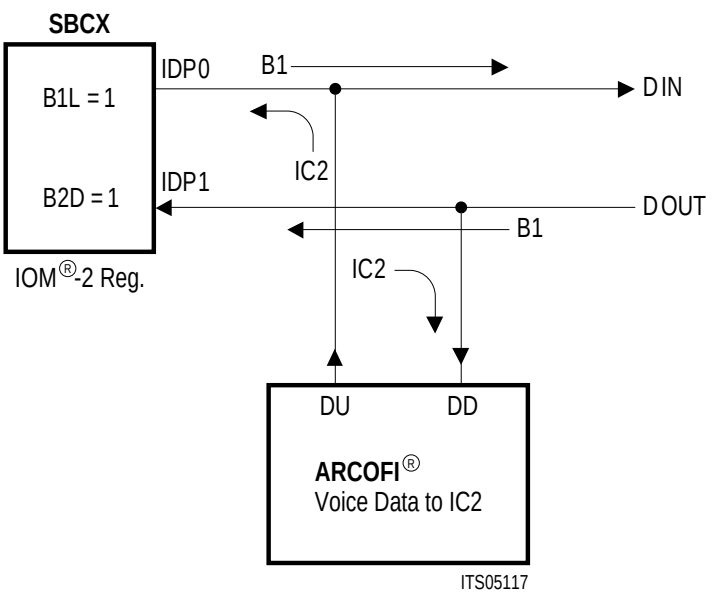
Figure 43
Intelligent NT-Configuration for IOM®-2 Channel Switching

The following four examples illustrate typical switching operations. Three of them are programmed in the “IOM-2 Channel” register, example No. 4 makes use of the “Loop-back” register. All register bits related to the B1 or B2 channel are set to ZERO unless otherwise stated.

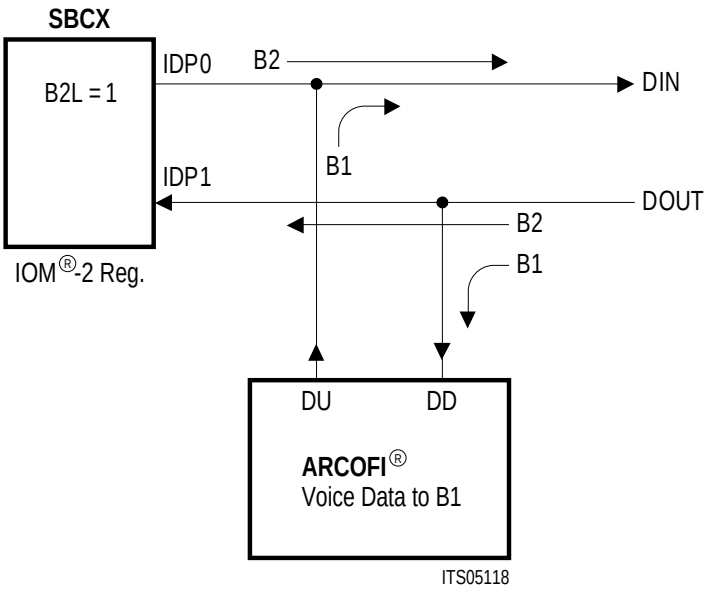
1. Connection B1 (e.g. TE1) → Exchange, B2 (e.g. TE8) → Exchange



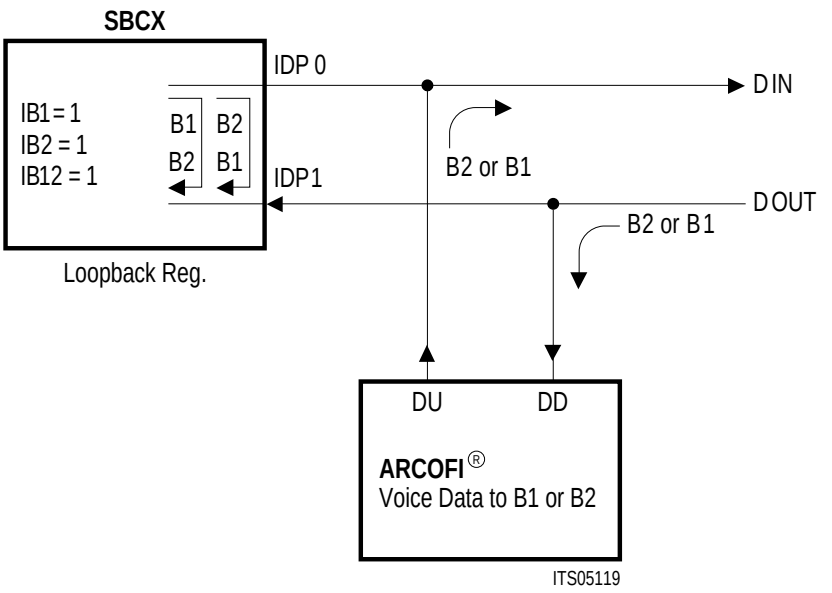
2. Connection B1 (e.g. TE1) → Exchange, B2 (e.g. TE8) → U-TE



3. Connection U-TE (B1) → Exchange, B2 (e.g. TE1) → Exchange



4. Connection TE1 (B1) ↔ TE8 (B2), U-TE (B1 or B2) → Exchange



3.4 Maintenance Functions

This chapter summarizes all features provided by the SBCX V 3.4 to support system maintenance and system measurements. Two main groups may be distinguished:

- maintenance function to close and open test loop-backs.
- test modes required for system measurements.

The next sections describe these maintenance functions and their applications.

3.4.1 Test Loop-Backs

Test loop-backs are specified by national PTTs in order to facilitate the location of defect systems. Each position of defined (ITU I.430 Appendix I) loop-backs is illustrated in **figure 44**.

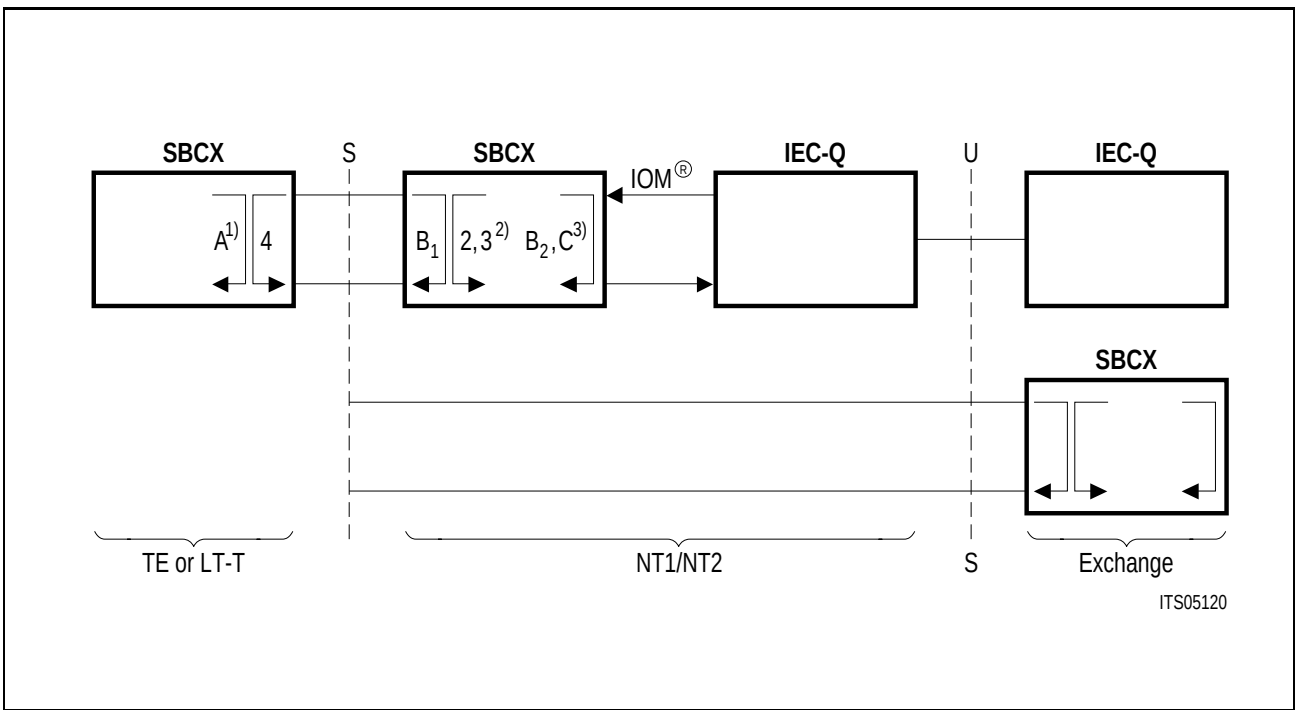


Figure 44
Test Loop-Backs Supported by PEB 2081

Notes:

1. In previous data sheets for the PEB 2081 ITU loop-back A was referred to as loop-back 3.
2. Loop-back 2 is closed in a NT1, loop-back 3 is closed in a NT2.
3. Loop-back C is closed in a NT1, loop-back B_2 is closed in a NT2.

Loop-back 2 is controlled by the exchange. Loop-back 4 may be under exchange or local control. Loop-backs A, B1, B2, C are initiated by the terminal or the NT2. Loop-back 3 is started by the NT2.

All loop-backs may be either transparent or non-transparent. Loops are closed in the SBCX with C/I commands or MON-8 register access [loop-back register]. The following sections describe the implementation of these loops in detail.

3.4.1.1 Complete Loop-Backs (No. 2, No. 3, and No. A)

Internal Loop-Backs

In a complete loop, all three channels (B1, B2 and D) are looped back at the S/T-interface. In a “transparent loop” the data are also sent forward (in addition to being looped back), whereas in a “non-transparent loop” the forward data path is blocked (ITU I.430).

Loop A is activated with C/I channel command Activate Request Loop (ARL). An S/T-interface is not required since INFO3 is looped back to the receiver internally. When the receiver has synchronized itself to this signal, the message “Activate Indication Loop” (AIL) is delivered in the C/I channel. No signal (INFO0) is transmitted over the S/T-interface. If, during loop A, an incoming signal is detected on the line, this is indicated by the message “Resynchronization” (RSY), although the loop is maintained. It is in the responsibility of layer-2 control to release loop A.

Loop 2 and Loop 3 is similarly activated over the IOM-2 interface with Activate Request Loop (ARL). No S/T line is required. INFO4 is looped back to the receiver and also sent to the S/T-interface. When the receiver is synchronized, the message “AI” is sent in the C/I channel. Setting the LP-bit in the configuration register to ONE will make loop 2,3 non-transparent.

While loop-back A is closed unconditionally (i.e. loop-back A may be started from any state in TE or LT-T mode), loop-backs 2 and 3 may be initiated from three (LT-S) resp. four (NT) states (see state machine NT and LT-S mode in **chapter 4**).

The following examples demonstrate the use of loop-backs A, 2 and 3.

1. Loop-Back A (TE or LT-T)

	TE/LT-T	**IOM-2**		
←	C/I	Any state XX	(XXXXb)	; Unconditional command
→	**C/I**	**ARL**	**(1010b)**	; Close loop-back A
←	C/I	ARL	(1010b)	
←	C/I	AIL	(1110b)	; Loop-back closed successfully
(→	C/I	RSY	(0100b)	; Incoming signal detected)

2. Loop-Back 2, 3 Transparent (NT1 or NT2)

	LT-S/NT	**IOM®-2**		
→	C/I	DC	(1111b)	; Initial state is “G1 deactivated”
←	C/I	DI	(1111b)	
→	C/I	ARL	(1010b)	; Close loop-back 2, 3
←	C/I	AR	(1000b)	
←	C/I	AI	(1100b)	; Loop-back closed successfully

External Loop-Backs

In order to enable complete systems diagnostics (including transformers etc.) it is possible to close an external loop at the four wire S/T-interface. In that case the signal transmitted onto the line is fed to the receiver.

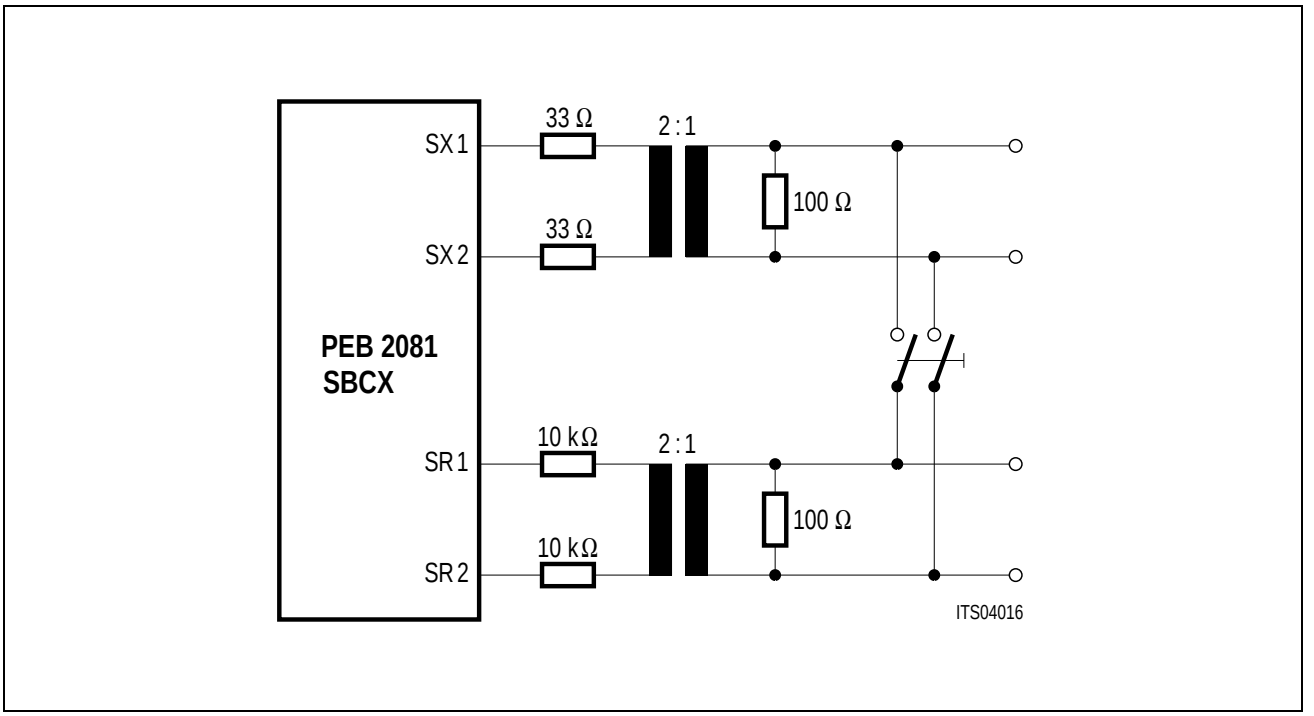


Figure 45
External Loop at the S/T-Interface

In **NT/LT-S mode** the SBCX is ready to run in this configuration by performing a normal activation.

In **TE/LT-T mode** the LP-bit (configuration register) has to be set to one and then the loop has to be activated using the “ARL” command. The C/I sequence occurring at the IOM-2 interface will correspond to that of the activation of loop A. The SBCX is in the state ‘loop A activated’ and transmits the indication RSY instead of AIL.

3.4.1.2 Single Channel Loop-Backs (No. 4, No. B1/2, No. C)

With the S/T-interface being in the activated state single channel loops are possible for the B channels in all directions, i.e. from the S/T-interface to the IOM-2 interface and back or vice versa. They are involved by setting the according bit in the Loop-back Register. Please note, that setting the SC-bit has the same effect as closing loops No. 2 or 3 respectively with the equivalent C/I command.

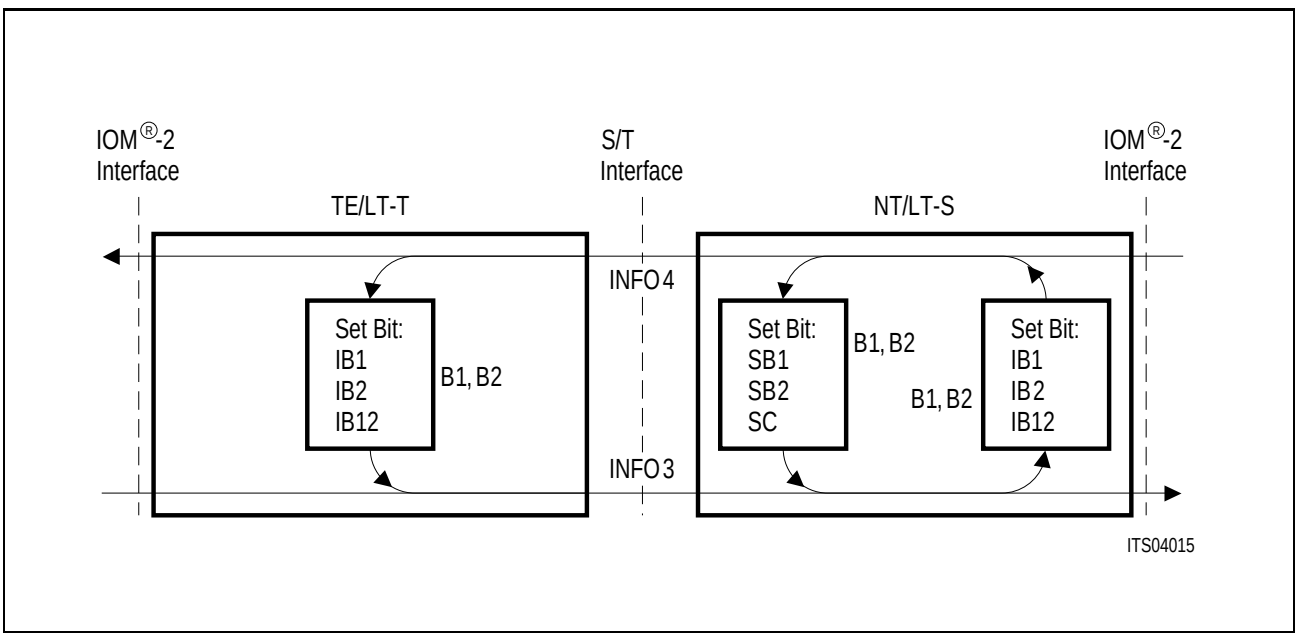


Figure 46
Single Loops of the SBCX

3.4.2 Monitoring of Illegal Code Violations

The SBCX V 3.4 offers the option of monitoring the S-bus for illegal code violations. If bit RCVE in the configuration register is set to ONE a Far End Code Violation (FECV) function according to ANSI T1.605 is implemented. This feature is available independently of multiframing on the S/T-interface.

3.4.3 Test Modes and System Measurements

The SBCX V 3.4 supports system measurements with two special test modes. In the next section these modes are described in detail. The sections following the test mode description present an overview over the most important system measurements.

3.4.3.1 Test Mode 1

In test mode 1 the SBCX issues alternating pulses at a frequency of 2 kHz. In other S-interface devices this mode is also referred to as “Send Single Zeros”. Test mode 1 (TM1) may be used in all operational modes supported by the SBCX.

This mode is selected with a C/I command:

– software selection: C/I = TM1 (0010b)

In case the SBCX is operated in TE or LT-T mode the device will return the same binary C/I code after the test mode has been started successfully.

In NT or LT-S mode the C/I indication “TIM” is issued from the “Test Mode” state.

3.4.3.2 Test Mode 2

In Test Mode 2 (TM2) the SBCX issues alternating pseudo-ternary pulses at a frequency of 96 kHz. In other S-interface devices this mode is also referred to as “Send Continuous Zeros”. Test mode 2 may be used in all operational modes supported by the SBCX.

This mode is selected with a C/I command:

– software selection: C/I = TM1 (0011b)

In case the SBCX is operated in TE or LT-T mode the device will return the same binary C/I code after the test mode has been started successfully.

In NT or LT-S mode the C/I indication “TIM” is issued from the “Test Mode” state.

3.4.3.3 Pulse Mask Measurement

- Pulse Mask defined in ITU I.430 section 8.5.3
- S-interface is terminated with:
  - 50 Ω (TE and NT equipment)
  - 400 Ω (TE equipment only)
  - 5.6 Ω (TE equipment only)
- B-channel loop is neccessary
  → IB1, IB2 in Loopback Register
  or
  → Loop in switching unit
- Measurement performed with oscilloscope or Siemens K1403
- Possible problems:
  - 50 Ω test not successful → modify transmitter resistors on S/T-interface circuitry
  - 400 Ω test shows undershoot → minimize capacitances in the external circuitry

3.4.3.4 NT Transmitter Output/Receiver Input Impedance

- Impedance Templates defined in ITU I.430 sections 8.5.1.1 and 8.6.1.2
- Output impedance measurement:
  - inactive or transmission of binary ONEs. Applies sinusoidal voltage of 100 mVrms. Requirement: template
  - transmission of binary ZEROs. Requirement: ≥ 20 Ω
    - 50 Ω S-interface termination
    - 400 Ω S-interface termination
- Input impedance measurement:
  - Applied sinusoidal voltage of 100 mVrms.
    Requirement: template
  - Applied 96 kHz frequency with 1.2 V peak value.
    Requirement: current ≤ 0.6 mA
- SBCX is in “deactive” state when transmission of binary ONEs is required and in TM1 when transmission of binary ZEROs is required.
- Measurement performed with impedance analyzer or Siemens K1403
- Possible problems: Not known.

3.4.3.5 TE Transmitter Output/Receiver Input Impedance

- Impedance templates defined in ITU I.430 sections 8.5.1.2 and 8.6.1.1.
- Input and output measurements are identical:
  - inactive and power-down or transmission of binary ONEs. Applied sinusoidal voltage of 100 mVrms.
    Requirement: template.
  - inactive and power-down or transmission of binary ONEs. Applied 96-kHz frequency with 1.2 V peak value.
    Requirement: Current ≤ 0.6 mA
- Terminal and SBCX not powered.
- Measurement performed with impedance analyzer or Siemens K1403.

- Possible problems:
  - Impedance measurement with 96 kHz exceeds current limit → transfer 10 kΩ resistors in S/T-interface circuitry between transformer and protection circuit (see also S/T-interface recommendation in **chapter 4**).

3.4.3.6 NT/TE Timing Extraction Jitter

- Requirement defined by ITU I.430 sections 8.2.2 and 8.3.
- TE timing extraction jitter input data sequences:
  - Binary ONEs in 2B+D+E
  - 40 frames “10” pattern in B1 and B2 and continuous ONEs in D and E channels followed by 40 frames continuous binary ZEROs in 2B+D+E.
  - Pseudo random pattern with length $2^{-19} - 1$ in 2B+D+E channels

  The output sequence in all cases consists of binary ZEROs in B1 and B2.
  Requirement: 14 % of a bit period (≙ 729 ns) may not be exceeded.
- NT jitter requirements input data sequences:
  - Pseudo random pattern with length $2^{-19} - 1$ in 2B+D channels.

  The output data sequence consists of binary ONEs in 2B+D channels.
  Requirement: jitter ≤ 5 % of a bit period.
- The SBCX is in state ”F7/G3 Activated” transmitting continuous ZEROs in B1 and B2.
- For a first jitter evaluation the envelope function of an oscilloscope may be used. Detailed analysis with Siemens K1403.
- Possible problems:
  - Technically no problems exist, confusion may be caused by interpretation of results in TE jitter measurements. The specification requires ± 7 %, due to lack of a fixed reference point this results in 14 % peak to peak tolerance.

3.4.3.7 TE Total Phase Deviation

- Requirement defined by ITU I.430 in section 8.2.3.
- TE phase deviation input patterns:
  - Continuous binary ONEs in 2B+D+E
  - Continuous binary “10” pattern in B1 and B2 combined with continuous binary ONEs in D+E channels.
  - Continuous binary ZEROs in 2B+D+E
  - Pseudo random pattern with length $2^{-19} - 1$ in 2B+D+E.

  Requirement: in addition to the 2 bit default offset the output phase must be within
  – 7% – + 15 % of a bit period.
- The SBCX is in the state “F3 Activated” transmitting continuous ZEROs in B1 and B2.
- For a first evaluation an oscilloscope may be used. Detailed analysis with Siemens K1403.
- Possible problems: Not known.

3.4.3.8 TE and NT Longitudinal Conversion Loss (LCL)

- Requirement defined by ITU I.430 in section 8.5.6.1.
- Measurement conditions:
  - all possible power feeding conditions.
  - all possible connections set to ground.
  - 100 Ω termination across transmit and receive ports.

  Requirements: template
- For LCL tests the SBCX is put into power-off, deactivated and activated condition. The test setup is described in ITU.
- Spectrum analyzer and signal generator in combination with S-interface measurement bridge or Siemens K1403.
- Possible problems: Not known.

3.4.3.9 TE and NT Output Signal Balance (OSB)

- Requirements defined by ITU I.430 in section 8.5.6.2.
- Measurement conditions:
  - all possible power feeding conditions.
  - all possible connections of the equipment to ground.
  - 100 Ω termination across transmit and receive ports.

  Requirements: template.
- SBCX is in active state and transmits continuous ZEROs in B1 and B2 channels. For test setup refer to ITU.
- Spectrum analyzer and signal generator in combination with S-interface measurement bridge or Siemens K1403.
- Possible problems: Not known.

3.4.3.10 TE Frame Rate Info1

- Requirements defined by ITU I.430 in section 8.1
- The nominal frame rate of Info1 should be 24 kHz ± 100 ppm
- Frequency counter or Siemens K1403
- Possible problems: frame rate exceeds limit
  - adjust oscillator frequency, take crystal with less tolerance

3.4.3.11 Loss and Regain of Frame Alignment (TE)

- Values have to be stated in PICS/PIXIT list
- SBCX V3.4: m = 3 or 4, n = 2

4 Technical Description

Chapter 4, “Technical Description”, is structured similar to **chapter 3** in order to facilitate cross-referencing. **Chapter 4** is dedicated to technical information only. It describes the interfaces, control procedures, maintenance functions and the analog line port. The user is intended to refer to chapter 4 when in need of specific technical details. For information on a particular application please refer to **chapter 3**.

4.1 Interfaces

This section describes the interfaces IOM-2, S, and MAI. In addition, a section with technical information on the analog line port (analog receiver and transmitter for the S-interface) was included. All dynamic characteristics are treated in these sections.

4.1.1 IOM®-2 Interface

General

Via the IOM-2 interface data is transmitted in both directions (DU and DD) at half the data clock rate. The data clock (DCL) is a square wave signal with a duty cycle ratio of typically 1:1. Incoming data is sampled on the falling edge of the DCL clock. The frequency is variable and can be set for values ranging from 512 kHz to 4.096 MHz.

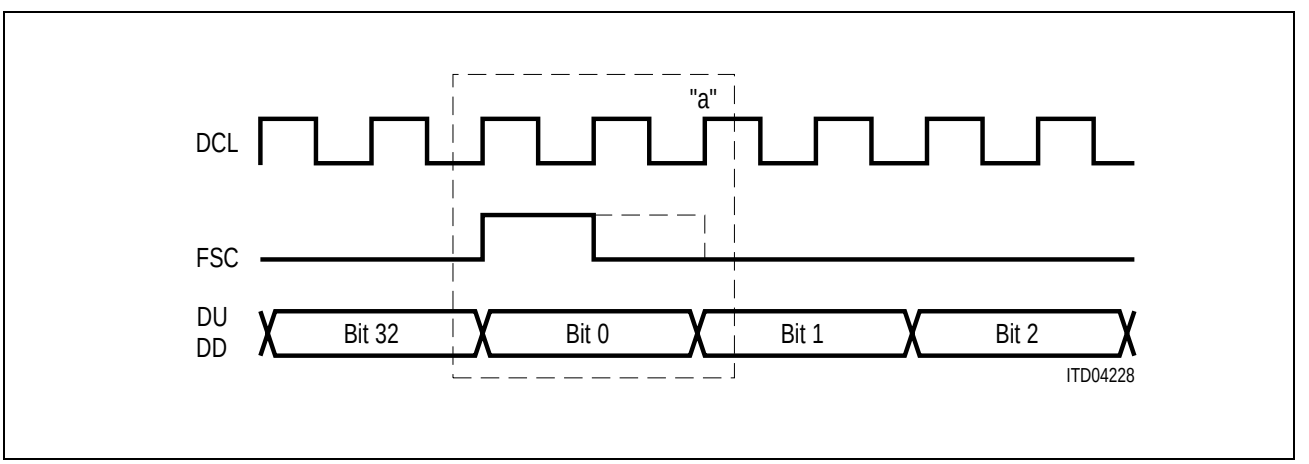


Figure 47
IOM®-2 Interface Timing

The frame clock (FSC) is an 8-kHz signal for synchronizing data transmission on DU and DD. The rising edge of this signal gives the time reference for the first bit transmitted in the first IOM-2 channel.

The IOM-2 interface specification describes open drain data lines with external pull-ups. However if operation is logically point-to-point, tristate operation is possible as well. After reset, the SBCX V3.4 senses whether an external pull-up resistor is connected to pin IDP0. If not the SBCX switches automatically to tristate operation (refer to **chapter 4.4.3**).

Multiframe Marker

In **NT** and **LT-S mode the signaling** of the multiframe identification on the S-interface is performed automatically by the SBCX. The multiframe generation can be disabled by pin strap (NT pin MAI1 tied to high) or by programming (MFD-bit configuration register).

In NT and LT-S mode the S/T-interface superframe with 5 ms period can be synchronized to a master device by modulation of the pulse width of FSC.

The SBCX samples the FSC input with the second falling edge of DCL in the very first bit of the frame and resets the S/T-interface transmit frame, including multiframe, if the sample bit is zero. The remaining FSC clocks must be of **at least two DCL periods** duration.

The relationship between the IOM-2 multiframe marker of the slave, the S-interface, and the IOM-2 superframe marker of the master is fixed after activation of the S-interface. I.e. data inserted on LT side in the first B1-channel after the IOM-2 slave superframe marker will always appear on NT side with a fixed offset.

The following figure shows the frame relationship between IOM-2 interface and S/T-Interface.

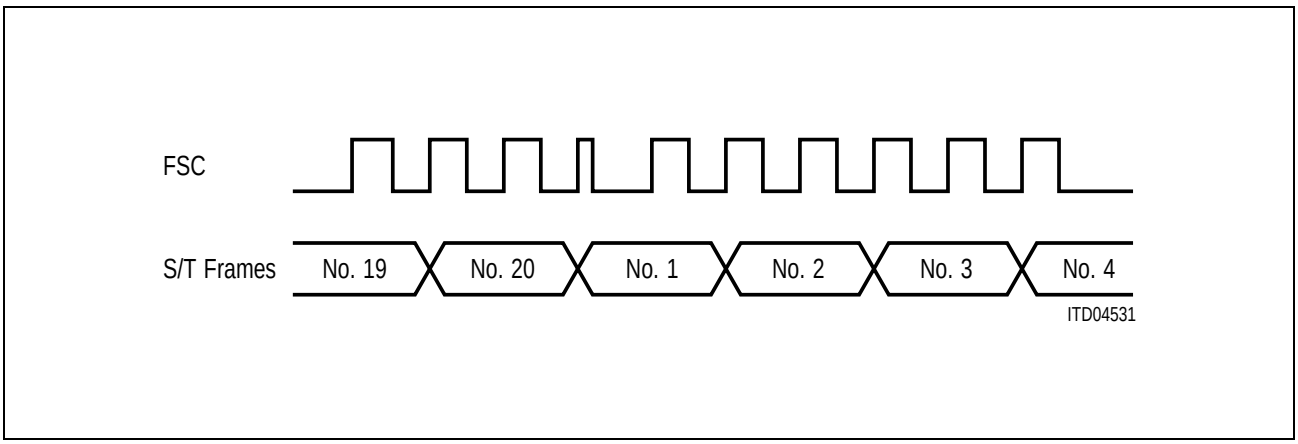


Figure 48
S/T-Interface Multi-Frame Synchronization

Please note, that in a NT application the superframe marker of IEC-Q must be disabled due to different multiframe periods of U- and S-interface.

Power-Down

For power saving reasons, the IOM-2 interface can be switched into a “power-down” state (i.e. state “DEACTIVATED” in the status diagram). In this case, the idle state of the data lines are HIGH, while those of the clock lines are LOW.

4.1.1.1 IOM®-2 Dynamic Characteristics

In case the period of signals is stated the time reference will be at 1.4 V; in all other cases 0.8 V (LOW) and 2.0 V (HIGH) thresholds are used as reference.

The following two diagrams illustrate the timing requirements for TE mode and NT, LT-S or LT-T mode.

Timing Characteristics IOM®-2 Interface in TE Mode

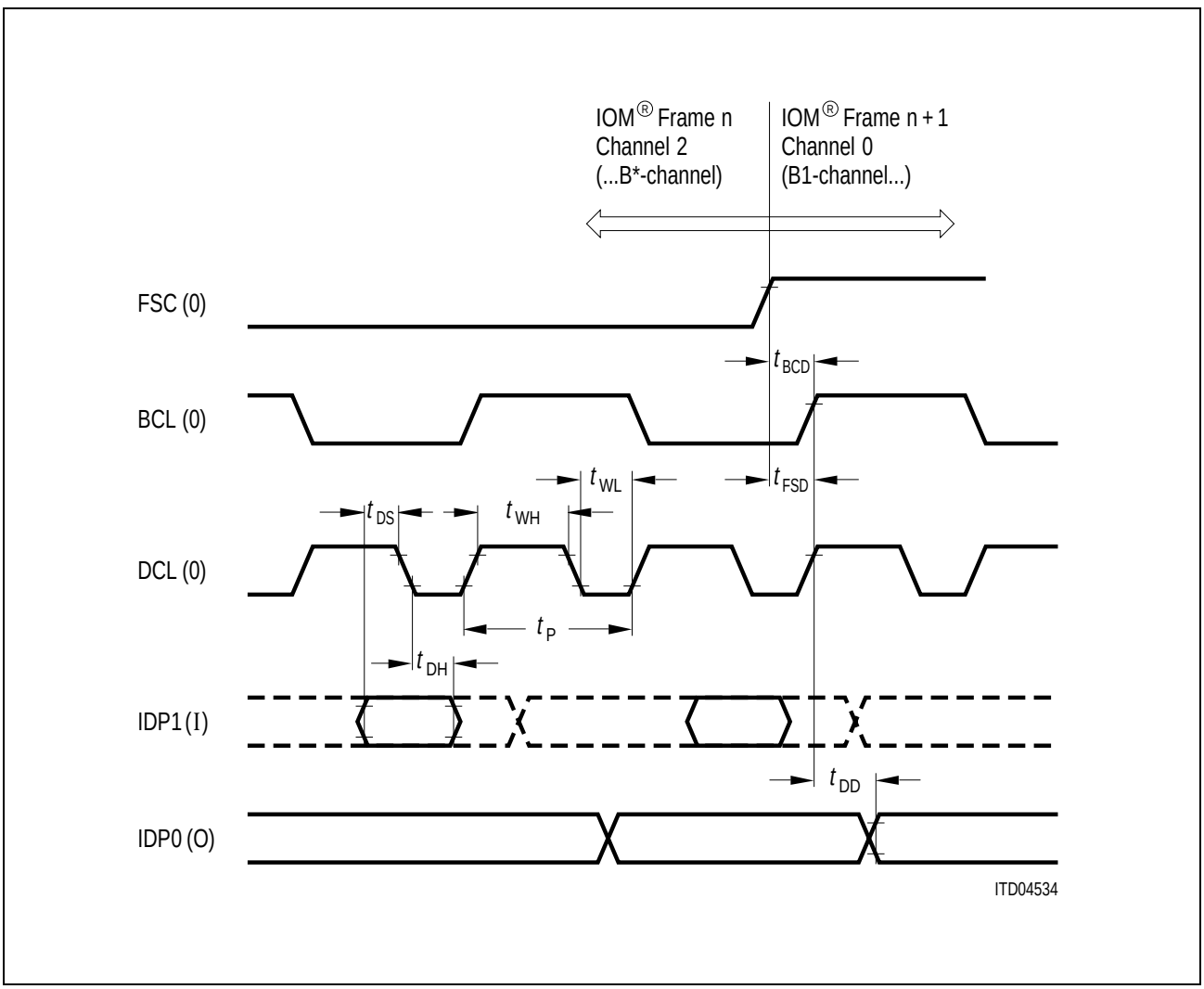


Figure 49
Timing of the IOM®-2 Interface in TE Mode

Table 12
Timing Characteristics of the IOM®-2 Interface TE Mode

Parameter	Symbol	Limit Values			Unit	Condition
		min.	typ.	max.		
Frame sync delay	t_{FSD}	65		195	ns	C_L = 150 pF
Bit clock delay	t_{BCD}	65		195	ns	C_L = 150 pF
Data delay	t_{DD}			100	ns	C_L = 150 pF
Data setup	t_{DS}	20			ns	
Data hold	t_{DH}	50			ns	
Data clock high	t_{WH}	175	325	475	ns	osc $\pm$ 100 ppm
Data clock low	t_{WL}	300	325	350	ns	osc $\pm$ 100 ppm
Data clock period	t_P	520	651	782	ns	osc $\pm$ 100 ppm

Timing Characteristics IOM®-2 Interface in NT / LT-S and LT-T Mode

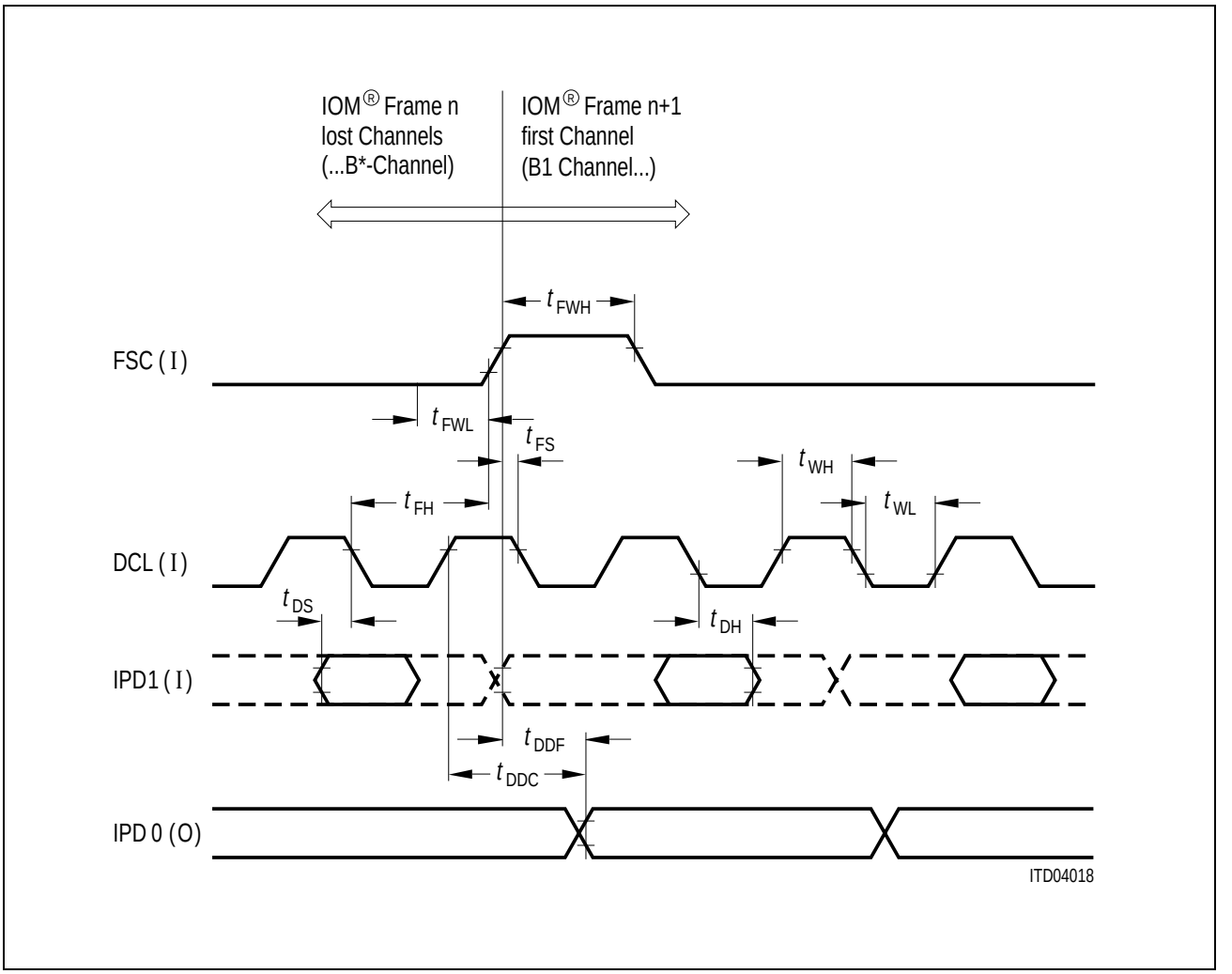


Figure 50
Timing of the IOM®-2 Interface in NT / LT-S and LT-T Mode

Table 13
Timing Characteristics of the IOM®-2 Interface NT / LT-S and LT-T Mode

Parameter	Symbol	Limit Values			Unit	Condition
		min.	typ.	max.		
Data clock high	t_{WH}	90			ns	
Data clock low	t_{WL}	90			ns	
Frame sync hold	t_{FH}	30			ns	
Frame sync setup	t_{FS}	70			ns	
Frame sync high [1)]	t_{FWH}	130			ns	
Frame sync low	t_{FWL}	t_{DCL}				
Data delay to clock	t_{DDC}			100	ns	
Data delay to frame	t_{DDF}			150	ns	
Data setup	t_{DS}	20			ns	
Data hold	t_{DH}	50			ns	

Note:
1) This is in accordance with the IOM-2 specification. For correct functional operation the high period must be 1 * DCL for multiframe markers and at least 2 DCL periods for non-multiframe markers.

4.1.1.2 Timing Characteristics CEB (NT / LT-S)

The form and the AC characteristics of the CEB input/output (pin X3 in NT and LT-S mode) are given in the following figures for the case of two S/T-interfaces having a minimum loop delay and a maximum loop delay respectively.

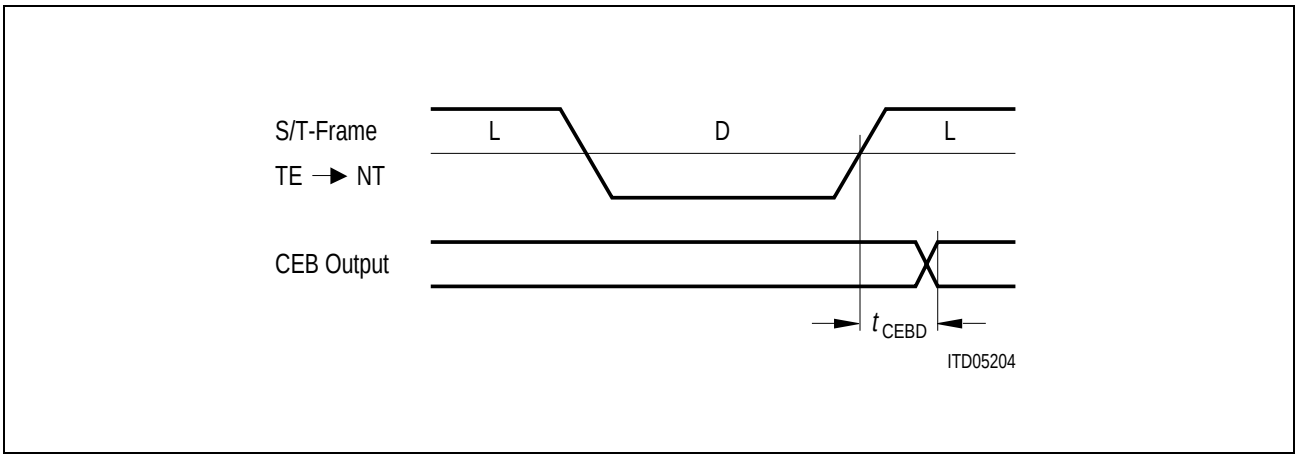


Figure 51
Timing of the CEB Output

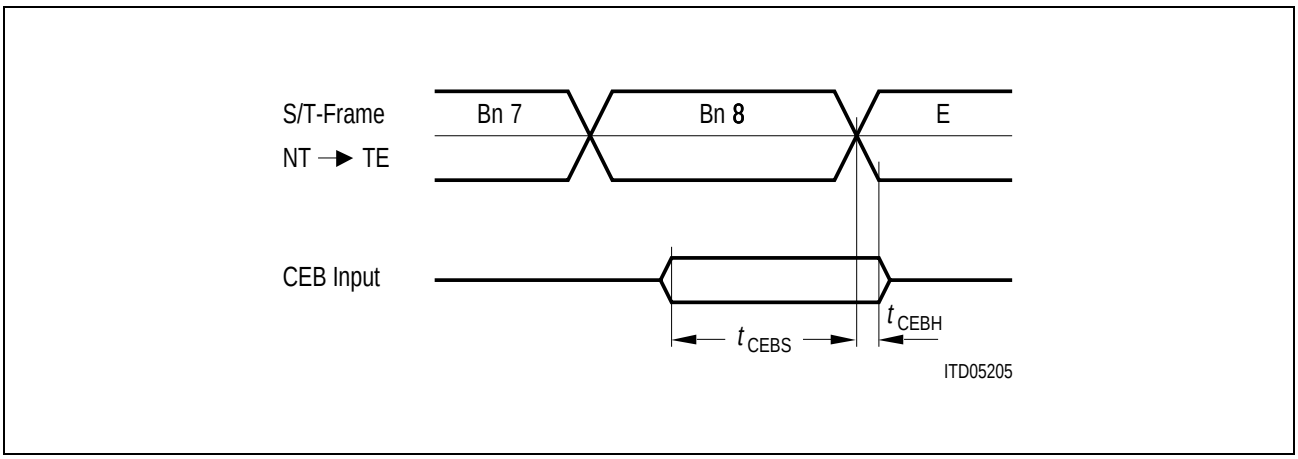


Figure 52
Timing of the CEB Input

Table 14
Timing Characteristics of the CEB Input / Output

Parameter	Symbol	Limit Values			Unit	Condition
		min.	typ.	max.		
CEB delay	t_{CEBD}	3		5	µs	C_L = 100 pF
CEB setup	t_{CEBS}	5			µs	
CEB hold	t_{CEBH}	0			µs	

The influence of more SBCXs connected to the CEB line is illustrated in the following figure. Two stations one with minimal frame delay (station A), the second with maximum frame delay (station B) determine the echo bit to be sent downstream by evaluating the common echo bit (CEB) line. **Figure 53** indicates at what point the CEB value is updated (after reception of D bit on S/T) and when the CEB line is sampled to determine the value of the transmitted echo bit.

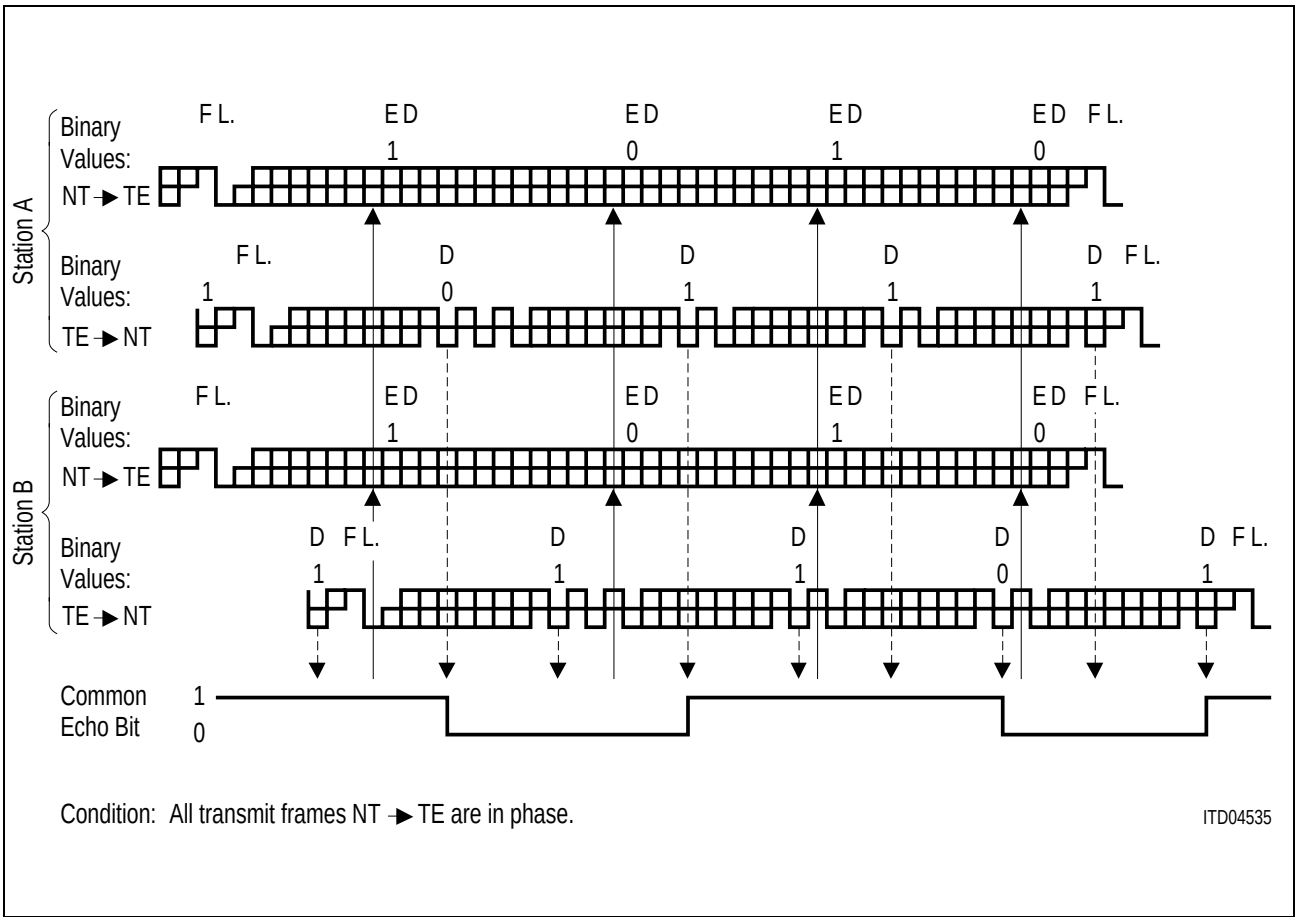


Figure 53
Functional Timing of the CEB

4.1.1.3 Command/Indicate Channel

Structure

4 bit wide, located at bit positions 27-30 in each time-slot.

Verification

Double last-look criterion. A new command or indication will be recognized as valid after it has been detected in two successive IOM frames.

Codes

Both commands and indications depend on the SBCX mode and the data direction. **Table 15** presents all defined C/I codes. A command needs to be applied continuously until the desired action has been initiated. Indications are strictly state orientated. Refer to the state diagrams in **section 4.3** for commands and indications applicable in various states. C/I commands issued by the control device in IOM-1 mode (512 kHz) will be interpreted correctly by the SBCX. Indications sent by the PEB 2081 in 512-kHz modes will also be recognized correctly by a control device operating in IOM-1 mode.

Table 15
C/I Codes

Code	LT-S		NT		TE/LT-T	
	IN	**OUT**	**IN**	**OUT**	**IN**	**OUT**
0 0 0 0	DR	TIM	DR	TIM	TIM	DR
0 0 0 1	RES	–	RES	–	RES	RES
0 0 1 0	TM1	–	TM1	–	TM1	TM1
0 0 1 1	TM2	–	TM2	–	TM2	TM2 SLIP [1]
0 1 0 0	–	RSY	RSY	RSY	–	RSY
0 1 0 1	–	MAIC	–	MAIC	–	MAIC
0 1 1 0	–	–	–	–	–	–
0 1 1 1	–	–	–	–	–	PU
1 0 0 0	AR	AR	AR	AR	AR8	AR
1 0 0 1	–	–	–	–	AR10	–
1 0 1 0	ARL	–	ARL	–	ARL	ARL
1 0 1 1	–	CVR	–	CVR	–	CVR
1 1 0 0	–	AI	AI	AI	–	AI8
1 1 0 1	–	–	–	–	–	AI10
1 1 1 0	–	–	AIL	–	–	AIL
1 1 1 1	DC	DI	DC	DI	DI	DC

1) In LT-T mode only

AI	Activation Indication
AI8	Activation Indication with high priority
AI10	Activation Indication with low priority
AIL	Activation Indication Loop
AR	Activation Request
AR8	Activation Request with high priority
AR10	Activation Request with low priority
ARL	Activation Request Loop
CVR	Code Violation Received
DC	Deactivation Confirmation
DI	Deactivation Indication
DR	Deactivation Request
MAIC	MAI Change
PU	Power-Up
RES	Reset
RSY	Resynchronizing
SLIP	IOM Frame Slip
TIM	Timer
TIM1	Test Mode 1 (2-kHz signal)
TM2	Test Mode 2 (96-kHz signal)

4.1.1.4 Monitor Channel

Modes

Automode and non-auto mode are available. These affect MON-1 and MON-2 messages only and will be described in the sections dealing with these monitor categories.

Structure

The structure of the monitor channel is 8 bit wide, located at bit position 17-24 in every time slot. Monitor messages sent to the SBCX are 1 or 2 bytes long, monitor messages returned by the SBCX are 0, 1, 2, or 5 bytes long depending on the command. Transmission of multiple monitor bytes is specified by IOM-2 (see next “Handshake Procedure” for details). For handshake control in multiple byte transfers, bit 31, monitor read “MR”, and bit 32 monitor transmit “MX”, of every time slot are used.

Verification

A double last-look criterion is implemented for both bytes of the monitor message.

Codes

3 categories of monitor messages are supported by the SBCX V3.4:

- MON-1 S_1/Q channel
- MON-2 S_2 channel
- MON-8 Register access

The order of listing corresponds to the priority attributed to each category. MON-1 messages will be transmitted first, MON-8 messages last in case several messages are initiated simultaneously.

4.1.1.4.1 Handshake Procedure

The monitor channel is full duplex and operates on a pseudo-asynchronous basis, i.e. while data transfer on the bus takes place synchronized to frame synchronization, the flow of monitor data is controlled by the MR and MX bits. Monitor data will be transmitted repeatedly until its reception is acknowledged.

Figure 55 illustrates a monitor transfer at maximum speed. The transmission of a 2-byte monitor command followed by a 2-byte SBCX response requires a minimum of 12 IOM-2 frames. In case the controller is able to confirm the receipt of first SBCX response byte in the frame immediately following the MX transition on DOUT from HIGH to LOW (i.e. in frame No. 6), 1 IOM frame may be saved.

Note:

Transmission and reception of monitor messages can be performed simultaneously by the SBCX. This feature is used by the SBCX to send back the response before the transmission from the controller is completed (SBCX does not wait for EOM from controller).

M1/2: Monitor message 1. and 2. byte

R1/2: Monitor response 1. and 2. byte

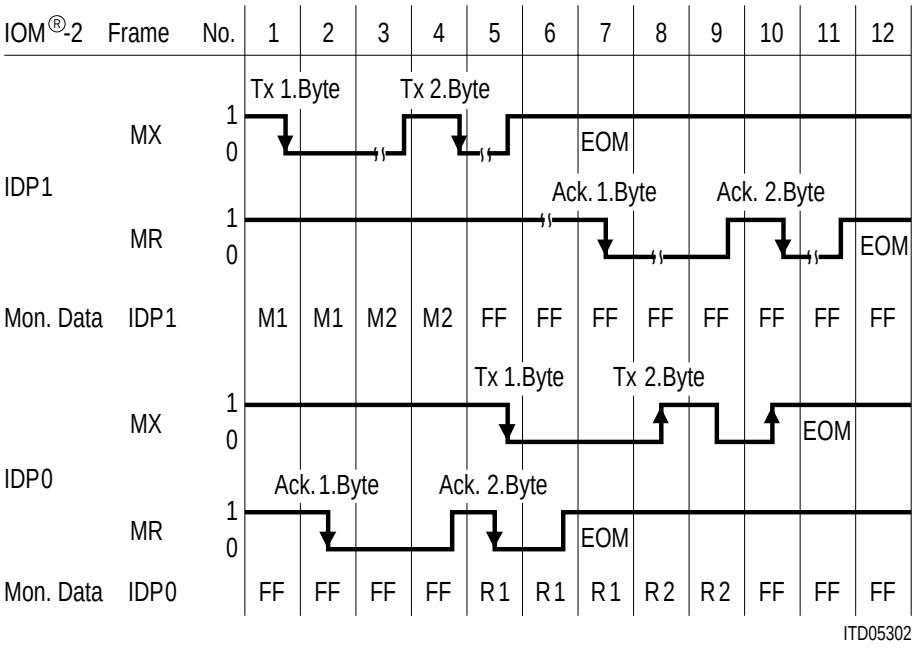


Figure 54
Handshake Protocol with a 2-Byte Monitor Message/Response

Idle State

After the bits MR and MX have been held inactive (i.e. HIGH) for two or more successive IOM frames, the channel is considered idle in this direction.

Standard Transmission Procedure

1. The first byte of monitor data is placed by the external controller (e.g. ICC, EPIC) on the IDP1 line of the SBCX and MX is activated (LOW; frame No 1).
2. The SBCX reads the data of the monitor channel and acknowledges by setting the MR bit of IDP0 active if the transmitted bytes are identical in two received frames (frame No. 2 because the PEB 2081 reads and compares data already while the MX bit is not activated).
3. The second byte of monitor data is placed by the controller on IDP1 and the MX bit is set inactive for one single IOM frame. This is performed at a time convenient to the controller.
4. The SBCX reads the new data byte in the monitor channel after the rising edge of MX has been detected. In the frame immediately following the MX transition active-to-inactive, the MR bit of IDP0 is set inactive. The MR transition inactive-to-active exactly one IOM frame later is regarded as acknowledgment by the external controller (frame No. 4-5).
   The response of the SBCX will always be sent immediately after the 2. byte has been received and acknowledged.
5. After both monitor data bytes have been transferred to the SBCX, the controller transmits “End of Message” (EOM) by setting the MX bit inactive for two or more IOM frames (frame No. 5-6).
6. In the frame following the transition of the MX bit from active to inactive, the SBCX sets the MR bit inactive (as was the case in step 4). As it detects EOM, it keeps the MR bit inactive (frame No. 6). The transmission of the monitor command by the controller is complete.
7. If the SBCX is requested to return an answer it will commence with the response as soon as the second controller byte was acknowledged (i.e. response starts in frame 5).
   The procedure for the response is similar to that described in points 1-6 except for the transmission direction. It is assumed that the controller does not latch monitor data. For this reason one additional frame will be required for acknowledgment.
   Transmission of the 2. monitor byte will be started by the SBCX in the frame immediately following the acknowledgment of the first byte. The PEB 2081 does not delay the monitor transfer.

Error Treatment and Transmission Abortion

In case the SBCX does not detect identical monitor messages in two successive frames, transmission is not aborted. Instead the SBCX will wait until two identical bytes are received in succession.

Transmission is aborted only if errors in the MR/MX handshake protocol occur. An abort is indicated by setting the MR bit inactive for two or more IOM-2 frames. The controller must react with EOM. This situation is illustrated in the following figure.

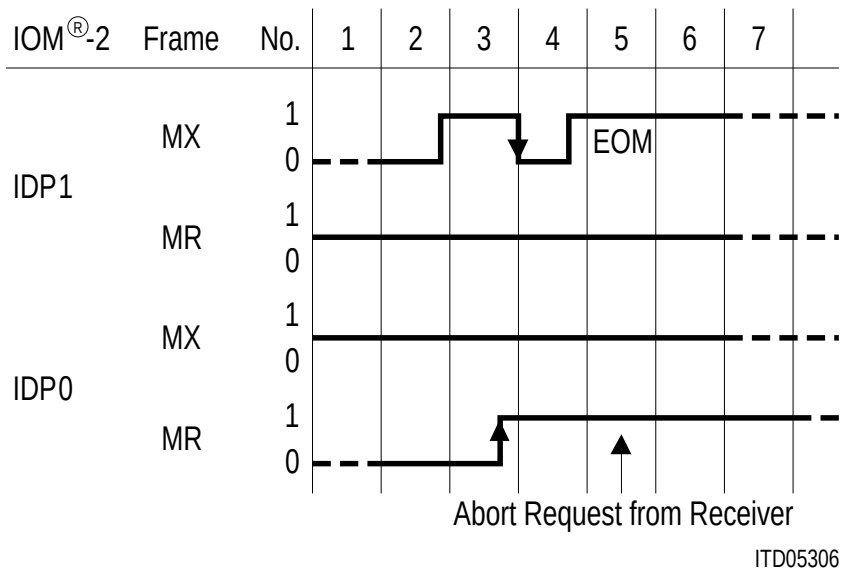


Figure 55
Abortion of Monitor Channel Transmission

4.1.1.4.2 Monitor Procedure Timeout (TOD)

The PEB 2081 V3.4 can operate with or without the “Monitor Timeout Procedure”. The TOD bit in the SM/CI (Timeout Disable) controls the timeout function. TOD = ZERO enables the function, TOD = ONE disables it.

With the timeout procedure enabled, the SBCX checks the monitor status once per multi-frame. This check is performed at the same time the 20th (i.e. last) S-frame is transmitted within the S-interface multi-frame structure.

In case the monitor is active the current status of the monitor channel is saved. This condition will be compared with the status at the next check (i.e. 5 ms later). If the condition of the monitor channel has not changed within this period the SBCX assumes a lock-up situation.

The SBCX will resolve this lock-up situation by transmitting on IDP0 a EOM (End of Message) command (MX bit set to ONE for 2 IOM frames). After the transmission of EOM the SBCX will retransmit the previous monitor channel data. No monitor channel data will therefore be lost.

4.1.1.4.3 MON-1, MON-2 Commands (S/Q Channel Access)

Function: MON-1 and MON-2 commands provide access to the SBCX internal S/Q registers. MON1 controls the S_1 and Q channel, MON-2 controls the S_2 channel on the S-interface. In order to synchronize onto multiframing pulses (TE, LT-T modes) and issue monitor-messages (NT, LT-S modes) the MFD (Multi-frame disable) bit in the configuration register must be set to ZERO.
MON-1 and MON-2 commands may be passed at any instant provided the S-interface is activated. They are always one byte long.

Direction S $\rightarrow$ IOM:
In the direction S-interface to IOM interface a 1 byte buffer is implemented. Every time a S/Q message has been received on the S-interface which needs to be forwarded to the IOM interface this message will be saved in a latch. This latch allows retransmission of the old S/Q data on IOM in case the message has not been read by the controller before a monitor timeout occurred.
While the latched data has not been read correctly from the monitor channel the S/Q receiver will not reload the latch. Thus the IOM controller must read out the S/Q messages from IOM once per 5 ms (multi-frame period). If this is not guaranteed S/Q channel data may be lost.

Direction IOM $\rightarrow$ S:
No buffering is available in the direction IOM-interface to S-interface.
The SBCX will acknowledge a S/Q command correctly and transfer the command into an internal S/Q transmit buffer if this command is received during frame numbers 1-17. Once a command has been transferred into the internal transmit register new S/Q commands received during frames 1-17 will not be accepted by the SBCX (i.e. no acknowledgment issued with MR bit). During frame numbers 18-20 however the monitor channel data is transferred directly into the transmit register. During this period previously accepted S/Q data could therefore be overwritten. To avoid this situation the controller must be programmed to send no more than one S/Q command per multi-frame (5 ms).

Note that for both S_1 and S_2 channel a separate transmit register is reserved. The above stated restriction thus applies only to S/Q commands referring to the same channel.
Transmission of the stored data will commence with the new multi-frame.

Priority: MON-1 commands have the highest priority, MON-2 command are treated with second priority.

Modes: Non-auto mode and transparent mode are available in all operational modes. The SQM (SQ Mode) bit selects transparent mode (ONE) and non-auto mode (ZERO).

Non-Auto Mode

In non-auto mode only MON-1 functions to access the S_1 and Q channel are available. MON-2 messages (for S_2 channel access) are ignored.

In non-auto mode monitor messages are only released after new data has been received. In this mode traffic on the IOM monitor channel is reduced. The controller only receives changes in the S_1 or Q channel reducing its processing demands as well.

Transparent Mode

In transparent mode all S/Q channels are available to the user. MON-1 commands/messages service the S_1 and Q channel, MON-2 commands/messages related exclusively to the S_2 channel. In this mode the data received on S_1, S_2 or Q will be forwarded directly to the IOM-interface. No comparison with previously sent data is performed so that one MON-1 and one MON-2 monitor message will be issued every 5 ms (once per multi-frame) in TE or LT-T modes. In NT and LT-S modes one MON-1 message will indicate every multi-frame the current Q channel data received.

Codes:

MON-1 Command/Message (S_1/Q channel)

1 Byte							
0	0	0	1	S_1/Q	S_1/Q	S_1/Q	S_1/Q
MON-1				Data			

S1: Data in S_1 channel (NT, LT-S input; TE, LT-T output)

Q: Data in Q channel (TE, LT-T input; NT, LT-S output)

MON-2 Command/Message (S_2 channel)

1 Byte							
0	0	1	0	S_2	S_2	S_2	S_2
MON-2				Data			

S_2: Data in S_2 channel (NT, LT-S input; TE, LT-T output)

Currently neither S_1, S_2 nor Q channel commands have been standardized.

4.1.1.4.4 MON-8 Commands (Register Access)

Function: MON-8 commands provide access to the SBCX internal registers. MON-8 commands allow to configure the SBCX. With the exception of the identification register (read only) all registers have read/write capability. In case a write operation is selected the command is two bytes long. For a read operation the two byte long read request command will be followed by a two byte long response message. Only exception is a read request from the µP MAI interface. Here a single 5 byte response monitor message is optional.

Buffering: After **hard- or software** reset, the register values specified in "Initial State" overwrite all customer settings.
Modifications in the internal registers will be latched until they are overwritten with a new MON-8 command.

Modes: MON-8 commands are independent of the operational SBCX mode or other mode selections. Depending on the operational mode the meaning of single register bits may change.

Codes

Write to Register Structure

1. Byte								2. Byte							
1	0	0	0	r	r	r	r	D7	D6	D5	D4	D3	D2	D1	D0
MON-8				Reg. Address				Register Data Write							

r: Register Address – 1 … 5 (Configuration Reg. – MAI Pin Reg.)

D0-D7: Write Data – Depending on Register

Read Register Request Structure

1. Byte								2. Byte							
1	0	0	0	0	0	0	0	0	0	0	0	r	r	r	r
MON-8				–				–				Reg. Address			

r: Register Address – 0 … 5 (Identification Reg. – MAI Pin Reg.)

Read Response Structure

1. Byte								2. Byte							
1	0	0	0	r	r	r	r	D7	D6	D5	D4	D3	D2	D1	D0
MON-8				Reg. Adr.				Register Data Read							

r: Register Address Confirmation – 0 … 5 (Identification Reg. – MAI Pin Reg.)

D7 … D0: Receive Data – Depending on Register

MON-8 Identification Register – (Read, Address: 0_H)

Format:	0	1	0	0	0	0	1	0

Initial Value: 42_H

Older SBCX Versions identify themself with the following IDs:

Versions: A1 to A3 ID = 40_H

Versions: B1 and 2.2 ID = 41_H

MON-8 Configuration Register – (Read/Write, Address: 1_H)

Format:	MFD	MAIM	FSMM	LP	SQM	RCVE	C/W/P	MODE

Initial Value: 00_H

Table 16

Bit-name	Description
MODE	Pin MODE = V_{DD} (LT-S, LT-T): 0: LT-S mode selected 1: LT-T mode selected
C/W/P	LT-S and NT mode: Configuration 0: point-to-point or extended passive bus configuration (adaptive timing recovery). In NT mode the pin X0 (= BUS) must be low. 1: short passive bus configuration (fixed timing recovery) in LT-T mode: Wander detection (warning in C/I, data may be lost!) 0: “SLIP” after 50 µs wander 1: “SLIP” after 25 µs wander in TE mode: Power converter clock frequency supplied at pin 40 0: 32 kHz 1: 16 kHz
SQM	SQ channel handling mode selection 0: non automode only S_1 and Q channels 1: transparent mode S_1, S_2 and Q channels
RCVE	0: normal operation 1: Far-end-code-violation (FECV) function according to ANSI T1.605 implemented. After each multiframe the receipt of at least one illegal code violation is indicated by the occurance of six times the C/I code 1011(CVR).
LP	NT/LT-S mode: 0: transparent analog loop 1: non-transparent analog loop TE / LT-T mode: 0: non-transparent analog loop 1: external transparent loop

Table 16 (cont'd)

FSMM	NT/LT-S mode: 0: normal operation 1: Finite state machine interchanged (LT-S ↔ N)
MAIM	MAI pins mode: 0: I/O-specific or standard I/O MAI interface 1: µP interface mode for MAI interface
MFD	Multi-frame disable (write): 0: All multi-frame functions active. In NT mode the pin MAI1 (= MFD) must be low. 1: Multi-frame generation (NT, LT-S) or synchronization (TE, LT-T) prohibited. No SQ monitor messages released. Multi-frame detected (read): 0: No multi-frame synchronization achieved. 1: Multi-frame synchronization achieved.

MON-8 Loop-Back Register – (Read/Write, Address: 2_H)

Format:	AST	SB1	SB2	SC	IB1	IB2	1	IB12

Initial value: 02_H

Table 17

Bit-name	Description
AST	ASynchronous Timing NT and LT-S mode; only NT state machine 0: LT-S: command TIM in C/I NT: asynchronous wake up 1: LT-S: asynchronous wake up (useful for the Intelligent NT) NT: command TIM in C/I
SB1	Loop-back B1 channel at S/T-interface in LT-S/NT-mode
SB2	Loop-back B2 channel at S/T-interface in LT-S/NT-mode
SC	Loop-back complete (2B+D) at S/T-interface in LT-S/NT-mode
IB1	Loop-back B1 channel at IOM-2 interface
IB2	Loop-back B2 channel at IOM-2 interface
IB12	Loop-back B1 into B2 channel and vice versa at IOM-2 interface. Additionally IB1 and/or IB2 must be set.

MON-8 IOM-2 Channel Register - (Read/Write, Address: 3_H)

Format:	B1L	B1D	B2L	B2D	DL	DH	CIL	CIH

Initial value: 00_H

Table 18

Bit-name	Description
B1L	B1 channel location 0: normal [1)] 1: B1 channel in IOM-2 channel 0
B2L	B2 channel location 0: normal [1)] 1: B2 channel in IOM-2 channel 0
DL	D-channel location 0: normal [1)] 1: D-channel in IOM-2 channel 0
CIL	CI channel location 0: normal [1)] 1: in IOM-2 channel 0
B1D	B1 channel direction 0: normal (IDP0 is data output, IDP1 is data input) 1: IDP0 and IDP1 interchanged for B1 channel
B2D	B2 channel direction 0: normal (IDP0 is data output, IDP1 is data input) 1: IDP0 and IDP1 interchanged for B2 channel
DH	D-channel handling 0: LT-S, LT-T and NT mode: transparent TE mode: collision detection according to ITU I.430 (BAC and A/B bit evaluation) 1: NT and LT-S mode: D-channel access control TE mode: transparent D-channel LT-T mode: D-channel collision resolution according to ITU I.430
CIH	CI channel handling 0: normal C/I access in the pin strapped IOM-2 channel 1: disabled, access to C/I is only possible via the SM/CI register

Notes:
1) In LT-S and LT-T mode: pin strapped IOM-2 channel
In NT and TE mode: IOM-2 channel 0

MON-8 SM/CI Register – (Read/Write, Address: 4_H)

Format:	CI3	CI2	CI1	CI0	TOD	SGE	0	MIO

Initial value: CI, 0_H

Table 19

Bit-name	Description
CI (3:0)	CI channel When CIH-bit is set to one the commands are input in the monitor channel CI (3:0) The indication can always be read via monitor channel CI (3:0)
TOD	Time-Out Disable 0: monitor timeout (minimum 5 ms) enabled 1: monitor timeout disabled
SGE	Stop / Go Enable 0: normal 1: In TE mode pin MAI5 outputs S/G signal
MIO	Maintenance Input Output (MAIM = 0) 0: I/O-specific functions on MAI interface 1: Standard I/O function on MAI interface

MON-8 MAI Pin Register - (Read/Write, Address: 5_H)

Format:	MPR7	MPR6	MPR5	MPR4	MPR3	MPR2	MPR1	MPR0

Initial value: 00_H

Bit-name	Description
MPR (7:0)	access to MAI(7:0) pins if MAI interface is set to standard I/O or I/O specific function mode.

In case the µP interface was selected for the MAI interface mode (MAIM = 1) the MAI pin register are defined as follows (only “write to register” operation will be accepted).

Format:	$\overline{WR}$	$\overline{RD}$	A1	A0	$\overline{INT}$	D2	D1	D0

(write only)

Table 20

Bit-name	Description
D0…D2 MAI0:2	Data pin (input/output)
$\overline{INT}$ (MAI3)	Interrupt (input), Read request control: 0: Single Address read operation 1: Complete address (0…3) read operation.
A0 … A1 (MAI4:5)	Address pins (output)
$\overline{RD}$ (MAI6)	Read signal (output) 0: Read operation 1: Write operation (if $\overline{WR}$ = 0)
$\overline{WR}$ (MAI7)	Write Signal (output). 0: Write operation 1: Read operation (if $\overline{RD}$ = 0)

4.1.2 S/T-Interface

Transmission over the S/T-interface is performed at a rate of 192 kbit/s. Pseudo-ternary coding with 100 % pulse width is used (**see following section**). 144 kbit/s are used for user data (B1+B2+D), 48 kbit/s are used for framing and maintenance information. The SBCX uses two symmetrical, differential outputs (SX1, SX2) and two symmetrical, differential inputs (SR1, SR2). These signals are coupled via external circuitry and two transformers onto the 4 wire S-interface. The nominal pulse amplitude on the S-interface is 750 mV (zero-peak).

4.1.2.1 S/T-Interface Coding

The following figure illustrates the code used. A binary ONE is represented by no line signal. Binary ZEROs are coded with alternating positive and negative pulses with a single exception: the first binary ZERO following the framing balance bit is of the same polarity as the framing-balancing bit (required code violation).

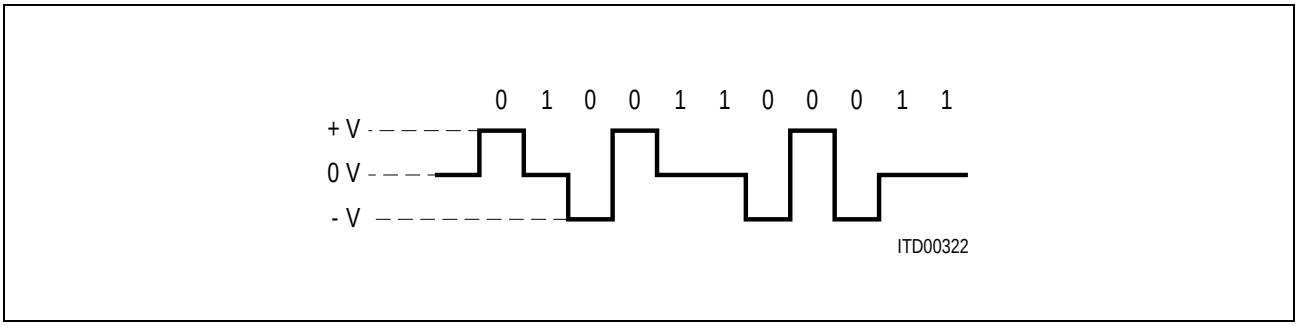


Figure 56
S/T -Interface Line Code (without code violation)

A standard S/T frame consists of 48 bits. In the direction TE → NT the frame is transmitted with a two bit offset. For details on the framing rules please refer to ITU I.430 section 6.3. The following figure illustrates the standard frame structure for both directions (NT → TE and TE → NT) with all framing and maintenance bits.

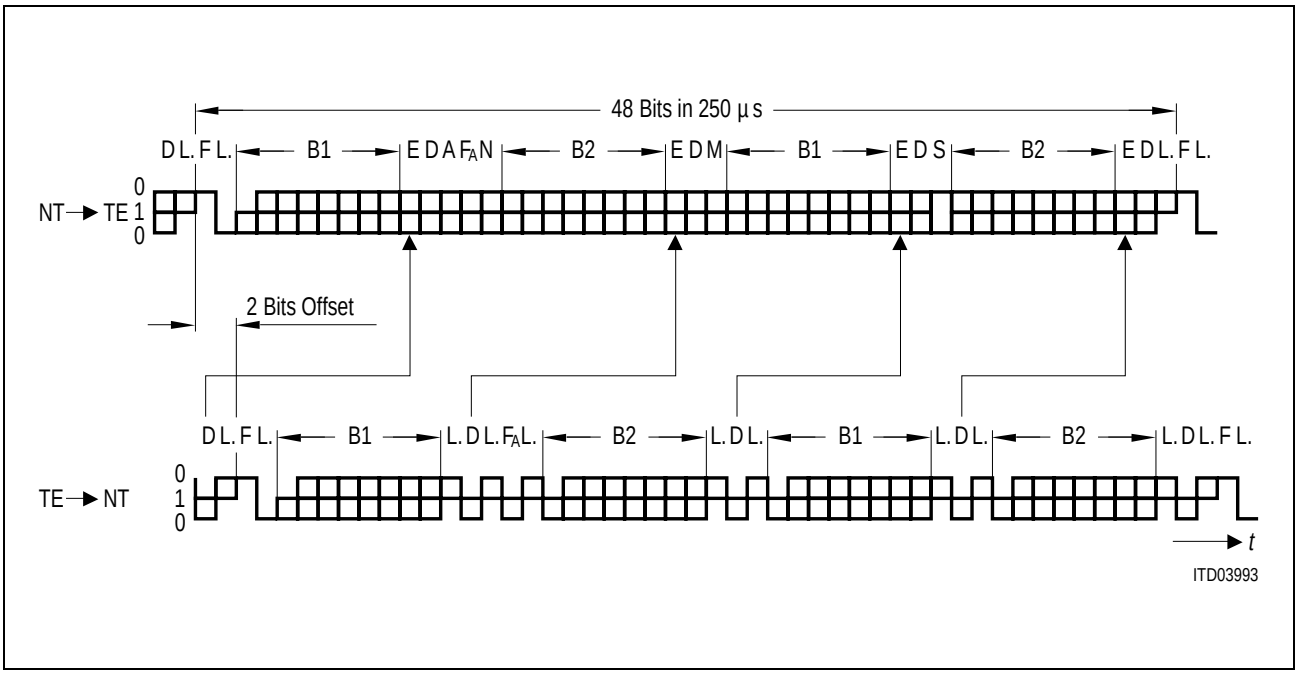


Figure 57
Frame Structure at Reference Points S and T (ITU I.430)

– F	Framing Bit	F = (0b) → identifies new frame (always positive pulse)
– L.	D.C. Balancing Bit	L. = (0b) → number of binary ZEROs sent after the last L. bit was odd
– D	D-Channel Data Bit	Signaling data specified by user
– E	D-Channel Echo Bit	E = D → no D-channel collision. ZEROs overwrite ONEs
– F_A	Auxiliary Framing Bit	See section 6.3 in ITU I.430
– N		N = $\overline{F_A}$
– B1	B1-Channel Data Bit	User data
– B2	B2-Channel Data Bit	User data
– A	Activation Bit	A = (0b) → INFO 2 transmitted A = (1b) → INFO 4 transmitted
– S	S-Channel Data Bit	S_1 or S_2 channel data
– M	Multiframing Bit	M = (1b) → Start of new multi-frame

4.1.3 S/T-Interface Multiframing

According to ITU recommendation I.430 a multi-frame provides extra layer 1 capacity in the TE-to-NT direction through the use of an extra channel between the TE and NT (Q-channel). The Q bits are defined to be the bits in the F_A bit position.

In the NT-to-TE direction the S channel bits are used for information transmission. Two S channels (S1 and S2) out of five possible S channels can be accessed by the SBCX.

The S and Q channels are accessed via the IOM-2 interfaces monitor channel.

The following table shows the S and Q bit positions within the multi-frame.

Table 21

Frame Number	NT-to-TE F_A Bit Position	NT-to-TE M Bit	NT-to-TE S Bit	TE-to-NT F_A Bit Position
1	ONE	ONE	S11	Q1
2	ZERO	ZERO	S21	ZERO
3	ZERO	ZERO	ZERO	ZERO
4	ZERO	ZERO	ZERO	ZERO
5	ZERO	ZERO	ZERO	ZERO
6	ONE	ZERO	S12	Q2
7	ZERO	ZERO	S22	ZERO
8	ZERO	ZERO	ZERO	ZERO
9	ZERO	ZERO	ZERO	ZERO
10	ZERO	ZERO	ZERO	ZERO
11	ONE	ZERO	S13	Q3
12	ZERO	ZERO	S23	ZERO
13	ZERO	ZERO	ZERO	ZERO
14	ZERO	ZERO	ZERO	ZERO
15	ZERO	ZERO	ZERO	ZERO
16	ONE	ZERO	S14	Q4
17	ZERO	ZERO	S24	ZERO
18	ZERO	ZERO	ZERO	ZERO
19	ZERO	ZERO	ZERO	ZERO
20	ZERO	ZERO	ZERO	ZERO
1	ONE	ONE	S11	Q1
2	ZERO	ZERO	S21	ZERO

In **TE** and **LT-T** mode the SBCX identifies the Q-bit position (after multi-frame synchronization has been established) by waiting for the F_A bit inversion in the received S/T-interface data stream (F_A [NT $\rightarrow$ TE] = binary ONE). After successful identification, the Q data will be inserted at the upstream (TE $\rightarrow$ NT) F_A bit position. When synchronization is not achieved or lost, it mirrors the received F_A bits.

Multi-frame synchronization is achieved after two complete multi-frames have been detected with reference to F_A/N bit and M bit positions. Multi-frame synchronization is lost after two or more bit errors in F_A/N bit and M bit positions have been detected in consequence, i.e. without a complete valid multi-frame between.

The multi-frame synchronization can be disabled by programming (MFD-bit configuration register).

4.1.4 Maintenance Auxiliary Interface (MAI)

Selection of MAI interface configuration:

Table 22

Configuration Reg. MAIM	SM/CI Reg MIO	MAI Interface Mode
0	0	I/O specific
0	1	Standard I/O
1	0	µP interface mode
1	1	not applicable

After a hard- or software reset the default setting is “I/O specific” interface.

4.1.4.1 I/O Specific Mode

Please refer to **section 3.2.3.1** in the application chapter for details on the I/O specific signals. Register access is performed as described for standard I/O mode.

4.1.4.2 Standard I/O Mode

Provides four input and four output lines. Interface access via MON-8 MAI pin register.

The MAI pins may be written by the following 2-byte sequence via the IOM-2 monitor channel:

Write message (to SBCX)		
write command (access to MAI Pin Register MPR)		data D(7:4) to be written to MAI pin (7:4)
85_H		D7 D6 D5 D4 ****

*** means don't care

The MAI pins may be read by the following 2-byte sequence via the IOM-2 monitor channel:

Read message (to SBCX)		
read command		MAI pin Register MPR
80_H		05_H
response (from SBCX)		
8 + internal address (i.e. MPR)		data
85_H		D7 D6 D5 D4 D3 D2 D1 D0

where D(7:4) are the previously written MAI (7:4) bits and D(3:0) are the MAI (3:0) inputs.

4.1.4.3 µP MAI Mode

In case the µP mode is selected (MIO, MAIM bits) the following timing applies for read and write operations.

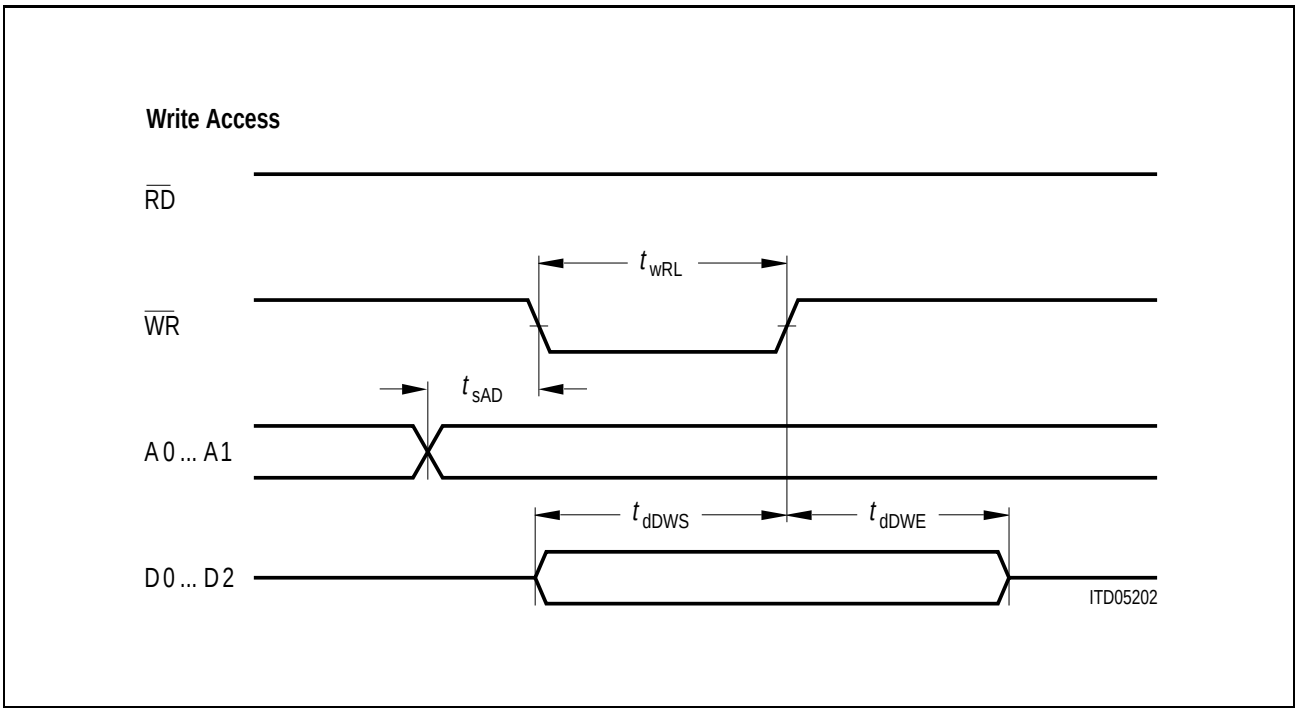


Figure 58
Dynamic Characteristics of µP Interface Write Access

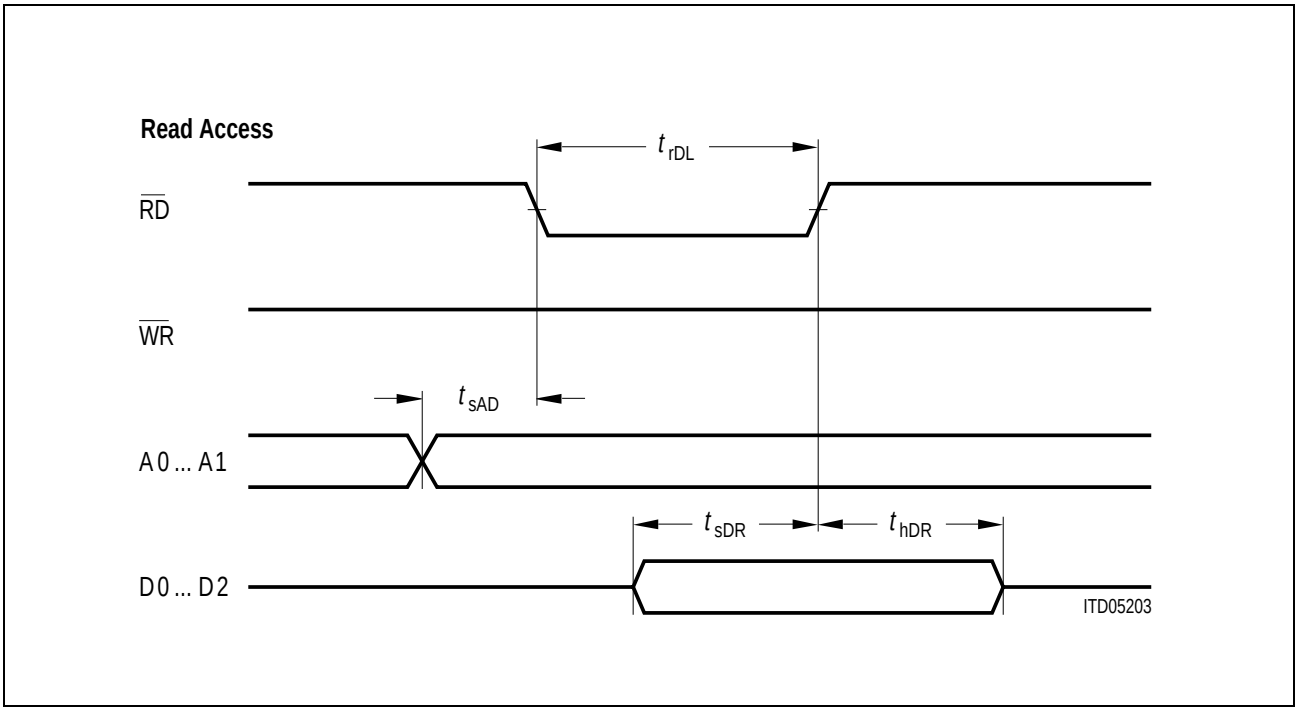


Figure 59
Dynamic Characteristics of µP Interface Read Access

Table 23
Dynamic Characteristics of Data Port

Parameter	Signal	Abbreviation	Min.	Typ.	Max.	Units
Write Width Low		t_{wRL}	2 x DCL – 200			ns
Address Delay Read/Write	A0 … 1	t_{sAD}	2 x DCL – 200		2 x DCL + 200	ns
Data Delay Write Start	D0 … 2	t_{dDWS}	– 200		+ 200	ns
Data Delay Write End		t_{dDWE}	1 x DCL – 200		1 x DCL + 200	ns
Setup Data Read		t_{sDR}	100			ns
Hold Data Read		t_{hDR}	50			ns
Read Width Low		t_{rDL}	2 x DCL – 200			ns

Interrupt

For every change at the input pin “INT”, the SBCX V 3.4 will transmit a C/I channel code (0101b), MAIC, in 4 successive IOM-2 frames. The INT pin is sampled continuously.

Monitor Message Sequences

MAI “write” message (from SBCX to e.g. IEPC)												
1	0	0	0	0	1	0	1	0	1	address	*	data

MAI “single read” message (from SBCX to e.g. IEPC)														
1	0	0	0	0	1	0	1	1	0	address	1	*	*	*
MAI “single read” response (response from e.g. IEPC to SBCX)														
1	0	0	0	0	1	0	1	1	0	address	1	data		

MAI “multiple read” message MAI (from SBCX to e.g. IEPC)														
1	0	0	0	0	1	0	1	1	0	0	0	0	*	*	*
MAI “single read” response (response from e.g. IEPC to SBCX)														
1	0	0	0	0	1	0	1	1	0	0	0	0	data		
								1	0	0	1	0	data	
								1	0	1	0	0	data	
								1	0	1	1	0	data	

*** means don’t care
data Data(2:0)
address Address(1:0)

4.2 Control Procedures

Chapter 4.2 illustrates the interactions between two SBCX stations during activation and deactivation. The behaviour of a single SBCX station is described in the state diagrams of **chapter 4.3**. With a knowledge of the state machine and the interactions involved, it is possible to predict the behaviour of the device under all conditions.

The activation and deactivation procedures implemented by the SBCX in its different operating modes were designed according to ITU I.430.

The following table explains all S/T-interface signals used in the following sections (definition in ITU I.430).

Table 24
S/T-Interface Signals

Signals from NT to TE		Signals from TE to NT	
INFO 0	No signal.	INFO 0	No signal.
		INFO 1	A continuous signal with the following pattern: Positive ZERO, negative ZERO, six ONEs.
INFO 2	Frame with all bits of B, D, and D-echo channels set to binary ZERO. Bit A set to binary ZERO. N and L bits set according to the normal coding rules.		
		INFO 3	Synchronized frames with operational data on B and D-channels.
INFO 4	Frames with operational data on B, D, and D-echo channels. Bit A set to binary ONE.		

4.2.1 Complete Activation Initiated by Exchange (LT-S)

The following figure depicts the procedure if activation has been initiated by the exchange side and the exchange SBCX is set to LT-S mode.

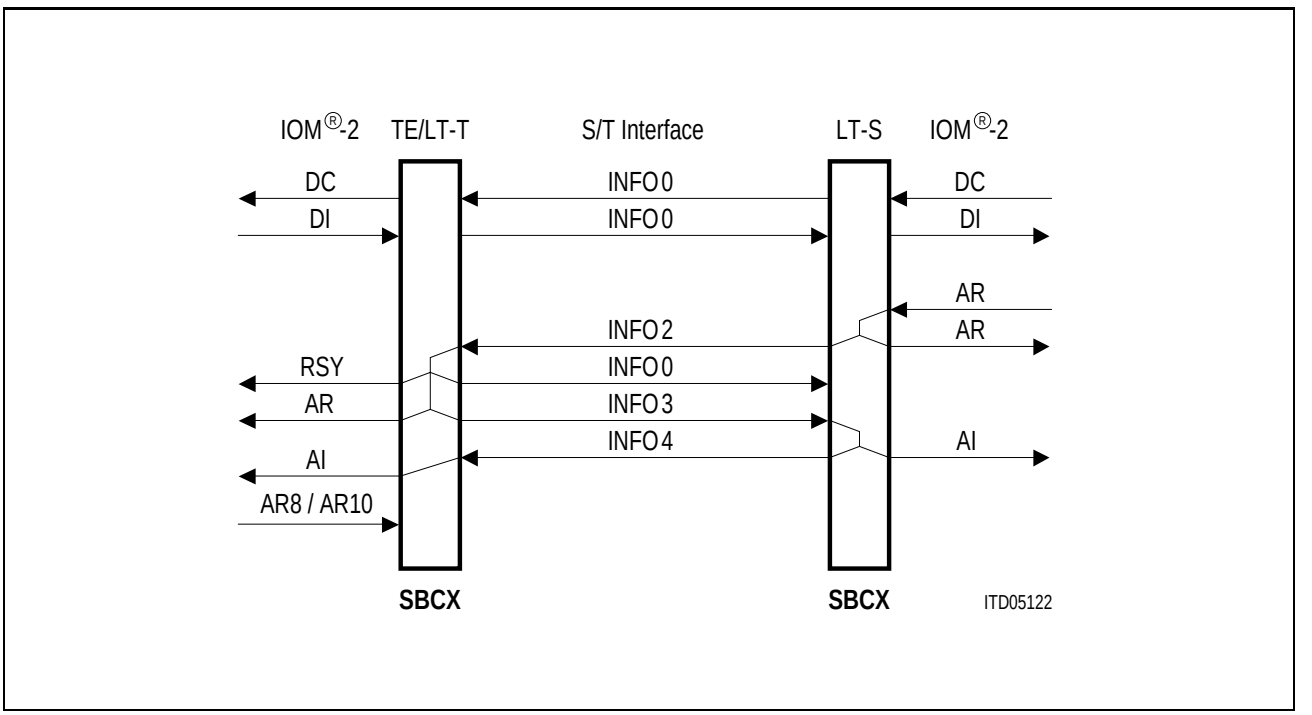


Figure 60
Complete Activation Initiated by Exchange (LT-S)

4.2.2 Complete Activation Initiated by Exchange (NT)

Figure 61 illustrates the activation procedure when the exchange starts the activation.

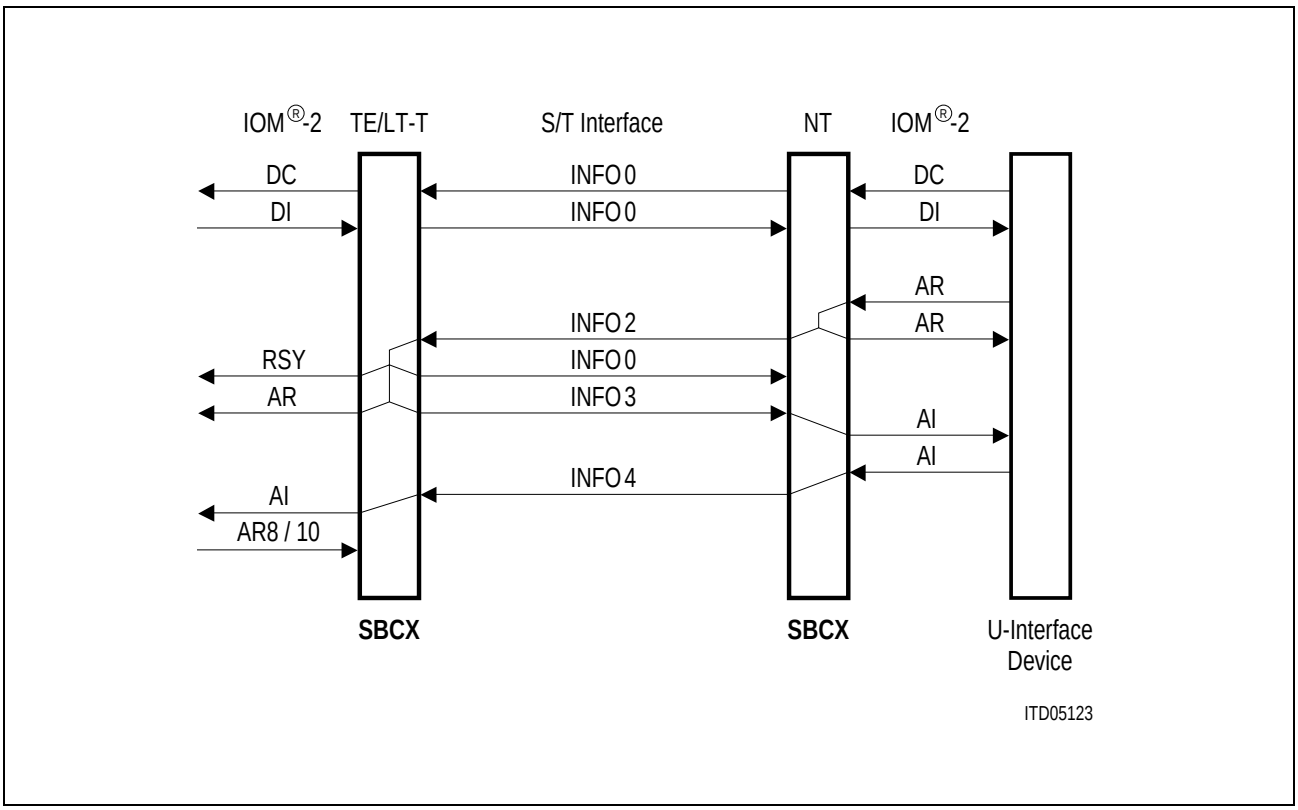


Figure 61
Complete Activation Initiated by Exchange (NT)

4.2.3 Complete Activation Initiated by Terminal

The following figure illustrates the activation process if started from the terminal side (or LT-T). This illustration only shows the part of the activation which differs from the previously described exchange initiated activation.

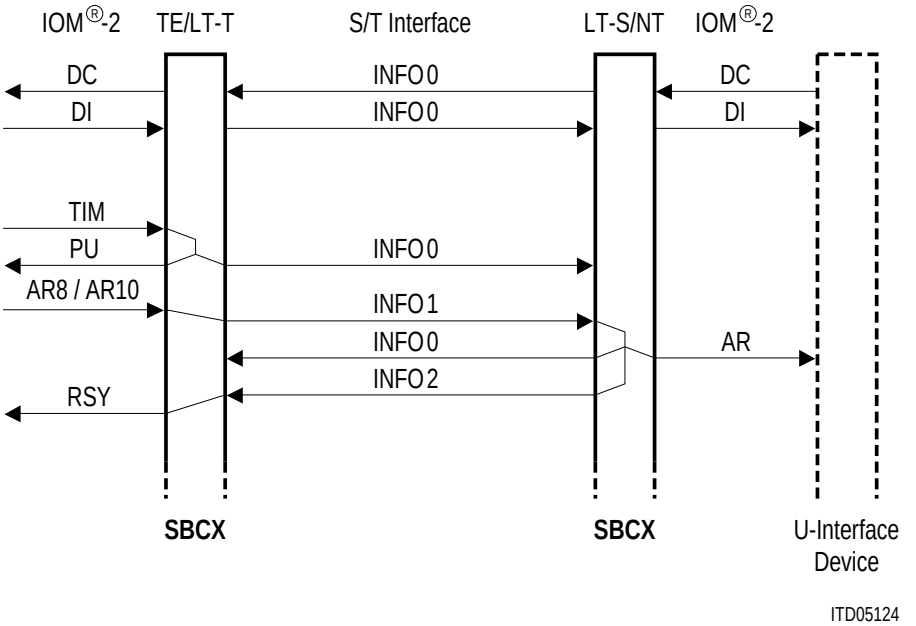


Figure 62
Complete Activation Initiated by TE

In the case where activation is requested from a terminal, the NT SBCX first requests timing on the IOM-2 interface by pulling DU (Data upstream line) to a static low level. The length of the low level is programmable (AST-bit of the Loop-Back Register). The SBCX enters the power-up state immediately after timing has been applied.

4.2.4 Complete Deactivation

A deactivation will always be initiated by the exchange side.

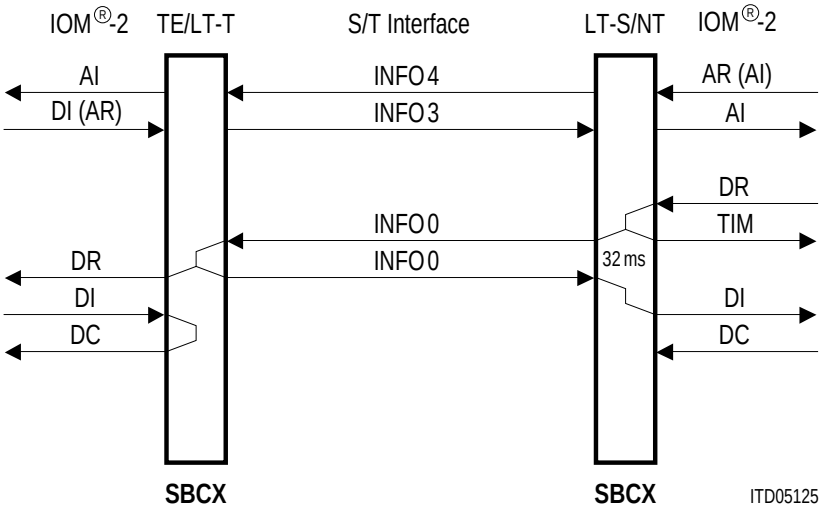


Figure 63
Deactivation Procedure

For the NT case (DCL = 512 kHz) the deactivation procedure is shown in the following figure. After detecting the code DI (Deactivation Indication) from the downstream unit SBCX, the upstream unit responds by transmitting DC (Deactivate Confirmation) during subsequent frames and stops the timing signals synchronously with the end of the last C/I channel bit of the fourth frame.

Please note, in the deactivated state the oscillator is switched off.

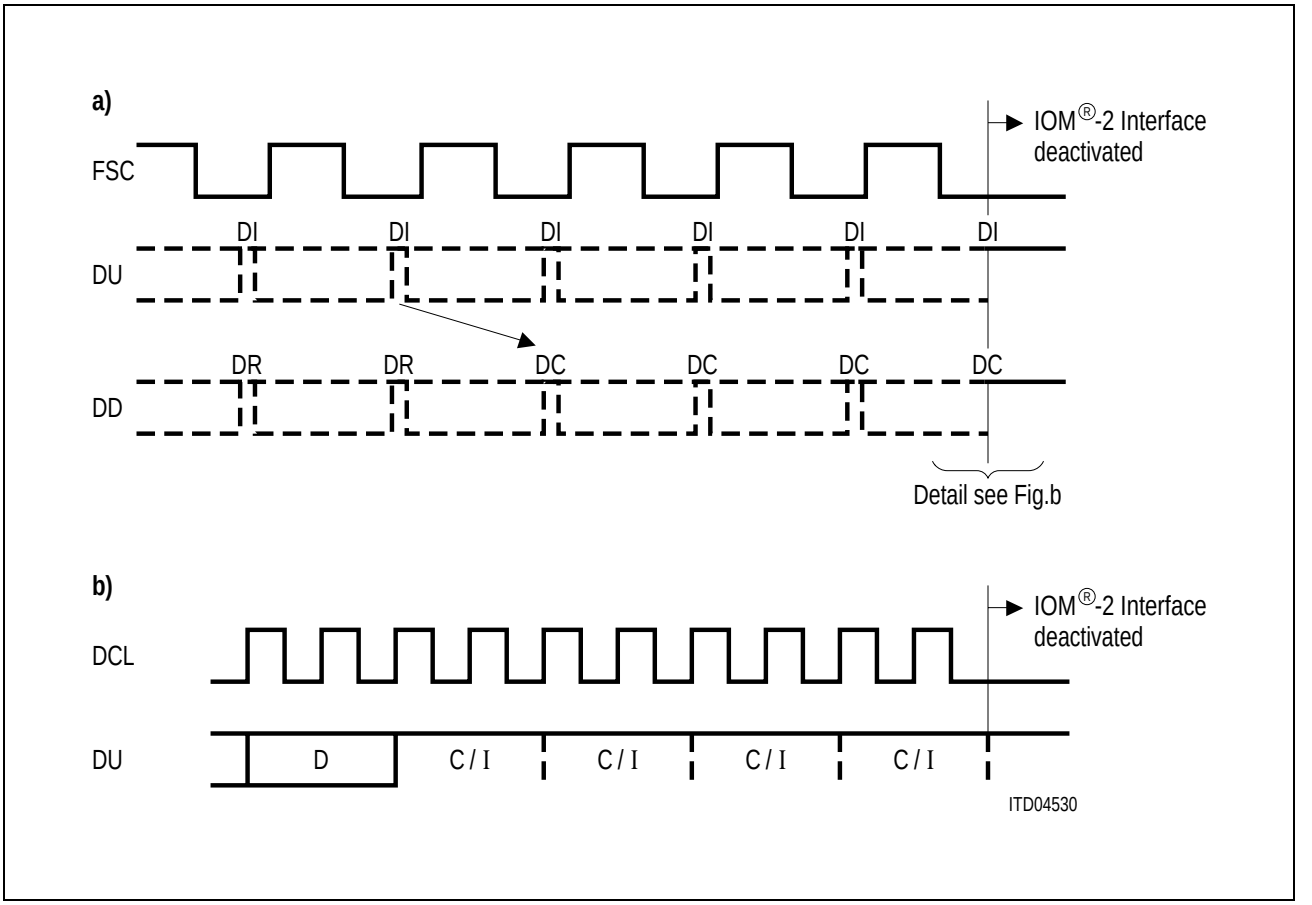


Figure 64
Deactivation of the IOM®-2 Interface in the NT (DCL = 512 kHz)

4.3 State Machine

State machines are the key to understanding the SBCX in different operational modes. They include all information relevant to the user and enable him to understand and predict the behaviour of the SBCX. The informations contained in the state diagrams are:

- state name (based on ITU I.430)
- S/T signal transmitted
- C/I code received
- C/I code transmitted
- transition criteria

It is essential to be able to interpret the state diagrams.

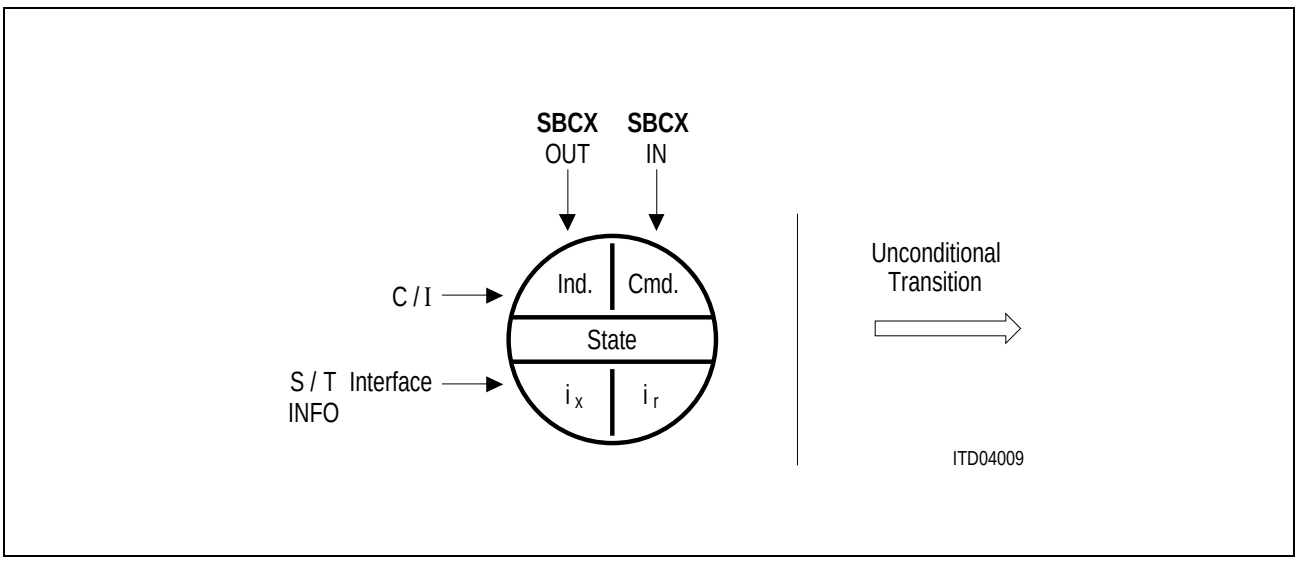


Figure 65
State Diagram Notation

The following example illustrates the use of a state diagram with an extract of the TE state diagram. The state explained is “F3 power down”.

The state may be entered by either of two methods:

- from state “test mode i” after the C/I command “DI” has been received.
- from state “F3 pending deactivation” after the C/I command “DI” been received.

The following informations are transmitted:

- INFO 0 (no signal, see **chapter 4.2**) is sent on the S/T-interface.
- C/I message “DC” is issued on the IOM-2 interface.

The state may be left by either of the following methods:

- Leave for the state “F3 power up” after synchronous or asynchronous “TIM” code has been received on IOM.
- Leave for state “F5/8 unsynchron” after any kind of signal (not INFO 0) has been recognized on the S/T-interface.
- Leave for state “F4 pending activation” in case C/I = AR8 or AR10 is received and the MAI pin CON is set to high (i.e. INFO 1 transmission not disabled).

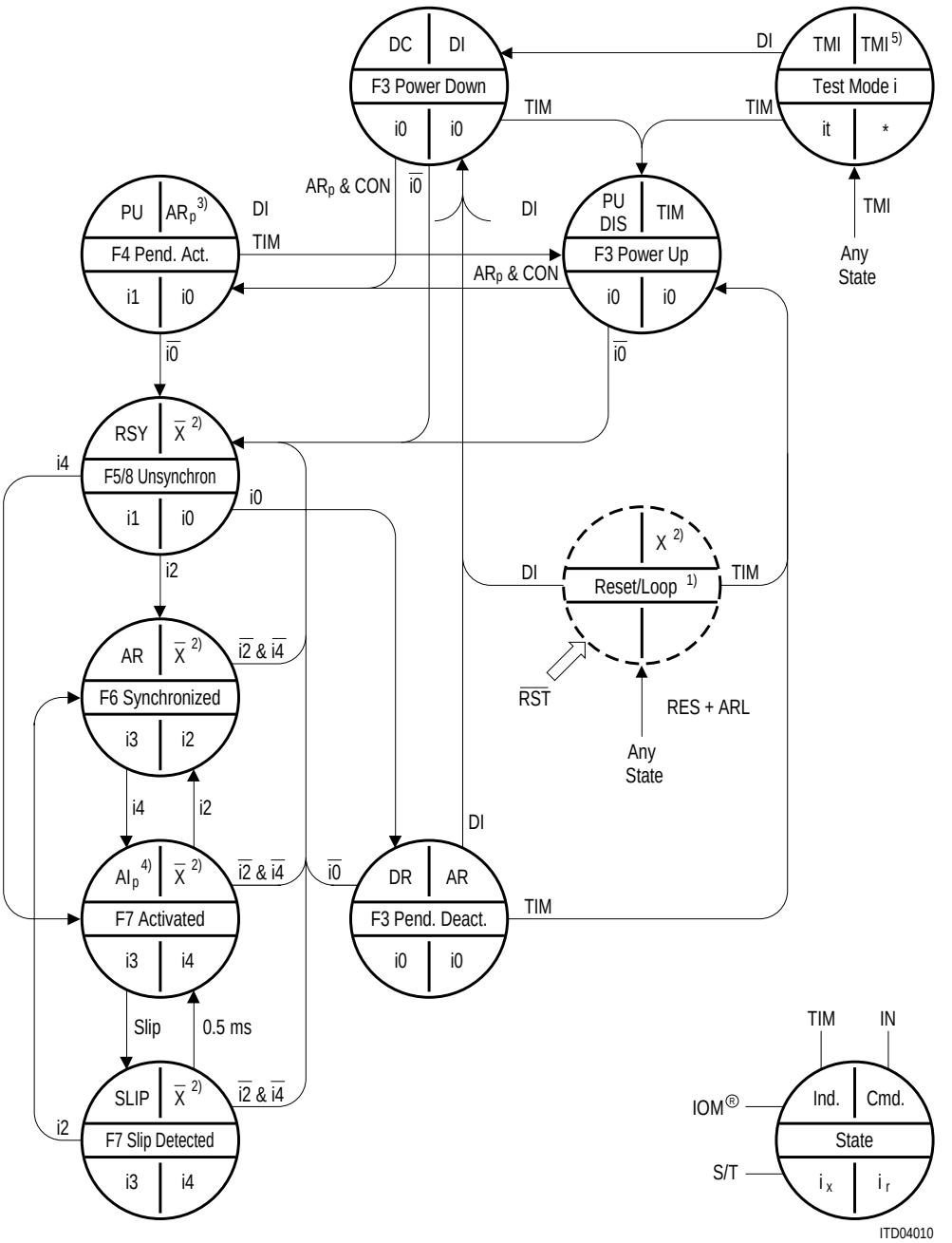
As can be seen from the last transition criteria described combinations of multiple conditions are possible as well. A “&” stands for a logical AND combination. An “or” indicates a logical OR combination.

The sections following the state diagram contain detailed information on all states and signals used. These details are mode dependent and may differ for identically named signals/states. They are therefore listed for each mode.

4.3.1 State Machine TE/LT-T Modes

Section 4.3.1 is applicable for both TE and LT-T operational modes.

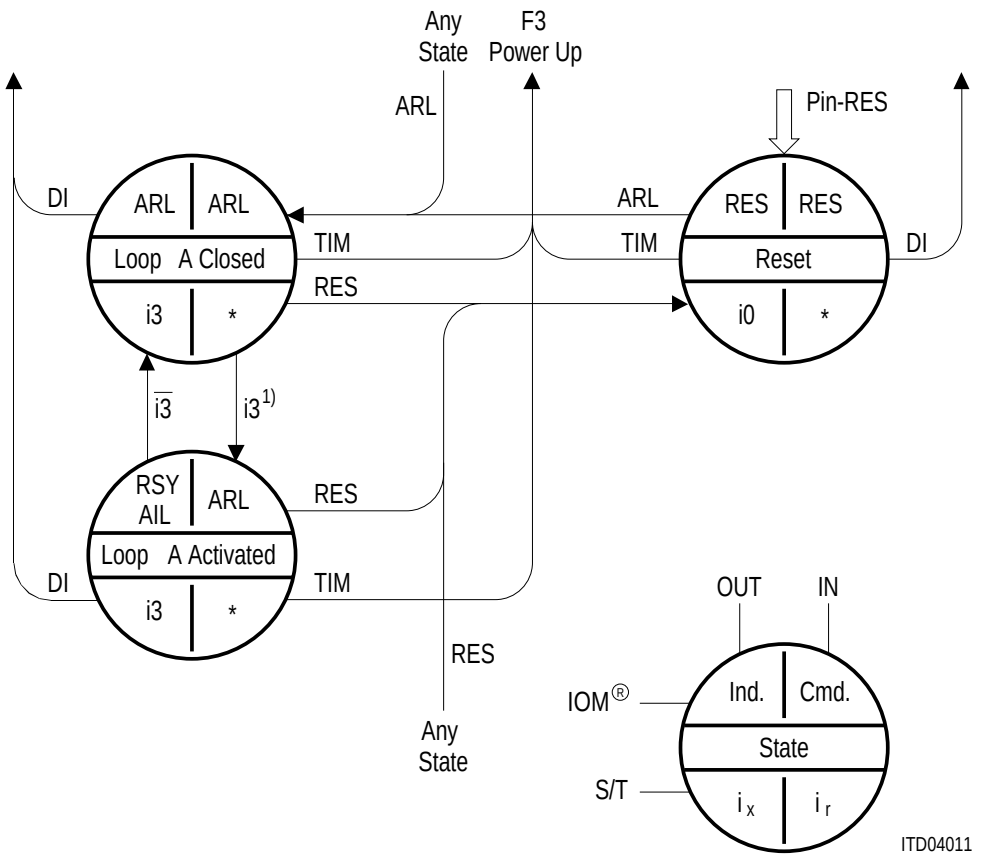
4.3.1.1 TE/LT-T Modes State Diagram



Notes:

1. See state diagram for unconditional transitions for details
2. x = TM1 or TM 2 or RES or ARL
   $\overline{x}$ = $\overline{TM1}$ & $\overline{TM2}$ & $\overline{RES}$ & $\overline{ARL}$
3. AR_P = AR8 or AR10
4. AI_P = AI8 or AI10
5. TMI = TM1 or TM2

Figure 66
State Transition Diagram in TE/LT-T Modes



Note:

1. In state “loop A activated” I3 is the internal signal, the external signal is I0.

Figure 67
State Diagram of the TE/LT-T Modes, Unconditional Transitions

4.3.1.2 TE/LT-T Modes Transition Criteria

The transition criteria used by the SBCX are described in the following sections. They are grouped into:

- C/I commands
- Pin states
- Events related to the S/T-interface

4.3.1.2.1 C/I Commands

AR8 Activation Request with priority 8 for D-channel transmission. This command is used to start a TE initiated activation. D-channel priority 8 is the highest priority. It should be used to request signaling information transfer.

AR10 Activation request with priority 10 for D-channel transmission. This command is used to start a TE initiated activation. D-channel priority 10 is the lower priority. It should be used to request packet data transfer.

ARL Activation request loop. The SBCX is requested to operate an analog loop-back close to the S/T-interface. ARL is an unconditional command.

DI Deactivation indication. This command transfers the SBCX into “F3 power down” mode and disables the IOM-2 clocks.

RES Reset of state machine. Transmission of Info 0. No reaction to incoming infos. RES is an unconditional command.

All **MAI pins** are tristate during $\overline{RST}$ = 0 or when the SBCX is in the state “reset”, unless MAIM is programmed to 1. After reset four pins, MAI (3:0), are operated as input pins and four pins, MAI (7:4), as output pins (push/pull). The value after reset is 0.

TIM Timing Request. Requests the SBCX to change into power-up state and provide timing signals on IOM-2.

TM1 Test Mode 1. Transmission of single pulses on the S/T-interface. The pulses are transmitted with alternating polarity at a frequency of 2 kHz. TM1 is an unconditional command.

TM2 Test Mode 2. Transmission of continuous pulses on the S/T-interface. The pulses are sent with alternating polarity at a rate of 96 kHz. TM2 is an unconditional command.

4.3.1.2.2 Pin States

Pin-RES Pin-Reset. Corresponds to a low level at pin $\overline{RST}$. At power up, a reset pulse ($\overline{RST}$ low active) of minimum 1 µs should be applied to bring the SBCX to the state “reset”. After that the SBCX may be operated according to the state diagrams. In NT mode the DCL is needed during the hardware reset (RES = 0) for initialization. The devices working together with the SBCX in NT mode (i.e. IECs and IBC) automatically deliver the necessary clocks. The function of this pin is identical to the C/I code RES concerning the state machine.

Pin-CON A low at this input disables the TE/LT-T activation capability by preventing INFO 1 to be sent. This pin is used in conjunction with power-controllers to control activation capability under emergency power conditions.

4.3.1.2.3 S/T-Interface Events

I0 INFO 0 detected

$\overline{I0}$ A signal different to INFO 0 was detected

I2 INFO 2 detected

I4 INFO 4 detected

SLIP SLIP detected (applicable in LT-T mode only) IOM-2 interface framing and S/T-interface framing differences have exceeded the specified limit. It is likely that data will be lost to enable a resynchronization.

4.3.1.3 Transmitted Signals and Indications in TE/LT-T Modes

The following signals and indications are issued on the IOM-2 and S/T-interface.

4.3.1.3.1 C/I Indications

Abbreviation	Indication	Remark
DR	Deactivate Request	Deactivation request via S/T-interface
RES	Reset	Reset acknowledge
TM1	Test mode 1	TM1 acknowledge
TM2	Test mode 2	TM2 acknowledge
SLIP	Slip detected (LT-T only)	Wander is larger than 50 µs peak-to-peak (or 25 µs peak-to-peak if programmed, refer to the C/W/P-bit of the Configuration Register)
RSY	Resynchronization during level detect	Signal received, receiver not synchronous
MAIC	MAI change	Pin MAIn has changed
DIS	Disconnected	Pin CON (pin MAI1) connected to GND
PU	Power up	IOM-2 interface clocking is provided
AR	Activate request	Info 2 received
ARL	Activate request loop	Loop A closed
CVR	Far-end-code-violation	After each multi-frame the receipt of at least one illegal code violation is indicated six times. This function must be enabled by setting the RCVE-bit in the configuration register.
AIL	Activate indication loop	Loop A activated
AI8	Activate indication with priority class 8	Info 4 received, D-channel priority is 8 or 9
AI10	Activate indication with priority class 10	Info 4 received, D-channel priority is 10 or 11
DC	Deactivate confirmation	Clocks will be disabled, (in TE), quiescent state

4.3.1.3.2 S/T-Interface Signals

I0	INFO 0
I1	INFO 1
I3	INFO 3
It	Pseudo-ternary pulses at 2 kHz frequency (alternating, TM1) Pseudo-ternary pulses at 96 kHz frequency (alternating, TM2)

4.3.1.4 States TE/LT-T Mode

F3 power down

This is the deactivated state of the physical protocol. The received line awake unit is active. In TE mode, clocks are disabled.

F3 power up

This state is dependent of the logical level of CON (pin MAI1)

CON = 1: This state is similar to “F3 power down”. The state is invoked by a C/I command TIM = “0000” (or DI static low). After the subsequent activation of the clocks the “Power Up” message is output.

CON = 0: This state is similar to “F3 power down”. The state is invoked by a C/I command TIM = “0000” (or DI static low). After the subsequent activation of the clocks the “Disconnected” message is output.

F3 pending deactivation

The SBCX reaches this state after receiving INFO0 (from states F5 to F8) from F6 and F7 via F5/8. From this state an activation is only possible from the line (transition “F3 pend. deact.” to “F5 unsynchronized”). The power down state may be reached only after receiving DI.

F4 pending activation

Activation has been requested from the terminal, INFO 1 is transmitted, INFO 0 is still received, “Power Up” is transmitted in the C/I channel. This state is stable: timer T3 (I.430) is to be implemented in software.

F5/8 unsynchronized

At the reception of any signal from the NT, the SBCX ceases to transmit INFO 1, adapts its receiver circuit, and awaits identification of INFO 2 or INFO 4. This state is also reached after the SBCX has lost synchronism in the states F6 or F7 respectively.

F6 synchronized

When the SBCX receives an activation signal (INFO 2), it responds with INFO 3 and waits for normal frames (INFO 4).

F7 activated

This is the normal active state with the layer 1 protocol activated in both directions. From state “F6 synchronized”, state F7 is reached almost 0.5 ms after reception of INFO 4.

F7 slip detected

When a slip is detected between the S/T-interface clocking system and the IOM-2 interface clocks (phase wander greater than 50 µs, data may be disturbed, or 25 µs if programmed in the configuration register) the SBCX enters this state, synchronizing again the internal buffer. After 0.5 ms this state is left again (only possible in LT-T mode).

Unconditional States TE/LT-T Mode

Loop A closed

On Activate Request Loop command, INFO 3 is sent by the line transmitter internally to the line receiver (INFO0 is transmitted to the line). The receiver is not yet synchronized.

Loop A activated

The receiver is synchronized on INFO 3 which is looped back internally from the transmitter. Data may be sent. The indication “AIL” is output to indicate the activated state. When the S/T line awake detector, which is switched to the line, detects an incoming signal, this is indicated by “RSY”.

Test mode 1

Single alternating pulses are sent on the S/T-interface (2 kHz repetition rate)

Test mode 2

Continuous alternating pulses are sent on the S/T-interface (96 kHz)

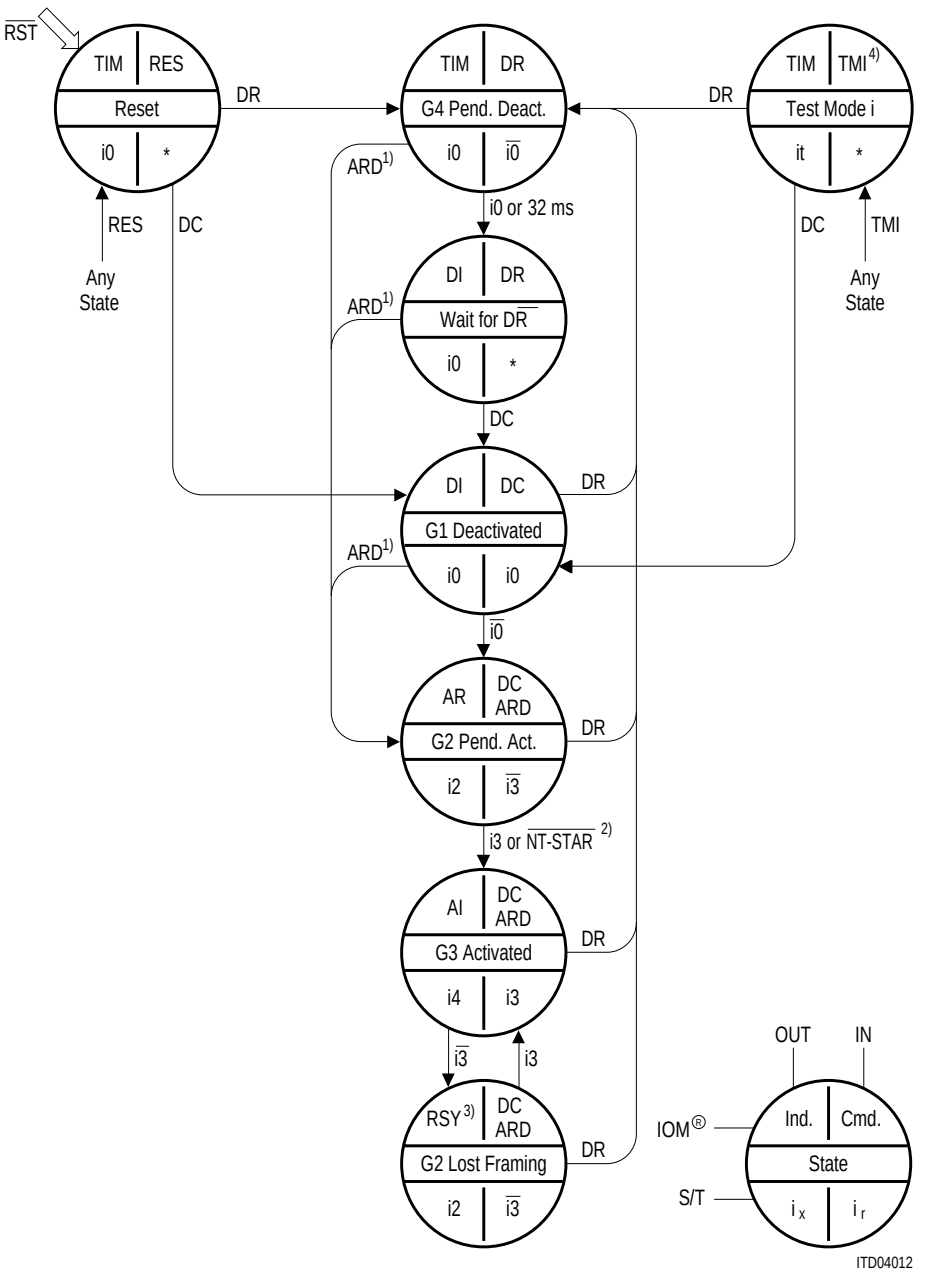
Reset state

A hardware or software reset (RES) forces the SBCX to an idle state where the analog components are disabled (transmission of INFO0) and the S/T line awake detector is inactive. Thus activation from the NT is not possible. Clocks are still supplied and the outputs are in a low impedance state.

4.3.2 State Machine LT-S Mode

Section 4.3.2 is applicable for LT-S mode.

4.3.2.1 LT-S Mode State Diagram



Notes:

1. ARD stands for AR or ARL
2. NT star: transition from ‘G2 pend. act.’ to ‘G3 activated’ takes place when the first branch of the star is synchronized
3. NT star: Transition from state ‘G3 activated’ to ‘G2 Lost Framing’ is disabled.
4. TMI = TM1 or TM2

Figure 68
State Transition Diagram in LT-S Mode

4.3.2.2 LT-S Mode Transition Criteria

The transition criteria used by the SBCX are described in the following sections. They are grouped into:

- C/I commands
- Pin states
- Events on the S/T-interface.

4.3.2.2.1 C/I Commands

AR Activation Request. This command is used to start an exchange initiated activation.

ARL Activation request loop. The SBCX is requested to operate an analog loop-back close to the S/T-interface.

DC Deactivation Confirmation. Transfers the LT-S into a deactivated state in which it can be activated from a terminal (detection of $\overline{\text{INFO 0}}$ enabled).

DR Deactivation Request. Initiates a complete deactivation from the exchange side by transmitting INFO 0. Unconditional command.

RES Please refer to **section 4.3.1.2.1** for details.

TM1 Test Mode 1. Transmission of single pulses on the S/T-interface. The pulses are transmitted with alternating polarity at a frequency of 2 kHz. TM1 is a unconditional command.

TM2 Test Mode 2. Transmission of continuous pulses on the S/T-interface. The pulses are sent with alternating polarity at a rate of 96 kHz. TM2 is a unconditional command.

4.3.2.2.2 Pin States

Pin-$\overline{\text{RES}}$ Pin Reset. Please refer to **section 4.3.1.2.2**

Pin-$\overline{\text{NT-STAR}}$ Device operates in NT-STAR mode. In this mode detection of INFO 3 is not essential in the state"G2 pend. act." for a transfer to "G3 activated". The transfer will be accomplished as soon as any one branch of the star is synchronized.
$\overline{\text{NT-STAR}}$ set to LOW will disable the transition from "G3 activated" to "G2 Lost framing". Therefore, C/I indication "AI" will stay even when i3 is lost.

4.3.2.2.3 S/T-Interface Events

I0 INFO 0 detected

$\overline{\text{I0}}$ Level detected (signal different to I0)

I3 INFO 3 detected

$\overline{\text{I3}}$ Any INFO other than INFO 3

4.3.2.3 Transmitted Signals and Indications in LT-S Mode

The following signals and indications are issued on the IOM-2 and S/T-interface.

4.3.2.3.1 C/I Indications

Abbreviation	Indication (upstream) LT-S mode	Remark
TIM	Timing	Interim indication during deactivation procedure
RSY	Resynchronizing	Receiver is not synchronous
MAIC	MAI change	Pin MAIn has changed. MAI (3:0) pins summarized and monitored in one indication.
AR	Activate request	$\overline{\text{INFO 0}}$ received from terminal. Activation proceeds.
CVR	Far-end-code-violation	After the receipt of at least one illegal code violation CVR is indicated six times. This function must be enabled by setting the RCVE-bit in the configuration register.
AI	Activate indication	Synchronous receiver, i.e. activation completed.
DI	Deactivate indication	Timer (32 ms) expired or INFO 0 received after deactivation request

4.3.2.3.2 S/T-Interface Signals

I0	INFO 0
I2	INFO 2
I4	INFO 4
It	Pseudo ternary pulses at 2-kHz frequency (TM1). Pseudo ternary pulses at 96-kHz frequency (TM2).

4.3.2.4 States LT-S Mode

G1 deactivated

The SBCX is not transmitting. There is no signal detected on the S/T-interface, and no activation command is received in the C/I channel.

G2 pending activation

As a result of an $\overline{\text{INFO 0}}$ detected on the S/T line or an ARD command, the SBCX begins transmitting INFO 2 and waits for reception of INFO 3. The timer to supervise reception of INFO 3 is to be implemented in software. In case of an ARL command, loop 2 is closed.

G3 activated

Normal state where INFO 4 is transmitted to the S/T-interface. The SBCX remains in this state as long as neither a deactivation nor a test mode is requested, nor the receiver loses synchronism.

When receiver synchronism is lost, INFO 2 is sent automatically. After reception of INFO 3, the transmitter keeps on sending INFO 4.

G2 lost framing

This state is reached when the SBCX has lost synchronism in the state G3 activated.

G4 pending deactivation

This state is triggered by a deactivation request DR. It is an unstable state: indication DI (state “G4 wait for DR.”) is issued by the SBCX when:

either INFO0 is received,

or an internal timer of 32 ms expires.

G4 wait for DR

Final state after a deactivation request. The SBCX remains in this state until a response to DI (in other words DC) is issued.

Test mode 1

Single alternating pulses are sent on the S/T-interface (2-kHz repetition rate).

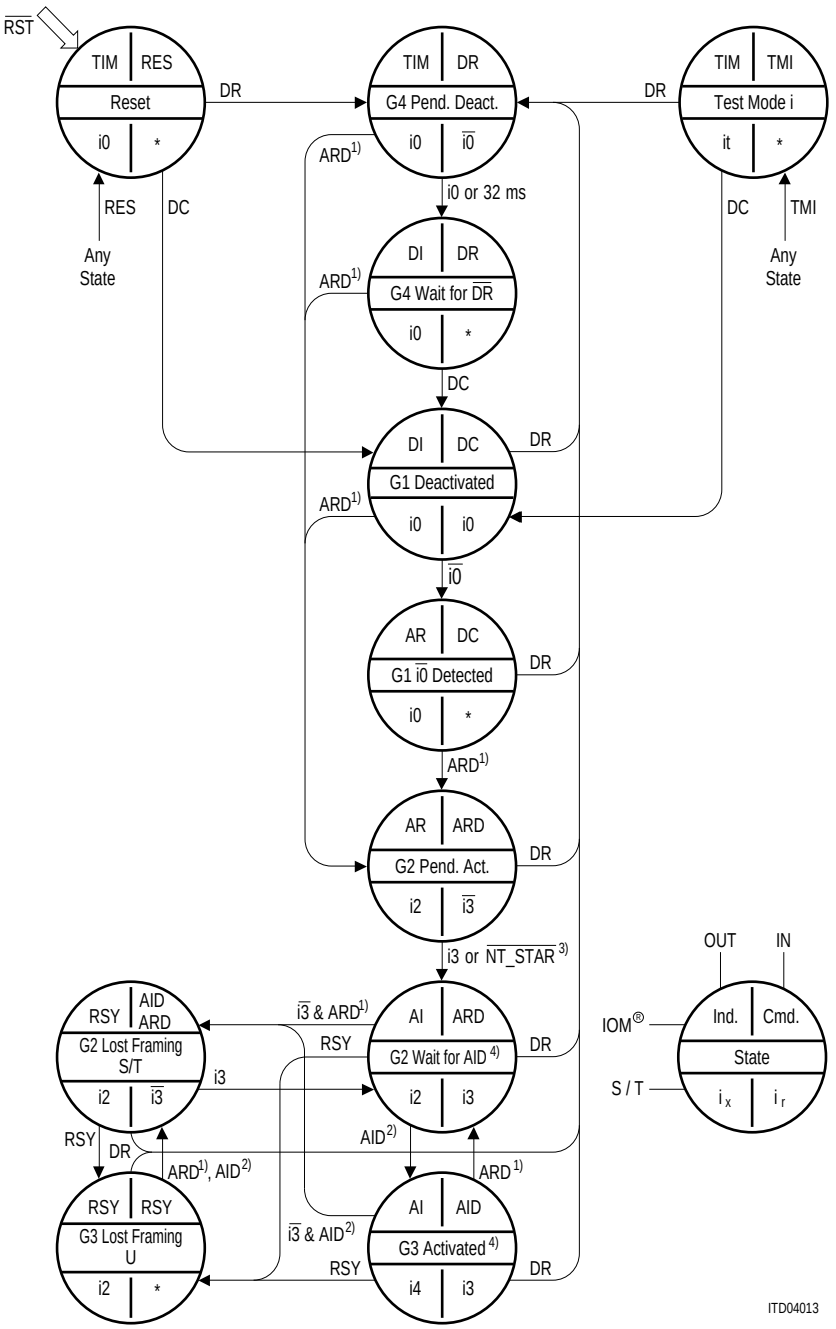
Test mode 2

Continuous alternating pulses are sent on the S/T-interface (96 kHz).

4.3.3 State Machine NT Mode

Section 4.3.3 is applicable for NT mode.

4.3.3.1 NT Mode State Diagram



Notes:

1. ARD = AR or ARL
2. AID = AI or AIL
3. Transition takes place as soon as one branch of the star has detected INFO 3.
4. With NT-STAR selected transfer to “G2 lost framing” state is not possible.

Figure 69
NT Mode State Diagram

4.3.3.2 NT Mode Transition Criteria

The transition criteria used by the SBCX are described in the following sections. They are grouped into:

- C/I commands
- Pin states
- Events or the S/T-interface.

4.3.3.2.1 C/I Commands

AR Activation Request. This command is used to start an exchange initiated activation.

ARL Activation request loop. The SBCX is requested to operate an analog loop-back close to the S/T-interface.

AI Activation Indication. Confirms that the U-interface is fully transparent, on D-channel data transfer is allowed.

AIL Activation Indication loop.

DC Deactivation Confirmation. Transfers the NT into a deactivated state in which it can be activated from a terminal (detection of $\overline{\text{INFO 0}}$ enabled).

DR Deactivation Request. Initiates a complete deactivation from the exchange side by transmitting INFO 0. Unconditional command.

RES Please refer to **section 4.3.1.2.1** for details.

RSY Resynchronizing. The U-interface has not obtained or lost synchronization. INFO 2 is transmitted consequently by the SBCX.

TM1 Test Mode 1. Transmission of single pulses on the S/T-interface. The pulses are transmitted with alternating polarity at a frequency of 2 kHz. TM1 is an unconditional command.

TM2 Test Mode 2. Transmission of continuous pulses on the S/T-interface. The pulses are sent with alternating polarity at a rate of 96 kHz. TM2 is an unconditional command.

4.3.3.2.2 Pin States

Pin-$\overline{\text{RES}}$ Pin Reset. Please refer to **section 4.3.1.2.2** for details.

Pin-$\overline{\text{NT-STAR}}$ Device operates in NT-STAR mode. In this mode detection of INFO 3 is not essential for a transfer to “G2 wait for AI”. The transfer will be accomplished as soon as any one branch of the star is synchronized.

A transfer from states “G2 wait for AI” and “G3 activated” to state “G2 lost framing” is not possible with $\overline{\text{NT-STAR}}$ pin set to low.

Pin-TM1 Transfers the SBCX into the “Test mode i” state. Here a 2-kHz signal of alternating pulses is transmitted on the S/T-interface.

Pin-TM2 Transfers the SBCX into “Test Mode i” state. Here a signal consisting of continuous binary ZEROs is sent at the rate of 96 kHz.

4.3.3.2.3 S/T-Interface Events

I0 INFO 0 detected

$\overline{\text{I0}}$ Level detected (any signal different to I0)

I3 INFO 3 detected

$\overline{\text{I3}}$ Any INFO other than INFO 3.

4.3.3.3 Transmitted Signals and Indications in NT Mode

The following signals and indications are issued on the IOM-2 and S/T-interface.

4.3.3.3.1 C/I Indications

Abbreviation	Indication (upstream) NT Mode	Remark
TIM	Timing	S transceiver requires clock pulses
RSY	Resynchronizing	Receiver is not synchronous
MAIC	MAI change	Pin MAIn has changed
AR	Activate request	$\overline{\text{INFO 0}}$ received
CVR	Far-end-code-violation	After each multi-frame the receipt of at least one illegal code violation is indicated six times. This function must be enabled by setting the RCVE-bit in the configuration register.
AI	Activate indication	Synchronous receiver
DI	Deactivate indication	Timer (32 ms) expired or INFO 0 received after deactivation request

4.3.3.3.2 S/T-Interface Signals

I0	INFO 0
I2	INFO 2
I4	INFO 4
It	Pseudo ternary pulses at 2-kHz frequency (TM1). Pseudo ternary pulses at 96-kHz frequency (TM2).

4.3.3.4 States NT Mode

G1 Deactivated

The SBCX is not transmitting. No signal is detected on the S/T-interface, and no activation command is received in C/I channel. DI is output in the normal deactivated state, and TIM is output as a first step when an activation is requested from the S/T-interface.

G1 $\overline{\text{I0}}$ Detected

An $\overline{\text{INFO 0}}$ is detected on the S/T-interface, translated to an “Activation Request” indication in the C/I channel. The SBCX is waiting for an AR command, which normally indicates that the transmission line upstream (usually a two-wire U interface) is synchronized.

G2 Pending Activation

As a result of the ARD command, and INFO 2 is sent on the S/T-interface. INFO 3 is not yet received. In case of ARL command, loop 2 is closed.

G2 wait for AID

INFO 3 was received, INFO 2 continues to be transmitted while the SBCX waits for a “switch-through” command AID from the device upstream.

G3 Activated

INFO 4 is sent on the S/T-interface as a result of the “switch through” command AID: the B and D-channels are transparent. On the command AIL, loop 2 is closed.

G2 Lost Framing S/T

This state is reached when the SBCX has lost synchronism in the state G3 activated.

G3 Lost Framing U

On receiving an RSY command which usually indicates that synchronization has been lost on the two-wire U interface, the SBCX transmits INFO 2.

G4 Pend. Deact.

This state is triggered by a deactivation request DR, and is an unstable state. Indication DI (state “G4 wait for DR”) is issued by the SBCX when:

either INFO0 is received

or an internal timer of 32 ms expires.

G4 wait for DR

Final state after a deactivation request. The SBCX remains in this state until an “acknowledgment” to DI (DC) is issued.

Test Mode 1

Single alternating pulses are sent on the S/T-interface (2-kHz repetition rate).

Test Mode 2

Continuous alternating pulses are sent on the S/T-interface (96 kHz).

4.4 Reset

4.4.1 C/I Command RES

Reset of the layer-1 state machine. SBCX is transmitting info 0 and does not react on received infos. RES is an unconditional command.

4.4.2 Hardware Reset $\overline{\text{RST}}$

All SBCX registers are set back to their initial values. At power up a reset pulse ($\overline{\text{RST}}$ = low active) of minimum 1 µs should be applied to bring SBCX to the state “reset” in the L1 state machine. After that the SBCX may be operated according to the state diagrams.

In NT mode the DCL is needed during the hardware reset for initialization. The devices fitting to the SBCX in NT mode (i.e. IECs and IBC) deliver the necessary clocks automatically.

All MAI pins are tristate during $\overline{\text{RST}}$ = 0 or when the SBCX is in the state ‘reset’, unless MAIM is programmed to 1. After reset MAI (3:0) are operated as input pins and MAI (7:4) as output pins (push/pull). The value after reset is 0.

IDP0 and IDPI are tristate during $\overline{\text{RST}}$ = ‘0’.

4.4.3 Push/Pull Sensing

After the hardware reset the SBCX senses in the monitor channel timeslot during the first two IOM frames, whether an external pull-up resistor is connected or not to pin IDP0. During this time of sensing it is necessary, that no other device connected to IDP0 sends informations in the monitor channel. As a result of the sensing procedure the pins IDP0, IDP1, X3 (if CEB) and MAI5 (if S/G) are either open drain outputs and therefore require the same pull-up resistor as pin IDP0 or push/pull outputs. Please note that the IOM-2 Interface Specification describes open drain data lines (IDP0 and IDP1) with external pull-up resistors. However, if operation is logical point-to-point, tristate operation is possible as well for the data lines.

4.4.4 Initializing LT-T Mode

If the ‘Mode’ pin is pin strapped to 1, after Hw-Reset the SBCX will start in LT-S mode. Until the SBCX is switched to LT-T mode by register setting, it may react to incoming signals on S_0. Therefore the following sequence should be used:

Hw-Reset
Sw-Reset (write command ‘RES’ to C/I)
release Hw-Reset
program Configuration Register: MODE to 1 for LT-T Mode
write command ‘TIM’ to C/I

4.5 Maintenance Functions

The technical description of maintenance functions follows in the next sections. The sections “Test Modes” and “System Measurement” of chapter 3 have not been included as they contain primarily application information.

4.5.1 Test Loop-Backs

4.5.1.1 Complete Loop-Backs (No. 2, No. 3, and No. A)

Function

The analog loop may be closed in three different locations: in the NT1 (No. 2), the NT2 (No. 3) and the terminal or PBX (No. A). The loop is closed close to the S/T-interface. No external S/T-interface circuitry is required to close these loop-backs.

Initialization

Two alternatives are provided to close the complete loop-back.

The first method makes use of the C/I command ARL. In TE and LT-T modes “ARL” is regarded as an unconditional command. It may therefore be issued independently of the current operational state. In NT and LT-S modes the “ARL” command is recognized in the states:

- G4 pending deactivation
- G4 wait for $\overline{DR}$
- G1 deactivated
- G1 $\overline{I0}$ detected (NT only)

The command “ARL” has to be applied continuously while the loop-back is required.

The second alternative to close the analog loop-back is to set the “SC” bit in the loop-back register. This option is only available in LT-S and NT mode when the device is fully activated (C/I = AI).

Transparency

The user may choose whether the complete loop-back data is to be put transparently onto the S/T-interface or not. The selection is performed with the “LP” bit in the configuration register.

4.5.1.2 Single Channel Loop-Backs (No. 4, No. B_2, No. C)

Function

Partial loop-backs may be closed on the IOM-2 or the S/T-interface. Loop-backs No. B_2 (NT2), No. C (NT1) and No. 4 (terminal and PBX) are closed on IOM-2 and loop-back the data from the S/T-interface.

Initialization

Partial loop-backs are entirely controlled by the loop-back register. Loop-backs are available for both B channels on the S/T and IOM-2 interface.

By setting the corresponding bit in the loop-back register to ONE a loop-back is closed. IOM-2 loop-backs (IB1, IB2) may be closed in combination, i.e. IB1 = ONE and IB2 = ONE will close loop-backs for both B channels. Additionally the command IB12 allows to interchange the B1 and B2 channel. IB12 only works in conjunction with IB1 and IB2. S/T loop backs (SB1, SB2) can be closed in LT-S and NT mode.

Single channel loop-backs can only be closed in the fully activated state.

Transparency

All single channel loop-backs are transparent.

4.5.2 Monitoring of Illegal Code Violations

Function

Any illegal code violations on the S/T bus result in the C/I Code “CVR” to be issued in 6 successive IOM-2 frames. This function is implemented according to ANSI T1.605. It is independent of multiframing.

Initialization

The detection of illegal code violations is enabled by setting bit “RCVE” in the configuration register to ONE.

4.6 Clock Generation and Clock Characteristics

This section deals with clock generation requirements for slave and master modes and the characteristics of clock signals produced by the SBCX.

The following requirements apply to all operational SBCX modes:

Clock Requirements

Master clock nominal frequency: 7.68 MHz

Master clock overall tolerance: ± 100 ppm

Master clock duty cycle: **see figure 70**

The inputs are driven at 2.4 V for a logic “1” and 0.45 V for a logic “0”.

The timing measurements are made at 3.5 V for a logic “1” and 0.8 V for a logic “0”.

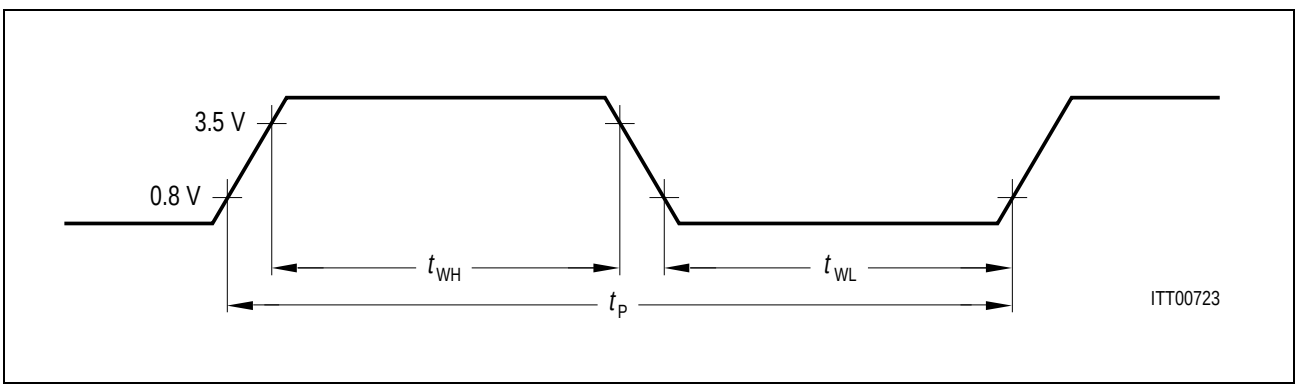


Figure 70
Dynamic Characteristics of Duty Cycle

Table 25
Duty Ratio

Pin	Parameter	Symbol	Limit Values		Unit
			min.	max.	
XTAL1, XTAL2	High phase of crystal/clock	t_{WH}	35		ns
	Low phase of crystal/clock	t_{WL}	35		ns
	Period of crystal/clock	t_P	130.08	130.34	ns

Crystal specification and recommendations regarding the oscillator circuit are presented in **section 4.7.2**.

Propagation Delay

The delay from the IOM-2 to the S/T-interface and vice versa is independent of the direction.

Table 26

Parameter	Limit Values			Unit	Condition
	min.	typ.	max.		
Signal delay S → IOM	45	65	90	µs	C_L = 150 pF
Signal delay IOM → S	45	65	90	µs	C_L = 150 pF

The requirements for input jitter and the operation of the implemented transmit and receive PLLs are dependent on the operational SBCX modes. Details on these themes are described in the following sections.

4.6.1 NT and LT-S Mode

4.6.1.1 Transmit and Receive PLL

The transmit PLL (XPLL) synchronizes a 192 kHz transmit bit clock to the IOM-2 clock FSC (8 kHz) derived from the oscillator clock.

When the oscillator clock is synchronous to FSC (fixed divider ratio of 960) the XPLL will not perform any tracking after having locked the phase, i.e. the input jitter on clocks XTAL and FSC will not be increased.

Alternatively, when a free running oscillator is used, XPLL tracking increases FSC jitter by 130 ns. This reduces the allowable input jitter of FSC to less than 130 ns peak-to-peak (see also following section “jitter”).

- In a point-to-point or extended bus configuration the Receive PLL (RPLL) recovers bit timing from the detector´s output signal and provides a synchronous 1536-kHz clock (adaptive timing recovery from the receive data stream on the S-interface). Divided by eight this clock is used as 192-kHz receive data clock (PP).
- In a passive bus configuration, a 192-kHz receive clock (MP) generated by the transmit PLL (XPLL) is used to sample the input data (fixed timing recovery).

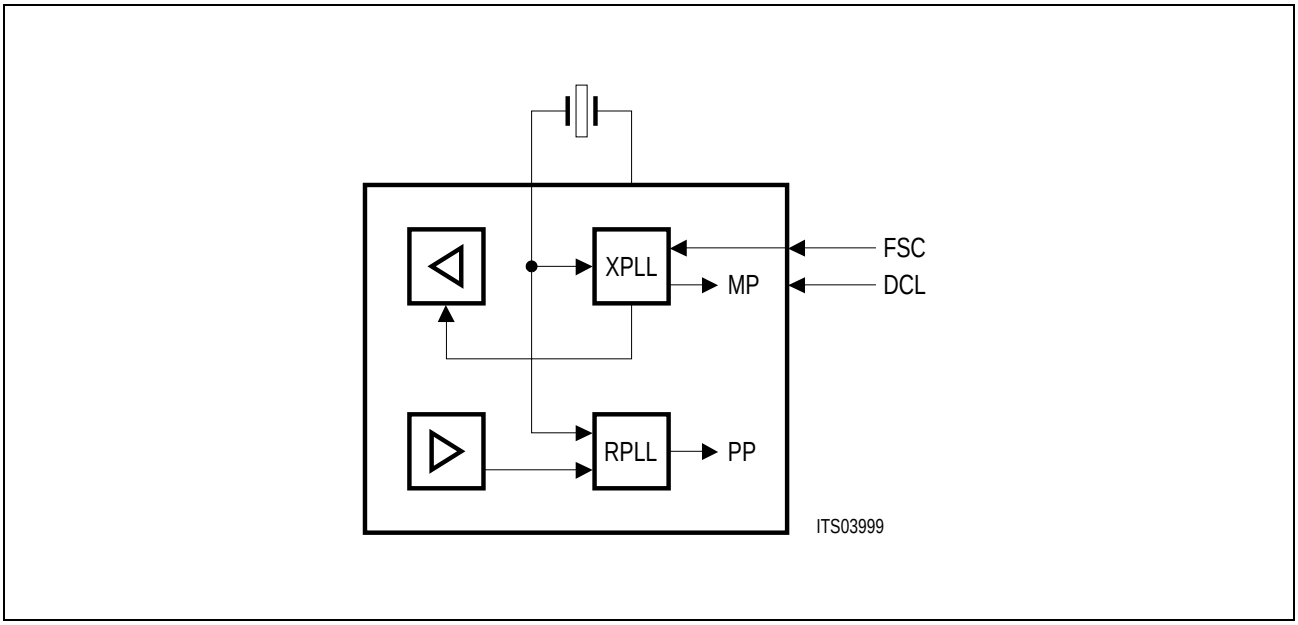


Figure 71
Clock System of the SBCX in NT and LT-S Mode

4.6.1.2 Jitter Requirements

According to ITU I.430 the maximum jitter in an NT output sequence is 5 % of a bit period (260 ns).

Two cases need to be distinguished for SBCX input jitter requirements:

- Crystal as clock source
  With a crystal as clock source the PLL works permanently to synchronize the master clock on to the FSC reference signal. Each tracking step produces 65 ns jitter so that a total of 130 ns “self-initiated” jitter results under ideal circumstances.
  To be below the specified limit the FSC input jitter should not exceed 100 ns (30 ns margin) in this configuration.
- Synchronized, external clock source
  In case an externally synchronized master clock is provided at pin XTAL1, the XPLL stops regulating once it has locked successfully. Therefore no “self-initiated” jitter is produced. All input jitter (FSC and master clock) is passed on transparently to the S/T-interface. The super imposed jitter of FSC and master clock may therefore not exceed 260 ns.

4.6.2 LT-T and TE Mode

4.6.2.1 Receive PLL in TE and LT-T Mode

The Receive PLL (RPLL) recovers bit timing from the detector's output signal and provides a synchronous 1536-kHz clock (adaptive timing recovery). Divided by eight this clock is used as 192-kHz receive data clock and as transmit data clock (PP).

The receive PLL performs PLL tracking each 250 µs after detecting the phase between the F/L transition of the receive signal and the covered clock. A phase adjustment is done by adding or subtracting 65 ns to or from a 1536-kHz clock cycle. The 1536-kHz clock is then used to generate any other clock synchronized to the line.

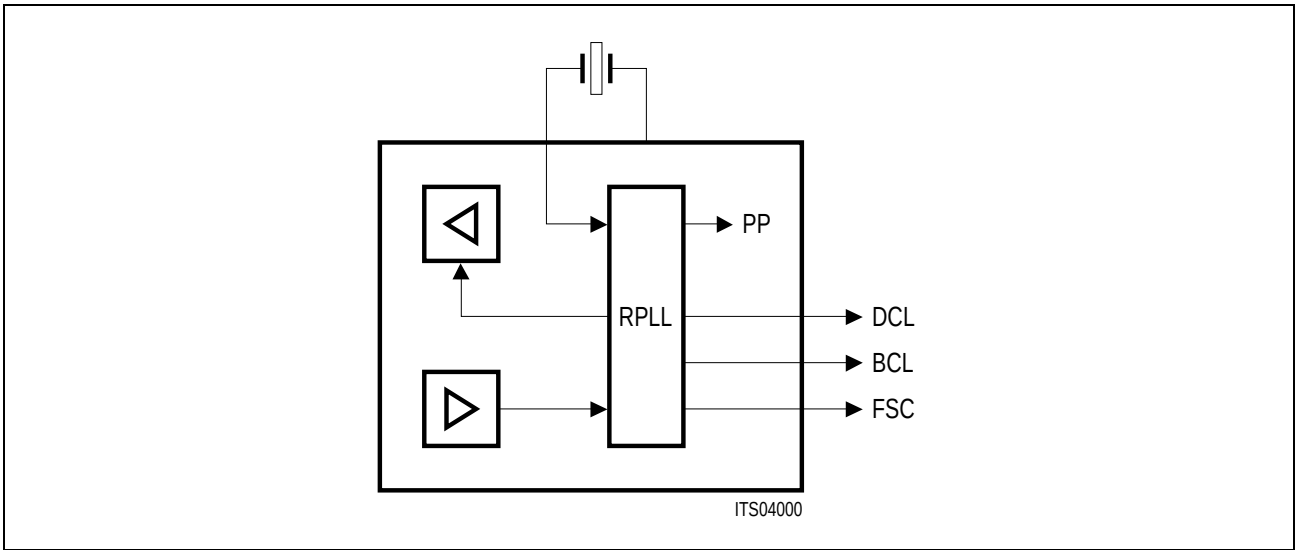


Figure 72
Receive PLL of the SBCX in TE Mode

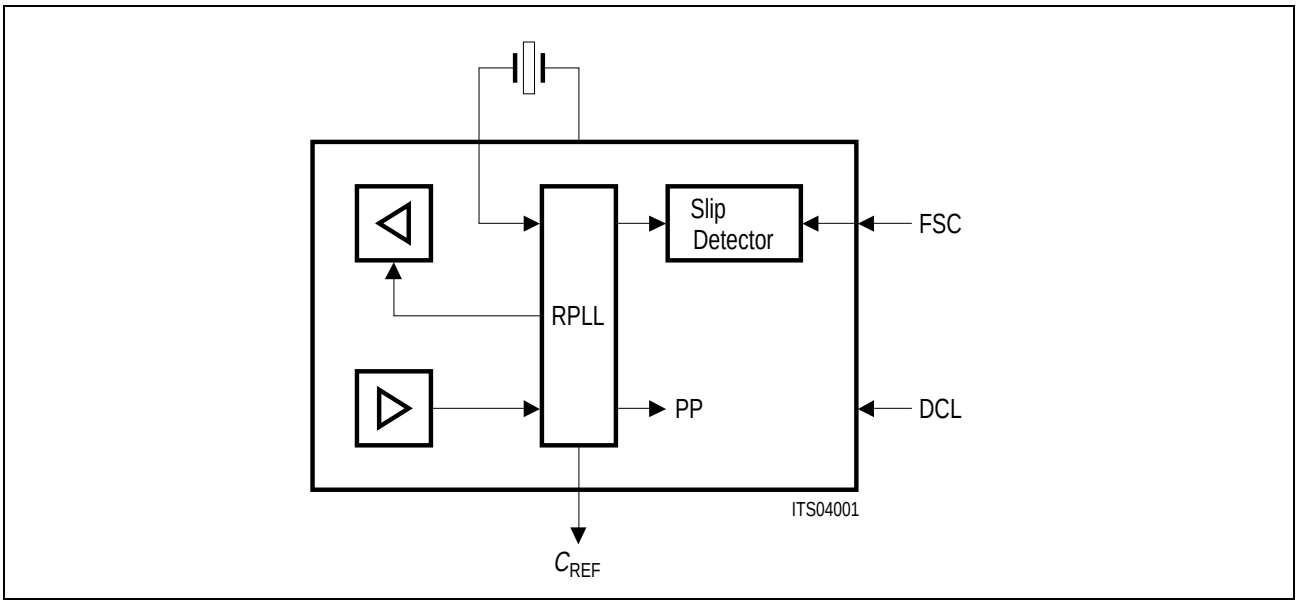


Figure 73
Receive PLL of the SBCX in LT-T Mode

4.7 Elastic Buffers in LT-T Mode

4.7.1 Elastic Buffer

In LT-T mode the SBCX provides a buffer designed as a wander-tolerant system. This is required because the SBCX is a slave to both interfaces and the data clocks of the two interfaces have a time dependent phase relationship. The SBCX enables intermediate storage of 3 x B1 octets, 3 x B2 octets and 6 D-bits for phase difference and wander absorption. The elastic buffer of the SBCX compensates a maximum phase wander of 50 µs peak-to-peak and a slip detector indicates when this limit is exceeded. Setting the C/W/P-bit in the configuration register gives a warning when a slip of 25 µs is exceeded. An indication (Slip detected) is released in the C/I channel. Note that the C/I is only a warning, data has not been lost at this stage.

4.7.1.1 Jitter Requirements

In TE and LT-T mode ITU I.430 specifies a maximum jitter in transmit direction of – 7 % to + 7 %. Because the zero reference is difficult to determine 14 % of bit period (peak to peak) are accepted (i.e. 730 ns).

This specification will be met by the SBCX provided that the master clock source is accurate within 100 ppm (dependent of crystal or external source).

4.7.1.2 Output Clock Characteristics

In TE and LT-T mode various clock signals are supplied by the SBCX to facilitate system design. The following two tables specify these clock signals for TE and LT-T Mode.

Table 27
Clock Characteristics TE Mode

Pin	Parameter	Symbol	Limit Values			Unit	Condition
			min.	typ.	max.		
DCL	Output: 1536 kHz	t_P	520	651	782	ns	osc ± 100 ppm
	Output: 1536 kHz	t_{WH}	175	325	475	ns	osc ± 100 ppm
	Output: 1536 kHz	t_{WL}	300	325	350	ns	osc ± 100 ppm
X3	Output: 768 kHz	t_P	1150	1302	1450	ns	osc ± 100 ppm
	Output: 768 kHz	t_{WH}	520	651	782	ns	osc ± 100 ppm
	Output: 768 kHz	t_{WL}	520	651	782	ns	osc ± 100 ppm
X0 and C/W/P-bit = 0	Output: 32 kHz	t_P	31.1	31.25	31.4	µs	osc ± 100 ppm
	Output: 32 kHz	t_{WH}	15.4	15.6	15.8	µs	osc ± 100 ppm
	Output: 32 kHz	t_{WL}	15.4	15.6	15.8	µs	osc ± 100 ppm

Table 27
Clock Characteristics TE Mode (cont'd)

Pin	Parameter	Symbol	Limit Values			Unit	Condition
			min.	typ.	max.		
X0 and C/W/P-bit = '1'	Output: 16 kHz	t_P	62.3	62.5	62.7	µs	osc ± 100 ppm
	Output: 16 kHz	t_{WH}	31.1	31.25	31.4	µs	osc ± 100 ppm
	Output: 16 kHz	t_{WL}	31.1	31.25	31.4	µs	osc ± 100 ppm

Duty Ratios

Table 28
TE Clock Signals (IOM®-2 mode)

Application	DCL	FSC	X3
TE	o:1536 kHz[1)] 1:1	o:8 kHz[1)] 1:2	o:768 kHz[1)] 1:1

The 1536-kHz clock is phase-locked to the receive S signal and derived using the internal DPLL and the 7.68 MHz ± 100 ppm crystal.

A phase tracking with respect to "S" is performed once in 250 µs. As a consequence of this DPLL tracking, the "high" state of the 1536-kHz clock may be either reduced or extended by one half 7.68-MHz period once every 250 µs. Since the other signals are derived from this clock, the "high" or "low" states may likewise be reduced or extended by the same amount once every 250 µs.

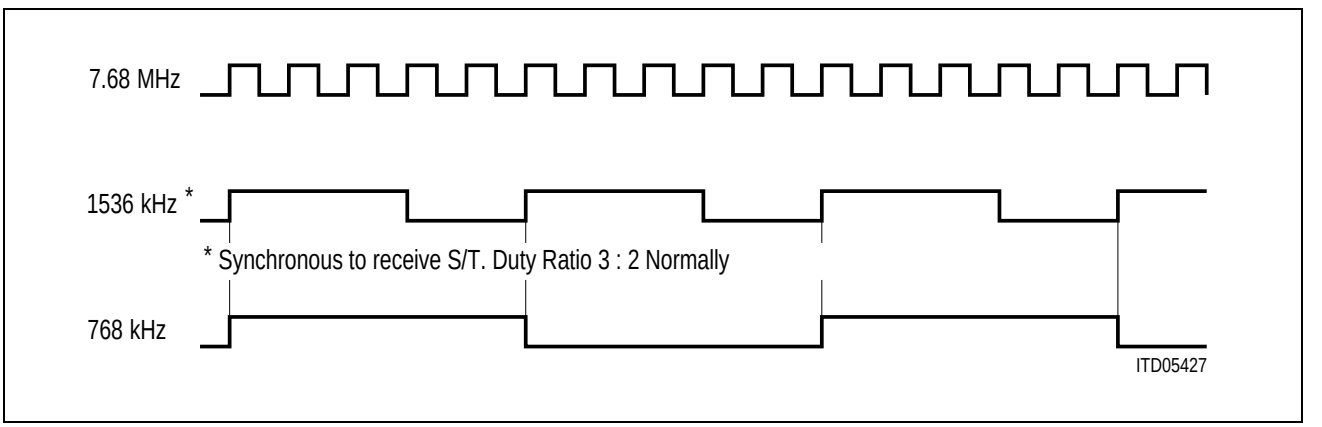


Figure 74
Phase Relationships of TE Clock Signals

Note: 1.536 and 768 kHz may also start with falling edge of 7.68 MHz clock due to the phase tracking mentioned above.

1) Synchronous to receive "S" line

Table 29
Clock Characteristics LT-T Mode

Pin	Parameter	Symbol	Limit Values			Unit	Condition
			min.	typ.	max.		
X3	Output: 1536 kHz	t_P	586	651	716	ns	osc ± 100 ppm
	Output: 1536 kHz	t_{WH}	306	391	476	ns	osc ± 100 ppm
	Output: 1536 kHz	t_{WL}	240	260	281	ns	osc ± 100 ppm

4.7.2 Recommended Oscillator Circuit

In all applications the user has the choice to supply the master clock by crystal or by an external source.

In case a crystal (serial resonance) is connected it should meet the following requirements:

Nominal frequency	7.68 MHz
Overall tolerance (crystal, capacitance…)	100 ppm
Load capacitance	20 pF ± 0.5 pF
Resonance resistance	60 Ω
Shunt capacitance	7 pF
External load capacitance C_L	≤ 50 pF

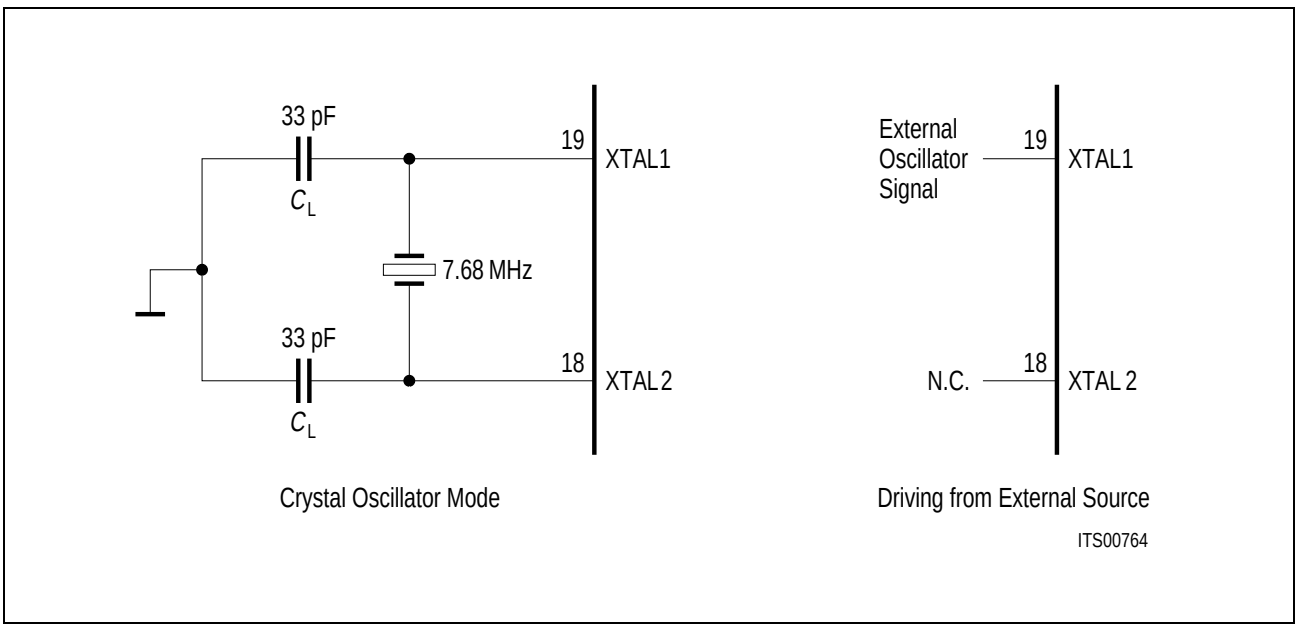


Figure 75
Recommended Oscillator Circuits

4.8 Analog Line Port

The analog part of the SBCX consists of two major building blocks:

- Receiver
- Transmitter

In addition external circuitry is required to connect both transmitter and receiver to the S/T-interface.

The following three sections describe these functional blocks in detail.

4.8.1 Receiver Characteristics

The receiver consists of a differential to single ended input stage, a peak detector and a set of comparators. Additional noise immunity is achieved by digital oversampling after the comparators. The following figure describes the functional blocks of the receiver.

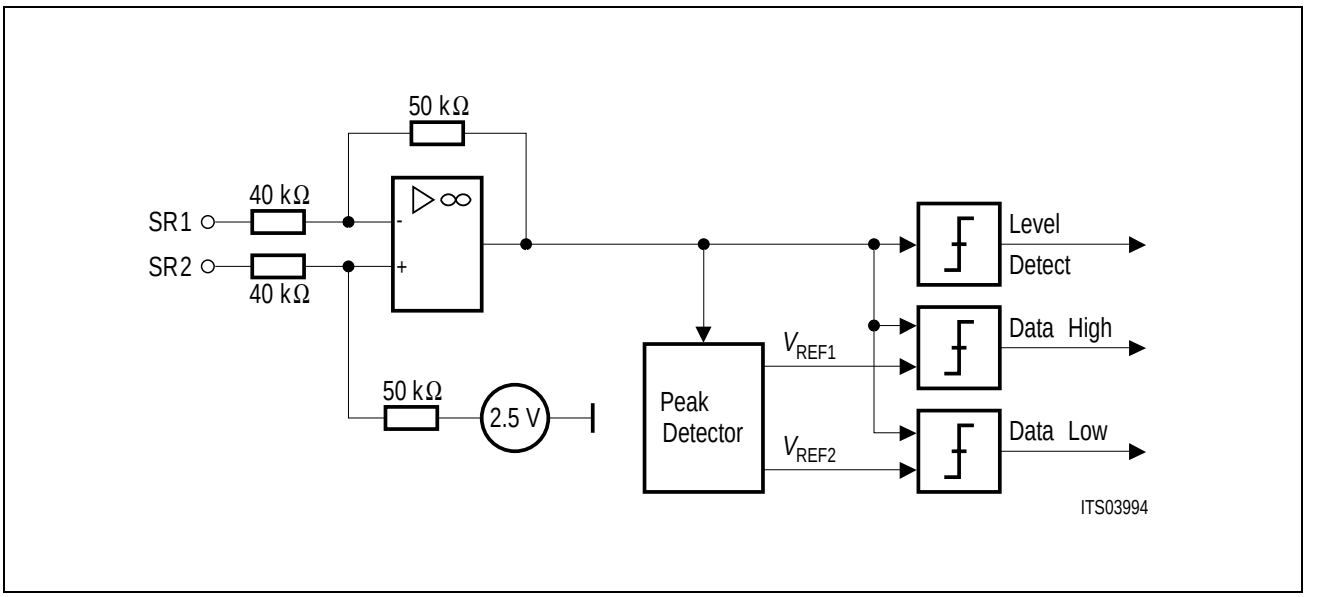


Figure 76
Receiver Circuit

The input stage works together with external 10 kΩ resistors to match the input voltage to the internal thresholds. The data detection thresholds are chosen to 35 % of the peak voltage to increase the performance in extended passive bus configurations. However they never go below 85 mV with respect to the line signal level. This guarantees a maximum line attenuation of at least 13 dB in point-to-point configurations with a margin of more than 70 mVpp with respect to the specified 100 mVpp noise.

Figure 77
Receiver Thresholds

The peak detector requires maximum 2 µs to reach the peak value while storing the peak level for at least 250 µs (RC > 1 ms).

The additional level detector for power up/down control works with fixed thresholds at 100 mV. The level detector monitors the line input signals to detect whether an INFO is present. In TE and LT-T mode, when closing an analog loop, it is therefore possible to indicate an incoming signal during activated loop. In NT and LT-S analog loop-back mode the level detector monitors its own loop signal and an incoming signal is not recognized.

4.8.2 Transmitter Characteristics

The transmitter stage consists of two identical current limited voltage sources, one for each polarity of output pulses. The voltage source guarantees the required output voltages on 50 Ω and 400 Ω loads whereas the 5.6 Ω load is current limited to maximum 13.4 mA. The opposite pin is always switched to ground. The rising and falling edges of the pulses on the 50 Ω load is typically 300 ns. The following figure illustrates the transmitter stage.

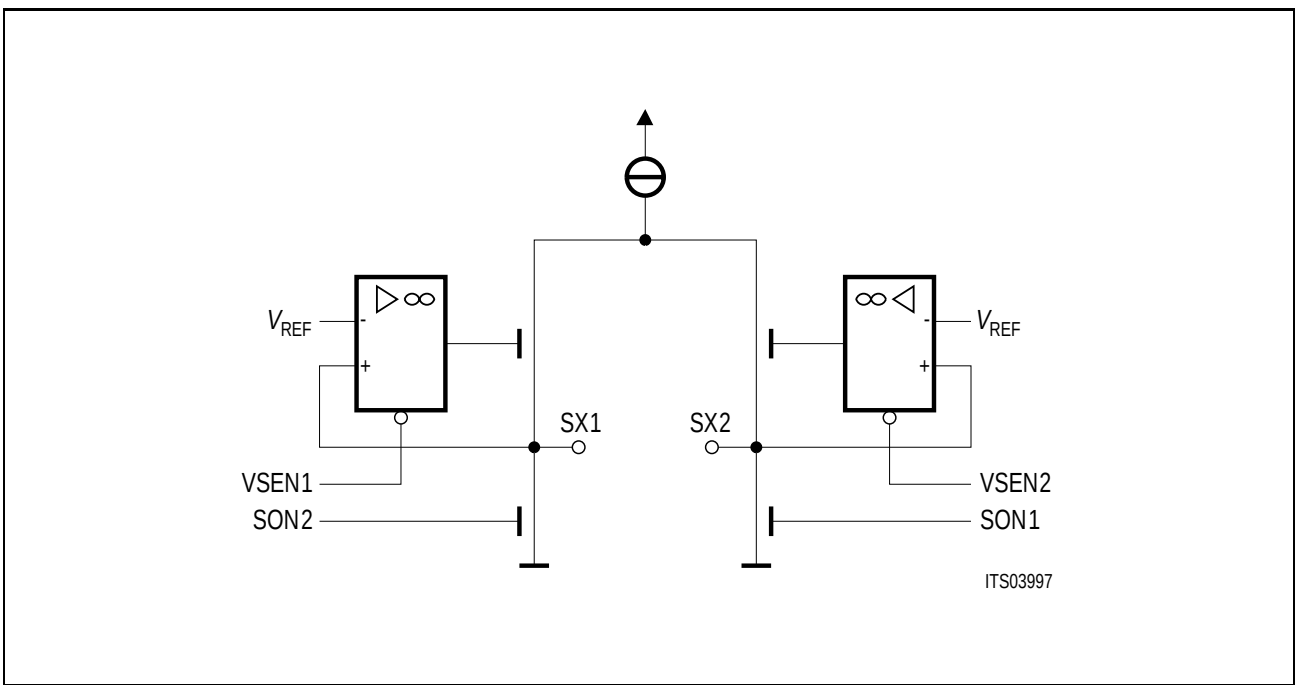


Figure 78
Transmitter Output Stage

The dynamic transmitter characteristics are given by the control signals VSEN1,2 and SON1,2 delivered to the output stage. Both the switch and the voltage source enable signals are simple binary signals with slightly different timing according to the following figure.

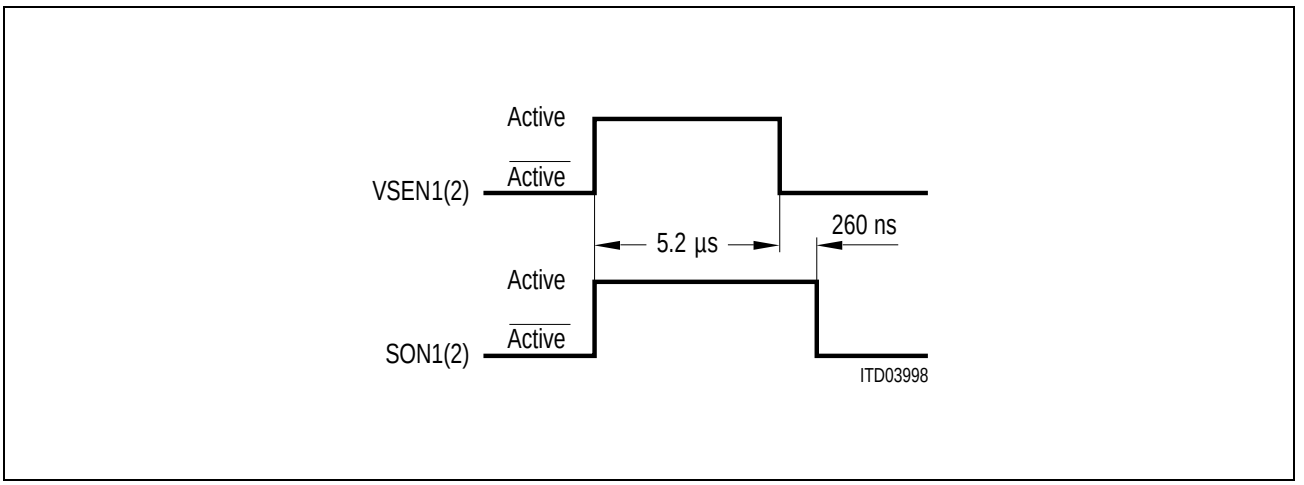


Figure 79
Dynamic Transmitter Characteristics

4.8.3 S/T-Interface Circuitry

In order to comply to the physical requirements of ITU recommendation I.430 and considering the national requirements concerning overvoltage protection and electromagnetic compatibility (EMC), the SBCX needs some additional circuitry.

The **transmitter** of the SBCX is identical to that of both PEB 2080 S-Bus Interface Circuit (SBC) and PEB 2086 ISDN Subscriber Access Controller (ISAC®-S), hence the line interface circuitry should be the same. The external resistors (20 … 40 Ω) are required in order to adjust the output voltage to the pulse mask (nominal 750 mV according to ITU I.430, to be tested with the command “TM1”) on the one hand and in order to meet the output impedance of minimum 20 Ω (transmission of a binary zero according to ITU I.430, to be tested with the command “TM2”) on the other hand.

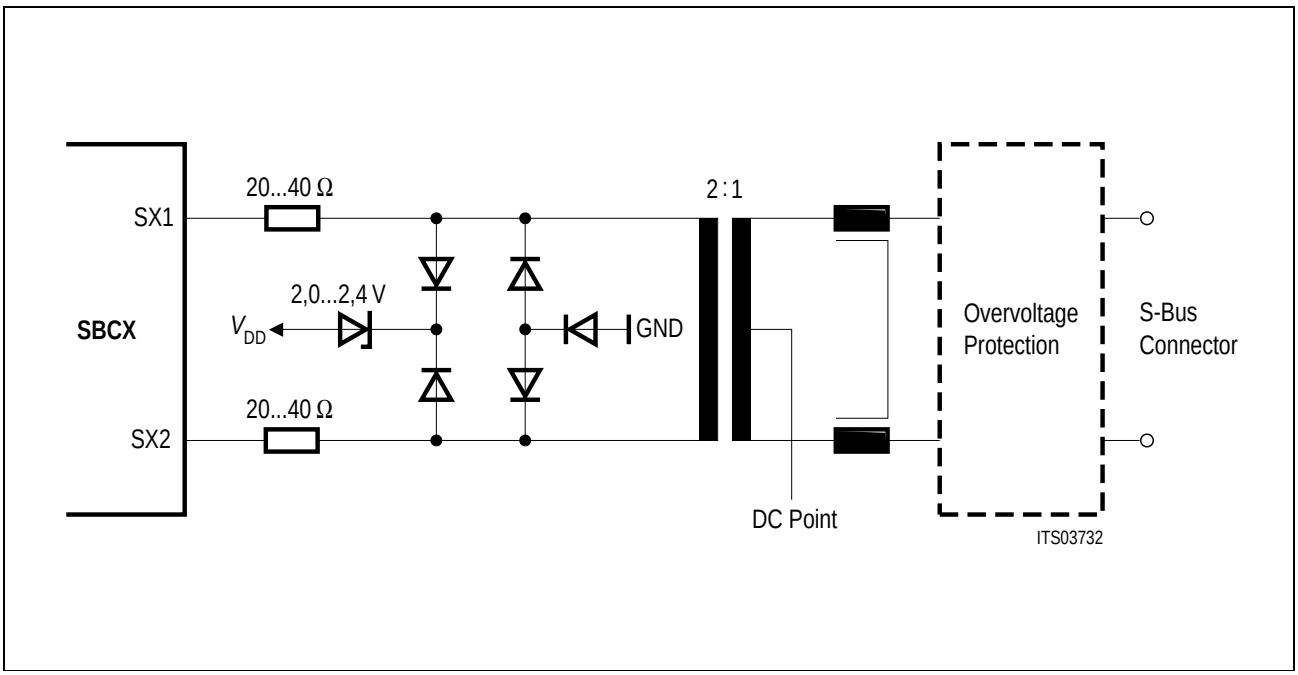


Figure 80
External Circuitry Transmitter

The **receiver** of the SBCX is symmetrical. 10 kΩ overall resistance are recommended in each receive path. Although it is possible to place two single 10 kΩ resistors either between transformer and diode circuit or between chip and diode circuit it is preferable to split the resistance into two resistors for each line. This allows to place a high resistance between the transformer and the diode protection circuit (required to pass 96 kHz input impedance test of ITU I.430). The remaining resistance (2 kΩ) protects the SBCX itself from input current peaks. The following figure illustrates this recommendation.

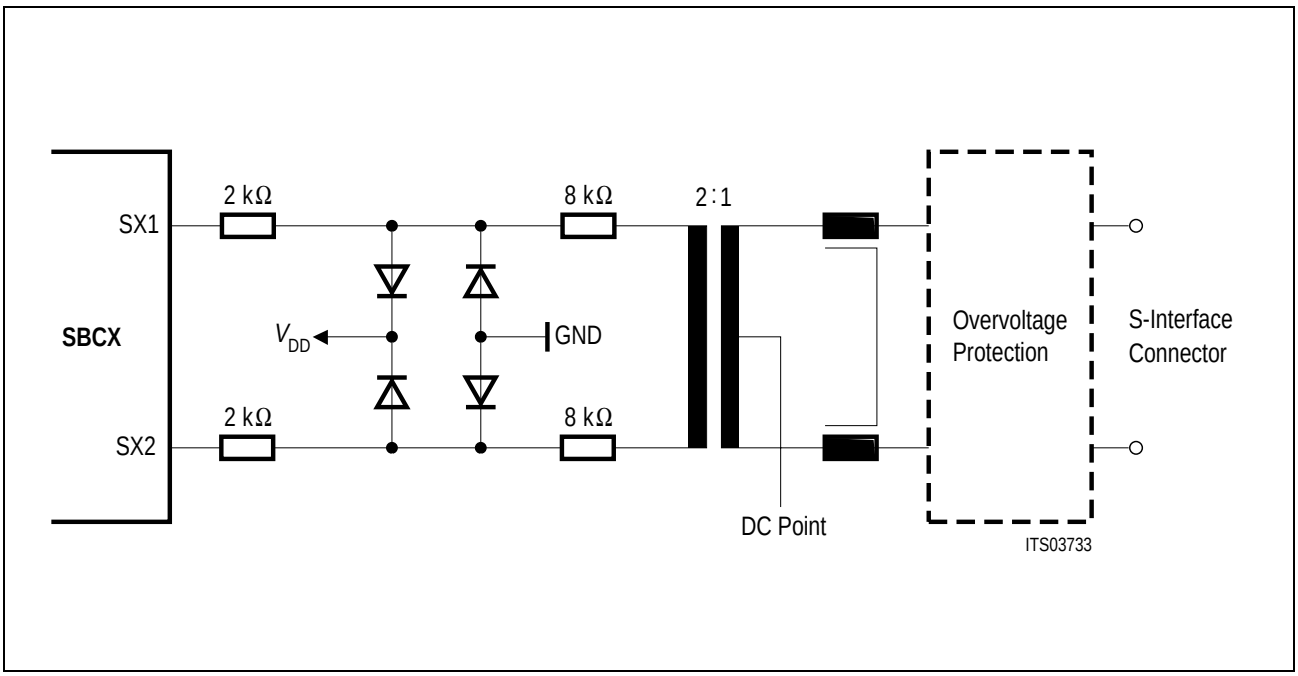


Figure 81
External Circuitry Receiver

4.8.3.1 S/T-Interface Transformer

The SBCX is connected to the S/T-interface by the use of a 2:1 transformer for the receiver and the transmitter respectively. The line side of the transformer should be centre tapped for the phantom power supply.

The model parameters of the transformer are defined below (all measurements at 10 kHz):

primary to secondary transformer ratio:	1:2 ± 1 %
primary total DC resistance:	$R \leq 10\ \Omega$
primary inductance:	L_M > 20 mH
primary inductance with secondary short circuited:	L_P < 20 µH
primary capacitance with secondary open:	C < 40 pF

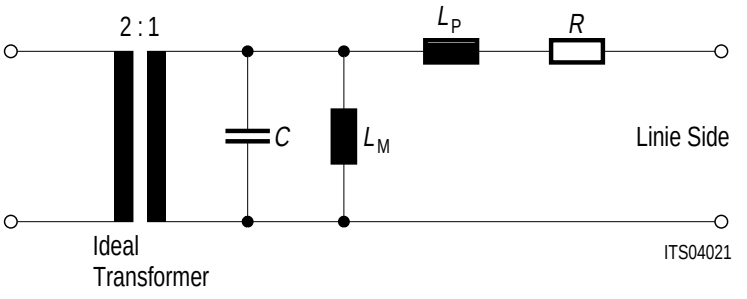


Figure 82
Transformer Model

4.8.3.2 Line Overload Protection (Transmitter, Receiver)

In order to protect the SBCX from over-current pins SX1, SX2 and SR1, SR2 are equipped with internal protection circuits. The following figures indicate what limits may not be exceeded to avoid permanent damage to the analog port.

These figures may be used to deduct requirements for external over voltage protection.

The maximum input current (under overvoltage conditions) is given as a function of the width of a rectangular input current pulse as outlined in the following figure.

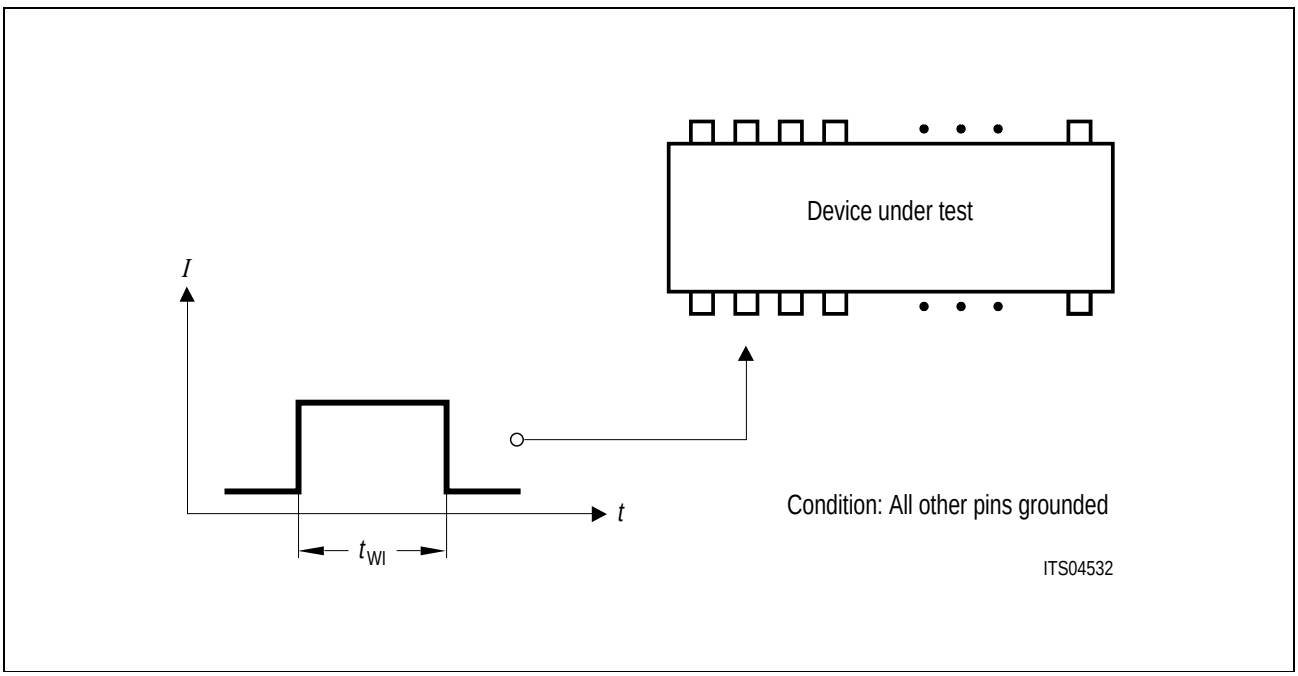


Figure 83
Test Condition for Maximum Input Current

4.8.4 Transmitter Input Current

The destruction limits for negative input signals ($R_i \geq 2\ \Omega$) and for positive input signals ($R_i \geq 200\ \Omega$) are given in the following figure.

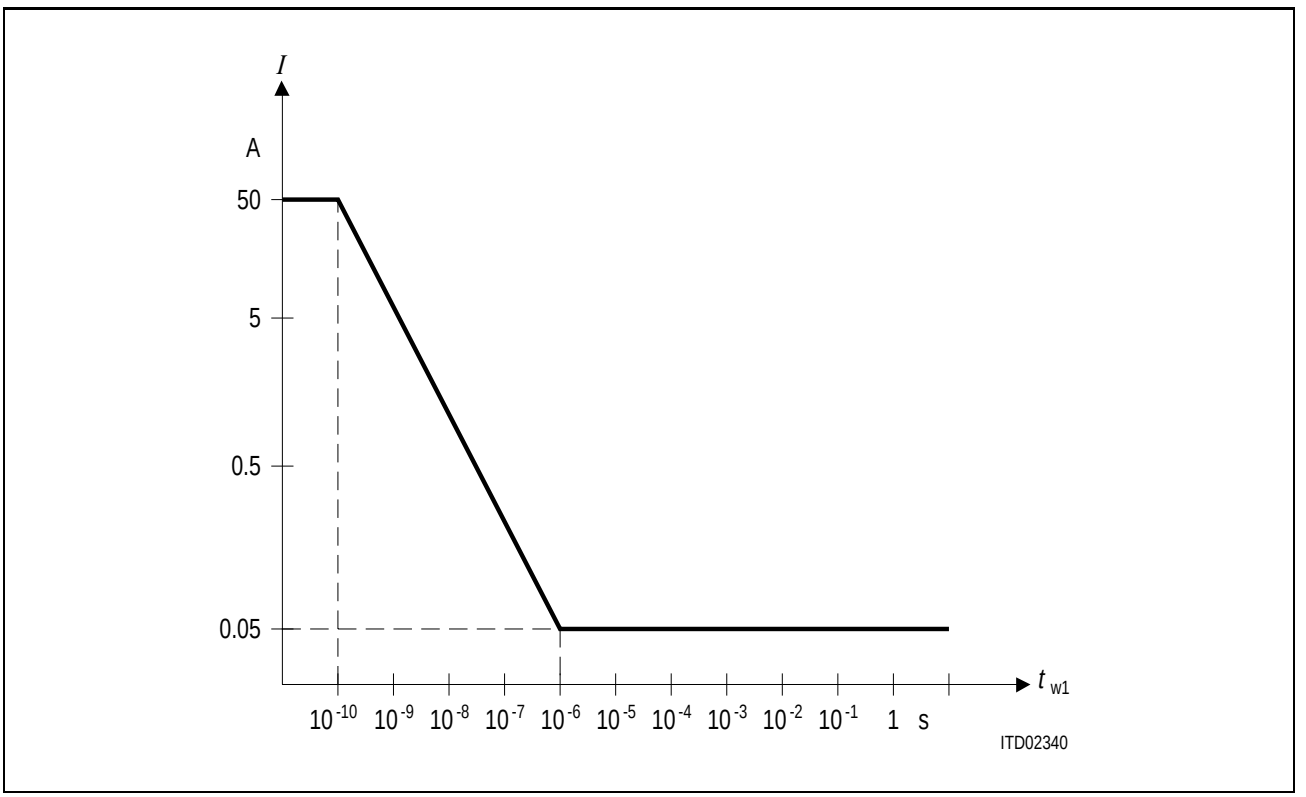


Figure 84
Destruction Limits Transmitter Input Current

4.8.5 Receiver Input Current

The destruction limits ($R_i \geq 300\ \Omega$) are given in the following figure.

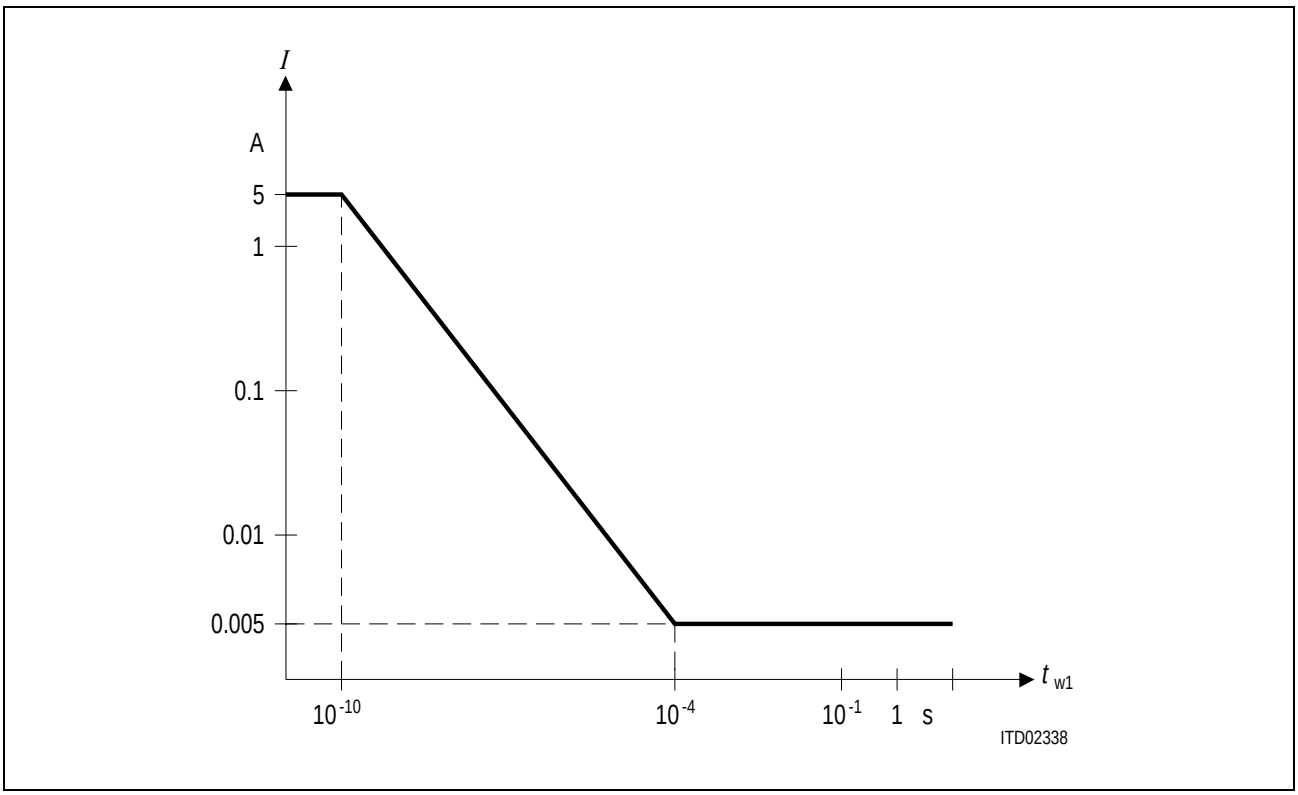


Figure 85
Destruction Limits Receiver Input Current

5 Electrical Characteristics

All characteristics given are valid under the following conditions unless otherwise indicated:
T_A = – 20 to 70 °C; V_{DD} = 5 V ± 5 %; V_{SS} = 0 V

5.1 Absolute Maximum Ratings

Ambient temperature under bias	– 20 to 70 °C
Storage temperature	– 65 to 125 °C
Voltage on any pin with respect to ground	– 0.4 to V_{DD} + 0.4 V
Power dissipation	1 W

Note:

Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Contact Resistance

	Silicon-Case R_{THK}	**Silicon-Environment R_{THU}**
P-DIP-28	29.6 K/W	49 K/W
P-LCC-28-R	11.5 K/W	60 K/W

5.2 Power Supply

V_{DD} = 5 V ± 0.25 V

The analog receiver part has a power supply rejection of better than – 40 dB up to 100 kHz as shown in the following figure. However, due to the digital oversampling technique the overall receiver characteristics exceed the given value beyond 200 kHz.

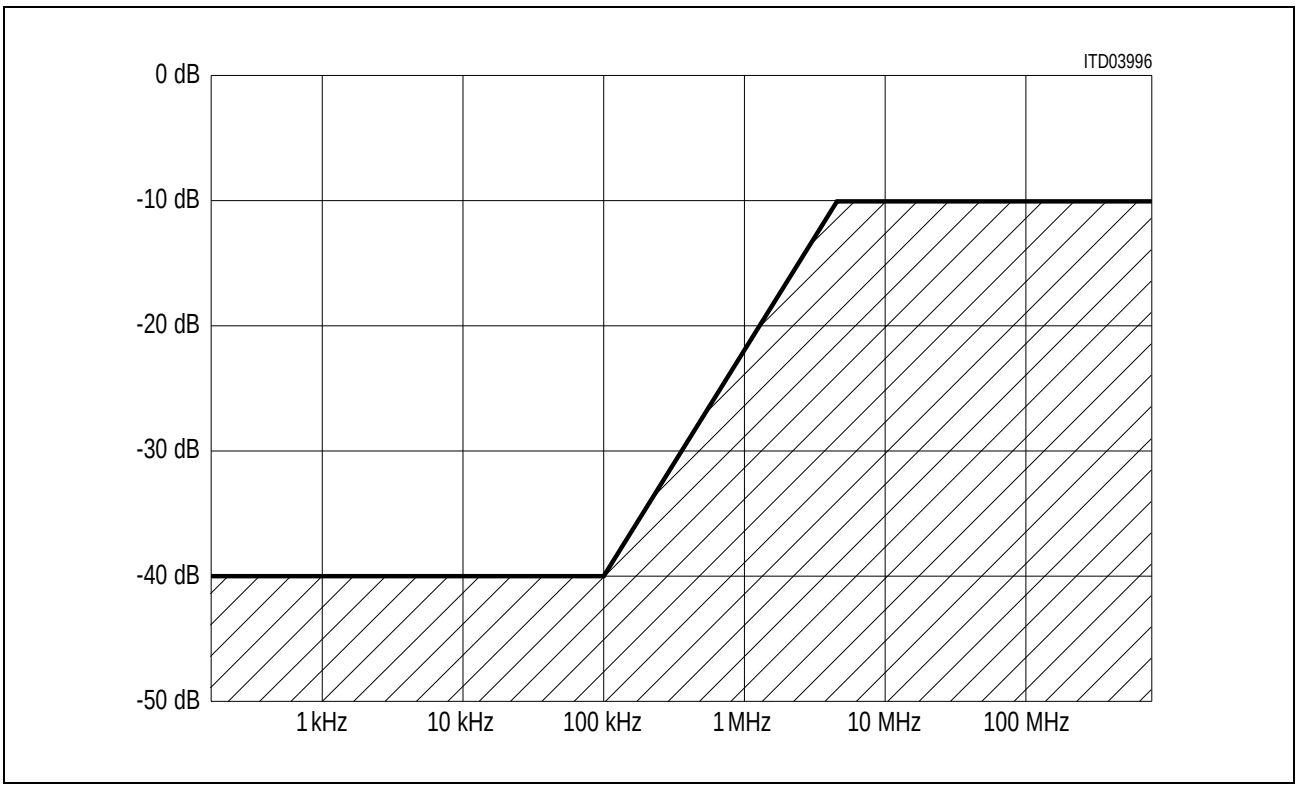


Figure 86
Power Supply Rejection SBCX Receiver

5.3 Capacitances

T_A = 25 °C; V_{DD} = 5 V ± 5 %; V_{SS} = 0 V; f_C = 1 MHz

Pin	Parameter	Symbol	Limit Values		Unit
			min.	max.	
All pins except SX1, 2	Pin capacitance	C_{IO}		7	pF
SX1, 2	Output capacitance against V_{SS}	C_{OUT}		10	pF
XTAL1, 2	External load capacitance	C_L		50	pF

5.4 DC Characteristics

Pin	Parameter	Symbol	Limit Values		Unit	Test Condition
			min.	max.		
All pins except SX1, 2; SR1, 2; XTAL1, 2	Input low voltage	V_{IL}	– 0.4	0.8	V	
	Input high voltage	V_{IH}	2.0	V_{DD} + 0.4	V	
	Output low voltage	V_{OL}		0.45	V	I_{OL} = 2 mA
IDP1, 0	Output low voltage	V_{OL1}		0.45	V	I_{OL} = 7 mA
All pins except SX1, 2; SR1, 2; XTAL1, 2	Output high voltage	V_{OH}	2.4		V	I_{OH} = – 400 µA
			V_{DD} – 0.5		V	I_{OH} = – 100 µA
	Input leakage current	I_{LI}		1	µA	0 V ≤ V_{IN} ≤ V_{DD}
	Output leakage current	I_{LO}		1	µA	0 V ≤ V_{OUT} ≤ V_{DD}
SX1, SX2	Absolute value of output pulse amplitude ($V_{SX2} - V_{SX1}$)	V_X	2.03 2.10	2.31 2.39	V V	R_L = 50 Ω[1)] R_L = 400 Ω[1)]
SX1, SX2	Transmitter output current	I_X	7.5	13.4	mA	R_L = 5.6 Ω[1)]
SX1, SX2	Transmitter output impedance	Z_X	10 0		kΩ Ω	inactive or during binary one (V_{DD} = 0 … 5 V) during binary zero R_L = 50 Ω
SR1, SR2	Receiver input impedance	Z_R	10 100		kΩ Ω	V_{DD} = 5 V V_{DD} = 0 V
XTAL1	Input high voltage	V_{IH}	3.5	V_{DD} + 0.4	V	
XTAL1	Input low voltage	V_{IL}	– 0.4	1.5	V	
XTAL2	Output high voltage	V_{OH}	4.5		V	I_{OH} = 5 µA, C ≤ 50 pF
XTAL2	Output low voltage	V_{OL}		0.4	V	I_{OH} = 5 µA, C ≤ 50 pF

Note:
1) Due to the transformers, the load resistance as seen by the circuit is four times R_L

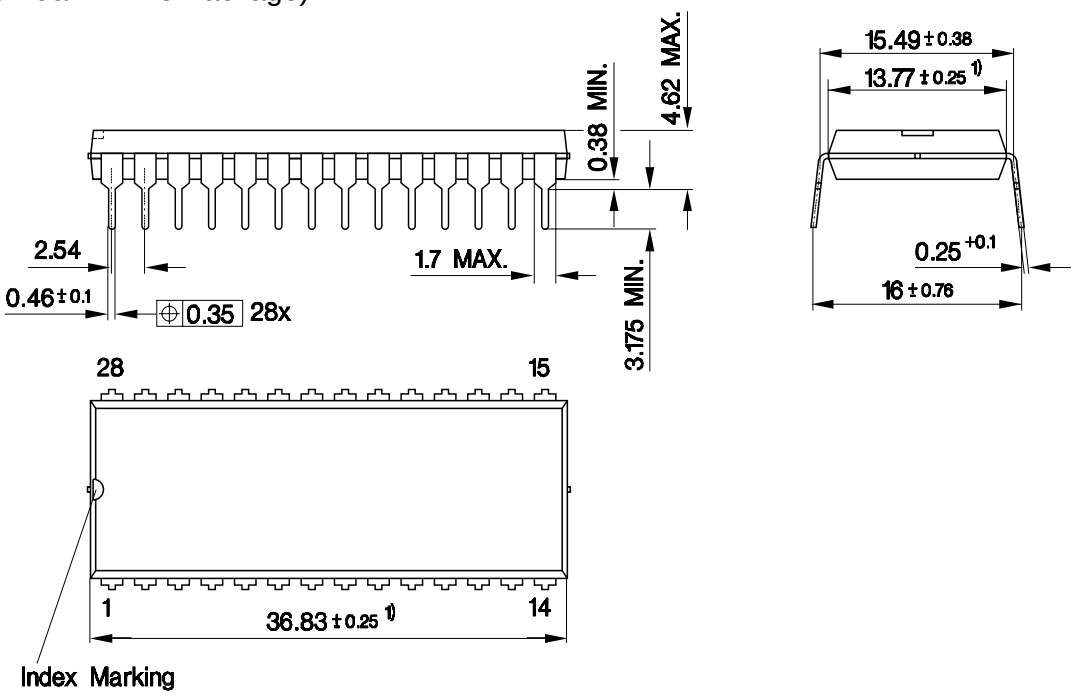
5.5 Power Consumption

Parameter	Limit Values			Comment
	min.	typ.	max.	
50 Ω chip load, inputs at V_{SS}/V_{DD}, 50 % bin. ZEROs in B1 and B2 channel			60 mW	Power-up
No output loads			4 mW	Power-down
0 Ω chip load and INFO2 transmitted			108 mW	Worst-case

Note: For power consumption under emergency conditions please refer to corresponding application note.

6 Package Outlines

P-DIP-28-3
(Plastic Dual In-Line Package)



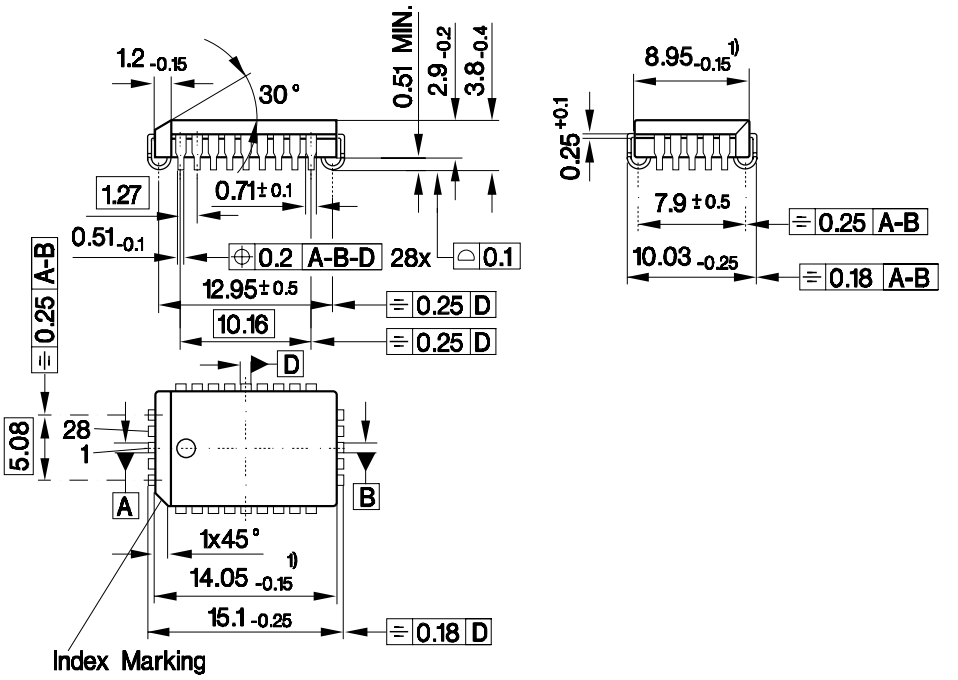
1) Does not include plastic or metal protrusion of 0.25 max. per side

GPD05590

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

Dimensions in mm

P-LCC-28-1
(Plastic Leaded Chip Carrier Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPL05018

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm

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7 Appendix

The appendix comprises three sections:

Appendix A contains a collection of Delta- and Errata Sheets published for the SBCX, PEB 2081. These allow the user to identify technical differences between the latest SBCX versions.

Appendix B summarizes the requirements of external components and gives addresses of recommended suppliers.

Appendix C is a Quick Reference Guide containing the most important information regarding the SBCX.

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Appendix A

7.1 Delta and Errata Sheets

SIEMENS

S/T Bus Interface Circuit Extended (SBCX)

PEB 2081

Delta Sheet **CMOS**

Differences between PEB 2081 Version 3.4 and Version 3.3

1. Programming the IOM®-2 channel register (address: 3_H) with the value xxxx x1xx (DH = 1) in the LT-T mode has no influence on the indication.
   The indication in the state “activated” is always 1100 (AI).
2. Enabling the far-end-code violation function (FECV) according to ANSI T1.605 (RCVE = 1 in configuration register; address = 1_H) the detection of at least one code violation within multiframe is indicated by the occurrence of six times the CI code 1011 (CVR).

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S/T Bus Interface Circuit Extended (SBCX)

PEB 2081

Errata Sheet for the Version 3.3 **CMOS**

1. Activation Indication

After programming the IOM-2 Channel Register (address: 3_H) with the value xxxx x1xx (DH = 1) in the LT-T Mode, the indication of the state “activated” may be 0100 (RSY) instead of 1100 (AI). Although the indication is wrong the device works correctly.

2. Illegal Code Violation Indication

After enabling the far-end code violation function (FECV) according to ANSI T1.605 (RCVE = 1 in configuration register; address: 1_H) the device indicates illegal code violation in the CI channel: 1011 (CVR). The indication, once occurred, will only disappear when leaving the activated state.

This function should not be programmed if using the versions 3.2 and 3.3.

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S/T Bus Interface Circuit Extended (SBCX)

PEB 2081

Errata Sheet for the Version 3.4 **CMOS**

1. Statemachine Toggling

Receiving INFOX in TE or LT-T mode the statemachine may toggle betweenstateF5/F8 and state F6 or between state F5/F8 and state F7. While toggling the device stays in F6 or F7 for one IOM frame only.

2. NT Star Operation

D-Channel handling in a star configuration (several SBCX in NT/LT-S mode, tied together at CEB and IOM) doesn't work properly. Corrupted D-channel data may be sent in DU direction on IOM.

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Appendix B

7.2 External Components Information

Transformers and Crystals Vendor List

Crystals:

Frischer Electronic
Schleifmühlstraße 2
D-91054 Erlangen, Germany

KVG
Waibstadter Straße 2-4
D-74924 Neckarbischofsheim 2, Germany
Tel.: (…7263) 648-0

NDK
2-21-1 Chome Nishihara Shibuya-Ku
Tokyo 151, Japan
Tel.: (03)-460-2111
or
Cupertino, CA, USA
Tel.: (408) 255-0831

Saronix
4010 Transport at San Antonio
Palo Alto, CA 94303, USA
Tel.: (415) 856-6900
or
via Arthur Behrens KG
Schrammelweg 3
D-82544 Egling-Neufahrn, Germany

Tele Quarz
Landstraße 13
D-74924 Neckarbischofsheim 2, Germany

Transformers:

Advanced Power Components (APC)
47 Riverside
Medway City Estate Strood
County of Kent, GB
Tel.: (044) 634-290 588

Pulse Engineering
P.O. Box 12235
San Diego, CA 92112, USA
Tel.: (619) 268-2454
or
4, avenue du Quebéc
F-91940 Les Ulis, France
or
Dunmore Road
Tuam County Galway, Ireland
Tel.: (093) 24107

S+M Components
Balanstraße 73
P.O. Box 801709
D-81617 Munich, Germany
Tel.: (…89) 4144-8041
Fax.: (…89) 4144-8483

Siemens Oostcamp
Belgium

Schott Corporation
Suite 108
1838 Elm Hill Pike, Nashville, TN 37210, USA
Tel.: (615) 889-8800

TDK
Christinenstraße 25
D-40880 Ratingen 1, Germany
Tel.: (…2192) 487-0

Universal Microelectronics

Vacuumschmelze (VAC)
Grüner Weg 37
Postfach 2253
D-63412 Hanau 1, Germany
Tel.: (…6181) 380
or
186 Wood Avenue South
Iselin, NJ OB830, USA
Tel.: (908) 603 5905

Valor
Steinstraße 68
D-81667 München, Germany
Tel.: (…89) 480 2823
Fax.: (…89) 484 743

Vogt electronic AG
Postfach 1001
D-94128 Obernzell, Germany
Tel.: (…8591) 17-0
Fax.: (…8591) 17-240

List of Transformer Manufacturers and S_0 Transformers

The following list contains transformers recommended by different manufacturers for use with Siemens S_0 transceivers.

Transformers marked with [1)] have been tested in Siemens S evaluation boards and have shown positive test results concerning pulse shape and impedance requirements of ETS 300 012.

This list is not completed, there may be other manufacturers as well as more types fitting to the SBCX.

Manufacturers	Transformers
APC	
	APC 2040 S
	APC 1020 S
	APC 3060 S
	APC 9018 D
	APC 3366 D
Pulse Engineering	
	PE-68975[1)]
	PE-64995
	PE-65495
	PE-65795
	PE-68995
S + M Components	
	B78384-A1060-A2[1)]
	B78384-P1111-A2
Vacuumschmelze VAC	
	T60403-L4025-X021[1)]
	T60403-L4097-X011[1)]
	T60403-L5051-X006[1)]
	T60403-L4021-X066
	T60403-L4025-X095
	T60403-L4097-X029
	T60403-L5032-X002
VALOR	
	PT 5001
	PT 5069
	ST 5069
VOGT	
	543 21 002 00[1)]
	543 21 004 00[1)]

SIEMENS

Appendix C

7.3 Quick Reference Guide

Modes of Operation

Configuration	LT-S Point-Point/Bus	NT Point-Point/Bus	LT-T	TE

Pin

Mode	1	0	1	0
X0	i:TS0	i:0/i:1 [1]	i:TS0	o:32/16kHz (1:1)
X1	i:TS1	i:0	i:TS1	i:0
X2	i:TS2	i:1	i:TS2	i:0
X3	i/o:CEB	i/o:CEB	o:1536kHz (3:2)	o:768kHz (1:1)
MAI0	i:$\overline{\text{NT-STAR}}$	i:$\overline{\text{NT-STAR}}$	i:MPR0	i:MPR0
MAI1	i:MPR1	i:MFD	i:CON[2]	i:CON[3]
MAI2	i:MPR2	i:$\overline{\text{TM1}}$	i:MPR2	i:MPR2
MAI3	i:MPR3	i:$\overline{\text{TM2}}$	i:MPR3	i:MPR3
MAI4	o:MPR4	o:MPR4	o:MPR4	o:MPR4
MAI5	o:MPR5	o:MPR5	o:S/G	o:S/G if SGE = 1
MAI6	o:MPR6	o:MPR6	o:MPR6	o:MPR6
MAI7	o:MPR7	o:MPR7	o:MPR7	o:MPR7
FSC	i:8kHz	i:8kHz	i:8kHz	o:8kHz (1:2)
DCL	i:512-8192kHz	i:512-8192kHz	i:512-8192kHz	i:1536kHz (1:1)

(cont'd)

i: input
o: output

i: 0 input fixed to V_{SS}
i: 1 input fixed to V_{DD}

Note:

1) Choice for bus configuration (1 = bus). In LT-S mode only programmable. In NT mode programmable or pin strapping. Pin strapping has the higher priority.

2) CON-pin functionality is enabled if DH = "1" in the IOM-2 Channel register in LT-T mode.

3) CON-pin functionality is enabled if DH = "0" in the IOM-2 Channel register in TE mode.

Modes of Operation (cont'd)

Configuration	LT-S Point-Point/Bus	NT Point-Point/Bus	LT-T	TE
Register				
Configuration Bit 0 (Mode) [0]	0	0/1[7]	1	0/1[7]
Configuration Bit 1 (C/W/P) [0]	0/1[1]	0/1[1]	0/1[2]	0/1[3]
Configuration Bit 5 (FSMM) [0]	0/1	0/1	0	0
Configuration Bit 6 (MAIM) [0]	0	0	0	0
SM/CI Bit 0 (MIO) [0]	0	0	0	0
SM/CI Bit 2 (SGE) [0]	0	0	0	0/1[8]
IOM-2 Channel Bit 2 (DH) [0]	0/1[5]	0/1[5]	0/1[6]	0/1[7]

Notes:
1) Choice for bus configuration (1 = bus). In LT-S Mode only programmable. In NT mode programmable or pin strapping. Pin strapping has the higher priority.
2) Slip warning control. C/W/P = 0 will issue C/I "Slip" code warning after 50 µs wander. C/W/P = 1 will issue the "Slip" code warning after 25 µs.
3) PCK (pin X0) frequency select. C/W/P = 0 will issue a power converter clock frequency of 32 kHz, C/W/P = 1 will issue 16 kHz.
4) Select "1" for intelligent NT applications to ensure partial TIC Bus evaluation (**see section 3.3.5.5)**.
5) Select "1" for point-to-multipoint configurations to ensure D-channel collision resolution according to ITU I.430 (**see section 2.1.7 and 3.3.5.4**).
6) For normal D-channel collision procedure program DH = "0".
7) 0: MAI pins I/O specific; 1: MAI pins only I/O.
8) In TE Mode pin MAI5 outputs a D-channel enable signal, which may be used by a general purpose HDLC controller for LAP D handling. The signal contiuously monitors the D-E channel status and provides a stop/go information.

[0] Initial register bit value after hard- or software reset.

MON-8 Configuration Register – (Read/Write, Address: 1_H)

Format:	MFD	MAIM	FSMM	LP	SQM	RCVE	C/W/P	MODE

Initial Value: 00_H

Bit-name	Description
MODE	Pin MODE = V_{DD} (LT-S, LT-T): 0: LT-S mode selected 1: LT-T mode selected
C/W/P	LT-S and NT mode: Configuration 0: point-to-point or extended passive bus configuration (adaptive timing recovery). In NT mode the pin X0 (= BUS) must be low. 1: short passive bus configuration (fixed timing recovery) in LT-T mode: Wander detection (warning in C/I, data may be lost!) 0: "SLIP" after 50 µs wander 1: "SLIP" after 25 µs wander in TE mode: Power converter clock frequency supplied at pin X0 0: 32 kHz 1: 16 kHz
SQM	SQ channel handling mode selection 0: non-auto mode only S1 and Q channels 1: transparent mode S1, S2 and Q channels
RCVE	0: normal operation 1: Far-end-code-violation (FECV) function according to ANSI T1.605 implemented.
LP	NT/LT-S mode: 0: transparent analog loop 1: non-transparent analog loop TE / LT-T mode: 0: non-transparent analog loop 1: external transparent loop
FSMM	NT/LT-S mode: 0: normal operation 1: Finite state machine interchanged (LT-S ↔ NT)
MAIM	MAI pins mode: 0: I/O-specific or standard I/O MAI interface 1: µP interface mode for MAI interface
MFD	Multi-frame disable (write): 0: All multi-frame functions active. In NT mode the pin MAI1 (= MFD) must be low. 1: Multi-frame generation (NT, LT-S) or synchronization (TE, LT-T) prohibited. No SQ monitor messages released. Multi-frame detected (read): 0: No multi-frame synchronization achieved. 1: Multi-frame synchronization achieved.

MON-8 Loop-Back Register – (Read/Write, Address: 2_H)

Format:	AST	SB1	SB2	SC	IB1	IB2	1	IB12

Initial value: 02_H

Bit-name	Description
AST	ASynchronous Timing In NT and LT-S mode; only NT state machine 0: LT-S: command TIM in C/I NT: asynchronous wake up 1: LT-S: asynchronous wake up (useful for the Intelligent NT) NT: command TIM in C/I
SB1	Loop-back B1 channel at S/T-interface in NT/LT-S mode
SB2	Loop-back B2 channel at S/T-interface in NT/LT-S mode
SC	Loop-back complete (2B + D) at S/T-interface in NT/LT-S mode
IB1	Loop-back B1 channel at IOM-2 interface
IB2	Loop-back B2 channel at IOM-2 interface
IB12	Loop-back B1 into B2 channel and vice versa at IOM-2 interface. Additionally IB1 and/or IB2 must be set.

MON-8 IOM®-2-Channel Register - (Read/Write, Address: 3_H)

Format:	B1L	B1D	B2L	B2D	DL	DH	CIL	CIH

Initial value: 00_H

Bit-name	Description
B1L	B1 channel location 0: normal [1] 1: B1 channel in IOM-2 channel 0
B2L	B2 channel location 0: normal [1] 1: B2 channel in IOM-2 channel 0
DL	D-channel location 0: normal [1] 1: D-channel in IOM-2 channel 0
CIL	CI channel location 0: normal [1] 1: in IOM-2 channel 0
B1D	B1 channel direction 0: normal (IDP0 is data output, IDP1 is data input) 1: IDP0 and IDP1 interchanged for B1 channel
B2D	B2 channel direction 0: normal (IDP0 is data output, IDP1 is data input) 1: IDP0 and IDP1 interchanged for B2 channel
DH	D-channel handling 0: LT-S, LT-T and NT mode: transparent TE mode: Collision detection according to ITU I.430 1: NT and LT-S mode: D-channel access control TE mode: transparent D-channel LT-T mode: D-channel collision resolution according to ITU I.430
CIH	CI channel handling 0: normal C/I access in the pin strapped IOM-2 channel 1: disabled, access to C/I is only possible via the SM/CI register

Notes:

[1] In LT-S and LT-T mode: pin strapped IOM-2 channel
In NT and TE mode: IOM-2 channel 0

MON-8 SM/CI Register – (Read/Write, Address: 4_H)

Format:	CI3	CI2	CI1	CI0	TOD	SGE	0	MIO

Initial value: CI, 0_H

Bit-name	Description
CI (3:0)	CI channel When CIH-bit is set to one the commands are input in the monitor channel CI (3:0). The indication can always be read via monitor channel CI (3:0).
TOD	Time-Out Disable 0: monitor timeout (minimum 5 ms) enabled 1: monitor timeout disabled
SGE	Stop / Go Enable 0: normal 1: In TE mode pin MAI5 outputs S/G
MIO	Maintenance Input Output (MAIM = 0) 0: I/O-specific functions on MAI interface 1: Standard I/O functions on MAI interface

MON-8 MAI Pin Register - (Read/Write, Address: 5_H)

Format:	MPR7	MPR6	MPR5	MPR4	MPR3	MPR2	MPR1	MPR0

Initial value: 00_H

Bit-name	Description
MPR (7:0)	access to MAI(7:0) pins if MAI interface in standard I/O or I/O specific function mode

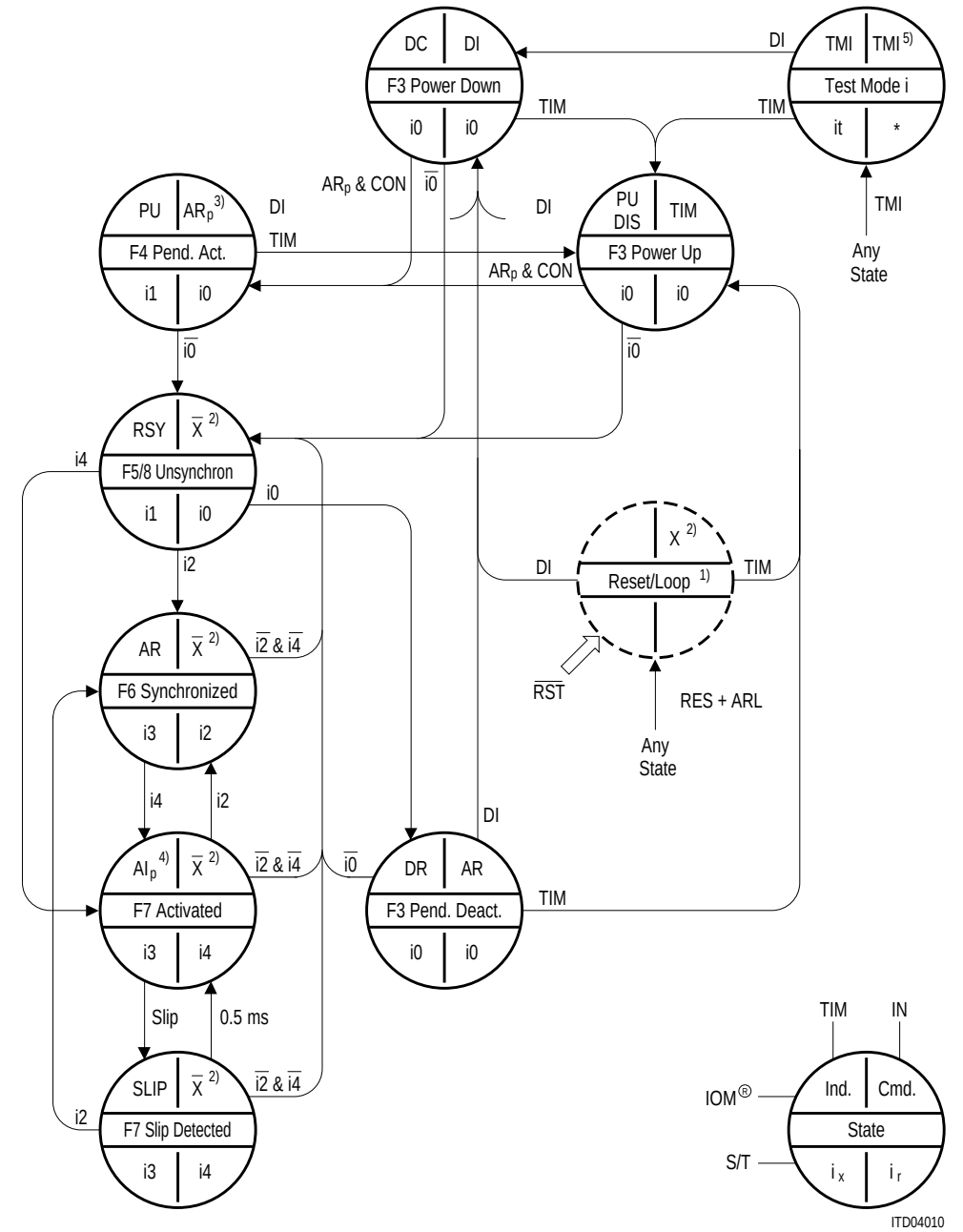
In case the µP interface was selected as the MAI interface mode (MAIM = 1) the MAI pin register is defined as follows (only “write to register” operation will be accepted).

Format:	$\overline{WR}$	$\overline{RD}$	A1	A0	$\overline{INT}$	D2	D1	D0

(write only)

Bit-name	Description
D0 … D2 (MAI0:2)	Data pin (input/output)
$\overline{INT}$ (MAI3)	Interrupt (input), Read request control: 0: Single Address read operation 1: Complete Address (0 … 3) read operation
A0 … A1 (MAI4:5)	Address pins (output)
$\overline{RD}$ (MAI6)	Read signal (output) 0: Read operation 1: Write operation (if $\overline{WR}$ = 0)
$\overline{WR}$ (MAI7)	Write Signal (output) 0: Write operation 1: Read operation (if $\overline{RD}$ = 0)

TE/LT-T Modes State Diagram

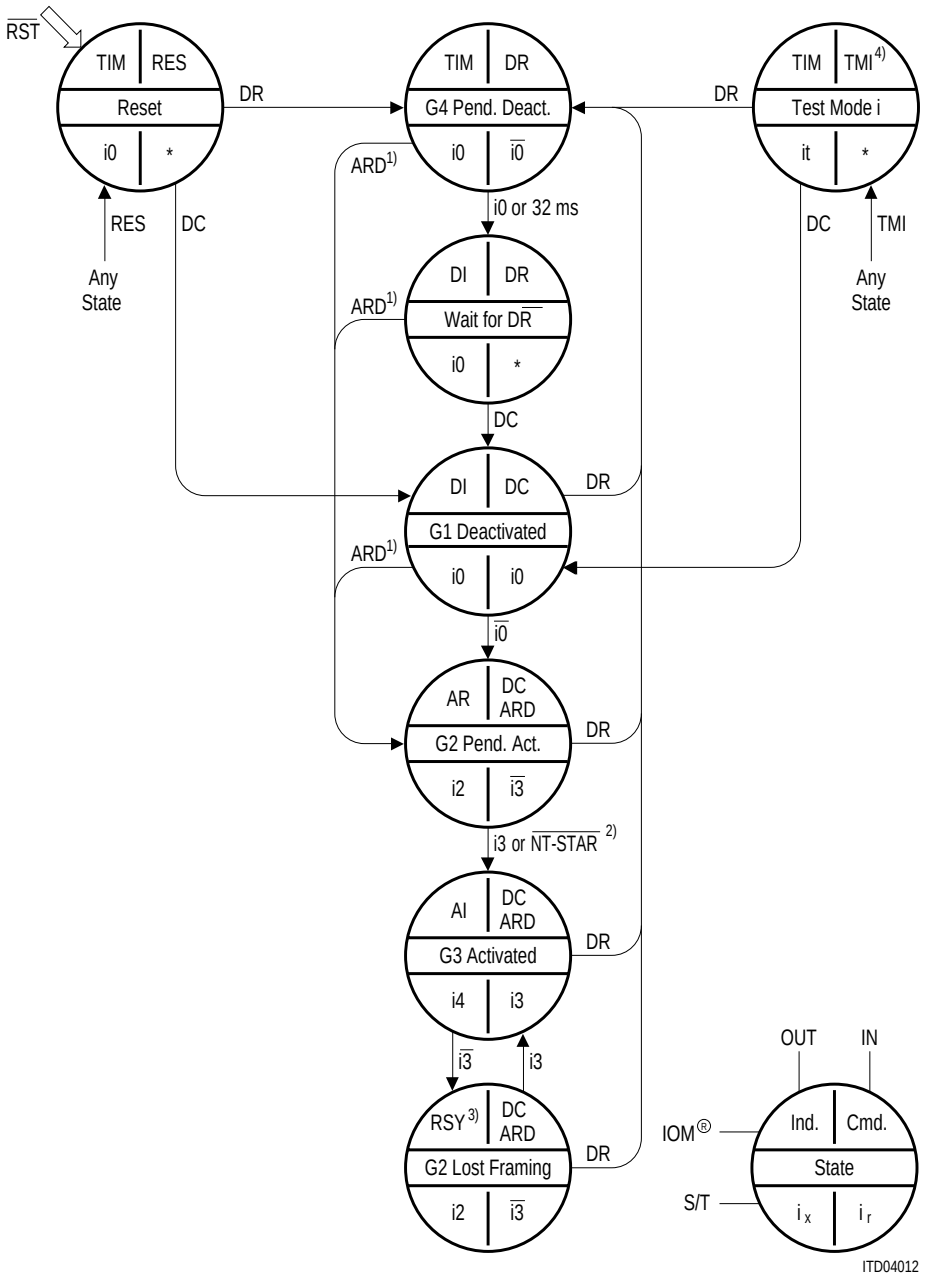


Notes:

1. See state diagram for unconditional transitions for details
2. x = TM1 or TM 2 or RES or ARL
   $\overline{x}$ = $\overline{TM1}$ & $\overline{TM2}$ & $\overline{RES}$ & $\overline{ARL}$
3. AR_P = AR8 or AR10
4. AI_P = AI8 or AI10
5. TMI = TM1 or TM2

Figure 87
State Transition Diagram in TE/LT-T Modes

LT-S Mode State Diagram

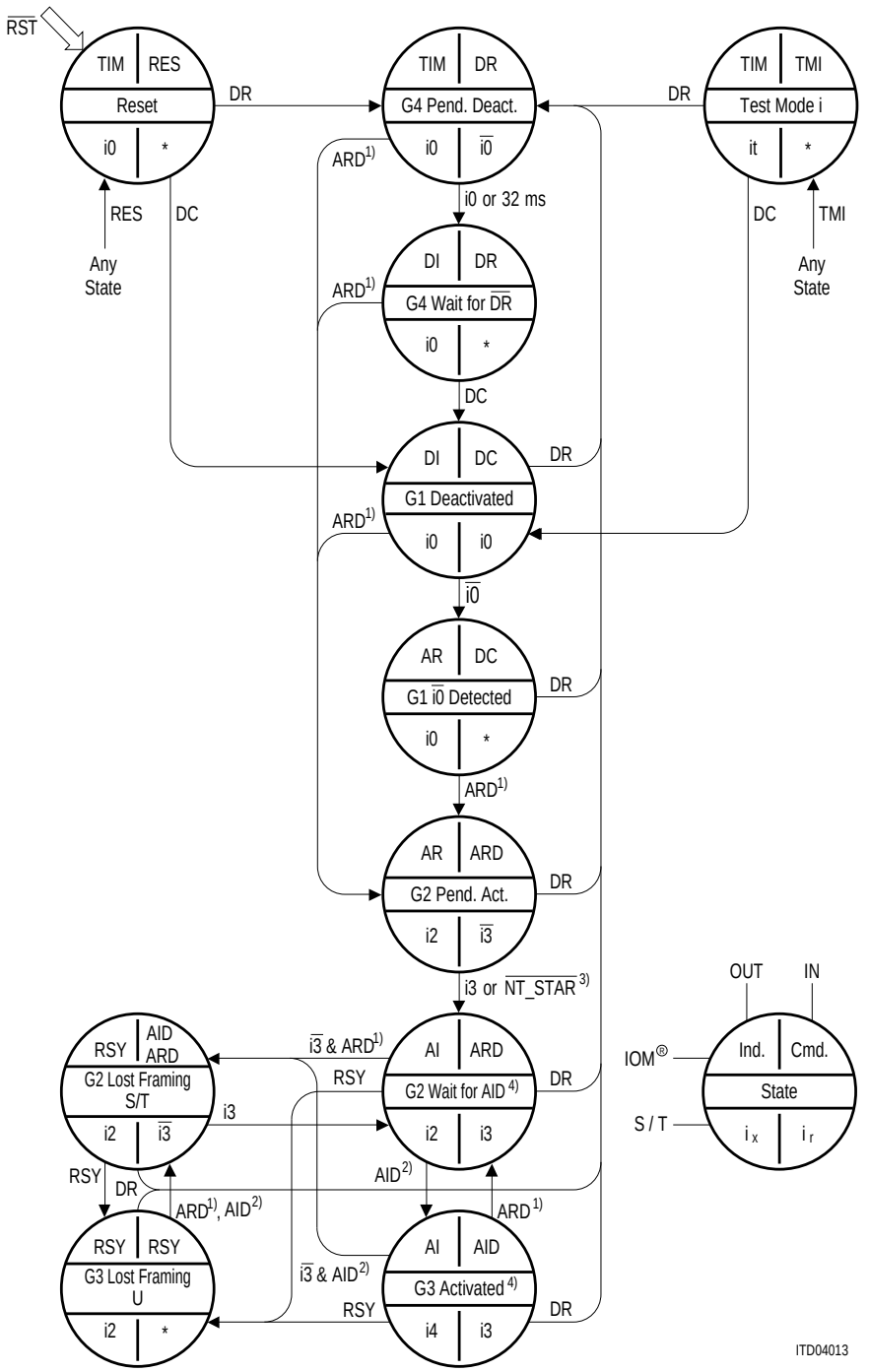


Notes:

1. ARD stands for AR or ARL
2. NT star: transition from ‘G2 pend. act.’ to ‘G3 activated’ takes place when the first branch of the star is synchronized
3. NT star: transition from state ‘G3 activated’ to ‘G2 Lost framing’ is disabled.
4. TMI = TM1 or TM2

Figure 88
State Diagram of the LT-S Mode

NT Mode State Diagram



Notes:

1. ARD = AR or ARL
2. AID = AI or AIL
3. Transition takes place as soon as one branch of the star has detected INFO
4. With $\overline{\text{NT-STAR}}$ selected transfer to “G2 lost framing” state is not possible

Figure 89
NT Mode State Diagram

C/I Codes

Code	LT-S		NT		TE/LT-T	
	IN	**OUT**	**IN**	**OUT**	**IN**	**OUT**
0 0 0 0	DR	TIM	DR	TIM	TIM	DR
0 0 0 1	RES	–	RES	–	RES	RES
0 0 1 0	TM1	–	TM1	–	TM1	TM1
0 0 1 1	TM2	–	TM2	–	TM2	TM2 SLIP[1)]
0 1 0 0	–	RSY	RSY	RSY	–	RSY
0 1 0 1	–	MAIC	–	MAIC	–	MAIC/DIS
0 1 1 0	–	–	–	–	–	–
0 1 1 1	–	–	–	–	–	PU
1 0 0 0	AR	AR	AR	AR	AR8	AR
1 0 0 1	–	–	–	–	AR10	–
1 0 1 0	ARL	–	ARL	–	ARL	ARL
1 0 1 1	–	CVR	–	CVR	–	CVR
1 1 0 0	–	AI	AI	AI	–	AI8
1 1 0 1	–	–	–	–	–	AI10
1 1 1 0	–	–	AIL	–	–	AIL
1 1 1 1	DC	DI	DC	DI	DI	DC

1) In LT-T mode only