VITESSE SEMICONDUCTOR CORPORATION

IQ2000™

VSC2100
Network Processor

DESCRIPTION

The VSC2100 IQ2000, a member of Vitesse's family of intelligent packet processors, is designed to provide flexible, programmable high performance packet processing at up to OC-48 data rates for Layer 3/Layer 4 Routing Switches and other demanding packet processing applications.

Tasks for which the IQ2000 is particularly suitable include: complex multi-protocol routing algorithms, information classification and management (audio and video streams), filtering/firewall functions, security filters, and class of service based on application or policies. The IQ2000 also facilitates the collection of application-level as well as RMON traffic statistics on a per port basis to provide enhanced troubleshooting of network problems and more-detailed accounting of network usage.

FEATURES

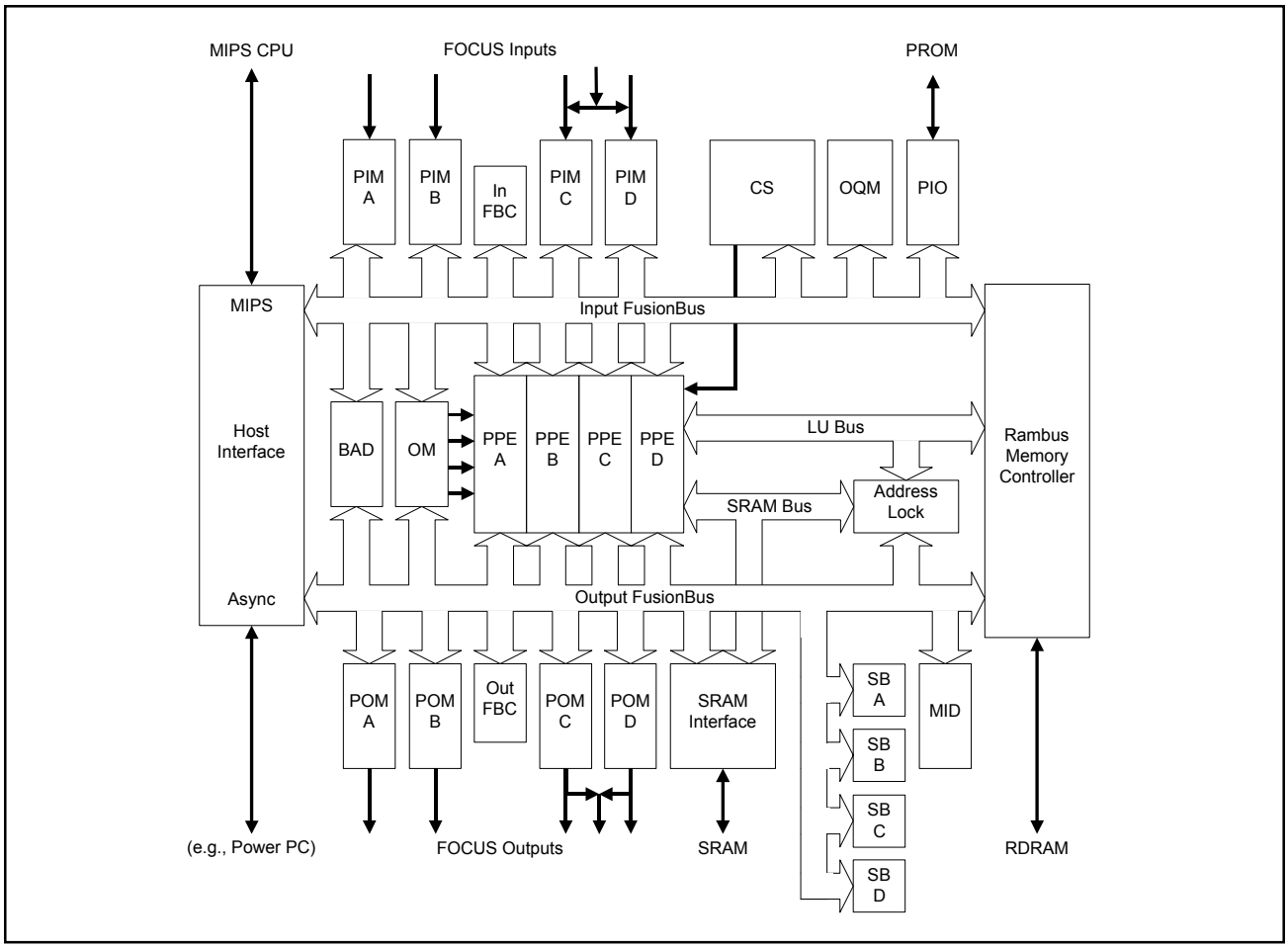
The following features make the IQ2000 the ideal choice as the key building block in powerful packet handling systems, especially Networking and Communications applications that require complex packet operations at high data bandwidth:

- **Four 200 MHz RISC CPU packet processing engines**
- **Powerful packet management system**
- **32/64-bit interface to external MIPS CPU**
- **Alternative 32-bit asynchronous host interface**
- **12.8-Gbps Direct RamBus Memory Controller**
- **Two internal GigaMAC Ethernet connections**
- **Up to four 16-bit/one 32-bit FOCUS peripheral interconnection buses:**
  - support a variety of peripheral and switching fabric connections
  - support full-duplex speeds up to 1.6Gbps/3.2Gbps per 16-bit/32-bit bus
- **Hardware support for Multicast**
- **Component of Vitesse IQ2000 Family of Network Processors**
- **Supports multiple protocols and network interfaces:**
  - Gigabit Ethernet, 10/100 Ethernet, high performance optical interfaces up to OC-48
  - broad array of legacy and low/medium speed WAN interfaces such as FDDI, Token Ring, T1 and T3
- **Up to eight queues per output channel, or 64 queues on one channel in Single-Port Mode**
- **Support for Quality of Service (QoS) algorithms:**
  - Weighted Fair Queuing (WFQ)
  - Rate Limiting Queues
  - (Weighted) Random Early Discard (WRED and RED per Differentiated Services - DiffServ - recommendation)
- **Comprehensive development tools**
  - evaluation platforms
  - design and debug tools for embedded RISC processor and VxWorks MIPS development environments

G52385-0, Rev 4.1 12/14/01

IQ2000 Block Diagram

The IQ2000 consists of several hardware Modules connected via two separate segments of FusionBus, Vitesse's proprietary 12.8 Gbps on-chip interconnection fabric. The internal structure of the IQ2000 is shown below.



VSC2100 Block Diagram

Architecture

The modules of the IQ2000 can be divided into three categories:

Data Flow Modules

- FOCUS Interfaces
- Packet Input Modules (PIM)
- Packet Output Modules (POM)
- Gigabit MACs (GMAC)
- Smart Buffer Modules (SB)
- Buffer Allocator/Deallocator (BAD)
- Multicast ID Manager (MID)

Packet Processing Modules

- Four Programmable 200-MHz internal FACET RISC CPUs
- Lookup co-processors
- DMA co-processors
- Local data and header buffer storage
- Instruction Control Store (CS)
- Order Manager (preserves packet ordering) (OM) in conjunction with the Overflow Queue Module (OQM)
- Lock Address Block

System Modules

- Host Interface
- Direct RamBus Memory Controller (MEMC)
- Static RAM Controller (SRAM)
- PROM I/O Controller (PIO)
- FusionBus Controllers (FBC)

The following section provides a functional overview description of each of the IQ2000 modules.

Data Flow Modules

FOCUS Interfaces

Each of the IQ2000's four FOCUS16 interfaces is a point-to-point interface used to transfer data very efficiently between the IQ2000's Packet Input and Output Modules (PIM and POM) and a peripheral-interface chip or network fabric chip. Additionally, the FOCUS16 interfaces of two IQ2000s can be connected to cascade the processing power of the IQ2000s. FOCUS16 is simple and flexible enough to support both the needs of Vitesse's family of network processors and to support customer-unique connections. The FOCUS16 interface is very pin-efficient, utilizing two unidirectional 16-bit buses per peripheral chip connection. Each FOCUS16 bus uses a separate clock and a Ready/Request line for a total of 18 signals per bus or 36 signals for a full FOCUS16 interface.

These buses can also run in a 32-bit mode. A Pair of FOCUS16 interfaces (named FOCUSC and FOCUSD) may be combined to form a single FOCUS32 connection. Four FOCUS16 interfaces can run simultaneously in 16-bit mode, or one pair in 32-bit mode and two in 16-bit mode. Each FOCUS32 bus also uses a separate clock and a Ready/Request line for a total of 34 signals per bus or 68 signals for the full FOCUS32 interface. Clock rates up to 100 MHz are supported, giving a peak bandwidth of 3.2 Gbps in each direction for FOCUS32. Lower clock rates can be used to support FPGA-based customer-unique solutions. FOCUS16 supports in-band access to all statistics and peripheral-chip command/status registers. This avoids the need for a secondary processor or any kind of sideband control interface.

For transfer across the FOCUS16 interface, packets and other data streams are divided into data groups called FOCUS16 Cells (FCells). Each FCell is from 1 to 128 bytes long. For example, a 278-byte packet could be broken up into two 128-byte FCells and one 22-byte FCell. Each packet is divided into a first FCell, some number of middle FCells, and a last FCell. Short packets may not contain any middle FCells, and very short packets may fit entirely within a single FCell. The first FCell typically included the complete packet header, or headers. FOCUS32 is similar, except that the maximum FCell size is 256 bytes.

FOCUS16 supports up to eight independent data streams (channels) in each direction. In addition, commands and status are transmitted over a ninth (auxiliary) channel in each direction. Each FCell has a two-byte header in FOCUS16 (or a four-byte header in FOCUS32) added that specifies the channel

number and the FCell size as well as flags for start and end-of-packet and abort signaling. FCells from different channels can be transferred over the FOCUS16 interface in any order. The receiving IQ2000 or FOCUS16-based peripheral chip sorts out the intermixed FCell traffic and re-constructs the original packets.

Each unidirectional data bus has a single Ready/Request line in the opposite direction to the data flow. The Ready/Request line can be configured either as a simple interface Ready line or as a serially encoded next-FCell Request line. When configured as a Ready line, all data transfers over the bus are held up until the Ready line is active. When configured as a serial FCell Request line, each channel sends out asynchronous serially encoded next-FCell requests. This allows the transmitting IQ2000 to send FCells for any of up to nine "ready" channels in whatever sequence is most convenient (first available, highest priority, etc.).

Packet Input Module (PIM)

The IQ2000 includes a Packet Input Module (PIM) for each FOCUS16 Interface. Each PIM manages the transfer of data from the FOCUS16 Interface to other IQ2000 modules over the FusionBus. The FCell data is stored in a dual-port RAM (FCell buffer) that holds 512 bytes. The RAM is divided into four sections of 128 bytes each, which are loaded and unloaded simultaneously in an alternating fashion. PIMs parse each FOCUS16 FCell header to determine the FCell port, length, start and end of packet and error state. This information is used to reconstruct the FCells into packets, queue the packets to the Order Manager (OM) for processing, and to keep track of the current state of all of the input channels of the FOCUS16 Interface.

Each PIM includes a classification accelerator that parses the first FCell of every packet and supplies Ethernet and IP information in a form which is easy for FACET to use.

Packet Output Module (POM)

The IQ2000 includes a Packet Output Module (POM), for each FOCUS16 interface. Each POM manages the transfer of data from internal IQ2000 modules to devices on its FOCUS16 Bus. POM manages up to eight queues for each of the eight FOCUS16 output data channels and one auxiliary channel. The major function of the POM is to select the next FOCUS16 FCell to be sent from among the various queues. POM transfers packets from the IQ2000 to devices connected to the FOCUS16 Bus as a sequence of FOCUS16 Cells (FCells). These are defined by a structure called an Output Header Descriptor (OHD), which is accessed through the IQ2000 Smart Buffer (SB) Module. The OHD consists of two sections: an Output Descriptor that describes the packet, and the header data that is the first segment of the packet. Small packets may be completely held in the header data of the OHD. Larger packets have additional data beyond the header, known as the payload. The payload is held in a data buffer in main memory. The Output Descriptor contains the location of the payload, and other information about the packet. One of the key POM functions is merging the header and payload into a single packet and transferring the packet to a peripheral device as a series of FCells over the FOCUS16 Bus.

For peripherals that require higher queuing capability, the POM provides Single-Port Mode in which all 64 queues are mapped to Port 0. However, in this mode the POM operation is reduced to that single data channel and the auxiliary channel.

The POM's dynamic output queue reprioritization scheme, time-based per-channel byte-counting, and queue byte counts provide the flexibility to support powerful Quality of Service (QoS) algorithms including Weighted Fair Queuing (WFQ), Rate Limiting Queues, and (Weighted) Random Early Discard (WRED and RED per Differentiated Services - DiffServ - recommendation).

Each output channel is dynamically prioritized by a vector that orders the priority of the eight queues that feed the output channel. Software manipulation of this vector enables all manner of complex QoS behaviors.

Each output channel's packet is provided by its 12-bit queue semaphore. When an OHD is written to one of the output queues in the Smart Buffer corresponding to an output queue in the POM, the corresponding queue semaphore is incremented. When the POM transfers a packet from an output queue, the corresponding semaphore is decremented. Thus a non-zero semaphore indicates that there is at least one packet in the output queue.

A critical piece of information for a variety of QoS algorithms is the amount of data that is currently held on an output queue. POM maintains this for each output queue in a queue counter. This counter is increased whenever an OHD is written to the corresponding queue in the Smart Buffer, and decreased whenever POM fetches an OHD for this queue. The counter value is used to assist in functions such as Per Flow Queuing, Bandwidth Allocation, and the Drop Preference function.

Buffer Allocation/De-allocation Module

The Buffer Allocation/De-allocation module (BAD) manages a set of eight pools of data buffers in main memory, which are used to store the payload part of data packets. Each of the eight pools is a contiguous block of main memory assigned by software at initialization. BAD manages a set of pointers, one to each data buffer, known as data buffer pointers (DBPs). Any IQ2000 module that requires access to one or more data buffers, such as the MIPS Host Interface, or the PIM, will perform a read from BAD across the Input FusionBus, which will supply the requested number of DBPs (the allocation process). When a module such as the POM has completed operation on a data buffer, it returns the DBP to the pool by writing it to BAD (the de-allocation process) across the Output FusionBus.

Smart Buffer Module

The Smart Buffer (SB) Module manages the Output Header queues between the completion of forwarding by the Packet Processing Engine (PPE) or MIPS CPU and the actual output transmission by the POM. Output Headers in each queue may be resident in the Local Buffer Memory of the Smart Buffer, or they may be held in main memory while SB maintains pointers to them. In either case the source of output headers always writes them to the same Smart Buffer address for each queue, and the POM always reads output headers for processing from the same address. Keeping Output Headers in the local Smart Buffer memory significantly improves performance for small packets. The IQ2000 contains four Smart Buffer modules, referred to as SB A, SB B, SB C, and SB D, that provide a combined total of 256 queues and 256 local memory buffers.

Multicast ID Module

The Multicast ID Module (MID) provides hardware support for broadcast and multicast packets. Broadcast and multicast packets have a single source and multiple destinations, therefore a separate packet must be transmitted for each destination port. The broadcast/multicast Output Header is copied into the Smart Buffer for each of the destination ports of a broadcast/multicast packet. However, the Payload Data Buffer from a broadcast/multicast packet is not duplicated for each destination port. The MID tracks a unique Multicast Identifier (MCID) and Multicast Count for each multicast packet that has payload data. When an agent attempts to de-allocate a multicast packet DBP, MID uses the MCID to reference the Multicast Count. The Multicast Count is decremented each time an agent attempts to de-allocate the DBP. When the Multicast Count is decremented to zero, the DBP is de-allocated by MID and the MCID is released for assignment to another multicast/broadcast packet with payload data.

Packet Processing Modules

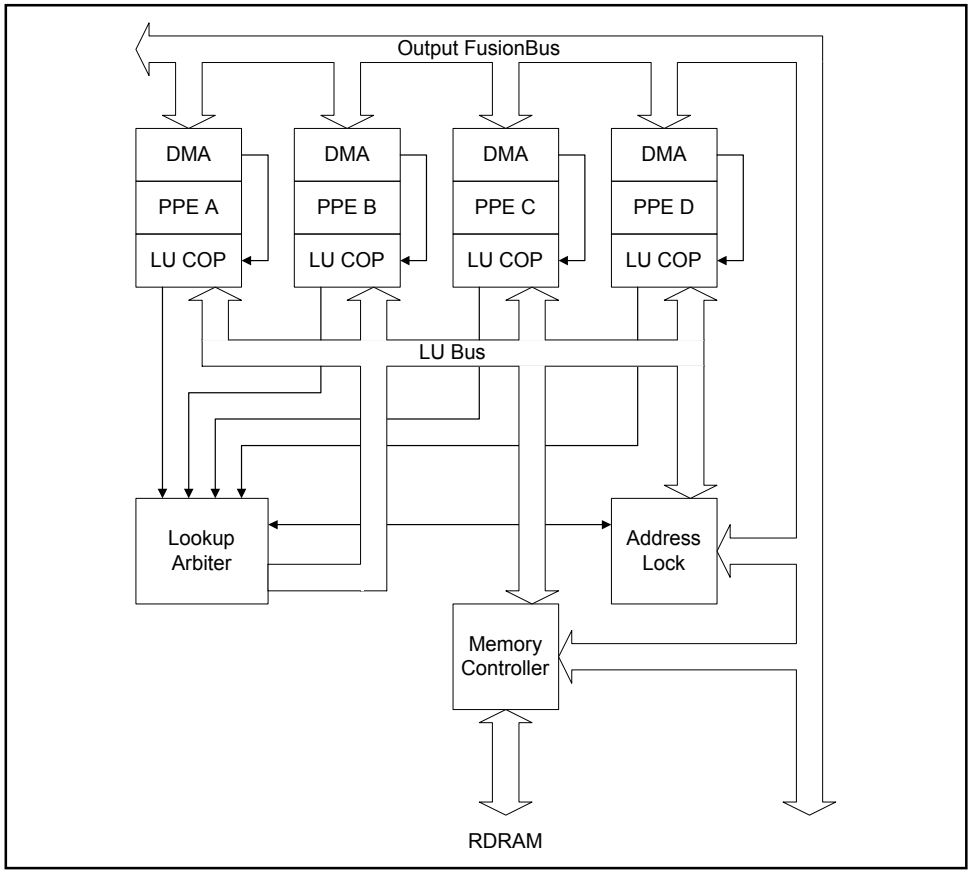
The IQ2000 Packet Processing System is the heart of the IQ2000 Packet Processor. This extremely powerful processing system is built around four Packet Processing Engines (PPE), each of which consists of a 200 MHz RISC CPU known as FACET with significant hardware-acceleration features to facilitate the rapid and efficient movement of data between the PPE and other IQ2000 elements. In addition to the four PPE sub-systems, the Packet Processing System includes several shared resources for moving data between the assigning packets, to PPEs, and to accelerate table-lookup operations.

FACET CPU

FACET, the IQ2000's embedded RISC CPU, contains a CPU core that provides a general- purpose instruction set for use in embedded packet processing applications. The instruction set is standards-based, minus a few instructions, but features additional instructions specifically to accelerate packet processing. FACET is a 32-bit, 200-MHz enhanced version of a standard RISC processor. It contains five sets of 32 32-bit registers, allowing up to four separate contexts to be active simultaneously. The processor has a five-stage pipelined architecture, and includes separate busses for instruction, data, and coprocessor access. The device contains a 16-instruction microbuffer with intelligent instruction lookahead and branch prediction. FACET includes several powerful debug features designed to simplify the process of code development and debug. These features include single-step and other clock-control functions, direct register and state access from the MIPS Host CPU, and a variety of traps and other exception checks. FACET incorporates some implementation features that are not part of standard implementations but do adhere to the standard instruction-set architecture. Specifically, the instructions include non-blocking scheduled loads, dual-cycle stalled branches, back-to-back branching, context-register- window mode, hardware interrupt-priority mode, special application-specific instructions, and special debug and test features.

Lookup Coprocessors

The Lookup System of the IQ2000 accelerates typical lookup functions by supplying all four FACET processors with highly efficient, content-based accesses to main memory, and providing coherency between the multiple FACETs and MIPS host CPU concurrently accessing the same data.



IQ2000 Lookup System

The Lookup System consists of a central resource called the Local Address Block (LAB), which provides coherency, and a Co-processor function in each of the PPEs that provides an efficient interface to the RDRAM. Each of the PPEs makes Lookup Requests through its Lookup Coprocessor (LU COP) to the RDRAM, presenting necessary information to initiate the lookup. The LU COP arbitrates among these requests to select memory references, which are made over a special interface to the Memory Controller called the LU Bus. The LU Bus is a high-speed, read-only bus that supports up to four pipelined 32-byte references. Once the selected data has been read from memory, the LU COP performs an equality check on the fields in the data to see if the correct information has been found.

Once the proper data is found, the data is placed in a 32-byte block in the PPE Local Memory Data Store and the requesting PPE is signaled that the data has been retrieved. The PPEs can then look at this data, and modify it in their Local Memory. When the operation is complete, the PPE may write the data back to main memory using the DMA Coprocessor. Because multiple PPEs may be simultaneously accessing the same lookup entry, the LAB maintains coherency. PPEs may lock lookup entries, in which case other PPEs may not have write access to this data until the lock is released.

The IQ2000 Lookup System accesses data in main-memory data structures called lookup tables, which may vary in the number of lookup entries. To initiate the lookup process, FACET supplies to the LU COP: a lookup address, which is the main memory address where the search for the data should begin; a local memory address which defines where the lookup result is placed; and a key, which is the data value being looked up. The LU COP then fetches 32 bytes starting at the lookup address, and compares a fixed-position field within the lookup entry with the key. If the key matches the field within the lookup entry, the lookup is complete; if the key does not match, the next lookup entry is checked. Entries are maintained in a 32-byte block linked list.

This process continues until one of three things occurs:

1. The key matches, and the lookup is Complete.
2. A lookup entry is encountered which has the INVALID bit set. This indicates that all lookup entries that could contain this value have been checked, and thus the key does not have a corresponding lookup entry in the table. In this case the lookup is unsuccessful.
3. The number of entries to check, as defined by the parameter block, are checked and neither the key nor an INVALID entry is found.

DMA Co-Processor

The DMA co-processor provides the FACET RISC CPU with the capability of executing block data transfers of header and data buffers between local memory and system memory. Of particular value is the fact that these transfers occur in parallel with the operation of the CPU, so that memory transfers may be very effectively overlapped with other CPU execution. The DMA co-processor transfers blocks of data from 1 to 128 bytes in length using DMA byte-transfer instructions, of 8 to 1024 bytes (1 to 128 double words) in length, using DMA extended-transfer instructions.

Order Manager Module

The Order Manager (OM) directs the flow of input headers from the MIPS Host Interface or a Packet Input Module (PIM) to the Header Memory in one of the Packet Processing Engines (PPE) and preserves packet order through the PPE. The PPE may process several packets concurrently and the processing may complete in a different order than the arrival order into the IQ2000. The OM preserves packet ordering by tracking packet-release dependencies and notifying the PPE of packets that are cleared for output to the Smart Buffer (SB) and, ultimately, the Packet Output module (POM).

Overflow Queue Module

The Overflow Queue Module (OQM) provides a linear overflow queue in system memory for the Order Manager to store packet headers and input completion messages in the event that all of the active PPE header buffers are busy.

Data and Header Memory

Each FACET processor has very fast access to its own 4KB of Local Memory divided equally between Header Buffer and the Data Memory. The Data Memory is typically used by the PPE software for local data storage. The Header Buffer is typically used to store Headers transferred from the PIM (via the Order Manager) or the MIPS Host CPU.

Control Store

The Control Store (CS) Module provides the four Packet Processing Engines (PPE) with a high-speed, on-chip 32KByte (8K instruction) or 64KB (16K instruction) control store for executing code. The Control Store requires minimal configuration and management by software and allows the CPUs to execute with a minimum of instruction-fetch stalls.

System Modules

Host Interface

The IQ2000 Host Interface module provides an external microprocessor with access to FusionBus devices and memory via the MIPS Host Interface (MHIF) or the Asynchronous Host Interface (AHIF). It translates the external CPU bus cycles into the corresponding FusionBus transactions, stalling the external CPU bus interface only when necessary. This module also contains logic and registers to generate configuration cycles on FusionBus for configuring other IQ2000 modules within the chip. The interface also includes a 256 byte programmable Burst Buffer.

The MHIF provides a 32/64-bit connection to MIPS® microprocessors. Because this is a relatively high bandwidth interface, an IQ2000 chip can be used as a MIPS “system chip” and is fast enough to service MIPS code and data accesses.

The AHIF provides a 32-bit connection to other microprocessors, such as a Power PC. It allows the IQ2000 to be used as a “peripheral chip” rather than a “system chip”. Although the same internal IQ2000 resources can be accessed, microprocessor code access via this interface would be quite slow. So, it will most likely be used by connection to a peripheral bus controller. This interface is designed to be less complex and connector and backplane-friendly.

Direct RDRAM Memory Controller

The Direct RDRAM Memory Controller (MEMC) provides access to external system memory on a single RAMBUS TM channel. It handles simultaneous MIPS Host Processor and FusionBus transaction requests, and transfers the data between external memory and all system masters. MEMC support includes up to 32 devices, an 18-bit (16-bit + 2 parity) 800 MHz data path, programmable timing parameters, a programmable memory base, and PROM shadowing. Sophisticated arbitration, buffering, and memory bank management logic helps remove possible bottlenecks in the system.

Static RAM Memory Controller

The Static RAM Memory Controller (SRAM) provides access to external SRAM memory. It handles simultaneous MIPS Host Processor and FusionBus transaction requests, and transfers the data between external memory and all system masters.

PROM I/O

The PROM-I/O (PIO) Module provides the IQ2000 with a variety of external connections and system features. The external connections include Boot PROM, Flash PROM, general-purpose external registers, and devices such as full function UARTs. Up to 256 MB of external address space is provided, with up to eight separate chip-selects available. System features include a minimum-function UART and four 32-bit timer/counters.

FusionBus™

The interconnection between Modules in the IQ2000 is a 12.8-Gbps fabric called the FusionBus. The IQ2000 includes two separate segments of the FusionBus, which are each connected to the Host Interface and the Memory Controller. From the logical system perspective, the two FusionBuses are similar to a PCI Bus and each internal IQ2000 Module appears as a separate device. Most internal Modules function as both masters (i.e. initiators of transactions) and slaves on the FusionBus, although the Memory Controller, Smart Buffer, Buffer Allocator/Deallocator, SRAM Interface and PROM/IO Modules are only slaves. Each FusionBus Module occupies a portion of the 4-GB address space of the MIPS CPU.

The FusionBus provides a common connection between all IQ2000 modules. It supports multiple simultaneous transactions between a master, which initiates the transaction, and a slave. A master initiates an operation with a slave by addressing it over the FusionBus, and then transferring data (1-2048 bytes) in an interleaved burst fashion.

Electrical Specifications

Pin Assignment

For complete signal to pin (ball) assignment, refer to Vitesse's *IQ2000 Design Manual*.

Pinout

IQ2000 pins, associated signals and corresponding directions are indicated below. Pins are grouped by system or device function. Pin types include A (analog), O (CMOS output), I (CMOS input), I-PD (input with internal pull-down), B (CMOS bidirectional), B-PD (bidirectional with internal pull-down), RSL (Rambus Signal Level), power, and ground (the latter two are not designated by an identifier).

Module	Signal Name	Qty	Pin Type	Description
CLOCK & RESET				
	XTAL_IN	1	A	Main PLL crystal.
	XTAL_OUT	1	A	Main PLL crystal.
	OSCOUT	1	O	Internal Oscillator Output
	SYS_RST_N	1	I	System reset.
	RST_PHASE_N	1	I	Phase Aligner reset
	CLKINSEL	1	I-PD	Clock select input for PLL bypass.
FOCUSA				
	FCSA_TXD[15: 0]	16	O	Transmit data bus
	FCSA_TX_CLK	1	B	Transmit clock
	FCSA_TX_REQ	1	I	Transmit request signal
	FCSA_RXD[15: 0]	16	I	Receive data bus
	FCSA_RX_CLK	1	I	Receive clock
	FCSA_RX_RDY	1	O	Receive ready signal
FOCUSB				
	FCSB_TXD[15: 0]	16	O	Transmit data bus
	FCSB_TX_CLK	1	B	Transmit clock
	FCSB_TX_REQ	1	I	Transmit request signal
	FCSB_RXD[15: 0]	16	I	Receive data bus
	FCSB_RX_CLK	1	I	Receive clock
	FCSB_RX_RDY	1	O	Receive ready signal
FOCUSC				
	FCSC_TXD[15: 0]	16	O	Transmit data bus
	FCSC_TX_CLK	1	B	Transmit clock
	FCSC_TX_REQ	1	I	Transmit request signal
	FCSC_RXD[15: 0]	16	I	Receive data bus
	FCSC_RX_CLK	1	I	Receive clock
	FCSC_RX_RDY	1	O	Receive ready signal

Module	Signal Name	Qty	Pin Type	Description
FOCUSD				
	FCSD_TXD[15: 0]	16	O	Transmit data bus
	FCSD_TX_CLK	1	B	Transmit clock
	FCSD_TX_REQ	1	I	Transmit request signal
	FCSD_RXD[15: 0]	16	I	Receive data bus
	FCSD_RX_CLK	1	I	Receive clock
	FCSD_RX_RDY	1	O	Receive ready signal
MIPS				
	MIPS_CLK_OUT	1	O	Master clock, output
	MIPS_CLK_IN	1	I	Master clock, input
	MIPS_VCCOK	1	O	VCC okay
	MIPS_RST_N	1	O	Reset.
	MIPS_COLDRST_N	1	O	Cold reset.
	MIPS_SYSAD[63:0]	64	B	Data Bus
	MIPS_SYSADC[7: 0]	8	B	Parity on the Data Bus
	MIPS_SYSCMD[8: 0]	9	B	System command/data identifier bus.
	MIPS_WRRDY_N	1	O	Write ready.
	MIPS_VALIDOUT_N	1	I	Valid output.
	MIPS_RELEASE_N	1	I	Release interface.
	MIPS_VALIDIN_N	1	O	Valid input.
	MIPS_SCTCE_N	1	I	Tag RAM chip enable
	MIPS_SCMATCH	1	I	Cache Tag match
	MIPS_SCDOE_N	1	O	Data RAM output enable
	MIPS_SCWORD[1: 0]	2	O	Data RAM word index
	MIPS_INT_N[3: 0]	4	O	Interrupt.
	MIPS_NMI_N	1	O	Non-maskable interrupt.
SRAM				
	SRAM_ADDR[19:0]	20	O	SRAM Address
	SRAM_DATA[31:0]	32	B	SRAM Data
	SRAM_PAR[3:0]	4	B	SRAM Parity
	SRAM_CEN[1:0]	2	O	SRAM Chip Enables
	SRAM_WEN[3:0]	4	O	SRAM Write Enables
	SRAM_CLK	1	O	SRAM Clock
	SRAM_OEN	1	O	SRAM Output Enable
	SRAM_R_WR_N	1	O	SRAM Read/Write Not

Module	Signal Name	Qty	Pin Type	Description
PROM and Serial UART and Serial Bus Ports				
	PROM_SCL	1	O	Serial Bus Clock
	PROM_SDA	1	B	Serial Bus Data
	UART_RI	1	I	Ring Indicator
	UART_CTS	1	I	Clear to Send
	UART_DSR	1	I	Data Set Ready
	UART_DCD	1	I	Data Carrier Detect
	UART_RXD	1	I	Serial receive data.
	UART_TXD	1	O	Serial transmit data.
	UART_DTR	1	O	Data Terminal Ready
	UART_RTS	1	O	Ready to Send
	PROM_AD[15: 0]	16	B-PD	PROM address/data bus
	PROM_OE_N	1	O	PROM output enable
	PROM_LO_WE_N	1	O	PROM write enable low 8 bits.
	PROM_HI_WE_N	1	O	PROM write enable high 8 bits
	PROM_LO_ADR_CLK	1	O	PROM clock lower latch
	PROM_HI_ADR_CLK	1	O	PROM clock higher latches
	PROM_READ	1	O	PROM read/write direction bit
RDRAM				
	RDRAM_DQA[8: 0]	9	RSL	Data bus low
	RDRAM_DQB[8: 0]	9	RSL	Data bus high
	RDRAM_RQ[7: 0]	8	RSL	Request Byte
	RDRAM_REFCLK	1	O	RDRAM Reference Clock Output
	RDRAM_CTM	1	RSL	Differential Clock In
	RDRAM_CTM_N	1	RSL	Differential Clock In
	RDRAM_CFM	1	RSL	Differential Clock Out
	RDRAM_CFM_N	1	RSL	Differential Clock Out
	RDRAM_SIO	1	B	Serial Data In/Out
	RDRAM_SIOCLK	1	O	Serial/Command Clock
	RDRAM_SIOCMD	1	O	Serial Command
	RDRAM_SCLKN	1	O	SCLK for phase alignment
	RDRAM_PCLKM	1	O	PCLK for phase alignment
	RDRAM_MULTI[1:0]	2	O	External Clock Multiply Ratio
NO CONNECT				
	NC_I[1:0]	2	O	No connection
	NC_O[2:0]	3	O	No connection

Module	Signal Name	Qty	Pin Type	Description
TEST				
	PLS800_ITEST	1	A	Reserved
	PLS800_TS0	1	I	Reserved
	PLS800_TS1	1	I	Reserved
	ROFF_TRIGGER	1	I-PD	Trigger to latch Read-only flip-flops
	TCK	1	I	JTAG clock
	TDO	1	O	JTAG data out
	TDI	1	I-PU	JTAG data in
	TMS	1	I-PU	JTAG mode select
	TRST_N	1	I-PU	JTAG reset
	SCANMODE	1	I-PD	Scan mode
	TESTMODE	1	I-PD	FusionBus test mode
POWER & GROUND				
	AVDD	1		Analog Power - 3.3 Volts
	VDD_CORE	26		Core power - 2.5 Volts
	VDD_IO	32		IO power - 3.3 Volts
	VDD_RAMBUS	4		Rambus power -3.3 Volts
	VDDA_RAMBUS	2		Rambus power - 2.5 Volts
	RDRAM_VREF	2		Voltage Reference - 1.4 Volts
	VSS	205		Ground

Asynchronous Host Interface Signal Mapping

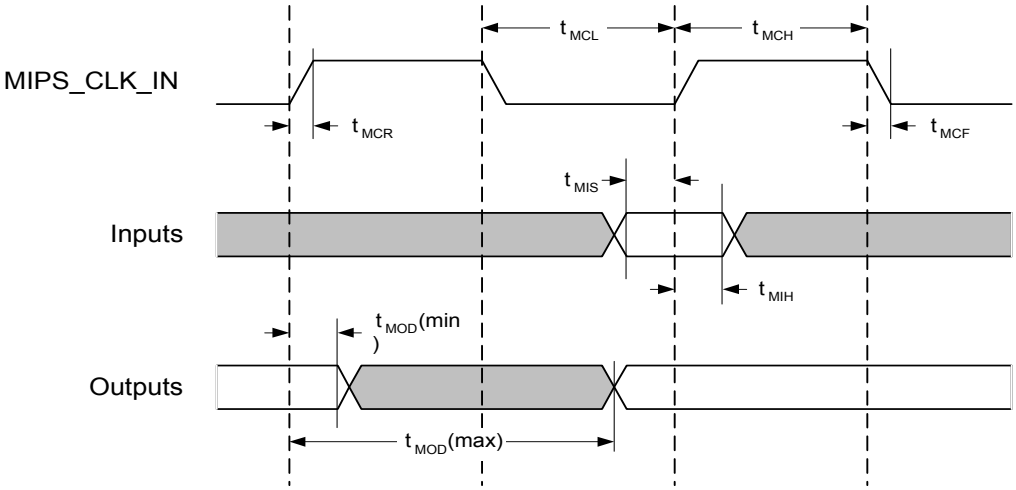
The signals described in the preceding table assume connection to a MIPS-compatible microprocessor for use as a “system chip” via the MHIF. Instead, if the IQ2000 is to be used as a “peripheral chip”, the host microprocessor is connected to the IQ2000 via the alternative Asynchronous Host Interface (AHIF). The following table defines the AHIF to MHIF signal mapping.

Async Host Interface	Signal Name
AH_AD[31:0]	MIPS_SYSAD[31:0]
AH_WE_N	MIPS_SYSCMD [0]
AH_CS_N	MIPS_SYSCMD [1]
AH_DS_N	MIPS_SYSCMD [2]
AH_RDY	MIPS_VALIDIN_N
AH_ERR_N	MIPS_WRRDY_N
AH_INT_N[3:0]	MIPS_INT_N[3:0]

To enable the asynchronous mode, the pins (balls) of the MIPS_INT_N[3], MIPS_VALIDIN_N, MIPS MIPS_WRRDY_N, MIPS_VALIDOUT_N, MIPS_RELEASE_N, and PROM)AD[15] signals must be pulled high; MIPS_INT_N[2:0] signals should be individually pulled high if the interrupts are used, or connected together and pulled high if unused. The MIPS_NMI_N signal must be pulled low. 47.5K ohm resistors should be used with all pulled-high or pulled-low signals. These are static configuration bits that are latched on reset.

AC Electrical Specifications

MIPS System Interface Timing



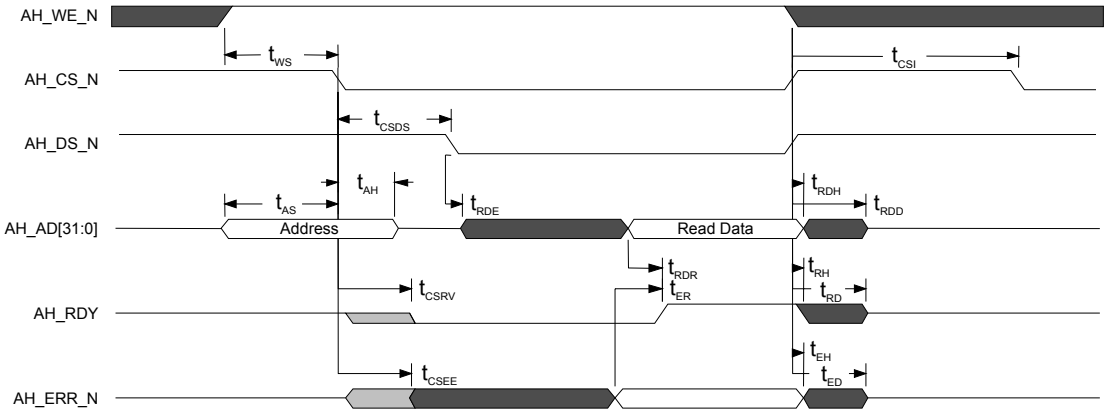
Inputs = all input signals whose signal names start with MIPS_

Outputs = all output signals whose signal names start with MIPS_

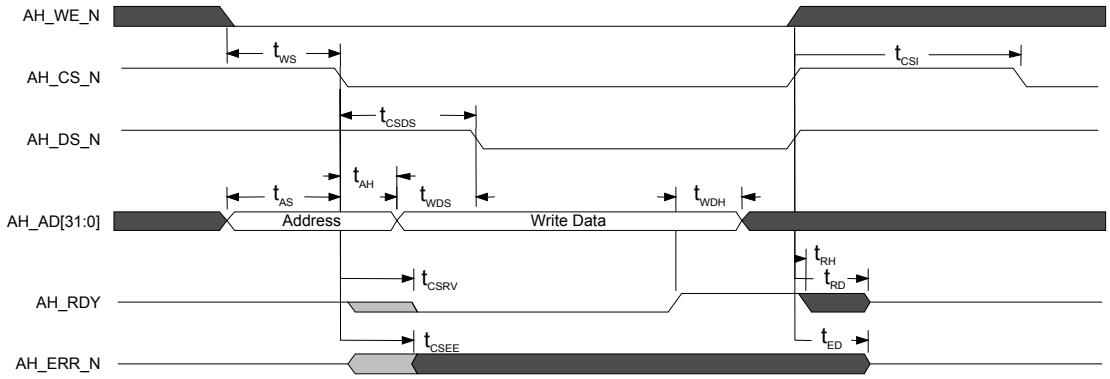
Symbol	Parameter	Direction	Min	Max	Unit
f_{MC}	MIPS_CLK_IN frequency	I	-	100	MHz
t_{MCL}	MIPS_CLK_IN low	I	3	-	ns
t_{MCH}	MIPS_CLK_IN high	I	3	-	ns
t_{MCF}	MIPS_CLK_IN fall	I	-	2	ns
t_{MCR}	MIPS_CLK_IN rise	I	-	2	ns
t_{MIS}	Input setup	I	2	-	ns
t_{MIH}	Input hold	I	1	-	ns
t_{MOD}	Output delay	O	2	11.5	ns

Asynchronous Host Interface Timing

Asynchronous System Interface Read Timing



Asynchronous System Interface Write Timing



Asynchronous Host Interface Timing (cont.)

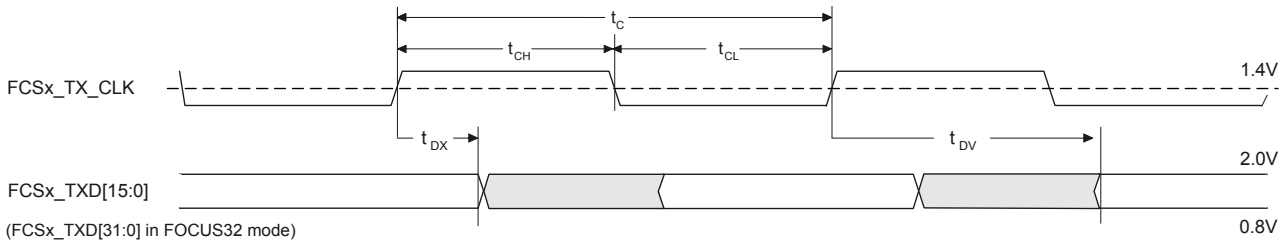
Symbol	Description	Minimum	Typical	Maximum	Unit	Notes
t_{WS}	AH_WE_N Setup	8			ns	1
t_{AS}	Address Setup	8			ns	1
t_{AH}	Address Hold	6			ns	
t_{CSDS}	AH_CS_N to AH_DS_N	MCLK+6			ns	2
t_{CSRV}	AH_CS_N to AH_RDY Low	2		13	ns	
t_{CSEE}	AH_CS_N to AH_ERR_N Enabled	2		13	ns	3
t_{WDS}	Write Data Setup	0			ns	
t_{WDH}	Write Data Hold	0			ns	
t_{RDE}	Read Data Enabled	2			ns	4
t_{RDR}	Read Data to AH_RDY High	MCLK-4			ns	2
t_{ER}	ERR_N to AH_RDY	MCLK-4			ns	2
t_{RDH}	Read Data Hold	2			ns	5
t_{RDD}	Read Data Disabled			13	ns	5
t_{RH}	AH_RDY Hold	2			ns	6
t_{RD}	AH_RDY Disabled			13	ns	6
t_{EH}	AH_ERR_N Hold	2			ns	7
t_{ED}	AH_ERR_N Disabled			13	ns	7
t_{CDI}	AH_CS_N Inactive	4*MCLK			ns	2

Notes on Asynchronous Host Interface timing parameters:

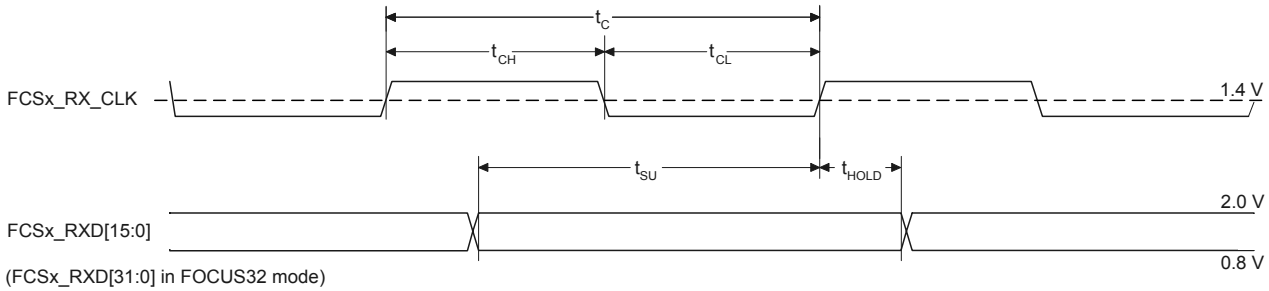
1. AH_WE_N & AH_AD are latched on AH_CS_N falling edge.
2. MCLK is the period of the Module Clock that is ½ FCLK, the clock frequency of the IQ2000.
3. AH_ERR_N is asserted when a read error has occurred. AH_ERR_N should be ignored for writes.
4. On a read, IQ2000 starts driving the data bus after AH_DS_N is asserted. The Host must release the bus before AH_DS_N is asserted to allow time for bus turnaround.
5. Read Data Hold and Disable time are relative to AH_CS_N or AH_DS_N or AH_WE_N.
6. AH_RDY Hold and Disable time are relative to AH_CS_N.
7. AH_ERR_N Hold and Disable time are relative to AH_CS_N or AH_WE_N.

FOCUS Interface Timing

FOCUS Interface PIM Receive Data Timing

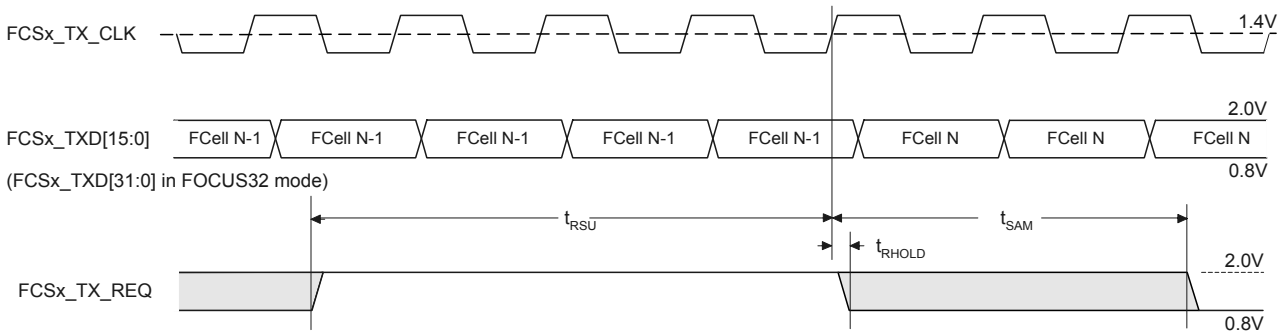


FOCUS Interface POM Transmit Data Timing

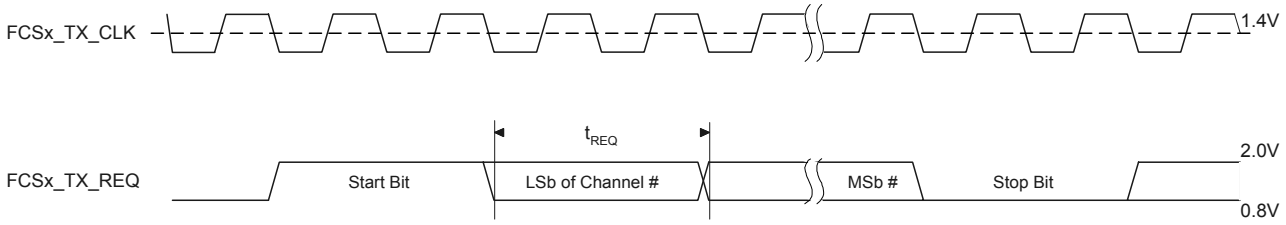


FOCUS Interface Timing (cont.)

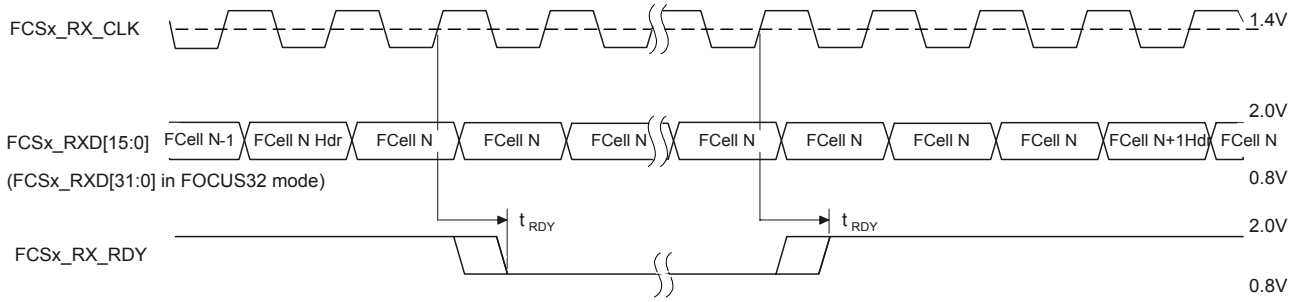
FOCUS Interface POM Ready Mode Input Timing



FOCUS Interface POM Request Mode Input Timing



FOCUS Interface PIM Ready Mode Output Timing



FOCUS Interface Timing (cont.)

Symbol	Description	Minimum	Typical	Maximum	Notes
t_C	Clock period	10.0 ns			1
t_{CL}	Clock low	0.4*T_C	0.5* T_C	0.6* T_C	2
t_{CH}	Clock high	0.4*T_C	0.5* T_C	0.6* T_C	2
t_{DX}	Clock to data out invalid	2ns			3
t_{DV}	Clock to data out valid			6.5ns	4
t_{SU}	Input data setup to clock	2ns			
t_{HOLD}	Input data hold from clock	1ns			
t_{RSU}	Ready high setup to start of FCell	3*T_C + 6ns			5
t_{RHOLD}	Ready high hold from start of FCell	0 ns			6
t_{SAM}	Start of FCell to Ready sampled	3*T_C - 6ns			7
t_{REQ}	Serial Request bit period	1.9*T_C	2*T_C	2.1*T_C	8
t_{RDY}	Clock to Ready delay	2ns		6ns	9
	t_{RISE}, t_{FALL}	1.5V/ns		4V/ns	

Notes on FOCUS interface timing parameters:

1 IQ2000 supports clock rates from DC to 100MHz. No clock rate relationships have been assumed.

2 t_{CL},t_{CH} apply to FCSx_RX_CLK. t_{CL},t_{CH} also apply to FCSx_TX_CLK when using external clock mode (CLK-MODE=000).

3 This value specifies how long old data is held valid on the bus after clock. t_{DX} applies to FCSx_TX_CLK when using either internal or external clock mode.

4 This value specifies how long from clock to new data being valid for signals driven onto the FOCUS bus. t_{DV} applies to FCSx_TX_CLK when using either internal or external clock mode.

5 Meeting this value insures the start of the next FCell. If this value is not met, the FCell start will be delayed by 1 or more clocks.

6 This is the time that Ready must be held valid after the start of a FCell.

7 This is the time from the start of a FCell until Ready is sampled again. If any FCell, 6 clocks or greater, is being transferred and Ready is high at t_{SAM}, then back-to-back FCell transfers can occur. For larger FCells, use t_{RSU}. This delay can be increased by programming the POM_CTRL:FCELL_DIST register.

8 The RDY/REQ signal in serial Request mode is sampled at Clk/2. The nominal bit period can vary slightly without causing mis-synchronization. There is no required timing relationship between serial requests and FCell transfers. The next serial request for a given channel can be sent at any time after the FCell for that channel starts transferring.

9 Ready needs to be asserted ~4 clocks before the end of a FCell to allow back-to-back FCell transfers without any idle gaps.

10 FOCUS timing characterized with 1ns input transition times and 20pF output loads.

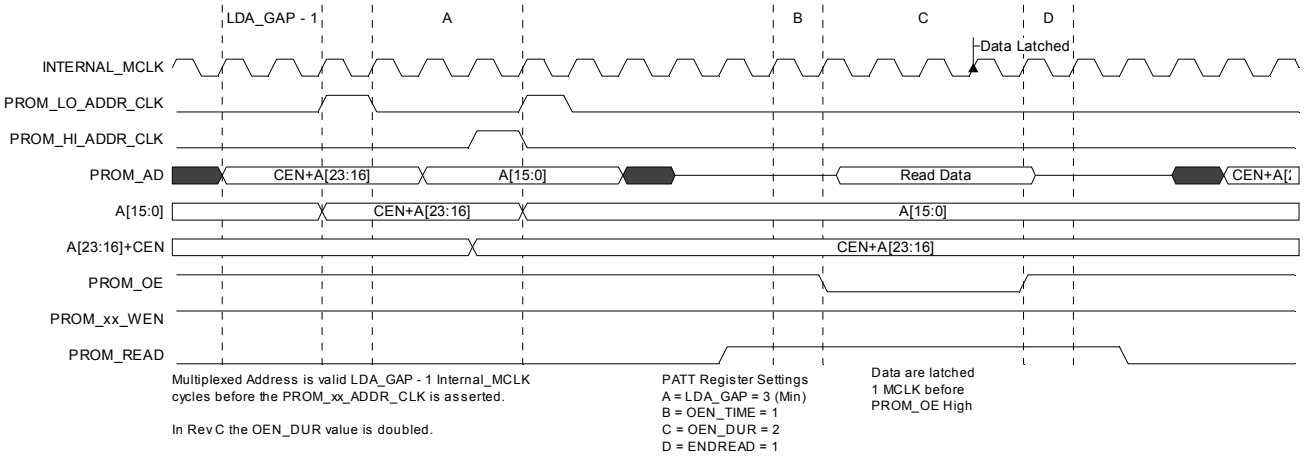
PROM Timing

The PROM Attribute Register (PATT) provides the capability to tune the timing of external transactions on the PROMIO connection. For each operation, several cycles occur in which the address and chip select (CSN) signals are loaded into the external registers. The LDA_GAP parameter defines the number of MCLK cycles that occur between clock pulses on the address load signal. MCLK is the FusionBus clock divided by two, and typically has 10 ns cycles.

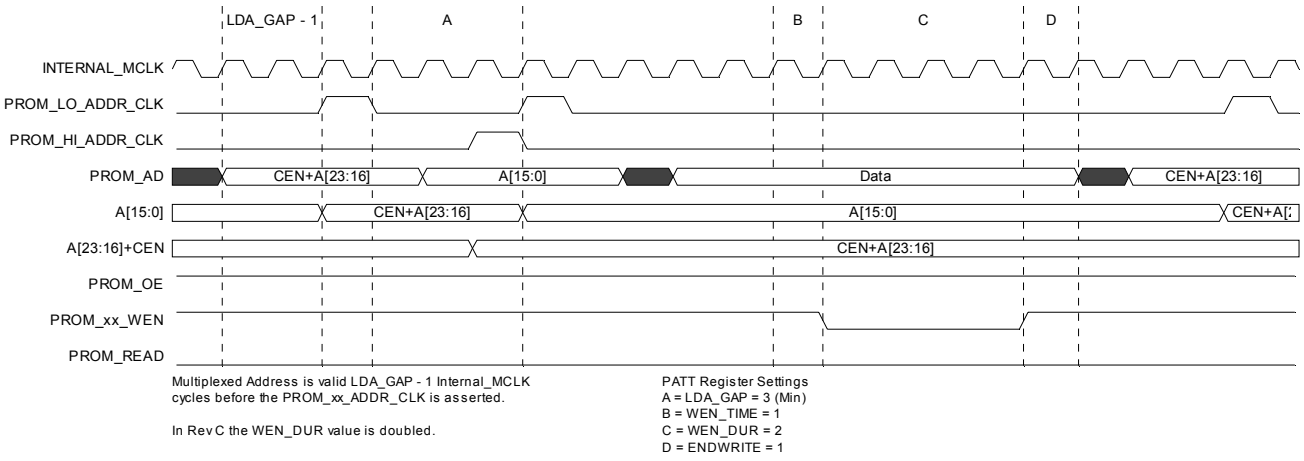
From the point in time that the last load address clock occurs, PATT defines the timing of the PROM_LO_WEN, PROM_HI_WE_N and PROM_OE_N signals, in increments of MCLK cycles. WEN_TIME and OEN_TIME define the number of clock periods between the final clock to the address register and the assertion of PROM_LO_WEN, PROM_HI_WE_N or PROM_OE_N. WEN_DUR and OEN_DUR describe the number of clocks from the assertion of PROM_LO_WEN, PROM_HI_WE_N or PROM_OE_N and the deassertion, and thus define the pulse widths for these two signals. ENDWRITE and ENDREAD describe the number of clocks from the deassertion of PROM_LO_WEN, PROM_HI_WE_N or PROM_OE_N and the next cycle on which the address and CSn signals can change, thus supplying address and CSn hold time from PROM_LO_WEN, PROM_HI_WE_N or PROM_OE_N.

The following diagrams shows the timing sequence for a single 8 or 16 bit access.

PROM IO Read Cycle



PROM IO Write Cycle



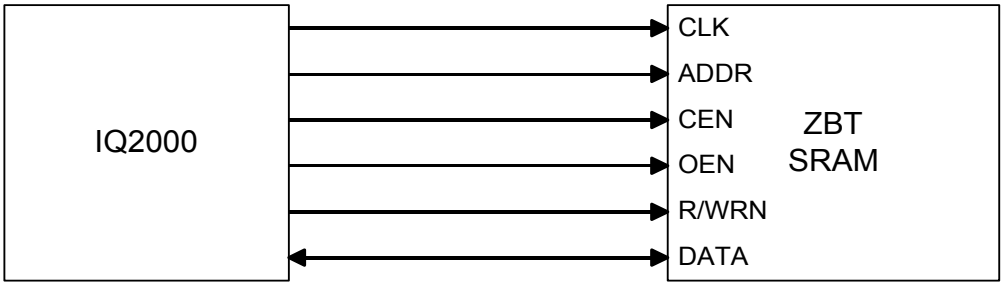
The sequence of operations is:

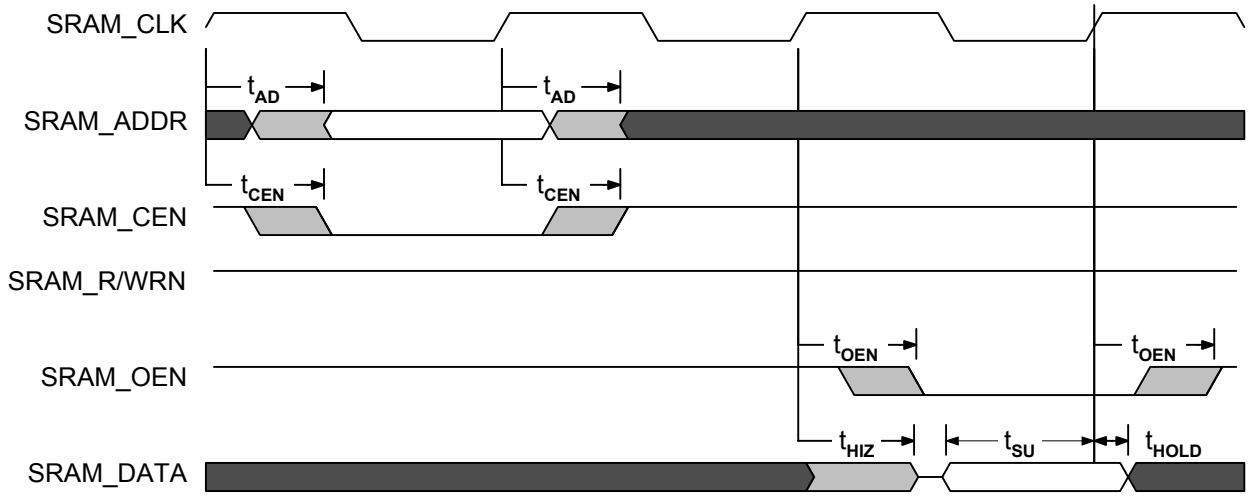
1. The LOAD_AD signal represents either the PROM_LO_ADR_CLK or the PROM_HI_ADR_CLK. In some cases there will be two, three or four clocks to load the address register, depending on the PROM configuration. LDA_GAP specifies time “A”, the gap between successive loads. This will typically be programmed to 0x1 (10 ns).
2. When the last rising edge of the load clock occurs, the address and chip select signals become valid, and the access starts.
3. WEN_TIME or OEN_TIME define time period “B”, the time from the last address clock to the assertion of PROM_OE_N, PROM_LO_WE_N or PROM_HI_WE_N. This is a six bit value, so the time is from 0 ns to 630 ns.
4. WEN_DUR or OEN_DUR define the time period “C”, the duration of the write enable or output enable signal. This is a four bit value, so the duration is from 0 ns to 150 ns.
5. If hold time on the address or chip select is required after write enable or output enable, ENDWRITE or ENDREAD define the time period “D”, before the next load clock which changes the address.
6. The address/chip select time is the sum of periods “B” and “C”, which can be a maximum of 780 ns.

If a burst of multiple accesses is made, for example by initiating a 64 bit read from an eight bit device, the upper address and CSN signals will remain constant, and only the lower address will be changed. A series of cycles like the one shown will occur for the number of accesses required to complete the burst.

The PATT Register is initialized to the longest values for all parameters, to insure that any device may be accessed at initialization. Software should immediately adjust these values to the appropriate ones to improve Boot performance.

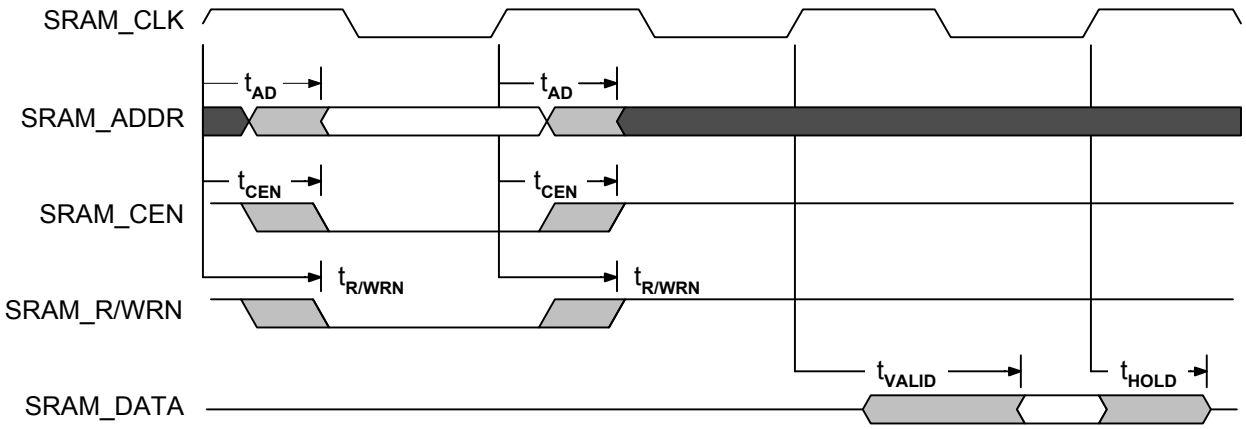
SDRAM Interface Read Timing





Symbol	Description	Min	Max	Units
t_{AD}	clock to address valid	0.8	4.5	ns
t_{CEN}	clock to CEN valid	0.8	4.5	ns
t_{OEN}	clock to OEN valid	0.8	4.5	ns
t_{HIZ}	clock to DATA_IN HighZ	0.52	0.96	ns
t_{SU}	clock to DATA Setup	2.62	–	ns
t_{HOLD}	clock to DATA Hold	-0.85	–	ns

SDRAM Interface Write Timing



Symbol	Description	Min	Max	Units
t_{AD}	clock to address valid	0.8	4.5	ns
t_{CEN}	clock to CEN valid	0.8	4.5	ns
t_{WEN}	clock to WEN valid	0.8	4.5	ns
$t_{R/WRN}$	clock to R/WRN valid	0.8	4.5	ns
t_{VALID}	clock to DATA valid	3.1	6.8	ns
t_{HOLD}	clock to DATA Hold	0.52	–	ns

RDRAM Interface Timing

Contact RAMBUS Corporation for information related to RDRAM interface and timing issues. RAMBUS technical product documentation may be found online at:

http://www.rambus.com/developer/quickfind_documents.html

Serial UART Interface Timing

This will be provided in a later revision of this document.

I/O Test Conditions

3.3V AC Test Conditions (exclusive of FCS/GM* signals)*

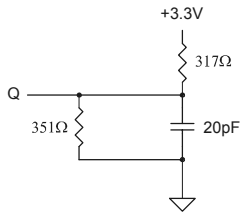
Input pulse levels . . . . . Vss to 3.3V

Input rise and fall times. 1ns

Input timing reference levels 1.5V

Output reference levels. 1.5V

3.3 I/O output load equivalents . . . . . .(shown below)



3.3V I/O AC Test Conditions (FCS/GM* signals only)*

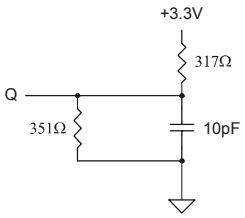
Input pulse levels . . . . . .Vss to 3.3V

Input rise and fall times 1ns

Input timing reference levels 1.5V

Output reference levels 1.5

3.3 I/O output load equivalents . . . . . (shown below)



Power Supply Considerations

The IQ2000 requires separate 3.3V (nominal) and 2.5V (nominal) power supplies for its I/O and core logic, respectively. All VDD_I/O pins should be connected to the 3.3V supply, and all VDD_CORE pins should be connected to the 2.5V supply.

Absolute Maximum Ratings

The following table sets forth the absolute maximum ratings for the IQ2000. Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational characteristics section. Exposure to absolute maximum ratings for extended periods can adversely affect the device's reliability

Symbol	Description	Minimum	Maximum	Unit
$V_{Vdd3.3}$	I/O supply with respect to VSS	–	3.465	V
$V_{Vdd2.5}$	Core supply with respect to VSS	–	2.625	V
V_{ESD}	Electrostatic discharge, Human Body Model	2000	–	V
V_{IN}	Input voltage	VSS - 0.5	$V_{Vdd3.3}$ + 0.5	V
$V_{IN - 5.5}$	Input voltage for 5V tolerant I/O	VSS - 0.5	5.5	V
$T_{ambient}$	Ambient temperature condition	0	70	°C
$T_{storage}$	Ambient storage temperature	-55	125	°C

Operational Characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{Vdd3.3}$	I/O supply with respect to VSS	0ºC - 70ºC	3.135	3.3	3.465	V
$V_{Vdd2.5}$	Core supply with respect to VSS	0ºC - 70ºC	2.375	2.5	2.625	V
$I_{Vdd3.3}$	Supply current	0ºC - 70ºC $V_{Vdd3.3}$ Max	0	0.22	0.29	A
$I_{Vdd2.5}$	Supply current	0ºC - 70ºC $V_{Vdd3.3}$ Max	0	4.0	4.267	A
$P_{Vdd3.3}$	I/O power dissipation	0ºC - 70ºC $V_{Vdd3.3}$ Max	0	0.73	1.00	W
$P_{Vdd2.5}$	Core power dissipation	0ºC - 70ºC $V_{Vdd2.5}$ Max	0	10.0	11.2	W
V_{IL}	Input voltage - low	–	VSS - 0.3	–	0.8	V
$V_{IH-3.3}$	nput voltage -highI	–	2.0	–	$V_{Vdd3.3}$+0.3	V
$V_{IH-5.0}$	Input voltage - high for 5V tolerant I/O Pins: CLKINSEL, PLL800_TS*, PROM_*, ROFF_TRIGGER, RST_PHASE_N, SCANMODE, SYS_RST_N, TCK, TDO, TDI, TESTMODE, TMS, TRST_N, UART_*	–	2.0	–	5.5	V
V_{OL}	Output voltage - low	$V_{Vdd3.3}$ = 3.6V I_{OH} = 4mA* I_{OH} = 8mA* I_{OH} = 16mA*	–	–	0.4	V
V_{OH}	Output voltage - high	$V_{Vdd3.3}$ = 3.0V I_{OH} = 4mA* I_{OH} = 8mA* I_{OH} = 16mA*	2.4	–	–	V
I_{IL-D}	Input leakage current - low for pull-downs Pins: CLKINSEL,PROM_AD*, SCANMODE, ROFF_TRIGGER, PLL800_TS*, TESTMODE	V_{IN} = VSS	-5	< 0.1	5	µA
I_{IL}	Input leakage currrent - low Pins: all other inputs and bidirectionals	V_{IN} = VSS	-5	0	5	µA
I_{IL-U}	Input leakage current - low for pull-ups Pins: TDI, TMS, TRST_N	V_{IN} = VSS	-70	-29	-5	µA
I_{IH-D}	Input leakage current - high for pull-downs Pins: CLKINSEL, PROM_AD*, SCANMODE, ROFF_TRIGGER, PLL800_TS*, TESTMODE	V_{IN} = $V_{Vdd3.3}$	-5	44	90	µA
I_{IH}	Input leakage current - high Pins: all other inputs and bidirectionals	V_{IN} = $V_{Vdd3.3}$	-5	< 0.1	5	µA
I_{IH-U}	Input leakage current - high for pull-ups Pins: TDI, TMS, TRST_N	V_{IN} = $V_{Vdd3.3}$	-5	< 0.1	5	µA
C_{IN}	Pin capacitance	–	3	4	5	pF

* Refer to Tables 2-2, 2-7 and 2-8 of IQ2000 Design Manual for affected balls/signals

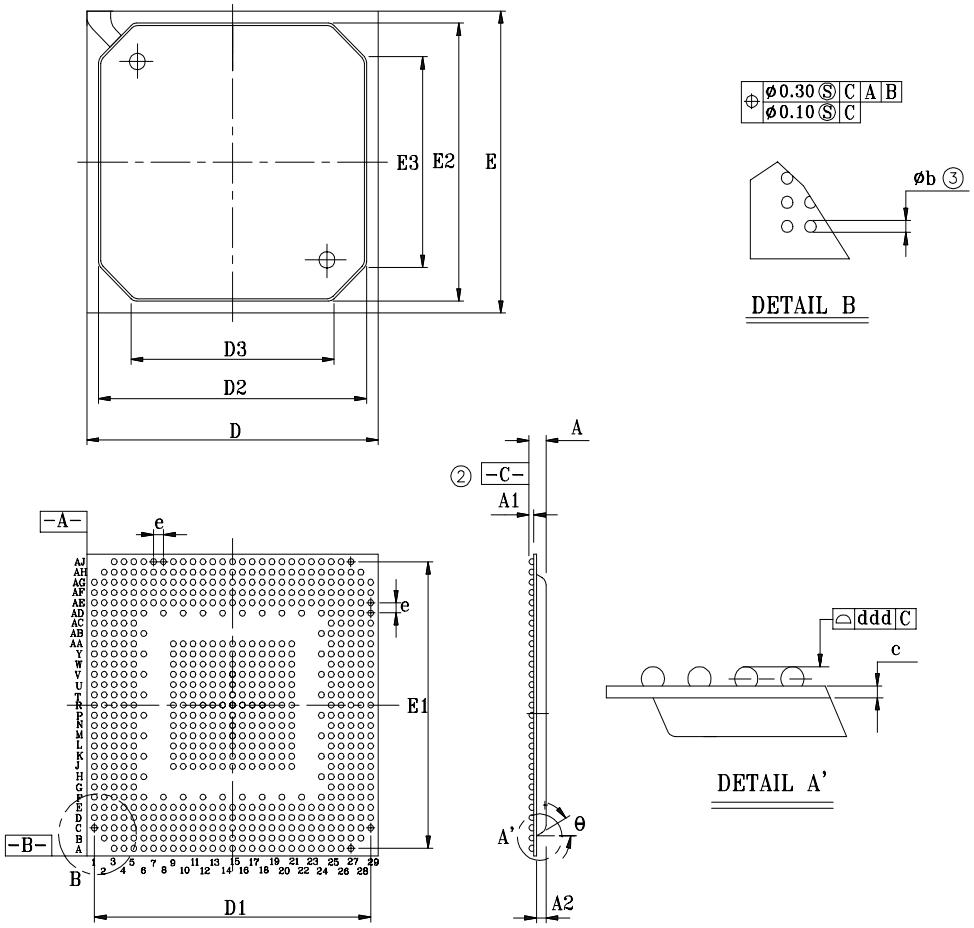
Thermal Specifications

The thermal specifications set forth below are based on modeling described in the IQ2000 Design Manual. The specificed maximum junction temperature is 125°C and the minimum is 0°C.

Air Flow	θ_{JA} (Typ) with No Heat Sink	θ_{JA} (Typ) with (35mm) [2] Heat Sink	θ_{JB}	θ_{JC}
Still Air	8.4ºC/W	5.6ºC/W	0.9ºC/W	2.5ºC/W
1 m/s	7.0ºC/W	3.8ºC/W	–	–
2 m/s	6.4ºC/W	3.4ºC/W	–	–
3 m/s	6.0ºC/W	3.2ºC/W	–	–

Mechanical Specifications

Packaging — 673 BGA



Packaging Dimensions

Symbol	Dimension in mm			Dimension in inches		
	Min	*Nom*	*Max*	*Min*	*Nom*	*Max*
A	2.13	2.33	2.53	0.084	0.092	0.100
A1	0.50	0.60	0.70	0.020	0.024	0.028
A2	1.12	1.17	1.22	0.044	0.046	0.048
b	0.60	0.75	0.90	0.24	0.030	0.035
c	0.51	0.56	0.61	0.020	0.022	0.024
D	37.30	37.50	37.70	1.469	1.476	1.484
D1		35.56 BSC			1.400 BSC	
D2	34.30	34.50	34.70	1.350	1.358	1.366
D3		26.5 REF			1.04 REF	
E	37.30	37.50	37.70	1.469*	1.476	1.484
E1		35.56 BSC			1.400 BSC	
E2	34.30	34.50	34.70	1.350	1.358	1.366
E3		26.5 REF			1.043 REF	
e		1.27 BSC			0.050 BSC	
dd	—	—	0.20	—	—	0.008
θ		30° TYPICAL			30° TYPICAL	

Note:

1. Controlling dimension: millimeter

② Primary datum C and seating plane are defined by the spherical crowns of the solder balls.

③ Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.

4. There shall be a minimum clearance of 0.25 mm between the edge of the solder ball and the body edge.

5. Reference document: JEDEC MO-151, BAT-1

Ordering Information

IQ2000 Network Processor P/N VSC2100-xxUQ , where xx: 08 (for 32KBytes memory)
16 (for 64KBytes memory)

Features:

- selectable FOCUS interface configurations of:
  - FOCUS A & B ports as 2 FOCUS16 ports
    with
    FOCUS C & D ports as 1 FOCUS32 port, or 2 FOCUS16 ports
- 32K or 64K bytes of memory

Contact Information

Advanced Network Processor Division

Vitesse Semiconductor Corporation
1820 Lefthand Circle
Longmont, CO 80501-6720
TEL: (303) 651-1000
FAX: (303) 651-1199
Email: anp-sales@vitesse.com
Website: http://www.vitesse.com/platform

Corporate Headquarters

Vitesse Semiconductor Corporation
741 Calle Plano
Camarillo, CA 93012
TEL: (805) 388-3700
(FAX: (805) 986-5896
Email: sales@vitesse.com
Website: http://www.vitesse.com