AAL1GATOR™ PRODUCT FAMILY

TECHNICAL OVERVIEW

PRELIMINARY

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CONTENTS

1 INTRODUCTION

Network infrastructures of telecommunications service providers are evolving, driven by the need for cost-effective deployment and management of new and existing services such as public and private telephony, leased line, Frame Relay and ATM. The carrier's separate voice, leased line and packet networks are transitioning from a large collection of different equipment including Narrowband, Broadband and Wideband Digital Cross Connects, ADMs, ATM and Frame Relay switches towards a single network of ATM Multi-service switches. The net result is twofold. Firstly, the convergence of voice, leased line and packet networks results in reduced total operating costs attributed to lower network management and overall equipment requirements. Secondly, carriers can capitalize on ATM's inherent capabilities of supporting multiple services, guaranteed QoS, bandwidth on demand, scaleability and reliability.

As Digital Cross Connects are upgraded to support ATM or are replaced by ATM Multi-service switches, TDM traffic which includes voice, data and private leased line services must be circuit emulated across the ATM network. The ATM Forum has defined the Circuit Emulation Service (CES) Interoperability Specification to enable the transport of Constant Bit Rate (CBR) voice, data and leased line traffic over ATM networks using the ATM Adaptation Layer 1 (AAL1) protocol.

The AAL1 protocol provides the ability to transfer constant bit rate traffic, timing information and structure information between source and destination. To achieve this AAL1 uses the ATM CBR service category and defines the information payload within each cell to support these capabilities.

Circuit emulation is also used in next generation Customer Premise Equipment (CPE) and Customer Located Equipment (CLE) applications such as in Optical Network Units for ATM Passive Optical Networks (APON) and in Integrated Access Devices (IADs) where TDM traffic, for example from a PBX, is converted into ATM cells.

This technical overview describes how the AAL1gator product family satisfies a wide range of system level requirements for enabling high density ATM CES in Central Office applications and lower density CES in CPE and CLE applications. This document assists designers of communications equipment in understanding and evaluating the AAL1gator devices by answering the following questions:

1. What functions do the AAL1gator products fulfill in the overall system architecture?

2. What are the applications and equipment that the AAL1gator devices are designed for?
3. How the AAL1gator devices interface seamlessly with other PMC devices to provide complete CES designs for rates ranging from T1/E1 to channelized OC-12.

This is a companion document to the following:

- PMC-1981419 – AAL1gator-32 Telecom Standard Product Data Sheet
- PMC-200-0097– AAL1gator-8 Telecom Standard Product Datasheet
- PMC-200-0098– AAL1gator-4 Telecom Standard Product Datasheet
- PMC-1991820– AAL1gator Product Family Programmers Guide

2 AAL1GATOR PRODUCT FAMILY OVERVIEW

The AAL1gator products are highly integrated and flexible monolithic single chip devices that provide DS1, E1, J1, DS3, E3, J2, STS-1 and STM-0 line interface access to an ATM Adaptation Layer 1 (AAL1) Constant Bit Rate (CBR) ATM network. The AAL1gator products enable a variety of circuit emulation services, ranging from structured DS1/E1/J1 for carrying voice traffic, unstructured DS1/E1/J2 for private line consolidation to unstructured DS3/E3/J2/STS-1/STM-0.

The AAL1gator product family comprises five products: AAL1gator-I, PM73121 AAL1gator-II, PM73122 AAL1gator-32, PM73123 AAL1gator-8 and PM73124 AAL1gator-4 as shown in Figure 1.

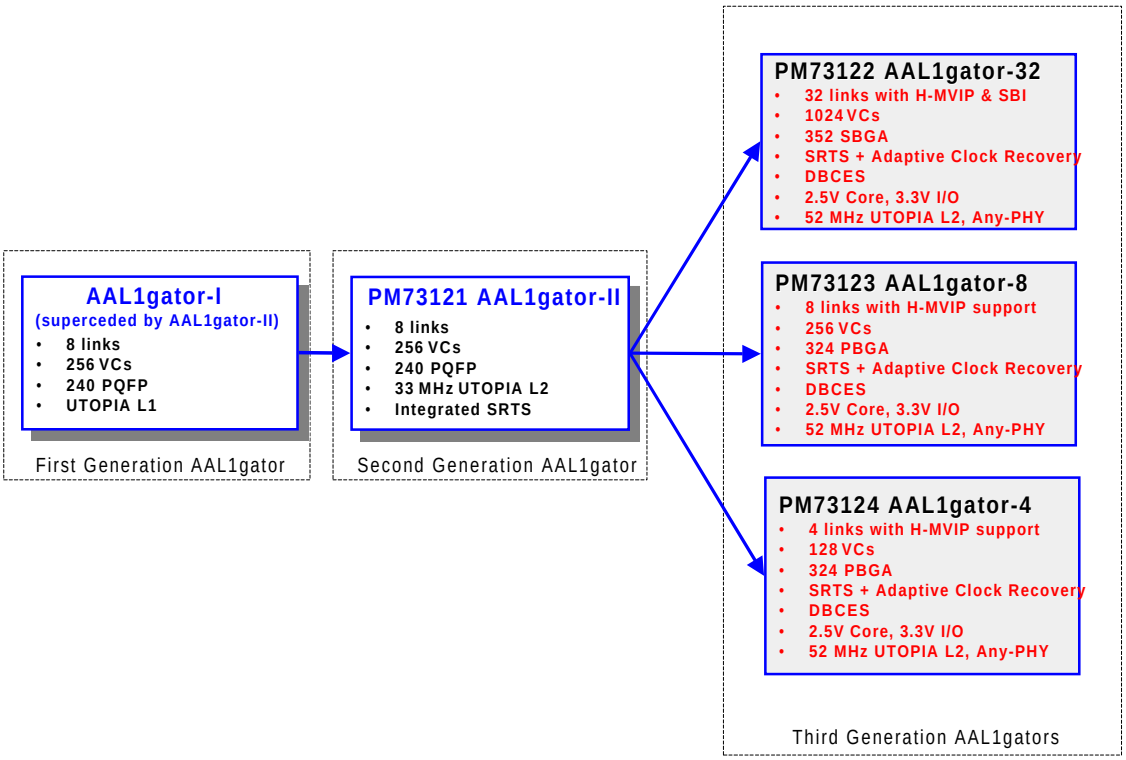

Figure 1. AAL1gator Product Family.

2.1 AAL1gator-I and AAL1gator-II

The AAL1gator-I and PM73121 AAL1gator-II, provide circuit emulation of eight T1/E1 links or a single DS3/E3 link over an ATM network. The AAL1gator-II is the second generation AAL1gator device and supercedes the AAL1gator-I with

key enhancements such as increased UTOPIA L2 bandwidth from 25 MHz to 33 MHz and integrated SRTS timing recovery. For a complete list of enhancements see the AAL1gator-II datasheet.

A typical T1/E1 channelized DS3 design using the AAL1gator-II is shown on the left side of Figure 2. The AAL1gator-II design comprises a DS3 Line Interface Unit (LIU), an M13 multiplexer such as PMC's PM8313 D3MX, 28 T1 Framers implemented as seven PMC PM4344 TQUADs and four AAL1gator-IIs. This design provides transport of 28 T1s over ATM.

However, as carriers migrate more and more TDM traffic onto their ATM backbones, the demand for circuit emulation services is driving networking equipment architects to design next generation systems with:

- higher link density for accommodating more TDM traffic per port card
- lower power per link
- Dynamic Bandwidth CES (DBCES) which reduces network bandwidth through intelligent suppression of ATM cell transmission when TDM links are idle. The freed up bandwidth from the idle channels can be used by other traffic classes such as Available Bit Rate (ABR) and Unspecified Bit Rate (UBR).

PMC-Sierra introduces the third generation AAL1gator products, PM73122 AAL1gator-32, PM73123 AAL1gator-8 and PM73124 AAL1gator-4 to address these new requirements.

2.2 AAL1gator-32

The AAL1gator-32 enables the design of low power, high density, DBCES-capable circuit emulation port cards for a wide range of network equipment including ATM Multi-service switches and Digital Cross Connects. The AAL1gator-32 in combination with the PM8315 TEMUX provides over four times the density as compared to previous channelized DS3 designs as illustrated in Figure 2.

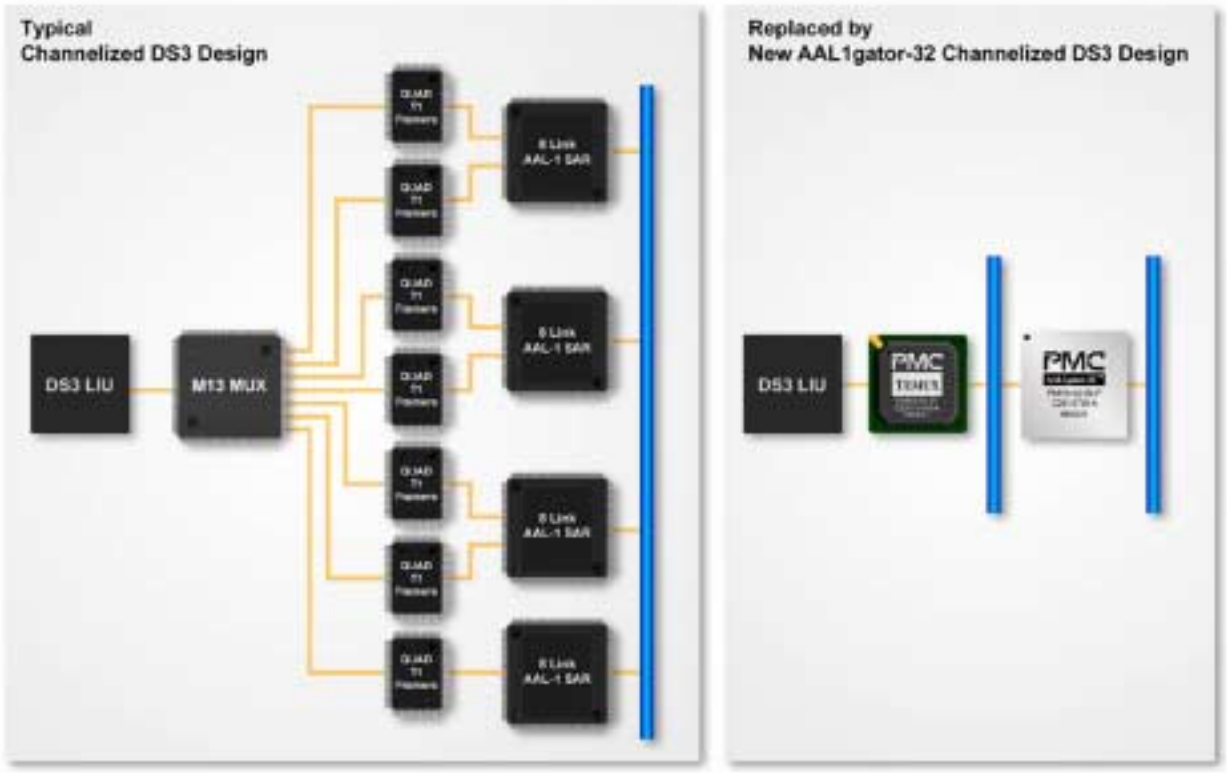

Figure 2. Channelized DS3 Design Comparing the AAL1gator-II with the AAL1gator-32 / TEMUX.

The TEMUX integrates a DS3 Framer, M13 Multiplexer and 28 T1/E1 Framers. Each of the 28 clock, sync, signaling and data signals is communicated to the AAL1gator-32 across the Scalable Bandwidth Interconnect (SBI™) bus. The SBI bus is an 8-bit, 19.44 MHz time-division multiplexed bus capable of transferring both synchronous and asynchronous data up to OC-3 rates. Over the SBI bus, each of the 28 clock signals can be completely independent or common.

The AAL1gator-32 provides AAL1 CES/DBCES processing for up to 32 DS1/E1 links; in this example 28 DS1 links are processed. Each DS1 link can be independently configured as either unstructured or structured, with or without CAS and with or without DBCES. On the ATM side of the AAL1gator-32 device, a UTOPIA / Any-PHY interface is used to interconnect to an ATM Physical Layer chip, Traffic Management device or other ATM component.

The two-chip AAL1gator-32 / TEMUX design in Figure 2 replaces twelve individual components providing lower power per link, lower cost per link and a significant savings in board space. With the reduction in board space and power, the optimized AAL1gator-32 / TEMUX solution enables a new generation of high

density circuit emulation port cards such as channelized OC-3 and OC-12 as shown in Figure 3 and Figure 4.

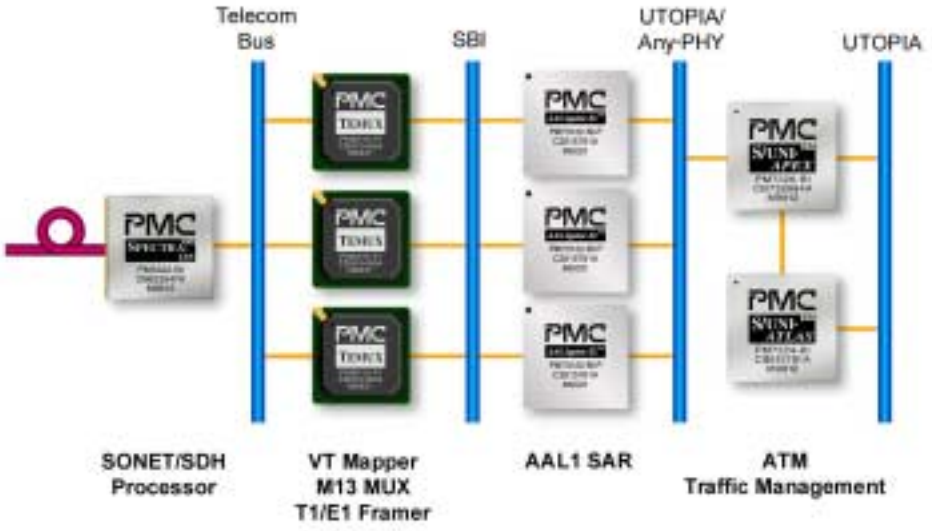

Figure 3. T1/E1 Channelized OC-3 Application.

For the T1/E1 channelized OC-3 application shown in Figure 3 a PM5342 SPECTRA-155 provides SONET/SDH overhead processing at the OC-3 rate of 155.52 Mbps. The Telecom Bus which is an 8-bit parallel bus running at 19.44 MHz interface is used to directly interface the SPECTRA-155 to the TEMUX. The TEMUX provides a VT/TU Mapper in addition to the DS3 Framer, M13 Multiplexer and T1/E1 Framers. In this example three TEMUXs, configured in VT mapper mode, and three AAL1gator-32s share a common SBI bus to support 84 T1 links.

In this example, the ATM side of each AAL1gator-32 is configured for either UTOPIA Level 2 or Any-PHY for interconnecting to the PM7326 S/UNI-APEX ATM Traffic Manager and Switch device. The PM7324 S/UNI-ATLAS performs policing and address translation functions.

With the densities afforded by the AAL1gator-32 and TEMUX devices a single port card can provide an OC-12 worth of T1 links (336 T1 links) as shown in Figure 4. In this example the PM5313 SPECTRA-622 provides SONET/SDH overhead processing at the OC-12 rate of 622 Mbps. As the Telecom and SBI Buses support OC-3 rates, separate buses are required to interconnect each of four groups of three TEMUX and AAL1gator-32 devices.

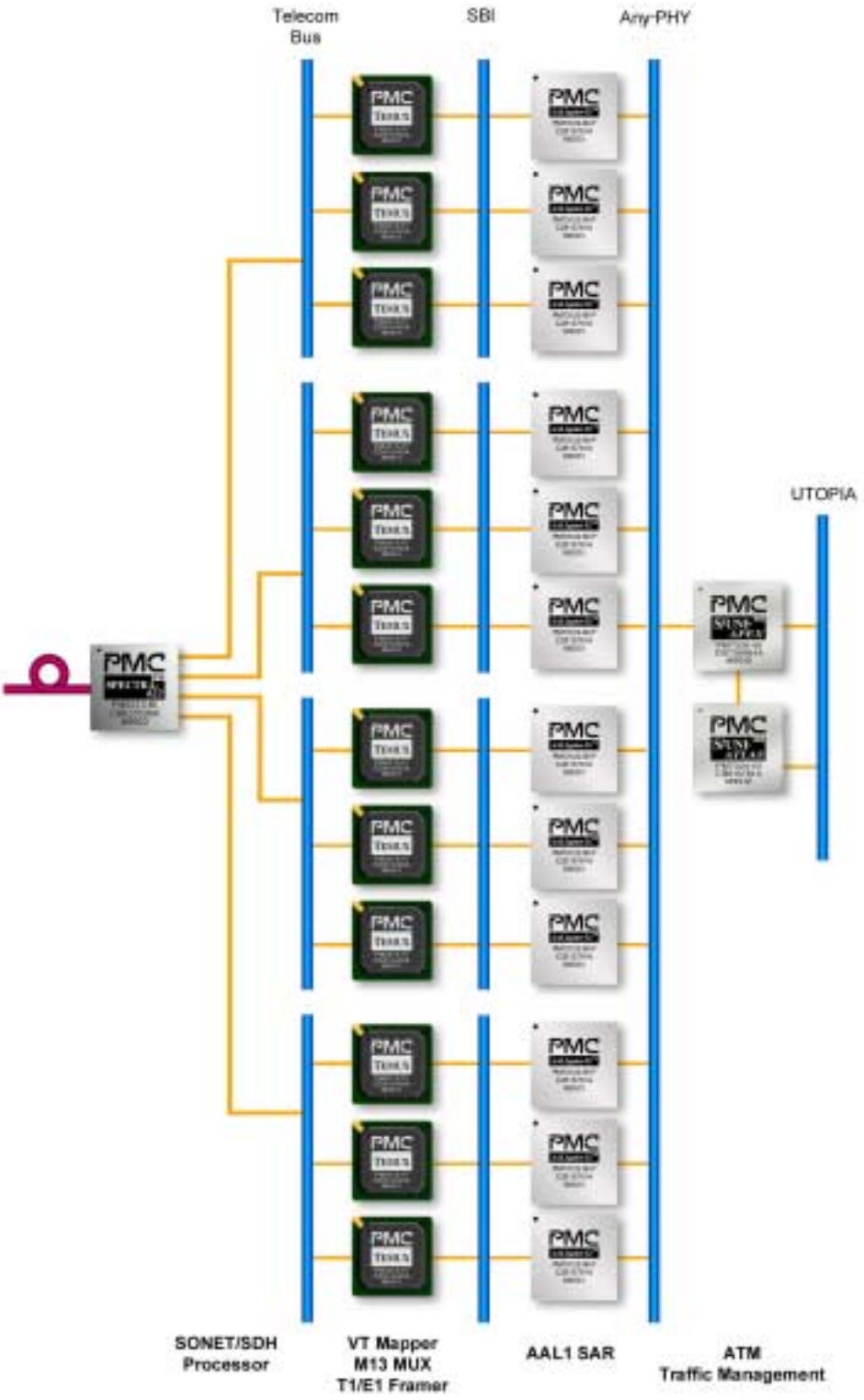

Figure 4. T1/E1 Channelized OC-12 Application.

In addition to providing high link density, the AAL1gator-32 provides significantly lower power per link than previous solutions.

2.3 AAL1gator-8 and AAL1gator-4

The other two new members of the AAL1gator family, the AAL1gator-8 and AAL1gator-4, address CPE and CLE applications where support for a small number of links is required. The AAL1gator-8 and AAL1gator-4 provide low power, DBCES-capable, eight and four link circuit emulation, respectively, for applications such as Integrated Access Devices (IADs), ATM Multi-service Access Switches, Optical Networking Units and base stations in wireless networks.

Like the AAL1gator-II, the AAL1gator-8 provides circuit emulation of eight DS1/E1 links or a single DS3/E3 link; key enhancements provided by the AAL1gator-8 over the AAL1gator-II include:

- Lower power: AAL1gator-8 has 2.5V with 3.3V, 5V tolerant I/O
- DBCES support
- Both SRTS and Adaptive Clock recovery modes are supported internally for T1/E1 rates
- Robust Sequence Number Processing
- Increased UTOPIA L2 bandwidth from 33 MHz to 52 MHz with parity support
- UTOPIA loopback support
- Support for 2 H-MVIP lines
- Support for unstructured STS-1/STM-0 over ATM
- The RAM interface is now decoupled from the microprocessor interface for ease of system design
- Improved OAM cell processing, interrupt processing and DS3 AIS support

The AAL1gator-4, pin-compatible with the AAL1gator-8, supports four DS1/E1 links or a single DS3 /E3 link. The AAL1gator-4 is targeted for low link applications such as Optical Networking Units and base stations in wireless networks.

2.4 AAL1gator Product Family Comparison

Table 1 compares the features of the AAL1gator product family (features are described in later sections of the document). Note that the AAL1gator-32, AAL1gator-8 and AAL1gator-4 are recommended for new designs over the AAL1gator-II.

Feature	AAL1gator-32	AAL1gator-8	AAL1gator-4	AAL1gator-II
VCs Supported	1024	256	128	256
DBCES	Yes	Yes	Yes	No
Internal SRTS & Adaptive Clock Timing Recovery	Yes	Yes	Yes	SRTS only
Sequence Number Processing	Fast and Robust	Fast and Robust	Fast and Robust	Fast
Line Interface				
SBI Mode				
DS1/E1	32	N/A	N/A	N/A
DS3	2	N/A	N/A	N/A
DS3 & 16 DS1/E1 Support	Yes	No	No	No
H-MVIP Mode				
TX / RX Lines	8 / 8	2 / 2	1/ 1	N/A
DS1/E1	32	8	4	N/A
High Speed Mode (AAL1gator-32)				
DS3/E3	2	See Direct Mode	See Direct Mode	See Direct Mode
STS-1/STM-0	2	See Direct Mode	See Direct Mode	See Direct Mode
Direct Low Speed Mode (AAL1gator-32)				
DS1/E1	16	See Direct Mode	See Direct Mode	See Direct Mode
MVIP-90	16	See Direct Mode	See Direct Mode	See Direct Mode
Unstructured J2	6	See Direct Mode	See Direct Mode	See Direct Mode
Direct Mode (AAL1gator-8 and AAL1gator-4)				
DS3/E3	See High Speed Mode	1	1	1
STS-1/STM-0	See High Speed Mode	1	1	1
DS1/E1	See High Speed Mode	8	4	8

MVIP-90	See High Speed Mode	8	4	N/A
Unstructured J2	See High Speed Mode	3	3	N/A
System Side Loopback	Yes	Yes	Yes	No
UTOPIA Interface				
UTOPIA L2	52 MHz 16-bit with parity / Any-PHY Option to respond as a 4-port device.	52 MHz 16-bit with parity / Any-PHY Responds as a single port device only.	52 MHz 16-bit with parity / Any-PHY Responds as a single port device only.	33 MHz
General				
RAM	Two 256k x 16 (18) 10 ns Synchronous SRAM or ZBT RAM	One 128k x 16 (18) 10 ns Synchronous SRAM or ZBT RAM	One 128k x 16 (18) 10 ns Synchronous SRAM or ZBT RAM	128kx 16 SRAM
Supply Voltage	2.5V core 3.3V I/O	2.5V core 3.3V I/O	2.5V core 3.3V I/O	5V
Power, Typical, Max	1.7W typical 2.3W max: • 0.5W (3.3V) • 1.8W (2.5V)	0.75W typical 1W max: • 0.4W (3.3V) • 0.6W (2.5V)	0.75W typical 1W max: • 0.4W (3.3V) • 0.6W (2.5V)	2.15W typical 2.53W max
Package Type & Size	352 SBGA (35mm x 35mm)	324 PBGA (23 mm x 23mm)	324 PBGA (23 mm x 23mm)	240 PQFP (32mm x 32mm)

Table 1. AAL1gator Product Family Comparison.

3 SYSTEM APPLICATIONS

The AAL1gator products have been optimized for various applications. The high link density of the AAL1gator-32 makes it ideal for Central Office applications such as ATM Multi-service Switches, DACS and Optical Line Termination units for ATM Passive Optical Networks (APON).

Using the AAL1gator-8 and AAL1gator-4 with T1/E1 framers and integrated LIUs such as the PM4351 COMET, enables ATM transport of up to 8 and 4 T1/E1 circuits, respectively, for applications such as Integrated Access Devices (IADs), ATM Multi-service Access Switches, Optical Networking Units and base stations in wireless networks. Table 2 summarizes the various system applications where the AAL1gator devices are used.

AAL1gator Application	AAL1gator-32	AAL1gator-8	AAL1gator-4
ATM Multi-service Switch	√	√	
DACS with an ATM Interface	√	√	
Access Service Concentrator	√	√	
Unstructured DS3/E3/STS-1/STM-0 over ATM	√	√	
Optical Line Termination (OLT) Unit in an ATM Passive Optical Network (APON)	√		
Integrated Access Device (IAD), PBX		√	√
Optical Network Unit (ONU) in APON			√
LMDS			√

Table 2. AAL1gator System Applications.

3.1 ATM Multi-service Switch

An ATM Multi-service Switch is typically located at the edge of the wide area network. It interfaces to Frame Relay, ATM as well as TDM services and consolidates these different services to ATM cells for transport over a single high-bandwidth ATM core network.

Figure 5 shows a reference design that uses PMC's SPECTRA-155, TEMUX, FREEDM-84A672 and AAL1gator-32 in a multi-service port adapter design that supports channelized DS3 and channelized OC-3 densities.

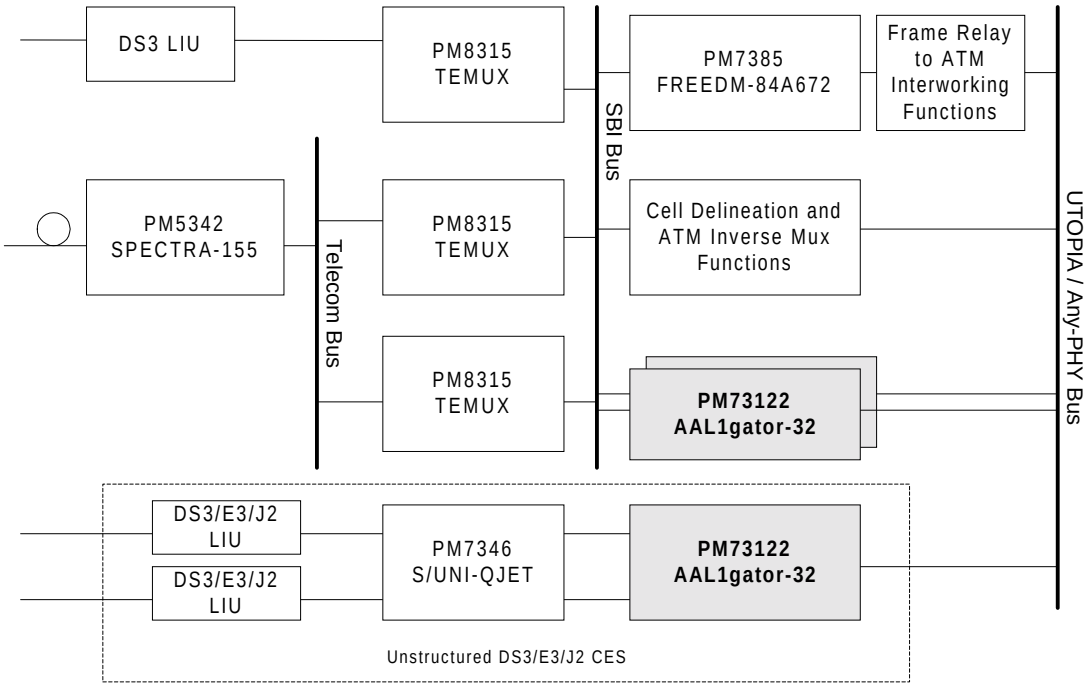

Figure 5. Multi-service Switch Application

3.2 Digital Access Cross Connect (DACS)

Narrowband, wideband or broadband Digital Access Cross Connects (DACS) that need to support ATM uplink interfaces to a core ATM switch can use one or more AAL1gator-32s to emulate a TDM service over an ATM network. DACs with CES capabilities allow service providers to consolidate legacy private line services onto a high speed ATM backbone network and reduce the number of network elements and physical connections that need to be managed. Figure 6 shows the AAL1gator-32 in a DACS application.

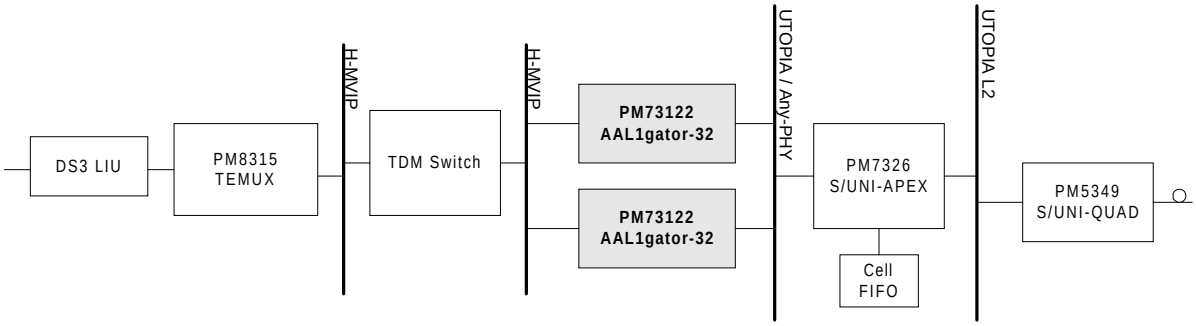

Figure 6. Using the AAL1gator-32 in a DACS application.

3.3 Integrated Access Device

An Integrated Access Device (IAD) consolidates voice, data, Internet, and video wide-area network services using ATM over shared T1/E1 lines. IADs can also unify the functions of many different types of equipment including CSUs, DSUs and multiplexers. Figure 7 shows the AAL1gator-4 connected to four PM4351 COMETs, a PM7326 S/UNI-APEX Traffic Manager, an Inverse Multiplexing over ATM device, the PM7344 S/UNI-MPH and eight PM4351 COMETs for the WAN uplink.

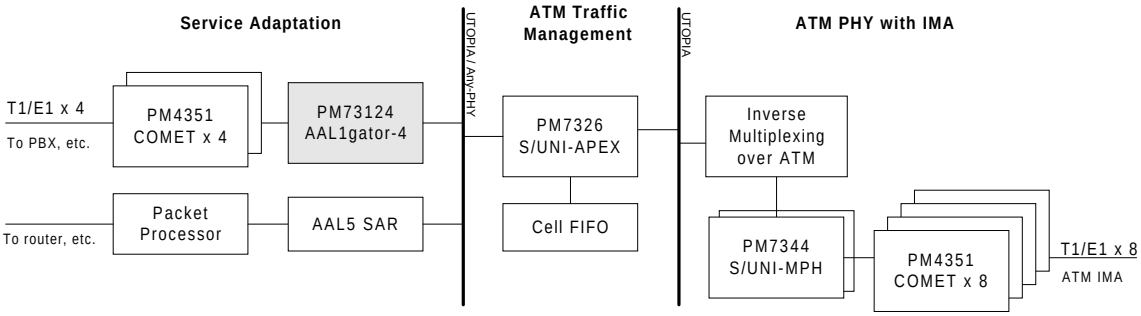

Figure 7. Using the AAL1gator-4 in an Integrated Access Device (IAD) Application.

4 DEVICE SELECTION CRITERIA

The third generation AAL1gator devices, AAL1gator-32, AAL1gator-8 and AAL1gator-4, provide a very flexible and configurable line interface. The line interface is configured through hardware pins to operate in one of the following modes:

- Scaleable Bandwidth Interconnect (SBI™) (AAL1gator-32 only)
- High Speed Multi-Vendor Integration Protocol (H-MVIP)
- High Speed Mode (AAL1gator-32 only)
- Direct Low Speed (AAL1gator-32 only)
- Direct Mode (AAL1gator-8 and AAL1gator-4 only)

These line interface modes are described in Section 5 - AAL1gator-32 Device Overview and Section 6 - AAL1gator-8 / AAL1gator-4 Device Overview. This section is intended to aid in the selection of the appropriate AAL1gator device and its line interface mode of operation.

In the first column of Table 3 various line interface type and density requirements are listed. The following three columns describe, for each AAL1gator device, whether or not the line interface requirement is supported, the possible line interface modes of operation or a recommendation to use a different AAL1gator device. Note that third generation AAL1gator devices are recommended for new designs over the AAL1gator-II.

Line Interface Type and Density Requirements	AAL1gator-32, Line Interface Mode	AAL1gator-8, Line Interface Mode	AAL1gator-4, Line Interface Mode
32 DS1/E1 Where each link can be individually configured for: • Basic Service (no CAS) or Service with CAS • Unstructured or Structured (H-MVIP supports structured mode only) • Synchronous, SRTS or Adaptive Timing Recovery • Independent or common clock	• SBI • H-MVIP (structured service only) • Direct Low Speed (Two AAL1gator-32 devices req'd)	Not Supported	Not Supported

16 or 8 DS1/E1	AAL1gator-32 for 16 DS1/E1: • Direct Low Speed Mode (Clk/Data) • SBI • H-MVIP (structured service only)	AAL1gator-8 for 8 DS1/E1: • Direct Mode • H-MVIP (structured service only)	Use AAL1gator-32 or AAL1gator-8
4 DS1/E1	Use AAL1gator-4	Use AAL1gator-4	• Direct Mode • H-MVIP (structured service only)
Dual DS3 Unstructured	• SBI • High Speed Mode	• Two AAL1gator-8 devices in Direct Mode	• Two AAL1gator-4 devices in Direct Mode
Dual E3 Unstructured	• High Speed Mode	• Two AAL1gator-8 devices in Direct Mode	• Two AAL1gator-4 devices in Direct Mode
Single DS3 /E3 Unstructured	• High Speed Mode or use AAL1gator-8	• Direct Mode	• Direct Mode
Single DS3 Unstructured & 16 DS1/E1	• SBI	Not Supported	Not Supported
Dual STS-1/STM-0 Unstructured	• Dual High Speed Mode	• Two AAL1gator-8 devices in Direct Mode	• Two AAL1gator-4 devices in Direct Mode
Single STS-1/STM-0 Unstructured	• High Speed Mode or use AAL1gator-8	• Direct Mode	• Direct Mode
J2 Unstructured	• Direct Low Speed Mode • 6 J2 links	• Direct Mode • 3 J2 links	• Direct Mode • 3 J2 links

Table 3. Recommended AAL1gator Device and Line Interface Mode of Operation.

5 AAL1GATOR-32 DEVICE OVERVIEW

The AAL1gator-32 is available in a 352-pin SBGA 35mm x 35mm package. It internally comprises four AAL1 SAR Processors (A1SPs), a UTOPIA / Any-PHY Interface, Line Interface, Processor Interface, External Clock Interface, JTAG Interface, RAM Interfaces and a Clock MUX as shown in Figure 8,

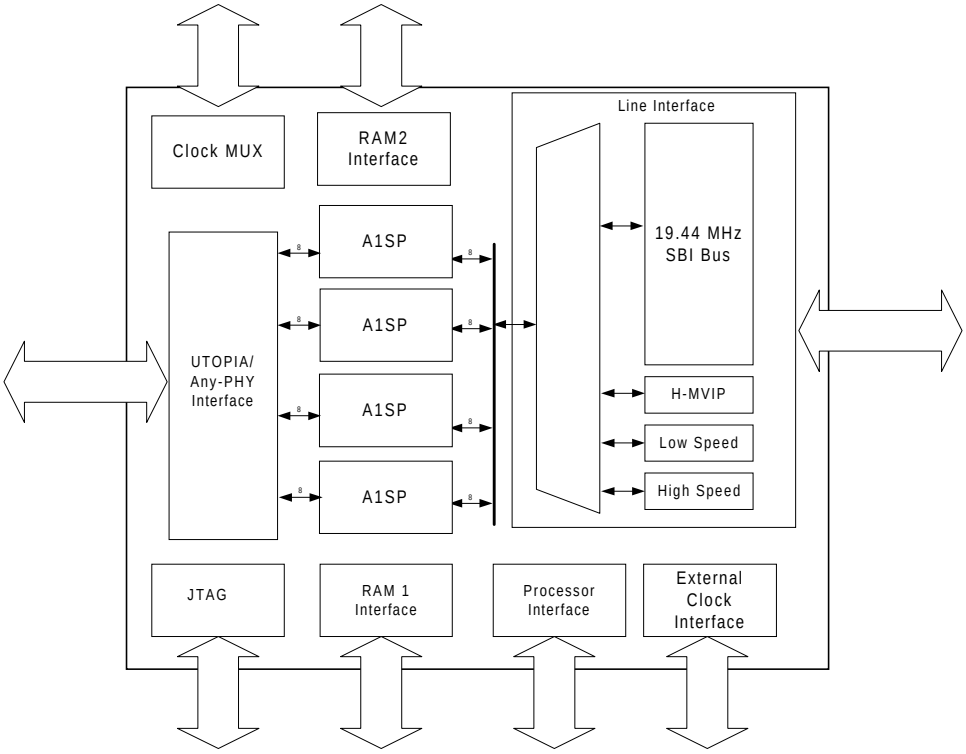

Figure 8. AAL1gator-32 Block Diagram.

The A1SP blocks interface to a UTOPIA / Any-PHY interface on one side and a flexible Line Interface on the other. The upper two A1SP blocks share the RAM2 Interface while the lower two A1SP blocks share the RAM1 Interface.

The Processor Interface is provided for the purposes of device configuration, supporting AAL1, AAL0, AAL5, OAM cells, loopback modes, interrupt processing and management functions such as retrieving MIB variables, performance monitoring and alarm detection and indication.

The Clock MUX and External Clock Interface provide the clock signals for system, line interface and timing recovery modes.

Each functional block is described in more detail in the following subsections. The first three subsections describe the Line Interface, A1SP and UTOPIA / Any-PHY Interface blocks of the AAL1gator-32 (shaded blocks at top of Figure 9) and how these blocks implement the CES/DBCES functions. The functions performed by these blocks are shown from a layering perspective at the bottom of Figure 9.

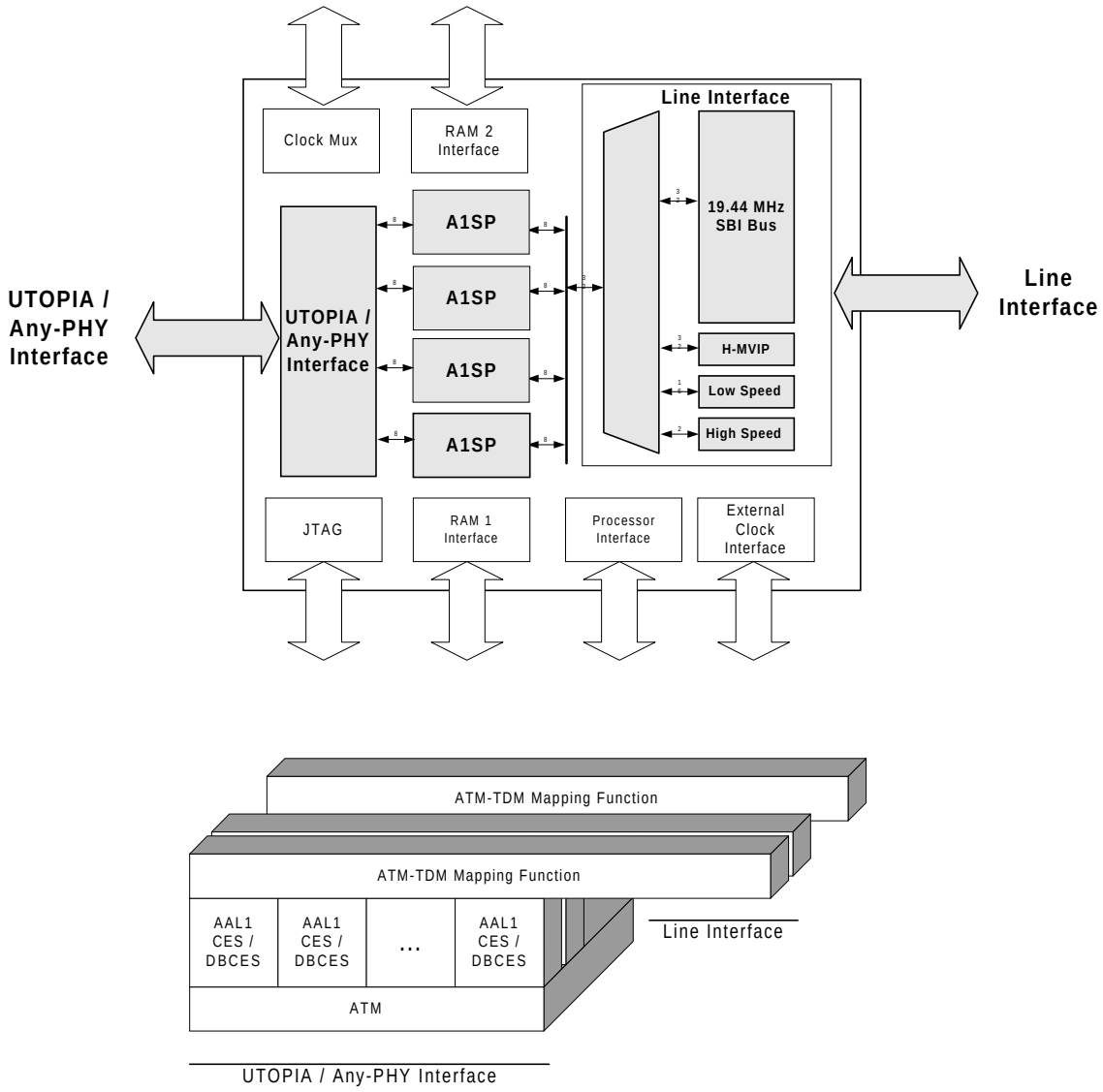

Figure 9. AAL1gator-32 CES/DBCES Functions – Layering Perspective.

5.1 Line Interface

The AAL1gator-32 provides a very flexible and configurable line interface. Depending on the system application, the AAL1gator-32 is configured through hardware pins to operate in one of the following Line Interface modes:

- Scaleable Bandwidth Interconnect (SBI™)
- High Speed Multi-Vendor Integration Protocol (H-MVIP)
- High Speed
- Direct Low Speed

Figure 10 illustrates, at a block level, the Line Interface modes of operation (further described in Sections 5.1.1 to 5.1.4) for interconnecting to a wide range of standard T1, E1, T3, E3 and J2 framers.

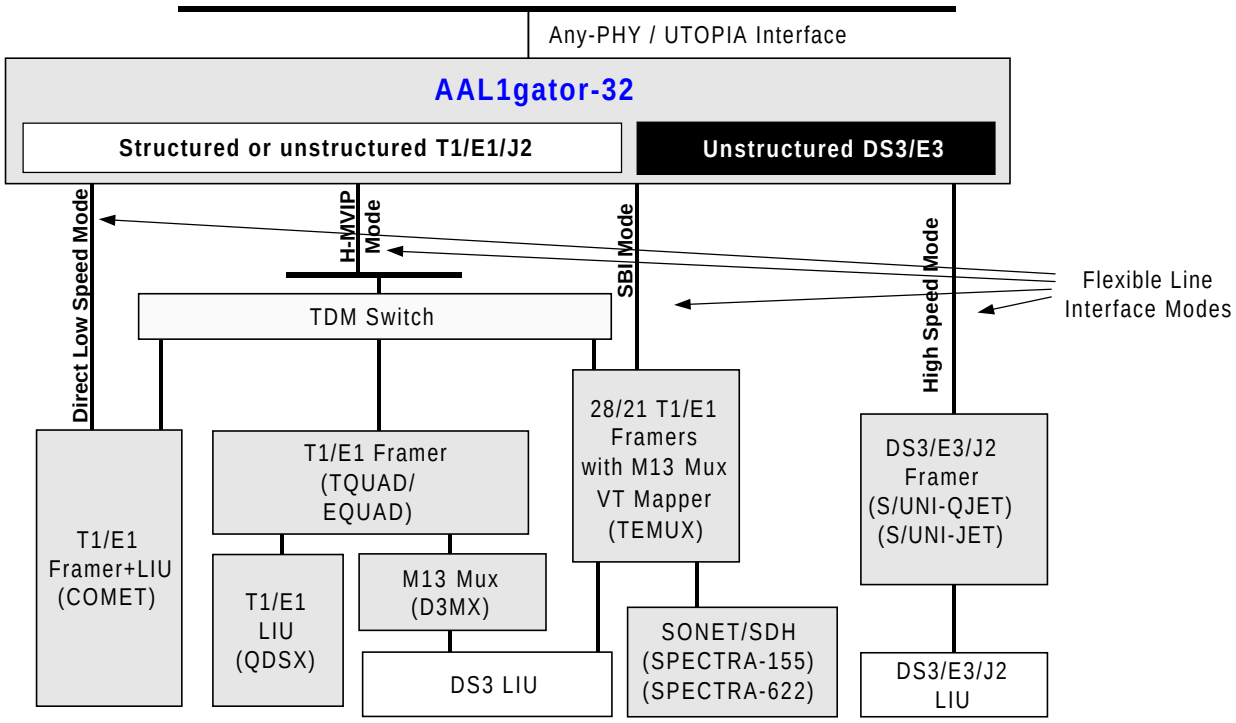

Figure 10. AAL1gator's Flexible Modes of Operation – Line Interface and UTOPIA / Any-PHY.

5.1.1 Scaleable Bandwidth Interconnect (SBI™) Line Interface Mode

The Scaleable Bandwidth Interconnect (SBI) bus is an 8-bit time-division multiplexed bus designed to efficiently and seamlessly interconnect several multi-port Layer 2 devices such as the AAL1gator-32 to multiple high density Layer 1 framers such as the PM8315 TEMUX[1]. The maximum number of devices sharing the bus is limited only by the need to meet AC timing requirements. The SBI bus operates at a 19.44 MHz clock rate and is capable of transferring both synchronous and asynchronous data up to OC-3 rates. The data format on the data bus allows for compensating between clock differences on the PHY, SBI and Line Interface links. This is achieved by floating data structures within the SBI format.

The time division multiplexed SBI bus uses the SONET/SDH virtual tributary structure to carry T1 links and E1 links. Unchannelized DS3 payloads follow a byte synchronous structure modeled on the SONET/SDH format.

The interfaces that are supported over the SBI bus are varied over a wide range of rates and requirements. Table 4 summarizes the links that are supported by the AAL1gator-32 over the SBI bus. The AAL1gator can switch links from one of a total of three Synchronous Payload Envelopes (SPEs) to another so all the links being processed by the AAL1gator do not have to reside within the same SPE. However all links processed by either the upper 16 links or lower 16 links of the AAL1gator-32 have to be of the same type (i.e. T1, E1, DS3).

Link	Mapping	Timing Method	Links
DS3	Unchannelized DS3	Floating Payload	2
E1	Byte Synchronous	Floating Payload or Locked Payload	32
T1	Byte Synchronous	Floating Payload or Locked Payload	32

Table 4. Supported links over SBI.

The AAL1gator-32, in SBI mode, is configured through software to support one of the following combinations of links:

- 32 DS1/E1 links (see 5.1.1)

[1] The PM8315 TEMUX device integrates 28 T1/E1 framers, an M13 Multiplexer and a VT/TU Mapper and uses the SBI bus to interface seamlessly to the AAL1gator-32.

- Dual Unstructured DS3 Service, or
- Single Unstructured DS3 Service and 16 DS1/E1 links

Each DS1/E1 link can be individually configured for:

- Basic Service (no CAS) or Service with CAS
- Unstructured or Structured
- Synchronous, SRTS or Adaptive Timing Recovery
- Independent or common clock

5.1.2 High Speed Multi-Vendor Integration Protocol (H-MVIP) Line Interface Mode

The High Speed Multi-Vendor Integration Protocol (H-MVIP) bus provides synchronous, time-division multiplexed transport of N x 64 kbps constant bit rate (CBR) data streams. The H-MVIP bus consists of a group of related clock signals and serial data streams which operate at 8 Mbps [6].

When configured in H-MVIP Line Interface Mode, the AAL1gator can be interconnected to devices such as Time-Slot Interchangers (TSI) that support the H-MVIP interface as shown in Figure 11. Note that the MVIP-90 standard is supported in Direct Low Speed Mode as described in Section 5.1.4.

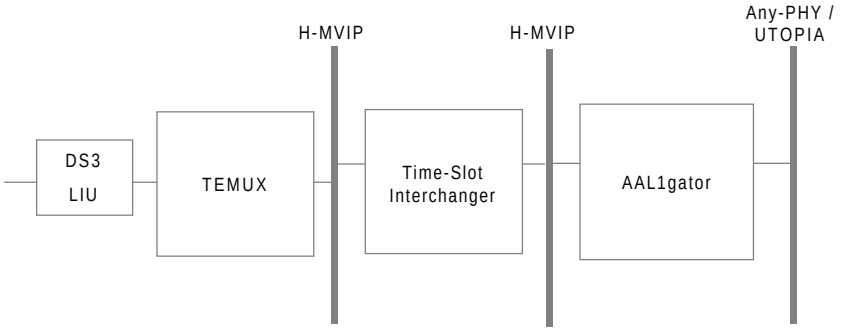

Figure 11. AAL1gator-32 Configured in H-MVIP Line Interface Mode.

In the line interface-to-ATM direction, each Rx H-MVIP line receives an incoming 8 Mbps H-MVIP data stream. Internally to the chip the 8 Mbps stream is separated into four 2 Mbps streams. In the ATM-to-line interface direction the 64 kbps timeslots within a group of four 2 Mbps streams are combined and output onto the Tx H-MVIP lines.

By mapping a J2 frame into an H-MVIP frame, the AAL1gator-32 can circuit emulate individual N x 64 kbps timeslots or groups of timeslots.

5.1.3 High Speed Line Interface Mode

The High Speed Line Interface comprises Transmit Clock and Data pins and Receive Clock and Data pins used to interface to high speed clear channel, unstructured data streams. Timing recovery is supported externally. The AAL1gator's External Clock Interface outputs various signals including SRTS and Adaptive Clock status values.

5.1.3.1 DS3 / E3 / STS-1 / STM-0 Links

When configured in High Speed Mode, the AAL1gator-32 supports two DS3, E3, STS-1 or STM-0 links using the Clock and Data interface. Figure 12 is an example of the AAL1gator-32 used in a dual unstructured DS3 application.

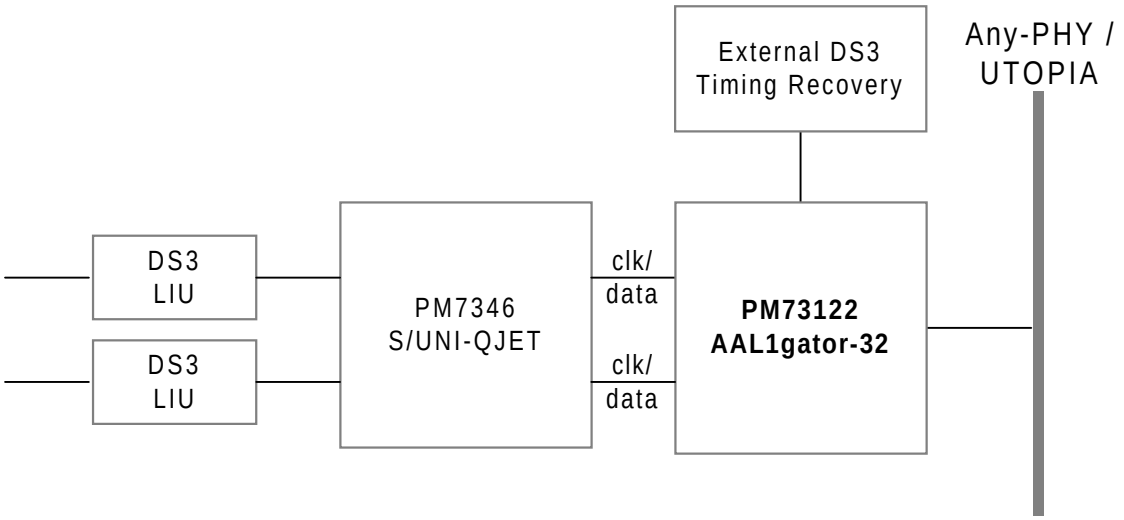

Figure 12. High Speed Line Interface Mode.

5.1.4 Direct Low Speed Line Interface Mode

Direct Low Speed Mode is used for interconnecting to standard T1 or E1 Framers and to devices which support the MVIP-90 protocol.

5.1.4.1 DS1 / E1 Links

When configured in Direct Low Speed Mode, the AAL1gator-32 supports sixteen DS1/E1 links where each link interface comprises a clock, data, frame pulse, and signaling pin for each direction. In addition low speed clear channel data streams can be passed in this mode. A common clock pin is also available, which can be shared across all receive lines or all transmit lines and is selectable on a per line basis. Figure 13 shows an example of the AAL1gator-32 supporting sixteen T1 links.

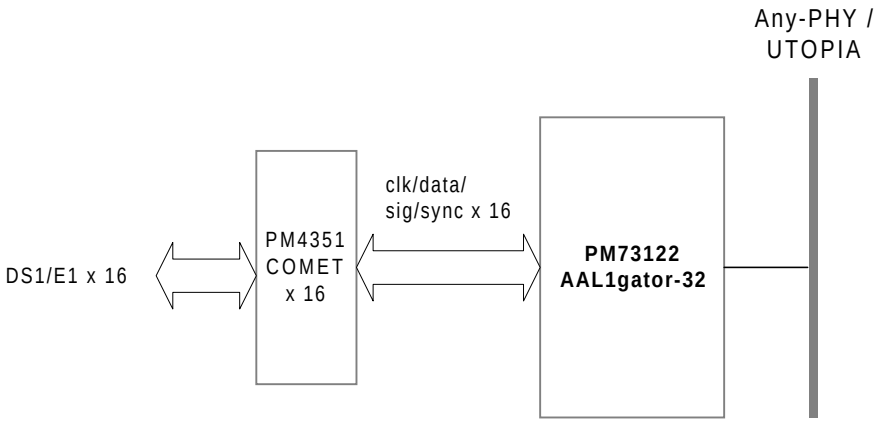

Figure 13. Direct Low Speed Line Interface Mode.

Some framers also share a clock and signaling pin, where the clock pin becomes a signaling pin when signaling is required or remains as a clock pin when individual clocks per line are required. When this pin carries signaling information a common clock is used, which is shared across all lines. This option can be configured on a per line basis.

5.1.4.2 MVIP-90

2 Mbps MVIP mode is also supported where the line is handled in accordance with the MVIP-90 specification. MVIP mode can be individually selected per line for all lines. Tri-stating of individual time slots is not supported. There is a common 4 MHz clock and a common framing reference signal.

5.1.4.3 Unstructured J2

Using the clock and data pins in Direct Low Speed Mode, the AAL1gator-32 devices support unstructured J2 transport over ATM. The AAL1gator-32 supports up to six unstructured J2.

5.2 UTOPIA / Any-PHY Interface

The following modes are supported by the AAL1gator-32 devices:

- UTOPIA Level 1 PHY, Master (8-bit only) and Slave (8 or 16-bit)
- UTOPIA Level 2 MPHY
- Any-PHY

Both 8-bit and 16-bit UTOPIA interfaces with an optional single parity bit are supported. Each direction can be configured independently and has its own configuration registers.

5.2.1 UTOPIA Level 1

UTOPIA Level 1 defines the interface between the Physical Layer (PHY) and upper layers such as the ATM Layer and various management entities. The definition allows a common PHY interface in ATM subsystems across a wide range of speeds and media types up to OC-3c rates (155 Mbps). UTOPIA Level 1 has the restriction that only one PHY device can be supported [4].

The AAL1gator-32 devices can be configured as an 8-bit UTOPIA Level 1 Master or 8-bit or 16-bit UTOPIA Level 1 Slave.

5.2.2 UTOPIA Level 2

UTOPIA Level 2 enhances UTOPIA Level 1 by defining the physical operation of the interface to support up to 31 PHY devices with an aggregate data rate of up to 622 Mbps [5]. With the AAL1gator-32 in UTOPIA Level 2 mode, the UTOPIA interface can be configured to respond as a single port device or as a four-port device. The UTOPIA Level 2 interface is a 16-bit interface and operates at up to 52 MHz.

5.2.2.1 Four-Port Device Configuration

In the ATM-to-Line Interface direction of the AAL1gator's UTOPIA interface, a four cell deep UTOPIA FIFO is used to buffer cells for delivery to the internal

AAL1 processors. In addition, each AAL1 processor is preceded with an eight cell deep AAL1 PROCESSOR FIFO.

During normal operation there may be situations where cell streams targetted to a given internal AAL1 processer may be clumped together. If the AAL1 PROCESSOR FIFO backs up into the UTOPIA FIFO, then a head-of-line blocking problem can exist (i.e. cells targetted to other AAL1 processors are blocked because of the full condition of the UTOPIA FIFO). To alleviate such a situation, the ATM-to-Line Interface direction can be configured as four separate addresses, where the bottom two bits of the address indicate which of the four internal AAL1 processors is targeted to receive the cell. When polling any of the AAL1 processor addresses, a full indication will be given when any of the AAL1 PROCESSOR FIFOs reaches a half full state (room for four more cells). This will always allow room for any cells that may still be queued in the four cell FIFO and thus head-of-line blocking is prevented.

5.2.3 Any-PHY

PMC-Sierra developed the Any-PHY interface - a high bandwidth, low latency system bus interface modeled after the popular POS-PHY interface. The Any-PHY interface is a 16-bit, 52 MHz bus that can support over 800 Mbps of raw bandwidth. By using very few overhead cycles to transmit and receive packets the Any-PHY interface is suitable for designs that need to scale up to OC-12 (622 Mbps) bandwidths. Like POS-PHY and UTOPIA bus interfaces, the Any-PHY interface is a master/slave bus. An Any-PHY bus master can interface with multiple devices.

The Any-PHY interface extends beyond the 31 PHY device limit of UTOPIA Level 2 through the use of in-band addressing. One extra word indicating the port address, is prepended to the front of each cell that is transmitted.

Figure 4 is an example of a T1/E1 Channelized OC-12 application where a single Any-PHY bus is used to interconnect twelve AAL1gator-32s to an ATM Traffic Manager device such as the PM7326 S/UNI-APEX.

5.3 AAL1 SAR Processor (A1SP)

The A1SP blocks provide the processing for the following services compliant to ATM Forum's AF-VTOA-0078 Circuit Emulation Service (CES) specification:

- Structured DS1/E1 Nx64 kbps Basic Service and Service with CAS,

- Unstructured DS1/E1/J2 Service with internal or external support for Synchronous Residual Timestamp (SRTS) and Adaptive Clock Timing Recovery
- Unstructured DS3 /E3 Service,

These services are described in detail in AF-VTOA-0078 [2]. The A1SP blocks also support:

- STS-1/STM-0 unstructured data transfer (AAL1gator-32, AAL1gator-8 only) as described in Section 5.1.3.1
- Dynamic Bandwidth Circuit Emulation Service (DBCES),
- Partially Filled Cells
- Support for AAL0, AAL5 and OAM Cells.

5.3.1 Dynamic Bandwidth Circuit Emulation Service

The AAL1gator devices are compliant to ATM Forum's Dynamic Bandwidth Circuit Emulation Service (DBCES) specification AF-VTOA-0085 which specifies a method for enabling dynamic bandwidth utilization in an ATM network based on detecting which time slots of a given TDM trunk are active and which are inactive. When an inactive state is detected in a specific time slot, the time slot is dropped from the next ATM structure and the bandwidth it was using may be reutilized for other services.

The AAL1gator devices support the following methods for detecting time slot activity/inactivity on a per-channel basis:

- CAS Idle Detection
- Out of Band Signaling Idle Detection (Processor Controlled)
- Pattern Match Idle Detection

5.3.1.1 CAS Idle Detection

CAS Idle Detection looks at the ABCD bits in both the receive and transmit directions on a per-channel basis and compares them to values in registers which are programmed by an external processor. If two consecutive CAS values match in both the receive and transmit directions the channel is considered to be idle.

5.3.1.2 Out of Band Signaling Idle Detection

With Out of Band Signaling Idle Detection, it is the responsibility of the processor to add or drop channels. This method can be used in conjunction with common channel signaling (CCS) or if the processor makes its own determination of channel activity based on the CAS bits.

5.3.1.3 Pattern Match Idle Detection

Pattern Match Idle Detection compares the received byte with a programmed pattern and a mask. If there is a mismatch of received data with the programmed pattern during a programmable length of time, then the channel is considered active. Otherwise, if the received channel bytes match the unmasked pattern bits over the programmable length of time, the channel is considered in an idle state and cell transmission will be suppressed.

Interval length refers to the amount of time that the patterns must match for it to be considered a match event. This value is programmed in a Pattern Matching Line Configuration register for the associated line.

5.3.1.4 Non-DBCES Idle Detection

A mode is available on the AAL1gator-32 for completely suppressing all cell transmission when all channels of the nx64 structure format are idle. The method for determining idle channels are the same as for DBCES (Sections 5.3.1.1 through 5.3.1.3). Note that when any one of the channels becomes active the entire structure is transmitted containing the data for the active channel and idle codes for the idle channels.

5.3.2 AAL0

The AAL1gator supports AAL0, selectable on a per VC basis. With AAL0, the entire AAL payload contains data. No AAL1 information (i.e. CSI bit, sequence number, sequence number protection field) is inserted in the first byte of the payload.

5.3.3 AAL5

The AAL1gator provides a transmit buffer which can be used for user-generated cells such as AAL5 cells for ATM signaling as well as for Operations, Administration and Maintenance (OAM) cells. A corresponding receive buffer exists for the reception of AAL5, OAM or non-AAL1 data cells.

5.3.4 OAM Cells

Because OAM cells have higher priority than cells containing data, when an OAM cell transmission is requested, it is sent at the first available opportunity. Therefore care should be taken to ensure that OAM cells do not overwhelm the transmitter resulting in increased CDV (i.e. data cells are starved of adequate opportunities for transmission).

To send an OAM cell, the microprocessor writes OAM cells into one of two dedicated cell buffers followed by setting an appropriate bit in a Command Register. Upon completion of the cell transmission an attention bit is cleared to indicate the completion status. OAM cells can optionally have the 48-byte OAM payload CRC-10 protected.

There are three methods for detecting an incoming OAM cell. The first method uses a data indicator bit (VCI[8]) in the header. The second method uses the customary PTI field. If the data indicator is not set or the Payload Type Indicator (PTI) = 4 to 7, the cell is interpreted as an OAM cell and is stored in a queue. The third method is a special mode used when VPI mapping is used instead of VCI mapping. In this mode, the VCI field is used to detect an OAM cell. If the VCI is less than or equal to 31 then the cell is interpreted as an OAM cell.

When an OAM cell arrives, it is stored in an OAM queue whose head pointer is maintained by an external microprocessor and whose tail pointer is updated by the AAL1gator. A maskable interrupt is generated to inform the external microprocessor of the OAM cell arrival. The AAL1gator-32 also checks the CRC-10 of the cell and records the results.

5.4 External Clock Interface

The External Clock Interface transmits and receives line clock related information that allows the line clocks to be controlled externally. It serves two functions:

- external playout of Adaptive, SRTS, and Channel Status data
- receipt of external frequency select data.

The External Clock Interface block transmits either SRTS, Adaptive, or Channel Status information on a line basis which enables an external decision to made about altering the line clock frequency. The SRTS output data is the difference between the local and remote SRTS nibble. The adaptive output data is the averaged relative buffer depth in units of bytes. If the adaptive weighting is set to 0 this value becomes the raw buffer depth in units of bytes.

The External Clock Interface allows an external source to directly select the line clock frequency from any one of 171 T1 or 240 E1 frequencies centered around the nominal clock rate. For T1 the legal input values are –83 to 88. For E1 the legal input values are –128 to 111. Any values outside of this range will be clamped to these levels. These levels correspond to a +/-200 ppm T1 clock and a +/- 100 ppm E1 clock.

When a link enters or exits underrun, the link status can be output the External Clock Interface. See the datasheets for detailed information.

5.5 Clock Mux

The Clock Mux Interface provides inputs for the Network Clock and, depending on the Line Interface Mode and the individual link configurations, provides line clock inputs and/or outputs.

5.6 RAM Interface

The RAM Interface is the central arbiter for all memory accesses. It provides a priority mechanism that incorporates fairness to satisfy all real-time requirements of the various blocks. All blocks, including the Processor Interface block, that request a data transfer with the common memory supply the address, control signals and, for write operations, the data. When the RAM Interface actually grants the transfer, it provides a grant signal to the requesting block, indicating that the transfer has been performed. The memory is arbitrated on a cycle-by-cycle basis. No device is granted the bus for an indefinite time.

The AAL1gators have a separate SRAM and processor interface. Either one or two SRAMs are needed, depending on the mode of operation. If using either the SBI interface, the upper four 8 Mbps H-MVIP interfaces or the upper High Speed interface, two 256K x 16 or 256K x 18 SRAMs are required. Table 5 summarizes the AAL1gator-32 SRAM requirements for different line interface modes.

Line Interface	SRAM
SBI	Two 256Kx16 or x18
H-MVIP, Eight 8 Mbps lines	Two 256Kx16 or x18
H-MVIP, Four 8 Mbps lines (lower four)	One 256Kx16 or x18
High Speed Mode, 2 interfaces	Two 256Kx16 or x18
High Speed Mode, 1 interface (lower)	One 256Kx16 or x18

Table 5. AAL1gator-32 SRAM Requirements.

Either a synchronous SRAM with a single cycle deselect or a pipelined ZBT or ZBT compatible SRAM can be used. For most applications the synchronous SRAM is sufficient, but if additional performance is needed, such as in cross connect applications which need to use partial cells to lower delay, the ZBT ram is recommended.

5.7 Processor Interface Block

The Processor Interface is provided for the purposes of device configuration, supporting AAL1, AAL0, AAL5, OAM cells, loopback modes, interrupt processing and management functions such as retrieving MIB variables, performance monitoring and alarm detection and indication.

5.7.1 Device Configuration

The Processor Interface block provides 16-bit access to normal mode registers, test mode registers and memory mapped registers. The normal mode registers and memory mapped registers are required for normal operation and for supporting AAL1, AAL0, AAL5, OAM cells and loopback modes while test mode registers are used to enhance the testability of the AAL1gator. Memory maps for the register sets are found in the datasheets.

5.7.2 Interrupt Processing

The AAL1gator provides a single maskable, open-collector interrupt with a master interrupt register to facilitate interrupt processing. The master interrupt register indicates the following maskable conditions:

- Error/status condition with one of the AAL1 processing blocks
- RAM parity error
- UTOPIA parity error

- Transmit UTOPIA FIFO is full
- UTOPIA loopback FIFO is full
- UTOPIA runt cell is detected
- SBI error detected

5.8 Management and Diagnostics

This section describes the AAL1gator's management and diagnostic capabilities such as retrieving MIB variables, performance monitoring and alarm detection and indication.

5.8.1 ATM Forum's CES-IS 2.0 MIB

In the Cell Receive direction counters are provided for the following events which include all counters required by the ATM Forum's CES-IS 2.0 MIB:

- Incorrect sequence numbers per queue
- Incorrect sequence number protection fields per queue
- Total number of received cells per queue
- Total number of dropped cells per queue
- Total number of underruns per queue
- Total number of lost cells per queue
- Total number of overruns per queue
- Total number of reframes per queue
- Total number of pointer parity errors per queue
- Total number of misinserted cells per queue
- Total number of OAM or non-data cells received
- Total number of OAM or non-data cells dropped.

In the Cell Transmit direction counters are provided for:

- Conditioned cells transmitted for each queue
- Cells which were suppressed for each queue
- Total number of cells transmitted for each queue

5.8.2 Alarm Indication Signals

The AAL1gator provides per-VC data and signaling conditioning in the transmit cell direction and per DS0 data and signaling conditioning in the transmit line direction. Data and signaling conditioning can be individually enabled and includes DS3 Alarm Indication Signals (AIS) conditioning support in both directions. Transmit line conditioning options include programmable byte pattern, pseudo-random pattern or old data. Conditioning automatically occurs on underruns.

5.8.3 Line Side Loopbacks

The AAL1gator devices support Line Side Loopback which can be enabled either on single Nx64 channels or on groups of Nx64 channels.

5.8.4 UTOPIA Loopbacks

The AAL1gator devices support two forms of UTOPIA to UTOPIA loopback; global loopback and VC based loopback. In global loopback all cells received from the UTOPIA bus are sent back out onto the UTOPIA bus. In VC based loopback mode, cells received with a VC that matches the value in a loopback VC register are sent back out onto the UTOPIA bus. A three cell FIFO is used for supporting loopback.

5.9 JTAG Interface

The JTAG Interface block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported.

6 AAL1GATOR-8 / AAL1GATOR-4 DEVICE OVERVIEW

The AAL1gator-8 and AAL1gator-4 devices address CPE and CLE applications where support for a small number of links is required. The AAL1gator-8 supports eight DS1/E1 links while the AAL1gator-4 supports four. Both devices can also be configured to support either one DS3/E3/STS-1/STM-0 or three unstructured J2 links.

The AAL1gator-8 and AAL1gator-4 are pin-compatible devices that are both available in a 324 PBGA 23mm x 23mm package. The AAL1gator-8 and AAL1gator-4 internally comprise an AAL1 SAR Processor, a UTOPIA / Any-PHY Interface, Line Interface, Processor Interface, External Clock Interface, JTAG Interface, RAM Interface and a Clock MUX as shown in Figure 14.

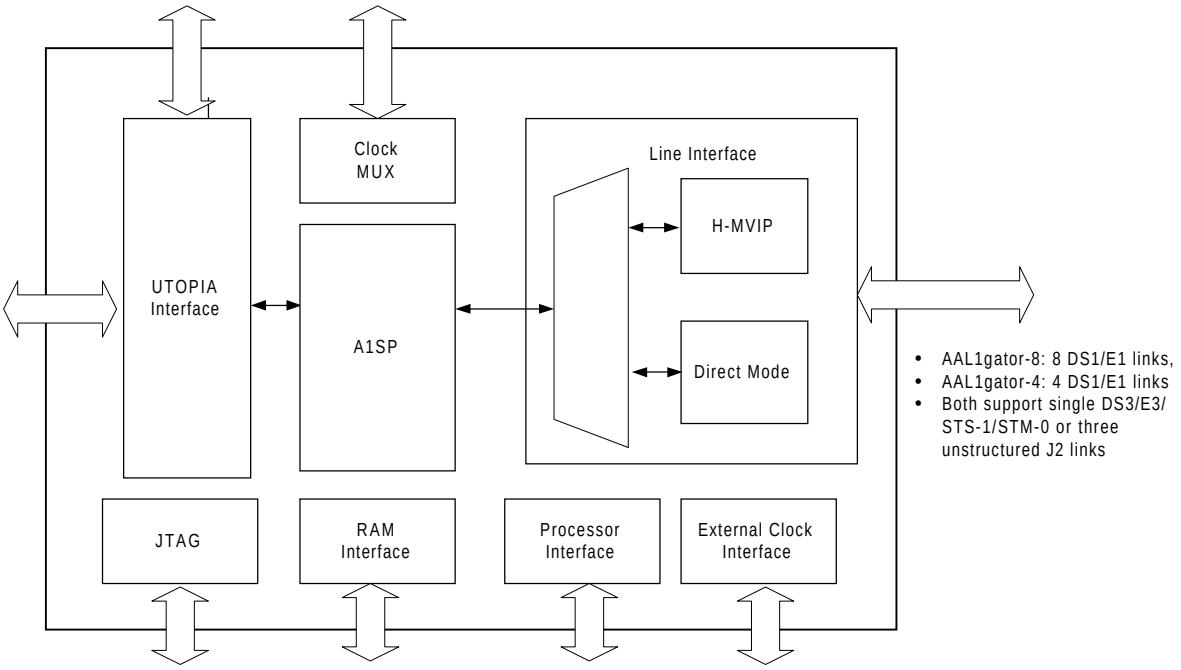

Figure 14. AAL1gator-8 and AAL1gator-4 Block Diagram.

The AAL1gator-8 and AAL1gator-4 devices have similar UTOPIA / Any-PHY, JTAG, Processor and External Clock Interface functional blocks to the AAL1gator-32 (see Section 5 for descriptions of these blocks). The key differences in the functional blocks of the AAL1gator-8, AAL1gator-4 and AAL1gator-32 are summarized in Table 6.

AAL1gator-8 / AAL1gator-4	AAL1gator-32
Single A1SP Block	Four A1SP Blocks
Single RAM Interface Block for one 128Kx16 or x18 SRAM	Dual RAM Interface Blocks for up to two 256Kx16 or x18 SRAMs
Line Interface Modes Supported: • H-MVIP • Direct Mode	Line Interface Modes Supported: • SBI • H-MVIP • High Speed Mode • Direct Low Speed Mode
Less I/O on Clock Mux Block	More I/O on Clock Mux Block

Table 6. AAL1gator-32, AAL1gator-8 / AAL1gator-4 Functional Block Differences.

6.1 Line Interface

The AAL1gator-8 and AAL1gator-4 provide a configurable line interface which, depending on the system application, is configured through a hardware pin to operate in one of the following two modes:

- High Speed Multi-Vendor Integration Protocol (H-MVIP)
- Direct Mode

6.1.1 High Speed Multi-Vendor Integration Protocol (H-MVIP) Mode

The H-MVIP mode of the AAL1gator-8 and AAL1gator-4 are similar to the AAL1gator-32 H-MVIP mode described in Section 5.1.2. Differences exist only in total capacity. While the AAL1gator-32 supports a total of eight H-MVIP lines, the AAL1gator-8 and AAL1gator-4 support two and one H-MVIP line, respectively.

As with the AAL1gator-32 each H-MVIP line supports four DS1/E1 links each and each link can be individually configured for either DS1 or E1 and with Basic Service (no CAS) or Service with CAS.

6.1.2 Direct Mode

Direct Mode can be used to interconnect the AAL1gator to standard T1 or E1 Framers, to devices which support the MVIP-90 protocol or to T3/E3/J2/STS-1/STM-0 framers for high speed unstructured data transfer.

6.1.2.1 DS1 / E1 Links

The Direct Mode interface comprises a clock, data, frame pulse, and signaling pin for each direction. A common clock pin is also available, which can be shared across all receive lines or all transmit lines and is selectable on a per line basis.

Some framers also share a clock and signaling pin, where the clock pin becomes a signaling pin when signaling is required or remains as a clock pin when individual clocks per line are required. When this pin carries signaling information a common clock is used, which is shared across all lines. This option can be configured on a per line basis.

Timing recovery is supported internally or externally for DS1/E1 links. For external timing recovery, the AAL1gator's External Clock Interface outputs various signals including SRTS and Adaptive Status values.

6.1.2.2 MVIP-90

2 Mbps MVIP mode is also supported where the line is handled in accordance with the MVIP-90 specification. MVIP mode can be individually selected per line for all lines. Tri-stating of individual time slots is not supported. There is a common 4 MHz clock and a common framing reference signal.

6.1.2.3 Unstructured J2

Using the clock and data pins in Direct Mode, the AAL1gator-8 and AAL1gator-4 devices can each support three unstructured J2 links.

6.1.2.4 DS3/E3/STS-1/STM-0 Links

Using the clock and data pins in Direct Mode, the AAL1gator-8 and AAL1gator-4 devices can each support one unstructured DS3, E3, STS-1 or STM-0 link.

Timing recovery is supported externally for DS3/E3/J2/STS-1/STM-0 links. The AAL1gator's External Clock Interface outputs various signals including SRTS and Adaptive Status values.

7 APPENDIX

Table 7 lists the AAL1gator reference material which can be found at http://www.pmc-sierra.com:

Reference Material	Document #	Availability
AAL1gator Product Family Technical Overview	PMC-200-0024	Now
AAL1gator-32		
Longform Datasheet	PMC-1981419	Now
Shortform Datasheet	PMC-1991271	Now
VHDL Model		Now
BSDL Model		April '00
IBIS Model		Now
AAL1gator-32 Reference Design	PMC-1990887	Now
AAL1gator-8		
Longform Datasheet	PMC-200-0097	Now
Shortform Datasheet	PMC-1991272	Now
VHDL Model		Now
BSDL Model		April '00
IBIS Model		Now
AAL1gator-8 Reference Design	PMC-1991089	Now
AAL1gator-4		
AAL1gator-8 (PM73123) to AAL1gator-4 (PM73124) Migration (enables use of AAL1gator-8 in AAL1gator-4 socket). As availability of the AAL1gator-4 is later than the AAL1gator-8 this application note enables the implementation of AAL1gator-4 designs using the AAL1gator-8 device immediately.	PMC-200-0095	Now
Longform Datasheet	PMC-200-0098	March '00
Shortform Datasheet	PMC-1991273	Now
VHDL Model		Now
BSDL Model		April '00
IBIS Model		Now

Software		
AAL1gator-32 / -8 / -4 Programmers Guide	PMC-1991820	Now
AAL1gator-32 / -8 / -4 Software Drivers		mid March '00
AAL1gator-32 / -8 / -4 Software Driver User's Guide		mid March '00
Application Notes		
Jitter and Wander Characteristics		end April '00
Development Kits		
AAL1gator-32 Development Kit		June '00

Table 7. AAL1gator Reference Material Available.

8 GLOSSARY

A32/A8/A4	AAL1gator-32 / AAL1gator-8 / AAL1gator-4
AIS	Alarm Indication Signal
CAS	Channel Associated Signaling
CCS	Common Channel Signaling
CES	Circuit Emulation Service
CPE	Customer Premise Equipment
CLE	Customer Located Equipment
DBCES	Dynamic Bandwidth Circuit Emulation Service
DS0	Digital Service, level 0: There are 24 DS0 channels in a DS1. Each DS0 channel has a bandwidth of 64 Kbps full duplex.
DS1	Digital Service, level 1. 1.544 Mbps
DS3	Digital Service, level 3. 44.736 Mbps
E1	E1 carries information at the transmission rate of 2 Mbps. This is the rate used by European CEPT carriers to transmit 30, 64 Kbps digital channels for voice or data calls, plus a 64 Kbps channel for signaling and a 64 Kbps channel for framing.
E3	E3 carries information at the transmission rate of 34.368 Mbps. This is the rate used by CEPT to transmit 512 simultaneous voice conversations.
H-MVIP	High Speed Multi-Vendor Integration Protocol: A synchronous time division multiplexed bus of Nx64 Kbps constant bit rate data streams. The H-MVIP standards are defined by the GO-MVIP organization.
ISO	International Standards Organization: An international standards-setting organization.
J2	The Japanese version of the T Carrier system of North America. 6.312 Mbps used to carry 96 voice channels.
LIU	Line Interface Unit
LMDS	Local Multipoint Distribution System
MAN	Metropolitan Area Network: A term used to describe a data network covering an area larger than a local area network, but less than a wide area network. A MAN may carry voice, video and multimedia data.
MIB	Management Information Base
OAM	Operations, Administration and Maintenance
OC-12	Optical Carrier 12. SONET channel of 622.08 Mbps.

OC-3	Optical Carrier 3. A SONET channel that has a bandwidth of 155.52 Mbps
OSI	Open Systems Interconnect: A standard that defines seven independent layers of communication protocols. Each layer enhances the communication services of the layer just below it and shields the layer above it from the implementation details of the lower layer.
SBI	Scaleable Bandwidth Interconnect: A synchronous, time-division multiplexed bus designed to transfer, in a pin-efficient manner, data belonging to a number of independently timed links.
SDH	Synchronous Digital Hierarchy: A set of standard fiber-optic transmission standards used outside North America.
SONET	Synchronous Optical NETwork: A family of fiber optic transmission standards used in North America.
SPE	Synchronous Payload Envelope
SRTS	Synchronous Residual Timestamp Timing Recovery
STM-0	Synchronous Transport Module - 0
STS-1	Synchronous Transport Signal Level 1. Basic transmission rate used in SONET – equivalent to 51.84 Mbps.
T1	Trunk Level 1: A digital transmission link with a total signaling speed of 1.544 Mbps.
TSI	Time-Slot Interchanger
UTOPIA	Universal Test and Operations Interface: Refers to an electrical interface between the TC and PMD sublayers of the physical layer. UTOPIA is the interface for devices connecting to an ATM network.
VT	Virtual Tributary: A structure designed for transport and switching of sub-DS3 payloads. A unit of sub-SONET bandwidth that can be combined or concatenated, for transmission through the network. VT1.5 is equivalent to 1.544 Mbps and VT2 equals 2.048 Mbps
WAN	Wide Area Network: A data network that is used to interconnect remote LANs or users over leased lines, packet or cell switch services

9 REFERENCES

1. ATM Adaptation Layer 1 Segmentation and Reassembly Processor-32 (AAL1gator-32) Telecom Standard Product Engineering Document, Issue 3.

2. Circuit Emulation Service Interoperability Specification Version 2.0. AF-VTOA-0078. January 1997.

3. Specifications of (DBCES) Dynamic Bandwidth Utilization in 64 kbps Time Slot Trunking over ATM Using CES. AF-VTOA-0085. July 1997.

4. ATM Forum, UTOPIA, an ATM-PHY Layer Specification, Level 1, V. 2.01, Foster City, CA USA, March 1994.

5. ATM Forum, UTOPIA, an ATM-PHY Layer Specification, Level 2, V. 1.0, Foster City, CA USA, June 1995.

6. H-MVIP Standard Release 1.1. GO_MVIP.

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