ANALOG DEVICES

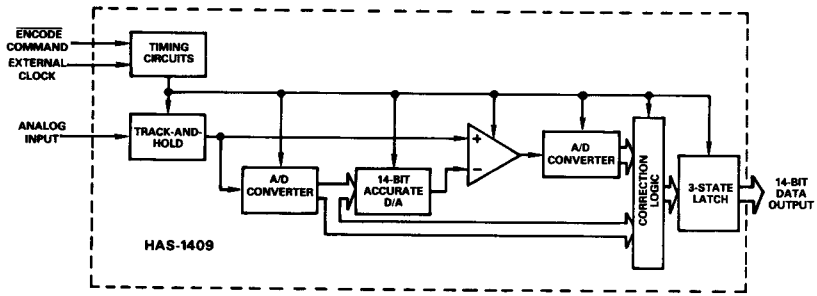
14-Bit, 125kHz Analog-to-Digital Converter

HAS-1409

FEATURES
14-Bit Resolution
125kHz Word Rates
Internal Track-and-Hold
40-Pin DIP

APPLICATIONS
FDM/TDM Transmultiplexers
CAT/NMR Scanners
PCM Systems
Digital Audio
General Instrumentation

HAS-1409 FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

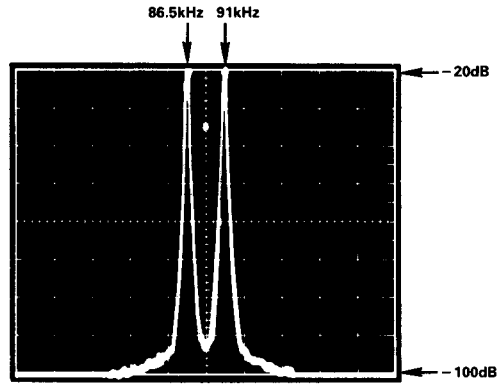
The HAS-1409KM, HAS-1409LM, and HAS-1409AKM hybrid A/D converters offer designers performance characteristics which have never before been available.

Now, for the first time, high resolution and high speed come together in a hybrid package which includes an internal track-and-hold. The HAS-1409 units have resolutions of 14 bits, are capable of word rates up to 125kHz, and are complete with track-and-hold; all of these features are housed in a single 40-pin DIP package which dissipates only two watts.

The HAS-1409KM and HAS-1409LM both include internal clocks, which allow the converters to be operated at any word rate from dc through 120kHz; the HAS-1409AKM is designed for applications which use an external system clock whose frequency establishes the user's optimum word rate, up to 125kHz.

The HAS-1409 A/D has been characterized with a companion D/A converter, the HDD-1409KM, to emphasize the superior ac performance needed for use in Frequency Division Multiplex/Time Division Multiplex (FDM/TDM) transmultiplexer systems. Although specifically designed for these kinds of applications, it can also be used for other digital signal processing such as Computer Aided Tomography (CAT) and Nuclear Magnetic Resonance (NMR) scanners, and Pulse Code Modulation (PCM).

Conventional data converters often display errors at midscale which make them inadequate for use in the types of systems cited above. The unique Digitally Corrected Subranging technique pioneered by Analog Devices, used with other proprietary techniques, virtually cancels midscale errors in the HAS-1409, thereby eliminating a major source of system errors.



10dB/div Vertical; 5kHz/div Horizontal
Spectrum analyzer shows extremely low intermodulation (IM) products of back-to-back HAS-1409 A/D and HDD-1409 D/A

The logic outputs are TTL-compatible and are presented as 14 bits of parallel data. Buffer output registers and a 3-state format provide dual advantages of good drive and bus compatibility.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Model	Units	HAS-1409KM	HAS-1409AKM	HAS-1409LM
RESOLUTION (FS = Full Scale)	Bits (%FS)	14 (0.006)	*	*
LSB WEIGHT	μV	610 or 1221, depending on input range	*	*
ACCURACY				
Linearity @ dc	%FS ± 1/2LSB	0.006	*	*
Monotonicity	°C	Guaranteed 0 to +85	*	*
Nonlinearity vs. Temperature	ppm/°C	5	*	*
Gain Error	%FS	1	*	*
Gain vs. Temperature	ppm/°C	20	*	*
DYNAMIC CHARACTERISTICS[1]				
Harmonics[2]	dB	−100	*	−80
Intermodulation Products[2]	dB	−100	*	−90
Conversion Rate	kHz	120 (112 guaranteed)	125[3]	120 (112 guaranteed)
Aperture Time (Delay)	ns	50	*	*
Signal to Noise Ratio (SNR)[4]	dB	80	*	*
Noise Power Ratio (NPR)[5]	dB	68	*	65
Transient Response[6]	μs	8	*	2
Overvoltage Recovery	μs	8	*	6
Input Bandwidth				
Small Signal, 3dB[8]	kHz	200	*	800
Large Signal, 3dB[9]	kHz	200	*	300
Idle Noise/kHz[10]	dB	−104	*	*
ANALOG INPUT				
Voltage Ranges	V, FS	±5; ±10	*	*
Overvoltage	V, max	±20	*	*
Input Type		Bipolar	*	*
Impedance	kΩ	5; 10	*	*
Offset				
Initial–Set at Factory	mV (max)	2 (10)	*	*
vs. Temperature	μV/°C	100	*	*
ENCODE COMMAND INPUT[11]				
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4	*	*
		"1" = +2.4 to +5	*	*
Impedance	TTL Loads	1	*	*
Width				
Min	ns	50	1 Clock	*
Max	ns	T–50[12]	Period	*
Frequency	kHz	dc to 125	Synchronous to External Clock	*
CLOCK INPUT				
Logic Levels, TTL-Compatible	V			
		N/A	"0" = 0 to +0.4	N/A
		N/A	"1" = +2.4 to +5	N/A
Impedance	TTL Loads	N/A	2	N/A
Frequency[13]	MHz, max	N/A	4.5	N/A
DIGITAL OUTPUT				
Format	Bits	14 Parallel; 3 State	*	*
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4	*	*
		"1" = +2.4 to +5	*	*
Drive	TTL Loads	5	*	*
Time Skew	ns, max	20	*	*
Coding		Offset Binary (MSB);	*	*
		2's Complement ($\overline{\text{MSB}}$)	*	*
POWER REQUIREMENTS				
+15V ± 5%	mA	20	*	*
−15V ± 5%	mA	40	*	*
+5V ± 5%	mA	220	200	*
Power Dissipation	W (max)	2.0 (2.4)	1.8 (2.2)	*
TEMPERATURE RANGE[14]				
Operating	°C	−25 to +85	*	*
Storage	°C	−55 to +150	*	*
THERMAL RESISTANCE[15]				
Junction to Air, θ_{JA}				
(Free Air)	°C/W	25	*	*
Junction to Case, θ_{JC}	°C/W	16	*	*
MEAN TIME BETWEEN FAILURES[16]				
(MTBF)	Hours	4.15×10^4	*	*
PACKAGE OPTION[17]				
M-40		HAS-1409KM	HAS-1409AKM	HAS-1409LM

For applications assistance, phone Computer Labs Division at (919) 668-9511

NOTES

[1] AC performance characteristics are based on back-to-back performance with HDD-1409 D/A Converter. All signals are referenced to rms value of full-scale sinewave.

[2] Harmonics and intermodulation products measured at 112kHz encode rate, with input frequencies of 86.5kHz and 91kHz at −21dB (see Figure 5).

[3] Requires external clock.

[4] Full-scale signal to rms noise with 10kHz analog input frequency and encode rate of 112kHz; input signal at −6dB.

[5] 60kHz to 108kHz white noise bandwidth with slot frequency of 70kHz; and encode rate of 112kHz (see Figure 6).

[6] For full-scale 10-volt input, ±1LSB attained in specified time.

[7] Recovers to 14-bit accuracy in specified time after 2 × FS input overvoltage.

[8] With analog input 40dB below FS.

[9] With FS analog input. (Large-signal bandwidth flat within 0.5dB, dc to 100kHz).

[10] Idle noise measured at 112kHz encode rate, with input frequency of 84kHz at −41dB (see Figure 7).

[11] HAS-1409KM has pin-selectable positive- or negative-edge triggering. HAS-1409AKM requires negative pulse synchronized to rising clock edge.

[12] T = Encode Command clock period.

[13] Clock frequency shown based on typically using 50% duty cycle and 36:1 division of external clock.

[14] Case Temperature.

[15] Maximum junction temperature = 150°C

[16] Calculated for using MIL-HDBK 217; Ground Benign; Case Temperature = 60°C.

[17] See Section 14 for package outline information.

* Specifications same as HAS-1409KM.

Specifications subject to change without notice.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

HAS-1409 PIN DESIGNATION

PIN	FUNCTION (ALL)	PIN	FUNCTION (AKM)	PIN	FUNCTION (KM & LM)
1	±10V INPUT	21	DIGITAL GROUND	21	DIGITAL GROUND
2	±5V INPUT	22	BIT 1 (MSB)	22	BIT 1 (MSB)
3	ANALOG GROUND	23	BIT 1 (MSB)	23	BIT 1 (MSB)
4	DIGITAL GROUND	24	BIT 2	24	BIT 2
5	+5V	25	BIT 3	25	BIT 3
6	+5V	26	BIT 4	26	BIT 4
7	N/C	27	BIT 5	27	BIT 5
8	N/C	28	BIT 6	28	BIT 6
9	+5V	29	ENABLE HIGH (MSBs)	29	ENABLE HIGH (MSBs)
10	DIGITAL GROUND	30	CLOCK	30	ENCODE
11	ENABLE LOW (LSBs)	31	ENCODE	31	ENCODE
12	BIT 14 (LSB)	32	+5V	32	+5V
13	BIT 13	33	DIGITAL GROUND	33	DIGITAL GROUND
14	BIT 12	34	−15V	34	−15V
15	BIT 11	35	+15V	35	+15V
16	BIT 10	36	DIGITAL GROUND	36	DIGITAL GROUND
17	BIT 9	37	ANALOG GROUND	37	ANALOG GROUND
18	BIT 8	38	ANALOG GROUND	38	ANALOG GROUND
19	BIT 7	39	+5V	39	+5V
20	DIGITAL GROUND	40	ANALOG GROUND	40	ANALOG GROUND

ALL +5V PINS ARE CONNECTED TOGETHER INTERNALLY (5, 6, 9, 32, 39). MUST ALSO BE CONNECTED TOGETHER EXTERNALLY CLOSE TO CASE.
ALL ANALOG GROUND PINS ARE CONNECTED TOGETHER INTERNALLY (3, 37, 38, 40).
ALL DIGITAL GROUND PINS ARE CONNECTED TOGETHER INTERNALLY (4, 10, 20, 21, 33, 36).
FOR BEST PERFORMANCE, ANALOG GROUND AND DIGITAL GROUND PINS MUST ALL BE CONNECTED TOGETHER AND TO GROUND EXTERNALLY AS CLOSE TO THE CASE AS POSSIBLE.

HAS-1409KM/HAS-1409AKM TIMING

Refer to the block diagram of the HAS-1409AKM A/D converter.

In the HAS-1409KM, and HAS-1409LM, signals applied to the timing circuits will be different from those shown. For them, these signals will be ENCODE or $\overline{\text{ENCODE}}$.

In all units, the analog input to be digitized is applied first to a track-and-hold (T/H) circuit, which is normally in "track", following all changes in analog as they occur since the T/H is operating as a buffer amplifier.

Refer to Figure 1, the timing diagram for the HAS-1409KM and HAS-1409LM A/D converters.

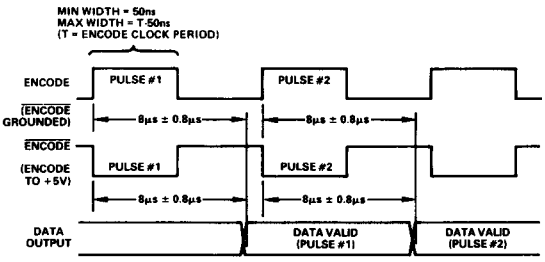


Figure 1. HAS-1409KM and HAS-1409LM A/D Timing Diagram

The user determines the point at which digitizing is to be done by applying an external TTL-compatible signal to the timing circuits; this causes the T/H to switch from the "track" mode to the "hold" mode. In the HAS-1409KM and HAS-1409LM, this "track" to "hold" transition can be accomplished with either positive triggering or negative triggering. As shown, positive-edge triggering is done with an ENCODE command and $\overline{\text{ENCODE}}$ connected to ground. Negative-edge triggering is accomplished with an $\overline{\text{ENCODE}}$ signal and ENCODE connected to +5V. The HAS-1409KM and HAS-1409LM return to "track" automatically approximately 5μs after the encode command.

Output data will be valid after a nominal delay of 8μs from the leading edge of the encode command. Strobing the output data into external circuits might best be accomplished by using a square-wave signal for the encode command and using its negative-going trailing edge as a time reference for the strobing action. Output data will not yet be valid when that trailing edge occurs, but the edge can be used as a known reference point for measuring the 8μs conversion time.

Internal timing circuits within the HAS-1409 generate the necessary control and timing pulses to operate the unit at a word rate of 112kHz. This rate is based on:

KM/LM: The internal clocks are adjusted at the factory for this conversion rate.

AKM: The HAS-1409AKM divides the external clock frequency of 4.032MHz by a factor of 36:1 and provides 14 bits of parallel data at the 112kHz word rate established by this ratio. The 112kHz cited in this example is the minimum guaranteed word rate of the HAS-1409, and is a sample rate commonly used in transmultiplexer applications. (See FDM/TDM Transmultiplexers section of data sheet).

Figure 2 shows the timing relationship of the HAS-1409AKM A/D converter signals when the converter is being operated from an external clock.

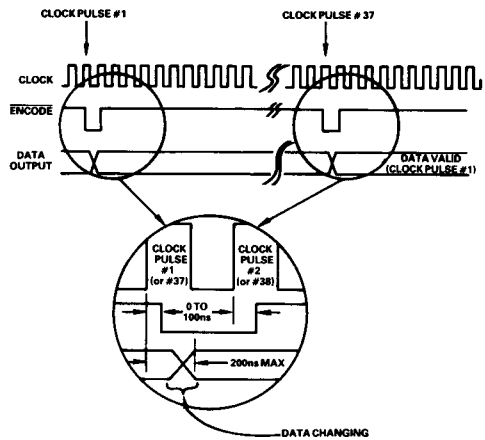


Figure 2. HAS-1409AKM A/D Timing Diagram (External Clock Operating at 4.032MHz)

As shown, the leading edge of the negative-going $\overline{\text{ENCODE}}$ pulse supplied by the user should occur from 0 to 100ns after the leading edge of the clock pulse which is shown (for purposes of illustrating timing relationships) as Clock Pulse #1. The trailing edge of this pulse should occur from 0 to 100ns after the leading edge of the *next* clock pulse (designated here as Clock Pulse #2).

The output data associated with the *preceding* clock pulse and $\overline{\text{ENCODE}}$ pulse will be valid within 200ns of the leading edge of Clock Pulse #1. Data associated with Clock Pulse #1 will be valid within 200ns of the leading edge of Clock Pulse #37. When the HAS-1409AKM is operated from a 4.032MHz clock, the trailing edge of the $\overline{\text{ENCODE}}$ pulse could be used to determine when the output data will be strobed into external circuits.

The $\overline{\text{ENCODE}}$ pulse is used to insure output data will remain in synchronization with the clock pulses. Using the leading edge of the first $\overline{\text{ENCODE}}$ as a reference, the HAS-1409AKM goes into "track" after 21 clock pulses (on Clock Pulse #22); and goes into "hold" after 34 clocks (Clock Pulse #35).

THEORY OF OPERATION

With the exception of the difference in input signals applied to the timing circuits, all converters operate in essentially the same way.

Referring again to the block diagram, the timing circuits "freeze" the analog signal at the output of the track-and-hold. This held value is applied to an A/D converter in the HAS-1409, and the same value is applied to one input of a difference amplifier.

The output of the internal A/D converter is digitized and applied to a D/A converter which is 14-bit accurate and optimized for ac applications; the A/D output is also applied to correction logic circuits.

The D/A output is applied to the second input of the difference amplifier, which generates an error signal indicative of the difference between the "held" analog input and a digital representation of that signal. This residue signal is then converted and is also applied to the digital correction circuits.

The correction circuits combine the two bytes to compensate for nonlinearities and other circuit errors. Basically, the information contained in the second byte is used as the Least Significant Bits (LSBs) and determines what corrective action is needed for the first byte (the MSBs) to insure its accuracy.

APPLICATIONS/TESTING

For FDM/TDM applications, the analog input frequency applied to the HAS-1409 will be in the frequency band of 60-108kHz; the combined HAS-1409/HDD-1409 performance parameters have been optimized for this use.

Refer to Figure 3 HAS-1409 Basic Interface.

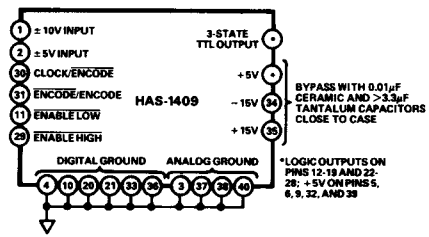


Figure 3. HAS-1409 Basic Interface

As shown, the anlog input is applied to Pin 1 or Pin 2, depending on the amplitude of the signal to be digitized. A TTL-compatible pulse is applied as $\overline{\text{ENCODE}}$; and another TTL-compatible signal is applied as the clock. As indicated earlier in the timing diagram, these signals must be synchronous.

The $\overline{\text{ENABLE HIGH}}$ and $\overline{\text{ENABLE LOW}}$ signals applied to Pins 29 and 11 control the state of the digital outputs. The TTL $\overline{\text{ENABLE HIGH}}$ signal affects $\overline{\text{BIT 1}}$ (MSB), Bit 1 ($\overline{\text{MSB}}$), and Bits 2-6; the $\overline{\text{ENABLE LOW}}$ affects Bits 7-14. When $\overline{\text{ENABLE HIGH}}$ and/or $\overline{\text{ENABLE LOW}}$ inputs are connected

to ground or logical "0", their corresponding bit outputs will be present. When they are connected to a logical "1" voltage, their associated bit outputs will be open.

The 3-state TTL digital output signals will be available at Pins 12-19 and Pins 22-28. Pins 34 and 35 are used for −15V and +15V supplies; +5V is applied to several places–Pins 5, 6, 9, 32, and 39 (all pins should be connected). All three supplies should be bypassed as close as possible to the hybrid case. For best performance, all ANALOG GROUND and DIGITAL GROUND pins *must* be connected together and to ground externally; this should also be done close to the case.

Refer to Figure 4 Basic Test Setup.

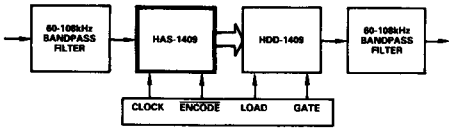


Figure 4. Basic Test Setup

The HAS-1409 A/D converter has been characterized for performance in a back-to-back hook-up with the HDD-1409 D/A converter. The analog signal to be digitized and reconstructed is applied to this test arrangement through a bandpass filter of 60kHz-108kHz; the resulting analog output is also passed through the same kind of filter.

CLOCK and $\overline{\text{ENCODE}}$ signals are generated in synchronization with one another and are timed for correct interaction with the STROBE and GATE signals applied to the D/A. Because of the back-to-back configuration of the two converters, the performance tests are indicative of the baseline characteristics of *both* units.

Refer to Figure 5 Intermodulation (Total Harmonic) Distortion Test Circuit.

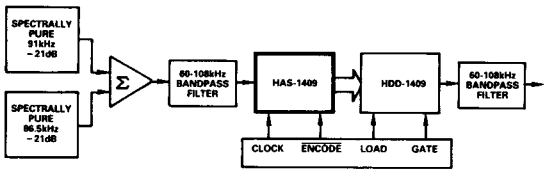


Figure 5. Intermodulation (Total Harmonic) Distortion Test Circuit

Harmonics levels and intermodulation (IM) products are measured in the same way to assure optimum performance in FDM/TDM system applications. The purpose of the testing is to insure that "beat" frequencies generated by the interaction of two signals are sufficiently suppressed to avoid interfering with the carrier frequencies and masking their information contents.

In these tests, the HAS-1409 is operated at a 112kHz word rate, established by the external 4.032MHz clock. Two pure sinewave signals at frequencies of 91kHz and 86.5kHz are applied to a summation amplifier at precise levels 21dB below the rms value of a full-scale sinewave.

These particular input frequencies are selected on the basis that their interaction with one another will generate second and third-order harmonics and IM products which are easily distinguished and measurable. As in any sampling scheme, these signals are "folded" back into the passband of interest and their amplitudes are a measure of A/D and D/A performance.

The output of the summation amplifier is applied through the 60-108kHz filter, digitized, reconstructed, and refiltered. Typically, the levels of harmonics and intermodulation products are −100dB.

Refer to Figure 6 Noise Power Ratio Test Circuit.

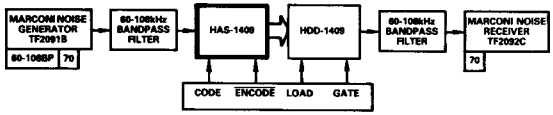


Figure 6. Noise Power Ratio Test Circuit

Noise Power Ratio (NPR) is a critical measure of A/D and D/A performance for FDM/TDM systems and the method of measuring this ratio must replicate the conditions which are present when the units are operating as a part of those systems. In this test, also, the HAS-1409 is operating at 112kHz word rates.

White noise in the frequency band of 60kHz to 108kHz is applied to the A/D, and the total power which is present in a narrow "slot" at a frequency of 70kHz is computed. A narrow bandstop filter whose center frequency is 70kHz is then switched in, and the total power remaining in the "slot" is computed. The ratio of these two readings is the NPR and the result for the HAS-1409 is typically 68dB. CAUTION: The high-performance characteristics of the HAS-1409 stress the measurement capabilities of most NPR test sets.

Refer to Figure 7 Idle Noise Test Circuit. In this test, a spectrally-pure sinewave of 84kHz is applied through a filter to the HAS-1409/HDD-1409 combination at a level of −41dB. An encode rate of 112kHz is used; the combination of input frequency and encode rate cancels all harmonics, leaving only the fundamental input frequency and noise components.

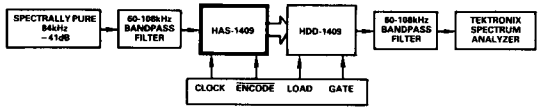


Figure 7. Idle Noise Test Circuit

The results of digitizing and reconstructing this signal are examined with a spectrum analyzer to determine the level of noise components contributed by the converters. Acceptable performance will show average idle noise components to be at −104dB when using a 1kHz-resolution filter.

FDM/TDM TRANSMULTIPLEXERS

There are two standard formats used in telephony for multiplexing voice signals. The older of the two, frequency division multiplex (FDM), is used throughout the world for transmitting long distance telephone calls. In this scheme, voiceband signals are "stacked" into adjacent 4kHz channels in their assigned frequency domain by using single sideband (SSB) amplitude modulation.

Standard FDM hierarchy assembles twelve of these 4kHz channels into units called "groups", and then assembles five groups (60 channels) into "supergroups." The frequencies of group bands range from 60kHz to 108kHz, and the supergroup bands have center frequencies between 312kHz and 552kHz.

In the newer time division multiplex, or TDM, each voice signal is digitized using pulse code modulation (PCM), at an 8kHz sample rate. The resulting pulse streams are then interleaved in time and transmitted.

The assembly of time slots (channels) for TDM is not as universal as it is for FDM. In North America and Japan, the basic unit is 24 time slots, all of which are available to users. In Western Europe, the basic unit is 32 time slots; 30 are active, one is for signaling, and one is for framing.

TDM processing is growing at a rapid pace because the voice signals have good fidelity, and the hardware which is used benefits from the economics of lower and lower prices for digital integrated circuits.

Digital toll switching offices were first installed in the United States in the latter part of the 1970s. One of the major characteristics of these types of telephone offices is that they switch signals exclusively in the TDM format within the office. But their need to operate also with the older FDM format means all incoming and outgoing signals must be converted to and from digital form.

The interface between the two standard signal multiplexing formats used to make this conversion is the FDM/TDM transmultiplexer system. The translation from one format to the other can be accomplished with conventional analog and digital techniques by demultiplexing signals in one format down to baseband, and remultiplexing them again into the other format.

Digital signal processing (DSP) for the interface is attractive, however. The frequency ranges of the signals which are involved make efficient use of available technology; and the stringent interface specifications benefit from the inherent precision of a digital approach. Since the problem is well defined, digital techniques are distinctly viable solutions. An example of these techniques is shown in Figure 8.

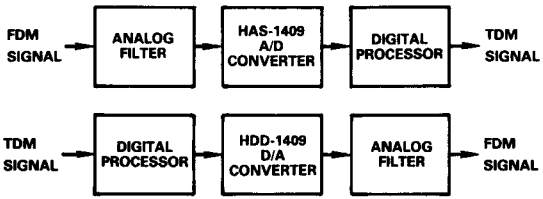


Figure 8. Digital FDM/TDM Translation

Undesirable out-of-band components are removed from the FDM signal by the analog filter. The output of the filter is then applied to the HAS-1409 A/D converter whose output is a digital word stream. The individual channels within this stream are separated via a real-time processing algorithm in the block labeled Digital Processor. The resulting signal is now in the TDM format for switching and/or transmitting.

The lower portion of Figure 8 depicts the process of going from TDM to FDM, using the HDD-1409 D/A converter, in a procedure which is basically an inverse operation. The exception is the analog filter, which performs essentially the same function in both directions.

Interfacing FDM and TDM occurs at two different levels. In North America and Japan, this translation takes place between two 12-channel group bands and a 24-channel TDM unit. In Europe, it is between a 60-channel supergroup and two 30-channel European TDM units.

Theoretically, the minimum word rate for the HAS-1409 A/D is equal to twice the bandwidth of the FDM group signal; that signal, in turn, is equal to the word rate of the TDM signal, i.e., 96kHz for the group band.

This minimum rate falls into the passband of interest because group frequencies occupy the band from 60kHz to 108kHz; as a consequence, the theoretical minimum rate would severely complicate the processing algorithm and introduce aliasing errors into the signal.

Operating at a conversion rate near this minimum is desirable, however, because the cost of the A/D and D/A converters increases as their word rates increase. In addition, a sampling rate which is an even multiple of the basic 8kHz PCM frequency simplifies the algorithm.

Since any sampling rate between the (108kHz) upper band and two times the 60kHz lower band (120kHz) will suffice, the HAS-1409 A/D converter is operated at 112kHz.

This rate provides the benefits enumerated above and prevents overlapping between channels caused by aliasing. A conversion rate of 112kHz also supplies a guard band of 8kHz between signal images; that guard band reduces the complexity of the analog reconstruction filter.

Computer Labs Division of Analog Devices uses this 112kHz word rate when testing the performance of the HAS-1409 A/D and HDD-1409 D/A converters back-to-back to help assure test conditions are a good replication of the operating conditions.

For some of the testing, the word rate interacts with the analog input frequencies to provide additional insight into performance. Harmonics tests and intermodulation products tests are examples.

Another is the test for idle noise, the sum of various noise spectra not influenced by modulation. Thermal noise, oscillator shot noise, baseband amplifier noise, and other sources are examples. Their sum is measured on a power basis because of their uncorrelated nature.

In the test, the input frequency is a spectrally-pure 84kHz. The combination of input frequency and encode rate cancels all harmonics, leaving only the fundamental frequency and the idle noise components.

Evaluating the amount of idle noise generated by the converters helps evaluate their nonlinear distortion, without rigorously testing for that characteristic. In transmultiplexer systems, the converters are the only important sources of this distortion, but converters which meet requirements for idle noise easily meet requirements for nonlinearity.