



## SHM-20

### High Speed, 0.01% Monolithic Sample/Hold

T-73-65

#### FEATURES

- Internal hold capacitor
- 1 Microsecond acquisition time
- 1 Nanosecond aperture uncertainty
- 0.01% Accuracy
- 0.08 MicroV/Microsecond droop rate
- Differential Inputs

#### GENERAL DESCRIPTION

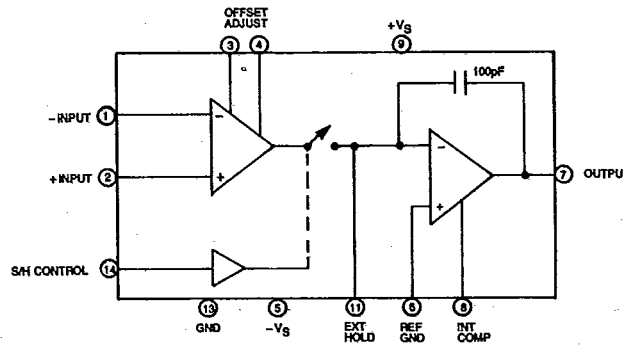
DATEL's SHM-20 is a low-cost, complete monolithic sample/hold amplifier which includes an internal 100 pF MOS hold capacitor. Primarily designed for high speed analog signal processing applications, the SHM-20 features a typical acquisition time of 1.0 microsecond for a 10V input step to 0.01%. Aperture uncertainty is typically 1 nanosecond and droop rate is as low as 0.08  $\mu\text{V}/\text{microsecond}$ .

The SHM-20 consists of an input transconductance amplifier, a low leakage analog switch, an output integrating amplifier and a 100 pF MOS hold capacitor. Charge injection on the hold capacitor is constant over the entire input/output voltage range. The pedestal voltage resulting from this charge injection can be adjusted to zero by using the offset adjust inputs. For improved droop rate, an external hold capacitor may be added at the expense of acquisition time.

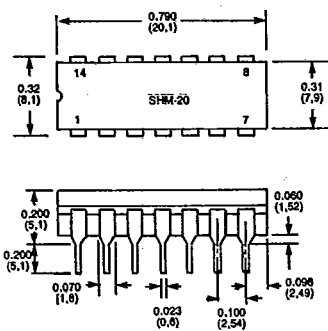
Other important features of the SHM-20 include a 30 nanosecond aperture delay time, 1 mV pedestal error, a minimum dc gain of  $10^6\text{V}/\text{V}$  and fully differential inputs with a  $\pm 10\text{V}$  input voltage range. Maximum input offset voltage is as low as 0.5 mV with a maximum input offset voltage drift as low as  $15 \mu\text{V}/^\circ\text{C}$ .

Its low cost and high performance make the SHM-20 an excellent choice for innumerable applications including, precision data acquisition systems, deglitching circuits, auto-zero circuits, data distribution systems and peak amplitude detectors. Power requirement is  $\pm 15\text{V}$  dc.

The SHM-20 is available in two models for operation over the commercial,  $0^\circ\text{C}$  to  $+70^\circ\text{C}$ , and military,  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  temperature ranges. Both models are packaged in a 14-pin ceramic DIP.



#### MECHANICAL DIMENSIONS INCHES (MM) MAX.



#### INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	-INPUT
2	+INPUT
3	OFFSET ADJUST
4	OFFSET ADJUST
5	-V <sub>S</sub>
6	REFERENCE GROUND
7	OUTPUT
8	INTEGRATOR COMPENSATION
9	+V <sub>S</sub>
10	NO CONNECTION
11	EXTERNAL HOLD CAPACITOR
12	NO CONNECTION
13	SUPPLY VOLTAGE GROUND
14	SH CONTROL

## SHM-20

T-73-65 

ABSOLUTE MAXIMUM RATINGS, BOTH MODELS		SHM-20C	SHM-20M
Voltage between Supply Pins (Pins 9, 5) .....		40V	
Differential Input Voltage .....		±24V	
Digital Input Voltage, Pin 14 .....		+8V to -15V	
Output Current, Continuous <sup>1</sup> .....		±20 mA	

PHYSICAL/ENVIRONMENTAL	
Operating Temp. Ranges	
SHM-20C .....	0°C to +70°C
SHM-20M .....	-55°C to +125°C
Storage Temp. Range .....	
	-65°C to +150°C
Package Type ..	14 Pin, Ceramic DIP

## FUNCTIONAL SPECIFICATIONS, BOTH MODELS

Typical at +25°C, ±15V dc, using internal hold capacitor, unless otherwise noted.

ANALOG INPUTS		SHM-20C	SHM-20M
Input Voltage Range, <sup>2</sup> minimum .....		±10V	
Input Impedance, minimum .....		1 MΩ	
Input Capacitance, maximum .....		3 pF	
Input Offset Voltage, maximum .....		1 mV	0.5 mV
Input Offset Voltage Drift, maximum .....		20 μV/°C	15 μV/°C
Input Bias Current, maximum .....		300 nA	200 nA
Input Offset Current, maximum .....		300 nA	100 nA
DIGITAL INPUTS <sup>2</sup>			
Logic Level High, Vin ("1"), minimum, Hold Mode .....		2.0V	
Logic Level Low, Vin ("0"), maximum, Sample Mode .....		0.8V	
High Level Input Current, maximum .....		0.1 μA	
Low Level Input Current, maximum .....		10 μA	
OUTPUT			
Output Voltage Range <sup>2</sup> , minimum .....		±10V	
Output Current <sup>2</sup> , minimum .....		±10 mA	
Output Impedance, Hold Mode <sup>2</sup> .....		1 Ω	
PERFORMANCE			
Accuracy .....		0.01%	
DC Gain, minimum .....	3 x 10 <sup>5</sup> V/V	10 <sup>5</sup> V/V	
Gain Accuracy <sup>4</sup> .....		0.5 x 10 <sup>-4</sup> %FSR	
Gain Error Tempo .....		±0.6 ppm/°C	
Gain Bandwidth Product <sup>5</sup> .....		2 MHz	
Hold Mode Feedthrough, 10V P-P, 100 kHz <sup>2</sup> .....		2 mV	
Drop Rate .....		0.08 μV/μsec.	
Drop Rate <sup>2</sup> .....	1.2 μV/μsec.	17 μV/μsec.	
Charge Transfer <sup>4</sup> .....		0.1 pc	
Pedestal Error .....		1 mV	
Total Output Noise, DC to 10 MHz, maximum .....		200 μV RMS	
Power Supply Rejection Ratio, minimum +VS .....		80 dB	
		65 dB	
Pedestal Error .....		1 mV	
DYNAMIC CHARACTERISTICS			
Acquisition Time, 10V to 0.1% .....		0.8 μsec.	
10V to 0.01% .....		1.0 μsec.	
Aperture Delay Time .....		30 nsec.	
Aperture Uncertainty Time .....		1 nsec.	
Aperture Time .....		25 nsec.	
Hold Mode Settling Time, 0.01% <sup>2</sup> .....		185 nsec.	
Rise Time .....		100 nsec.	
Overshoot .....		15%	
Slew Rate <sup>7</sup> .....		45 V/μsec.	
POWER REQUIREMENTS <sup>8</sup>			
Positive Supply, Pin 9 .....		+15V ±0.5V at 11 mA	
Negative Supply, Pin 5 .....		-15V ±0.5V at -11 mA	

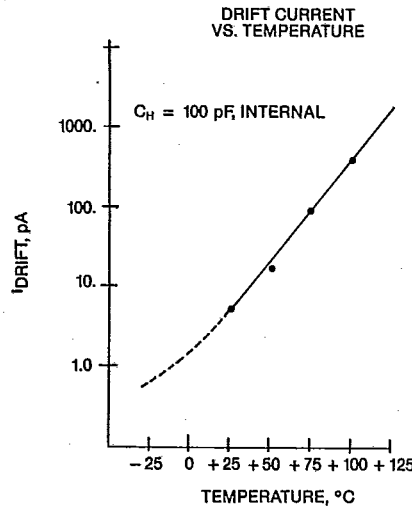
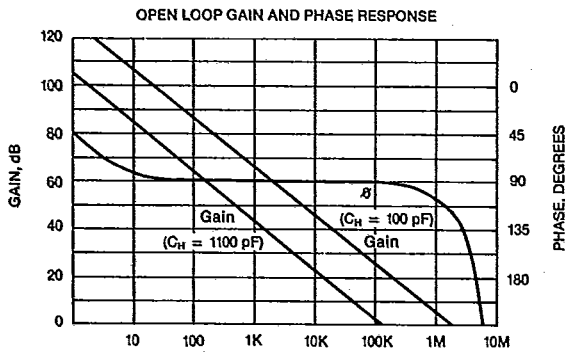
## FOOTNOTES:

1. Internal power dissipation may limit output current below +20 mA.
2. Over full operating temperature range.
3. Cannot tolerate even a momentary short circuit to ground or either supply.
4. Voltage gain = +1
5. Voltage gain = +1, load resistance = 1 kΩ, load capacitance = 50 pF, output voltage = 100 mV P-P.
6. Input voltage = 0V, digital input voltage = 3.5V
7. Output voltage = 10V step.
8. A power supply voltage as low as ±12V may be used. However, this will cause some degradation in performance.

## TECHNICAL NOTES

1. A printed circuit board with ground plane is recommended for best performance. The supply pins (Pins 5,9) should be bypassed to ground with a 0.01 to 0.1 μF ceramic capacitor as close to the pins as possible.
2. If an external hold capacitor (C<sub>H</sub>) is used, 8 then a noise bandwidth capacitor with a value of 0.1 C<sub>H</sub> (10% of the value of the external hold capacitor) should be connected from Pin 8 to ground. Exact value and type are not critical.
3. The Hold Capacitor (C<sub>H</sub>) should have high insulation resistance and low dielectric absorption to minimize droop error. For operating temperatures up to 70°C, polystyrene dielectric is a good choice. Any PC connections to the hold capacitor terminal (Pin 11) should be kept short and "guarded" by the ground plane to avoid errors due to drift currents from nearby signal lines or power supply voltages.

TYPICAL PERFORMANCE AND DEFINITIONS



SAMPLE AND HOLD DEFINITIONS:

**ACQUISITION TIME:** The time required, after the sample command is given, for the hold capacitor to charge to a full-scale voltage change and then remain within a specified error band around the final value.

**APERTURE TIME:** The time required for the Sample & Hold switch to open, independent of delays through the switch driver and input amplifier circuitry.

**APERTURE DELAY TIME:** The time elapsed from the hold command to the actual opening of the sampling switch.

**APERTURE UNCERTAINTY TIME:** The time variation, or time jitter, in the opening of the sampling switch; also the variation in aperture delay time from sample to sample.

**CHARGE TRANSFER:** The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the hold mode. This is caused by the switch control voltage change coupling through switch capacitance to the hold capacitor. Also called charge dumping or charge injection.

**DRIFT CURRENT:** The net leakage current from the hold capacitor during hold mode.

**HOLD MODE DROOP:** The output voltage change per unit time with the sampling switch open. Commonly expressed in V/seconds or  $\mu\text{V}/\text{microseconds}$

**PEDESTAL ERROR:** For a sample-hold, the change in output voltage from the sample-mode to the hold-mode, with constant input voltage. This error is caused by the sampling switch transferring charge onto the hold capacitor as it opens.

TYPICAL SAMPLE AND HOLD PERFORMANCE AS FUNCTION OF HOLDING CAPACITOR

