

# ADC-303<sup>™</sup> 8-Bit Video Flash A/D Converter

T-51-10-08

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### FEATURES

- 8-Bit resolution
- Speed up to 100 MHz guaranteed
- $\pm 1/2$ LSB linearity
- Input bandwidth 40 MHz
- Output latch and buffer
- Low input capacitance, 35 pF typical

### GENERAL DESCRIPTION

The ADC-303 is a video speed 8-bit flash converter capable of digitizing analog signals at conversion rates up to 100 MHz minimum and with a power consumption of only 1.2 watts at 100 MHz sampling rate.

The 256 clocked comparators have the analog voltage applied to one input and a voltage derived from the reference voltage and reference resistors applied to the other comparator input.

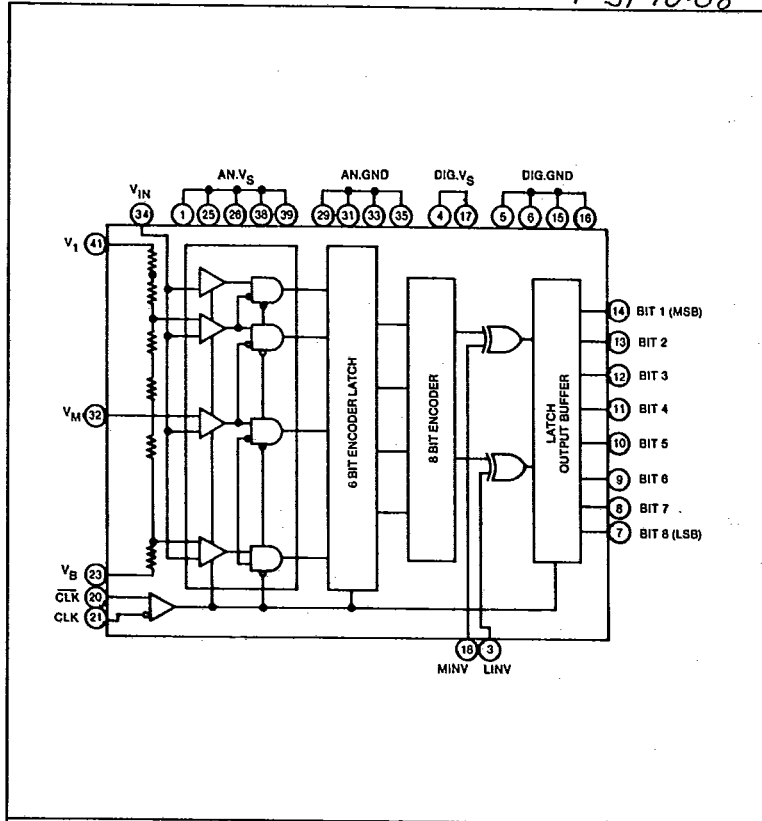
The comparator outputs are 'anded' with adjacent outputs and these outputs latched into a 6-bit encoder. These 6-bit codes are further encoded to 8-bit codes and latched. The final ECL output buffer stage requires external pull down resistors, the output being delayed from the sampling point by the time of one clock cycle.

Output polarity of the MSB and LSB's respectively can be controlled on two digital input lines.

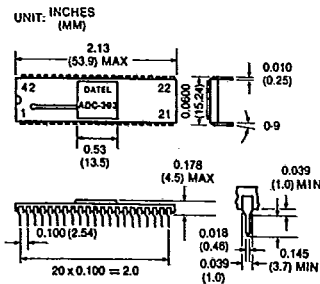
With a reference of -2V the analog input range will be 0 to -2V.

### APPLICATIONS

- High speed data acquisition
- Radar pulse analysis
- TV video encoding
- High energy physics
- Transient analysis
- Medical electronics
- Fluid flow analysis
- Sonar systems



### MECHANICAL DIMENSIONS



### INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	ANALOG SUPPLY V <sub>S</sub> 5.2V	42	N/C
2	N/C	41	REFERENCE V <sub>REF</sub> 0V
3	ENV	40	N/C
4	DIGITAL SUPPLY V <sub>D</sub> 5.2V	39	ANALOG SUPPLY V <sub>A</sub> 5.2V
5	DIGITAL GROUND	38	ANALOG SUPPLY V <sub>A</sub> 5.2V
6	DIGITAL GROUND	37	N/C
7	BIT 8 (LSB)	36	N/C
8	BIT 7	35	ANALOG GROUND
9	BIT 6	34	INPUT
10	BIT 5	33	ANALOG GROUND
11	BIT 4	32	REFERENCE V <sub>REF</sub>
12	BIT 3	31	ANALOG GROUND
13	BIT 2	30	INPUT
14	BIT 1 (MSB)	29	ANALOG GROUND
15	DIGITAL GROUND	28	N/C
16	DIGITAL GROUND	27	N/C
17	DIGITAL SUPPLY V <sub>D</sub> 5.2V	26	ANALOG SUPPLY V <sub>A</sub> 5.2V
18	MINV	25	ANALOG SUPPLY V <sub>A</sub> 5.2V
19	N/C	24	N/C
20	CLK	23	REFERENCE V <sub>REF</sub> -2V
21	CA	22	N/C

**ADC-303**



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**ABSOLUTE MAXIMUM RATINGS**

Power Supply - $V_s$	0 to -7V
Analog Input ( $V_M$ )	+0.5V to $V_s$
Reference Voltage	
$V_T + V_M + V_s$	+0.5V to $V_s$
$ V_T - V_s $	2.5V
Input current at $V_M$	-3 mA to +3 mA
Digital Inputs	0.5V to -4.0V
Digital Output Current	0 to -10 mA
Operating Temp.	-20°C to +100°C
Storage Temp.	-55°C to +150°C
Power Dissipation	3.1 Watts

**TECHNICAL NOTES**

- Even with the input capacitance down to 35 pF, or less, the converter still requires an input amplifier with good drive capability. The amplifier will require wide bandwidth and high slew rate (250V/μS typical) to take full advantage of the 40 MHz bandwidth of the converter.
- The input impedance of the A/D is capacitive which may result in the input amplifier becoming unstable and cause oscillations. A resistor with a value between 2 and 10 Ohms between the amplifier and the input to the converter will stop any oscillations.
- Clock and Clock (ECL) are usually differentially supplied to pins 20 and 21. However a single clock input can be used if a 1000 pF capacitor is added between pin 20 (clock) and pin 16 (digital ground).
- The polarity of the output data is controlled by two polarity inversion inputs, MINV (pin 18) which controls the MSB alone and LINV (pin 3) which controls bit-2 to bit-8 (LSB). The combination of '0's and '1' on these inputs offer the user various code options. Refer to the coding table. Logic level '0' is obtained by leaving inputs open, logic level '1' is obtained by connecting a 3.9K Ohm resistor to digital ground.
- The digital outputs, bits 1 to 8, require pull down resistors, in the range of 500 to 1000 Ohms, connected to the negative supply rail to prevent waveform distortion by reflection.
- The reference voltage range (-2.0V to 0V typical) determines the dynamic range of the input voltage. Adjustments to this range can be made within the range of  $V_s = 2 \pm 0.2V$  and  $V_T = 0V \pm 0.1V$ . The reference input  $V_s$  (pin 23) should be decoupled to analog ground using 1 μF and 0.01 μF capacitors. Improvement in the high frequency stability can be achieved by decoupling terminal  $V_M$  (pin 32) using a 0.01 μF.
- Terminal  $V_M$  is used to achieve a less than  $\pm 1/2$  LSB linearity error. The external circuit to achieve this is shown in the application drawing.
- All pins not being used should be grounded.
- Substantial analog and digital ground planes must be provided. It is recommended that these ground planes are taken to a common point, the power ground line, as close to the ADC-303 as possible.
- The power supplies to analog and digital inputs (-5.2V) should be supplied from separate, isolated power supplies. If one of the power supplies fails or is shorted to ground for more than 1 second there is a possibility the device may be destroyed. Both -5.2V lines should be decoupled using 1 μF and 0.01 μF capacitors located as close to the pins as possible.

**FUNCTIONAL SPECIFICATIONS.**

Typical at +25°C,  $V_s = -5.2$  V dc,  $V_B = -2.0V$  unless otherwise stated.

ELECTRICAL PERFORMANCE	MIN.	TYP.	MAX.	UNIT
Conversion Rate	100	—	—	MHz
Input Capacitance	—	35	40	pF
Input Bias Current				
( $V_M = -1V$ )	—	150	220	μA
Ref. Voltage	-1.8	-2.0	-2.2	V
Reference Resistance				
( $V_T$ to $V_s$ )	70	80	100	Ohms
Offset Voltage $V_T$	6	9	12	mV
$V_s$	14	17	20	mV
Digital Input Voltage $V_{IH}$	-0.7	-0.9	-1.0	V
$V_{IL}$	-1.6	-1.75	-1.9	V
Digital Input Current				
( $V_{IH}$ Typ.) $I_{IH}$	0	—	0.4	mA
( $V_{IL}$ Typ.) $I_{IL}$	-0.05	—	0.35	mA
Digital Output Voltage				
( $R_L = 620$ ) $V_{OH}$	-1.0	—	—	V
$V_{OL}$	—	—	-1.6	V
Integral Non-Linearity				
(100 MHz)	—	—	$\pm 1/2$	LSB
Differential Non-Linearity				
(35 MHz)	—	—	$\pm 1/2$	LSB
Differential Gain	—	—	1.5	%
Differential Phase	—	—	0.5	Deg.
Aperture Jitter	—	15	—	psec.
Supply Voltage	-5.2	-5.2	-5.7	V
Supply Current	-180	-220	-260	mA
Output Data Delay	3.0	3.5	4.2	nSec
( $R_L = 620$ )				
Sampling Delay	1.9	2.2	2.5	nSec

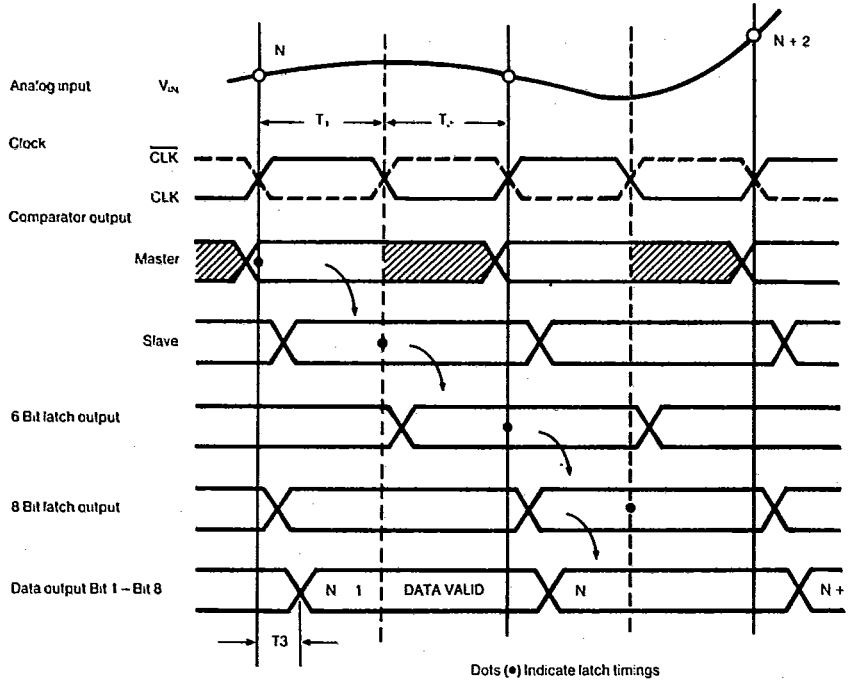
**DIGITAL OUTPUT CODES**

MINV LINV	0 0	0 1	1 0	1 1
0.0000V -0.0078V	1111 1111 1111 1110	1000 0000 1000 0001	0111 1111 0111 1110	0000 0000 0000 0001
-0.9961V -1.0039V	1000 0000 0111 1111	1111 1111 0000 0000	0000 0000 1111 1111	0111 1111 1000 0000
-1.9922V -2.0000V	0000 0001 0000 0000	0111 1110 0111 1111	1000 0001 1000 0000	1111 1110 1111 1111

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TIMING DIAGRAM

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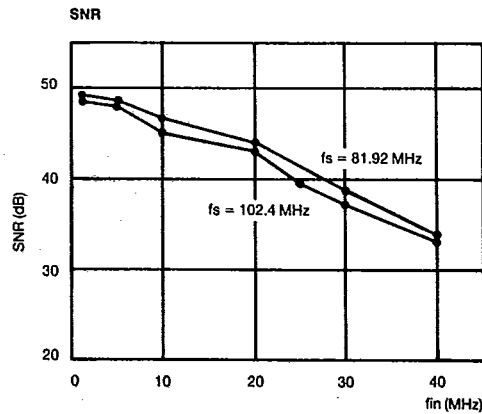
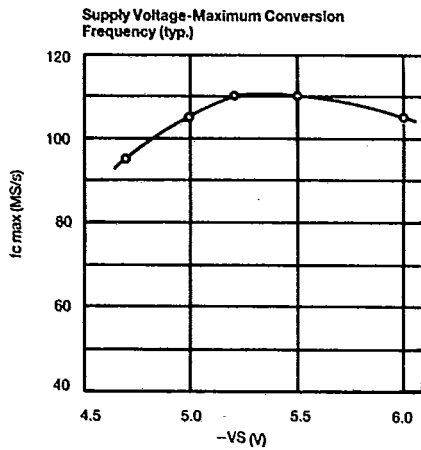
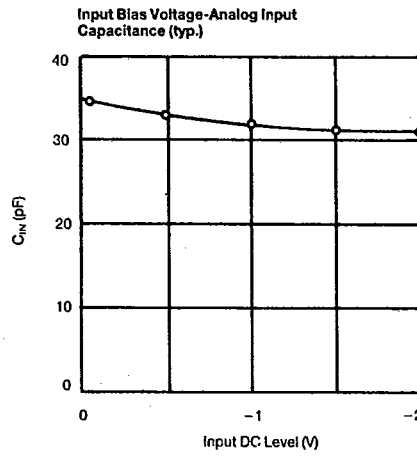
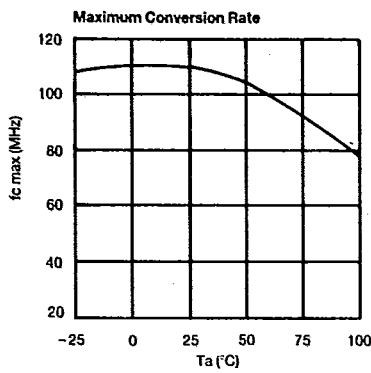
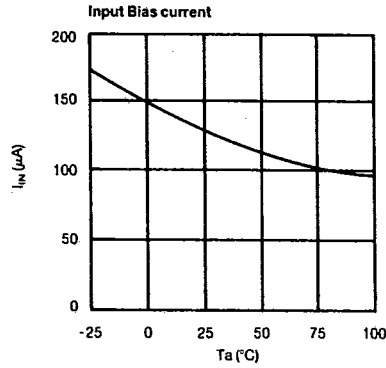
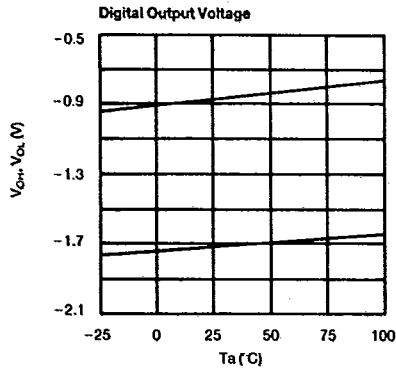
Dots (•) Indicate latch timings

TIMING NOTES

- Both Clock and  $\overline{\text{Clock}}$  are required and the input levels are ECL. The timing  $T_1$  and  $T_2$  should be  $T_1 \text{ min.} = 7.5 \text{ nsec.}$   $T_2 \text{ min.} = 2.5 \text{ nsec.}$
- The positive transition of the clock latches the comparator outputs into the 'and' gates.
- The negative transition latches the 'anded' outputs into the 6-bit encoder.
- The next positive transition will latch the 6-bit encoder output as well as starting the next conversion cycle.
- The 8-bit encoder will appear at the output pins 3.5 nsec. (typical)  $T_3$  after 6-bit encoder output has been latched on the next negative transition of the clock.

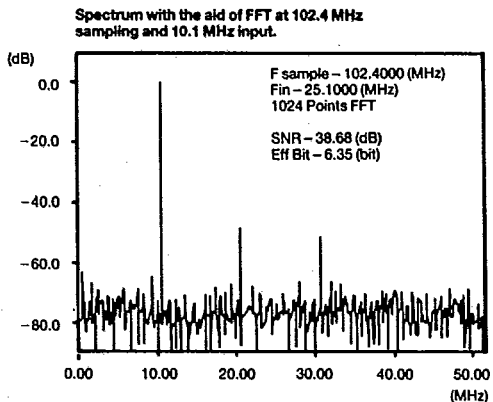
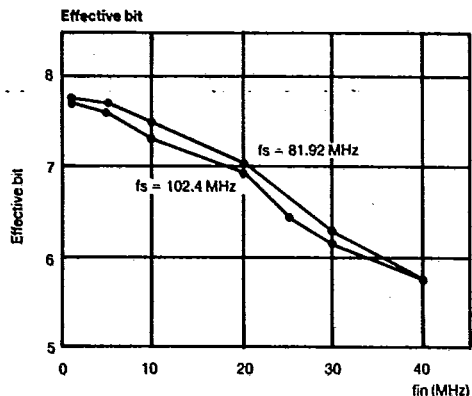
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PERFORMANCE CURVES

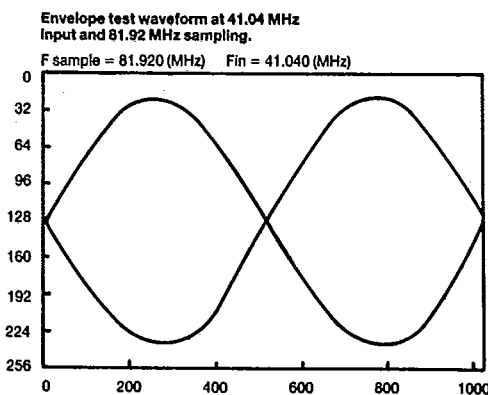
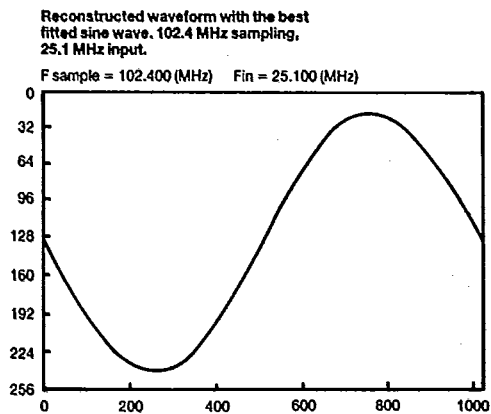
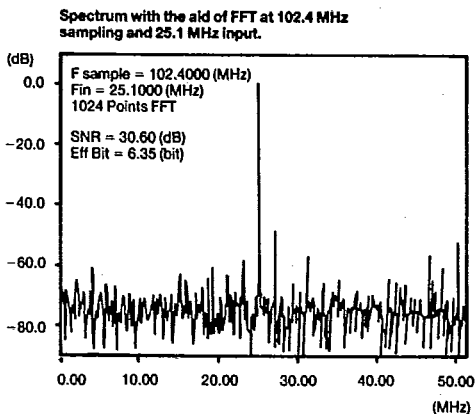
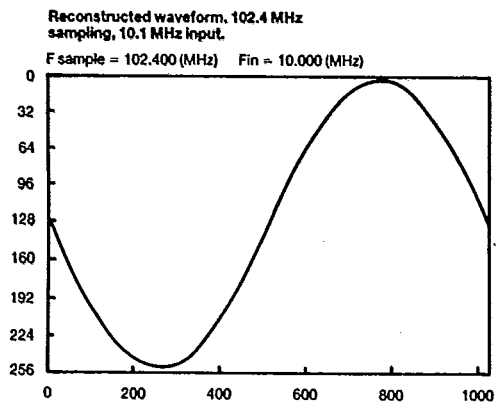


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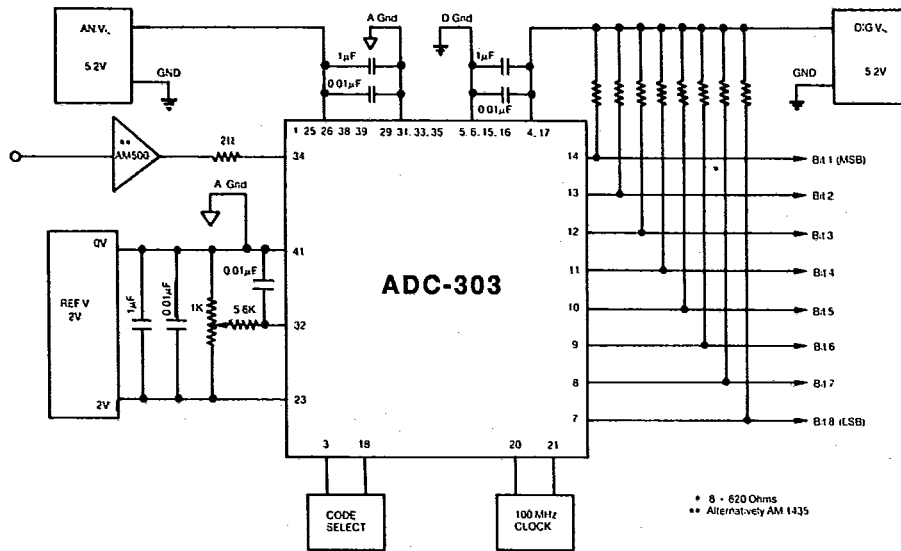


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CONNECTION AND APPLICATION



• 8 - 620 Ohms  
 \*\* Alternatively AM 1435

ORDERING INFORMATION

MODEL NO.	OPERATING TEMPERATURE RANGE
ADC-303	-20°C to +100°C

NOTE: For units with British Standard BS-9000 or other high-reliability processing, contact DATEL.