PLESSEY
Semiconductors

SP1650 (HIGH Z)
SP1651 (LOW Z)
DUAL A/D COMPARATOR

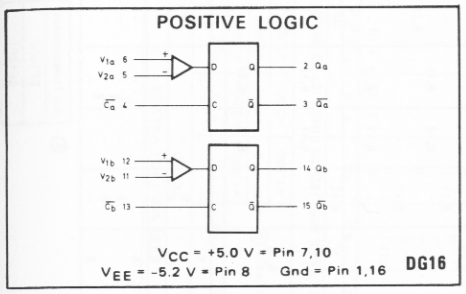


Fig. 1 Logic diagram

FEATURES

- P_D = 330mW typ/pkg (No load)
- t_{pd} = 3.5ns typ. (SP1650)
  = 3.0ns typ. (SP1651)
- Input Slew Rate = 350 V/μs (SP1650)
  = 500 V/μs (SP1651)
- Differential Input Voltage:
  −5.0V to +5.0V (−30°C to +85°C)
- Common Mode Range:
  −3.0V to +2.5V (−30°C to +85°C) (SP1650)
  −2.5V to +3.0V (−30°C to +85°C) (SP1651)
- Resolution: ≤ 20mV (−30°C to +85°C)
- Drives 50Ω lines

The SP1650 and the SP1651 are very high speed comparators utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The SP1650 provides high impedance Darlington inputs, while the SP1651 is a lower impedance option, with higher input slew rate and higher speed capability.

Complementary outputs permit maximum utility for applications in high speed test equipment, frequency measurement, sample and hold, peak voltage detection, transmitters, receivers, memory translation, sense amplifiers and more.

The clock inputs ($\overline{C_a}$ and $\overline{C_b}$) operate from ECL III or ECL 10,000 digital levels. When $\overline{C_a}$ is at a logic high level, Q_a will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). $\overline{Q_a}$ is the logic complement of Q_a. When the clock input goes to a low logic level, the outputs are latched in their present state.

Assessment of the performance differences between the SP1650 and the SP1651 may be based upon the relative behaviour shown in Figs. 5 and 8.

TRUTH TABLE

$\overline{C}$	V_1, V_2	Q_{n+1}	$\overline{Q}_{n+1}$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	Q_n	$\overline{Q}_n$

ϕ = Don't Care

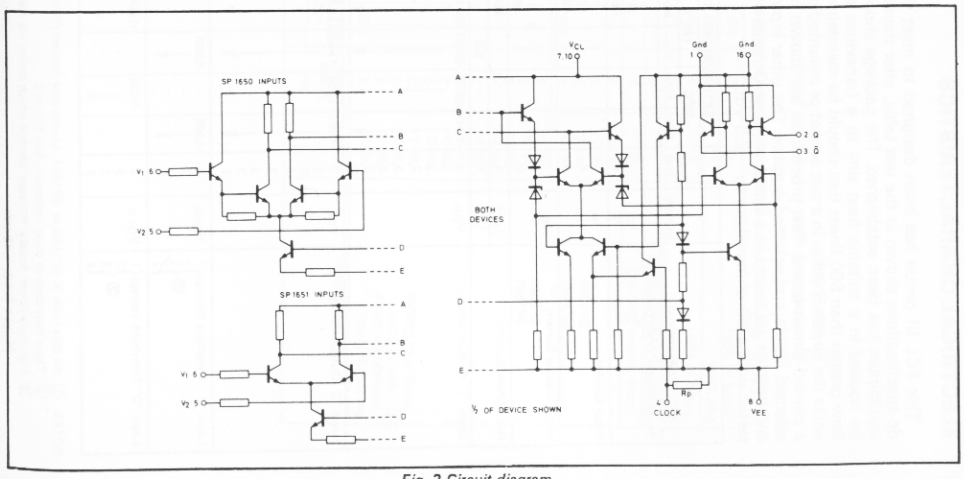


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equiblirium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to −2.0 Vdc.

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③
	TEST VOLTAGE VALUES (Volts)											
-30°C	-0.875	-1.890	-1.180	-1.515	+0.020	-0.020	See Note ④				+5.0	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	+0.020	-0.020					+5.0	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	+0.020	-0.020					+5.0	-5.2

Characteristic	Symbol	Pin Under Test	SP1650/SP1651 Test Limits (1) -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③	Gnd
			TEST VOLTAGE APPLIED TO PINS LISTED BELOW																			
Power Supply Drain Current																						
Positive	I_{CC}	7,10				25*			mAdc		4,13			6,12		–	–		–	7,10	8	1,5,11,16
Negative	I_E	8				55*			mAdc	4,13				6,12						7,10	8	1,5,11,16
Input Current	I_{in}																					
SP1650		6				10			μAdc	4	13			12	–	6	–	–	–	7,10	8	1,5,11,16
SP1651		6				40			μAdc	4	13			12		6	–	–	–	7,10	8	1,5,11,16
Input Leakage Current	I_R																					
SP1650		6				7			μAdc	4	13			12	–	–	–	6	–	7,10	8	1,5,11,16
SP1651		6				10			μAdc	4	13			12	–	–	–	6	–	7,10	8	1,5,11,16
Input Clock Current	$I_{in}H$	4				350			μAdc	4	13			6,12		–	–	–	–	7,10	8	1,5,11,16
	$I_{in}L$	4			0.5	–	–	–	μAdc	–	13			6,12	–	–	–	–	–	7,10	4,8	1,5,11,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4,13				6,12				–	–	7,10	8	1,5,11,16
		2													5,11			–	–			1,6,12,16
		2												–		6,12	5,11	–	–			1,16
		3																5,11	6,12			1,16
		3													6,12	–		–	–			1,5,11,16
		3												5,11		–	–	–	–			1,6,12,16
		3													–	5,11	6,12	–	–			1,16
																–	–	6,12	5,11			1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4,13					6,12	–	–	–	–	7,10	8	1,5,11,16
		2												5,11	–			–	–			1,6,12,16
		2													–	5,11	6,12	–	–			1,16
		3														–	–	6,12	5,11			1,16
		3												6,12		–	–	–	–			1,5,11,16
		3													5,11	–		–	–			1,6,12,16
		3														6,12	5,11	–	–			1,16
																–	–	5,11	6,12			1,16
Logic "1" Threshold Voltage ② 1	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc		13	4	–	6	–	–	–	–	–	7,10	8	1,5,16
2		2		–		–						–	4	–	6	–	–	–	–			
3		3		–		–						4	–	–	6	–	–	–	–			
4		3		–		–							4	6	–	–	–	–	–			
Logic "0" Threshold Voltage ② 1	V_{OLA}	3	–	-1.630	–	-1.600		-1.555	Vdc		13	4	–	6		–	–	–	–	7,10	8	1,5,16
2		3			–							–	4		6	–	–	–	–			
3		2	–		–		–					4	–	–	6	–	–	–	–			
4		2			–							–	4	6	–	–	–	–	–			

NOTES: ① All data is for ½ SP1650 or SP1651 except data marked (*) which refers to the entire package
② These tests done in order indicated. See Figure 6
③ Maximum Power Supply Voltages (beyond which device life may be impaired):
$|V_{EE}| + |V_{CC}| \leq 12$ Vdc

④

All Temperatures	V_{A3}	V_{A4}	V_{A5}	V_{A6}
SP1650	+3.000	+2.980	-2.500	-2.480
SP1651	+2.500	+2.480	-3.000	-2.980

@ Test Temperature	V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①
-30°C	+2.000	See Note ④		+1.040	+2.00	+7.00	-3.20
+25°C	+2.000			+1.110	+2.00	+7.00	-3.20
+85°C	+2.000			+1.190	+2.00	+7.00	-3.20

TEST VOLTAGE VALUES (Volts)

See Figure 4

Characteristic	Symbol	Pin Under Test	SP1650/SP1651 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①	P1	P2	P3	P4
										TEST VOLTAGE APPLIED TO PINS LISTED BELOW										
Switching Times Propagation Delay (50% to 50%) V-Input to Output	t_{6+2+}	2	2.0	5.0	2.0	5.0	2.0	5.7	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{6+2+}	2								–	5	–					–	6	–	–
	t_{6+2+}	2										5					–	–	6	–
	t_{6+3-}	3								5	–	–					6	–	–	–
	t_{6+3-}	3								–	5	–					–	6	–	–
	t_{6+3-}	3								–	–	5					–	–	6	–
	t_{6-2-}	2								5	–	–					6	–	–	–
	t_{6-2-}	2								–	5	–					–	6	–	–
	t_{6-2-}	2								–	–	5					–	–	6	–
	t_{6-3+}	3								5	–	–					6	–	–	–
	t_{6-3+}	3								–	5	–					–	6	–	–
	t_{6-3+}	3								–	–	5					–	–	6	–
Clock to Output ②	t_{4+2+}	2	2.0	4.7	2.0	4.7	2.0	5.2	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
	t_{4+2-}	2								6	–	–	–				5	–	–	
	t_{4+3+}	3								6	–	–	–				5	–	–	
	t_{4+3-}	3								5	–	–	–				6	–	–	
Clock Enable Time ③	t_{setup}	6	–	–	2.5	–	–	–	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
Clock Aperture Time ③	t_{ap}	6	–	–	1.5		–	–	ns	5		–	–	1,11,16	7,10	8	6	–	–	4
Rise Time (10% to 90%)	t_{2+}	2	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{3+}	3	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
Fall Time (10% to 90%)	t_{2-}	2	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{3-}	3	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–

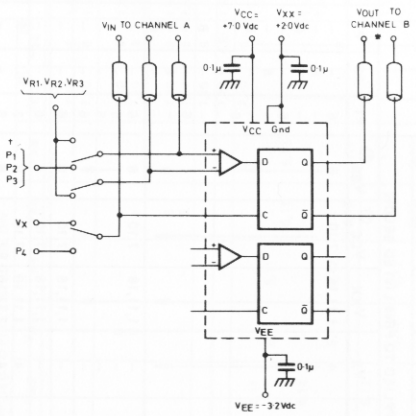
NOTES: ① Maximum Power Supply Voltages (beyond which device life may be impaired:
$|V_{CC}| + |V_{EE}| = 12$ Vdc.

② Unused clock inputs may be tied to ground

③ See Figure 10

④

All Temperatures	V_{R2}	V_{R3}
SP1650	+4.900	-0.400
SP1651	+4.400	-0.900



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

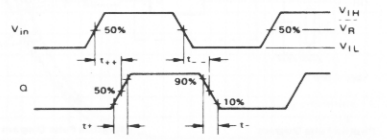
†Refer to Fig. 4 for input pulse definitions.

* Complement of output under test should always be loaded with 50ohms to ground

Fig. 3 Switching time test circuit at +25°C

The pulse levels shown are used to check ac parameters over the full common-mode range.

V – Input to Output

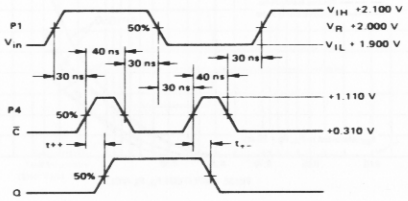


Test pulses: $t_+, t_- = 1.5 \pm 0.2$ ns (10% to 90%)
f = 5.0 MHz
50% Duty Cycle
V_{IH} is applied to $\bar{C}$ during tests.

TEST PULSE LEVELS

	Pulse 1		Pulse 2		Pulse 3	
	SP1650	SP1651	SP1650	SP1651	SP1650	SP1651
V_{IH}	+2.100V	+2.100V	+5.000V	+4.500V	–0.300V	–0.800V
V_R	+2.000V	+2.000V	+4.900V	+4.400V	–0.400V	–0.900V
V_{IL}	+1.900V	+1.900V	+4.800V	+4.300V	–0.500V	–1.000V

Clock to Output



P4: $t_+, t_- = 1.5 \pm 0.2$ ns.

Fig. 4 Switching and propagation waveforms @ 25°C

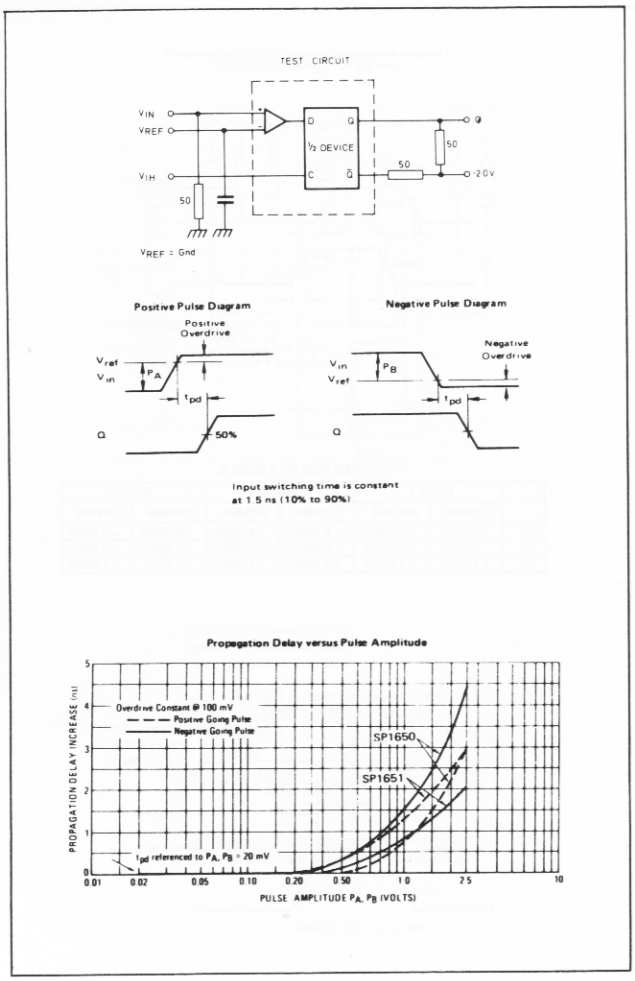


Fig. 5 Propagation delay (t_{pd}) v. input pulse amplitude and constant overdrive

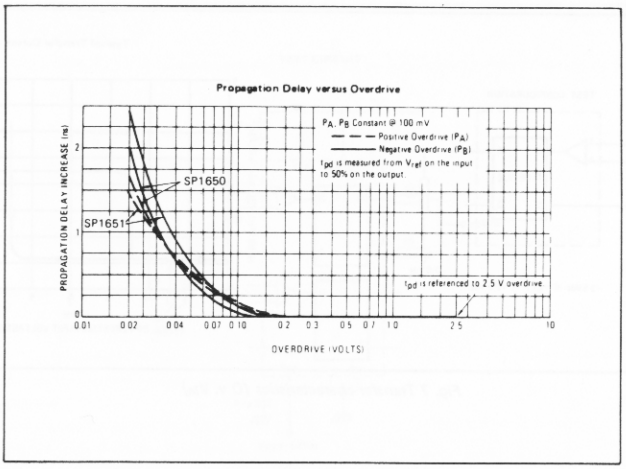


Fig. 5 (continued)

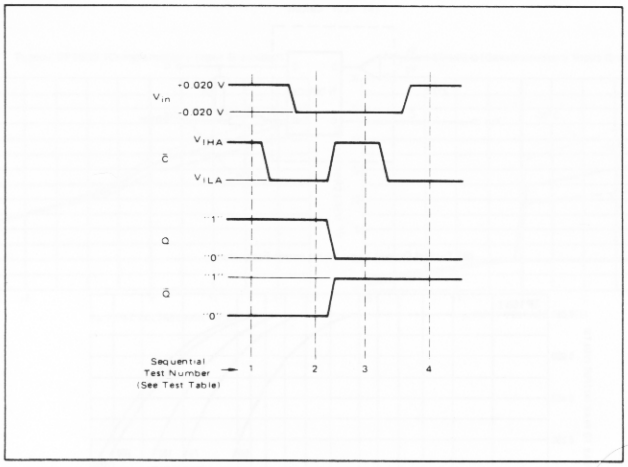


Fig. 6 Logic threshold tests (waveform sequence diagram)

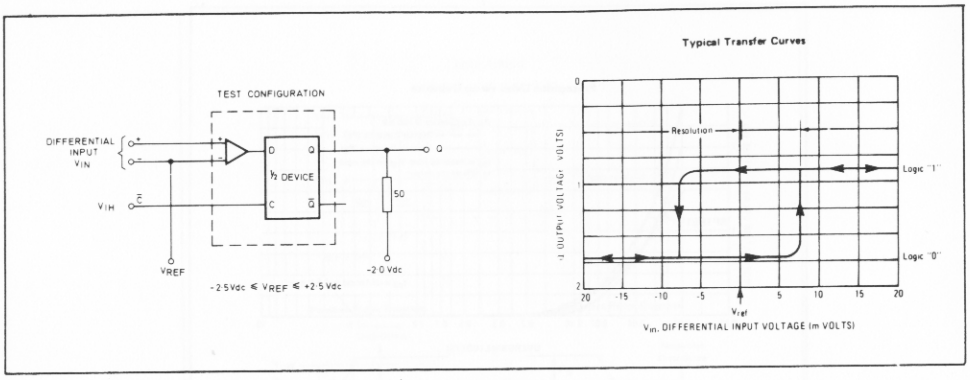


Fig. 7 Transfer characteristics (Q v. Vin)

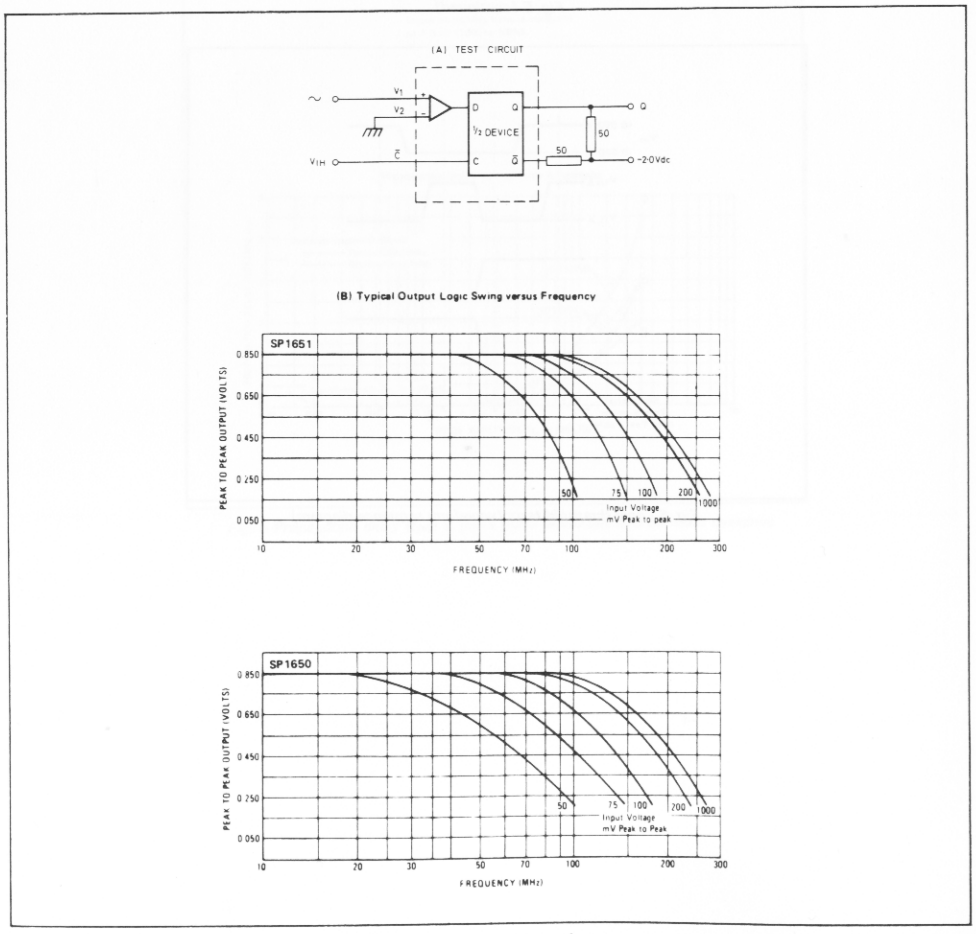
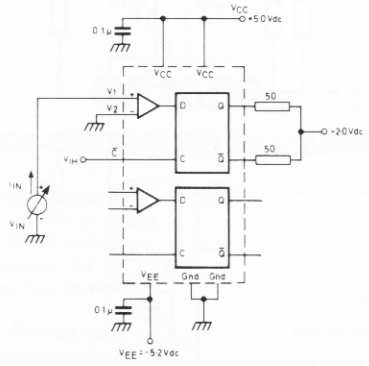


Fig. 8 Output voltage swing v. frequency

TEST CIRCUIT



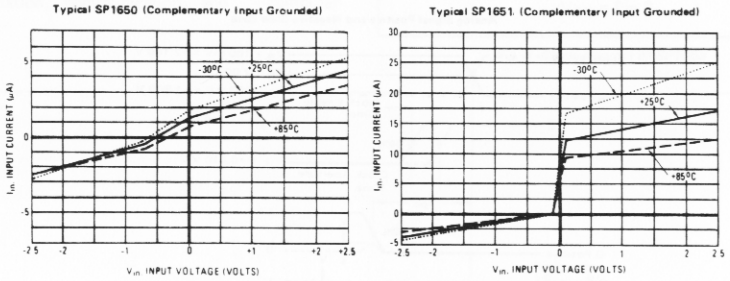
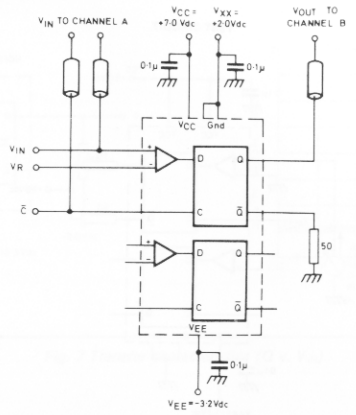


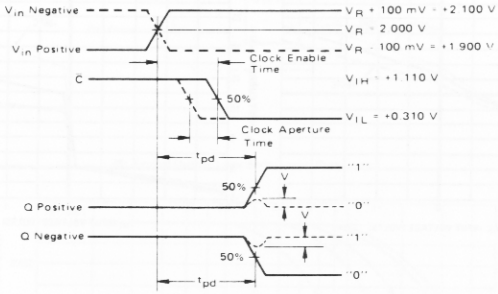
Fig. 9 Input current v. input voltage



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

Analog Signal Positive and Negative Slew Case



——— Clock enable time = minimum time between analog and clock signal such that output switches, and t_{pd} (analog to Q) is not degraded by more than 200ps.

- - - - - Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150 mV.

Fig. 10 Clock enable and aperture time test circuit and waveforms @ 25°C