VITESSE

VSC3139
Data Sheet

3.6Gb/s 72 x 72 Asynchronous Crosspoint Switch

FEATURES

- 72 input by 72 output crosspoint switch
- 3.6Gb/s Non-Return-to-Zero (NRZ) data bandwidth
- Global and per-channel programmable Input Signal Equalization (ISE) and output drive levels
- On-board Pseudo-Random Bit Sequence (PRBS) Generator/Detector
- 2.5/3.3V Complimentary Metal-Oxide Semiconductor/Transistor-Transistor Logic (CMOS/TTL) control Input/Output (I/O)
- Parallel and serial programming modes
- Differential Current Mode Logic (CML) data output driver
- Soft power-down for unused channels
- Secondary access port for configuation and monitoring
- Boundary scan support for data I/O
- 125MHz multimode program port
- Multicast and "striping" programming modes
- On-chip input and output terminations
- Single 2.5V supply, 3.3V option for control port
- 9W/13W typical power in Nominal and High Drive mode
- Integrated temperature sensor/alarm
- High performance, ball-grid array (BGA) package

APPLICATIONS

- Large, 3-stage (Clos) fabrics of up to 2880 x 2880 I/O ports with up to 10 terabytes per second (Tb/s) data throughput
- Dense Wavelength, Division Multiplexing (DWDM) switches
- Wavelength routers
- Storage Area Network (SAN) switch fabrics
- Packet-switching fabrics

GENERAL DESCRIPTION

The VSC3139 is a 72 x 72, asynchronous, crosspoint switch. It is designed to carry broadband data streams in a variety of applications. Its fully non-blocking switch core is programmed using a multi-mode port interface that allows random access programming of each I/O port. A high degree of signal integrity is maintained throughout the device by virtue of its fully differential signal paths.

Each data output can be programmed to connect to any one of the 72 inputs. The signal path is unregistered and fully asynchronous, so there are no restrictions on the phase, frequency, of signal pattern on any input. Each high-speed output is a fully differential, switched current driver with on-die terminations for maximum signal integrity. Data inputs are terminated on die using 100Ω resistors between true and complement inputs with a common connection to an internal bias source that facilitates AC coupling to the switch inputs.

The VSC3139 provides a multi-mode, programming interface that allows commands to be sent as either serial data or multiplexed parallel data. Core programming can be sequential on a port-by-port basis, or multiple program assignments can be queued and issued simultaneously using the CONFIG bit. By default, the device's $\overline{\text{INIT}}$ feature resets the entire switch to a "straight-through" configuration (A0 to Y0, A1 to Y1, and so on); alternatively, the user can configure $\overline{\text{INIT}}$ to initialize to any other configuration.

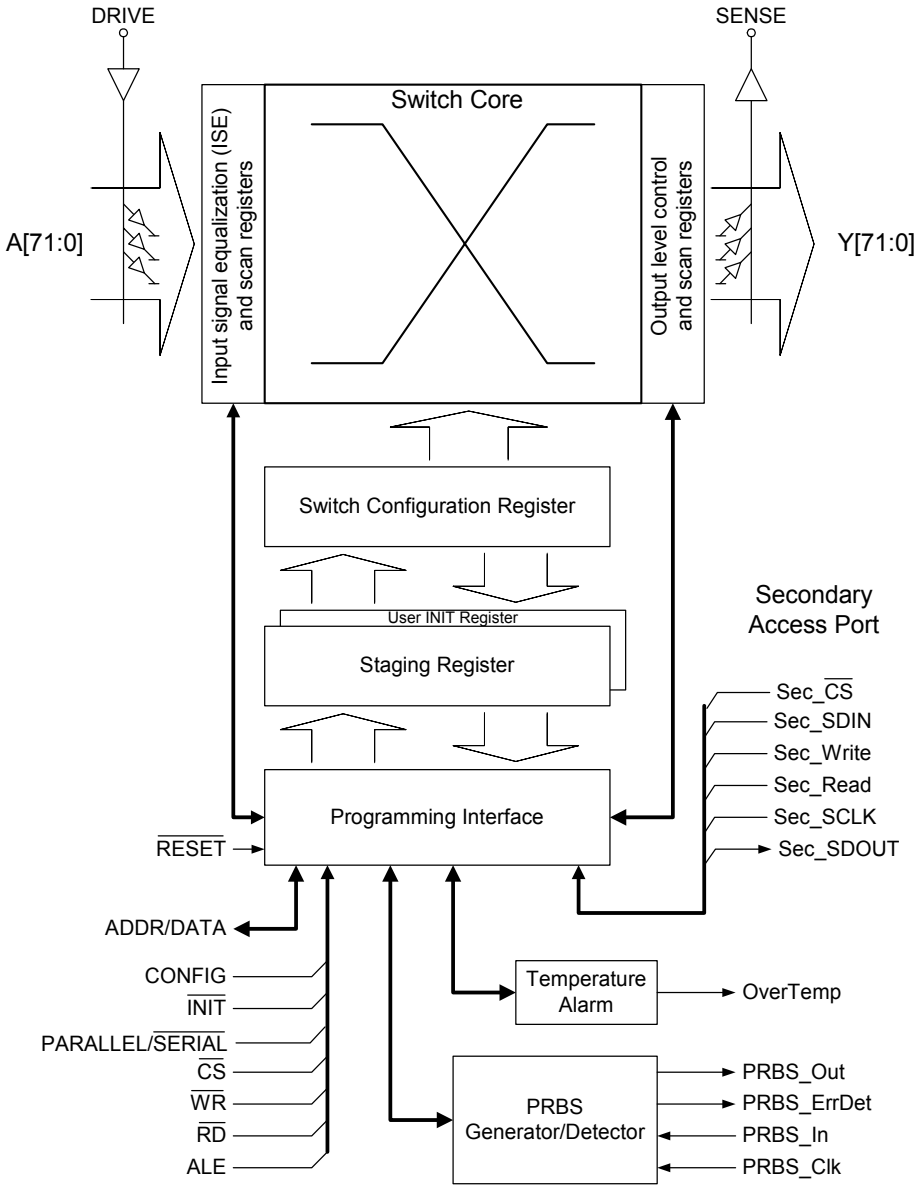
The VSC3139 is programmed using an 11-bit, multiplexed address/data (ADDR/DATA) bus in conjunction with the device's ALE, $\overline{RD}$, $\overline{WR}$, CONFIG, and $\overline{INIT}$ pins. CONFIG and $\overline{INIT}$ signals can also be set via an internal control register to reduce the number of signals required to interface with the switch.

Disabling $\overline{INIT}$ and CONFIG in software locks in programming of switch connections. This is accomplished by setting the appropriate bits in the Setup register to zero, blocking input on these controls and preventing them from changing the switch configuration.

Unused channels can be powered down to allow efficient use of the switch in applications that require only a subset of the channels. Power-down is enabled in software by programming individual unused outputs with a power-down code.

A Secondary Access Port allows asynchronous readback and configuration control to take place even while the primary programming port is in use.

VSC3139 Functional Block Diagram



FUNCTIONAL DESCRIPTION

DRIVE Input

The VSC3139 provides a DRIVE input that can be connected internally to any of the 72 data input connections. By connecting an external signal to the DRIVE input and then switching it to one of the data inputs, a test signal can be placed on that input.

The DRIVE input can be used to verify signal path integrity. Because of this, input to the switch is not multiplexed between the DRIVE input and data input; multiplexing the input would alter the configuration after an integrity test. Instead, the signal from the DRIVE input is superimposed onto the data input path. For correct operation, the signal present on the selected input must either be in a neutral state or in a high-impedance state to allow the DRIVE inputs to influence the input.

The DRIVE input can also be used in conjunction with the SENSE output and an external test generator/receiver to verify programmed signal path integrity.

The DRIVE input can be programmed to drive any or all of the 72 data inputs. Writing to the appropriate address either connects or disconnects a data input from the specified DRIVE input.

SENSE Output

The VSC3139 has a SENSE output that can be used to monitor any one of the 72 data outputs. This SENSE output monitors the data output signal at the package pin, thereby facilitating true verification of the complete signal path through the switch.

The SENSE output can also be used in conjunction with the external monitoring circuit and the DRIVE input to determine the presence of a signal on any output, or to verify signal path integrity.

Boundary Scan Support

The VSC3139 incorporates registers that can be used to drive and sense the state of every pin of the high-speed data paths. These registers can be accessed through the programming port in serial mode, allowing the chip to be fully tested using only five active pins.

Power-On RESET

The VSC3139 has a built-in power-on RESET function to ensure the matrix is fully disconnected and powered off prior to its being powered up. When the device is powered up, the switch draws additional power as each output is programmed. The power-on RESET circuit trip point is between 1.9VDC and 2.1VDC. Care must be taken to keep power supply excursions above 2.2VDC by providing adequate supply decoupling.

Temperature Sensor/Alarm

The VSC3139 has circuitry that detects and flags temperatures exceeding a user-set range. The temperature range is set using "Register 5: Temperature Sensor". The device's temperature alarm is asserted when the die temperature meets or exceeds the maximum temperature in the user-set range. There are 15 temperature range presets between 30ºC and 160ºC. Each range is approximately 8ºC, ± 8ºC.

PRBS Generator/Detector

The PRBS Generator/Detector is capable of generating and detecting any of the four NRZ patterns described in the "Register 8 (page 21)" and "Register 10 (page 22)" data tables that appear later in this document. The main purpose of the PRBS Generator/Detector is in switch diagnostics and signal tracing. For more information, see the block diagram of the PRBS Generator/Detector in Figures 1 and 2.

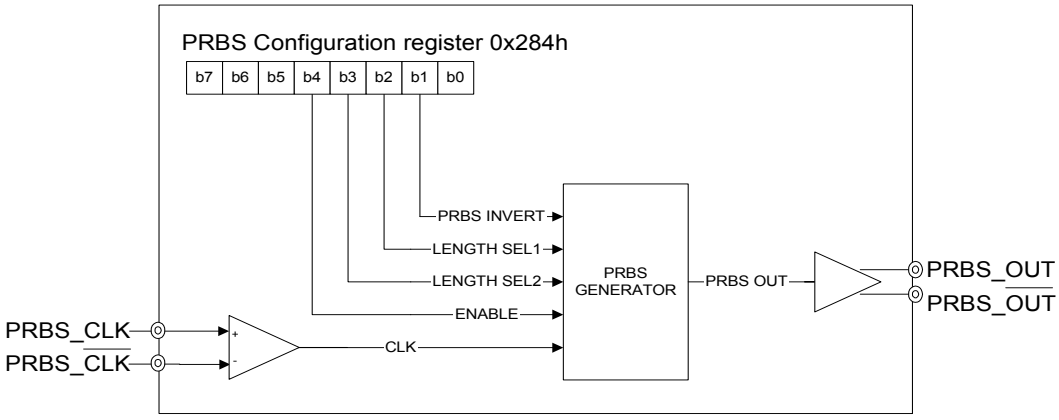


Figure 1. PRBS Generator

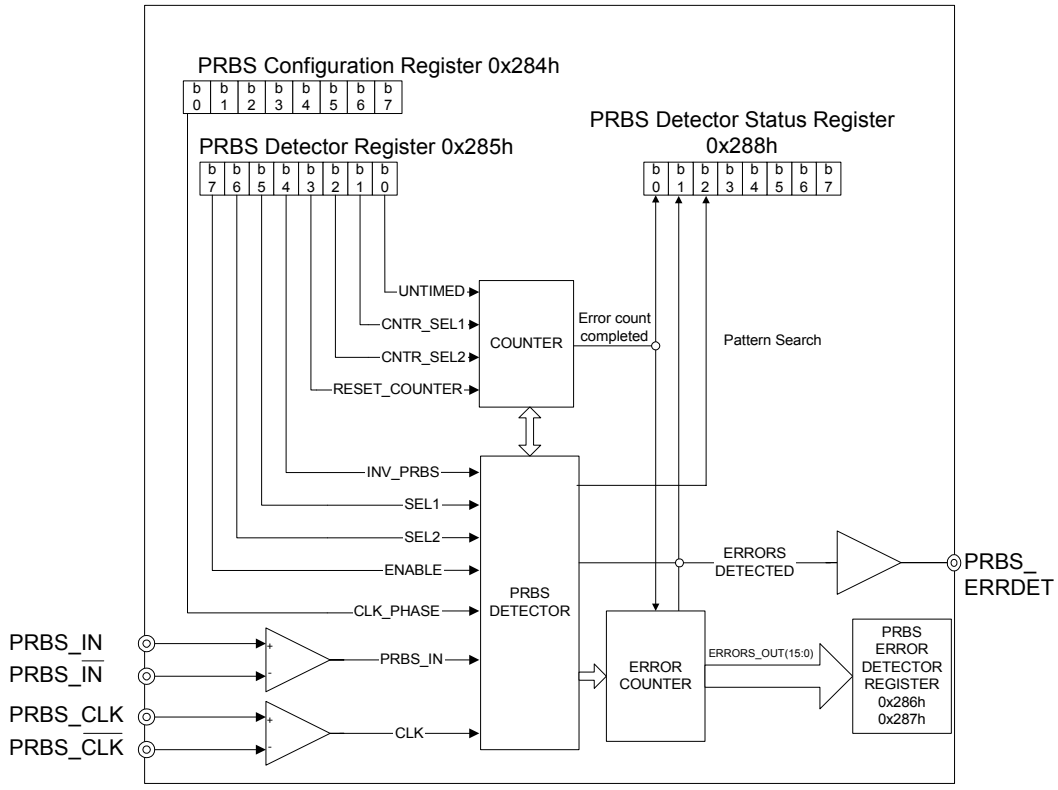


Figure 2. PRBS Error Detector

Figure 3 illustrates how the PRBS function can be connected to the switch core for signal path tracing to and from the switch.

Refer to Figure 3 and use the following set of steps to effect a trace.

1. Connect PRBS_OUT and PRBS_$\overline{\text{OUT}}$ to DRIVE and $\overline{\text{DRIVE}}$, respectively.
2. Connect SENSE and $\overline{\text{SENSE}}$ to PRBS_IN and PRBS_$\overline{\text{IN}}$, respectively.
3. Select channel to send pattern through.
4. Generate pattern with PRBS generator.
5. Check Detector for errors.

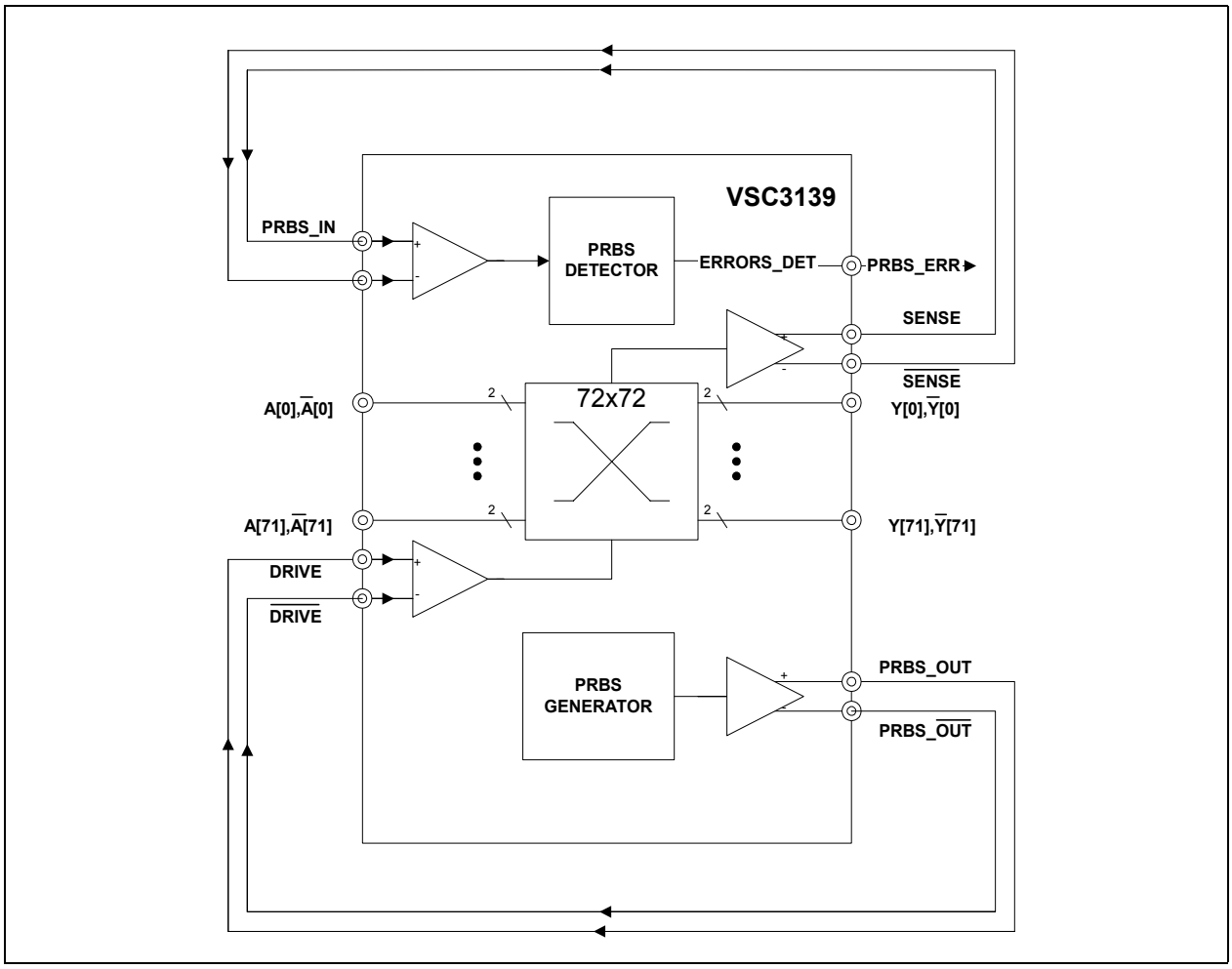


Figure 3. PRBS Connection Example

PROGRAMMING INTERFACE

The VSC3139 programming interface uses a multiplexed address/data bus. The ALE signal differentiates whether the binary word on the multiplexed bus is address or data information. Table 1 lists the conventions used in this document to describe the various terms used in the programming interface.

Table 1. VSC3139 Data Sheet Programming Interface Conventions

Convention	Description
SIGNAL NAME	Active HIGH signal
$\overline{\text{SIGNAL NAME}}$	Active LOW signal
ADDR	Identifies OUTPUT channel to be programmed
DATA	Identifies INPUT channel to be programmed
1	A logic level high signal. Also denoted by ‘HIGH’
0	A logic level low signal. Also denoted by ‘LOW’

Register Use

All registers are accessed in the manner described in the programming interface description for parallel and serial read and write functions. Each register has a corresponding address which, when written to with a data word, alters the functions defined for that register (see “Registers” on page 13). Table 4 on page 11 provides an overview of all of the device registers, including detailed descriptions of the functions controlled in each register.

Note that all bits in all registers initialize to 0.

Parallel Mode—Write Operation

Parallel mode is enabled when PARALLEL/$\overline{\text{SERIAL}}$ = 1. When ALE = 1, the information on the ADDR/DATA bus is used as the address and it specifies the OUTPUT port that is being programmed in the write cycle. The falling edge of the ALE pin latches the address value. When ALE = 0, the information on the ADDR/DATA bus designates the INPUT port that is to be connected to the previously selected OUTPUT port. The connection between the specified input and output is programmed into memory when $\overline{\text{WR}}$ = 1.

When CONFIG = 1, all new programming data is transferred directly to the switch core and any new connections are configured as they are entered. When CONFIG = 0, newly programmed connections are held in staging registers. Asserting CONFIG = 1 transfers the data from the staging registers to the switch core independent of other control signals so that any changes occur concurrently. CONFIG may be tied HIGH so that all programming changes take effect sequentially as they are written. Alternatively, it may be toggled HIGH and LOW to store multiple programming steps and activate them simultaneously.

Figure 5 on page 29 shows the programming sequence for parallel mode write operations.

Parallel Mode—Read Operation

The VSC3139 supports parallel readback using the multiplexed bus to read programming information from the switch fabric. The falling edge of ALE latches the address (OUTPUT) value of the connection to be read. The chip then drives the requested data out onto the bus after the falling edge of $\overline{RD}$, where it remains valid until $\overline{RD}$ = 1.

Figure 5 on page 29 shows the programming sequence for parallel mode read operations.

Serial Mode—Write Operation

Serial mode operation is enabled when PARALLEL/$\overline{SERIAL}$ = 0. In this mode, the ADDR/DATA[0] pin becomes the serial data input (SDIN) pin and the ADDR/DATA[1] pin becomes the serial clock (SCLK) pin which is rising-edge-triggered.

In addition, in serial mode the sense of the $\overline{WR}$ pin is inverted from parallel operation. That is, the pin should normally be set LOW, and set HIGH to write the address and data information to the programming port. A serial word of the form [Output][Input] is shifted into the internal shift register (MSB-first), and the $\overline{WR}$ pin is set HIGH, coincident with the last bit of the data word to indicate the last bit of a connection. This transfers the input identifier to the staging register of the addressed output. CONFIG is then asserted (1, asynchronously) to transfer one or more program commands to the switch core. The programming information that is shifted in during the write cycle is repeated back to the SDOUT (ADDR/DATA[2]) pin, but delayed by 22 clock cycles. This allows for easy confirmation of the previous programming step. The output field is 11 bits long, representing the binary numerical identifier of the output to be programmed. The input field is also 11 bits long, representing the numerical identifier of the input that will be connected to the specified output.

Figure 7 on page 30 shows the programming sequence for serial mode write operations. During normal Serial port operations, the ALE pin must be held LOW. Setting ALE HIGH is used in Serial Multicast programming mode.

Serial Mode—Read Operation

During serial mode read back, the sense of the $\overline{RD}$ pin is inverted from its operation during parallel mode. To read back information about a specific output connection, the address corresponding to the output of interest is shifted in while $\overline{RD}$ is held LOW. $\overline{RD}$ is set HIGH with the last bit of the output address and is held HIGH for three clock cycles thereafter. The data begins to be shifted out on the SDOUT pin beginning four SCLK cycles after $\overline{RD}$ was initially set HIGH and for the following 11 clock cycles.

Figure 6 on page 30 shows the programming sequence for serial mode read operations.

INIT

Asserting the $\overline{INIT}$ pin or the $\overline{INIT}$ bit in the Control register activates a preset connection matrix. The $\overline{INIT}$ feature connects the inputs to the outputs in a “straight-through” fashion. Each input is connected to the output of the same value. For example, A0 -> Y0, A1 -> Y1 … A71 -> Y71. Asserting $\overline{INIT}$ will program all connections without exception.

To prevent accidental activation of this feature, disable the $\overline{INIT}$ function in the Setup register.

Note that using the $\overline{INIT}$ feature to program the VSC3139 into a “straight-through” configuration may cause excessive power supply droop due to the large transient currents when the switch is re-configured in this manner. Adequate power supply filtering/decoupling must be implemented close to the VSC3139 to prevent activation of the power-on RESET circuitry. Power supply transients/droop must be kept above 2.2VDC.

Software Power-Down

With this feature, unused outputs may be disabled using software controls. This is accomplished by programming each unused output with a power-down code. Programming a valid input address will reactivate the channel.

It is recommended that any changes in power programming be executed only as part of an initialization sequence. This will guard against the effects of any switching transients that might result from changing the power supply current suddenly.

Multicasting Mode

Multicast mode provides programming efficiency when a single input is to be connected to multiple outputs. By modifying the use of the ALE bit, it is possible to latch the DATA[10:0] value, and use it to represent the input value in subsequent programming steps.

To use multicast mode, ALE is held LOW while the input to be multicasted is written to the data word space of the Switch Array Connection register (or the multicast input storage register). ALE is then raised and held HIGH for programming steps to follow. Connections to the saved input value are programmed solely with the rising edge of the $\overline{WR}$ control signal.

Figure 7 on page 30 shows the programming sequence in parallel mode.

Normal programming is resumed by following the standard programming sequence. The input value is retained as long as ALE remains HIGH but will change once ALE is brought LOW. The input value will also be cleared when information is read from the control interface regardless of the value of ALE.

Multicast is also available in serial programming mode. ALE is held LOW during normal operation of the serial port. To initiate Multicast during serial programming, the first connection is made in the regular manner by first shifting in the 11-bit address and then the 11-bit DATA. The $\overline{WR}$ signal is raised HIGH to clock in the last bit and then negated at the next falling edge of SCLK. As the $\overline{WR}$ signal is negated, the ALE control is raised, prior to the next rising edge of SCLK. As long as ALE is held HIGH, the input port that was designated in the data portion of the first programming sequence will be retained. To configure the outputs after the first connection, only the ADDR value is shifted in and written. The value will also be cleared during a read instruction regardless of the sense of ALE.

Figure 8 on page 31 shows the programming sequence in serial mode.

Address Striping Mode

Setting bit 5 of the Switch Configuration register enables striping mode, which allows groups of four inputs to be connected to four outputs with a single programming instruction.

The groups are predetermined and have been selected according to the physical locations of their pins on the package and their numerical ordering. Because even and odd inputs and outputs are on opposite sides of the chip, the groups consist of consecutively numbered even and odd inputs or outputs. The end result is that the inputs and outputs are arranged in 18 “stripes”, and any of the 18 input stripes can be connected to any of the 18 output stripes.

Programming of the connections is accomplished by using only the nine MSBs of the ADDR/DATA bus. The two LSBs of the each address or data word should be ignored. For example, the ADDR/DATA word ‘00000010000’b’ specifies stripe 4, which includes inputs or outputs 16, 18, 20, and 22.

A complete list of the ADDR/DATA words is shown in Table 2 on page 10.

In Striping mode, the only functionality that is striped is the switch core programming. All other functions such as readback, SENSE control, DRIVE control, precompensation, and output drive level select are accessed and programmed individually.

Table 2. Address Striping Mode I/O Grouping

Group Number	Input/Output Designations	Group Address	Group Number	Input/Output Designations	Group Address
0	0, 2, 4, 6	00000000000	1	1, 3, 5, 7	00000000100
2	8, 10, 12, 14	00000001000	3	9, 11, 13, 15	00000001100
4	16, 18, 20, 22	00000010000	5	17, 19, 21, 23	00000010100
6	24, 26, 28, 30	00000011000	7	25, 27, 29, 31	00000011100
8	32, 34, 36, 38	00000100000	9	33, 35, 37, 39	00000100100
10	40, 42, 44, 46	00000101000	11	41, 43, 45, 47	00000101100
12	48, 50, 52, 54	00000110000	13	49, 51, 53, 55	00000110100
14	56, 58, 60, 62	00000111000	15	57, 59, 61, 63	00000111100
16	64, 66, 68, 70	00001000000	17	65, 67, 69, 71	00001000100

Secondary Access Port

The Secondary Access Port is an interface to the VSC3139 registers that operates concurrently with the primary programming interface. The main purpose of the Secondary Access Port is to facilitate monitoring and to maintain the operational state of the switch (verify and monitor port connections, die temperature, set drive and equalization levels, and so on) without interrupting the primary port programming operations. The Secondary Access Port allows the primary port to focus strictly on establishing connections while the secondary port performs all other operations “off line”.

Before it can be used, the Secondary Access Port must be enabled using the Secondary Access Port Enable bit [7] in the Switch Configuration register (281’h). This bit allows the primary port controller to grant or deny access of the Secondary Access Port as required. If the intention is to have the Secondary Access Port enabled continously, then this bit only needs to be set once during intialization.

To protect the integrity of the Primary Port programming operations, there are two areas of the VSC3139 that are not writeable by the Secondary Access Port. The Switch Connection registers at addresses 000h to 08Fh, and the first two Configuration registers at addresses 280’h and 281’h (register 1 and register 2) may be read by the Secondary Access Port but can only be written to through the Primary Port.

The two interfaces share some logic, therefore care should be exercised when executing certain concurrent operations. In the event that coincident operations are in conflict, an arbitration circuit will grant control as appropriate. A conflict is defined as an overlap of an $\overline{RD}$ or $\overline{WR}$ assertion on the primary port with an assertion of the SecRead or SecWrite signals on the Secondary Access Port. There is one exception to this rule, and that is when the primary port writes a switch connection. The Secondary Access Port cannot write switch connections, so there is never conflict when the primary port writes a connection, regardless of the activity on the Secondary Access Port.

The Secondary Access Port provides an indication when a read or write operation has been overridden by a Primary Port operation. Upon completion of a successful write operation, the Secondary Access Port echoes back the address and data bits following the SecWrite pulse. In the event of a failed write operation on the Secondary Access Port, the echoed data stream is fully or partially inverted.

For a Secondary Access Port read, the 12th bit (the bit after the last bit of valid data) indicates the status of the read. If the bit is a 1, then the previous 11 bits are correct. If the 12th bit is a 0, the last read operation was interrupted by an operation on the primary port and the data is corrupt. The primary port is only overridden when a read operation conflicts with a write operation on the Secondary Access Port. In this case, there is no indication of the failed read. In the event the primary port needs to perform uninterrupted read operations, the Secondary Access Port can be disabled.

Table 3 shows the decision matrix for conflicts between the primary and secondary ports.

Table 3. Programming Port Conflict Resolution Decision Matrix

Conflict Combinations	Primary Port Write	Primary Port Read
Secondary Port Write	**Result:** Priority given to primary port. **Indication:** SecWrite echoed on SecSDOUT will be fully or partially inverted. **Exception:** Primary port writes to connection matric do not conflict with secondary port writes.	**Result:** Priority given to secondary port. **Indication:** None
Secondary Port Read	**Result:** Priority given to primary port. **Indication:** 13th bit of the SecSDOUT will be 0.	**Result:** Priority given to primary port. **Indication:** 13th bit of the SecSDOUT will be 0.

Table 4. VSC3139 Register Map

Register Name	ADDR[10:0]	DATA[10:0]										
		Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Switch Array Connection	0'h - 47'h	Input Connections 0'h Through 47'h										
Switch Setup	280'h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	CONFIG Register	INITB Register	CONFIG Disable	INITB Disable
Switch Configuration	281'h	Not Used	Not Used	Not Used	Secondary Access	Not Used	Address Striping	Staging Readback	Switch State Store	User INITB	Software CONFIG	Software INITB
DRIVE/SENSE Control	282'h	Not Used	Not Used	Not Used	Not Used	Global SENSE	Global DRIVE	DRIVE Input Select				
SENSE Connection	300'h	Not Used	Drive Level	Power-On State	Address of Output Port Connection to SENSE							
Temperature Sensor	28B'h	Not Used	Not Used	Not Used	Current Chip Temperature				Alarm Threshold Temperature			
Global Input Channel Configuration	283'h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Global Clear for Equalization		Global Set for Equalization	
Individual Input Channel Configuration	600'h - 647'h	Not Used	Not Used	Scan State	Equalization State		Drive Input Connection State		Drive Input Source Select			
PRBS Generator Configuration	284'h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	PRBS Control	PRBS Pattern Length Control		Invert Pattern	Invert Clock
PRBS Receiver/ Error Detector Configuration	285'h	Not Used	Not Used	Not Used	Receiver Control	Receiver Pattern Length Control		Input Pattern	Detector Reset	Detection Pattern Length Control		Error Run Length

Table 4. VSC3139 Register Map (continued)

Register Name	ADDR[10:0]	DATA[10:0]										
		Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRBS Receiver/ Error Count Read	286'h=LS Byte 287'h=M SByte	Not Used	Not Used	Not Used	Error Count							
PRBS Error Status	288'h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Pattern Search	Count Period	Error Flag
Global Output Level Control	28A'h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Output Level HIGH	Output Level Nomi-nal
Individual Output Level Control	400'h - 447'h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Over-ride Value	Output Over-ride	Output Control	Output Status
Boundary Scan Control	289'h	Not Used	Not Used	Not Used	Global Override Value		Global Output Override		Not Used	Not Used	Not Used	Latch Input
User Status	28C'h - 28F'h	Storage Registers for Transfer Between Primary and Secondary Ports										

REGISTERS

Switch Setup and Configuration

Register 1: Switch Setup

Reg Name:	Switch Setup	**Reg. Address:**	280'h
Reg Type:	R/W		
Description:	Configuration for various modes of operation.		

Bit(s)	Bit Description	Reset Value	R/W
10-4	Not used		
3	Input pin or software control for CONFIG 0 = Use input pin for CONFIG control 1 = Use register for CONFIG control	0	R/W
2	Input pin or software control for $\overline{\text{INIT}}$ 0 = Use input pin for $\overline{\text{INIT}}$ control 1 = Use register for $\overline{\text{INIT}}$ control	0	R/W
1	CONFIG lockout 0 = CONFIG function enable 1 = CONFIG function disable (overrides bit 3)	0	R/W
0	$\overline{\text{INIT}}$ lockout 0 = $\overline{\text{INIT}}$ function enable 1 = $\overline{\text{INIT}}$ function disable (overrides bit 2)	0	R/W

$\overline{\text{INIT}}$ Lockout

In order to prevent accidental reprogramming of the switch interconnects, the VSC3139 programming interface provides the option of disabling this feature through software. Setting this bit in the Switch Setup register to a 1 will inhibit the use of either the external $\overline{\text{INIT}}$ pin or the $\overline{\text{INIT}}$ bit in the Switch Configuration register from reprogramming the interconnects.

On power-up, this bit is 0 and $\overline{\text{INIT}}$ is enabled.

CONFIG Disable

In order to prevent accidental reprogramming of the switch interconnects, the VSC3139 programming interface provides the option of disabling the CONFIG feature using the software. Setting the CONFIG bit in the Setup register to a 1 inhibits the use of either the external CONFIG pin or the CONFIG bit in the Control register from reprogramming the interconnects.

On power-up, this bit is 0; CONFIG is enabled.

Register 2: Switch Configuration

Reg Name:	Switch Configuration	**Reg. Address:**	281'h
Reg Type:	R/W		
Description:	Provides access to features and external pin functions via the programming interface. Writing updates the value and reading returns the current settings.		

Bit(s)	Bit Description	Reset Value	R/W
10-8	Not used		
7	Secondary access port enable 0 = Disable secondary access port 1 = Enable secondary access port	0	R/W
6	Not Used		
5	Address stripping mode select 0 = Standard address mode 1 = Address stripping mode	0	R/W
4	Staging readback select 0 = Read present switch configuration 1 = Read pending switch configuration	0	R/W
3	Save User $\overline{\text{INIT}}$ The rising edge of the signal stores the user programmed switch configuration in the user programming registers	0	R/W
2	User $\overline{\text{INIT}}$ programming 0 = Straight-through configuration upon $\overline{\text{INIT}}$ asserted LOW 1 = User programmed switch configuration upon $\overline{\text{INIT}}$ asserted LOW, stored using bit 3 of this register	0	R/W
1	Software programmable CONFIG 0 = CONFIG LOW when bit 3 of Switch Setup register, address 280'h, is 1 1 = CONFIG HIGH when bit 3 of Switch Setup register, address 280'h, is 1	0	R/W
0	Software programmable $\overline{\text{INIT}}$ 0 = $\overline{\text{INIT}}$ active when bit 3 of Switch Setup register, address 280'h, is 1 1 = $\overline{\text{INIT}}$ inactive when bit 3 of Switch Setup register, address 280'h, is 1	0	R/W

CONFIG and $\overline{\text{INIT}}$

The functionality of the CONFIG and $\overline{\text{INIT}}$ pins is duplicated in the two LSBs of the Control register. Writing to either of these bits has the same effect as driving the external pins to the same value. These bits are multiplexed with the external pins through logic and initialize to the state that uses the external pins. The states are therefore mutually exclusive. In order to pulse CONFIG or $\overline{\text{INIT}}$, write an active signal and then an inactive signal to the register bit of interest. Holding CONFIG HIGH causes the programming to be active upon asserting load. Holding $\overline{\text{INIT}}$ LOW locks the initial programming configuration, whether it be the straight through or the user-defined configuration, as set by bit 2 of the Switch Configuration register.

Staging Register Readback

When the CONFIG control is used to accumulate a number of program steps and execute them simultaneously, it is possible to verify the pending switch programming prior to asserting the CONFIG control. Setting the staging readback pin to a 1 and reading the programming information from the switch returns configuration information about the pending switch programming rather than the current connections.

If CONFIG is 1, all programming propagates directly to the switch matrix, and the information returned during a readback is the same regardless of the setting of the Staging register readback bit.

Save User $\overline{\text{INIT}}$

The VSC3139 provides an alternate set of user-programmable registers that can save and recall the current programming of the staging registers. The programming information in these registers is activated with the $\overline{\text{INIT}}$ control.

When the Save User $\overline{\text{INIT}}$ bit is set to 0, the current programming held in the staging registers is transferred into the User Programming registers. Asserting the Save User bit (1) latches the programming information for future use. This switch programming may be recalled by asserting the User $\overline{\text{INIT}}$ bit (see below).

The Save User $\overline{\text{INIT}}$ bit in the Control register saves the current programming of the VSC3139 switch into the User Programming register(s). The values in the User Programming register(s) are retained until the Save User $\overline{\text{INIT}}$ bit is set to 0 or until power to the device is removed. If the Save User $\overline{\text{INIT}}$ bit is asserted while the User $\overline{\text{INIT}}$ Programming bit is 1, the switch assumes an undefined configuration. On power-up, these registers are in an unknown state.

User $\overline{\text{INIT}}$

Asserting the Save User $\overline{\text{INIT}}$ bit in the Switch Configuration register, address 281'h, selects the User Programming registers as the source for switch programming with the $\overline{\text{INIT}}$ control. With this bit set, if the $\overline{\text{INIT}}$ pin or bit is asserted, the switch is programmed to reflect the switch connections saved in the User Programming registers.

Because the User $\overline{\text{INIT}}$ feature is used in conjunction with the $\overline{\text{INIT}}$ bit or pin, it can also be disabled using the $\overline{\text{INIT}}$ Lockout bit in the Switch Setup register, address 280'h.

When activated, the User $\overline{\text{INIT}}$ Programming bit makes the programming in the user register available to the switch fabric. However, programming does not take place until the Software Programmable $\overline{\text{INIT}}$ bit or the $\overline{\text{INIT}}$ pin is asserted. Asserting the $\overline{\text{INIT}}$ Lockout bit HIGH inhibits any programming of the switch fabric using either the normal or user $\overline{\text{INIT}}$ registers.

To read back programming information from the User Memory, both the Staging Readback and the User $\overline{\text{INIT}}$ Programming bit must be set. In this configuration, any information read from a specific output represents the programming stored in the User Memory.

Switch Connection Register

Table 5. Switch Array Connection Examples

Output ADDR[10:0]	Input ADDR[10:0]	Description	Reset Value[1]	R/W
0000000000'b	0000000000'b	Program output Y0 to input A0	7FF	R/W
0000000001'b	0000000000'b	Program output Y1 to input A0	7FF	R/W
0000000010'b	0000000000'b	Program output Y2 to input A0	7FF	R/W
0000000011'b	0000000000'b	Program output Y3 to input A0	7FF	R/W
0000000100'b	0000000000'b	Program output Y4 to input A0	7FF	R/W
0000000101'b	0000000000'b	Program output Y5 to input A0	7FF	R/W
. . .	. . .	. . .	. . .	. . .
0001000111'b	0000000000'b	Program output Y71 to input A0	7FF	R/W
. . .	. . .	. . .	. . .	. . .
0000000000'b	0001000111'b	Program output Y0 to input A71	7FF	R/W
0000000001'b	0001000111'b	Program output Y1 to input A71	7FF	R/W
0000000010'b	0001000111'b	Program output Y2 to input A71	7FF	R/W
0000000011'b	0001000111'b	Program output Y3 to input A71	7FF	R/W
0000000100'b	0001000111'b	Program output Y4 to input A71	7FF	R/W
0000000101'b	0001000111'b	Program output Y5 to input A71	7FF	R/W
. . .	. . .	. . .	. . .	. . .
0001000111'b	0001000111'b	Program output Y71 to input A71	7FF	R/W

1. 7FF is the power-down code.

Drive/Sense Control

Register 3: DRIVE/SENSE Control

Reg Name:	DRIVE/SENSE Control	**Reg. Address:**	282'h
Reg Type:	R/W		
Description:	Controls the DRIVE input and SENSE output functions.		

Bit(s)	Bit Description	Reset Value	R/W
10-7	Not used		
6	Global SENSE control 0 = No effect on existing state of SENSE control signals 1 = Clear SENSE connection and turns off output buffer	0	R/W
5-4	Global DRIVE control 00 = maintains current connection state 01 = activates connection to DRIVE input selected with bits 3-0 10 = clears DRIVE connection state 11 = maintains current connection state	00	R/W
3-0	DRIVE input source select 0000 = input channel connected to DRIVE input	0'h	R/W

Register 4: SENSE Connection

Reg Name:	SENSE	**Reg. Address:**	300'h
Reg Type:	R/W		
Description:	Controls the operating mode of SENSE output bit.		

Bit(s)	Bit Description	Reset Value	R/W
10	Not used		
9	Drive level for SENSE output. Always returns 1 when bit 8 = 1. 0 = nominal drive mode 1 = high drive mode	0	R/W
8	Power-on state of SENSE output. 0 = on 1 = off	0	Read only
7-0	Address of output port connection to SENSE (0 to 47'h for Y0 to Y71), returns FF'h when SENSE is powered off.	FF'h	R/W

Temperature Sensor/Alarm

The VSC3139 has circuitry that detects the approximate temperature of the die and flags temperatures exceeding a user-selected, preset range. Register 5 at address 28B'h allows the user to read the die temperature sensor value (an uncalibrated, approximate temperature), and set a temperature threshold at which to assert an alarm.

There are 15, read only temperature ranges for the sensor, and 15 alarm threshold settings.

When the detected die temperature exceeds the user-set threshold, the temperature alarm is asserted.

Register 5: Temperature Sensor

Reg Name:	Temperature Sensor	**Reg. Address:**	28B'h
Reg Type:	R/W		
Description:	User-controllable on-board temperature sensing function.		

Bit(s)	Bit Description	Reset Value	R/W
10-8	Not used		
7-4	Approximate die temperature (not a calibrated value) 0000 = 23ºC to 41ºC 0001 = 33ºC to 50ºC 0010 = 42ºC to 60ºC 0011 = 52ºC to 69ºC 0100 = 61ºC to 78ºC 0101 = 70ºC to 88ºC 0110 = 80ºC to 97ºC 0111 = 89ºC to 106ºC 1000 = 98ºC to 116ºC 1001 = 108ºC to 125ºC 1010 = 117ºC to 135ºC 1011 = 127ºC to 144ºC 1100 = 136ºC to 153ºC 1101 = 145ºC to 163ºC 1110 = 155ºC to 172ºC 1111 = 164ºC to 181ºC		Read Only
3-0	Temperature alarm threshold 0000 = 23ºC to 41ºC 0001 = 33ºC to 50ºC 0010 = 42ºC to 60ºC 0011 = 52ºC to 69ºC 0100 = 61ºC to 78ºC 0101 = 70ºC to 88ºC 0110 = 80ºC to 97ºC 0111 = 89ºC to 106ºC 1000 = 98ºC to 116ºC 1001 = 108ºC to 125ºC 1010 = 117ºC to 135ºC 1011 = 127ºC to 144ºC 1100 = 136ºC to 153ºC 1101 = 145ºC to 163ºC 1110 = 155ºC to 172ºC 1111 = 164ºC to 181ºC	00	R/W

Input Configuration

The following registers are used to configure the properties of the high-speed data inputs. The two primary properties that can be set for the inputs are the Input Signal Equalization (ISE) and the Drive assignment. These properties can be set both globally and individually on a per input basis. When a property is set globally, it affects the setting for all inputs without exception. When a bit is set in the global registers, that state overrides any attempts to change the setting on an individual basis. It forces the global setting until the bit in the global register is cleared.

The Individual Input Configuration registers also serve a function that is not available in the global registers; the Scan register table. Bit 8 of each Individual Input Configuration register reflects the latched state of the associated high-speed input at the time that bit 0 of register 14 is set to 1.

Register 6: Global Input Channel Configuration

Reg Name:	Global Input Channel Configuration	**Reg. Address:**	283'h	
Reg Type:	R/W			
Description:	Global input channel configuration control.			
Bit(s)	**Bit Description**		**Reset Value**	**R/W**
10-4	Not used			
3-2	Global clear for ISE setting. 00 = bits 6 and 7 of Individual Input Configuration registers are writeable 01 = bit 6 of all Individual Input Configuration registers forced to 0 10 = bit 7 of all Individual Input Configuration registers forced to 0 11 = bits 6 and 7 of all Individual Input Configuration registers forced to 0		00	R/W
1-0	Global set for ISE setting. 00 = bits 6 and 7 of Individual Input Configuration registers are writeable 01 = bit 6 of all Individual Input Configuration registers forced to 1 10 = bit 7 of all Individual Input Configuration registers forced to 1 11 = bits 6 and 7 of all Individual Input Configuration registers forced to 1		00	R/W

Register 7: Individual Input Channel Configuration

Reg Name:	Individual Input Channel Configuration	**Reg. Address:**	600'h = A0 601'h = A1 ° 647'h = A71	
Reg Type:	R/W			
Description:	Individual input channel configuration control.			
Bit(s)	Bit Description		Reset Value	R/W
10-9	Not used			
8	A[0:71] scan register table (values latched using register 14, bit 0.			
7-6	ISE setting. 00 = ISE disabled 01 = low ISE 10 = medium ISE 11 = high ISE		00	
5-4	DRIVE input connection state. 00 = maintains current connection state 01 = activates connection to DRIVE input as selected by bits 3 through 0 10 = removes DRIVE connection to input 11 = maintains current connection state		00	R/W
3-0	DRIVE input source select. 0000 = input channel connected to DRIVE input		0'h	R/W

PRBS CONTROL

The PRBS Generator/Detector is capable of generating and detecting four NRZ patterns: 2^7-1, 2^9-1, 2^{10}-1, and 2^{11}-1. The main purpose of PRBS Generator/Detector is to be used for switch diagnostics and signal tracing. See the block diagram of the PRBS Generator in Figure 1 on page 5. The data rate of the Generator/Detector is determined by the external clock signal to a maximum 400Mb/s. The PRBS output data is clocked on the rising edge of the clock. The PRBS function controls are located in the PRBS Configuration register 0x284'h. The PRBS Generator is enabled by writing 1 into bit 4 of register 0x284'h. Pattern length is selected via register 0x284'h bit 3 and 2. Selecting 00 will generate pattern 2^7-1, 01 = 2^9-1, 10= 2^{10}-1, 11 = 2^{11}-1. It is possible to invert the pattern by writing 1 into register 0x284'h bit 1.

The PRBS Detector uses the same clock as the Generator. See the block diagram of the PRBS Detector in Figure 2 on page 5.

The clock used by the Detector can be inverted by setting bit 0 of register 284'h to 1. It may be necessary to invert CLK in order to compensate for the phase difference between data input and clock.

The PRBS Detector is enabled by writing a 1 into bit 4 of register 285'h. The detector pattern length is selected by bit 6 and bit 5 of register 0x285'h, respectively, 00 represents pattern 2^7-1, 01 = 2^9-1, 10= 2^{10}-1, 11 = 2^{11}-1. The error counter is not enabled until the pattern detector matches the pattern coming into the Detector. It can take up to 30 clock cycles to match the pattern, and once the pattern has been detected, bit 2 of register 288'h goes to 1. This enables the error counter and fixed_error_count counter. The user has an option to choose the error count period by setting bits 2 and 1 of register 285'h. Respectively, bits 2 and 1 represent the following count lengths: 00= 2^7, 01 = 2^9, 10= 2^{11}, 11 = 2^{15}. When any one of the above periods is selected, error count will continue until that period has elapsed. At that time, the error counter is disabled and the fixed_error_count flag will be set to 1 in register 288'h bit 1.

If the errors_detected flag in register 288'h bit 0 is set to 1, it means that during above set time period, errors occurred and the user can read the error count from registers 267'h and 287'h. After the error count has been read, the error counter can be reset by setting bit 3 of register 285'h to 0. Upon reset, the error counter, errors_detected, and fixed_error_count counter will be set to 0. If the user is not interested in setting any of the above count periods, it is possible to overwrite them by setting bit 0 of register 285'h to 0. This will provide a free-running error count without a predetermined count period. It should be noted though, if error count period is not set, and if number of errors exceed 65535 (counter overflow), the error counter will restart count from 0. It is possible to invert the PRBS pattern that is coming into pattern detector by asserting 1 in register 285'h bit 4. This can be used to detect an inverted pattern from the PRBS Generator.

Register 8: PRBS Generator Configuration

Reg Name:	PRBS Generator/Detector Configuration	**Reg. Address:**	284'h
Reg Type:	R/W		
Description:	Configures the operating mode of the on-board PRBS Generator/Detector.		

Bit(s)	Bit Description	Reset Value	R/W
10-5	Not used		
4	PRBS Generator enable. 0 = Disable PRBS generator 1 = Enable PRBS generator	0	R/W
3-2	PRBS Generator pattern length selection. 11 = 2^{11}–1 10 = 2^{10}–1 01 = 2^{9}–1 00 = 2^{7}–1	00	R/W
1	PRBS output pattern. 0 = Non-inverted pattern 1 = Inverted pattern	0	R/W
0	PRBS Error Detector clock phase selection (to correct for timing skews). 0 = Non-inverted clock phase 1 = Inverted clock phase	0	R/W

Register 9: PRBS Error Status

Reg Name:	PRBS Error Status	**Reg. Address:**	288'h
Reg Type:	R/W		
Description:	Report error status from the on-board PRBS detector.		

Bit(s)	**Bit Description**	**Reset Value**	**R/W**
10-3	Not used		
2	Error Detector search status 0 = Error Detector has not locked onto a valid PRBS pattern 1 = PRBS pattern detected. Detector is counting errors.	0	Read Only
1	Error count period indicator (not valid if register 10, bit 0 = 0) 0 = Fixed error count period has not yet been completed 1 = Fixed error count period has been completed	0	Read Only
0	Error flag bit (reset when read) 0 = No errors detected since last reset 1 = Errors detected since last reset	0	Read Only

Register 10: PRBS Receiver/Error Detector Configuration

Reg Name:	PRBS Receiver/Error Detector Configuration	**Reg. Address:**	285'h
Reg Type:	R/W		
Description:	Configures the operating mode of the on-board PRBS receiver/error detector.		

Bit(s)	Bit Description	Reset Value	R/W
10-8	Not used		
7	PRBS receiver enable 0 = Disable PRBS 1 = Enable PRBS detector	0	R/W
6-5	Select receiver/error detector pattern length (to match PRBS generator) 11 = 2^{11}-1 10 = 2^{10}-1 01 = 2^{9}-1 00 = 2^{7}-1	00	R/W
4	PRBS input pattern 0 = Non-inverted PRBS input 1 = Inverted PRBS input	0	R/W
3	Error detector reset 0 = Resets error count 1 = Enables error count	0	R/W
2-1	Error counter length control (dependent on bit 0) 11 = 2^{15}-1 10 = 2^{11}-1 01 = 2^{9}-1 00 = 2^{7}-1	00	R/W
0	Error detection run length 0 = No stop length, free running error detection 1 = Run and stop at count length	0	R/W

Register 11: PRBS Error Count Read

Reg Name:	PRBS Error Count Read	**Reg. Address:**	286'h = LSB Reg 287'h = MSB Reg
Reg Type:	R/W		
Description:	Provides Error Count report.		

Bit(s)	Bit Description	Reset Value	R/W
10-8	Not used		
7-0	Number of errors since start of count or last reset.	00'h	Read only

Programmable Output Drive Levels

Two output drive levels can be set using the Output Level Control register. Output drive level can be controlled both globally and on a per-channel basis through either the primary programming port or the Secondary Access Port. If both HIGH and LOW output bits are enabled simultaneously, LOW output level mode takes precedence.

Register 12: Global Output Level Control

Reg Name:	Global Output Level Control	**Reg. Address:**	28A'h
Reg Type:	R/W		
Description:	Enables global output high drive/nominal drive mode.		

Bit(s)	Bit Description	Reset Value	R/W
10-8	Not used		
7-4	Internal use only		
3-2	Not used		
1	High output level mode 0 = No change 1 = Force all outputs to high drive mode	0	R/W
0	Low output level mode 0 = No change 1 = Force all outputs to nominal drive mode	0	R/W

Register 13: Individual Output Level Control

Reg Name:	Individual Output Level Control	**Reg. Address:**	400'h = Y0 401'h = Y1 to 447'h = Y71
Reg Type:	R/W		
Description:	Enables individual output high drive/nominal drive mode.		

Bit(s)	Bit Description	Reset Value	R/W
10-9	Internal use only	00	
8-4	Not used		
3	Override output value 0 = Force the addressed Y output value to 0 when bit 2 is HIGH 1 = Force the addressed Y output value to 1 when bit 2 is HIGH	0	R/W
2	Output override mode (boundary scan support) control 0 = Disable output override mode 1 = Enable output override mode. Y output forced to value stored in bit 3 of this register	0	R/W
1	Individual output level control 0 = Set output level nominal 1 = Set output level HIGH	0	R/W
0	Individual output status 0 = Y output OFF 1 = Y output ON	0	Read Only

Boundary Scan Support

The VSC3139 has provisions for sampling the current state of the high-speed data inputs, as well as driving the high-speed data outputs with a static value.

To reduce power consumption, the input buffers for the boundary scan are powered off after reset. Prior to using the Scanning feature, these buffers must be energized by setting bit 1 of the Boundary Scan Control register to 1. Once the boundary scan input feature is no longer in use, this bit can once again be set to 0 to reduce power consumption.

Sampling of the high-speed data inputs is triggered by writing a 1 to bit 0 of the Boundary Scan Control register. This bit is self-clearing; it does not need to be cleared prior to the next operation, as it returns a 0 when read. This operation latches the current value of the high-speed inputs into bit 8 of each respective Input Channel Configuration register (600'h - 647'h). These registers can be read one by one to determine the state of each input.

Access to the high-speed output scan support is through bits 2 and 3 of the Individual Output Level Control register (400'h - 447'h). Setting bit 2 HIGH enables the Scan drive for the output associated with the selected Output Level Control register. Once enabled, bit 3 of the Individual Output Level Control register determines the value of the high-speed data output.

Alternatively, all of the scan outputs can be enabled with a single instruction using the Boundary Scan Control register. Setting bit 5 of the Boundary Scan Control register simultaneously enables the Scan drive of all outputs. Writing a 1 to bits 6 or 7 drives either a 0 or a 1, respectively, on all outputs. These bits are not self-clearing. Because of this, writing a 1 to bit 4 of the Scan Support register inhibits the Scan support programming until it is cleared. This bit overrides any programming in the Output Level Control registers.

Register 14: Boundary Scan Control

Reg Name:	Boundary Scan Control	**Reg. Address:**	289'h
Reg Type:	R/W		
Description:	Controls the operating mode of the Boundary Scan function.		

Bit(s)	Bit Description	Reset Value	R/W
10-8	Not used		
7	Global override output value set HIGH 0 = No change 1 = Force all override output values (bit 3 in individual output level control registers) to 1. When scan mode is enabled, all outputs are forced to 1.	0	R/W
6	Global override output value set LOW 0 = No change 1 = Force all override output values (bit 3 in individual output level control registers) to 0. When scan mode is enabled, all outputs are forced to 0.	0	R/W
5	Global output override/scan mode enable 0 = No change 1 = Force all outputs into override/scan mode (bit 2 in the individual output control registers) to 1. Enables scan mode on all outputs (Y0 through Y71).	0	R/W
4	Global output override/scan mode disable 0 = No change 1 = Disables override/scan mode on all outputs (Y0 through Y71). Equivalent of writing 0 to bit 2 of all individual output control registers.	0	R/W
3-2	Not used		
1	Boundary scan input enable 0 = Boundary scan inputs disabled 1 = Boundary scan inputs enabled	0	R/W
0	Input state latch 0 = No change 1 = Triggers latch of input state (A0 through A71). Self-clearing.	0	W

Register 15: User Status

Reg Name:	User Status	**Reg. Address:**	28C'h through
Reg Type:	R/W		28F'h
Description:	Enables information exchange between primary and secondary ports/display user status.		

Bit(s)	Bit Description	Reset Value	R/W
7-0	Registers for user status or information transfer between primary and secondary ports.	00'h	R/W

ELECTRICAL SPECIFICATIONS

AC Characteristics

(Over Recommended Operating Conditions unless stated otherwise)

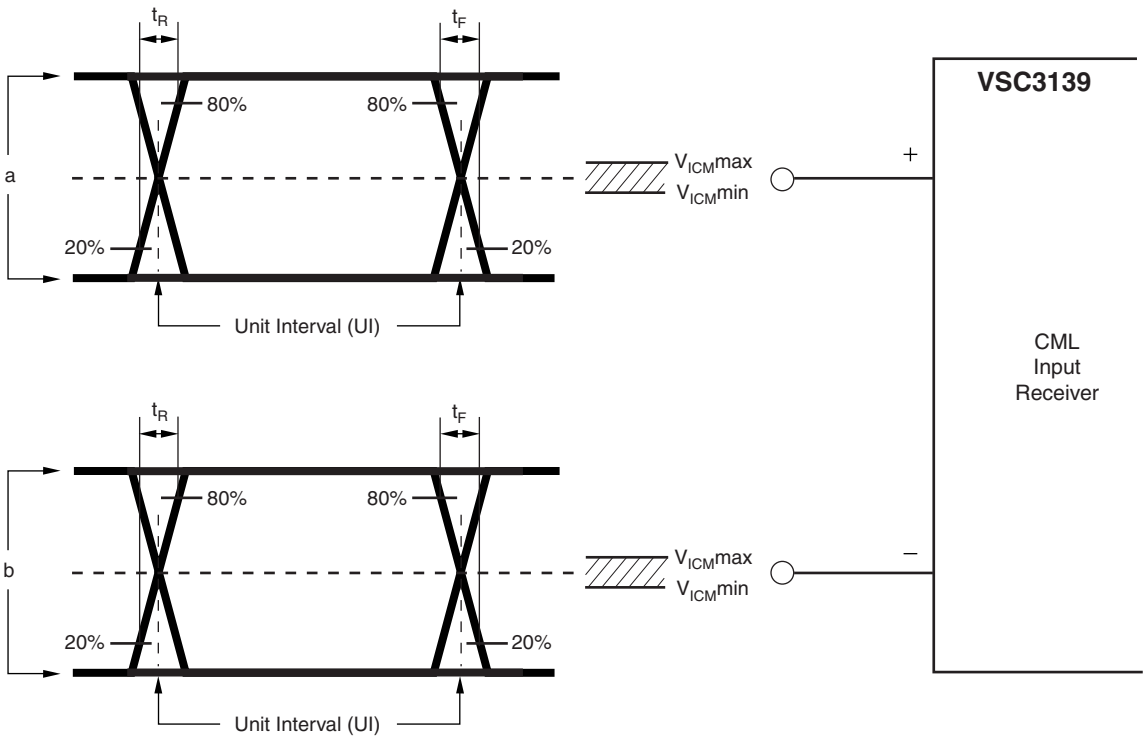
Table 6. High-Speed Inputs (A, $\overline{A}$)

Symbol	Parameter	Min	Typ	Max	Units	Condition
DR_A	Serial NRZ Input Data Rate			3.6	Gb/s	Minimum data rate will be limited by the AC-coupling capacitor value (if AC-coupled)
t_{PD_AY}	Propagation Delay from any A input to any Y output		1		ns	
t_{SKEW}	Output Channel to channel Delay Skew			40	ps	Across striping group
t_{R_A} , t_{F_A}	Serial Data Input Rise and Fall Times		100	150	ps	20% to 80%. See Figure 4.

Table 7. High-Speed Data Outputs (Y, $\overline{Y}$)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
DR_Y	Serial NRZ Output Data Rate			3.6	Gb/s	Minimum data rate will be limited by the AC-coupling capacitor value (if AC-coupled)
t_{J_rms}	Serial Output Data added delay jitter: rms(1, 2)			10	ps	20 to 80%. See Figure 4. With 50Ω to V_{CC}.
t_{Jp-p}	Serial Output Data added delay jitter: peak-peak(1, 2)			40	ps	20 to 80%. See Figure 4. With 50Ω to V_{CC}.
t_{R_Y} , t_{F_Y}	Serial Output Data Rise and Fall Times		80	120	ps	20 to 80%. See Figure 4. With 50Ω to V_{CC}.
DC_Y	Serial Data Output Duty Cycle	40	50	60	%	Only relevant with 101010 input data patterns. 0.1µF coupling capacitor with 50Ω to V_{CC}.

1. *Guaranteed by design, but not tested.*
2. *Broadband (unfiltered) deterministic jitter added to a jitter free input: 2^{23} -1 PRBS data pattern.*



If used differentially (true and complement), each signal should meet the requirements for a = b = V_{A_DE}. See Table 7.
If used single-ended (true only), the value required is a = 2 x V_{A_DE}.

Figure 4. Parametric Measurement Setup

Table 8. Program Interface[1]

Symbol	Parameter	Min	Typ	Max[2]	Unit
t_{sPS}	Setup time from PARALLEL/$\overline{SERIAL}$ selection to $\overline{CS}$ falling edge	2			ns
$t_{s\overline{CS}}$	Setup time from falling edge of $\overline{CS}$ to falling edge of ALE	3			ns
t_{sALE}	Setup time from ADDR[10:0] stable to falling edge of ALE	3			ns
t_{hALE}	Hold time for ADDR[10:0] after falling edge ALE	3			ns
t_{pwALE}	High pulse width for ALE	4			ns
$t_{pwl\overline{RD}}$	Pulse width for $\overline{RD}$ low	22			ns
$t_{pwh\overline{RD}}$	Pulse width for $\overline{RD}$ high	8			ns
$t_{h\overline{RD}}$	Hold time for DATA[10:0] after rising edge of $\overline{RD}$	3			ns
$t_{pwl\overline{WR}}$	Pulse width low of $\overline{WR}$	4			ns
$t_{s\overline{WR}}$	Setup time from DATA[10:0] stable to rising edge of $\overline{WR}$	2.3			ns
$t_{h\overline{WR}}$	Hold time for DATA[10:0] after rising edge of $\overline{WR}$	4.7			ns
$t_{pwh\overline{WR}}$	Pulse width high of $\overline{WR}$	8			ns
t_{pwCFG}	High and low pulse width for CONFIG	8			ns

Table 8. Program Interface[1] (continued)

Symbol	Parameter	Min	Typ	Max[2]	Unit
t_{sCFG}	Setup time between rising edge of $\overline{WR}$ and rising edge of CONFIG (if not permanently tied HIGH)	4.5			ns
t_{hCFG}	Hold time for CONFIG before rising edge of $\overline{CS}$	8			ns
$t_{h\overline{CS}}$	Hold time for $\overline{CS}$ after rising edge of $\overline{RD}$	8			ns
t_{sLOAD}	Time for LOAD stable before rising edge of SCLK	5			ns
t_{hLOAD}	Time to hold LOAD stable after rising edge of SCLK	5			ns
$t_{pwhLOAD}$	Time to hold LOAD stable after rising edge of SCLK	14		18	ns
t_{sSDIN}	Time for SDIN stable before rising edge of SCLK	5			ns
t_{hSDIN}	Time to hold SDIN stable after rising edge of SCLK	5			ns
$t_{s\overline{SERIAL}}$	Time for PARALLEL/$\overline{SERIAL}$ stable before falling edge of $\overline{CS}$	5			ns
$t_{s\overline{RD}}$	Time for $\overline{RD}$ stable before rising edge of SCLK	5			ns
$t_{pwh\overline{RD}}$	Time to hold $\overline{RD}$ stable after rising edge of SCLK	26			ns
t_{dSDOUT}	Delay for SDOUT valid after rising edge of SCLK			10	ns
t_{hSDOUT}	Time for SDOUT valid after rising edge of SCLK	2			ns
$t_{perSCLK}$	Period of SCLK	14			ns
t_{DRVN}	Time required for ADDR/DATA bus to change direction	3			ns
t_{VALID}	Time until data valid after falling $\overline{RD}$	20			ns
$t_{sSecSDIN}$	Setup time for SDIN to rising edge of SecSCLK	20			ns
$t_{hSecSDIN}$	Hold time for SDIN from rising edge of SecSCLK	25			ns
$t_{sSecWrite}$	Setup time for SecWrite rising edge to rising edge of SecSCLK	20			ns
$t_{hSecWrite}$	Hold time for SecWrite from rising edge of SecSCLK	34			ns
$t_{wSecWrite}$	Pulse width of SecWrite	54		73	ns
$t_{sSecRead}$	Setup time for SecRead rising edge to rising edge of SecSCLK	20			ns
$t_{hSecRead}$	Hold time for SecRead from rising edge of SecSCLK	34			ns
$t_{wSecRead}$	Pulse width of SecRead	54			ns
$t_{pSecSDOUT}$	Delay to data valid on SecSDOUT from rising edge of SecSCLK	12		62	ns
$t_{perSecSCLK}$	Minimum period for SecSCLK	67			ns
t_{pHI-Z}	Delay time from Sec$\overline{CS}$ to SecSDOUT active/inactive			20	ns
$t_{sSec\overline{CS}}$	Setup time from rising edge of Sec$\overline{CS}$ to SecSCLK in A10	20			ns
$t_{hSec\overline{CS}}$	Hold time for Sec$\overline{CS}$ from rising edge of SecSCLK in SecRead	67			ns

1. *Values listed are guaranteed by design, but not tested.*
2. *Except for $t_{dSecSDOUT}$, the maximum timing values are dependent on the period of SecSCLK. For every 2ns added to the period of SecSCLK beyond 67ns, add 1ns to the max values provided.*

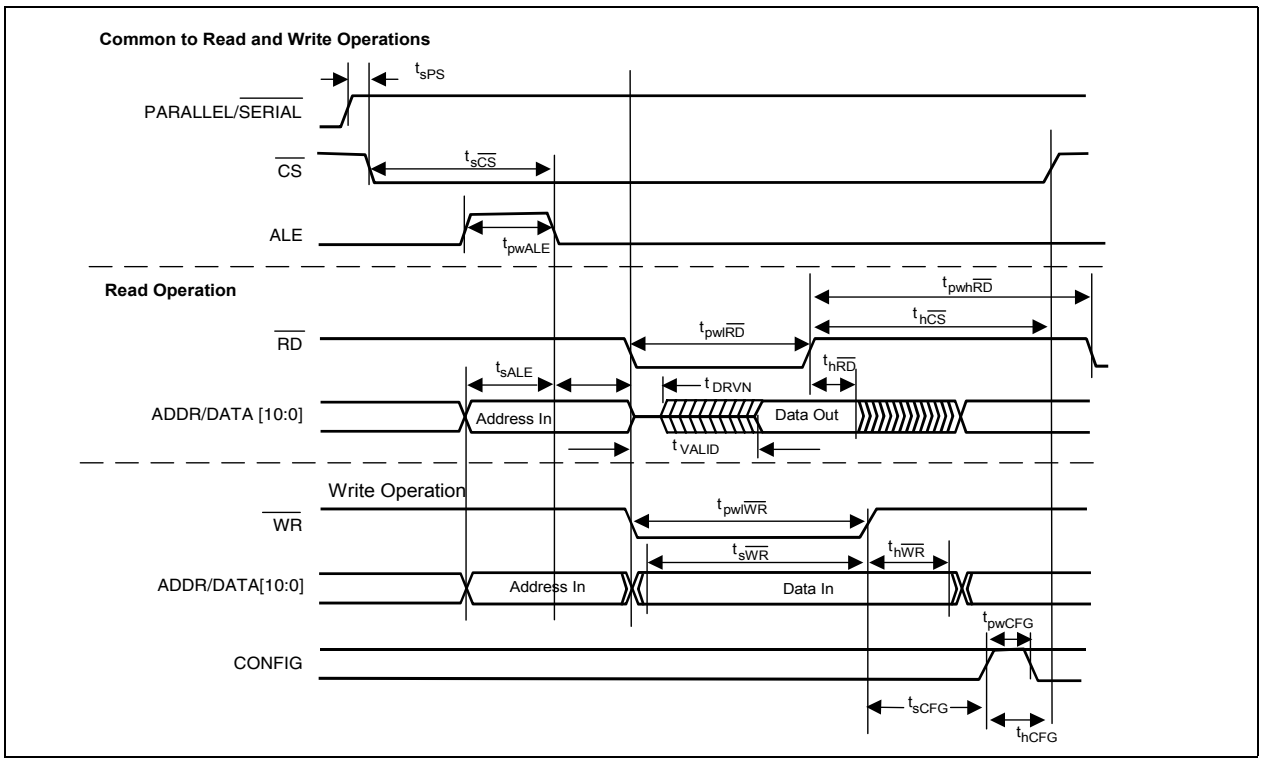


Figure 5. Parallel Mode Timing

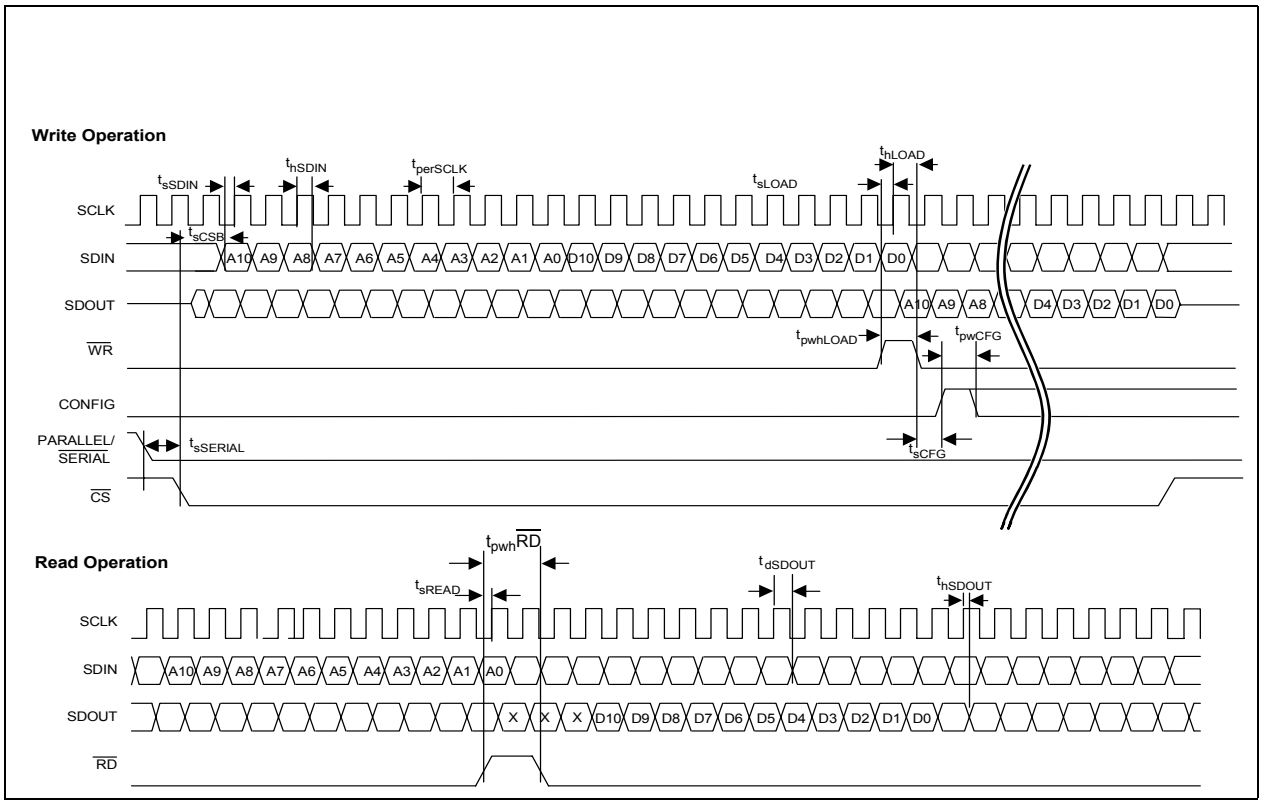


Figure 6. Serial Mode Timing

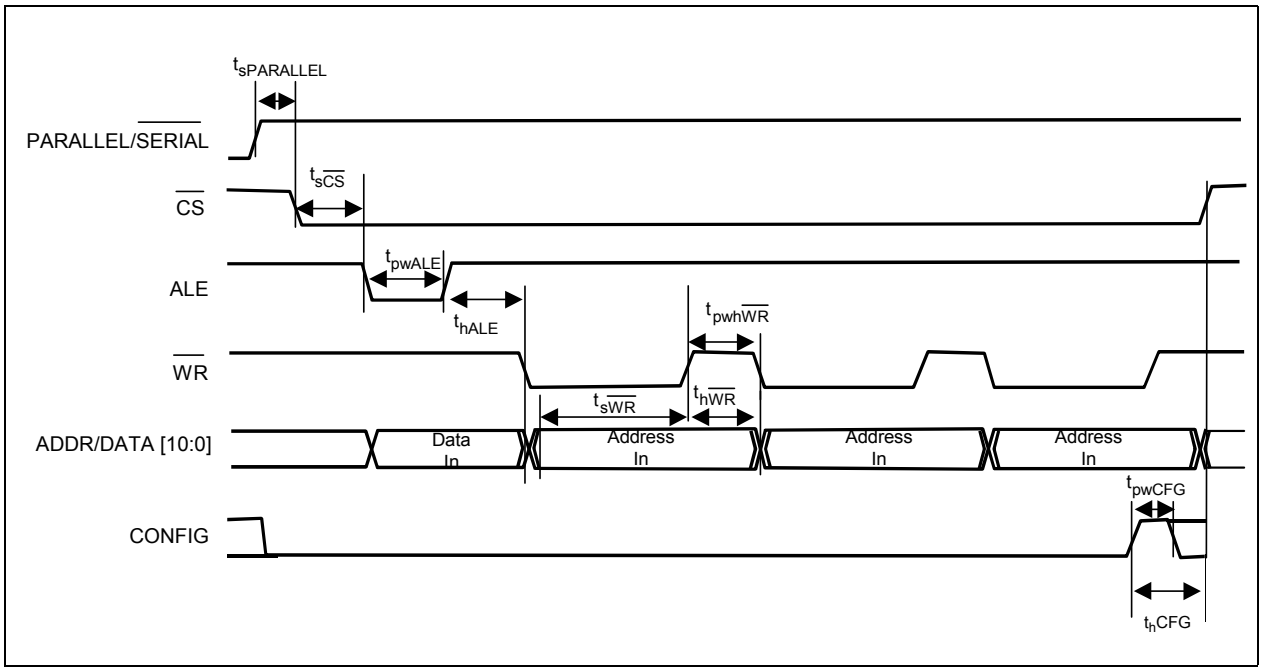


Figure 7. Parallel Multicast Mode

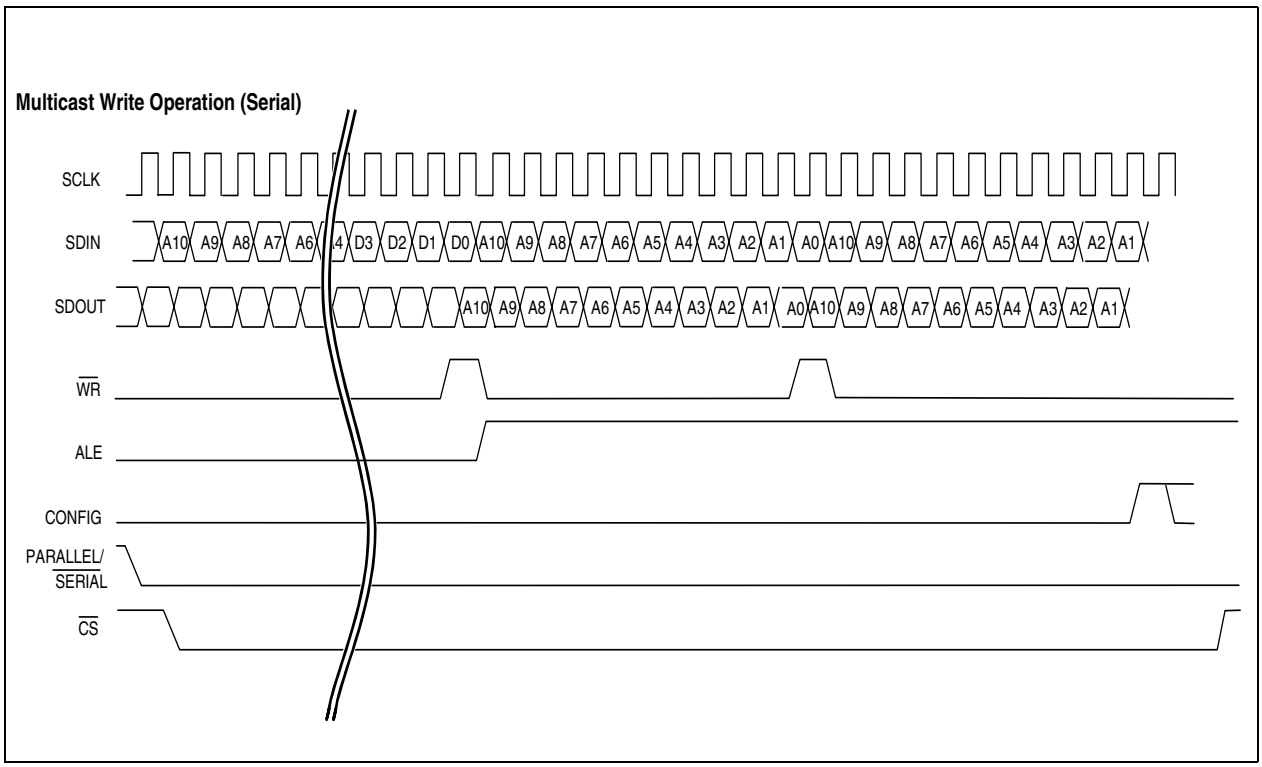


Figure 8. Serial Multicast Mode

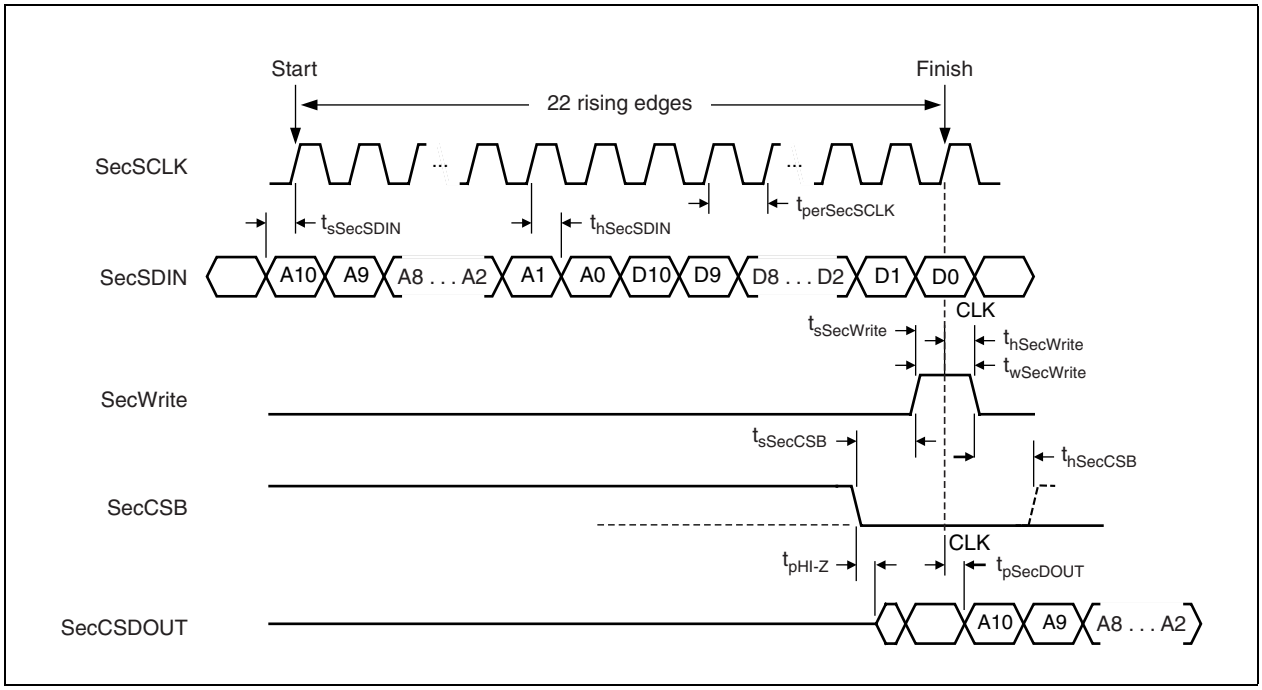


Figure 9. Secondary Access Port Write Timing Diagram

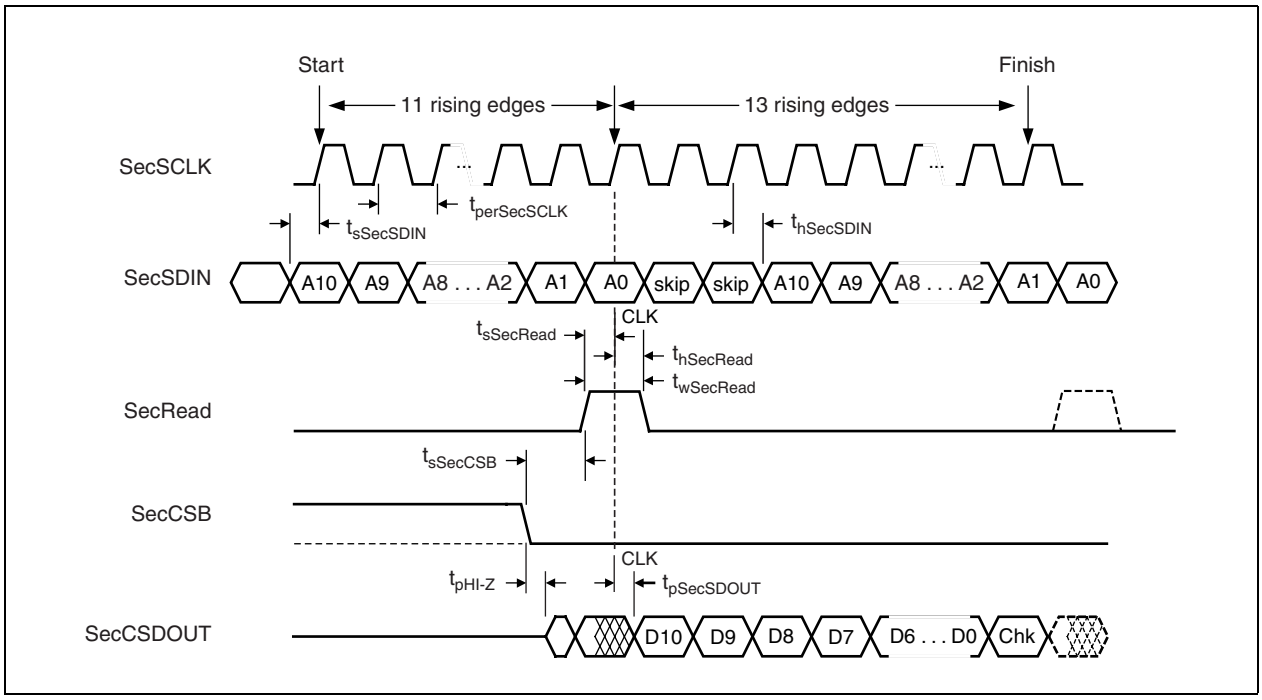


Figure 10. Secondary Access Port Read Timing Diagram

DC Characteristics

Specifications are considered to be over recommended operating conditions unless stated otherwise.

Table 9. High-Speed Data Inputs (A, $\overline{A}$)—Differential CML

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{A_DE}	Voltage Input Swing (Differential Drive)	100		550	mVp-p	Input signal on *both* true and complement inputs.
V_{ICM}	Input Common-Mode Voltage	V_{CC} – 0.7	2	V_{CC} – 0.3	V	
R_{IN_A}	Input Resistance	80	100	120	Ω	Between true and complement Inputs. See Figure 14.

Table 10. High-Speed Data Outputs (Y, $\overline{Y}$)—Differential CML

Symbol	Parameter	Min	Typ	Max	Unit	Condition
$V_{out\text{-}LD}$	Serial Data Output Voltage Swing: Low Drive Mode	500	650	800	mVp-p	Mean p-p differential amplitude between true and complement outputs. With 50Ω to V_{CC}.
$V_{out\text{-}HD}$	Serial Data Output Voltage Swing: High Drive Mode	1000	1300	1600	mVp-p	Vp-p swing on true and complement outputs. With 50Ω to V_{CC}.
$R_{out\text{-}Y}$	Back Terminated Output Resistance	40	50	60	Ω	See Figure 14.

Table 11. LVTTL/CMOS Input Signals

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	1.7		V_{CCD} + 1.0	V	V_{CCD} = 2.5V/3.3V
V_{IL}	Input LOW Voltage	0		0.8	V	V_{CCD} = 2.5V/3.3V
I_{IH}	Input HIGH Current			100	µA	
I_{IL}	Input LOW Current	–100			µA	

Table 12. LVTTL/CMOS Output Signals

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{OH}	Output HIGH Voltage	V_{CCD} – 0.2		V_{CCD}	V	DC load < 500µA
V_{OL}	Output LOW Voltage	0		0.2	V	DC load < 2mA

Table 13. Power Dissipation

Symbol	Parameter	Min	Typ	Max	Unit	Condition
P_{D_LD}	Total Power Dissipation: Nominal Drive Mode		9		W	V_{CC} = 2.5V ±5%
P_{D_HD}	Total Power Dissipation: High Drive Mode		13		W	V_{CC} = 2.5V ±5%

Recommended Operating Conditions

Table 14. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{CC}	Power Supply Voltage	2.375	+2.5	2.625	V	
V_{CCD}	Power Supply Voltage, Programming Port(1)		+2.5 or +3.3		V	
T	Operating Temperature(2)	0		+85	°C	

1. *All timing specifications and diagrams reflect +3.3V.*

2. *Lower limit of specification is ambient temperature and upper limit is case temperature.*

Absolute Maximum Ratings

Table 15. Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{CC}	Power Supply Voltage, Potential to GND	–0.5		+3.5	V	
	DC Input Voltage Applied (TTL)	–0.5		V_{CC} + 1.0	V	
	DC Input Voltage Applied (CML)	–0.5		V_{CC} + 0.5	V	
I_{OUT}	Output Current	–50		+50	mA	
T_C	Case Temperature Under Bias(1)	–30		+125	°C	
T_S	Storage Temperature	–40		+125	°C	
V_{ESD}	ESD Voltage (Human Body Model) PRBS data, clock, and device drive input pins All other pins	 –500 –1000		 +500 +1000	 V V	

1. VSC3139 has passed JESD22-A104 temperature cycling condition G for 1000 cycles.

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to the listed values for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliabiility of the device.

I/O Equivalent Circuits

Input Termination

Termination resistor pairs are isolated between each input to minimize crosstalk. The termination will self-bias to +2.0V (nominal) for AC-coupled applications.

All input data must be differential and nominally biased to +2.0V relative to V_{EE} or AC-coupled. Internal terminations are provided with nominally 50Ω from the true and complement inputs to a common bias point.

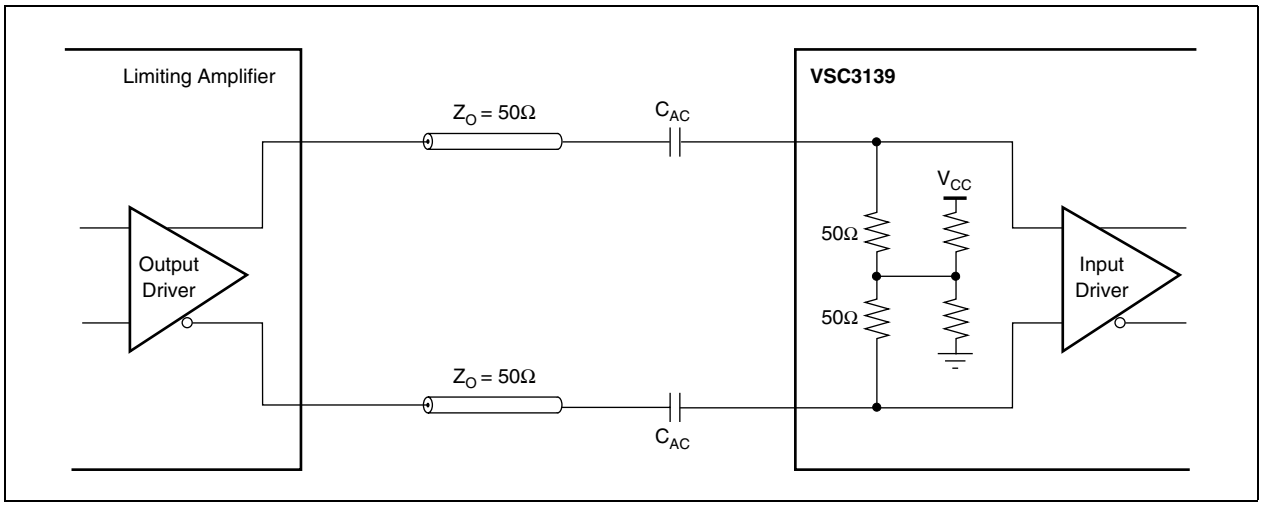


Figure 11. Differential AC-Coupled Input Termination

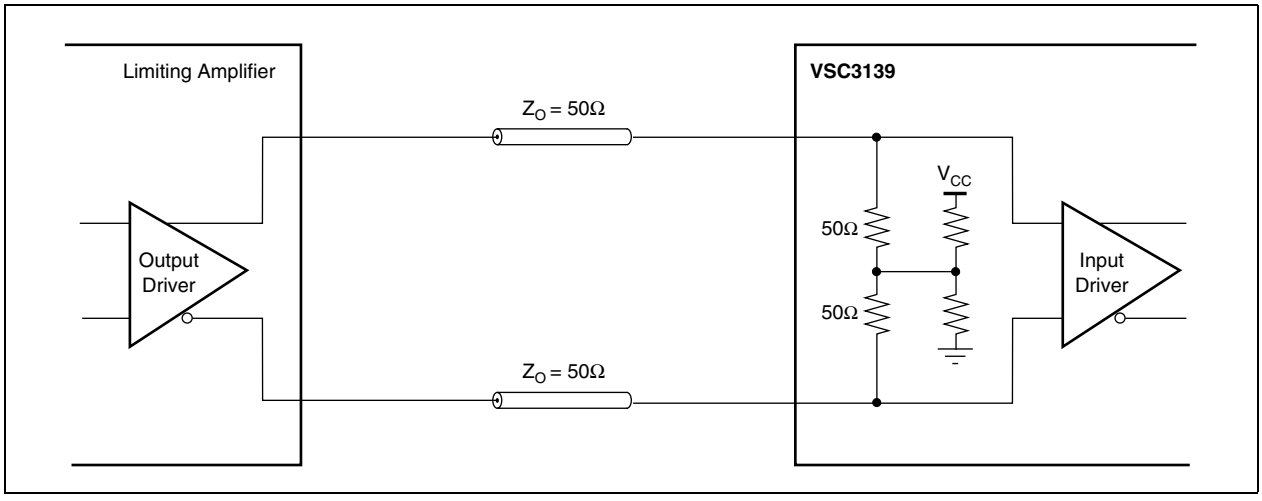


Figure 12. Differential DC-Coupled Input Termination

Output Termination

The high-speed outputs of the VSC3139 are current sinks, internally back-terminated by 50Ω pull-up resistors to the positive supply rail. Typical DC terminations are 50Ω pull-ups to the positive supply rail, 50Ω terminations to +2.0V, and 100Ω from true to complement.

Data outputs are provided through differential current switches with on-chip 50Ω back-termination. Two drive levels are provided to facilitate power/noise margin optimization on a per-output basis.

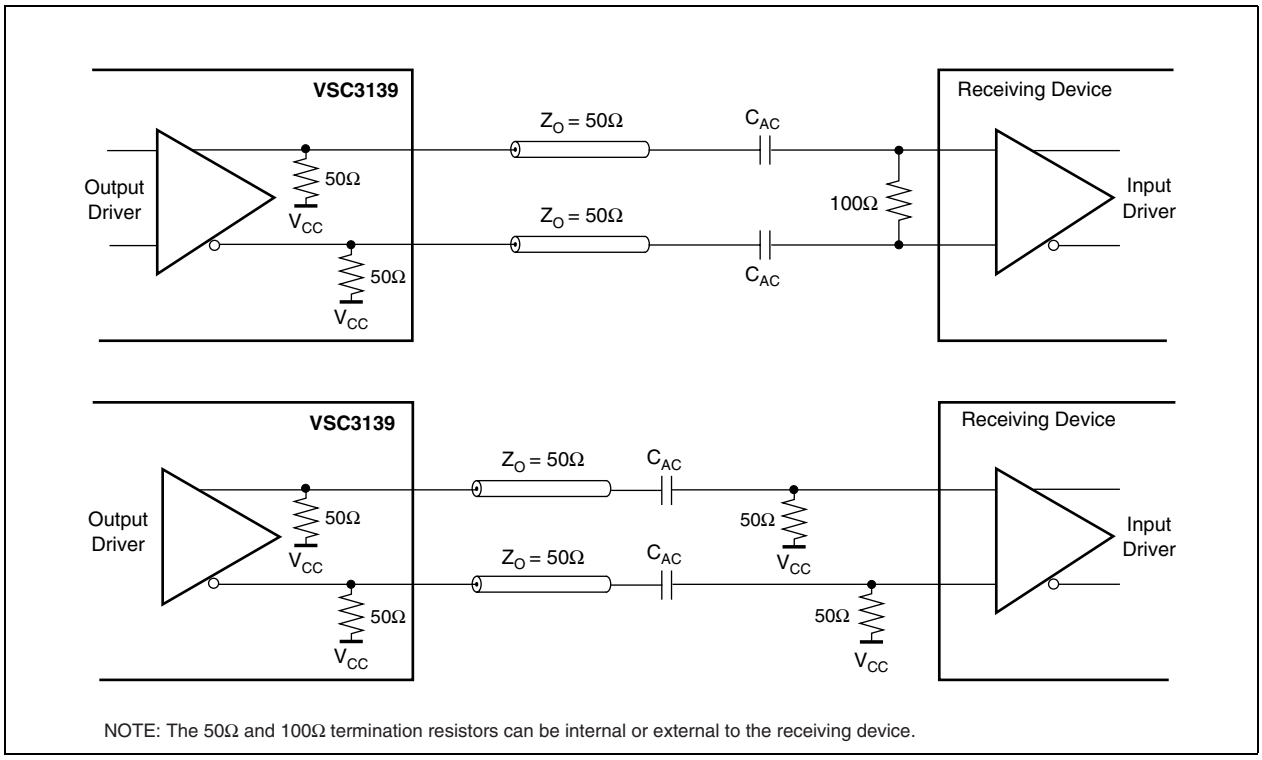


Figure 13. High-Speed Output—AC Coupled Terminations

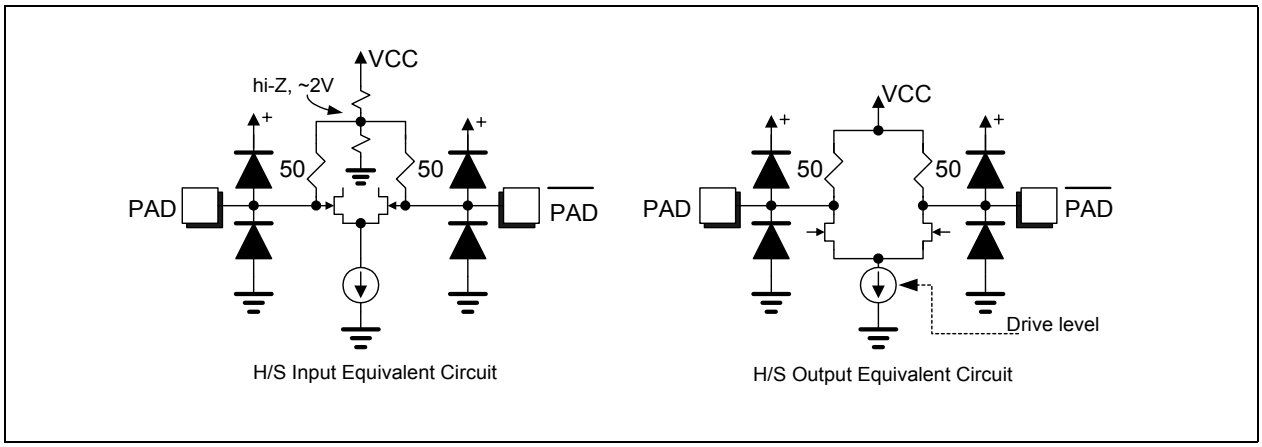


Figure 14. Input and Output Equivalent Circuits

PACKAGE INFORMATION

	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
AE	BLANK	BLANK	VCC	VEE	WRB	INITB	VCCD	RDB	CNFG	VCC	PARALLEL/ SERIAL	CSB	VEE	NC	NC	VCC	NC	NC	VCCD	NC	NC	VEE	VCC	BLANK	BLANK
AD	BLANK	VEE	VEE	YN44	Y46	Y48	Y54	Y56	Y62	Y64	Y70	Y69	Y67	Y61	Y59	Y53	Y51	Y45	Y43	Y37	Y35	Y29	VEE	VEE	BLANK
AC	VCC	VEE	Y44	VEE	YN46	YN48	YN54	YN56	YN62	YN64	YN70	YN69	YN67	YN61	YN59	YN53	YN51	YN45	YN43	YN37	YN35	YN29	VEE	VEE	VCC
AB	VEE	Y42	YN42	Y40	YN40	Y50	Y52	Y58	Y60	Y66	Y68	Y71	Y65	Y63	Y57	Y55	Y43	Y47	Y41	Y39	Y33	Y31	YN25	Y25	VEE
AA	ADDR/ DATA0	Y36	YN36	Y38	YN38	YN50	YN52	YN58	YN60	YN66	YN68	YN71	YN65	YN63	YN57	YN55	YN43	YN47	YN41	YN39	YN33	YN31	YN27	Y27	PRBS_ OUTB
Y	ADDR/ DATA1	Y34	YN34	Y32	YN32	VEE	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	Y23	Y23	YN21	Y21	VCCD
W	VCCD	Y28	YN28	Y30	YN30	VEE	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	YN17	Y17	YN19	Y19	PRBS_ OUT
V	ADDR/ DATA2	Y26	YN26	Y24	YN24	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	YN15	Y15	YN13	Y13	NC
U	ADDR/ DATA3	Y20	YN20	Y22	YN22	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	YN9	Y9	YN11	Y11	PRBS_ CLK
T	VCC	Y18	YN18	Y16	YN16	VEE	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	YN7	Y7	YN5	Y5	VCC
R	ADDR/ DATA4	Y12	YN12	Y14	YN14	VEE	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	YN1	Y1	YN3	Y3	PRBS_ CLKB
P	ADDR/ DATA5	Y10	YN10	Y8	YN8	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VCCD	VCCD	VCC	VCC	VEE	VEE	VCC	VCC	AN3	A3	AN1	A1	NC
N	VEE	Y4	YN4	Y6	YN6	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VCCD	VCCD	VCC	VCC	VEE	VEE	VCC	VCC	AN5	A5	AN7	A7	VEE
M	ADDR/ DATA6	Y2	YN2	Y0	YN0	VEE	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	AN11	A11	AN9	A9	NC
L	ADDR/ DATA7	A0	AN0	A2	AN2	VEE	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	AN13	A13	AN15	A15	PRBS_ INB
K	VCC	A6	AN6	A4	AN4	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	AN19	A19	AN17	A17	VCC
J	ADDR/ DATA8	A8	AN8	A10	AN10	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	AN21	A21	AN23	A23	PRBS_ IN
H	ADDR/ DATA9	A14	AN14	A12	AN12	VEE	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	AN27	A27	AN25	A25	PRBS_ ERRDET
G	VCCD	A16	AN16	A18	AN18	VEE	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	AN29	A29	AN31	A31	SEN SEN
F	ADDR/ DAT10	A22	AN22	A20	AN20	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	AN35	A35	AN33	A33	VCCD
E	ALE	A24	AN24	A26	AN26	AN36	AN42	AN44	AN50	AN52	AN58	AN60	AN66	AN68	AN69	AN67	AN61	AN59	AN53	AN51	AN37	A37	AN39	A39	SENSE
D	VEE	A30	AN30	AN36	AN34	A36	A42	A44	A50	A52	A58	A60	A66	A68	A69	A67	A61	A59	A53	A51	AN43	A43	AN41	A41	VEE
C	VCC	VEE	A28	A34	AN32	AN38	AN40	AN46	AN48	AN54	AN56	AN62	AN64	AN70	AN71	AN65	AN63	AN57	AN55	AN49	AN47	AN45	NC	VEE	VCC
B	BLANK	VEE	VEE	VEE	A32	A38	A40	A46	A48	A54	A56	A62	A64	A70	A71	A65	A63	A57	A55	A49	A47	A45	VEE	VEE	BLANK
A	BLANK	BLANK	VCC	VEE	SEC_ CSB	DRIVE	VCCD	DRIVEB	SEC_ READ	VCC	SEC_ WRITE	SEC_ SDIN	VEE	SEC_ SCLK	SEC_ SDOUT	VCC	NC	OVER TEMP	VCCD	RESET B	NC	VEE	VCC	BLANK	BLANK

Figure 15. Pin Diagram (Top View) for 613 BGA, 33mm x 33mm (SH)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
AE	BLANK	BLANK	VCC	VEE	NC	NC	VCCD	NC	NC	VCC	NC	NC	VEE	CSB	PARALLEL/ SERIAL	VCC	CNFG	RDB	VCCD	INITB	WRB	VEE	VCC	BLANK	BLANK
AD	BLANK	VEE	VEE	Y29	Y35	Y37	Y43	Y45	Y51	Y53	Y59	Y61	Y67	Y69	Y70	Y64	Y62	Y56	Y54	Y48	Y46	YN44	VEE	VEE	BLANK
AC	VCC	VEE	VEE	YN29	YN35	YN37	YN43	YN45	YN51	YN53	YN59	YN61	YN67	YN69	YN70	YN64	YN62	YN56	YN54	YN48	YN46	VEE	Y44	VEE	VCC
AB	VEE	Y25	YN25	Y31	Y33	Y39	Y41	Y47	Y43	Y55	Y57	Y63	Y65	Y71	Y68	Y66	Y60	Y58	Y52	Y50	YN40	Y40	YN42	Y42	VEE
AA	PRBS_ OUTB	Y27	YN27	YN31	YN33	YN39	YN41	YN47	YN43	YN55	YN57	YN63	YN65	YN71	YN68	YN66	YN60	YN58	YN52	YN50	YN38	Y38	YN36	Y36	ADDR/ DATA0
Y	VCCD	Y21	YN21	Y23	YN23	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VEE	YN32	Y32	YN34	Y34	ADDR/ DATA1
W	PRBS_ OUT	Y19	YN19	Y17	YN17	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VEE	YN30	Y30	YN28	Y28	VCCD
V	NC	Y13	YN13	Y15	YN15	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	YN24	Y24	YN26	Y26	ADDR/ DATA2
U	PRBS_ CLK	Y11	YN11	Y9	YN9	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	YN22	Y22	YN20	Y20	ADDR/ DATA3
T	VCC	Y5	YN5	Y7	YN7	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VEE	YN16	Y16	YN18	Y18	VCC
R	PRBS_ CLKB	Y3	YN3	Y1	YN1	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VEE	YN14	Y14	YN12	Y12	ADDR/ DATA4
P	NC	A1	AN1	A3	AN3	VCC	VCC	VEE	VEE	VCC	VCC	VCCD	VCCD	VCC	VCC	VEE	VEE	VCC	VCC	VEE	YN8	Y8	YN10	Y10	ADDR/ DATA5
N	VEE	A7	AN7	A5	AN5	VCC	VCC	VEE	VEE	VCC	VCC	VCCD	VCCD	VCC	VCC	VEE	VEE	VCC	VCC	VEE	YN6	Y6	YN4	Y4	VEE
M	NC	A9	AN9	A11	AN11	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VEE	YN0	Y0	YN2	Y2	ADDR/ DATA6
L	PRBS_ INB	A15	AN15	A13	AN13	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VEE	AN2	A2	AN0	A0	ADDR/ DATA7
K	VCC	A17	AN17	A19	AN19	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	AN4	A4	AN6	A6	VCC
J	PRBS_ IN	A23	AN23	A21	AN21	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	AN10	A10	AN8	A8	ADDR/ DATA8
H	PRBS_ ERRDET	A25	AN25	A27	AN27	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VEE	AN12	A12	AN14	A14	ADDR/ DATA9
G	SEN SEN	A31	AN31	A29	AN29	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VCC	VCC	VEE	VEE	VEE	AN18	A18	AN16	A16	VCCD
F	VCCD	A33	AN33	A35	AN35	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE	AN20	A20	AN22	A22	ADDR/ DAT10
E	SENSE	A39	AN39	A37	AN37	AN51	AN53	AN59	AN61	AN67	AN69	AN68	AN66	AN60	AN58	AN52	AN50	AN44	AN42	AN36	AN26	A26	AN24	A24	ALE
D	VEE	A41	AN41	A43	AN43	A51	A53	A59	A61	A67	A69	A68	A66	A60	A58	A52	A50	A44	A42	A36	AN34	AN36	AN30	A30	VEE
C	VCC	VEE	NC	AN45	AN47	AN49	AN55	AN57	AN63	AN65	AN71	AN70	AN64	AN62	AN56	AN54	AN48	AN46	AN40	AN38	AN32	A34	A28	VEE	VCC
B	BLANK	VEE	VEE	A45	A47	A49	A55	A57	A63	A65	A71	A70	A64	A62	A56	A54	A48	A46	A40	A38	A32	VEE	VEE	VEE	BLANK
A	BLANK	BLANK	VCC	VEE	NC	RESET B	VCCD	OVER TEMP	NC	VCC	SEC_ SDOUT	SEC_ SCLK	VEE	SEC_ SDIN	SEC_ WRITE	VCC	SEC_ READ	DRIVEB	VCCD	DRIVE	SEC_ CSB	VEE	VCC	BLANK	BLANK

Figure 16. Pin Diagram (Bottom View) for 613 BGA, 33mm x 33mm (SH)

Table 16. VSC3139 Pins

Diagram Coordinate	Pin Name	Description
High-Speed Data Inputs		
L24, L23	A0, AN0	High Speed Data Input, Channel A0, AN0 (True, Complement)
P2, P3	A1, AN1	High Speed Data Input, Channel A1, AN1 (True, Complement)
L22, L21	A2, AN2	High Speed Data Input, Channel A2, AN2 (True, Complement)
P4, P5	A3, AN3	High Speed Data Input, Channel A3, AN3 (True, Complement)
K22, K21	A4, AN4	High Speed Data Input, Channel A4, AN4 (True, Complement)
N4, N5	A5, AN5	High Speed Data Input, Channel A5, AN5 (True, Complement)
K24, K23	A6, AN6	High Speed Data Input, Channel A6, AN6 (True, Complement)
N2, N3	A7, AN7	High Speed Data Input, Channel A7, AN7 (True, Complement)
J24, J23	A8, AN8	High Speed Data Input, Channel A8, AN8 (True, Complement)
M2, M3	A9, AN9	High Speed Data Input, Channel A9, AN9 (True, Complement)
J22, J21	A10, AN10	High Speed Data Input, Channel A10, AN10 (True, Complement)
M4, M5	A11, AN11	High Speed Data Input, Channel A11, AN11 (True, Complement)
H22, H21	A12, AN12	High Speed Data Input, Channel A12, AN12 (True, Complement)
L4, L5	A13, AN13	High Speed Data Input, Channel A13, AN13 (True, Complement)
H24, H23	A14, AN14	High Speed Data Input, Channel A14, AN14 (True, Complement)
L2, L3	A15, AN15	High Speed Data Input, Channel A15, AN15 (True, Complement)
G24, G23	A16, AN16	High Speed Data Input, Channel A16, AN16 (True, Complement)
K2, K3	A17, AN17	High Speed Data Input, Channel A17, AN17 (True, Complement)
G22, G21	A18, AN18	High Speed Data Input, Channel A18, AN18 (True, Complement)
K4, K5	A19, AN19	High Speed Data Input, Channel A19, AN19 (True, Complement)
F22, F21	A20, AN20	High Speed Data Input, Channel A20, AN20 (True, Complement)
J4, J5	A21, AN21	High Speed Data Input, Channel A21, AN21 (True, Complement)
F24, F23	A22, AN22	High Speed Data Input, Channel A22, AN22 (True, Complement)
J2, J3	A23, AN23	High Speed Data Input, Channel A23, AN23 (True, Complement)
E24, E23	A24, AN24	High Speed Data Input, Channel A24, AN24 (True, Complement)
H2, H3	A25, AN25	High Speed Data Input, Channel A25, AN25 (True, Complement)
E22, E21	A26, AN26	High Speed Data Input, Channel A26, AN26 (True, Complement)
H4, H5	A27, AN27	High Speed Data Input, Channel A27, AN27 (True, Complement)
C23, D22	A28, AN28	High Speed Data Input, Channel A28, AN28 (True, Complement)
G4, G5	A29, AN29	High Speed Data Input, Channel A29, AN29 (True, Complement)
D24, D23	A30, AN30	High Speed Data Input, Channel A30, AN30 (True, Complement)
G2, G3	A31, AN31	High Speed Data Input, Channel A31, AN31 (True, Complement)
B21, C21	A32, AN32	High Speed Data Input, Channel A32, AN32 (True, Complement)
F2, F3	A33, AN33	High Speed Data Input, Channel A33, AN33 (True, Complement)
C22, D21	A34, AN34	High Speed Data Input, Channel A34, AN34 (True, Complement)
F4, F5	A35, AN35	High Speed Data Input, Channel A35, AN35 (True, Complement)
D20, E20	A36, AN36	High Speed Data Input, Channel A36, AN36 (True, Complement)

Table 16. VSC3139 Pins (continued)

Diagram Coordinate	Pin Name	Description
E4, E5	A37, AN37	High Speed Data Input, Channel A37, AN37 (True, Complement)
B20, C20	A38, AN38	High Speed Data Input, Channel A38, AN38 (True, Complement)
E2, E3	A39, AN39	High Speed Data Input, Channel A39, AN39 (True, Complement)
B19, C19	A40, AN40	High Speed Data Input, Channel A40, AN40 (True, Complement)
D2, D3	A41, AN41	High Speed Data Input, Channel A41, AN41 (True, Complement)
D19, E19	A42, AN42	High Speed Data Input, Channel A42, AN42 (True, Complement)
D4, D5	A43, AN43	High Speed Data Input, Channel A43, AN43 (True, Complement)
D18, E18	A44, AN44	High Speed Data Input, Channel A44, AN44 (True, Complement)
B4, C4	A45, AN45	High Speed Data Input, Channel A45, AN45 (True, Complement)
B18, C18	A46, AN46	High Speed Data Input, Channel A46, AN46 (True, Complement)
B5, C5	A47, AN47	High Speed Data Input, Channel A47, AN47 (True, Complement)
B17, C17	A48, AN48	High Speed Data Input, Channel A48, AN48 (True, Complement)
B6, C6	A49, AN49	High Speed Data Input, Channel A49, AN49 (True, Complement)
D17, E17	A50, AN50	High Speed Data Input, Channel A50, AN50 (True, Complement)
D6, E6	A51, AN51	High Speed Data Input, Channel A51, AN51 (True, Complement)
D16, E16	A52, AN52	High Speed Data Input, Channel A52, AN52 (True, Complement)
D7, E7	A53, AN53	High Speed Data Input, Channel A53, AN53 (True, Complement)
B16, C16	A54, AN54	High Speed Data Input, Channel A54, AN54 (True, Complement)
B7, C7	A55, AN55	High Speed Data Input, Channel A55, AN55 (True, Complement)
B15, C15	A56, AN56	High Speed Data Input, Channel A56, AN56 (True, Complement)
B8, C8	A57, AN57	High Speed Data Input, Channel A57, AN57 (True, Complement)
D15, E15	A58, AN58	High Speed Data Input, Channel A58, AN58 (True, Complement)
D8, E8	A59, AN59	High Speed Data Input, Channel A59, AN59 (True, Complement)
D14, E14	A60, AN60	High Speed Data Input, Channel A60, AN60 (True, Complement)
D9, E9	A61, AN61	High Speed Data Input, Channel A61, AN61 (True, Complement)
B14, C14	A62, AN62	High Speed Data Input, Channel A62, AN62 (True, Complement)
B9, C9	A63, AN63	High Speed Data Input, Channel A63, AN63 (True, Complement)
B13, C13	A64, AN64	High Speed Data Input, Channel A64, AN64 (True, Complement)
B10, C10	A65, AN65	High Speed Data Input, Channel A65, AN65 (True, Complement)
D13, E13	A66, AN66	High Speed Data Input, Channel A66, AN66 (True, Complement)
D10, E10	A67, AN67	High Speed Data Input, Channel A67, AN67 (True, Complement)
D12, E12	A68, AN68	High Speed Data Input, Channel A68, AN68 (True, Complement)
D11, E11	A69, AN69	High Speed Data Input, Channel A69, AN69 (True, Complement)
B12, C12	A70, AN70	High Speed Data Input, Channel A70, AN70 (True, Complement)
B11, C11	A71, AN71	High Speed Data Input, Channel A71, AN71 (True, Complement)
High-Speed Data Outputs		
M22, M21	Y0, YN0	High Speed Data Output, Channel Y0, YN0 (True, Complement)
R4, R5	Y1, YN1	High Speed Data Output, Channel Y1, YN1 (True, Complement)
M24, M23	Y2, YN2	High Speed Data Output, Channel Y2, YN2 (True, Complement)

Table 16. VSC3139 Pins (continued)

Diagram Coordinate	Pin Name	Description
High-Speed Data Outputs (continued)		
R2, R3	Y3, YN3	High Speed Data Output, Channel Y3, YN3 (True, Complement)
N24, N23	Y4, YN4	High Speed Data Output, Channel Y4, YN4 (True, Complement)
T2, T3	Y5, YN5	High Speed Data Output, Channel Y5, YN5 (True, Complement)
N22, N21	Y6, YN6	High Speed Data Output, Channel Y6, YN6 (True, Complement)
T4, T5	Y7, YN7	High Speed Data Output, Channel Y7, YN7 (True, Complement)
P22, P21	Y8, YN8	High Speed Data Output, Channel Y8, YN8 (True, Complement)
U4, U5	Y9, YN9	High Speed Data Output, Channel Y9, YN9 (True, Complement)
P24, P23	Y10, YN10	High Speed Data Output, Channel Y10, YN10 (True, Complement)
U2, U3	Y11, YN11	High Speed Data Output, Channel Y11, YN11 (True, Complement)
R24, R23	Y12, YN12	High Speed Data Output, Channel Y12, YN12 (True, Complement)
V2, V3	Y13, YN13	High Speed Data Output, Channel Y13, YN13 (True, Complement)
R22, R21	Y14, YN14	High Speed Data Output, Channel Y14, YN14 (True, Complement)
V4, V5	Y15, YN15	High Speed Data Output, Channel Y15, YN15 (True, Complement)
T22, T21	Y16, YN16	High Speed Data Output, Channel Y16, YN16 (True, Complement)
W4, W5	Y17, YN17	High Speed Data Output, Channel Y17, YN17 (True, Complement)
T24, T23	Y18, YN18	High Speed Data Output, Channel Y18, YN18 (True, Complement)
W2, W3	Y19, YN19	High Speed Data Output, Channel Y19, YN19 (True, Complement)
U24, U23	Y20, YN20	High Speed Data Output, Channel Y20, YN20 (True, Complement)
Y2, Y3	Y21, YN21	High Speed Data Output, Channel Y21, YN21 (True, Complement)
U22, U21	Y22, YN22	High Speed Data Output, Channel Y22, YN22 (True, Complement)
Y4, Y5	Y23, YN23	High Speed Data Output, Channel Y23, YN23 (True, Complement)
V22, V21	Y24, YN24	High Speed Data Output, Channel Y24, YN24 (True, Complement)
AB2, AB3	Y25, YN25	High Speed Data Output, Channel Y25, YN25 (True, Complement)
V24, V23	Y26, YN26	High Speed Data Output, Channel Y26, YN26 (True, Complement)
AA2, AA3	Y27, YN27	High Speed Data Output, Channel Y27, YN27 (True, Complement)
W24, W23	Y28, YN28	High Speed Data Output, Channel Y28, YN28 (True, Complement)
AD4, AC4	Y29, YN29	High Speed Data Output, Channel Y29, YN29 (True, Complement)
W22, W21	Y30, YN30	High Speed Data Output, Channel Y30, YN30 (True, Complement)
AB4, AA4	Y31, YN31	High Speed Data Output, Channel Y31, YN31 (True, Complement)
Y22, Y21	Y32, YN32	High Speed Data Output, Channel Y32, YN32 (True, Complement)
AB5, AA5	Y33, YN33	High Speed Data Output, Channel Y33, YN33 (True, Complement)
Y24, Y23	Y34, YN34	High Speed Data Output, Channel Y34, YN34 (True, Complement)
AD5, AC5	Y35, YN35	High Speed Data Output, Channel Y35, YN35 (True, Complement)
AA24, AA23	Y36, YN36	High Speed Data Output, Channel Y36, YN36 (True, Complement)
AD6, AC6	Y37, YN37	High Speed Data Output, Channel Y37, YN37 (True, Complement)
AA22, AA21	Y38, YN38	High Speed Data Output, Channel Y38, YN38 (True, Complement)
AB6, AA6	Y39, YN39	High Speed Data Output, Channel Y39, YN39 (True, Complement)
AB22, AB21	Y40, YN40	High Speed Data Output, Channel Y40, YN40 (True, Complement)

Table 16. VSC3139 Pins (continued)

Diagram Coordinate	Pin Name	Description
High-Speed Data Outputs (continued)		
AB7, AA7	Y41, YN41	High Speed Data Output, Channel Y41, YN41 (True, Complement)
AB24, AB23	Y42, YN42	High Speed Data Output, Channel Y42, YN42 (True, Complement)
AD7, AC7	Y43, YN43	High Speed Data Output, Channel Y43, YN43 (True, Complement)
AC23, AD22	Y44, YN44	High Speed Data Output, Channel Y44, YN44 (True, Complement)
AD8, AC8	Y45, YN45	High Speed Data Output, Channel Y45, YN45 (True, Complement)
AD21, AC21	Y46, YN46	High Speed Data Output, Channel Y46, YN46 (True, Complement)
AB8, AA8	Y47, YN47	High Speed Data Output, Channel Y47, YN47 (True, Complement)
AD20, AC20	Y48, YN48	High Speed Data Output, Channel Y48, YN48 (True, Complement)
AB9, AA9	Y49, YN49	High Speed Data Output, Channel Y49, YN49 (True, Complement)
AB20, AA20	Y50, YN50	High Speed Data Output, Channel Y50, YN50 (True, Complement)
AD9, AC9	Y51, YN51	High Speed Data Output, Channel Y51, YN51 (True, Complement)
AB19, AA19	Y52, YN52	High Speed Data Output, Channel Y52, YN52 (True, Complement)
AD10, AC10	Y53, YN53	High Speed Data Output, Channel Y53, YN53 (True, Complement)
AD19, AC19	Y54, YN54	High Speed Data Output, Channel Y54, YN54 (True, Complement)
AB10, AA10	Y55, YN55	High Speed Data Output, Channel Y55, YN55 (True, Complement)
AD18, AC18	Y56, YN56	High Speed Data Output, Channel Y56, YN56 (True, Complement)
AB11, AA11	Y57, YN57	High Speed Data Output, Channel Y57, YN57 (True, Complement)
AB18, AA18	Y58, YN58	High Speed Data Output, Channel Y58, YN58 (True, Complement)
AD11, AC11	Y59, YN59	High Speed Data Output, Channel Y59, YN59 (True, Complement)
AB17, AA17	Y60, YN60	High Speed Data Output, Channel Y60, YN60 (True, Complement)
AD12, AC12	Y61, YN61	High Speed Data Output, Channel Y61, YN61 (True, Complement)
AD17, AC17	Y62, YN62	High Speed Data Output, Channel Y62, YN62 (True, Complement)
AB12, AA12	Y63, YN63	High Speed Data Output, Channel Y63, YN63 (True, Complement)
AD16, AC16	Y64, YN64	High Speed Data Output, Channel Y64, YN64 (True, Complement)
AB13, AA13	Y65, YN65	High Speed Data Output, Channel Y65, YN65 (True, Complement)
AB16, AA16	Y66, YN66	High Speed Data Output, Channel Y66, YN66 (True, Complement)
AD13, AC13	Y67, YN67	High Speed Data Output, Channel Y67, YN67 (True, Complement)
AB15, AA15	Y68, YN68	High Speed Data Output, Channel Y68, YN68 (True, Complement)
AD14, AC14	Y69, YN69	High Speed Data Output, Channel Y69, YN69 (True, Complement)
AD15, AC15	Y70, YN70	High Speed Data Output, Channel Y70, YN70 (True, Complement)
AB14, AA14	Y71, YN71	High Speed Data Output, Channel Y71, YN71 (True, Complement)

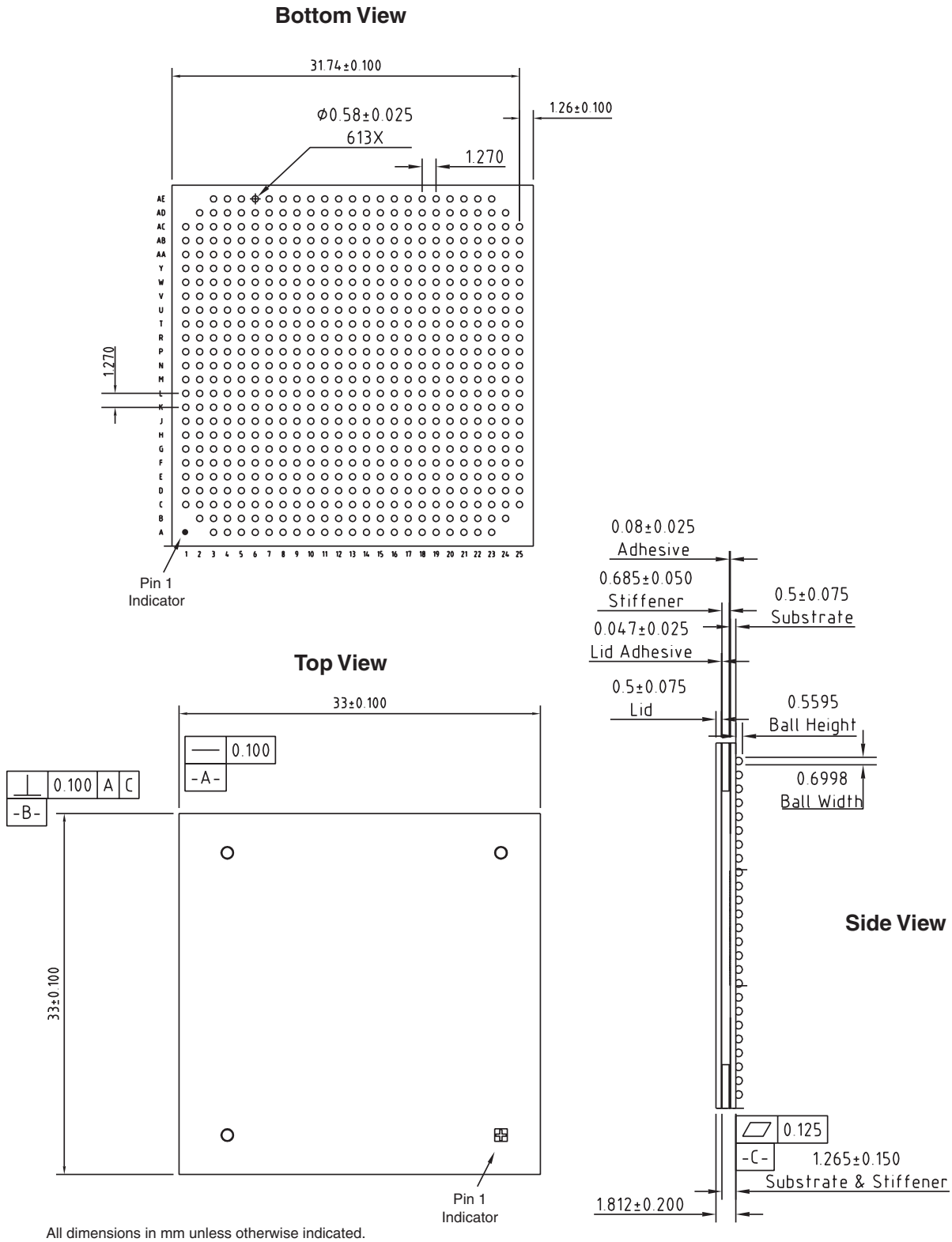
Table 16. VSC3139 Pins (continued)

Diagram Coordinate	Pin Name	Description
Power Supply		
A3, A10, A16, A23, C1, C25, G8, G9, G12, G13, G16, G17, H8, H9, H12, H13, H16, H17, J6, J7, J10, J11, J14, J15, J18, J19, K1, K6, K7, K10, K11, K14, K15, K18, K19, K25, L8, L9, L12, L13, L16, L17, M8, M9, M12, M13, M16, M17, N6, N7, N10, N11, N14, N15, N18, N19, P6, P7, P10, P11, P14, P15, P18, P19, R8, R9, R12, R13, R16, R17, T1, T8, T9, T12, T13, T16, T17, T25, U6, U7, U10, U11, U14, U15, U18, U19, V6, V7, V10, V11, V14, V15, V18, V19, W8, W9, W12, W13, W16, W17, Y8, Y9, Y12, Y13, Y16, Y17, AC1, AC25, AE3, AE10, AE16, AE23	VCC	Positive Power Supply, 2.5 volts
A7, A19, F1, G25, N12, N13, P12, P13, W25, Y1, AE7, AE19	VCCD	Positive Power Supply for Programming Interface, 2.5/3.3 volts
A4, A13, A22, B2, B3, B22, B23, B24, C2, C24, D1, D25, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, F16, F17, F18, F19, F20, G6, G7, G10, G11, G14, G15, G18, G19, G20, H6, H7, H10, H11, H14, H15, H18, H19, H20, J8, J9, J12, J13, J16, J17, J20, K8, K9, K12, K13, K16, K17, K20, L6, L7, L10, L11, L14, L15, L18, L19, L20, M6, M7, M10, M11, M14, M15, M18, M19, M20, N1, N8, N9, N16, N17, N20, N25, P8, P9, P16, P17, P20, R6, R7, R10, R11, R14, R15, R18, R19, R20, T6, T7, T10, T11, T14, T15, T18, T19, T20, U8, U9, U12, U13, U16, U17, U20, V8, V9, V12, V13, V16, V17, V20, W6, W7, W10, W11, W14, W15, W18, W19, W20, Y6, Y7, Y10, Y11, Y14, Y15, Y18, Y19, Y20, AB1, AB25, AC2, AC3, AC22, AC24, AD2, AD3, AD23, AD24, AE4, AE13, AE22	VEE	Negative Power Supply, 0 volts
Blanks		
A1, A2, A24, A25, B1, B25, AD1, AD25, AE1, AE2, AE24, AE25	(blank)	No Pin Present
No Connection		
A5, A9, C3, M1, P1, V1, AE5, AE6, AE8, AE9, AE11, AE12	NC	Do Not Connect
Programming Inputs		
AA25	ADDR/DATA0	Address/Data Programming Input [0]
Y25	ADDR/DATA1	Address/Data Programming Input [1]
F25	ADDR/DATA10	Address/Data Programming Input [10]
V25	ADDR/DATA2	Address/Data Programming Input [2]

Table 16. VSC3139 Pins (continued)

Diagram Coordinate	Pin Name	Description
Programming Inputs (continued)		
U25	ADDR/DATA3	Address/Data Programming Input [3]
R25	ADDR/DATA4	Address/Data Programming Input [4]
P25	ADDR/DATA5	Address/Data Programming Input [5]
M25	ADDR/DATA6	Address/Data Programming Input [6]
L25	ADDR/DATA7	Address/Data Programming Input [7]
J25	ADDR/DATA8	Address/Data Programming Input [8]
H25	ADDR/DATA9	Address/Data Programming Input [9]
E25	ALE	Address Latch Enable
AE17	CONFIG	Multiple Reconfiguration Strobe Input, active High
AE14	CSB	Chip Select, active Low
A20	DRIVE	High Speed DRIVE Input (True)
A18	DRIVEB	High Speed DRIVE Input (Complelement)
AE20	INITB	Switch Initialization Input, active Low
A8	OVERTEMP	Over-Temperature Alarm Output, active High
AE15	PARALLEL/ SERIALB	Parallel/Serial Mode Select, High=Parallel programming, Low=Serial programming
U1	PRBS_CLK	PRBS Generator Clock Input (True)
R1	PRBS_CLKB	PRBS Generator Clock Input (Complement)
H1	PRBS_ERRDET	PRBS Error Detector Output, active High
J1	PRBS_IN	PRBS Data Input (True)
L1	PRBS_INB	PRBS Data Input (Complement)
W1	PRBS_OUT	PRBS Data Output (True)
AA1	PRBS_OUTB	PRBS Data Output (Complement)
AE18	RDB	Read Strobe, active Low
A6	RESETB	Reset, active Low
A21	SEC_CSB	Seconday Port Chip Select, active Low
A17	SEC_READ	Seconday Port Read Strobe, active Low
A12	SEC_SCLK	Seconday Port Serial Clock
A14	SEC_SDIN	Seconday Port Serial Data Input
A11	SEC_SDOUT	Seconday Port Serial Data Output
A15	SEC_WRITE	Seconday Port Write Strobe, active High
E1	SENSE	High Speed Data Sense Output (True)
G1	SENSEN	High Speed Data Sense Output (Complement)
AE21	WRB	Write Strobe, active Low

Package Drawing



All dimensions in mm unless otherwise indicated.

MOISTURE SENSITIVITY

This device is rated moisture sensitivity level 4 as specified in JEDEC standard IPC/JEDEC J-STD-020B. For more information, see the JEDEC standard.

ORDERING INFORMATION

Part Number	Description
VSC3139SH	613 BGA, 33mm x 33mm, 1.27mm Ball Pitch

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