FREEDM™-84A1024

Frame Engine and Datalink Manager 84A1024

DATA SHEET

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Legal Information

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PMC-2000689 (R4)

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Patents

The technology discussed is protected by one or more of the following Patents:

U.S. Patent No. 5,640,398, 6,188,699 and 6,333,935

Can. Patent No. 2,161,921, 2,224,392, 2,234,493

Relevant patent applications and other patents may also exist.

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1. Acronyms

Table 1 - Terminology

Term	Definition
ADDR	The Address Field in a PPP header
ANY-PHY	Saturn Interface Specification and Interoperability Framework for Packet and Cell transfers between Physical layer and Link Layer devices
APPI	ANY-PHY Packet Interface
B	The Begin bit of a fragment
BECN	Backward Explicit Congestion Notification
C/R	Command/Response bit in the Q.922 Header
CI	Connection Identifier
CRC	Cyclic Redundancy Check
CRC-CCITT	Cyclic Redundancy Check as specified by the CCITT
CNTL	Control field in a PPP header
COS	Class of Service
Datagram	A fragment, packet or frame
DE	Discard Eligibility
DLL	Digital Delay Lock Loop
DSLAM	Digital Subscriber Loop Access Multiplexor
E	The End bit of a fragment
EC	Error Code
ECC	Error Correcting Code
Egress	Traffic flow from the switch to the line is defined as Egress traffic – equivalent to transmit
EOP	End of Packet
FECN	Forward Explicit Congestion Notification
FIFO	First In First Out
FCS	Frame Check Sequence
FR	Frame Relay
Fragment	A sub-unit of a packet of frame
Frame	A Frame Relay unit of transfer
FUNI	Frame Relay User to Network Interface
HDLC	High level Data Link Control
Ingress	Traffic flow from the line side to switch is defined as Ingress traffic – equivalent to receive
IETF	Internet Engineering Task Force

Term	Definition
MIB	Management Information Database
ML	Multilink
ML-FR	Multilink Frame Relay
ML-PPP	Multilink PPP
MTU	Maximum Transmission Unit
MRU	Maximum Receive Unit
NNI	Network-to-Network Interface
Packet	An IP data unit
PID	Protocol ID field in a PPP header
PPP	Point to Point Protocol
Q.922	ISDN Data Link Layer Specification for Frame Mode Bearer Services
RFC	Request For Comments
SBI	Scalable Bandwidth Interface
SDRAM	Synchronous Dynamic Random Access Memory
SN	Sequence Number
SPE	Synchronous Payload Envelop
SSRAM	Synchronous Static Random Access Memory
TM	Traffic Management
UNI	User-to-Network Interface
ZBT	Zero Bus Turnaround

2. Features

- Single-chip multi-channel HDLC controller with either a 52 MHz 16 bit ANY-PHY Level 2 or a 104MHz 8 bit ANY-PHY Level 3 packet interface for transfer of packet or frame data using an external controller.

- Supports line rate throughput for 84 T1s, 63 E1s, or 3 DS-3s. (40 byte packets encapsulated in PPP over HDLC (50 byte transfers (RFC 1661) or 55 byte transfers (RFC 1990))).

- Provides simultaneous support of PPP, Frame Relay, multilink-PPP and multilink-Frame Relay protocols. Alternative protocols supported via HDLC termination and full packet store of the data within the HDLC structure.

Interfaces

- A 52MHz, 16-bit ANY-PHY Level 2 or 104MHz, 8-bit ANY-PHY Level 3 packet interface for system side connection.

    - The interface is capable of supporting full datagram transfer on a per ANY-PHY channel basis or

    - Fragmented packets or frames on a per ANY-PHY channel basis.

- A single 19.44 or 77.76 MHz SBI/SBI336 bus supporting up to 84 links.

- 3 separate clock and data interfaces to support 3 links of arbitrary data rate up to 52MHz (e.g., DS3/E3)

- A 100 MHz, 48-bit SDRAM interface for ingress and egress per packet/fragment storage.

- A 100 MHz, 32-bit SDRAM interface for ingress re-sequencing data structures.

- A 100 MHz, 36-bit SSRAM interface for Ingress/Egress Context storage.

- The device provides the standard 5 signal P1149.1 JTAG test port for boundary scan.

- A 32-bit microprocessor interface for configuration and status monitoring.

Channelization/HDLC Features

- Support for up to 1024 HDLC channels in both the ingress and egress direction, with individual HDLC channel speeds ranging from 56Kbps to 52 Mbps.

- The 1024 HDLC channels can be assigned to a mixture of physical links via the SBI interface. The SBI transports the equivalent of 3 STS-1 synchronous payload envelopes (SPE). Each STS-1 SPE can be individually configured to carry 28 T1/J1s, 21 E1s,1 DS3 or 1 Fractional Rate DS3/E3.

- Supports 3 individual clock and data interfaces that can individually operate at up to 52 MHz. The device can be configured to process data from either the clock and data interfaces or from the SBI on a per clock-data-link/SPE basis.

- In a channelized application, the number of time-slots assigned to an HDLC channel is programmable from 1 to 24 (for T1/J1) and from 1 to 31 (for E1).

- For each channel, the HDLC receiver supports programmable flag sequence detection, bit de-stuffing and frame check sequence validation. The receiver supports the validation of both CRC-CCITT and CRC-32 frame check sequences.

- For each HDLC channel, the receiver checks for packet abort sequences, octet aligned packet length and for minimum and maximum packet length.

- For each HDLC channel, time-slots are selectable to be in 56 Kbps format or 64 Kbps clear channel format.

- For each HDLC channel, the HDLC transmitter supports programmable flag sequence generation, bit stuffing and frame check sequence generation. The transmitter supports the generation of both CRC-CCITT and CRC-32 frame check sequences. The transmitter also aborts packets under the direction of the external TM engine or automatically when the channel underflows.

PPP Features

- Link Control protocol packet identification. Packets are identified by the PID as control protocols and will be forwarded to the ANY-PHY interface.

- Capable of supporting line rate transfers of packet sizes from 40 to 9.6K bytes.

- Support for PPP header compression as per RFC 1661 on sequenced links. On receive, compressed headers are detected and processed appropriately as they arrive on an HDLC channel. Compressed PPP headers are passed to the system side via the ANY-PHY interface. On transmit, compressed headers are accepted from the system side device via the ANY-PHY interface. On sequenced links, all required processing is provided to correctly insert the compressed PPP headers into the 1024 HDLC channels. On non-sequenced links, header compression is only supported through the use of transparent mode.

- RFC-1990 Multilink PPP bundles:

    - Capable of supporting fragment sizes from 6 to 9.6K bytes with the restriction that the maximum number of fragments per packet is 81.

    - Support for 3 egress fragmentation sizes (128, 256, and 512 bytes) configurable per connection. Optionally full packet transfers are supported on a per connection basis. The FREEDM 84A1024 supports header compression but does not perform it.

    - Either 12 bit or 24bit sequence number, with short and long fragment header formats, is supported.

- Supports 42 bundles in ingress direction. These bundles are composed of independent HDLC channels.
- Supports 42 bundles in egress direction. These bundles are composed of independent HDLC channels.
- Support for fragmentation on a single HDLC channel.
- Support for 16 COS levels in accordance with RFC 2686.
- Support for up to 100ms of intra bundle skew in the receive direction when supporting the minimum fragment size. Capable of supporting larger skews (<400ms) with larger fragment sizes. The intra-bundle skew is limited by 12 bit sequence number capabilities.
- Up to 12 member links per bundle.
    - Each member link is required to operate at the same speed. Either T1/J1 or E1 rates.

Frame Relay Features

- Link layer address lookup can be performed based on HDLC channel and DLCI for HDLC channels supporting Frame Relay protocols. Optionally, the lookup can be performed on a per HDLC channel basis.
    - Capable of supporting line rate transfers of frame sizes from 40 to 9.6K bytes.
- FRF.16 Multilink FR bundles and FRF.12 UNI and NNI (not End-to-End) fragmentation:
    - Capable of supporting fragment sizes from 4 to 9.6K bytes with the restriction that the maximum number of fragments per packet is 81.
    - 10 bit DLCI format supported for channels operating in Frame Relay mode. Alternative DLCI formats supported when the lookup is based on HDLC channel only.
    - The lookup algorithm can support a maximum of 16K connection identifiers (CIs) amongst all channels in use.
    - FRF-16 Control frames (Link Integrity Protocol) are identified and forwarded to the ANY-PHY interface.
    - Support for 3 egress fragmentation sizes (128, 256, and 512 bytes) configurable per connection. Optionally full packet transfers are supported on a per connection basis.
    - 12 bit sequence numbers supported.

- Support for fragmentation on a single HDLC channel.
- 42 bundles in ingress direction. These bundles are composed of independent HDLC channels.
- 42 bundles in egress direction. These bundles are composed of independent HDLC channels.
- Support for up to 100ms intra-bundle skew within the limits of 12 bit sequence number capabilities when supporting the minimum fragment size. Capable of supporting larger skews (<400ms) with larger fragment sizes.
- Up to 12 member links per bundle.
    - Each member link operates at the same speed either T1/J1 or E1.
    - FECN, BECN, and DE ingress processing as per FRF.12. The C/R value passed out in frame out mode is the value received on the Begin fragment.

Statistics

- FREEDM 84A1024 maintains a suite of counters based on HDLC channels. These counters include:
    - CRC Errors observed by the HDLC framer.
    - HDLC framing aborts.
    - Non-Octet aligned frames.
    - HDLC MRU exceeded.
    - Bytes and datagrams received.
    - Bytes and datagrams transmitted.
- Additionally, the FREEDM 84A1024 provides the following global error counters:
    - Number of bytes discarded due to transmit overflows, receive overflows in the presence of link failures, and line rate arrivals of small (< 40 byte) packets.
    - Number of Lost fragment events
    - FIFO overflows and underruns.
    - Additional error states are also tracked.

- Additionally, FREEDM 84A1024 supports the MFR MIB by detecting and informing the host of unexpected sequence numbers and time outs.

Fault Isolation Features

- Three levels of loopback are provided:
- Three Clock and Data line loopbacks
- SBI tributary loopback
- System side loopback per HDLC channel.

Technologies

- 520 pin (1.27 mil pitch) thermally enhanced ball grid array (TEBGA) package.
- 342 signal pins, 3.3V I/O.
- Low power 0.18µm CMOS technology using 1.8V core power.

3. References

PPP

1. RFC 1661, The Point-to-Point Protocol (PPP).
2. RFC 1990, PPP Multilink Protocol.
3. RFC-2686, Multiclass Multilink PPP.

Frame Relay

1. ANSI T1.617a-1994, Annex F.
2. RFC 1490, Multiprotocol Interconnect over Frame Relay.
3. FRF.1.1, User-to-Network (UNI) Implementation Agreement.
4. FRF.3.1, Multiprotocol Encapsulation Implementation Agreement (MEI).
5. FRF.4.1, Frame Relay User-to-Network SVC Implementation Agreement.
6. FRF.12, Frame Relay Fragmentation Implementation Agreement.
7. FRF.16, Multilink Frame Relay (MFR) PVC Implementation Agreement.

HDLC Standards

1. International Organization for Standardization, ISO Standard 3309-1993, "Information Technology - Telecommunications and information exchange between systems - High-Level Data Link Control (HDLC) procedures - Frame structure", December 1993.
2. RFC-1662 - "PPP in HDLC-like Framing" Internet Engineering Task Force, July 1994.

Misc. References

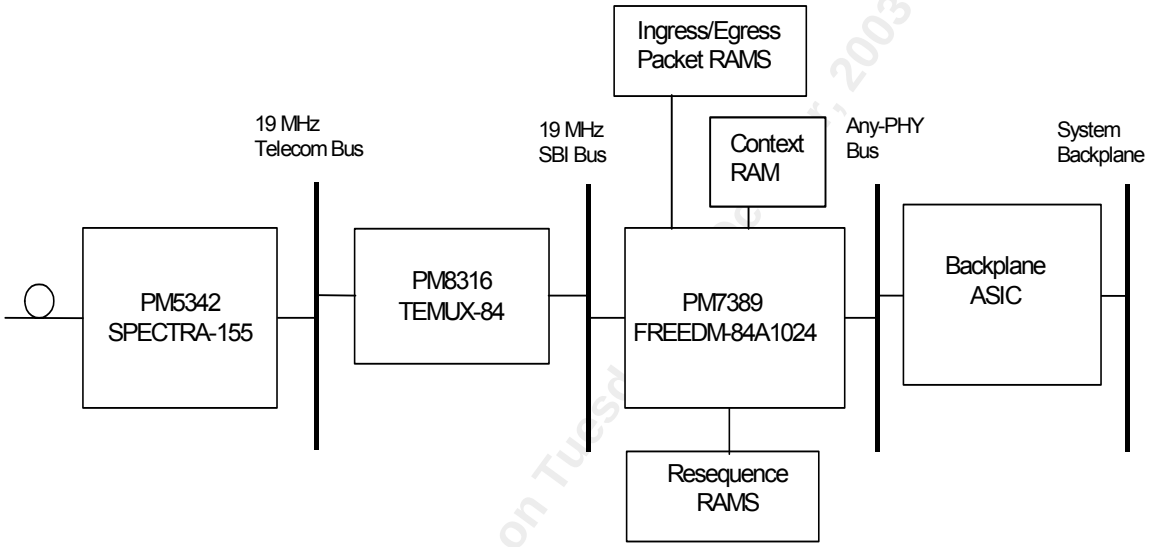
1. PMC-1991437 – “High Density T1/E1 Framer with Integrated VT/TU Mapper and M13 Multiplexer (TEMUX 84) Data Sheet”, PMC-Sierra Inc.

4. Applications

- IETF PPP interfaces for routers.
- Frame Relay interfaces for ATM or Frame Relay switches and multiplexers.
- FUNI or Frame Relay service inter-working interfaces for ATM switches and multiplexers.
- Internet/Intranet access equipment.
- Multiservice DSLAM equipment.

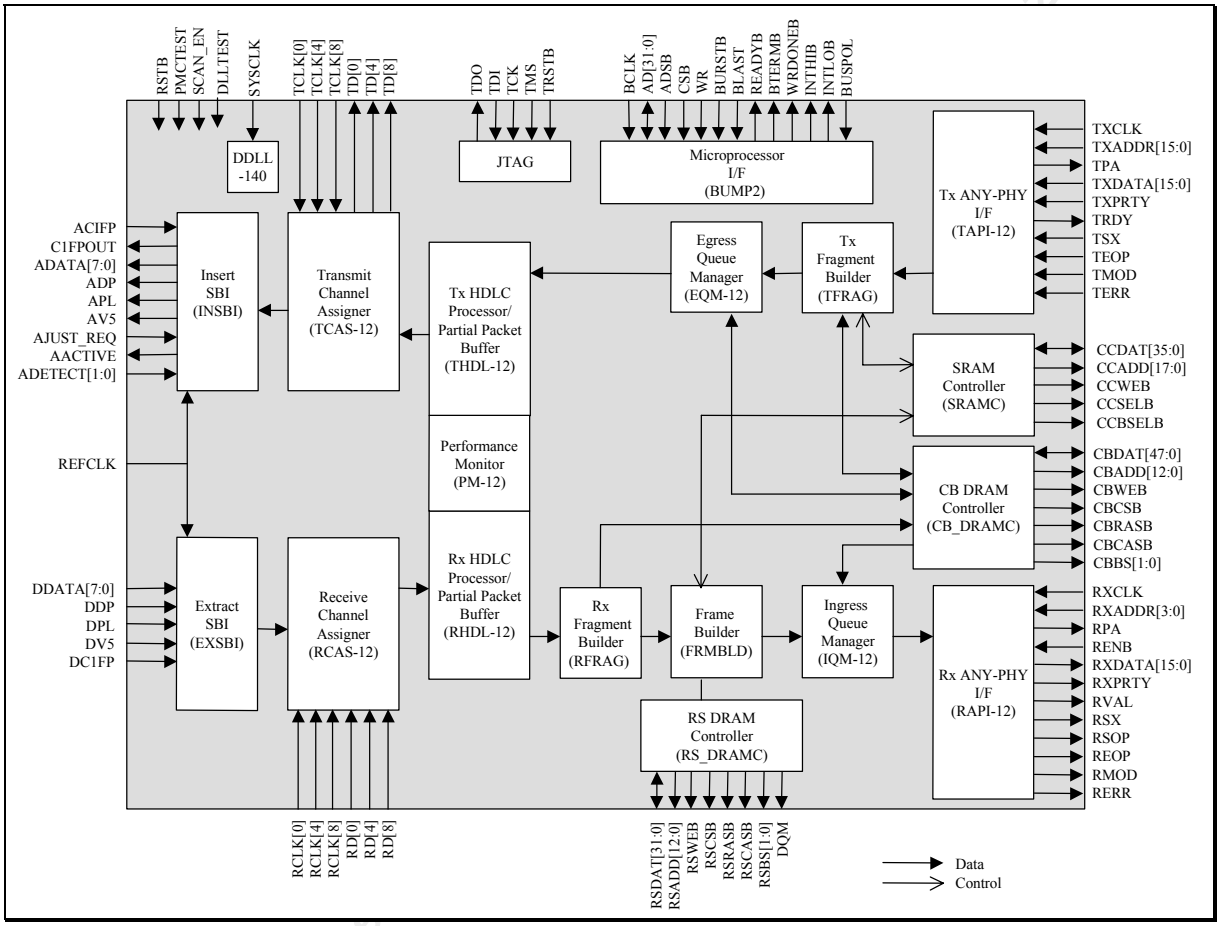
5. Application Examples

Figure 1 - OC3 Access Card for a Router



6. Block Diagram

Figure 2 - Block Diagram for FREEDM 84A1024



7. Description

The FREEDM 84A1024 device is a monolithic integrated circuit supporting highly channelized termination of HDLC-framed Point to Point Protocol (PPP) and Frame Relay, including multilink variants.

On the Line side, the FREEDM 84A1024 device supports an SBI interface and three clock and data interfaces for subrate DS3/E3 support. The FREEDM 84A1024 can support up to 1024 HDLC channels provisioned across these interfaces. On the system side, the FREEDM 84A1024 provides a Level 2 and Level 3 APPI presenting a channelized interface capable of supporting full frame/packet transfers as well as fragment data transfers. Rate adaptation between the line and system interfaces is provided by external buffers.

The FREEDM 84A1024 terminates up to 1024 HDLC channels of HDLC framed PPP or Frame Relay with speeds ranging from 56 Kbps to 52 Mbps in the ingress direction. HDLC channels may contain a mix of protocols and speeds up to an aggregate of 156 Mbps. FREEDM 84A1024 provides HDLC header removal, CRC checking and stripping. Data path termination including frame/packet re-assembly and multilink termination is provided in hardware.

In the egress direction, the FREEDM 84A1024 receives packets from the external controller. The FREEDM 84A1024 provides support for ML-FR and ML-PPP protocols by fragmenting transmitted packets, appending the appropriate sequence number and assigning the fragment to an HDLC channel within the multilink bundle. FREEDM 84A1024 is also capable of supporting full packet transfer on up to 1024 HDLC channels that are not configured to support multlilink. The HDLC processor within FREEDM 84A1024 encapsulates the data with HDLC flags, CRC bytes and performs the appropriate bit stuffing.

8. Pin Diagram

The FREEDM 84A1024 is manufactured in a 520 pin (1.27 mil pitch) enhanced ball grid array package.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VDD3V3	VSS	VSS	VSS	CCDAT27	VSS	CCDAT20	CCDAT17	CCDAT12	CCDAT8	VSS	CCDAT0	TDI	NC	TDO	VSS	VSS	VSS	VSS	INTLOB	VSS	CSB	AD29	AD26	AD21	VSS	AD14	VSS	VSS	VSS	VDD3V3	A
B	VSS	VDD3V3	VSS	CCDAT32	CCDAT29	CCDAT24	VDD1V8	NC	CCDAT14	CCDAT9	CCDAT5	CCDAT1	NC	TD4	NC	VSS	VSS	VSS	TCLK0	INTHIB	BLAST	ADSB	NC	AD24	AD20	AD17	AD12	AD9	VSS	VDD3V3	VSS	B
C	VSS	VSS	VDD3V3	VDD3V3	CCDAT31	CCDAT26	CCDAT22	NC	CCDAT15	CCDAT10	CCDAT6	CCDAT2	NC	NC	NC	VDD3V3	VSS	TCLK4	VDD1V8	WRDONEB	BURSTB	AD31	NC	AD23	AD19	AD15	AD10	VDD3V3	VDD3V3	VSS	VSS	C
D	VSS	CCDAT35	VDD3V3	VDD3V3	CCDAT33	CCDAT28	CCDAT23	CCDAT19	CCDAT16	CCDAT11	CCDAT7	CCDAT3	VDD1V8	NC	VDD1V8	VDD3V3	TCLK8	VSS	SCAN_EN	BTERMB	WR	AD30	AD27	AD22	AD18	AD13	AD8	VDD3V3	VDD3V3	AD6	VSS	D
E	CCADD15	CCADD17	CCSELB	CCDAT34	VDD3V3	CCDAT30	CCDAT25	CCDAT21	CCDAT18	CCDAT13	VDD3V3	CCDAT4	NC	NC	NC	VDD3V3	VSS	VSS	BUSPOL	READYB	VDD3V3	AD28	AD25	VDD1V8	AD16	AD11	VDD3V3	AD7	AD5	AD3	AD1	E
F	VSS	CCADD12	CCADD14	CCADD16	CCWEB																						AD4	AD2	AD0	TRSTB	VSS	F
G	CCADD8	CCADD9	CCADD10	CCADD11	CCADD13																						BCLK	TMS	TCK	VDD1V8	TDO	G
H	CCADD3	CCADD5	CCADD6	CCADD7	VDD1V8																						TDI	PMCTEST	RSTB	DLLTEST	SYSCLK	H
J	CCADD0	NC	NC	CCADD2	CCADD4																						NC	TERR	TMOD	TEOP	TRDY	J
K	C1FPOUT	AC1FP	CCBSELB	NC	CCADD1																						TSX	TXPRTY	TXDATA15	TXDATA14	TXDATA13	K
L	VSS	ADATA2	ADATA1	ADATA0	VDD3V3																						VDD3V3	TXDATA12	TXDATA11	TXDATA10	VSS	L
M	ADATA7	ADATA6	ADATA5	ADATA4	ADATA3																						TXDATA9	TXDATA8	TXDATA7	TXDATA6	TXDATA5	M
N	AJUST_REQ	AV5	VDD1V8	APL	ADP																						TXDATA4	VDD1V8	TXDATA3	TXDATA2	TXDATA1	N
P	DC1FP	REFCLK	ADETECT1	ADETECT0	AACTIVE																						TXDATA0	TPA	TXADDR15	TXADDR14	TXADDR13	P
R	DDATA4	DDATA3	DDATA2	DDATA1	DDATA0																						TXADDR12	VDD1V8	NC	TXADDR11	TXADDR10	R
T	VSS	VSS	VDD3V3	VDD3V3	VDD3V3																						VDD3V3	VDD3V3	VDD3V3	VSS	VSS	T
U	DDATA5	DDATA6	NC	NC	DDATA7																						TXADDR5	TXADDR6	TXADDR7	TXADDR8	TXADDR9	U
V	DDP	DPL	DV5	RSADD0	RSADD1																						TXADDR0	TXADDR1	TXADDR2	TXADDR3	TXADDR4	V
W	RSADD2	RSADD3	RSADD4	VDD1V8	RSADD5																						REOP	RMOD	VDD1V8	RVAL	RERR	W
Y	RSADD6	RSADD7	RSADD8	RSADD9	RSADD10																						RXDATA15	RXPRTY	TXCLK	RSX	RSOP	Y
AA	VSS	RSADD11	RSADD12	RSWEB	VDD3V3																						VDD3V3	RXDATA12	RXDATA13	RXDATA14	VSS	AA
AB	RSCSB	RSRASB	RSCASB	RSBS0	RSDAT0																						RXDATA6	RXDATA8	RXDATA9	RXDATA10	RXDATA11	AB
AC	RSBS1	RSDAT1	RSDAT2	RSDAT3	RSDAT5																						RXDATA2	RXDATA4	DQM	RXDATA5	RXDATA7	AC
AD	RSDAT4	NC	NC	RSDAT6	RSDAT8																						VDD1V8	RENB	RXDATA0	RXDATA1	RXDATA3	AD
AE	RSDAT7	VDD1V8	RSDAT9	RSDAT10	RSDAT12																						RXCLK	RXADDR1	RXADDR2	RXADDR3	RPA	AE
AF	VSS	RSDAT11	RSDAT13	RSDAT15	RSDAT17																						CBCSB	CBCASB	CBBS1	RXADDR0	VSS	AF
AG	RSDAT14	RSDAT16	RSDAT18	RSDAT20	VDD3V3	RSDAT24	RSDAT29	VDD1V8	VSS	NC	VDD3V3	VSS	VSS	CBDAT3	CBDAT8	VDD3V3	CBDAT15	CBDAT20	CBDAT24	CBDAT29	VDD3V3	CBDAT38	CBDAT43	CBDAT46	CBADD2	CBADD7	VDD3V3	CBADD11	CBWEB	CBRASB	CBBS0	AG
AH	VSS	RSDAT19	VDD3V3	VDD3V3	RSDAT21	RSDAT26	RSDAT31	VSS	RCLK4	VSS	VSS	VSS	CBDAT0	CBDAT4	CBDAT9	VDD3V3	NC	CBDAT19	VDD1V8	CBDAT28	CBDAT32	CBDAT36	CBDAT41	CBDAT44	CBADD0	CBADD5	CBADD10	VDD3V3	VDD3V3	CBADD12	VSS	AH
AJ	VSS	VSS	VDD3V3	VDD3V3	RSDAT23	RSDAT28	RCLK0	VSS	RD4	VSS	RCLK8	VSS	VDD1V8	CBDAT5	CBDAT10	VDD3V3	NC	CBDAT18	CBDAT23	CBDAT27	CBDAT31	CBDAT35	CBDAT40	NC	CBDAT47	CBADD3	CBADD8	VDD3V3	VDD3V3	VSS	VSS	AJ
AK	VSS	VDD3V3	VSS	RSDAT22	RSDAT25	RSDAT30	RD0	VSS	NC	VSS	RD8	VSS	CBDAT1	CBDAT6	CBDAT11	VSS	CBDAT14	CBDAT17	CBDAT22	CBDAT26	CBDAT30	CBDAT34	CBDAT39	NC	VDD1V8	CBADD1	CBADD6	CBADD9	VSS	VDD3V3	VSS	AK
AL	VDD3V3	VSS	VSS	VSS	RSDAT27	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CBDAT2	CBDAT7	CBDAT12	VSS	CBDAT13	CBDAT16	CBDAT21	CBDAT25	VSS	CBDAT33	CBDAT37	CBDAT42	CBDAT45	VSS	CBADD4	VSS	VSS	VSS	VDD3V3	AL
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

9. Pin Description

Table 2 SBI Interface signals (30 pins)

Pin Name	Type	Pin No.	Function
REFCLK	Input	P30	The SBI reference clock signal (REFCLK) provides reference timing for the SBI ADD and DROP busses. REFCLK is nominally a 50% duty cycle clock of frequency 19.44 MHz ±50ppm for SBI bus operation or 77.76 MHz ±20ppm for SBI336 bus operation.
DC1FP	Input	P31	The C1 octet frame pulse signal (DC1FP) for the drop bus provides frame synchronization for devices connected via an SBI interface. DC1FP must be asserted for 1 REFCLK cycle every 500 µs or multiples thereof (i.e. every 9720 x n REFCLK cycles, where n is a positive integer). All devices interconnected via the SBI drop interface must be synchronized to a DC1FP signal from a single source. DC1FP is sampled on the rising edge of REFCLK. Note – If the SBI bus is being operated in synchronous mode, DC1FP must be asserted for 1 REFCLK cycle every 6 ms or multiples thereof.
AC1FP	Input	K30	The C1 octet frame pulse signal (AC1FP) for the add bus provides frame synchronization for devices connected via an SBI interface. AC1FP must be asserted for 1 REFCLK cycle every 500 µs or multiples thereof (i.e. every 9720 x n REFCLK cycles, where n is a positive integer). All devices interconnected via the add SBI interface must be synchronized to an AC1FP signal from a single source. AC1FP is sampled on the rising edge of REFCLK. Note – If the SBI bus is being operated in synchronous mode, AC1FP must be asserted for 1 REFCLK cycle every 6 ms or multiples thereof.
C1FPOUT	Output	K31	The C1 octet frame pulse output signal (C1FPOUT) may be used to provide frame synchronization for devices interconnected via an SBI interface. C1FPOUT is asserted for 1 REFCLK cycle every 500 µs (i.e. every 9720 REFCLK cycles). C1FPOUT is updated on the rising edge of REFCLK. Note – The C1FPOUT pulse is not suitable for use in systems in which the SBI bus is operated in synchronous mode.
DDATA[0] DDATA[1] DDATA[2] DDATA[3] DDATA[4] DDATA[5] DDATA[6] DDATA[7]	Input	R27 R28 R29 R30 R31 U31 U30 U27	The SBI DROP bus data signals (DDATA[7:0]) contain the time division multiplexed receive data from the up to 84 independently timed links. Data from each link is transported as a tributary within the SBI TDM bus structure. Multiple PHY devices can drive the SBI DROP bus at uniquely assigned tributary column positions. DDATA[7:0] are sampled on the rising edge of REFCLK.

Pin Name	Type	Pin No.	Function
DDP	Input	V31	The SBI DROP bus parity signal (DDP) carries the even or odd parity for the DROP bus signals. The parity calculation encompasses the DDATA[7:0], DPL and DV5 signals. Multiple PHY devices can drive DDP at uniquely assigned tributary column positions. This parity signal is intended to detect accidental PHY source clashes in the column assignment. DDP is sampled on the rising edge of REFCLK.
DPL	Input	V30	The SBI DROP bus payload signal (DPL) indicates valid data within the SBI TDM bus structure. This signal is asserted during all octets making up a tributary. This signal may be asserted during the V3 or H3 octet within a tributary to accommodate negative timing adjustments between the tributary rate and the fixed TDM bus structure. This signal may be de-asserted during the octet following the V3 or H3 octet within a tributary to accommodate positive timing adjustments between the tributary rate and the fixed TDM bus structure. Multiple PHY devices can drive DPL at uniquely assigned tributary column positions. DPL is sampled on the rising edge of REFCLK.
DV5	Input	V29	The SBI DROP bus payload indicator signal (DV5) locates the position of the floating payloads for each tributary within the SBI TDM bus structure. Timing differences between the port timing and the TDM bus timing are indicated by adjustments of this payload indicator relative to the fixed TDM bus structure. Multiple PHY devices can drive DV5 at uniquely assigned tributary column positions. All movements indicated by this signal must be accompanied by appropriate adjustments in the DPL signal. DV5 is sampled on the rising edge of REFCLK.
ADATA[0] ADATA[1] ADATA[2] ADATA[3] ADATA[4] ADATA[5] ADATA[6] ADATA[7]	Tristate Output	L28 L29 L30 M27 M28 M29 M30 M31	The SBI ADD bus data signals (ADATA[7:0]) contain the time division multiplexed transmit data from the up to 84 independently timed links. Data from each link is transported as a tributary within the SBI TDM bus structure. Multiple link layer devices can drive the SBI ADD bus at uniquely assigned tributary column positions. When the FREEDM 84A1024 is not outputting data on a particular tributary column ADATA[7:0] are driven or tri-stated based on the DEFAULT_DRV register value. ADATA[7:0] are updated on the rising edge of REFCLK.
ADP	Tristate Output	N27	The SBI ADD bus parity signal (ADP) carries the even or odd parity for the ADD bus signals. The parity calculation encompasses the ADATA[7:0], APL and AV5 signals. Multiple link layer devices can drive this signal at uniquely assigned tributary column positions. When the FREEDM 84A1024 is not outputting data on a particular tributary column ADP is driven or tri-stated based on the DEFAULT_DRV register value. This parity signal is intended to detect accidental link layer source clashes in the column assignment. ADP is updated on the rising edge of REFCLK.

Pin Name	Type	Pin No.	Function
APL	Tristate Output	N28	The SBI ADD bus payload signal (APL) indicates valid data within the SBI TDM bus structure. This signal is asserted during all octets making up a tributary. This signal may be asserted during the V3 or H3 octet within a tributary to accommodate negative timing adjustments between the tributary rate and the fixed TDM bus structure. This signal may be de-asserted during the octet following the V3 or H3 octet within a tributary to accommodate positive timing adjustments between the tributary rate and the fixed TDM bus structure. Multiple link layer devices can drive this signal at uniquely assigned tributary column positions. When the FREEDM 84A1024 is not outputting data on a particular tributary column APL is driven or tri-stated based on the DEFAULT_DRV register value. APL is updated on the rising edge of REFCLK.
AV5	Tristate output	N30	The SBI ADD bus payload indicator signal (AV5) locates the position of the floating payloads for each tributary within the SBI TDM bus structure. Timing differences between the port timing and the TDM bus timing are indicated by adjustments of this payload indicator relative to the fixed TDM bus structure. Multiple link layer devices can drive this signal at uniquely assigned tributary column positions. When the FREEDM 84A1024 is not outputting data on a particular tributary column AV5 is driven or tri-stated based on the DEFAULT_DRV register value. AV5 is updated on the rising edge of REFCLK.
ADETECT[0] ADETECT[1]	Input	P28 P29	The SBI ADD bus conflict detection signals (ADETECT[1:0]) may be connected to the AACTIVE outputs of other link layer devices sharing the SBI ADD bus. FREEDM 84A1024 will immediately tristate the SBI ADD bus signals ADATA[7:0], ADP, APL and AV5 if either of ADETECT[1] and ADETECT[0] is asserted. ADETECT[1:0] are asynchronous inputs.
AJUST_REQ	Input	N31	The SBI ADD bus justification request signal (AJUST_REQ) is used to speed up or slow down the output data rate of the FREEDM 84A1024. Negative timing adjustments are requested by asserting AJUST_REQ during the V3 or H3 octet of the drop bus depending on the tributary type. In response to this the FREEDM 84A1024 will send an extra byte in the V3 or H3 octet of the next frame on the add bus along with a valid APL indicating a negative justification. Positive timing adjustments are requested by asserting AJUST_REQ during the octet following the V3 or H3 octet of the drop bus, depending on the tributary type. FREEDM 84A1024 will respond to this by not sending an octet during the octet following the V3 or H3 octet of the next frame on the add bus and de-asserting APL to indicate a positive justification. AJUST_REQ is sampled on the rising edge of REFCLK.

Pin Name	Type	Pin No.	Function
AACTIVE	Output	P27	The SBI ADD bus active indicator signal (AACTIVE) is asserted whenever FREEDM 84A1024 is driving the SBI ADD bus signals, ADATA[7:0], ADP, APL and AV5. All other Link Layer devices driving the SBI ADD bus should monitor this signal (to detect multiple sources accidentally driving the bus) and should cease driving the bus whenever a conflict is detected. AACTIVE is updated on the rising edge of REFCLK.

Table 3 Clock/Data Interface signals (12 pins)

Pin Name	Type	Pin No.	Function
RCLK0 RCLK4 RCLK8	Input	AJ25 AH23 AJ21	The receive line clock signals (RCLK[0,4,8]) contain the recovered line clock for the 3 independently timed links. RCLK[n] must be externally gapped during the bits or time-slots that are not part of the transmission format payload (i.e. not part of the HDLC packet). RCLK[0,4,8] is nominally a 50% duty cycle clock between 0 and 52 MHz. The RCLK[n] inputs are invalid and should be tied low when their associated link is not configured for operation.
RD0 RD4 RD8	Input	AK25 AJ23 AK21	The receive data signals (RD[0,4,8]) contain the recovered line data for the 3 independently timed links. RD[0,4,8] contain HDLC packet data. For certain transmission formats, RD[0,4,8] may contain placeholder bits or time-slots. RCLK[n] must be externally gapped during the place holder positions in the RD[n] stream. The FREEDM 84A1024 supports a maximum data rate of 52 Mbps on each link. RD[0,4,8] is sampled on the rising edge of the corresponding RCLK[0,4,8].
TCLK0 TCLK4 TCLK8	Input	B13 C14 D15	The transmit line clock signals (TCLK[0,4,8]) contain the transmit clocks for the 3 independently timed links. TCLK[n] must be externally gapped during the bits or time-slots that are not part of the transmission format payload (i.e. not part of the HDLC packet). TCLK[0,4,8] is nominally a 50% duty cycle clock between 0 and 52 MHz. The TCLK[n] inputs are invalid and should be tied low when their associated link is not configured for operation
TD0 TD4 TD8	Output	A17 B18 A19	The transmit data signals (TD[0,4,8]) contain the transmit data for the 3 independently timed links. TD[0,4,8] contains HDLC packet data. For certain transmission formats, TD[0,4,8] may contain placeholder bits or time-slots. TCLK[n] must be externally gapped during the place holder positions in the TD[n] stream. The FREEDM 84A1024 supports a maximum data rate of 52 Mbps on each link. In normal operation, TD[0,4,8] is updated on the falling edge of the corresponding TCLK[0,4,8] clock. In loopback mode, TD[0,4,8] are updated on the falling edge of the corresponding RCLK[0,4,8] clock.

Table 4 ANY-PHY Packet Interface signals (70 pins)

Note: ANY-PHY Level is s/w programmable.

Pin Name	Type	Pin No.	Function
TXCLK	Input	Y3	The transmit clock signal (TXCLK) provides timing for the transmit ANY-PHY packet interface. **ANY-PHY Level 2 Mode:** TXCLK is a nominally 50% duty cycle, 25 to 52 MHz clock. **ANY-PHY Level 3 Mode:** TXCLK is a nominally 50% duty cycle, 50 to 104 MHz clock
TXADDR[0] TXADDR[1] TXADDR[2] TXADDR[3] TXADDR[4] TXADDR[5] TXADDR[6] TXADDR[7] TXADDR[8] TXADDR[9] TXADDR[10] TXADDR[11] TXADDR[12] TXADDR[13] TXADDR[14] TXADDR[15]	Input	V5 V4 V3 V2 V1 U5 U4 U3 U2 U1 R1 R2 R5 P1 P2 P3	The transmit address signals (TXADDR[15:0]) provide a channel address for polling a transmit ANY-PHY channel FIFO. The FREEDM 84A1024 compares the TXADDR[15:0] to the base and range registers to determine if the ANY-PHY channel being polled resides within the FREEDM 84A1024 . An ANY-PHY channel with an address that is greater than or equal to the base register and less than or equal to the maximum address as defined by the range plus channel base address resides within the FREEDM 84A1024 . The TXADDR[15:0] signals are sampled on the rising edge of TXCLK.
TPA	Tristate Output	P4	The transmit packet available (TPA) signal reflects the status of a poll of a transmit ANY-PHY channel FIFO. TPA returns the polled results for ANY-PHY channel address ‘n’ provided on TXADDR[15:0]. TPA is coded as follows: TPA = “1” => Space to accept a 9600 byte packet TPA = “0” => No Space to accept a 9600 byte packet It is the responsibility of the external controller to prevent ANY-PHY channel underflow or overflow conditions by adequately polling each channel before data transfer. TPA is updated on the rising edge of TXCLK. TPA is tristate during reset. Once a packet has started to be transferred, TPA will reflect the ability to accept another complete packet. **ANY-PHY Level 2 Mode:** TPA is tristate when an ANY-PHY channel address other than ANY-PHY channels residing in the FREEDM is provided on TXADDR[15:0]. An ANY-PHY channel with an address that is less than the channel base address register or outside the range address register within the FREEDM 84A1024 is identified as an ANY-PHY channel that does not reside within the FREEDM 84A1024 . TPA is tristate when an unprovisioned channel is polled. It is recommended that TPA be connected externally to a weak pull-down, e.g. 470Ω.

Pin Name	Type	Pin No.	Function
cont'd			**ANY-PHY Level 3 Mode:** TPA returns the value "0" when an ANY-PHY channel address other than ANY-PHY channels residing in the FREEDM is provided on TXADDR[15:0]. The TPA poll response is invalid if it corresponds to a TXADDR poll coincident with the start of a segment transfer (ie on the cycle in which TSX is driven high). TPA is 0 when an unprovisioned channel is polled.
TXDATA[0] TXDATA[1] TXDATA[2] TXDATA[3] TXDATA[4] TXDATA[5] TXDATA[6] TXDATA[7] TXDATA[8] TXDATA[9] TXDATA[10] TXDATA[11] TXDATA[12] TXDATA[13] TXDATA[14] TXDATA[15]	Input	P5 N1 N2 N3 N5 M1 M2 M3 M4 M5 L2 L3 L4 K1 K2 K3	**ANY-PHY Level 2 Mode** The transmit data signals (TXDATA[15:0]) contain the transmit ANY-PHY packet interface (APPI) data provided by the external controller. Data must be presented in big endian order, i.e. the byte in TXDATA[15:8] is transmitted by the FREEDM 84A1024 before the byte in TXDATA[7:0]. The first word of each data transfer contains an address to identify the device and ANY-PHY channel associated with the data being transferred. This prepended address must be qualified with the TSX signal. The FREEDM 84A1024 compares the first two bytes to the base and range registers to determine if the ANY-PHY channel resides within the FREEDM 84A1024 .The FREEDM 84A1024 will not respond to ANY-PHY channel addresses outside the high and low address registers stored in the TAPI-12 base and range address registers. The second and any subsequent words of each data transfer contain packet data. The TXDATA[15:0] signals are sampled on the rising edge of TXCLK.
Cont'd			**ANY-PHY Level 3 Mode:** The transmit data signals (TXDATA[7:0]) contain the transmit ANY-PHY packet interface (APPI) data provided by the external controller. The first two bytes of each data transfer contains an address to identify the device and ANY-PHY channel associated with the data being transferred. The first byte of this prepended address must be qualified with the TSX signal. The FREEDM 84A1024 compares the first two bytes to the TAPI-12 base and range registers to determine if the ANY-PHY channel resides within the FREEDM 84A1024 .The FREEDM 84A1024 will not respond to ANY-PHY channel addresses outside the base and range registers. The third and any subsequent bytes of each data transfer contain packet data. The TXDATA[7:0] signals are sampled on the rising edge of TXCLK. TXDATA[15:8] are not used by FREEDM 84A1024 when operating in ANY-PHY Level 3 mode and should be tied low.

Pin Name	Type	Pin No.	Function
TXPRTY	Input	K4	**ANY-PHY Level 2 Mode:** The transmit parity signal (TXPRTY) reflects the odd parity calculated over the TXDATA[15:0] signals (regardless of TMOD state). TXPRTY is only valid when TXDATA[15:0] are valid. **ANY-PHY Level 3 Mode:** The transmit parity signal (TXPRTY) reflects the odd parity calculated over the TXDATA[7:0] signals. TXPRTY is only valid when TXDATA[7:0] are valid. Regardless of mode of operation TXPRTY is sampled on the rising edge of TXCLK.

Pin Name	Type	Pin No.	Function
TRDY	Tristate Output	J1	The transmit ready signal (TRDY) indicates the ability of the transmit ANY-PHY packet interface (APPI) to accept data. When TRDY is set low, the transmit APPI is unable to accept further data. When TRDY is set high, data provided on the transmit APPI will be accepted by the FREEDM 84A1024 device If TRDY is driven low, the external controller must hold the data on TXDATA until TRDY is driven high. TRDY may be driven low for 0 or more TXCLK cycles before it is driven high. TRDY is considered valid from two cycles after the start of transfer until the cycle in which it is asserted high (it can only backpressure once at the start of transfer). A new transfer can not be initiated earlier than one clock after TRDY is sampled high. TRDY is tristate during reset. TRDY is updated on the rising edge of TXCLK. **ANY-PHY Level 2 Mode** TRDY is valid one TXCLK cycle after TSX is sampled high. TRDY is asserted by the FREEDM 84A1024 device, which was selected by the in-band ANY-PHY channel address on TXDATA[15:0]. TRDY will only be driven high for one clock cycle, it is always driven tristate one TXCLK cycle after it is driven high. It is recommended that TRDY be connected externally to a weak pull-up, e.g. 10 kΩ. **ANY-PHY Level 3 Mode** TRDY is valid one TXCLK cycle after TSX is sampled high and remains valid up to and including the cycle in which it is driven high.

Pin Name	Type	Pin No.	Function
TSX	Input	K5	The transmit start of transfer signal (TSX) denotes the start of data transfer on the transmit APPI. The TSX signal is sampled on the rising edge of TXCLK. **ANY-PHY Level 2 Mode** When the TSX signal is sampled high, the sampled word on the TXDATA[15:0] signals contain the ANY-PHY channel address associated with the data to follow. When the TSX signal is sampled low, the sampled word on the TXDATA[15:0] signals does not contain an ANY-PHY channel address. **ANY-PHY Level 3 Mode:** When the TSX signal is sampled high, the sampled byte on the TXDATA[7:0] signals contain the most significant byte of the ANY-PHY channel address associated with the data to follow. When the TSX signal is sampled low, the sampled word on the TXDATA[7:0] signals does not contain the first byte of the ANY-PHY channel address.
TEOP	Input	J2	The transmit end of packet signal (TEOP) denotes the end of a packet. TEOP is only valid during data transfer. TEOP is sampled on the rising edge of TXCLK. **ANY-PHY Level 2 Mode** When TEOP is sampled high, the data on TXDATA[15:0] is the last word of a packet (fragment). When TEOP is sampled low, the data on TXDATA[15:0] is not the last word of a packet (fragment). **ANY-PHY Level 3 Mode:** When TEOP is sampled high, the data on TXDATA[7:0] is the last byte of a packet (fragment). When TEOP is sampled low, the data on TXDATA[7:0] is not the last byte of a packet (fragment).
TMOD	Input	J3	**ANY-PHY Level 2 Mode** The transmit word modulo signal (TMOD) indicates the size of the current word on TXDATA[15:0]. TMOD is only valid when TEOP is sampled high. When TMOD is sampled high and TEOP is sampled high, only the TXDATA[15:8] signals contain valid data and the TXDATA[7:0] signals are invalid. When TMOD is sampled low and TEOP is sampled high, the complete word on TXDATA[15:0] contains valid data. TMOD must be set low when TEOP is set low. TMOD is sampled on the rising edge of TXCLK. **ANY-PHY Level 3 Mode:** TMOD is not used. The last valid byte of data on TXDATA[7:0] is sampled when TEOP is sampled high.

Pin Name	Type	Pin No.	Function
TERR	Input	J4	The transmit error signal (TERR) indicates that the current packet is erred and should be aborted. TERR is only valid when TEOP is sampled high. When TERR is sampled high and TEOP is sampled high, the current packet is erred and the FREEDM 84A1024 will respond accordingly. When TERR is sampled low and TEOP is sampled high, the current packet is not erred. TERR must be set low when TEOP is set low. TERR is sampled on the rising edge of TXCLK.
RXCLK	Input	AE5	The receive clock signal (RXCLK) provides timing for the receive ANY-PHY packet interface (APPI). **ANY-PHY Level 2 Mode** RXCLK is a nominally 50% duty cycle, 25 to 52 MHz clock. **ANY-PHY Level 3 Mode:** RXCLK is a nominally 50% duty cycle, 50 to 104 MHz clock.
RXADDR[0] RXADDR[1] RXADDR[2] RXADDR[3]	Input	AF2 AE4 AE3 AE2	**ANY-PHY Level 2 Mode**: The receive address signals (RXADDR[3:0]) serve two functions – device polling and device selection. When polling, the RXADDR[3:0] signals provide an address for polling a FREEDM 84A1024 device for receive data available in any one of its 1024 ANY-PHY channels. Polling results are returned on the RPA tristate output. During selection, the address on the RXADDR[3:0] signals is qualified with the RENB signal to select a FREEDM 84A1024 device enabling it to output data on the receive APPI. Note that up to fifteen FREEDM 84A1024 devices may share a single external controller (one address is reserved as a null address). The Rx APPI of each FREEDM 84A1024 device is identified by the device base address in the RAPI-12 Base Address register. The RXADDR[3:0] signals are sampled on the rising edge of RXCLK. **ANY-PHY Level 3 Mode:** RXADDR is not used as the interface is point-to-point.

Pin Name	Type	Pin No.	Function
RPA	Tristate Output	AE1	The receive packet/fragment available signal (RPA) reflects the status of a poll on the receive APPI of a FREEDM 84A1024 device. RPA is tristate during reset and when a device address other than the FREEDM 84A1024 's device base address is provided on RXADDR[3:0]. An FREEDM 84A1024 device must not be selected for receive data transfer unless it has been polled and responded that it has data ready to transfer. When the RXADDR[3:0] inputs match the device base address in the RAPI-12 Base Address register, that FREEDM 84A1024 device drives RPA one RXCLK cycle after sampling RXADDR[3:0]. RPA is updated on the rising edge of RXCLK. **ANY-PHY Level 2 Packet Mode:** When RPA is set high, the polled FREEDM 84A1024 still has sufficient data to undertake another ANY-PHY transfer. When RPA is set low, the polled FREEDM 84A1024 device does not have data ready to transfer. **ANY-PHY Level 3 Mode:** RPA is not used and is tri-stated.
RENB	Input	AD4	The receive enable signal (RENB) is used to throttle the FREEDM 84A1024 . RENB is sampled on the rising edge of RXCLK. To commence data transfer, RENB must be sampled low. **ANY-PHY Level 2 Mode:** The receive enable signal (RENB) qualifies the RXADDR[3:0] signals for selection of a FREEDM 84A1024 device. When RENB is sampled high and then low in consecutive RXCLK cycles, the address on RXADDR[3:0] during the cycle when RENB is sampled high selects a FREEDM 84A1024 device enabling it to output data on the receive APPI. The Rx APPI of each FREEDM 84A1024 device is identified by the device base address in the RAPI-12 Base Address register. RENB may also be used to throttle the FREEDM 84A1024 during data transfer on the Rx APPI. When the FREEDM 84A1024 samples RENB high during data transfer, the FREEDM 84A1024 will pause the data transfer and tri-state the receive APPI outputs (except RPA) until RENB is returned low. Since the ANY-PHY bus specification does not support deselecting during data transfers, the address on the RXADDR[3:0] inputs during the cycle before RENB is returned low must either re-select the same FREEDM 84A1024 device or be a null address. The polling function of the RXADDR[3:0] and RPA signals operates regardless of the state of RENB.

Pin Name	Type	Pin No.	Function
Cont'd			It is the responsibility of the external controller to prevent overflow by providing each FREEDM 84A1024 device on an ANY-PHY point to multi-point bus sufficient bandwidth through selection. **ANY-PHY Level 3 Mode:** RENB is used to throttle the FREEDM 84A1024 during data transfer on Rx APPI. When the FREEDM 84A1024 samples RENB high during data transfer, the FREEDM 84A1024 will pause the data transfer until RENB is returned low.
RXDATA[0] RXDATA[1] RXDATA[2] RXDATA[3] RXDATA[4] RXDATA[5] RXDATA[6] RXDATA[7] RXDATA[8] RXDATA[9] RXDATA[10] RXDATA[11] RXDATA[12] RXDATA[13] RXDATA[14] RXDATA[15]	Tristate Output	AD3 AD2 AC5 AD1 AC4 AC2 AB5 AC1 AB4 AB3 AB2 AB1 AA4 AA3 AA2 Y5	**ANY-PHY Level 2 Mode** The receive data signals (RXDATA[15:0]) contain the receive ANY-PHY packet interface (APPI) data output by the FREEDM 84A1024 when selected. Data is presented in big endian format; i.e. the byte in RXDATA[15:8] was received by the FREEDM 84A1024 before the byte in RXDATA[7:0]. The first word of each data transfer (when RSX is high) contains an address to identify the device and ANY-PHY channel associated with the data being transferred. The second and any subsequent words of each data transfer contain valid data. The FREEDM 84A1024 may be programmed to overwrite RXDATA[7:0] of the final word of each packet transfer (REOP is high) with the status of packet reception when that packet is erred (RERR is high). This status information is encoded as follows: RXDATA[7:0] Error 01H Channel FIFO Overrun 02H Packet Length violation 04H FCS Error 08H Non-Octet Aligned 10H HDLC Packet Abort 81H Unexpected Presence of SN 82H Unsupported Header Format 84H Lost Datagram 88H Unexpected SN 90H Excessive Number of Fragments Note1: Excessive Number of Fragments only applies when the output format is frame/packet out (not fragment out). The RXDATA[15:0] signals are tristated when the FREEDM 84A1024 device is not selected via the RENB signal.

Pin Name	Type	Pin No.	Function
Cont'd			The RXDATA[15:0] signals are updated on the rising edge of RXCLK. **ANY-PHY Level 3 Mode:** The receive data signals (RXDATA[7:0]) contain the receive ANY-PHY packet interface (APPI) data output by the FREEDM 84A1024 when selected. The first and second bytes of each data transfer contains an address to identify the device and channel associated with the data being transferred. The third and any subsequent bytes of each data transfer contain valid data. The FREEDM 84A1024 may be programmed to overwrite RXDATA[7:0] of the final word of each packet transfer (REOP is high) with the status of packet reception when that packet is erred (RERR is high). This status information is encoded as for the ANY-PHY Level 2 Mode (above). The RXDATA[15:8] signals are tristated when the FREEDM 84A1024 device operating in 8 bit mode. The RXDATA[7:0] signals are driven but not considered valid when the RENB signal is high. The RXDATA[7:0] signals are updated on the rising edge of RXCLK.
RXPRTY	Tristate Output	Y4	**ANY-PHY Level 2 Mode** The receive parity signal (RXPRTY) reflects the odd parity calculated over the RXDATA[15:0] signals (regardless of RMOD state). RXPRTY is driven/tristated at the same time as RXDATA[15:0]. **ANY-PHY Level 3 Mode:** The receive parity signal (RXPRTY) reflects the odd parity calculated over the RXDATA[7:0] signals. RXPRTY is valid when RXDATA[7:0] is valid. Regardless of mode, RXPRTY is updated on the rising edge of RXCLK.

Pin Name	Type	Pin No.	Function
RSX	Tristate Output	Y2	The receive start of transfer signal (RSX) denotes the start of data transfer on the receive APPI. RSX is updated on the rising edge of RXCLK. **ANY-PHY Level 2 Mode** When the RSX signal is set high, the data on the RXDATA[15:0] signals contains the address that identifies the device and channel associated with the data to follow. When the RSX signal is sampled low, the word on the RXDATA[15:0] signals does not contain a channel address. RSX is tristated when the FREEDM 84A1024 device is not selected via the RENB signal. RSX is updated on the rising edge of RXCLK. It is recommended that RSX be connected externally to a weak pull-down, e.g. 10 kΩ. **ANY-PHY Level 3 Mode** When the RSX signal is set high, the data on the RXDATA[7:0] signals contains the most significant byte of the address that identifies the device and channel associated with the data to follow. When the RSX signal is sampled low, the byte on the RXDATA[7:0] signals does not contain the first byte of the channel address.
RSOP	Tristate Output	Y1	Receive Start of Packet. Marks the cycle containing the start of the packet. The FREEDM 84A1024 drives RSOP high at the start of a packet in a transfer period and holds RSOP low afterwards. RSOP is used when supporting both ANY-PHY Level 2 and 3 operating modes. **ANY-PHY Level 2 Mode:** RSOP is driven high one clock cycle after the RSX is driven high. RSOP is tri-stated after the last word of the packet is sent. **ANY-PHY Level 3 Mode:** RSOP is driven high two clock cycles after the RSX is driven high. RSOP is tri-stated after the last byte of the packet is sent.

Pin Name	Type	Pin No.	Function
REOP	Tristate Output	W5	The receive end of packet signal (REOP) denotes the end of a packet. REOP is only valid during data transfer. REOP is updated on the rising edge of RXCLK. **ANY-PHY Level 2 Mode:** When REOP is set high, RXDATA[15:0] contains the last data byte of a packet. When REOP is set low, RXDATA[15:0] does not contain the last data byte of a packet. REOP is tristated when the FREEDM 84A1024 device is not selected via the RENB signal. **ANY-PHY Level 3 Mode:** When REOP is set high, RXDATA[7:0] contains the last data byte of a packet. When REOP is set low, RXDATA[7:0] does not contain the last data byte of a packet.
RMOD	Tristate Output	W4	**ANY-PHY Level 2 Mode:** The receive word modulo signal (RMOD) indicates the size of the current word on RXDATA[15:0]. When RXDATA[15:0] does not contain the last byte of a packet (REOP set low), RMOD is set low. When RMOD is set high and REOP is set high, RXDATA[15:8] contains the last data byte of a packet. When RMOD is set low and REOP is set high, RXDATA[7:0] contains the last byte of the packet, or optionally, the error status byte. The behavior of RMOD relates only to packet data and is unaffected when the FREEDM 84A1024 device is programmed to overwrite RXDATA[7:0] with status information when erred packets are received. RMOD is tristated when the FREEDM 84A1024 device is not selected via the RENB signal. RMOD is updated on the rising edge of RXCLK. **ANY-PHY Level 3 Mode:** RMOD is not used. The last valid byte of data on RXDATA[7:0] is sampled when REOP is sampled high. RMOD is tristated when the FREEDM 84A1024 is operating in ANY-PHY level 3 mode.

Pin Name	Type	Pin No.	Function
RERR	Tristate Output	W1	The receive error signal (RERR) indicates that the current packet is erred and should be discarded. RERR is updated on the rising edge of RXCLK. The receive error signal (RERR) indicates that the current packet is erred and should be discarded. When RXDATA[15:0] (ANY-PHY Level 2 mode) or RXDATA[7:0] (ANY-PHY Level 3 mode) does not contain the last byte of a packet (REOP set low), RERR is set low. When RERR is set high and REOP is set high, the current packet is erred. When RERR is set low and REOP is set high, the current packet is not erred. The FREEDM 84A1024 may be programmed to overwrite RXDATA[7:0] of the final word of each packet transfer (REOP set high) with the status of packet reception when that packet is erred (RERR is high). **ANY-PHY Level 2 Mode:** RERR is tristated when the FREEDM 84A1024 device is not selected via the RENB signal. **ANY-PHY Level 3 Mode:** RERR is driven low when the FREEDM 84A1024 device is not selected via the RENB signal.
RVAL	Tristate Output	W2	The receive data valid (RVAL) is asserted when packet data is being output on RXDATA. It is de-asserted whenever the FREEDM 84A1024 device is selected, but not outputting packet data on RXDATA[15:0]. (E.g., when RSX is high and address prepend is being output on RXDATA, RVAL is de-asserted.) RVAL is updated on the rising edge of RXCLK. **ANY-PHY Level 2 Mode:** RVAL is tristated when the FREEDM 84A1024 device is not selected via the RENB signal. **ANY-PHY Level 3 Mode:** RVAL is driven low when the FREEDM 84A1024 device is not selected via the RENB signal.

Table 5 Re-Sequencing SDRAM Interface (52 Signals)

Pin Name	Type	Pin No.	Function
RSCSB	Output	AB31	Re-Sequencing SDRAM Chip Select Bar. RSCSB, RSRASB, RSCASB, and RSWEB define the command being sent to the SDRAM. RSCSB is updated on the rising edge of SYSCLK.
RSRASB	Output	AB30	Re-Sequencing SDRAM Row Address Strobe Bar. RSCSB, RSRASB, RSCASB, and RSWEB define the command being sent to the SDRAM. RSRASB is updated on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
RSCASB	Output	AB29	Re-Sequencing SDRAM Column Address Strobe Bar. RSCSB, RSRASB, RSCASB, and RSWEB define the command being sent to the SDRAM. RSCASB is updated on the rising edge of SYSCLK.
RSWEB	Output	AA28	Re-Sequencing SDRAM Write Enable Bar. RSCSB, RSRASB, RSCASB, and RSWEB define the command being sent to the SDRAM. RSWEB is updated on the rising edge of SYSCLK.
RSADD[0] RSADD[1] RSADD[2] RSADD[3] RSADD[4] RSADD[5] RSADD[6] RSADD[7] RSADD[8] RSADD[9] RSADD[10] RSADD[11] RSADD[12]	Output	V28 V27 W31 W30 W29 W27 Y31 Y30 Y29 Y28 Y27 AA30 AA29	Re-Sequencing SDRAM Address. The Re-Sequencing SDRAM address outputs identify the row address (RSADD[12:0]) and column address (RSADD[8:0]) for the locations accessed. RSADD[12:0] is updated on the rising edge of SYSCLK.
RSBS[0] RSBS[1]	Output	AB28 AC31	Re-Sequencing SDRAM Bank Select. The bank select signal determines which bank of a dual/quad bank Re-Sequencing SDRAM chip is active. RSBS[1:0] is generated along with the row address when RSRASB is asserted low. RSBS is updated on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
RSDAT[0] RSDAT[1] RSDAT[2] RSDAT[3] RSDAT[4] RSDAT[5] RSDAT[6] RSDAT[7] RSDAT[8] RSDAT[9] RSDAT[10] RSDAT[11] RSDAT[12] RSDAT[13] RSDAT[14] RSDAT[15] RSDAT[16] RSDAT[17] RSDAT[18] RSDAT[19] RSDAT[20] RSDAT[21] RSDAT[22] RSDAT[23] RSDAT[24] RSDAT[25] RSDAT[26] RSDAT[27] RSDAT[28] RSDAT[29] RSDAT[30] RSDAT[31]	I/O	AB27 AC30 AC29 AC28 AD31 AC27 AD28 AE31 AD27 AE29 AE28 AF30 AE27 AF29 AG31 AF28 AG30 AF27 AG29 AH30 AG28 AH27 AK28 AJ27 AG26 AK27 AH26 AL27 AJ26 AG25 AK26 AH25	Re-Sequencing SDRAM Data. The bi-directional Re-Sequencing SDRAM data bus pins interface directly with the Re-Sequencing SDRAM data ports. RSDAT[31:0] is updated/tristated on the rising edge of SYSCLK.
DQM	Output	AC3	Drives DQMH and DQML inputs of all SDRAMs. During the SDRAM initialization sequence this signal is set “high”. Otherwise it is “low” at all times as the DRAM Controllers do not utilize the “masking” functionality of the memories. DQM is updated on the rising edge of SYSCLK.

Table 6 Context Memory Synchronous SSRAM Interface (57 Signals)

Pin Name	Type	Pin No.	Function
CCDAT[0] CCDAT[1] CCDAT[2] CCDAT[3] CCDAT[4] CCDAT[5] CCDAT[6] CCDAT[7] CCDAT[8] CCDAT[9] CCDAT[10] CCDAT[11] CCDAT[12] CCDAT[13] CCDAT[14] CCDAT[15] CCDAT[16] CCDAT[17] CCDAT[18] CCDAT[19] CCDAT[20] CCDAT[21] CCDAT[22] CCDAT[23] CCDAT[24] CCDAT[25] CCDAT[26] CCDAT[27] CCDAT[28] CCDAT[29] CCDAT[30] CCDAT[31] CCDAT[32] CCDAT[33] CCDAT[34] CCDAT[35]	I/O	A20 B20 C20 D20 E20 B21 C21 D21 A22 B22 C22 D22 A23 E22 B23 C23 D23 A24 E23 D24 A25 E24 C25 D25 B26 E25 C26 A27 D26 B27 E26 C27 B28 D27 E28 D30	Context Memory SSRAM Data. The bi-directional SSRAM data bus pins interface directly with the synchronous SSRAM data ports. The FREEDM 84A1024 presents valid data on the CCDAT[35:0] pins upon the rising edge of SYSCLK during write cycles. CCDAT [35:0] is tristated on the rising edge of SYSCLK for read cycles. CCDAT [35:0] is sampled/updated/tristated on the rising edge of SYSCLK.
CCADD[0] CCADD[1] CCADD[2] CCADD[3] CCADD[4] CCADD[5] CCADD[6] CCADD[7] CCADD[8] CCADD[9] CCADD[10] CCADD[11] CCADD[12] CCADD[13] CCADD[14] CCADD[15] CCADD[16] CCADD[17]	Output	J31 K27 J28 H31 J27 H30 H29 H28 G31 G30 G29 G28 F30 G27 F29 E31 F28 E30	Context Memory SSRAM Address. The SSRAM address outputs identify the SSRAM locations accessed. CCADD[17:0] is updated on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
CCWEB	Output	F27	Context Memory SSRAM Write Bar. CCWEB determines the cycle type when CCSELB is asserted low. When CCWEB is asserted high, the cycle type is a read. When CCWEB is asserted low, the cycle type is a write. CCWEB is updated on the rising edge of SYSCLK.
CCSELB	Output	E29	Context Memory SSRAM Chip Enable Bar. CCSELB initiates an access. When CCSELB is asserted low, the external SSRAM samples the address and CCWEB asserted by the FREEDM 84A1024. CCSELB is updated on the rising edge of SYSCLK.
CCBSELB	Output	K29	SSRAM Bank Select This active low output is provided to enable glueless connection to 4 banks of Standard/ZBT SSRAM: CCBSELB is the inverse of CCADD[16]. CCBSELB and CCADD[16:17] are used to select 4 banks when 64x36 devices are used.

Table 7 Chunk Buffer SDRAM Interface (67 Signals)

Pin Name	Type	Pin No.	Function
CBCSB	Output	AF5	Chunk Buffer SDRAM Chip Select Bar. CBCSB, CBRASB, CBCASB, and CBWEB define the command being sent to the SDRAM. CBCSB is updated on the rising edge of SYSCLK.
CBRASB	Output	AG2	Chunk Buffer SDRAM Row Address Strobe Bar. CBCSB, CBRASB, CBCASB, and CBWEB define the command being sent to the SDRAM. CBRASB is updated on the rising edge of SYSCLK.
CBCASB	Output	AF4	Chunk Buffer SDRAM Column Address Strobe Bar. CBCSB, CBRASB, CBCASB, and CBWEB define the command being sent to the SDRAM. CBCASB is updated on the rising edge of SYSCLK.
CBWEB	Output	AG3	Chunk Buffer SDRAM Write Enable Bar. CBCSB, CBRASB, CBCASB, and CBWEB define the command being sent to the SDRAM. CBWEB is updated on the rising edge of SYSCLK.
CBADD[0] CBADD[1] CBADD[2] CBADD[3] CBADD[4] CBADD[5] CBADD[6] CBADD[7] CBADD[8] CBADD[9] CBADD[10] CBADD[11] CBADD[12]	Output	AH7 AK6 AG7 AJ6 AL5 AH6 AK5 AG6 AJ5 AK4 AH5 AG4 AH2	Chunk Buffer SDRAM Address. The Chunk Buffer SDRAM address outputs identify the row address (CBADD12:0]) and column address (CBADD[8:0]) for the locations accessed. CBADD[12:0] is updated on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
CBBS[0] CBBS[1]	Output	AG1 AF3	Chunk Buffer SDRAM Bank Select. The bank select signal determines which bank of a dual/quad bank Chunk Buffer SDRAM chip is active. CBBS[1:0] is generated along with the row address when CBRASB is asserted low. CBBS[1:0] is updated on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
CBDAT[0] CBDAT[1 CBDAT[2] CBDAT[3] CBDAT[4] CBDAT[5] CBDAT[6] CBDAT[7] CBDAT[8] CBDAT[9] CBDAT[10] CBDAT[11] CBDAT[12] CBDAT[13] CBDAT[14] CBDAT[15] CBDAT[16] CBDAT[17] CBDAT[18] CBDAT[19] CBDAT[20] CBDAT[21] CBDAT[22] CBDAT[23] CBDAT[24] CBDAT[25] CBDAT[26] CBDAT[27] CBDAT[28] CBDAT[29] CBDAT[30] CBDAT[31] CBDAT[32] CBDAT[33] CBDAT[34] CBDAT[35] CBDAT[36] CBDAT[37] CBDAT[38] CBDAT[39] CBDAT[40] CBDAT[41] CBDAT[42] CBDAT[43] CBDAT[44] CBDAT[45] CBDAT[46] CBDAT[47]	I/O	AH19 AK19 AL19 AG18 AH18 AJ18 AK18 AL18 AG17 AH17 AJ17 AK17 AL17 AL15 AK15 AG15 AL14 AK14 AJ14 AH14 AG14 AL13 AK13 AJ13 AG13 AL12 AK12 AJ12 AH12 AG12 AK11 AJ11 AH11 AL10 AK10 AJ10 AH10 AL9 AG10 AK9 AJ9 AH9 AL8 AG9 AH8 AL7 AG8 AJ7	Chunk Buffer SDRAM Data. The bi-directional Chunk Buffer SDRAM data bus pins interface directly with the Chunk Buffer SDRAM data ports. CBDAT[47:0] is updated/tristated on the rising edge of SYSCLK.

Table 8 Microprocessor Interface Signals (44)

Pin Name	Type	Pin No.	Function
BCLK	Input	G5	Bus Clock. This clock is the bus clock for the microprocessor interface. BCLK must cycle at 33-66 MHz instantaneous rate.
AD[0] AD[1] AD[2] AD[3] AD[4] AD[5] AD[6] AD[7] AD[8] AD[9] AD[10] AD[11] AD[12] AD[13] AD[14] AD[15] AD[16] AD[17] AD[18] AD[19] AD[20] AD[21] AD[22] AD[23] AD[24] AD[25] AD[26] AD[27] AD[28] AD[29] AD[30] AD[31]	I/O	F3 E1 F4 E2 F5 E3 D2 E4 D5 B4 C5 E6 B5 D6 A5 C6 E7 B6 D7 C7 B7 A7 D8 C8 B8 E9 A8 D9 E10 A9 D10 C10	Multiplexed Address Data Bus. The multiplexed address data bi-directional bus AD[31:0] is used to connect the FREEDM 84A1024 to the microprocessor. During the address phase when ADSB = 0, AD[1:0] are ignored as all transfers are 32 bits wide. AD[31:0] is sampled/updated/tristated on the rising edge of BCLK.
ADSB	Input	B10	Address Status. This signal is active-low and indicates a long-word address is present on the address/data bus AD[31:2]. ADSB is sampled on the rising edge of BCLK.
CSB	Input	A10	Active Low Chip Select. The chip select (CSB) signal is low during the address cycle (as defined by ADSB) FREEDM 84A1024 register accesses. CSB is sampled on the rising edge of BCLK.
WR	Input	D11	Write/Read. The write/read (WR) signal is evaluated when the ADSB and CSB are sampled active by FREEDM 84A1024. The BUSPOL input pin controls the polarity of this input. WR is sampled on the rising edge of BCLK.

Pin Name	Type	Pin No.	Function
BURSTB	Input	C11	Burst Bar. This signal is evaluated when the ADSB and CSB are sample active by FREEDM 84A1024. When low, this signal indicates that the current access is a burst access (and the BLAST input can be used to detect the end of the transaction). BURSTB is sampled on the rising edge of BCLK.
BLAST	Input	B11	Burst Last. This signal indicates the last data access of the transfer. When the BURSTB input is low, the BLAST input is driven active during the last transfer of a transaction (even if the transaction is one word in length). When the BURSTB input is high, the BLAST input is ignored by FREEDM 84A1024. The BUSPOL input pin controls the polarity of this input. BLAST is sampled on the rising edge of BCLK.
READYB	Tri-state Output	E12	Ready Bar. This active low signal indicates that data on the AD[31:0] bus has been accepted (for writes), or data on the AD[31:0] is valid (for reads). This signal may be used by FREEDM 84A1024 to delay a data transaction. This output is tristated one clock cycle after an FREEDM 84A1024 access, allowing multiple slave devices to be tied together in the system. This output should be pulled up externally. READYB is updated on the rising edge of BCLK.
BTERMB	Tri-state Output	D12	Burst Terminate Bar. This signal is asserted low by FREEDM 84A1024 when a data transfer has reached the address boundary of a burstable range. The maximum burst range supported is 4. Attempts to extend the burst transfer after this signal is asserted will be ignored. This output is tristated one clock cycle after an FREEDM 84A1024access, allowing multiple slave devices to be tied together in the system. This output should be pulled up externally. BTERMB is updated on the rising edge of BCLK.
WRDONEB	Output	C12	Write Done Bar. This signal is asserted low by FREEDM 84A1024when the most recent write access to internal registers is complete. This signal may be used by external circuitry to delay the issuance of a write operation address cycle until FREEDM 84A1024can accept write data. This signal is only needed in systems where the READYB output cannot be used to delay a write data transaction (due to microprocessor restrictions). WRDONEB is updated on the rising edge of BCLK.
INTHIB	OD	B12	Active Low Open-Drain High Priority Interrupt. This signal goes low when a FREEDM 84A1024 high priority interrupt source is active and that source is unmasked. The FREEDM 84A1024may be enabled to report many alarms or events via interrupts. INTHIB becomes high impedance when the interrupt is acknowledged via an appropriate register access. INTHIB is an asynchronous signal.

Pin Name	Type	Pin No.	Function
INTLOB	OD	A12	Active Low Open-Drain Low Priority Interrupt. This signal goes low when a FREEDM 84A1024 low priority interrupt source is active and that source is unmasked. The FREEDM 84A1024may be enabled to report many alarms or events via interrupts. INTLOB becomes high impedance when the interrupt is acknowledged via an appropriate register access. INTLOB is an asynchronous signal.
BUSPOL	Input	E13	Bus Control Polarity. This signal indicates the polarity of the WR and BLAST inputs to FREEDM 84A1024. When high, the BLAST pin is active high (high indicates the last word of the burst) and the WR pin is active low (low indicates write). When low, the BLAST pin is active low (low indicates the last word of the burst) and the WR pin is active high (high indicates write). BUSPOL is sampled on the rising edge of BCLK.

Table 9 Miscellaneous Interface Signals (10 pins)

Pin Name	Type	Pin No.	Function
SYSCLK	Input	H1	The system clock (SYSCLK) provides timing for the core logic. SYSCLK is nominally a 50% duty cycle clock of frequency 100 MHz ±50ppm.
RSTB	Input	H3	The active low reset signal (RSTB) signal provides an asynchronous FREEDM 84A1024 reset. RSTB is an asynchronous input. When RSTB is set low, all FREEDM 84A1024 registers are forced to their default states. This signal must be held low for a minimum of 320ns. In addition, all SBI, APPI and µP interface output pins are forced tristate and will remain tristated until RSTB is set high. RSTB must be asserted until the SDRAMs are out of reset.
PMCTEST	Input	H4	The PMC production test enable signal (PMCTEST) places the FREEDM 84A1024 in scan mode. PMCTEST must be tied low for normal operation (and during BIST).
DLLTEST	Input	H2	The DLL test enable signal (DLLTEST) places the DLL in scan mode. DLLTEST must be tied low for normal operation (and during BIST).
SCAN_EN	Input	D13	The PMC Production SCAN_EN signal is used during scan mode. It must be tied low for normal operation.
TCK	Input	G3	The test clock signal (TCK) provides timing for test operations that can be carried out using the IEEE P1149.1 test access port. TMS and TDI are sampled on the rising edge of TCK. TDO is updated on the falling edge of TCK.
TMS	Input	G4	The test mode select signal (TMS) controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.

Pin Name	Type	Pin No.	Function
TDI	Input	H5	The test data input signal (TDI) carries test data into the FREEDM 84A1024 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Tristate Output	G1	The test data output signal (TDO) carries test data out of the FREEDM 84A1024 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tristate output, which is inactive except when scanning of data is in progress.
TRSTB	Input	F2	The active low test reset signal (TRSTB) provides an asynchronous FREEDM 84A1024 test access port reset via the IEEE P1149.1 test access port. TRSTB is an asynchronous input with an integral pull up resistor. Note that when TRSTB is not being used, it must be connected to the RSTB input.

Table 10 Power and Ground Signals

Pin Name	Type	Pin No.	Function
VDD3V3	Power	A1 A31 B2 B30 C3 C4 C16 C28 C29 D3 D4 D16 D28 D29 E5 E11 E16 E21 E27 L5 L27 T3 T4 T5 T27 T28 T29 AA5 AA27 AG5 AG11 AG16 AG21 AG27 AH3 AH4 AH16 AH28 AH29 AJ3 AJ4 AJ16 AJ28 AJ29 AK2 AK30 AL1 AL31	The VDD3V3 pins should be connected to a well decoupled +3.3 V DC supply. These power pins provide DC current to the I/O pads

Pin Name	Type	Pin No.	Function
VDD1V8	Power	B25 C13 D17 D19 E8 G2 H27 N29 N4 R4 W3 W28 AD5 AE30 AG24 AH13 AJ19 AK7	The VDD1V8 pins should be connected to a well decoupled +1.8 V DC supply. These power pins provide DC current to the digital core.
VSS	Ground	A2 A3 A4 A6 A11 A16 A21 A26 A28 A29 A30 B1 B3 B16 B29 B31 C1 C2 C30 C31 D1 D31 F1 F31 L1 L31 T1 T2 T30 T31 AA1 AA31 AF1 AF31 AH1 AH31 AJ1 AJ2 AJ30 AJ31	The VSS pins should be connected to ground. They provide a ground reference for the 3.3 V rail and a ground reference for the 1.8 V rail.

Pin Name	Type	Pin No.	Function
VSS (Continued)	Ground	AK1 AK3 AK16 AK29 AK31 AL2 AL3 AL4 AL6 AL11 AL16 AL21 AL26 AL28 AL29 AL30 AL25 AJ24 AG23 AL23 AJ22 AL22 AG20 AJ20 AL20 AH24 AK24 AL24 AH22 AK22 AH21 AH20 AK20 AG19 A13 E14 D14 B14 A14 E15 C15 B15 A15	The VSS pins should be connected to ground. They provide a ground reference for the 3.3 V rail and a ground reference for the 1.8 V rail.

Pin Name	Type	Pin No.	Function
NC		B9 B24 C9 C17 C24 J5 J29 J30 R3 U28 U29 AD29 AD30 AG22 AH15 AJ8 AJ15 AK8 AK23 K28 B17 E17 A18 C18 D18 E18 B19 C19 E19	No Connect

Notes on Pin Description

1. All FREEDM 84A1024 inputs and bi-directionals present minimum capacitive loading.
2. All FREEDM 84A1024 outputs can be tristated under control of the IEEE P1149.1 test access port, even those which do not tristate under normal operation. All outputs and bi-directionals are 3.3 V tolerant when tristated.
3. Inputs TMS, TDI and TRSTB have internal pull-up resistors.
4. Power to the VDD3V3 pins should be applied *before* power to the VDD1V8 pins is applied. Similarly, power to the VDD1V8 pins should be removed *before* power to the VDD3V3 pins is removed.

10. Functional Description

10.1. Interfaces

10.1.1. Scaleable Bandwidth Interconnect (SBI) Interface

The Scaleable Bandwidth Interconnect is a synchronous, time-division multiplexed bus designed to transfer, in a pin-efficient manner, data belonging to a number of independently timed links of varying bandwidth. The SBI interface supported in FREEDM 84A1024 is a parallel 8 bit wide 19.44 MHz or 77.76 MHz bus.

Timing is communicated across the Scaleable Bandwidth Interconnect by floating data structures. Payload indicator signals in the SBI control the position of the floating data structure and therefore the timing. When sources are running faster than the SBI the floating payload structure is advanced by an octet by passing an extra octet in the V3 octet locations (H3 octet for DS3 mappings). When the source is slower than the SBI the floating payload is retarded by leaving the octet after the V3 or H3 octet unused. Both these rate adjustments are indicated by the SBI control signals.

The SBI multiplexing structure is modeled on the SONET/SDH standards. The SONET/SDH virtual tributary structure is used to carry T1/J1 and E1 links. Unchannelized DS3 payloads follow a byte synchronous structure modeled on the SONET/SDH format.

An SBI interface consists of a DROP BUS and an ADD BUS. On the DROP BUS all timing is sourced from the PHY and is passed onto the FREEDM 84A1024 by the arrival rate of data over the SBI. On the ADD BUS either the PHY or the FREEDM 84A1024 can control timing. When the FREEDM 84A1024 is the timing master, the PHY device determines it's transmit timing information from the arrival rate of data across the SBI. When the PHY device is the timing master, it signals the FREEDM 84A1024 to speed up or slow down with justification request signals. The PHY timing master indicates a speedup request to the Link Layer by asserting the justification request signal high during the V3 or H3 octet of the DROP bus. When this is detected by the FREEDM 84A1024 it will advance the channel by inserting data in the next V3 or H3 octet as described above. The PHY timing master indicates a slowdown request to the FREEDM 84A1024 by asserting the justification request signal high during the octet after the V3 or H3 octet of the DROP bus. The FREEDM 84A1024 responds by leaving the octet following the next V3 or H3 octet unused. Both advance and retard rate adjustments take place in the frame or multi-frame following the justification request.

The SBI structure uses a locked SONET/SDH structure fixing the position of the TUG-3/TU-3 relative to the STS-12/STM-4 transport frame. The SBI is also of fixed frequency and alignment as determined by the reference clock (REFCLK) and frame indicator signal (AC1FP or DC1FP). Adjusting the location of the T1/J1/E1/DS3 channels using floating tributaries as determined by the V5 indicator and payload signals (DV5, AV5, DPL and APL) compensates frequency deviations.

The multiplexed links are separated into three Synchronous Payload Envelopes. Each envelope may be configured independently to carry up to 28 T1/J1s, 21 E1s, 1 DS3 or 1 Fractional Rate DS3/E3.

10.1.2. ANY-PHY Interface

The ANY-PHY Interface is an asynchronous interface that supports the transfer of data to and from the ANY-PHY channels within the FREEDM 84A1024 . Two variants of the ANY-PHY interface are supported in FREEDM 84A1024 : a parallel 52 MHz 16 bit wide bus (ANY-PHY Level-2), and a parallel 8 bit wide 104 MHz bus (ANY-PHY Level-3).

ANY-PHY Modes of Operation

The figures below show the different transfer formats for each mode.

Datagrams are transferred across the interface as a series of continuous segments. A segment (Figure 3) consists of an address prepend and a fixed size of data. The address prepend indicates the ANY-PHY channel associated with the segment. For multilink bundles, the address prepend maps to the multilink bundle while the address prepend maps to an HDLC channel for single links. The address prepend is not included in this segment size. A transfer will be terminated early if the end of packet occurs before the end of a segment. The segment size is global across the ANY-PHY interface. Minimum packet/frame size supported is 2 bytes.

If the polled TPA=1, the FREEDM 84A1024 expects an entire packet to be transferred. It is not permitted to interleave the segments of packets destined for different channels.

The address prepend identifies the ANY-PHY channel associated with the segment. On transmit, the FREEDM 84A1024 uses the address prepend to index ANY-PHY channel records that dictate the processing options for an ANY-PHY channel. A connection identifier, in the transmit direction, is used to index connection context records that FREEDM 84A1024 uses in processing the datagram. The connection record contains various connection information including an indication if this connection is to be fragmented. A connection identifier must be present on all datagrams being transferred on a link that supports fragmentation or is a member of a multilink bundle (required for all modes of operation except transparent). Begin (B) and End (E) bits are used to identify the starting fragment of a packet (B=1) and the last fragment of a packet (E=1). These are needed to support FRF.12 and RFC 1990 fragment transfers across the ANY-PHY interface. When a complete packet is transferred across the interface both bits (B and E) are set to 1.

It should be noted that the PID values (PID(H) and PID(L)) referenced in the following documents refers to the multilink PID = 0x003D if the connection is sequenced or the PID of the actual datagram if the connection is non-sequenced. In the case of a sequenced connection, the first Payload data will then be the actual PID of the datagram.

For uncompressed PPP packets, the FREEDM 84A1024 will accept any value of address and control fields (so as not to prohibit future changes of these values).

Figure 3 - ANY-PHY Level 2 Mode Segment Transfer – Non Sequenced Datagrams on a Link supporting sequencing (i.e. Control, LCP, NCP packets) (ingress and egress)

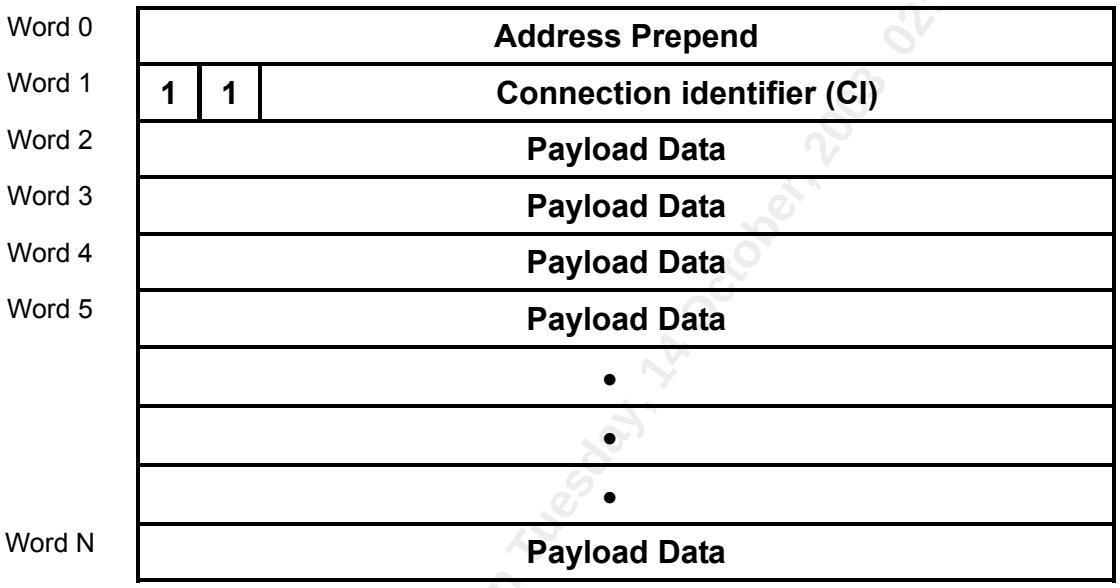
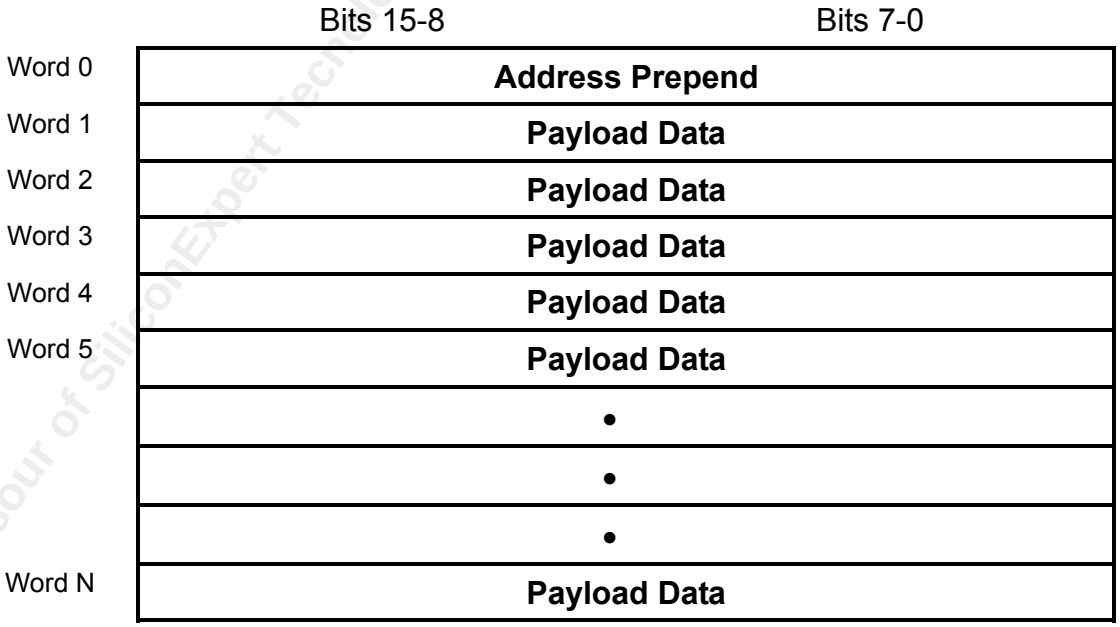


Figure 4 - ANY-PHY Level 2 Mode Segment Transfer – Non-Header Segment (i.e. not first segment of a datagram) or Transparent Mode (ingress and egress)



ANY-PHY Level 2 Mode – Figure 5 - Figure 10 illustrate the transfer requirements for the various transfer types using this mode.

Figure 5 - ANY-PHY Level 2 Mode Header Segment – PPP over sequenced link (ingress and egress)

	Bits 15-8		Bits 7-0
Word 0	Address Prepend		
Word 1	B	E	Connection Identifier (CI)
Word 2	Address		Control
Word 3	PID(H)		PID(L)
Word 4	Payload Data		
Word 5	Payload Data		
Word 6	Payload Data		
	•		
	•		
	•		
Word N	Payload Data		

Figure 6 - ANY-PHY Level 2 Mode Header Segment – FR over sequenced link (ingress and egress)

	Bits 15-8				Bits 7-0				
Word 0	Address Prepend								
Word 1	B	E	Connection Identifier (CI)						
Word 2	DLCI (msb)			C/R	EA=0	DLCI (lsb)	FECN	BECN	DE	EA=1
Word 3	Payload Data								
Word 4	Payload Data								
Word 5	Payload Data								
Word 6	Payload Data								
	•								
	•								
	•								
Word N	Payload Data								

Figure 7 illustrates the first segment of a datagram on the receive interface when the system side device receiving the segments supports fragmentation. In this application, the sequence number of the fragment is appended to the PPP header as defined in RFC 1990. This allows the system side device to detect lost fragments.

Figure 7 - ANY-PHY Level 2 Mode Header Segment – ML- PPP with Fragments out (Ingress Only)

	Bits 15-8					Bits 7-0
Word 0	Address Prepend					
Word 1	B	E	Connection Identifier (CI)			
Word 2	Address					Control
Word 3	PID(H)					PID(L)
Word 4	B	E	COS (3:0)	0	0	Sequence Number (Long)
Word 5	Sequence Number (Long)					
Word 6	Payload Data					
	Payload Data					
	Payload Data					
	•					
	•					
	•					
Word N	Payload Data					

For short Sequence numbers, Words 4 and 5 get replaced with one word:

B	E	COS(1:0)	Sequence Number (Short)

Figure 8 - Figure 10 are representative of packets with PPP header compression being performed.

Figure 8 - ANY-PHY Level 2 Mode Header Segment – PPP over a sequenced link with Address and Control Field Header Compression (ingress and egress)

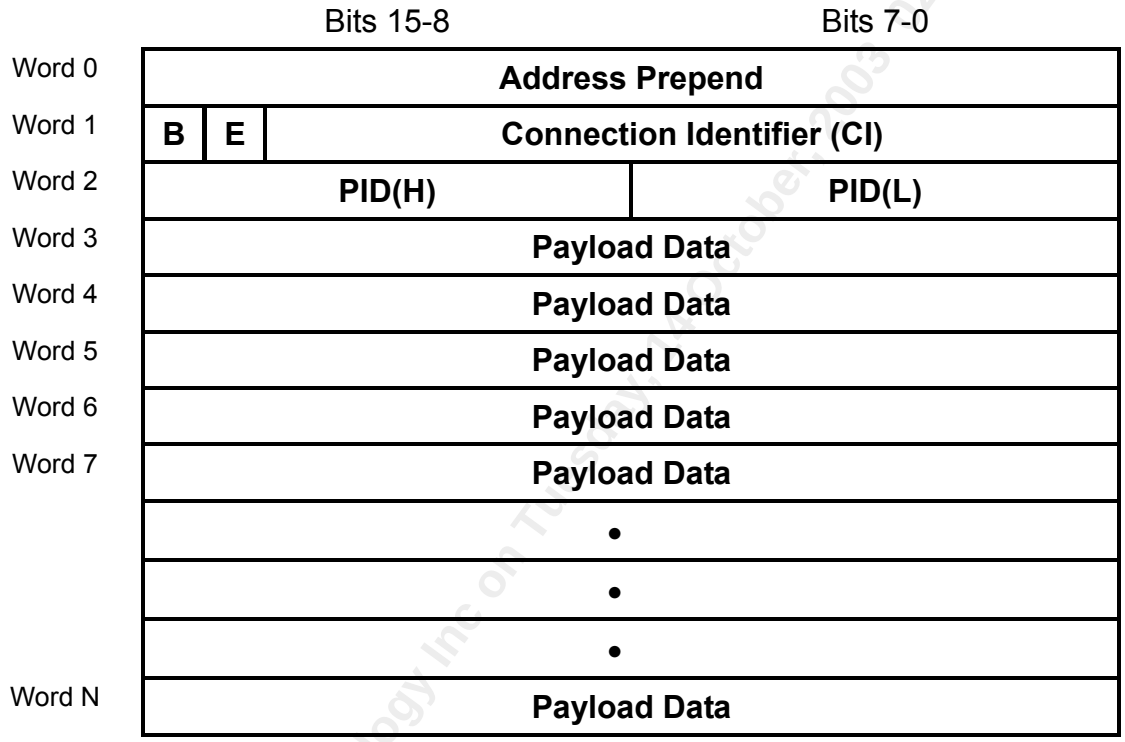
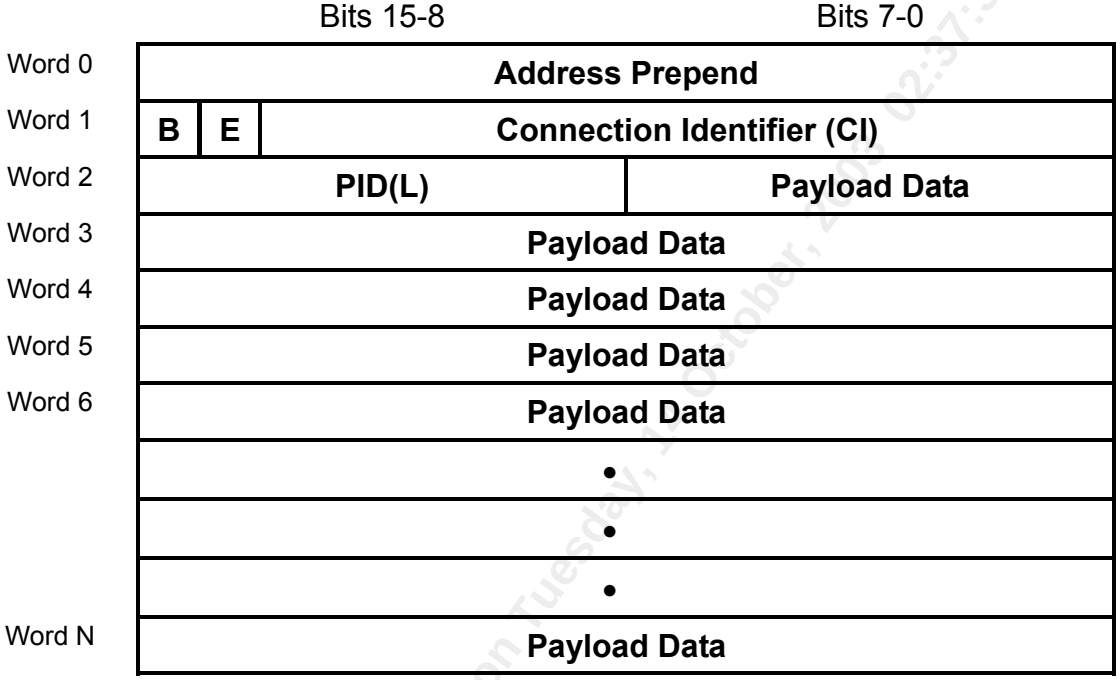


Figure 9 - ANY-PHY Level 2 Mode Header Segment – PPP over a sequenced link with PID Header Compression (ingress and egress)

	Bits 15-8	Bits 7-0
Word 0	Address Prepend	
Word 1	B E	Connection Identifier (CI)
Word 2	Address	Control
Word 3	PID(L)	Payload Data
Word 4	Payload Data	
Word 5	Payload Data	
Word 6	Payload Data	
Word 7	Payload Data	
	•	
	•	
	•	
Word N	Payload Data	

Figure 10 - ANY-PHY Level 2 Mode Header Segment – PPP over a sequenced link with Address /Control Field and PID Header Compression (ingress and egress)



ANY-PHY Level 3 mode. Figure 11 shows how words are transferred as bytes and Figure 12 gives an example of such a transfer. All transfer types shown in Level-2 are also supported in Level-3.

Figure 11 - ANY-PHY Level 3 Mode Segment – Transparent or Non-Header Segment (ingress and egress)

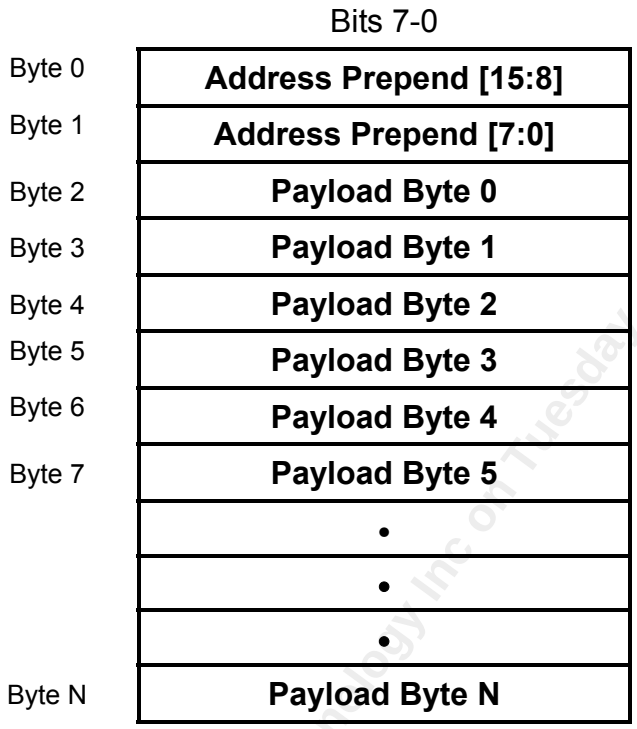
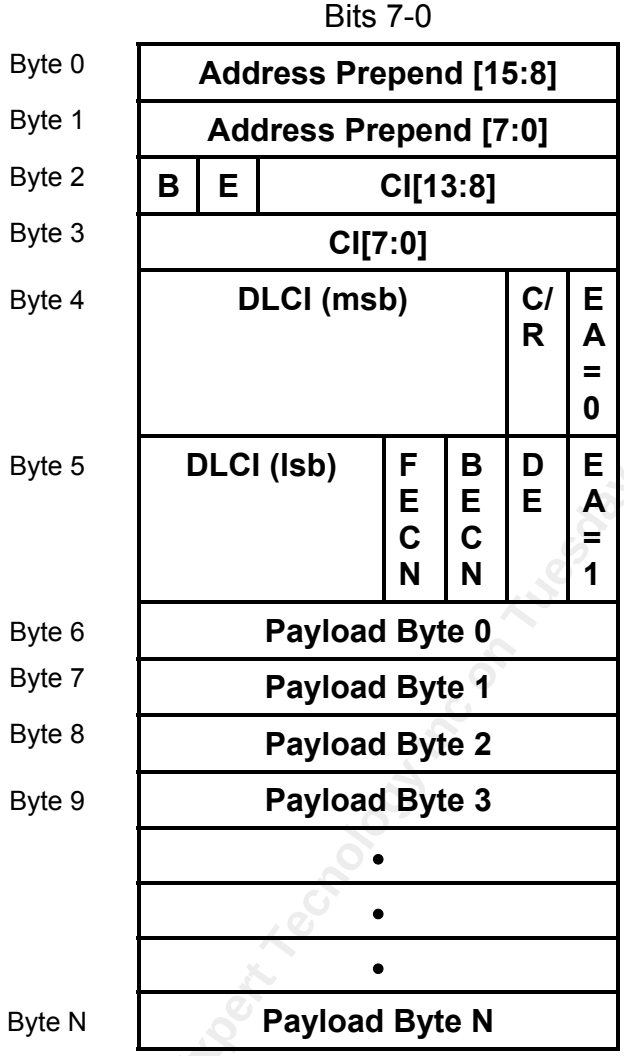


Figure 12 - ANY-PHY Level 3 Mode Header Segment – FR over a sequenced link (ingress and egress)



10.2. Memory Port

10.2.1. Writing

Write operations to external memory can be performed in up to 4-long word bursts to the memory port. The procedure is as follows:

1. The microprocessor polls the MPBusy bit of the Memory Port Control register (or monitors the MPISTATI interrupt) to verify that the previous write is complete. Alternatively, this step may be skipped if the system application allows FREEDM 84A1024 to withhold the READYB for write accesses. In this case, FREEDM 84A1024 will delay write operations to the write burst registers and overflow register until the previous write command is complete.

2. The microprocessor writes up to 4 long words of data into the write burst register array and the overflow register (for 48-bit accesses).

3. The microprocessor writes a command to the memory burst control register. The command indicates the aperture, the quad-long word address in memory, the type of write (masked or unmasked), and the 4 long word enables. MPBusy will be set until the write is complete.

4. FREEDM 84A1024 arbitrates for the appropriate memory, performs the write to memory, and clears the MPBusy bit in the control register.

10.2.2. Reading

Reads from external memory can be performed in 4-long word bursts from the memory port. The procedure is as follows:

1. The microprocessor issues a read command to the Memory Port Control register. The command indicates aperture, the quad-long word address in memory, and 4 long word enables. The MPBusy bit will be set by the FREEDM 84A1024.

2. FREEDM 84A1024 arbitrates for the appropriate memory, performs the read from memory and loads the read burst registers with the results, and clears the MPBusy bit in the control register.

3. The microprocessor polls the MPBusy bit of the Memory Port Control register status (or monitors the MPISTATI interrupt) to verify that the read is complete. Alternatively, this step may be skipped if the system application can tolerate long response times for read accesses. In this case, FREEDM 84A1024 will delay read operations from the read burst registers and overflow register until the read command is complete.

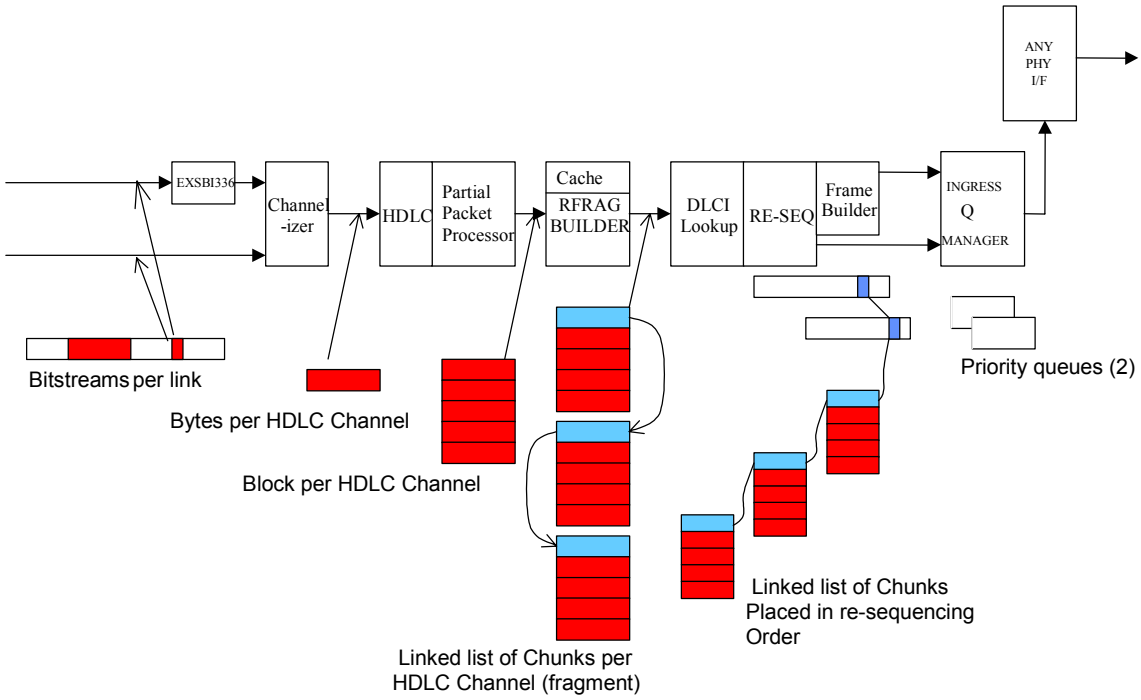
4. The microprocessor reads up to 4 long words of data from the read burst register array and the overflow register (for 48-bit accesses).

10.3. Packet Walkthrough

10.3.1. Ingress Path

Figure 13 shows the elements and data transformations that occur as data traverses the FREEDM 84A1024 from the SBI to the ANY-PHY interface.

Figure 13 - Ingress Data Flow



Data arriving via the SBI interface is extracted from the SBI format and associated with an HDLC channel. In addition to the SBI bus, 3 clock and data interfaces are also supported simultaneously. Each link is independent and has its own associated clock. For each link, a serial to parallel conversion forms the data bytes. The data bytes are multiplexed, in byte serial format, for delivery to the HDLC/Partial Packet Processor block

The HDLC engine receives the incoming byte stream and examines the byte stream to delineate the opening and closing of the HDLC packet. Bit de-stuffing is performed, FCS checking and minimum/maximum packet size checking is performed. The HDLC engine is capable of simultaneously processing 1024 independent HDLC channels. The resulting HDLC data and status information is passed to the Partial Packet Processor to be stored in the appropriate HDLC channel FIFO buffer.

The Partial Packet Processor controls a 64 Kbyte partial packet RAM. Data is written into the RAM at a location that is associated with the HDLC channel. As more data arrives for a given HDLC channel, it is stored with the previous bytes of data for a given HDLC channel forming a chunk of data. Packets are not intermingled within chunks. Completed chunks are passed to the fragment builder.

Fragments are defined as per FRF.12 and RFC 1990. The chunk is stored in external SDRAM in a data structure that is indexed on a per datagram basis. The fragment builder can simultaneously reconstruct 1024 datagrams (one per HDLC channel).

Completed datagrams are forwarded to the lookup and re-sequencing stage. This stage performs a header lookup that is used to determine connection identifier. A connection record associated with the CI contains a number of state variables used in the re-sequencing operation and to guide the remaining ingress operations for the datagram. Re-sequencing is required when ML-FR or ML-PPP is active on a given set of HDLC channels. Given the variable length of data transfers and skew between the physical links in the multilink bundle, re-sequencing is essential to enabling multilink protocols. Both 12 and 24 bit sequence numbers are supported for PPP while the 12 bit FRF.12 format is supported for FR.

The incoming sequence number is compared with the expected sequence number. If the two are equal, the datagram does not need to be re-sequenced and is logically passed to the ingress queue or the packet/frame builder depending on the style of data transfer (packet or fragment) requested for the ANY-PHY channel.

If the sequence numbers do not align, a re-sequencing operation is triggered and the datagram is logically placed in the re-sequencing buffers. The datagram is removed from the re-sequencing buffers when the re-sequencing operation has correctly re-sequenced the datagrams. These datagrams are passed to the frame builder or the ingress queue manager depending on the mode of transfer. In addition to re-sequencing, a loss detection algorithm detects lost datagrams.

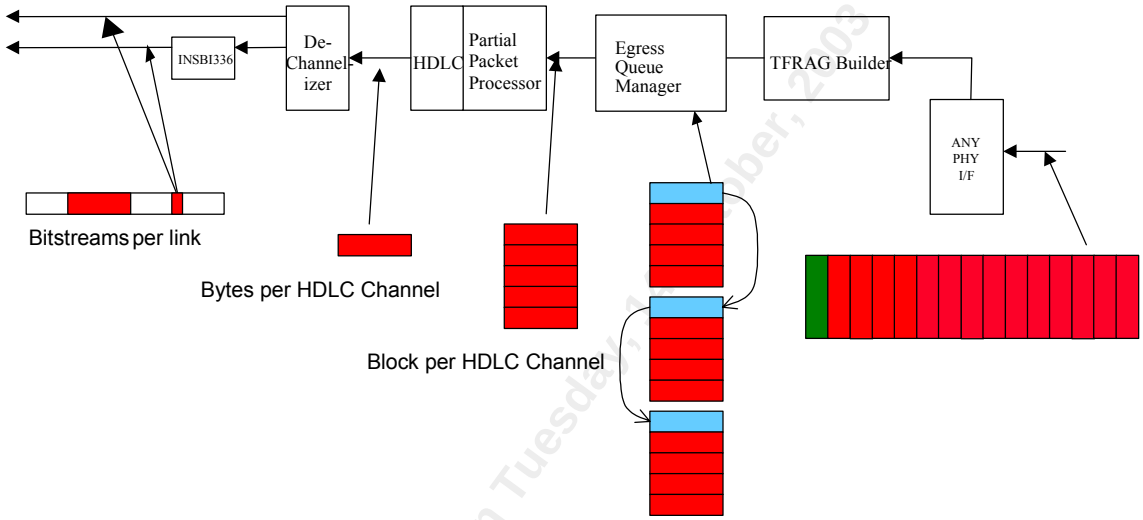
When the ANY-PHY transfer is frame/packet based, the frame builder constructs complete frames or packets from the datagrams that have been constructed by the fragmentation builder. These complete frames/packets are transferred to the ingress queue manager.

The ingress queue manager arbitrates between the packets/frames and fragments that are available to be sent. The resulting decision is passed to the ANY-PHY interface. The selected fragment/packet is transferred to the upstream system device via the ANY-PHY interface.

10.3.2. Egress Path

Figure 14 shows the elements and data transformations that occur as data traverses the FREEDM 84A1024 from the ANY-PHY to the SBI interface.

Figure 14 - Egress Data Flow



Full packets or fragments can be transferred from the upstream device to the FREEDM 84A1024 via the ANY-PHY interface. When supporting a multilink bundle, the ANY-PHY channel is mapped to multiple HDLC channels. The transmit fragmentor will fragment packets/frames and distribute the fragments across all the HDLC channels in the multilink bundle applying the appropriate sequence number to each of the fragments. The fragmentation size is programmable on a per multilink bundle basis. The fragmentation size is referenced to the number of bytes transferred on the link and includes the multilink header.

On an HDLC channel basis the datagrams are decomposed into chunks and are stored in an external SDRAM memory. A chunk is defined as a fixed length unit of data (32 bytes) plus a 4 byte header, or a partially completed unit of data. A chunk will only consist of data from one packet/frame.

The chunk transmitter controls a 64 Kbyte partial packet RAM. A data chunk is transferred from external memory into the partial packet RAM in a burst. Data is read from the RAM a byte at a time and delivered to the HDLC engine. The chunk transmitter can support 1024 simultaneous byte transfer sessions (one per HDLC channel). As chunks are depleted, the chunk transmitter requests the next chunk for the associated HDLC channel from the fragment transmitter.

The HDLC engine receives the incoming byte stream and encapsulates the data stream with a HDLC header, bit stuffing and a FCS trailer. The HDLC engine is capable of simultaneously processing 1024 independent HDLC channels. The resulting HDLC data and status is passed to the de-channelizer to be transferred onto the links.

Data arriving at the SBI interface is inserted into the SBI format at the correct tributary and timeslot associated with a HDLC channel. In addition to the SBI bus, 3 clock and data interfaces are also supported.

10.4. Loopback

Clock and Data Loopback

The line loopback enable bits in the Master Line Loopback Register control line loopback for the three serial clock and data links. When loopback is enabled, the data on RD[n] is passed verbatim to TD[n] which is then updated on the falling edge of RCLK[n]. TCLK[n] is ignored. When loopback is disabled, TD[n] is processed normally.

SBI Line Loopback

When enabled, the data on tributary #n output by the EXSBI block is looped back to the tributary #n in the INSBI block. When loopback is disabled, transmit data for tributary #n is provided by the TCAS-12 block (i.e. processed normally).

System Side Loopback

The loopback controller block in the RCAS-12 TSB implements the channel based diagnostic loopback function. Every valid data byte belonging to a channel with diagnostic loopback enabled from the Transmit HDLC Processor / Partial Packet Buffer block (THDL-12) is written into a 1024 word FIFO in the RCAS-12 block. The loopback controller monitors for an idle time-slot or a time-slot carrying a channel with diagnostic loopback enabled. If either condition holds, the current data byte is replaced by data retrieved from the loopback data FIFO.

10.5. Initialization Process

Configuration of a channel/CI cannot be changed while data is flowing on that channel/CI.

10.5.1. CB and RS Memory FPP Initialization

1. After a hardware or software reset are issued, the chip goes into an initialization sequence. The RST_DONEI bit in the F84 Master High Priority Interrupt Status register will indicate when this sequence is complete. At this stage, all the registers and memories internal to the chip and the external SRAM can be accessed.

2. Wait for SDRAM_INIT to be cleared in XX_DRAMC Status and Control Registers (PROV_MODE will also be set at this point).

3. Test memories if desired by s/w.

4. FPP FIFO Initialization

- Option 1 (s/w init)
  - write ECC_OFF bit as desired
  - write to the memory setting up the FPP FIFO as described in the XX_DRAMC memory map descriptions
  - write FUNC_MODE=1 and PROV_MODE=0 in the XX_DRAMC Status and Control Registers
- Option 2 (h/w init)
  - write ECC_OFF bit to 1
  - write FPP_INIT bit =1 and PROV_MODE=0 in the XX_DRAMC Status and Control Registers
  - wait for FUNC_MODE to be set indicating completion (PROV_MODE will also be cleared)

5. Initialization Complete

10.5.2. Connection Initialization for sequenced links

When adding a connection to a multilink bundle (including first connection setup), the FREEDM 84A1024 takes the first sequence number it receives to start re-sequencing. Due to differential delay between links, if this isn't the fastest link, this might not be the start of packet. All subsequent fragments with lower sequence numbers will not be included in the re-sequencing and will be sent out the ANY-PHY tagged as unexpected sequence number. The number of packets tagged as USN will depend on packet size and egress scheduling algorithm. Once the first re-sequenced packet is complete (if in packet out mode), this packet will be sent out missing the first few fragments but will not be tagged as erred. This will happen with every new connection. In order to avoid this, one of the following can be done:

1. Ensure the first fragment is sent down the fastest link.
2. Send the first fragment down any link and wait a time period equal to the worst case link skew but less than the programmed lost timeout period before sending the second fragment.

10.6. ANY-PHY Tear Down Procedure

Before tearing down an ANY-PHY channel, all CI's associated with that ANY-PHY channel must be torn down according to the procedure described in section 10.7. In addition, the data must be drained for the channel. This is done by:

1. Unprovision RCAS channel

2. Disable EXSBI channel

3. Reduce LOST timer for all constituent CIs to 10ms (this is not required, just suggested in case holes remain)

4. Wait for AP_NCHNKS (in RFRAG Memory Map) to go to zero.

10.7. CI Tear Down Procedure

A CI tear-down procedure must be followed when decommissioning an active CI to avoid loss of resources shared among all active CIs. Since the decommissioned CI continues to hold up to one LSB record, the algorithm that assigns active CI's from the pool of inactive CI's should recycle previously used CI's before assigning a previously unused CI. This will result in the best use of shared resources.

The tear-down procedure is comprised of the following seven steps:

1. Remove the CI from the CI Lookup table to ensure no additional datagrams are received for the CI undergoing decommissioning.

2. Read the FIFO Active (FIFO_ACT) bit in the connection context memory for the CI. Determine whether resequencing is still in progress by reading the HEAD, HOLE and TAIL_VALID fields in the connection context memory for the CI. Resequencing is in progress if the HEAD and HOLE fields are not equal of if the TAIL_VALID bit is 1.

3. If FIFO_ACT is 0 and resequencing has stopped, skip the next two steps.

4. If resequencing is still in progress set the Lost Timeout Period (LOST_CNT) register to "0001" in the connection context memory for the CI.

5. Periodically read the FIFO_ACT bit and test for resequencing in progress until FIFO_ACT is 0 and resequencing has stopped.

6. Read the MSB record associated with the CI and extract the valid LSB record pointer, if applicable. To identify a valid LSB record pointer within the MSB record structure all 128 locations of the MSB record must be read and examined. Bit 15, the 16^{th} bit, of each 32-bit data word returned indicates whether the lower 15-bits identify a valid LSB record pointer (LSB_POINTER). This pointer is used to determine what LSB status locations to clear for the CI being decommissioned. An MSB record is extracted from the external resequencing SDRAM memory by reading 128 consecutive locations beginning at the address as determined by the following equation: MSB Record begin address = 800,000H + CI_number x 80H.

7. If applicable, clear the LSB status for the active LSB record. Each 32-bit location within the LSB record status field contains status for 16 datagrams. Therefore to clear the status for the entire 128-location LSB record, 8 LSB status locations must be cleared to zero. The 8 consecutive locations requiring clearing begin at the address determined by the following equation: LSB status begin address = 400,000H + LSB_POINTER x 8H.

8. Clear connection context memory for the CI. At this point tear-down is completed.

10.8. Restrictions on ANY-PHY to CI mapping

For proper operation,

1. No CI may be shared across multiple Any-PHY channels.

2. A non-sequenced CI value may be shared among various DLCI's within a single HDLC channel.

3. In multilink applications, the sequenced CI value corresponding to a particular DLCI\COS value must be shared across all HDLC channels of the bundle. However, except in the case of the default CI, the sequenced CI value must NOT be shared across different DLCI\COS values.

4. HDLC channels of a ML bundle must map to the same Any-PHY channel.

5. Each HDLC channel must have 2 unique default CI's. One for all unused non-sequenced locations, and a second for all unused sequenced locations in the CI_LOOKUP records in the Resequence Structures (RS) memory.

10.9. Block Descriptions

10.9.1. Extract Scaleable Bandwidth Interconnect (EXSBI)

The SBI Extract block receives data from the SBI DROP BUS and converts it to an internal parallel bus format. The SBI Extract block may be configured to enable or disable reception of individual tributaries within the SBI DROP bus. Individual tributaries may also be configured to operate in framed or unframed mode. Tributaries may be configured to support channelized T1/J1/E1 traffic, unchannelized DS3 traffic or unframed traffic at T1/J1, E1, 1 DS3 or Fractional DS3/E3 rates.

10.9.2. Receive Channel Assignor (RCAS-12)

The Receive Channel Assignor block (RCAS-12) processes up to 84 links. When receiving data from the SBI blocks, links may be configured to support channelized T1/J1/E1 traffic, unchannelized DS3 traffic or unframed traffic at T1/J1, E1, DS3 or Fractional DS3/E3 rates. When receiving data from the RD inputs, links 0, 4 and 8 support unchannelized data at arbitrary rates up to 52 Mbps.

It should be noted that for every SBI/SPE used as a serial link, the SBI/SPE must be disabled on the SBI Bus interface and visa versa.

Each link is independent and has its own associated clock. When receiving data from the RD inputs, the RCAS-12 performs a serial to parallel conversion to form data bytes. The data bytes are multiplexed, in byte serial format together with data from EXSBI, for delivery to the Receive HDLC Processor / Partial Packet Buffer block (RHDL-12) at SYSCLK rate. In the event when multiple streams have accumulated a byte of data, multiplexing is performed on a fixed priority basis with link #0 having the highest priority and link #332 the lowest.

The 84 RCAS links have a fixed relationship to the SPE and tributary numbers on the SBI DROP BUS as shown in the following table.

Table 11 - SBI SPE/Tributary to RCAS Link Mapping

SPE No.	SBI Trib. No.	RCAS Link No.	SPE No.	SBI Trib. No.	RCAS Link No.	SPE No.	SBI Trib. No.	RCAS Link No.
1	1	0	2	1	4	3	1	8
1	2	12	2	2	16	3	2	20
1	3	24	2	3	28	3	3	32
●								●
●								●
●								●
1	28	324	2	28	328	3	28	332

Links containing a T1/J1 or an E1 stream may be channelized. Data at each time-slot may be independently assigned to a different HDLC channel. The RCAS-12 performs a table lookup to associate the link and time-slot identity with an HDLC channel. The position of T1/J1 and E1 framing bits/bytes is identified by frame pulse signals generated by the EXSBI. Links containing a DS3 stream are unchannelized, i.e. all data on the link belongs to one HDLC channel. The RCAS-12 performs a table lookup using only the link number to determine the associated HDLC channel, as time-slots are non-existent in unchannelized links. Links may additionally be configured to operate in an unframed “clear channel” mode, in which all bit positions, including those normally reserved for framing information, are assumed to be carrying HDLC data. Links so configured operate as unchannelized regardless of link rate and the RCAS-12 performs a table lookup using only the link number to determine the associated HDLC channel.

All timeslots in a link must be provisioned to a valid channel number before the link is enabled. For unused timeslots, a valid unused channel number must be set but the PROV bit is not set. All unused timeslots in the device can be mapped to the same unused channel number. When unprovisioning a channel, the INVERT bit in register 0x208 must be cleared (if set), The PROV bit is then set to 0 but the channel number must be written back into the channel number field. This will flush out any data on this channel still present in the chip. This sequence must occur before the link is disabled.

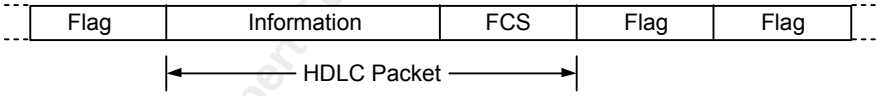
The loopback controller block implements the channel based diagnostic loopback function. Every valid data byte belonging to a channel with diagnostic loopback enabled from the Transmit HDLC Processor / Partial Packet Buffer block (THDL-12) is written into a 1024 word FIFO. The loopback controller monitors for an idle time-slot or a time-slot carrying a channel with diagnostic loopback enabled. If either conditions hold, the current data byte is replaced by data retrieved from the loopback data FIFO.

10.9.3. Receive HDLC Protocol Engine (RHDL-12)

The HDLC engine receives the incoming byte stream and examines the stream to determine the opening and closing of the HDLC packet. Bit de-stuffing, FCS checking and minimum/maximum packet size checking is performed. The HDLC engine is capable of simultaneously processing 1024 independent HDLC channels. The resulting HDLC data and status information is passed to the Partial Packet Processor to be stored in the appropriate HDLC channel FIFO buffer.

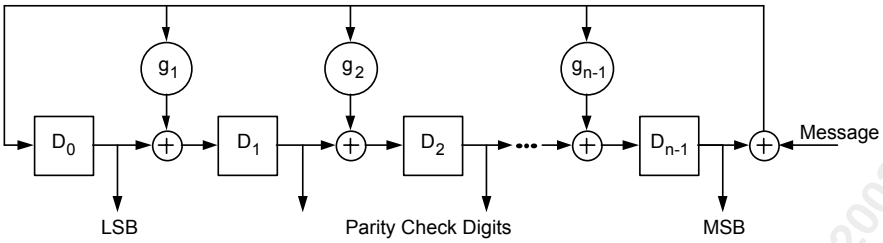
Figure 15 shows a diagram of the synchronous HDLC protocol supported by the FREEDM 84A1024 device. The incoming stream is examined for flag bytes (01111110 bit pattern) which delineate the opening and closing of the HDLC packet. The packet is bit de-stuffed which discards a "0" bit which directly follows five contiguous "1" bits. The resulting HDLC packet size must be a multiple of an octet (8 bits) and within the expected minimum and maximum packet length limits. The minimum packet length is that of a packet containing two information bytes (address and control) and FCS bytes. For packets with CRC-CCITT as FCS, the minimum packet length is four bytes while those with CRC-32 as FCS; the minimum length is six bytes. An HDLC packet is aborted when seven contiguous "1" bits (with no inserted "0" bits) are received. At least one flag byte must exist between HDLC packets for delineation. Contiguous flag bytes, or all ones bytes between packets are used as an "inter-frame time fill". Adjacent flag bytes may share zeros.

Figure 15 - HDLC Frame



The CRC algorithm for the frame checking sequence (FCS) field is either a CRC-CCITT or CRC-32 function. Figure 16 shows a CRC encoder block diagram using the generating polynomial $g(X) = 1 + g_1X + g_2X^2 + \ldots + g_{n-1}X^{n-1} + X^n$. The CRC-CCITT FCS is two bytes in size and has a generating polynomial $g(X) = 1 + X^5 + X^{12} + X^{16}$. The CRC-32 FCS is four bytes in size and has a generating polynomial $g(X) = 1 + X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$. The first FCS bit received is the residue of the highest term.

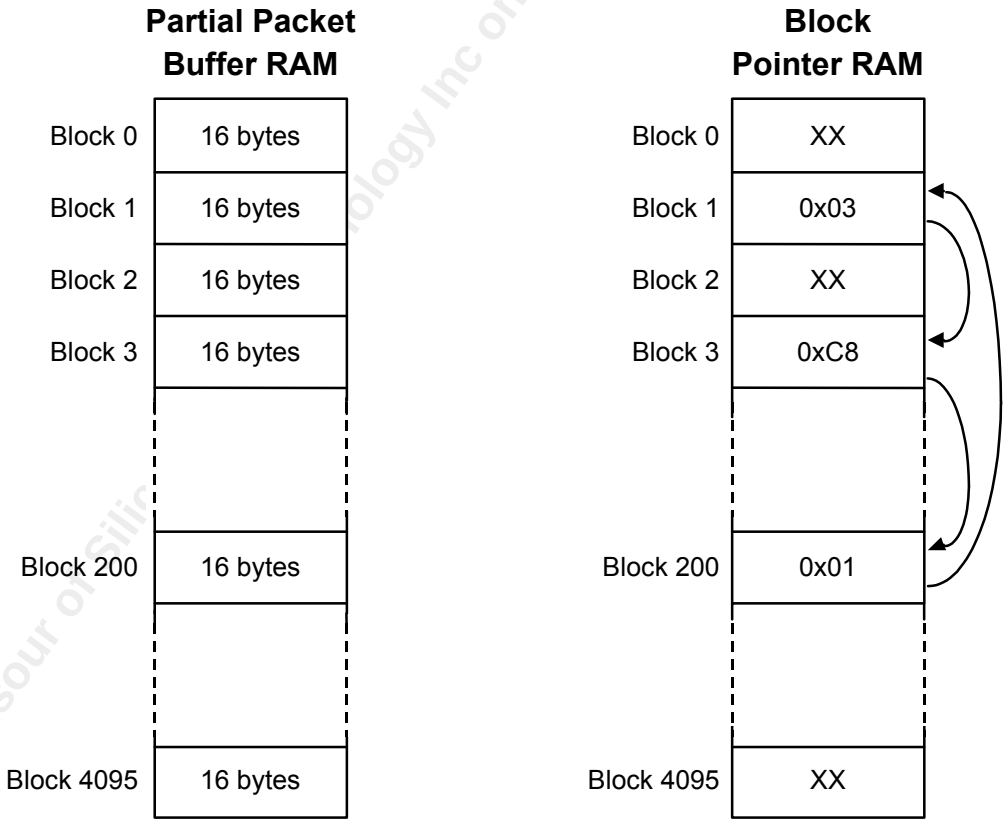
Figure 16 - CRC Generator



Partial Packet Buffer Processor

The partial packet buffer processor controls the 64 Kbyte partial packet RAM which is divided into 4K 16 byte blocks. A block pointer RAM is used to chain the partial packet blocks into circular HDLC channel FIFO buffers. Thus, non-contiguous sections of the RAM can be allocated in the partial packet buffer RAM to create an HDLC channel FIFO. System software is responsible for the assignment of blocks to individual HDLC channel FIFOs. Figure 17 shows an example of three blocks (blocks 1, 3, and 200) linked together to form a 48 byte HDLC channel FIFO.

Figure 17 - Partial Packet Buffer Structure



The partial packet buffer processor is divided into three sections: writer, reader and roamer. The writer is a time-sliced state machine which writes the HDLC data and status information from the HDLC processor into a channel FIFO in the packet buffer RAM. The reader transfers HDLC channel FIFO data from the packet buffer RAM to the downstream fragment builder block (RFRAG). The roamer is a time-sliced state machine which tracks HDLC channel FIFO buffer depths and signals the reader to service a particular HDLC channel. If a buffer over-run occurs, the writer ends the current packet from the HDLC processor in the HDLC channel FIFO with an overrun flag and ignores the rest of the packet.

The FIFO algorithm of the partial packet buffer processor is based on a programmable per-HDLC channel transfer size. Instead of tracking the number of full blocks in an HDLC channel FIFO, the processor tracks the number of transactions. Whenever the partial packet writer fills a transfer-sized number of blocks or writes an end-of-packet flag to the HDLC channel FIFO, a transaction is created. Whenever the partial packet reader transmits a transfer-size number of blocks or an end-of-packet flag to the RFRAG block, a transaction is deleted. Thus, small packets less than the transfer size will be naturally transferred to the RFRAG block without having to precisely track the number of full blocks in the HDLC channel FIFO.

The partial packet roamer performs the transaction accounting for all HDLC channel FIFOs. The roamer increments the transaction count when the writer signals a new transaction and sets a per-HDLC channel flag to indicate a non-zero transaction count. The roamer searches the flags in a round-robin fashion to decide for which HDLC channel FIFO to request transfer by the RFRAG block. The roamer informs the partial packet reader of the HDLC channel to process. The reader transfers the data to the RFRAG until the HDLC channel transfer size is reached or an end of packet is detected. The reader then informs the roamer that a transaction is consumed. The roamer updates its transaction count and clears the non-zero transaction count flag if required. The roamer then services the next HDLC channel with its transaction flag set high.

The writer and reader determine empty and full FIFO conditions using flags. Each block in the partial packet buffer has an associated flag. The writer sets the flag after the block is written and the reader clears the flag after the block is read. The flags are initialized (cleared) when the block pointers are written using indirect block writes. The writer declares an HDLC channel FIFO overrun whenever the writer tries to store data to a block with a set flag. In order to support optional removal of the FCS from the packet data, the writer does not declare a block as filled (set the block flag nor increment the transaction count) until the first double word of the next block in the HDLC channel FIFO is filled. If the end of a packet resides in the first double word, the writer declares both blocks as full at the same time. When the reader finishes processing a transaction, it examines the first double word of the next block for the end-of-packet flag. If the first double word of the next block contains only FCS bytes, the reader would, optionally, process next transaction (end-of-packet) and consume the block, as it contains information not transferred to the RFRAG block.

10.9.4. Receive Fragment builder (RFRAG)

The receive fragment builder re-constructs datagrams from the incoming data stream, moves data chunks from the partial packet processor into external memory, and manages the assignment of free external memory addresses to data chunks. The receive fragment builder also discards either small datagrams when an excessive number of datagrams are waiting to be processed by the re-sequencer, or any datagram when an ANY-PHY channel's chunk storage allocation has been exceeded.

The external chunk buffer memory is partitioned into data units called chunks. A chunk is a block (36 bytes) of contiguous memory used to store parts of the data frames. Associated with each chunk is an address that is used to index the chunk. The addresses are stored in the external memory in a free list FIFO. The Free list FIFO contains addresses of all the chunks that are available for the storage of data. A chunk of data is unavailable when the data stored within the chunk is part of a datagram that is being actively processed by the FREEDM 84A1024. Chunks become available when the FREEDM 84A1024 completes the processing of the data in the chunk (i.e. the datagram is transferred across the ANY-PHY interface to the rest of the system).

Fragments are defined as per FRF.12 or RFC 1990. This block can also support the creation of complete packets or frames if the HDLC channel is configured to Frame Relay or PPP modes. This can be supported on all 1024 HDLC channels simultaneously.

Data received from the partial packet RAM is encapsulated (Figure 18). The encapsulation contains the next address pointer, Last and Full flags, Error codes and an error correction code that covers the encapsulation header. The next address pointer is used to create a linked list of chunks that comprise a datagram (Figure 19).The address indicates where the next chunk of the datagram is located in the external memory. This effectively links the chunks of a datagram in external memory. The last flag is used to tag the last chunk of a datagram. The full flag indicates if the chunk contains 32 bytes of data. If the data chunk of a datagram is partially filled, the full flag is false and the number of valid bytes in the chunk is inserted in byte 0. The error codes are used to capture HDLC or RFRAG processing errors that have occurred. The error codes are provided to the system via the ANY-PHY interface enabling the system to observe the behavior of the HDLC channels.

The Partial packet RAM also passes the associated HDLC channel ID, End of datagram indication, and error flags (Bad FCS, Abort, etc.). The HDLC channel ID is used to index a data record that provides the next chunk pointer. This data record is also used to store frame relay header bits (Sequence number, DLCI, BE, FE, DE, B, E, C) or PPP header bits (Address, Control, PID, COS, and Sequence number, B, E), and the address of the first chunk in the datagram. These header fields are passed to the frame builder after the last chunk in a given datagram is stored. Header bits are extracted from the first data chunk of a datagram. Corrupted datagrams are tagged and the starting address is passed forward to the re-sequencer.

The RFRAG can be configured to accept compressed PPP headers. The RFRAG will correctly interpret the compressed header, and extract the information required for downstream processing from the packet.

The encapsulated data chunk, and an address pointer are passed to the DRAMC controller for storage in external SDRAM. The address pointer is contained in the HDLC channel record and points to the memory location that is placed in the next address pointer field of the previous data chunk for a given datagram. The initial chunk of a datagram is stored at an address location, (starting address of the datagram).

Datagrams may also be discarded before they are stored in the external SDRAM. When there are too many datagrams waiting to be processed by the re-sequencer, any datagram smaller than either a default 40-byte limit, or a programmable 0 to 56-byte threshold, will be discarded, except if it is tagged as the last fragment of a multi-fragment frame/packet. Furthermore, each ANY-PHY channel has a limit in the maximum number of chunks that it can have stored in the external SDRAM at any time. If this limit is exceeded, all datagrams for this ANY-PHY channel will be discarded until the number of chunks stored in the external SDRAM is reduced below the limit.

The free list FIFO is stored in external memory. To reduce the accesses to external memory, an address cache is used to hold addresses that can be used for next pointer values. When a chunk is encapsulated, the HDLC channel record will fetch, from the local cache, an address that can serve as the next address for the following data chunk in the datagram. As chunks are retrieved from the external memory for the address is returned to the cache. When the cache needs to be replenished, a request is made to the DRAMC. A set of new addresses is provided from external memory. The external read request is triggered off of a threshold. When the internal Cache crosses the threshold, it requests a read from external memory.

Figure 18 - Encapsulated Chunk Structures

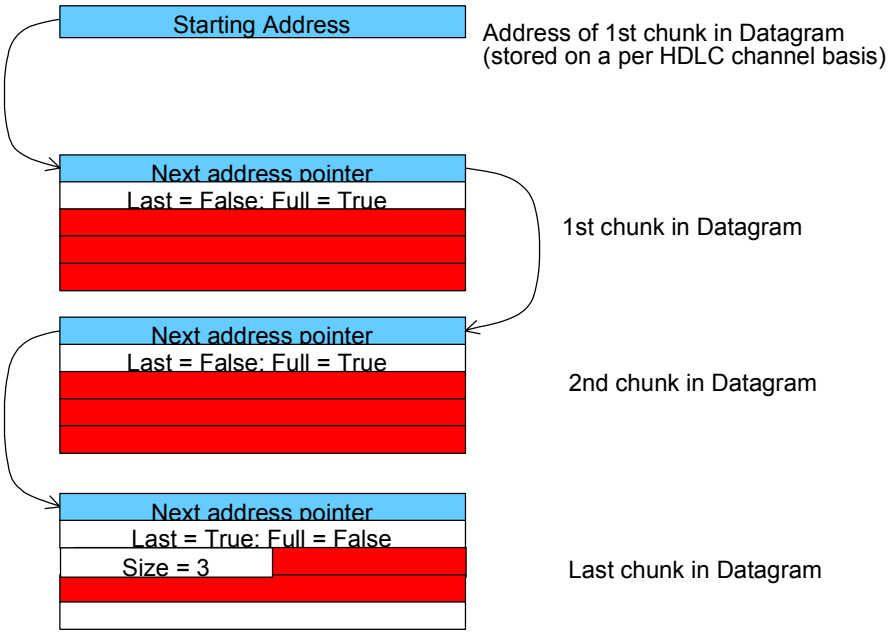
a) Encapsulated Chunk Structure (Full = True)

Byte 1	Byte 0	ECC(8)	L	F	EC(3)	NXT_CHUNK_PTR(19)	
Byte 7	Byte 6	Byte 5	Byte 4			Byte 3	Byte 2
Byte 13	Byte 12	Byte 11	Byte 10			Byte 9	Byte 8
Byte 19	Byte 18	Byte 17	Byte 16			Byte 15	Byte 14
Byte 25	Byte 24	Byte 23	Byte 22			Byte 21	Byte 20
Byte 31	Byte 30	Byte 29	Byte 28			Byte 27	Byte 26

b) Encapsulated Chunk Structure (Full = False)

Byte 0	Size	ECC(8)	L	F	EC(3)	NXT_CHUNK_PTR(19)	
Byte 6	Byte 5	Byte 4	Byte 3			Byte 2	Byte 1
Byte 12	Byte 11	Byte 10	Byte 9			Byte 8	Byte 7
Byte 18	Byte 17	Byte 16	Byte 15			Byte 14	Byte 13
Byte 24	Byte 23	Byte 22	Byte 21			Byte 20	Byte 19
Byte 30	Byte 29	Byte 28	Byte 27			Byte 26	Byte 25

Figure 19 - Linked list data structure of a Datagram



10.9.5. Frame Builder (FRMBLD)

To build frames/packets from fragments requires several steps. The specific multilink/single session has to be identified, re-sequencing (for multilink sessions) followed by the actual frame/packet building are the key steps in this process.

Connection identification

The header of the datagram is used to index internal record structures needed to support re-sequencing, and ingress queuing.

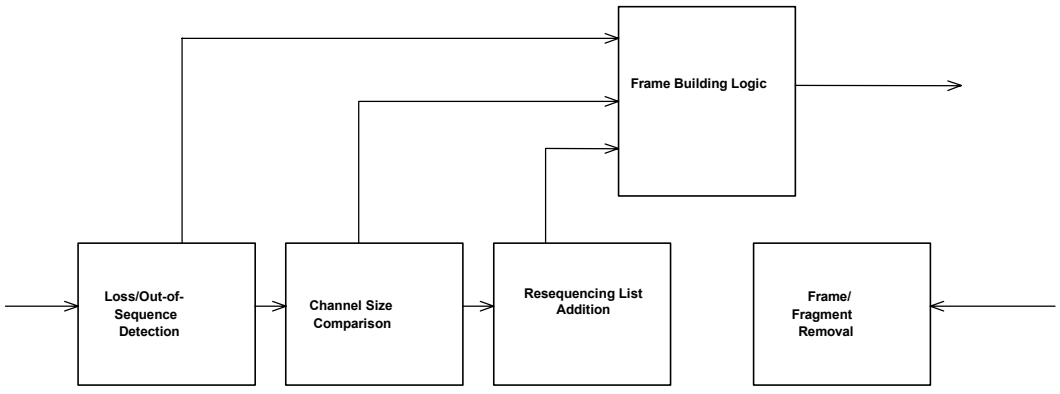
A lookup is used for HDLC channels supporting the Frame Relay protocol. The objective is to reduce the HDLC channel (10 bits) and the Q.922 header (10 bits DLCI, C bit and frag bit) to a 14-bit CI. The HDLC channel number is concatenated with two bits indicating if the datagram is corrupt or valid, if the datagram is a control datagram, if the datagram is sequenced or non sequenced. This value is then concatenated with the DLCI(1-1024) for sequenced and non sequenced datagrams to produce an index into the SSRAM memory. Contained at the memory location is the 14 bit CI.

For PPP header identification, the HDLC channel number is concatenated with two bits indicating if the datagram is corrupt or valid, if the datagram is an NCP or LCP datagram, if the datagram is sequenced or non sequenced. This value is then concatenated with the COS (1-16) for sequenced and non sequenced datagrams to produce an index into the SSRAM memory. Contained at the memory location is the 14 bit CI. Unique CI's must be used for each HDLC channel.

Re-Sequencing builder

The Re-Sequencing blocks provide the logic and data structures necessary to support the operations needed to support the re-ordering of ingress datagrams. These include detection of lost or out of bound datagrams, the placement of sequences in the correct order, construction of frames/packets out of fragments, and transfer the resequenced/reassembled frames/packets to the ingress queue manager.

Figure 20 - The elements in the Re-sequencing block



Loss Detection/Out of bounds checking

The loss detection block is based on the use of timers. Timers associated with each resequencing session would be used to detect the lost datagram and advance the resequencing engine. Each multilink re-sequencing session has an associated timer. When the multilink session transitions from in sequence to out of sequence, a timer is started. This timer is cleared when the session returns to being in sequence. All timers are periodically polled to detect sessions that have been out of sequence for an extended period of time.

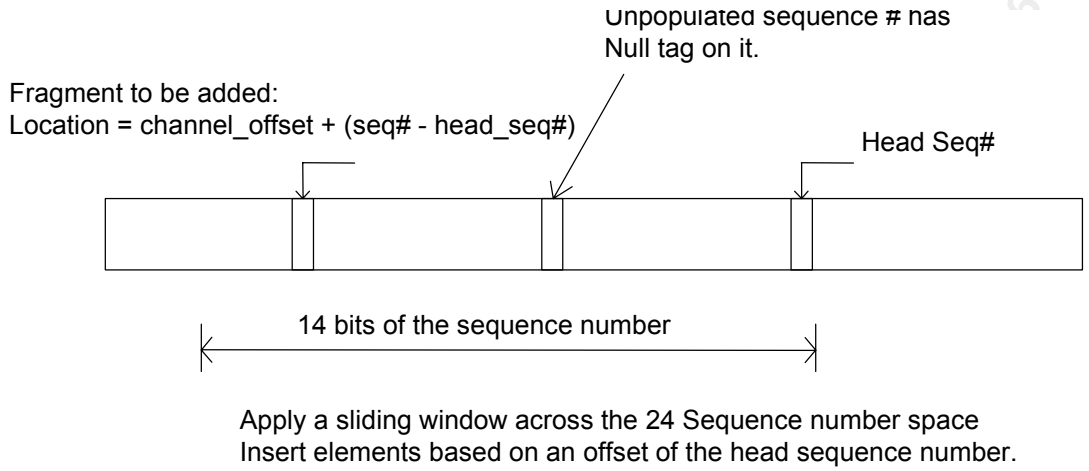
Size Comparison/Timers

The chunk buffer and re-sequencing structures are shared resources. To ensure that a multilink bundle or HDLC channel does not consume more than an allocated amount of resources the number of bytes in the bundle or channel is compared against a threshold (allocated bytes). If the threshold is exceeded, the datagram is discarded. The primary reasons for exceeding the threshold are loss of a link within a member bundle or a number of ML-FR DLCIs losing datagrams. The first situation would cause the re-sequencing engine to stall on the first lost datagram. Incoming fragments from other links would then build up and create a backlog of datagrams.

Re-sequencing List addition

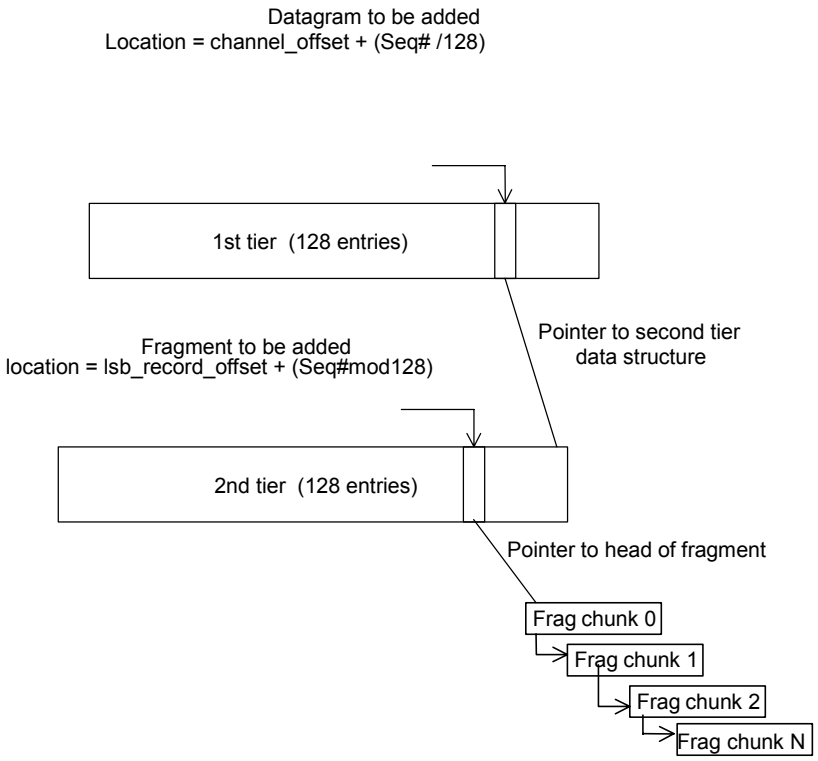
Datagrams that have not been discarded are entered in the re-sequencing list. The resequencing algorithm in FREEDM 84A1024 supports the worst case number of packets on a multilink bundle of T1/E1s that have experienced an intra skew delay of 100ms. To support that a subset of the 24-bit sequence number space is supported. Fourteen of the 24 bits are used for re-sequencing. All 12 bits are used when supporting 12 bit sequence numbers. On initialization, the Head Sequence number is set to the sequence number of the first fragment received. Subsequent sequence numbers are discarded if they are less than the Head Sequence number. Arriving datagrams are placed in the sliding window with an offset determined by distance (difference) between the sequence number at the head of the window and the current sequence number.

Figure 21 - The 14-bit sliding window used for re-sequencing



The sliding window (Figure 21) is realized as a two tiered data structure (Figure 22). This is done to reduce the memory required to support 16K simultaneous multilink sessions. The initial tier is present for all multilink sessions. Secondary tiers are added and removed when needed. The number of second tiers is limited. Enough are provided to support the simultaneous resequencing on all multilink sessions.

Figure 22 - The elements in the Re-sequencing block



The incoming sequence number is compared with the expected sequence number (head + 1). If the two are equal, the datagram is in sequence. The end of packet marker is examined to determine if a complete frame/packet is available for transfer. This is signaled to the frame builder block. A session that was previously out-of-sequence may have a backlog of frames/packets ready for transfer once the in-sequence frame/packet is received. This is signaled to the frame assembly block.

If the sequence numbers do not align, and the multilink session was previously in sequence, a re-sequencing operation is triggered and the datagram is logically placed in the re-sequencing buffers.

The datagram is removed from the re-sequencing buffers when the re-sequencing operation has correctly re-sequenced the datagrams. These datagrams are passed to the frame builder of the ingress queue manager depending on the mode of transfer.

Frames/packets without sequence numbers use the same data structures to queue frames. However the re-sequencing and frame detection logic is not required. FRF12 fragmentation (single link sequencing for QOS reasons) and the potential equivalent for PPP are supported via the structures in place.

In order to preserve integrity of the data structures in the event of a soft error the addresses are protected by ECC capable of detecting 2 and correcting 1 error.

Frame building

Frame or packet transfers across the ANY-PHY interface require all the fragments of a frame/packet to be present and in sequence before the transfer can occur. The frame building block monitors incoming datagrams determines when a complete frame/packet has been received and is ready for transfer. Examining status fields associated with datagrams that are entered in the 14 bit-sliding window provides the necessary information. Multilink sessions that are in-sequence require the end-of-packet marker of incoming packets to be examined. When the frame builder detects the end of packet marker, the CI is sent to the ingress queue manager. This signals that a frame/packet is ready for transfer.

Out-of-sequence multilink sessions require the frame builder to rapidly parse the fragment entries in the data structure once the multilink session returns to in-sequence state. This is required as there may be a large number of fragments that are available for transmission once the session becomes in-sequence (i.e. the outstanding fragment arrives and completes the sequence). To support this, the frame builder maintains a block of status structures. Each block contains 128 status entries. This enables the frame builder to review a large number of fragments once the session is in sequence. If one or more complete frames are identified, the frame builder provides the associated connection identifier to the ingress queue and the number of frames available.

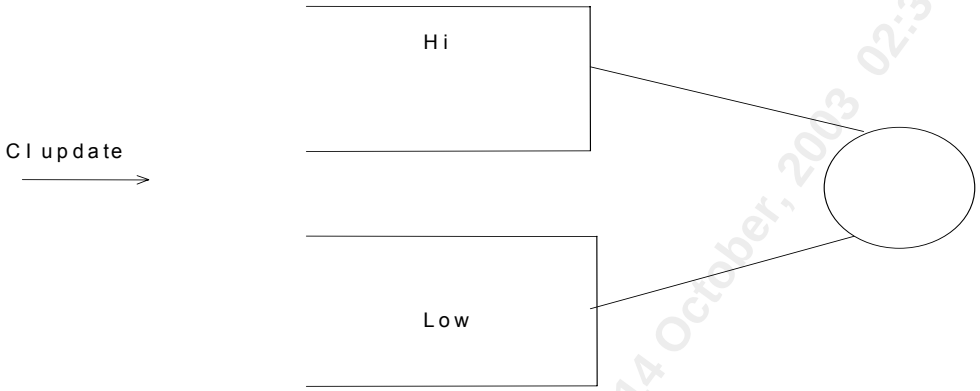
Frame/Fragment removal

The connection identifier selected by the ingress queue manager is used to extract the datagram at the head of the connection queue. If this is the last entry in a secondary tier, the re-sequencing data structure is returned to the free list of data structures. When the data is extracted, the corresponding status bits (EOP, Active, BECN, FECN, DE) are cleared. The address field is cleared and a Null pointer is placed in the location.

10.9.6. Ingress Queue manager (IQM-12)

The ingress queue manager (Figure 23) arbitrates between datagrams that are available to be sent. Datagram selection is based on the priority of the respective queue. The intent is to maximize the datagram transfers while ensuring that individual HDLC channels and connections receive adequate access to the ANY-PHY interface. It is not desirable to have a burst of traffic from a multilink bundle (due to re-sequencing) dominate the ANY-PHY interface at the expense of other HDLC channels that also have data to send.

Figure 23 - The Ingress Queue Manager block



The ingress queue manager supports arbitration between two queues. These are used to support two priorities. Each queue is a linked list of CIs that have data to transmit. When a datagram is formed, the re-sequencing block forwards a CI, to the ingress queue manager. If the CI is not on the list, the CI is added to the end of the linked list. The high priority queue is serviced before the low priority queue. The CI tag at the head of the selected queue is extracted and passed to the re-sequencing engine where it is used to extract the frame/fragment. If the CI has more datagrams to send (size $\neq$ 0) it is placed at the end of the queue.

10.9.7. Receive ANY-PHY Interface (RAPI-12)

The RAPI-12 contains a FIFO block for latency control as well as to segregate the APPI timing domain from the SYSCLK timing domain. The RAPI-12 contains the necessary logic to manage and respond to device polling from an upper layer device. The RAPI-12 also provides the upper layer device with status information on a per packet basis.

The RAPI-12 supports ANY-PHY Level-2, and ANY-PHY Level-3 modes of operation. When operating at 104 MHz the lower 8 bits of the data are active.

FIFO Storage and Control

The FIFO block temporarily stores ANY-PHY channel data during transfer across the Rx APPI. A separate storage element samples the 16-bit address prepend to associate the data in that FIFO with a specific ANY-PHY channel. This ANY-PHY channel ID is prepended in-band as the first word of every burst data transfer across the Rx APPI. In ANY-PHY Level-3 mode, the address prepend is appended on the first two bytes of the packet.

The writer controller provides a means for writing data into the FIFO. The reader controller provides a means of reading data out of the FIFO onto the Rx APPI. When selected to do so the reader controller will read the data out of the FIFO. To prevent from overloading the Rx APPI with several small bursts of data, the RAPI-12 automatically deselects after every burst transfer. This provides time for the upper layer device to detect an end of packet indication and possibly reselect a different FREEDM 84A1024 device without having to store the extra word or two which may have been output onto the Rx APPI during the time it took for deselection.

The RAPI-12 provides packet status information on the Rx APPI at the end of every packet transfer. The RAPI-12 asserts RERR at the end of packet reception (REOP high) to indicate that the packet is in error. The RAPI-12 may optionally be programmed to overwrite RXDATA[7:0] of the final word of each packet transfer (REOP is high) with the status of packet reception when that packet is erred (RERR is high). Overwriting of status information is enabled by setting the STATEN bit in the RAPI-12 control register.

Polling Control and Management

The RAPI-12 only responds to ANY-PHY channel polls, which match the device base address bits programmed in the RAPI-12 Base Address register. A positive poll response indicates that the FIFO is ready to be selected to transfer this data across the Rx APPI.

10.9.8. Transmit ANY-PHY Interface (TAPI-12)

The Transmit ANY-PHY Interface (TAPI-12) provides a low latency path for transferring data from the Transmit ANY-PHY Packet Interface (Tx APPI) to the TFRAG engine or the EQM. The TAPI-12 contains a FIFO block for latency control as well as to segregate the APPI timing domain from the SYSCLK timing domain. The TAPI-12 contains the necessary logic to manage and respond to ANY-PHY channel polling from an upper layer device.

The TAPI-12 supports ANY-PHY Level-2 and ANY-PHY Level-3. When operating at 104 MHz the lower 8 bits of the data are active.

FIFO Storage and Control

The FIFO block temporarily stores ANY-PHY channel data during transfer across the Tx APPI. TAPI-12 burst data transfers are transaction based on the writer side of the FIFO.

The first word of each burst transfer contains the address prepend field. A separate storage element samples the address prepend to associate the data with a specific ANY-PHY channel. The address prepend is compared to the base and range registers. The address prepend must correspond to an ANY-PHY channel that is supported by the FREEDM 84A1024 for the TAPI-12 to respond to the data transaction on the Tx APPI.

The writer controller provides a means for writing data from the Tx APPI into the FIFO. The whisper controller provides the ANY-PHY channel address of the data being written into the FIFO. As soon as the first word of data has been written into the FIFO, the whisper controller provides the ANY-PHY channel information for that data to the downstream block. The whisper controller will wait for acknowledgement and the reader controller is then requested to read the data from the FIFO. Once the reader controller has commenced the data transfer, the whisper controller will provide the ANY-PHY channel information for next data transfer received, if any.

The reader controller provides a means of reading data out of the FIFO. When the writer controller indicates that data has been written into the FIFO, the reader controller is permitted to read that data. The reader controller will then wait for a request for data from the downstream block. Because the reader controller reads data out of the FIFO in the order in which they were filled, the TFRAG block will request data for ANY-PHY channels in the order in which they were whispered.

Polling Control and Management

The TAPI-12 only responds to poll addresses, which are identified by the base and range address registers in the TAPI-12 Control registers. The TAPI-12 maintains a mirror image of the status of each channel FIFO in the EQM-12. The EQM-12 continuously reports the status of the 1024 FIFOs to the TAPI-12 and the TAPI-12 updates the mirror image accordingly. At the beginning of every data transfer across the Tx APPI, the TAPI-12 sets the mirror image status of the channel to "full". Only the TAPI-12 can cause the status to be set to "full" and only the EQM-12 can cause the status to be set to "space". In the event that both the TAPI-12 and the EQM-12 try to change the mirror image status of a particular channel simultaneously, the TAPI-12 takes precedence.

10.9.9. Transmit Fragmentor (TFRAG)

Datagrams are transferred from the upstream device to the FREEDM 84A1024 via the ANY-PHY interface. The transmit fragmentor fragments (if required) the packet, encapsulates the fragments with a sequence number (in multilink or fragmentation situations), assigns the datagram to an HDLC channel and segments the datagram into chunks for storage in the external SDRAM.

When supporting a multilink bundle, the address prepend and the connection identifier that is provided on the ANY-PHY interface are used to index the appropriate sequence number and an index to the HDLC channels associated with the multilink bundle. The sequence number and additional header bits (B, E, and COS) are appended to arriving datagrams. The datagram is assigned to an HDLC channel in the multilink bundle. HDLC channel assignment is based on the current occupancy of the HDLC channels in a multilink bundle. The datagram is assigned to the HDLC channel with the lowest number of bytes in the channel queue.

Compressed PPP headers are detected by the TFRAG. The TFRAG is capable of appending sequence numbers onto multilink packets with compressed headers.

On a per HDLC channel basis these datagrams are segmented into chunks and are stored in an external SDRAM memory. A HDLC chunk will only consist of data from one packet/frame. Segmented data is encapsulated (Figure 24) to form a 36 byte storage element. The encapsulation contains the next address pointer, the size and a local integrity check that covers the address field. The next address pointer is used to create a linked list of chunks that comprise a datagram.

The address indicates where the next chunk of the datagram is located in the external memory. This effectively links the chunks of a datagram in external memory. In the last data chunk, the next address is used to link to the start of the next datagram. The size field is used to indicate how many of the data bytes are actually valid, as the last chunk may not be completely full. The abort is used to trigger an HDLC abort. If an unexpected TSX error occurred during an ANY-PHY transfer or if the upstream device asserts the TERR signal, the abort is set.

The encapsulated data chunk, and an address pointer are passed to the DRAMC controller for storage in external SDRAM. The address pointer is contained in the HDLC channel record and points to the memory location that is placed in the next address pointer field of the previous data chunk for a given datagram. The initial chunk of a datagram is stored at an address location, (starting address of the datagram).

An address cache is used to hold addresses that can be used for next pointer values. When a chunk is encapsulated, the HDLC channel record will fetch, from the local cache, another address that can serve as the next address for the following data chunk in the datagram. The cache needs to be replenished, this is achieved by requesting, from the DRAMC, a set of new addresses after a threshold in the Cache has been crossed.

In order to preserve the address pointers in the presence of soft errors an ECC code is used to detect 2 errors and correct 1 error.

Figure 24 - Encapsulated Chunk Structures

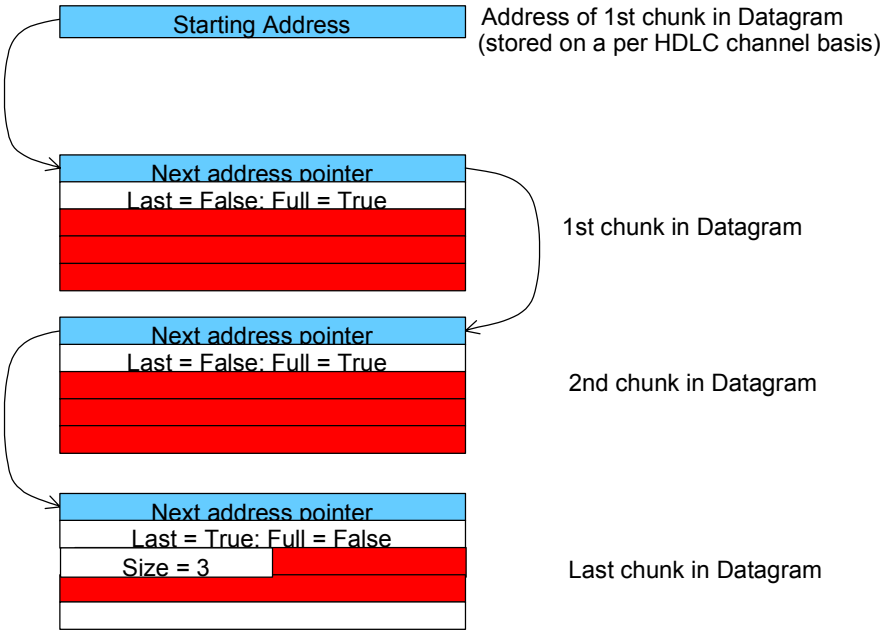
a) Encapsulated Chunk Structure (Full = True)

Byte 1	Byte 0	ECC(8)	L	F	A	0	NXT_CHUNK_PTR(19)		
Byte 7	Byte 6	Byte 5	Byte 4				Byte 3		Byte 2
Byte 13	Byte 12	Byte 11	Byte 10				Byte 9		Byte 8
Byte 19	Byte 18	Byte 17	Byte 16				Byte 15		Byte 14
Byte 25	Byte 24	Byte 23	Byte 22				Byte 21		Byte 20
Byte 31	Byte 30	Byte 29	Byte 28				Byte 27		Byte 26

b) Encapsulated Chunk Structure (Full = False)

Byte 0	Size	ECC(8)	L	F	A	00	NXT_CHUNK_PTR(19)		
Byte 6	Byte 5	Byte 4	Byte 3				Byte 2		Byte 1
Byte 12	Byte 11	Byte 10	Byte 9				Byte 8		Byte 7
Byte 18	Byte 17	Byte 16	Byte 15				Byte 14		Byte 13
Byte 24	Byte 23	Byte 22	Byte 21				Byte 20		Byte 19
Byte 30	Byte 29	Byte 28	Byte 27				Byte 26		Byte 25

Figure 25 - Linked list data structure of a Datagram



Egress Queue Manager (EQM-12)

Managing the ANY-PHY channel status, pushing the status to the TAPI-12, accepting transfer requests from the partial packet processor and arbitrating between the requests are the key tasks of the egress queue manager. Segmented datagrams are placed into external memory by the TFRAG block. The number of data bytes in chunk are added to the ANY-PHY channel size counter. The size is compared against a threshold. An ANY-PHY channel size that exceeds the threshold will cause the EQM-12 to push a status message to the TAPI-12 indicating the ANY-PHY channel is full and will not be accepting any more frames. The EQM-12 maintains the status of all 1024 ANY-PHY channels including the 42 multilink bundles and the 1024 HDLC channels.

The partial packet processor requests chunks, as memory becomes available. The egress queue manager determines the address of the chunk to be transferred to the partial packet processor. The EQM-12 updates the HDLC and ANY-PHY channel context status and pushes the status of the ANY-PHY channel to the TAPI-12. ANY-PHY channel status is determined by comparing the size of the ANY-PHY channel to the ANY-PHY channel threshold. The two level feedback mechanism is used to avoid starvation of the HDLC channels. The thresholds are programmable and support a number of different bandwidths (DS0, nxDS0, T1, E1, nxT1, nxE1, DS3) and ensure that starvation is avoided.

10.9.10. CB_DRAMC

The CB_DRAMC controls access to/from the Chunk Buffer SDRAM interface present on FREEDM 84A1024. The external SDRAMS provide buffer storage for chunks and addresses pointing to the chunks. The CB_DRAMC block supports a 48 bit wide SDRAM interface operating at 100 MHz. Refresh, bank switching, providing precharge and bus management are functions that reside in the CB_DRAMC. Figure 26 shows the configuration for the external SDRAMs that comprise the Chunk Buffer.

10.9.11. RS_DRAMC

The RS_DRAMC controls access to/from the Re-sequencing SDRAM interface present on FREEDM 84A1024. The external SDRAMS provide CI lookup information as well as pointers used in the resequencing operation. The RS_DRAMC block supports a 32 bit wide SDRAM interface operating at 100 MHz. Refresh, bank switching, providing precharge and bus management are functions that reside in the RS_DRAMC. Figure 27 shows the configuration for the external SDRAMs that comprise the Re-Sequencing buffer.

Figure 26 - DRAM configuration for the Chunk Buffer Interface

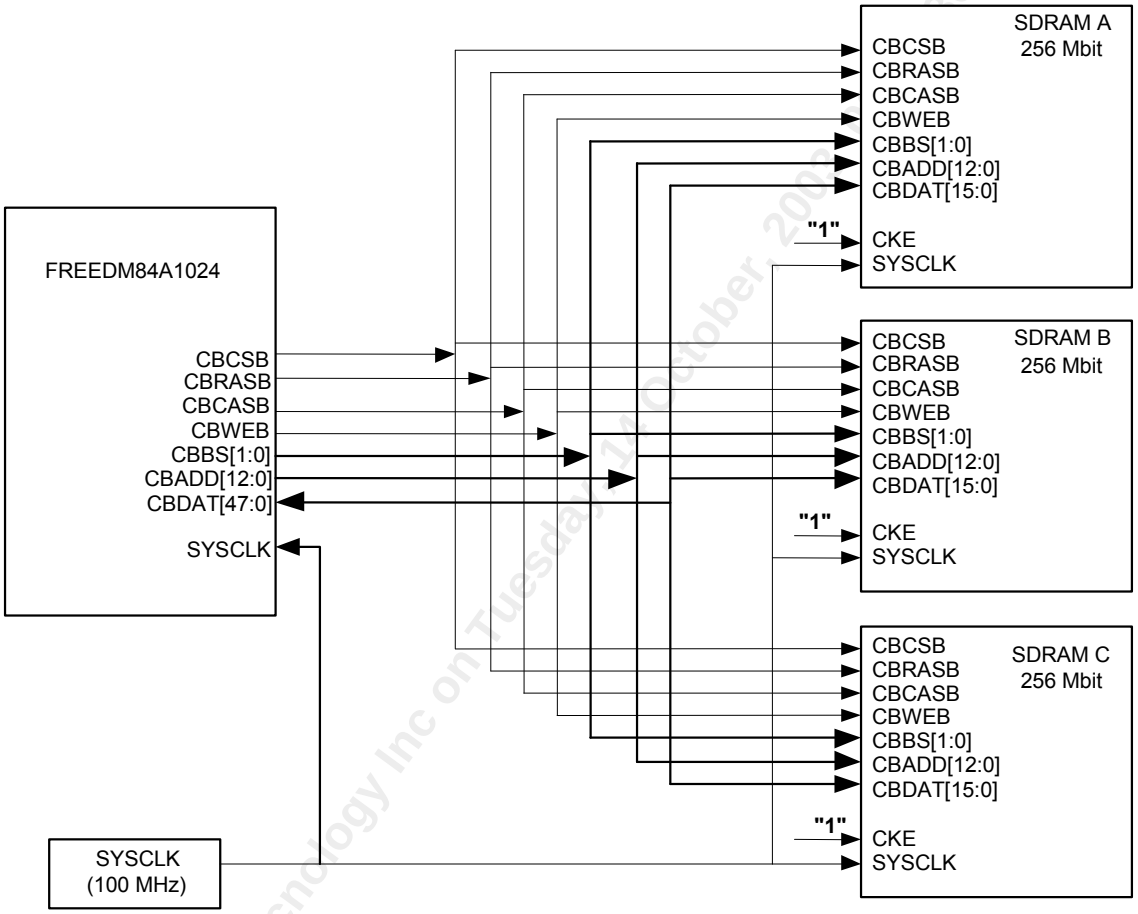
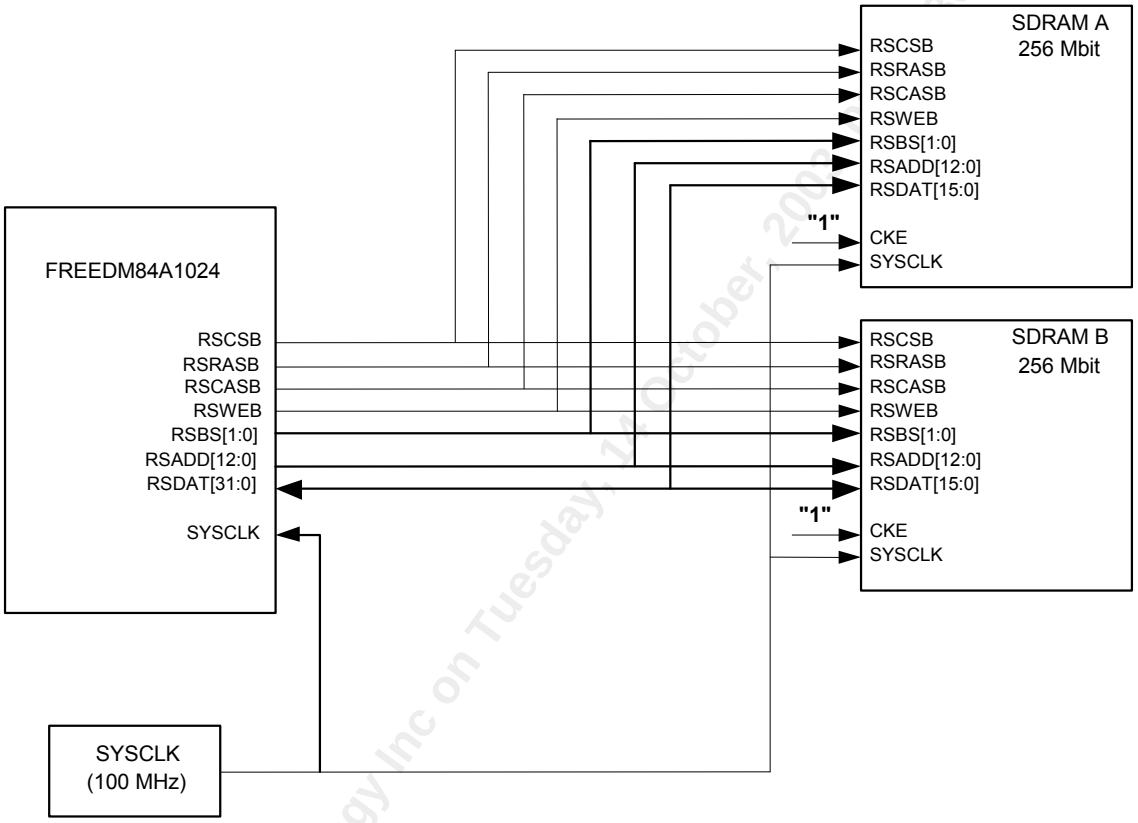


Figure 27 - DRAM configuration for the Re-Sequencing Memory Interface



10.9.12. SRAMC

The external context memory holds data that needs to be accessed by a number of internal blocks. The role of the SRAMC block is to arbitrate these accesses. The Connection context memory supports the frame building block, TFRAG, and IQM-12.

The SRAMC supports glueless access to 1, 2 or 4 banks of Pipelined ZBT-compatible1 or Standard SRAM. When FREEDM 84A1024 is configured to interface to Standard or ZBT-compatible SSRAM, CCBSELB is the inverse of CCADD[16]. CCBSELB and CCADD[16:17] are used to select 4 banks when 64Kx36 devices are used (see Figure 28).

1 The ZBT-compatible SRAM family includes

- ZBT, short for Zero Bus Turnaround, manufactured by IDT, Micron and Motorola,
- NoBL, short for No Bus Latency, manufactured by Cypress, and
- N*t* , short for No *t*urnaround, manufactured by Samsung

Figure 28 - 4 Bank Configuration for 8 MB of ZBT or Standard SSRAM

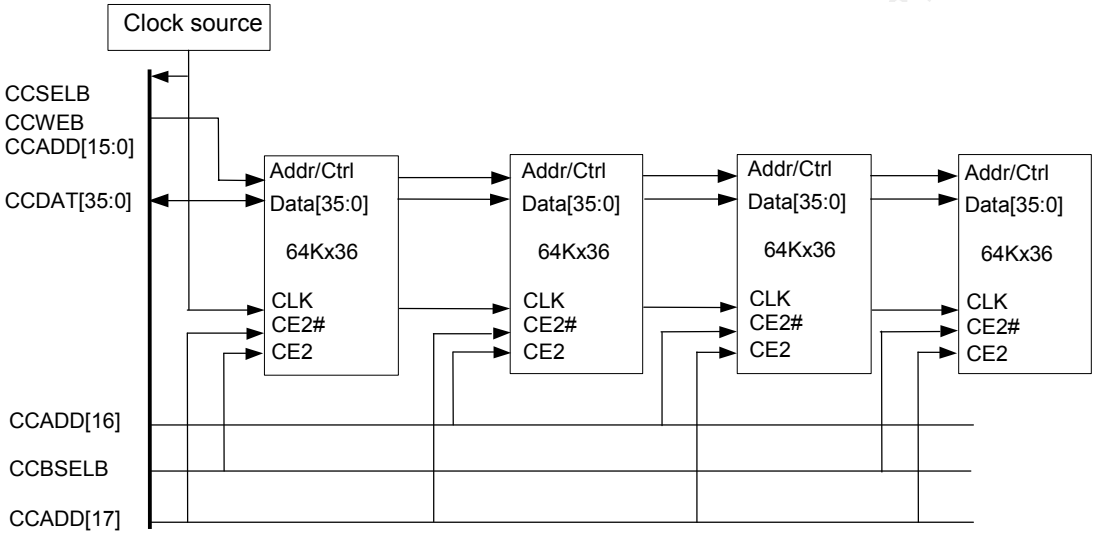


Figure 29 -2 Banks Configuration for 8 M bits of ZBT-compatible or Standard SSRAM

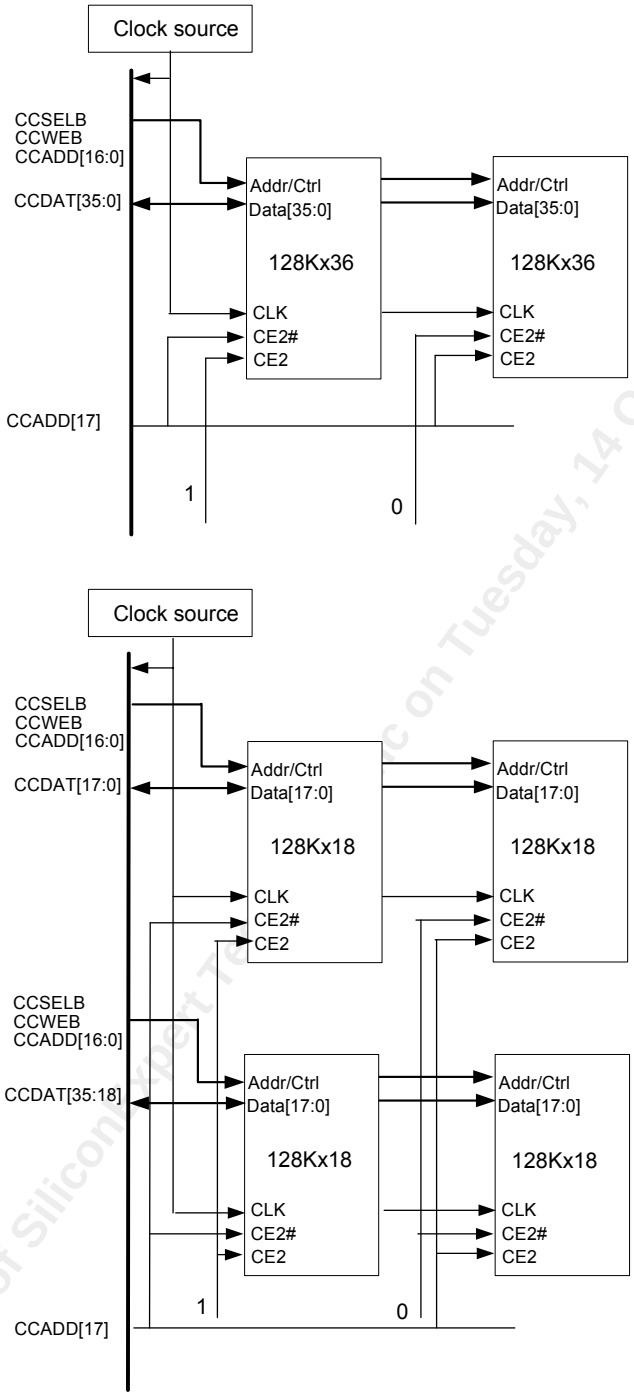
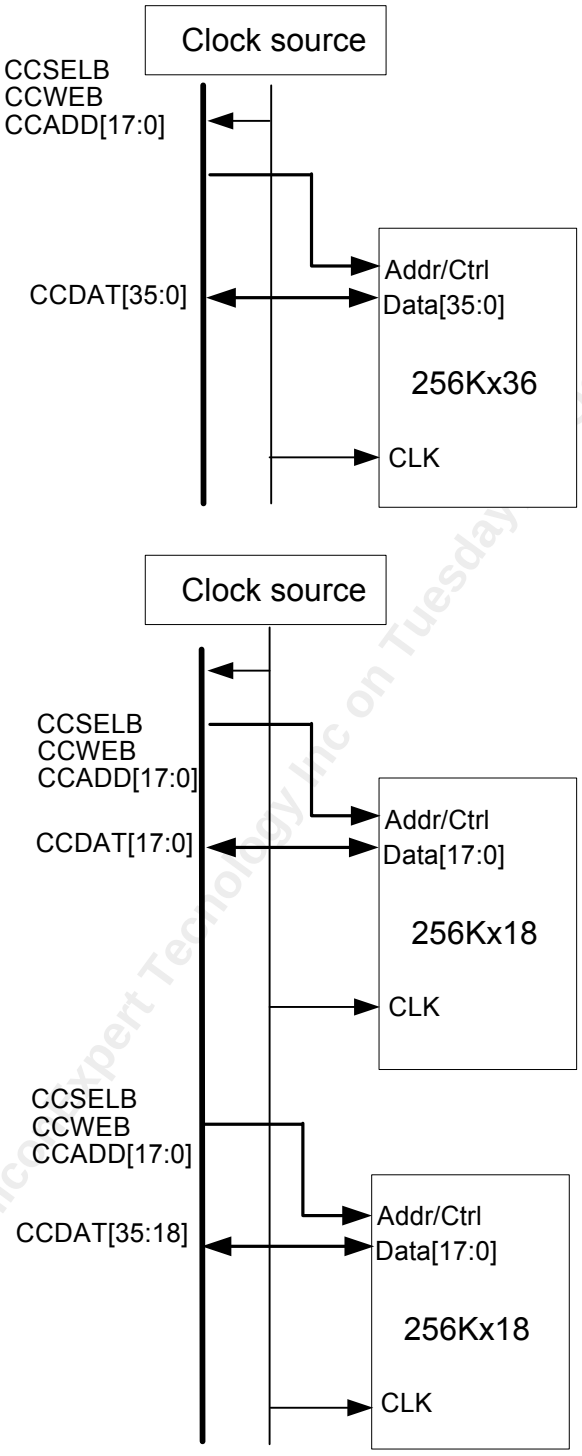


Figure 30 1 Bank Configuration for 8 M bits of ZBT or Standard SSRAM



10.9.13. Transmit HDLC Processor (THDL-12)

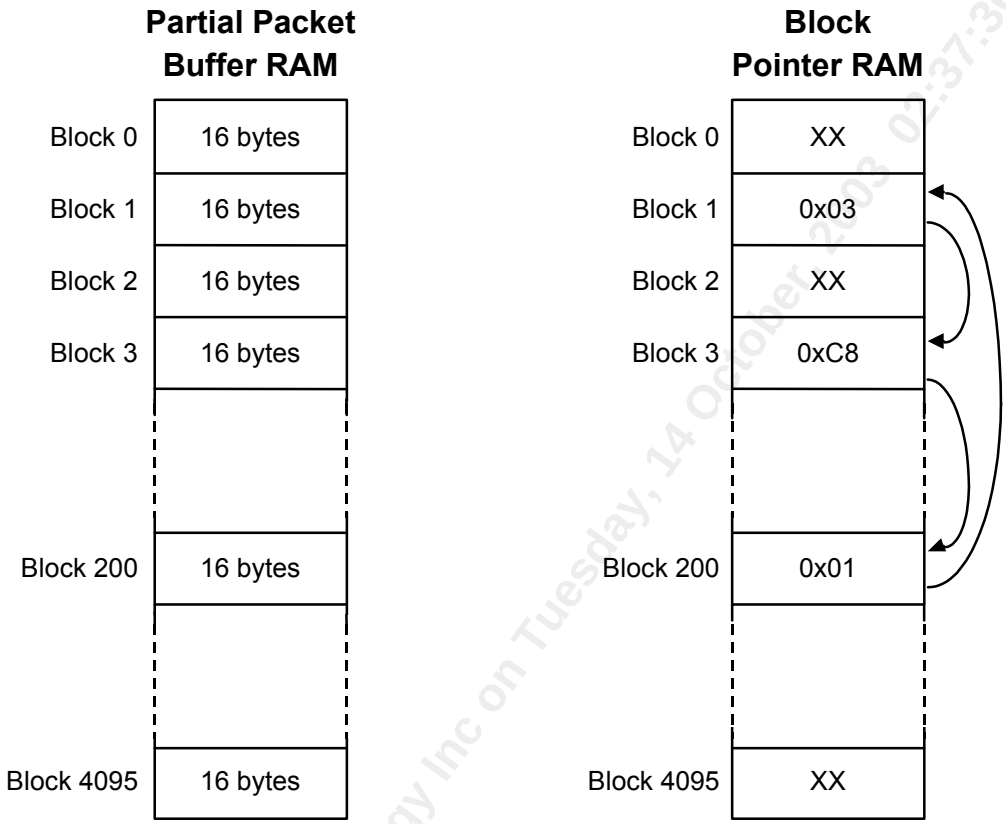
The HDLC processor is a time-slice state machine that can process up to 1024 independent HDLC channels. The state vector and provisioning information for each HDLC channel is stored in a RAM. Whenever the TCAS-12 requests data, the appropriate state vector is read from the RAM, processed and finally written back to the RAM. The HDLC state-machine can be configured to perform flag insertion, bit stuffing and CRC generation. The HDLC processor requests data from the partial packet processor whenever a request for HDLC channel data arrives. However, the HDLC processor does not start transmitting a packet until the entire packet is stored in the HDLC channel FIFO or until the FIFO free space is less than the software programmable limit. If an HDLC channel FIFO under-runs, the HDLC processor aborts the packet, and generates an interrupt.

The configuration of the HDLC processor is accessed using indirect channel read and write operations. When an indirect operation is performed, the information is accessed from RAM during a null clock cycle inserted by the TCAS-12 block. Writing new provisioning data to an HDLC channel resets the channel's entire state vector.

Transmit Partial Packet Buffer Processor

The partial packet buffer processor controls the 64 Kbyte partial packet RAM which is divided into 16 byte blocks. A block pointer RAM is used to chain the partial packet blocks into circular HDLC channel FIFO buffers. Thus, non-contiguous sections of RAM can be allocated in the partial packet buffer RAM to create an HDLC channel FIFO. Figure 31 shows an example of three blocks (blocks 1, 3, and 200) linked together to form a 48 byte HDLC channel FIFO. The three pointer values would be written sequentially using indirect block write accesses. When an HDLC channel is provisioned within this FIFO, the state machine can be initialized to point to any one of the three blocks.

Figure 31 - Partial Packet Buffer Structure



The partial packet buffer processor is divided into three sections: reader, writer and roamer. The roamer is a time-sliced state machine which tracks each HDLC channel's FIFO buffer free space and signals the writer to service a particular channel. The writer requests data from the EQM-12 block and transfers packet data from the EQM-12 to the associated HDLC channel FIFO. The reader is a time-sliced state machine that transfers the HDLC information from an HDLC channel FIFO to the HDLC processor in response to a request from the HDLC processor. If a buffer under-run occurs for an HDLC channel, the reader informs the HDLC processor and purges the rest of the packet. If a buffer overflow occurs for an HDLC channel (this can only happen if EQM-12 disregards the requests), the THDL-12 overwrites the FIFO contents resulting in data corruption on that particular HDLC channel. When an underflow or an overflow occurs, an interrupt is generated and the cause of the interrupt may be read via the interrupt status register using the microprocessor interface.

The writer and reader determine empty and full FIFO conditions using flags. Each block in the partial packet buffer has an associated flag. The writer sets the flag after the block is written and the reader clears the flag after the block is read. The flags are initialized (cleared) when the block pointers are written using indirect block writes. The reader declares an HDLC channel FIFO under-run whenever it tries to read data from a block without a set flag.

The FIFO algorithm of the partial packet buffer processor is based on per- HDLC channel software programmable transfer size and free space trigger level. Instead of tracking the number of full blocks in an HDLC channel FIFO, the processor tracks the number of empty blocks, called free space, as well as the number of end of packets stored in the FIFO. Recording the number of empty blocks instead of the number of full blocks reduces the amount of information the roamer must store in its state RAM.

The partial packet roamer records the FIFO free space and end-of-packet count for all HDLC channel FIFOs. When the reader signals that a block has been read, the roamer increments the FIFO free space and sets a per- HDLC channel request flag if the free space is greater than the hungry or starving threshold. The roamer pushes this status information to the EQM to indicate that it can accept at least one transfer of data. The roamer also decrements the end-of-packet count when the reader signals that it has passed an end of a packet to the HDLC processor. The roamer listens to control information from the EQM-12 to decide which HDLC channel FIFO requests data from the EQM block. The roamer informs the partial packet writer of the HDLC channel FIFO to process and the FIFO free space. The writer sends a request for data to the EQM-12 block, writes the response data to the HDLC channel FIFO, and sets the block full flags. The writer reports back to the roamer the number of blocks and end-of-packets transferred. The maximum amount of data transferred during one request is set by XFER.

The roamer round-robins between all HDLC channels FIFOs and pushes the status to the EQM-12 block. The status consists of two pieces of information: (1) is there space in the HDLC channel FIFO for at least 32 bytes of data, and (2) is this channel FIFO at risk of underflowing.

The configuration of the HDLC processor is accessed using indirect channel read and write operations as well as indirect block read and write operations. When an indirect operation is performed, the information is accessed from RAM during a null clock cycle identified by the TCAS-12 block. Writing new provisioning data to an HDLC channel resets the entire state vector.

10.9.14. Transmit Channel Assignor (TCAS-12)

The Transmit Channel Assignor block (TCAS-12) processes up to 1024 HDLC channels. Data for all HDLC channels is sourced from a single byte-serial stream from the Transmit HDLC Controller / Partial Packet Buffer block (THDL-12). The TCAS-12 demultiplexes the data and assigns each byte to any one of 84 links. When sending data to the SBI block, each link may be configured to support channelized T1/J1/E1 traffic, unchannelized DS3 traffic or unframed traffic at T1/J1, E1, DS3 or Fractional DS3/E3 rates. When sending data to the TD outputs, links 0, 4 and 8 support unchannelized data at arbitrary rates up to 52 Mbps. Each link is independent and has its own associated clock.

The 84 TCAS links have a fixed relationship to the SPE and tributary numbers on the SBI ADD BUS as shown in the following table.

Table 12 - SBI-SPE Tributary to TCAS Link Mapping

SPE No.	SBI Trib. No.	TCAS Link No.	SPE No.	SBI Trib. No.	TCAS Link No.	SPE No.	SBI Trib. No.	TCAS Link No.
1	1	0	2	1	4	3	1	8
1	2	12	2	2	16	3	2	20
1	3	24	2	3	28	3	3	32
●								●
●								●
●								●
1	28	324	2	28	328	3	28	332

As shown in the table above, TCAS links 0, 4 and 8 are mapped to tributary 1 of SPE 1, 2 and 3 respectively. These links may be configured to operate at DS3 rate. (They may also be configured to output data to the TD[0,4,8] outputs at rates up to 52 Mbps.) For each of these high-speed links, the TCAS-12 provides a 4 byte FIFO. For the remaining links (TCAS links 12 to 332 mapped to tributaries 2 to 28 of each SPE), the TCAS-12 provides a single byte holding register. In the event where multiple links are in need of data, TCAS-12 requests data from upstream blocks on a fixed priority basis with link 0 having the highest priority and link 332 the lowest.

It should be noted that for every SBI/SPE used as a serial link, the SBI/SPE must be disabled on the SBI Bus interface and visa versa.

Links containing a T1/J1 or an E1 stream may be channelized. Data at each time-slot can be independently assigned to be sourced from a different HDLC channel. The position of T1/J1 and E1 framing bits/bytes is identified by frame pulse. With knowledge of the transmit link and time-slot identity, the TCAS-12 performs a table look-up to identify the HDLC channel from which a data byte is to be sourced.

Links containing a DS3 stream are unchannelized, in which case, all data bytes on the link belong to one HDLC channel. The TCAS-12 performs a table look-up to identify the HDLC channel to which a data byte belongs using only the outgoing link identity, as no time-slots are associated with unchannelized links. Links may additionally be configured to operate in an unframed "clear channel" mode, in which case the FREEDM 84A1024 will output HDLC data in all bit positions, including those normally reserved for framing information. Links so configured operate as unchannelized regardless of link rate and the TCAS-12 performs a table lookup using only the link number to determine the associated HDLC channel.

10.9.15. SBI Inserter

The SBI transmit circuitry processes data for the three Synchronous Payload Envelopes (SPEs) conveyed on the SBI ADD BUS. It receives data bytes from the transmit channel assignor and inserts it into the SBI ADD BUS. The SBI Insert block may be configured to enable or disable transmission of individual tributaries on to the SBI ADD bus. Individual tributaries may also be configured to operate in framed or unframed mode.

10.9.16. Performance Monitor

The Performance Monitor block (PM) contains the HDLC channel counters plus a series of error registers. The HDLC channel counters include:

- Bytes received per HDLC channel
- Bytes transmitted per HDLC channel
- Total datagrams received
- Total datagrams transmitted
- Bytes discarded from excess small datagrams
- Bytes discarded of Chunk Buffer allocation exceeded events

In addition a number of error conditions are tracked on a per HDLC channel basis:

- Erred HDLC Frames
- Tx HDLC framing aborts
- Rx HDLC framing aborts
- Small Datagrams discarded events
- Chunk Buffer allocation exceeded events

Additionally, the PM-12 block contains global error counters track performance of various aspects of the FREEDM 84A1024.These include:

- Number of lost fragment events.
- Partial Packet overruns
- Partial Packet underruns
- Number of tiny Packets (min HDLC length)
- Number of excessive fragments per packet/frame events
- Number of unexpected sequence number events
- Number of bytes received with non-octet aligned errors
- Number of bytes received with MRU exceeded

- Number of bytes received with abort errors
- Number of bytes received with FCS errors
- Number of bytes received with partial packet overrun
- Number of bytes received with unexpected sequence number
- Number of bytes received with unsupported header format

10.9.17. Digital Delay Lock Loop (DDLL)

The DLL is used to minimize output delay on all external RAMs. The DLL measures the phase difference between the external clock and a reference clock and generates an internal clock which reduces the phase difference between the external clock and the reference clock to zero.

10.9.18. JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The FREEDM 84A1024 identification code is 373880CD hexadecimal.

10.9.19. Microprocessor Interface

The FREEDM 84A1024 supports microprocessor access to an internal register space for configuring and monitoring the device. All registers are on 32 bit boundaries. Address Bit 12 on all registers must be set to 0. The registers are described in Table 13.

Table 13 - Normal Mode Microprocessor Accessible Registers Memory Map

Address	Register
0x000	F84 Master Reset and Control
0x004	F84 Master High Priority Interrupt Enable
0x008	F84 Master High Priority Interrupt Status
0x00C	F84 Master Clock / Frame Pulse Activity Monitor and Accumulation Trigger
0x010	F84 Reserved
0x014	F84 Master Line Loopback
0x018	F84 Master Low Priority Interrupt Enable
0x01C	F84 Master Low Priority Interrupt Status
0x020-0x044	F84 Reserved
0x048	F84 SBI DROP BUS Master Configuration
0x04C	F84 SBI ADD BUS Master Configuration
0x050-0x064	F84 Reserved
0x068	DLL Configuration
0x06C	DLL Vernier Control
0x070	DLL Delay Tap Status

Address	Register
0x074	DLL Control Status
0x078 – 0x0FC	DLL Reserved
0x100	RCAS Indirect Context RAM Link Select
0x104	RCAS Indirect Context RAM Link Data
0x108	RCAS Indirect Channel Provision RAM TRIB Select
0x10C	RCAS Indirect Channel Provision RAM Time Slot and control Select
0x110	RCAS Indirect Channel Provision RAM Channel Data and Loopback enable.
0x114	RCAS Serial Link Select
0x118 – 0x1FC	RCAS Reserved
0x200	RHDL Indirect Channel Select
0x204	RHDL Indirect Channel Data Register #1
0x208	RHDL Indirect Channel Data Register #2
0x20C	RHDL Reserved
0x210	RHDL Indirect Block Select
0x214	RHDL Indirect Block Data Register
0x218 – 0x21C	RHDL Reserved
0x220	RHDL Configuration
0x224	RHDL Maximum Packet Length
0x228 – 0x23C	RHDL Reserved
0x240 – 0x37C	RHDL Reserved
0x380	THDL Indirect Channel Select
0x384	THDL Indirect Channel Data #1
0x388	THDL Indirect Channel Data #2
0x38C	THDL Indirect Channel Data #3
0x390	THDL Indirect Channel Data Register #4
0x394	THDL Indirect Channel Data Register #5
0x398	THDL Indirect Channel Data Register #6
0x39C	THDL Reserved
0x3A0	THDL Indirect Block Select
0x3A4	THDL Indirect Block Data
0x3A8 – 0x3AC	THDL Reserved
0x3B0	THDL Configuration
0x3B4 – 0x3BC	THDL Reserved
0x3C0 – 0x3FC	THDL Reserved
0x400	TCAS Indirect Context RAM Link Select
0x404	TCAS Indirect Context RAM Link Data
0x408	TCAS Indirect Channel Provision RAM TRIB Select
0x40C	TCAS Indirect Channel Provision RAM Timeslot and Control Select.
0x410	TCAS Indirect Channel Provision RAM Channel Data
0x414	TCAS Serial Link Select
0x418	TCAS Idle Time-slot Fill Data

Address	Register
0x41C - 0x508	TCAS Reserved
0x50C – 0x57C	TCAS Reserved
0x580	RAPI Control Register
0x584	RAPI Device Base Address Register
0x588	RAPI Channel Base Address Register
0x58C	RAPI Status Register
0x590 – 0x5BC	RAPI Reserved
0x5C0	SBI EXTRACT Control
0x5C4 – 0x5CC	SBI EXTRACT Reserved
0x5D0	SBI Reserved
0x5D4	SBI EXTRACT Tributary Indirect Access Address
0x5D8	SBI EXTRACT Reserved
0x5DC	SBI EXTRACT Tributary Indirect Access Data
0x5E0	SBI EXTRACT SBI1 SPE Configuration Register
0x5E4 – 0x5FC	SBI EXTRACT Reserved
0x600	TAPI Control
0x604	TAPI Indirect Channel Provisioning
0x608	TAPI Indirect Channel Data Register
0x60C	TAPI Reserved Register
0x610	TAPI Status Register
0x614	TAPI Base Address Register
0x618	TAPI Range Address Register
0x61C – 0x63C	TAPI Reserved
0x640 – 0x67C	TAPI Reserved
0x680	SBI INSERT Control
0x684 – 0x688	SBI INSERT Reserved
0x68C	SBI INSERT T1 Frame Pulse Offset
0x690	SBI INSERT E1 Frame Pulse Offset
0x694	SBI INSERT Tributary Indirect Access Address
0x698	SBI INSERT Reserved
0x69C	SBI INSERT Tributary Indirect Access Data
0x6A0	SBI INSERT SBI1 SPE Configuration Register
0x6A4 – 0x7FC	SBI INSERT Reserved
0x800	Memory Port Control
0x804 – 0x810	Memory Write Data (Burstable)
0x814-0x818	Memory Write Data Overflow (Burstable)
0x81C-0x828	Memory Read Data (Burstable)
0x82C-0x830	Memory Read Data Overflow (Burstable)
0x834-0x880	BUMP Reserved
0x884	Unexpected SN Register CI (USNCI)

Address	Register
0x888	Lost SN CI (LSNCI)
0x88C	SRAM Parity Error Address (SPERRADD)
0x890	Excessive number of Fragments CI (ENFCI)
0x894-0x8FC	BUMP Reserved
0x900	CB_DRAMC Status Register
0x904	CB_DRAMC_COECCE Register
0x908	CB_DRAMC_UNCOECCE Register
0x90C-0x914	CB_DRAMC Reserved
0x918	RS_DRAMC Status Register
0x91C	RS_DRAMC_COECCE Register
0x920	RS_DRAMC_UNCOECCE Register
0x924-0x99C	DRAM Reserved
0x9A0	BIST Controller
0x9A4	BIST Enable
0x8A8	BIST Result
0x9AC	BIST End
0x9B0	EXSBI BIST ERROR
0x9B4	INSBI BIST ERROR
0x9B8	RCAS-12 BIST ERROR
0x9BC	TCAS-12 BIST ERROR
0x9C0	RHDL-12 BIST ERROR
0x9C4	THDL-12 BIST ERROR
0x9C8	PM-12 BIST ERROR
0x9CC	RFRAG BIST ERROR
0x9D0	TFRAG BIST ERROR
0x9D4	RS_DRAMC BIST ERROR
0x9D8	CB_DRAMC BIST ERROR
0x9DC	IQM-12 BIST ERROR
0x9E0	EQM-12 BIST ERROR
0x9E4	FRMBLD BIST ERROR
0x9E8	RAPI-12 BIST ERROR
0x9EC	TAPI-12 BIST ERROR
0x9F0-0xEFF	Unused

11. Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the FREEDM 84A1024.

Notes on Normal Mode Register Bits

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. Except where noted, all configuration bits that can be written into can also be read back. This allows the processor controlling the FREEDM 84A1024 to determine the programming state of the block.

3. Writable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect FREEDM 84A1024 operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the FREEDM 84A1024 operates as intended, reserved register bits must only be written with their default values or defined setup values. Similarly, writing to reserved registers should be avoided.

6. The term “high” may be used to describe logic 1 and “low” may be used to describe logic 0.

11.1. Microprocessor Accessible Registers

For each register description below, the hexadecimal register number indicates the address in the FREEDM 84A1024 when accesses are made using the external microprocessor.

Note

These 32-bit registers are not byte addressable. Writing to any one of these registers modifies all bits in the register.

Register 0x000 : F84 Master Reset and Control

Bit	Type	Function	Default
Bit 31 To Bit 15		Unused	X
Bit 14	R/W	RESET	0
Bit 13	R/W	SRAMM1	0
Bit 12	R/W	SRAMM0	0
Bit 11	R	DTYPE[3]	1
Bit 10	R	DTYPE[2]	0
Bit 9	R	DTYPE[1]	0
Bit 8	R	DTYPE[0]	0
Bit 7	R	ID[7]	0
Bit 6	R	ID[6]	0
Bit 5	R	ID[5]	0
Bit 4	R	ID[4]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	1
Bit 0	R	ID[0]	1

This register provides software reset capability, device ID information and SRAM configuration setup.

RESET

The RESET bit allows the FREEDM 84A1024 to be reset under software control. If the RESET bit is a logic one, the entire FREEDM 84A1024, except the microprocessor interface, is held in reset. All registers are reset to their default values and some memories are set to their default values (for specific memory operation refer to memory descriptions). This bit is not self-clearing. Therefore, a logic zero must be written to bring the FREEDM 84A1024 out of reset. Holding the FREEDM 84A1024 in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset.

Note

Unlike the hardware reset input (RSTB), RESET does not force the FREEDM 84A1024's microprocessor interface pins tristate. RESET causes all registers to be set to their default values and forces the APPI outputs tristate.

SRAMM[1:0]

The SRAM Mode bits describe the choice of SSRAM used for the Connection Context (CC) external memory.

Table 14 - Memory mode Configuration

SRAMM[1:0]	Configuration
00	Standard SRAM
01	Reserved
10	ZBT-like SRAM
11	Reserved

DTYPE[3:0]:

The Device Type bits (DTYPE[3:0]) allow software to identify the device as the FREEDM 84A1024 member of the FREEDM family of products.

ID[7:0]:

The Device ID bits (ID[7:0]) allow software to identify the version level of the FREEDM 84A1024.

Register 0x004 : FREEDM 84A1024 Master High Priority Interrupt Enable

Bit	Type	Function	Default
Bit 31 To Bit 21		Unused	X
Bit 20	R/W	SBIC1FPSE	0
Bit 19	R/W	SDGMDE	0
Bit 18	R/W	CBAEXE	0
Bit 17	R/W	Reserved	0
Bit 16	R/W	Reserved	0
Bit 15	R/W	UNSUPHE	0
Bit 14	R/W	BADSIZEE	0
Bit13	R/W	RSFPPEE	0
Bit 12	R/W	EFPPEE	0
Bit 11	R/W	IFPPEE	0
Bit 10	R/W	DLLE	0
Bit 9	R/W	SBIPARI	0
Bit 8	R/W	TXCHQOVRE	0
Bit 7	R/W	CFOVRE	0
Bit 6	R/W	TPRTYE	0
Bit 5	R/W	TFOVRE	0
Bit 4	R/W	TFUDRE	0
Bit 3	R/W	SRAMPE	0
Bit 2	R/W	UECCRSE	0
Bit 1	R/W	UECCCBE	0
Bit 0	R/W	RFOVRE	0

This register provides interrupt enables for various events detected or initiated by the FREEDM 84A1024. Each interrupt enable bit corresponds to the equivalent bit in the Master High Priority Interrupt Status register. All interrupt enable bits are active high. When high, interrupts are enabled. When low, interrupts are masked. While interrupts are masked the status bit in the status register may still be polled to detect the error event. Enabled High priority interrupts cause the INTHIB interrupt pin to be asserted.

Reserved:

The Reserved bit must be set to 0 for correct operation of the FREEDM 84A1024 device.

Register 0x008 : F84 Master High Priority Interrupt Status

Bit	Type	Function	Default
Bit 31 To Bit 21		Unused	X
Bit 20	R/W	SBIC1FPSI	X
Bit 19	R/W	SDGMDI	0
Bit 18	R/W	CBAEXI	0
Bit 17	R/W	Reserved	X
Bit 16	R/W	RST_DONEI	0
Bit 15	R/W	UNSUPHFI	0
Bit 14	R/W	BADSIZEI	0
Bit13	R/W	RSFPPEI	0
Bit 12	R/W	EFPPEI	0
Bit 11	R/W	IFPPEI	0
Bit 10	R/W	DLLI	0
Bit 9	R/W	SBIPARI	0
Bit 8	R/W	TXCHQOVRI	0
Bit 7	R/W	CFOVRI	0
Bit 6	R/W	TPRTYI	0
Bit 5	R/W	TFOVRI	0
Bit 4	R/W	TFUDRI	0
Bit 3	R/W	SRAMPI	0
Bit 2	R/W	UECCRSI	0
Bit 1	R/W	UECCCBI	0
Bit 0	R/W	RFOVRI	0

This register reports the high priority interrupt status for various events detected or initiated by the FREEDM 84A1024. Reading this register acknowledges and clears the interrupts. The register is also writeable to allow s/w testing of interrupt generation and service routines.

RFOVRI:

The receive Partial Packet FIFO overrun error interrupt status bit reports receive Partial Packet FIFO overrun error interrupts to the microprocessor. RFOVRI is set high on attempts to write data into the logical FIFO of a channel when it is already full. RFOVRI remains valid when interrupts are disabled and may be polled to detect receive FIFO overrun events.

UECCCBI:

The Uncorrected ECC Error detected on Chunk Buffer Memory interrupt status bit reports such an event to the microprocessor. UECCCBI is set high when an ECC Error which could not be corrected is detected during a memory access to the Chunk Buffer Memory. When set, the CB_DRAMC_UNCOECCE Register will hold the last DRAM address that was being accessed when an ECC Error occurred. UECCCBI and CB_DRAMC_UNCOECCE remain valid when interrupts are disabled and may be polled to detect error events.

UECCRSI:

The Uncorrected ECC Error detected on Re-sequencing Memory interrupt status bit reports such an event to the microprocessor. UECCRSI is set high when an ECC Error which could not be corrected is detected during a memory access to the Re-sequencing Memory. When set, the RS_DRAMC_UNCOECCE Register will hold the last DRAM address that was being accessed when an ECC Error occurred. UECCRSI and RS_DRAMC_UNCOECCE remain valid when interrupts are disabled and may be polled to detect error events.

SRAMPI:

SRAM Parity Error interrupt status bit reports parity error interrupts to the microprocessor. SRAMPI is set high whenever a parity error is detected on accesses to external SRAM. When set, the SRAM Parity Error Address (SPERRADD) Register will hold the last SRAM address that was being accessed when a parity error occurred. SRAMPI and SPERRADD remain valid when interrupts are disabled and may be polled to detect error events.

TFUDRI:

The transmit Partial Packet FIFO underflow error interrupt status bit reports transmit Partial Packet FIFO underflow error interrupts to the microprocessor. TFUDRI is set high upon attempts to read data from the logical FIFO when it is already empty. TFUDRI remains valid when interrupts are disabled and may be polled to detect transmit FIFO underflow events.

TFOVRI:

The transmit Partial Packet FIFO overflow error interrupt status bit reports transmit Partial Packet FIFO overflow error interrupts to the microprocessor. TFOVRI is set high upon attempts to write data to the logical FIFO when it is already full. TFOVRI remains valid when interrupts are disabled and may be polled to detect transmit FIFO overflow events.

TPRTYI:

The transmit parity error interrupt status bit reports the detection of a parity error on the transmit APPI. TPRTYI is set high upon detection of a parity error. TPRTYI remains valid when interrupts are disabled and may be polled to detect parity errors.

CFOVRI:

The Circular FIFO Overflow interrupt status bit reports TAPI Circular FIFO overflow error interrupts to the microprocessor. CFOVRI is set high upon attempts to write to the circular FIFO when it is already full. CFOVRI remains valid when interrupts are disabled and may be polled to detect Circular FIFO Overflow events. (NOTE – Circular FIFO overflows will not occur if the TRDY is observed or specified minimum spacing between small packets is adhered.)

TXCHQOVRI:

The Transmit Channel Queue Overflow interrupt status bit reports EQM-12 Channel Queue overflow error interrupts to the microprocessor. TXCHQOVRI is set high upon attempts to write to the Queue when it is already full. TXCHQOVRI remains valid when interrupts are disabled and may be polled to detect Queue Overflow events. (NOTE – Queue overflows will not occur if Channel availability polling is observed and adhered.)

SBIPAR:

The SBI Parity interrupt status bit (SBIPARI) reports a parity on the SBI bus. SBIPARI remains valid when interrupts are disabled and may be polled to detect SBI Parity error conditions.

DLLI:

The delay line error event interrupt status bit (DLLI) indicates the DLL ERROR register bit has gone high. When the DLL ERROR register changes from a logic zero to a logic one, the DLLI register bit is set to logic one. DLLI remains valid when interrupts are disabled and may be polled to detect DLL error events.

IFPPEI:

The Ingress FPP Empty interrupt status bit (IFPPEI) indicates that the Ingress FPP FIFO is empty. IFPPEI is set high upon detection of such this condition. IFPPEI remains valid when interrupts are disabled and may be polled.

EFPPEI:

The Egress FPP Empty interrupt status bit (EFPPEI) indicates that the Egress FPP FIFO is empty. EFPPEI is set high upon detection of such a condition. EFPPEI remains valid when interrupts are disabled and may be polled.

RSFPPEI:

The Re-sequencing FPP Empty interrupt status bit (RSFPPEI) indicates that the Re-sequencing Memories FPP FIFO is empty. RSFPPEI is set high upon detection of such a condition. RSFPPEI remains valid when interrupts are disabled and may be polled.

BADSIZEI:

The Bad Size interrupt status bit (BADSIZEI) indicates that a segment of incorrect size was received by the RAPI-12 block. If such an interrupt occurs, the ANY-PHY specification will be violated. BADSIZEI remains valid when interrupts are disabled and may be polled. Under normal operation, this interrupt will never occur. Assertion of this interrupt should trigger a chip reset.

UNSUPHFI

The IQM-12 interrupt status bit reports a datagram with an unsupported header format was detected. (In particular, Frame Relay datagrams carrying a 16, 17, or 23 bit DLCI, or PPP datagrams with PID(H) odd and/or PID(L) even). UNSUPHFI remains valid when interrupts are disabled and may be polled.

RST_DONEI

The RST_DONEI interrupt status bit reports the ending of the hardware reset or software reset operation, it indicates that all of the flip-flops and internal RAMs have been initialized. The RST_DONEI cannot be enabled but can be polled to indicate reset completion.

Reserved:

The reserved bits can be set to any value.

CBAEXI

The Chunk Buffer Allocation Exceeded Interrupt status bit reports chunk buffer allocation exceeded events. CBAEXI remains valid when interrupts are disabled and may be polled.

SDGMDI

The Small Datagram discard Interrupt status bit reports small datagram discard events due to insufficient bandwidth to sustain the number of small datagrams (less than 40 bytes) received. SDGMDI remains valid when interrupts are disabled and may be polled.

SBIC1FPSI

The SBIC1FPS Interrupt status bit reports C1FP realignment events on the SBI bus. SBIC1FPSI remains valid when interrupts are disabled and may be polled.

Register 0x00C : F84 Master Clock / Frame Pulse Activity Monitor

Bit	Type	Function	Default
Bit 31 to Bit 27		Unused	X
Bit 26	R	RCLKA[8]	X
Bit 25 To Bit 23		Unused	X
Bit 22	R	RCLKA[4]	X
Bit 21 To Bit 19		Unused	X
Bit 18	R	RCLKA[0]	X
Bit 17 To Bit 15		Unused	X
Bit 14	R	TCLKA[8]	X
Bit 13 to Bit 11		Unused	X
Bit 10	R	TCLKA[4]	X
Bit 9 to Bit 7		Unused	X
Bit 6	R	TCLKA[0]	X
Bit 5	R	TXCLKA	X
Bit 4	R	RXCLKA	X
Bit 3	R	DC1FPA	X
Bit 2	R	AC1FPA	X
Bit 1	R	REFCLKA	X
Bit 0	R	SYSCLKA	X

This register provides activity monitoring on the FREEDM 84A1024 clock and SBI frame pulse inputs. When a monitored input makes a transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read periodically to detect stuck at conditions.

SYSCLKA:

The system clock active bit (SYSCLKA) monitors for low to high transitions on the SYSCLK input. SYSCLKA is set high on a rising edge of SYSCLK, and is set low when this register is read.

REFCLKA:

The SBI reference clock active bit (REFCLKA) monitors for low to high transitions on the REFCLK input. REFCLKA is set high on a rising edge of REFCLK, and is set low when this register is read.

AC1FPA:

The SBI Add Bus frame pulse active bit (AC1FPA) monitors for low to high transitions on the AC1FP input. AC1FPA is set high on a rising edge of AC1FP, and is set low when this register is read.

DC1FPA:

The SBI Drop Bus frame pulse active bit (DC1FPA) monitors for low to high transitions on the DC1FP input. DC1FPA is set high on a rising edge of DC1FP, and is set low when this register is read.

RXCLKA:

The ANY-PHY receive clock active bit (RXCLKA) monitors for low to high transitions on the RXCLK input. RXCLKA is set high on a rising edge of RXCLK, and is set low when this register is read.

TXCLKA:

The ANY-PHY transmit clock active bit (TXCLKA) monitors for low to high transitions on the TXCLK input. TXCLKA is set high on a rising edge of TXCLK, and is set low when this register is read.

TCLKA[0,4,8]:

The Serial Transmit Clock active bits (TCLKA) monitor for low to high transitions on the TCLKn inputs. TCLKA is set high on a rising edge of TCLK, and is set low when this register is read.

RCLKA[0,4,8]:

The Serial Receive Clock active bits (RCLKA) monitor for low to high transitions on the RCLKn inputs. RCLKA is set high on a rising edge of RCLK, and is set low when this register is read.

Register 0x014 : F84 Master Line Loopback

Bit	Type	Function	Default
Bit 31 To Bit 9		Unused	X
Bit 8	R/W	LLBEN[8]	0
Bit 7 To Bit 5		Unused	0
Bit 4	R/W	LLBEN[4]	0
Bit 3 To Bit 1		Unused	0
Bit 0	R/W	LLBEN[0]	0

This register controls line loopback for the three serial data links.

LLBEN[0,4,8]:

The line loopback enable bits (LLBEN[0,4,8]) control line loopback for links #0, 4 and 8. When LLBEN[n] is set high, the data on RD[n] is passed verbatim to TD[n] which is then updated on the falling edge of RCLK[n]. TCLK[n] is ignored. When LLBEN[n] is set low, TD[n] is processed normally.

Register 0x018 : F84 Master Low Priority Interrupt Enable

Bit	Type	Function	Default
Bit 31 To Bit 11		Unused	X
Bit 10	R/W	UNTSXE	0
Bit 9	R/W	TUNPVE	0
Bit 8	R/W	CECCRSE	0
Bit 7	R/W	CECCCBE	0
Bit 6	R/W	RPFEE	0
Bit 5	R/W	RABRTE	0
Bit 4	R/W	RFCSEE	0
Bit 3	R/W	MPISTATE	0
Bit 2	R/W	ENFEE	0
Bit 1	R/W	USNEE	0
Bit 0	R/W	LSNEE	0

This register provides low priority interrupt enables for various events detected or initiated by the FREEDM 84A1024. Each low priority interrupt enable bit corresponds to the equivalent bit in the Master Low Priority Interrupt Status register. All interrupt enable bits are active high. When high, interrupts are enabled. When low, interrupts are masked. While interrupts are masked the status bit in the status register may still be polled to detect the error event. Enabled low priority interrupts cause the INTLOB interrupt pin to be asserted.

Register 0x01C : F84 Master Low Priority Interrupt Status

Bit	Type	Function	Default
Bit 31 To Bit 11		Unused	X
Bit 10	R/W	UNTSXI	0
Bit 9	R/W	TUNPVI	0
Bit 8	R/W	CECCRSI	0
Bit 7	R/W	CECCCBI	0
Bit 6	R/W	RPFEI	0
Bit 5	R/W	RABRTI	0
Bit 4	R/W	RFCSEI	0
Bit 3	R/W	MPISTATI	0
Bit 2	R/W	ENFEI	0
Bit 1	R/W	USNEI	0
Bit 0	R/W	LSNEI	0

This register reports the interrupt status for various events detected or initiated by the FREEDM 84A1024. Reading these registers acknowledges and clears the interrupts. The register is also writeable to allow s/w testing of interrupt generation and service routines.

LSNEI:

The Lost Sequence Number Event interrupt status bit indicates a datagram has been declared lost. A datagram is declared lost after the timeout period specified by LOST_CNT in the CC Memory Map has expired. When set, the Lost SN CI Register (LSNCI) holds the CI number of the last connection to detect a lost SN event. LSNEI and LSNCI remain valid when interrupts are disabled and may be polled to detect lost SN events.

USNEI:

The Unexpected Sequence number interrupt status bit reports unexpected SN conditions to the microprocessor. USNEI is set high when an unexpected SN is detected. When set, the Unexpected SN CI Register (USNCI) holds the CI number of the last connection to detect an unexpected SN. USNEI and USNCI remain valid when interrupts are disabled and may be polled to detect unexpected SN events.

ENFEI:

The number of Fragments per packet greater than Maximum allowed interrupt status bit reports when a packet with 82 or more fragments has been detected. ENFEI is active high. When set, the Excessive Number of Fragments CI Register (ENFCI) holds the CI number that caused the interrupt. ENFEI and ENFCI remain valid when interrupts are disabled and may be polled. This interrupt is only generated when output format is frame/packet (not in fragment out mode).

MPISTATI:

When asserted, the Memory Port Idle Status bit indicates to the microprocessor that the memory port has completed it's last command. This signal is the inverse of MPBusy found in the Memory Port Control Register. MPISTATI remains valid when interrupts are disabled and may be polled to indicate idle status.

RFCSEI:

The receive frame check sequence error interrupt status bit reports receive FCS error interrupts to the microprocessor. RFCSEI is set high when a mismatch between the received FCS code and the computed CRC residue is detected. RFCSEI remains valid when interrupts are disabled and may be polled to detect receive FCS error events. Erred datagrams will be redirected during CI lookup and can be programmed to a separate CI. In addition, the RERR bit on the Rx ANY-PHY interface will be set.

RABRTI:

The receive abort interrupt status bit reports receive HDLC abort interrupts to the microprocessor. RABRTI is set high upon receipt of an abort code (at least 7 contiguous 1's). RABRTI remains valid when interrupts are disabled and may be polled to detect receive abort events.

RPFEI:

The receive packet format error interrupt status bit reports receive packet format error interrupts to the microprocessor. RPFEI is set high upon receipt of a packet that is longer than the maximum programmed length, of a packet that is shorter than 32 bits (CRC-CCITT) or 48 bits (CRC-32), or of a packet that is not octet aligned. RPFEI remains valid when interrupts are disabled and may be polled to detect receive packet format error events.

CECCCBI:

The Corrected ECC Error on Chunk Buffer Memory interrupt status bit reports such an event to the microprocessor. CECCCBI is set high when an ECC Error which was corrected is detected during a memory access to the Chunk Buffer Memory. When set, the CB_DRAMC_COECCE Register will hold the DRAM address that was being accessed when the ECC Error occurred. CECCCBI and CB_DRAMC_COECCE remain valid when interrupts are disabled and may be polled to detect error events.

CECCRSI:

The Corrected ECC Error on Re-sequencing Memory interrupt status bit reports such an event to the microprocessor. CECCRSI is set high when an ECC Error which was corrected is detected during a memory access to the Re-sequencing Memory. When set, the RS_DRAMC_COECCE Register will hold the DRAM address that was being accessed when the ECC Error occurred. CECCRSI and RS_DRAMC_COECCE remain valid when interrupts are disabled and may be polled to detect error events.

TUNPVI:

The transmit unprovisioned error interrupt status bit reports an attempted data transmission to an unprovisioned Any-PHY channel. TUNPVI is set high upon attempts to transfer data over the Any-PHY interface to an unprovisioned Any-PHY channel. TUNPVI remains valid when interrupts are disabled and may be polled to detect an attempt to write data to an unprovisioned channel.

UNTSXI:

The Unexpected TSX interrupt status bit reports observation of invalid arrival of TSX to the microprocessor. UNTSXI is set high when such an event is reported. UNTSXI remains valid when interrupts are disabled and may be polled.

Register 0x048 : F84 SBI DROP BUS Master Configuration

Bit	Type	Function	Default
Bit 31 To Bit 2		Unused	X
Bit 1 To Bit 0	R/W	Reserved	0

This register contains reserved bits.

Reserved:

The Reserved bit must be set to 0 for correct operation of the FREEDM 84A1024 device.

Register 0x04C : F84 SBI ADD BUS Master Configuration

Bit	Type	Function	Default
Bit 31 To Bit 4		Unused	X
Bit 3	R/W	DEFAULT_DRV	0
Bit 2	R/W	SBI_MODE	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	CLK_MSTR	0

This register configures the operation of the SBI ADD BUS.

CLK_MSTR:

The CLK_MSTR bit is used to specify whether the Insert block functions as a clock master or a clock slave. When this bit is a '1' the Insert block is a clock master. When set high, this bit overrides the individual tributary settings for clock master. The default state of this bit is clock slave.

Reserved:

The reserved bits must be set to 0 for correct operation of the FREEDM 84A1024 device.

SBI_MODE:

The SBI_MODE bit selects SBI versus SBI336 mode of operation. When set high, 19.44MHz (SBI bus) is selected. The default state of this bit is 77MHz (SBI336) mode of operation.

DEFAULT_DRV:

The Default Bus Driver selector bit (DEFAULT_DRV) enables the FREEDM 84A1024 to drive the SBI ADD BUS when no other device is doing so. When set to 1, the INSBI336 will drive the bus whenever the ADETECT[1:0] inputs are both 0. When set to 0, the INSBI336 will only drive the bus when it has data to send (and when ADETECT[1:0] are both 0). It is recommended that one device connected to an SBI Bus be nominated as a default driver and configured to drive the bus when no other device is doing so.

Register 0x068: DLL Configuration

Bit	Type	Function	Default
Bit 31 To Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R/W	ERRORE	X
Bit 1	R/W	VERN_EN	0
Bit 0	R/W	LOCK	0

The DLL Configuration Register controls the basic operation of the DLL.

LOCK:

The LOCK register is used to force the DLL to ignore phase offsets indicated by the phase detector after phase lock has been achieved. When LOCK is set to logic zero, the DLL will track phase offsets measured by the phase detector between the DLLSYSCLK and the DLLREFCLK inputs. When LOCK is set to logic one, the DLL will not change the tap after the phase detector indicates a zero phase offset between the DLLSYSCLK and the DLLREFCLK inputs for the first time.

VERN_EN:

The vernier enable register (VERN_EN) forces the DLL to ignore the phase detector and use the tap number specified by the VERNIER[7:0] register bits. When VERN_EN is set to logic zero, the DLL operates normally adjusting the phase offset based on the phase detector. When VERN_EN is set to logic one, the delay line uses the tap specified by the VERNIER[7:0] register bits.

ERRORE:

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, an interrupt is generated upon assertion event of the ERR output and ERROR register. When ERRORE is set low, changes in the ERROR and ERR status do not generate an interrupt.

Reserved:

The reserved bits must be set low for correct operation of the FREEDM 84A1024 device.

Register 0x06C: DLL Vernier Control

Bit	Type	Function	Default
Bit 31 To Bit 8		Unused	X
Bit 7	R/W	VERNIER[7]	0
Bit 6	R/W	VERNIER[6]	0
Bit 5	R/W	VERNIER[5]	0
Bit 4	R/W	VERNIER[4]	0
Bit 3	R/W	VERNIER[3]	0
Bit 2	R/W	VERNIER[2]	0
Bit 1	R/W	VERNIER[1]	0
Bit 0	R/W	VERNIER[0]	0

The Vernier Control Register provides the delay line tap control when using the vernier option.

VERNIER[7:0]:

The vernier tap register bits (VERNIER[7:0]) specifies the phase delay through the DLL when using the vernier feature. When VERN_EN is set high, the VERNIER[7:0] registers specify the delay tap used. When VERN_EN is set low, the VERNIER[7:0] register is ignored.

A VERNIER[7:0] value of all zeros specifies the delay tap with the minimum delay through the delay line. A VERNIER[7:0] value of 255 specifies the delay tap with the maximum delay through the delay line.

Register 0x070: DLL Delay Tap Status

Bit	Type	Function	Default
Bit 31 To Bit 8		Unused	X
Bit 7	R/W	TAP[7]	X
Bit 6	R/W	TAP[6]	X
Bit 5	R/W	TAP[5]	X
Bit 4	R/W	TAP[4]	X
Bit 3	R/W	TAP[3]	X
Bit 2	R/W	TAP[2]	X
Bit 1	R/W	TAP[1]	X
Bit 0	R/W	TAP[0]	X

The DLL Delay Tap Status Register indicates the delay tap used by the DLL to generate the outgoing clock.

Writing to this register performs a software reset of the DLL. A software reset requires a maximum of 24*256 DLLSYSCLK cycles for the DLL to regain lock. During this time the DLLDCLKO phase is adjusting from its current position to delay tap 0 and back to a lock position.

TAP[7:0]:

The tap status register bits (TAP[7:0]) specifies the delay line tap the DLL is using to generate the outgoing clock DLLDCLKO.

When TAP[7:0] is logic zero, the DLL is using the delay line tap with minimum phase delay. When TAP[7:0] is equal to 255, the DLL is using the delay line tap with maximum phase delay. TAP[7:0] is invalid when vernier enable VERN_EN is set to one.

Register 0x074: DLL Control Status

Bit	Type	Function	Default
Bit 31 To Bit 8		Unused	X
Bit 7	R	DLLSYSCLKI	X
Bit 6	R	DLLREFCLKI	X
Bit 5	R	ERRORI	X
Bit 4	R	CHANGEI	X
Bit 3		Unused	X
Bit 2	R	ERROR	X
Bit 1	R	CHANGE	X
Bit 0	R	RUN	X

The DLL Control Status Register provides information of the DLL operation.

RUN:

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap in which the phase difference between the rising edge of DLLREFCLK and the rising edge of SYSLCK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1.

The RUN register bit is cleared only by a hardware or a software reset. RUN is forced high when the VERN_EN register is set high.

CHANGE:

The delay line tap change register bit (CHANGE) indicates the DLL has moved to a new delay line tap. CHANGE is set high for eight DLLSYSCLK cycles when the DLL moves to a new delay line tap.

ERROR:

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. When ERROR is high, the DLL cannot generate a DLLDCLKO phase which causes the rising edge of DLLREFCLK to be aligned to the rising edge of DLLSYSCLK. ERROR is set low, when the DLL captures lock again.

ERROR is forced low when the VERN_EN register is set high.

CHANGEI:

The delay line tap change event register bit (CHANGEI) indicates the CHANGE register bit has changed value. When the CHANGE register changes from a logic zero to a logic one, the CHANGEI register bit is set to logic one.

ERRORI:

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. If the ERRORE interrupt enable is high, the DLLI bit in the F84 Master High Priority Interrupt Status Register is also asserted when ERRORI asserts.

DLLREFCLKI:

The reference clock event register bit DLLREFCLKI provides a method to monitor activity on the reference clock to the DLL. This reference clock is the feedback path from the far end of the clock tree to which the system clock is synchronized. When the DLLREFCLK primary input changes from a logic zero to a logic one, the DLLREFCLKI register bit is set to logic one.

DLLSYSCLKI:

The system clock event register bit DLLSYSLCKI provides a method to monitor activity on the system clock (SYSCLK). When the SYSCLK primary input changes from a logic zero to a logic one, the DLLSYSCLKI register bit is set to logic one. The DLLSYSCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

Register 0x100: RCAS Indirect Context RAM Link Select

Bit	Type	Function	Default
Bit 31 To Bit 12		Unused	X
Bit 11	R	BUSY	0
Bit 10	R/W	RWB	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	SBI	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

This register provides the link number used to access the RCAS context RAM. Writing to this register triggers an indirect register access.

Reserved:

The reserved bits must be set low for correct operation of the FREEDM 84A1024 device.

TRIB[4:0], SPE[1:0] and SBI:

The TRIB[4:0], SPE[1:0] and SBI fields are used to fully specify to which SBI tributary the RCAS context RAM write or read operation will apply.

TRIB[4:0] specifies the SBI tributary number within the SBI SPE as specified by the SPE[1:0] and SBI fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. SBI must be written to a logic one in the FREEDM 84A1024 device.

RWB:

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the RCAS context RAM. Writing a logic zero to RWB triggers an indirect write operation. Data to be written is taken from the LEN and SBI_MODE[2:0] bits of the RCAS Indirect context RAM Data register. Writing a logic one to RWB triggers an indirect read operation. The data read can be found in the LEN and SBI_MODE[2:0] bits of the RCAS Indirect context RAM Data register.

BUSY:

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when this register is written, to trigger an indirect access, and will stay high until the access is complete. At which point, BUSY will be set low. This register should be polled to determine when data from an indirect read operation is available in the Indirect Data register or to determine when a new indirect write operation may commence.

Register 0x104: RCAS Indirect Context RAM Data

Bit	Type	Function	Default
Bit 31 To Bit 4		Unused	X
Bit 3	R/W	SBI_MODE[2]	0
Bit 2	R/W	SBI_MODE[1]	0
Bit 1	R/W	SBI_MODE[0]	0
Bit 0	R/W	LEN	0

This register provides the link enable bit and the frame mode or data type associated to this particular link in the RCAS context RAM.

SBI_MODE[2:0]:

The SBI Frame Mode bits (SBI_MODE [2:0]), define the type of data for a specific link to be configured according to the following table.

Table 15 - SBI Mode

SBI_MODE [2:0]	Configuration
000	Single unframed unchannelized DS-3/Serial Link
001	28 Unframed T1/J1 links
010	21 Unframed E1 links
011	Unused
100	Single framed unchannelized DS-3
101	28 Framed Channelized T1/J1 links
110	21 Framed Channelized E1 links
111	unused

LEN:

The Link Enable bit (LEN) when set Low disables the link. If enabled, the corresponding serial link must be disabled by clearing the appropriate SLINK[n] bit in register 0x114. A link cannot be disabled (LEN->0) unless the link is first disabled in the SBI Extract (Reg 0x5DC), ENBL bit.

Register 0x108: RCAS Indirect Channel Provision RAM Link Select

Bit	Type	Function	Default
Bit 15 To Bit 13		Unused	X
Bit 12	R/W	SBI_MODE[2]	0
Bit 11	R/W	SBI_MODE[1]	0
Bit 10	R/W	SBI_MODE[0]	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	SBI	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

This register provides the link number used to access the RCAS channel provision RAM.

Reserved:

The reserved bits must be set low for correct operation of the FREEDM 84A1024 device.

SBI_MODE[2:0]:

This field must be set to the same value as Bits3:1 in Register 0x104.

TRIB[4:0], SPE[1:0] and SBI:

The TRIB[4:0], SPE[1:0] and SBI fields are used to fully specify to which SBI tributary the context RAM write or read operation will apply.

TRIB[4:0] specifies the SBI tributary number within the SBI SPE as specified by the SPE[1:0] and SBI fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. SBI must be written to a logic one in the FREEDM 84A1024 device.

Register 0x10C: RCAS Indirect Channel Provision RAM Timeslot and control Select

Bit	Type	Function	Default
Bit 31 To Bit 7		Unused	X
Bit 6	R	BUSY	0
Bit 5	R/W	RWB	0
Bit 4	R/W	TSLOT[4]	0
Bit 3	R/W	TSLOT[3]	0
Bit 2	R/W	TSLOT[2]	0
Bit 1	R/W	TSLOT[1]	0
Bit 0	R/W	TSLOT[0]	0

This register provides the link timeslot number and control bits used to access the channel provision RAM. The RCAS Indirect Channel Provision RAM Link Select register must be valid before writing this register. Writing to this register triggers an indirect register access.

TSLOT[4:0]:

The indirect timeslot number bits (TSLOT[4:0]) indicate the timeslot to be configured or interrogated in the indirect access. For a channelized T1/J1 link, timeslots 0 to 23 are valid. For a channelized E1 link, timeslots 0 to 31 are valid. For unchannelized links, only timeslot 0 is valid.

RWB:

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the RCAS channel provision RAM. The address to the channel provision RAM is constructed by combining the TSLOT[4:0] and LINK number. Writing a logic zero to RWB triggers an indirect write operation. Data to be written is taken from the PROV, and the CHAN[9:0] bits of the Indirect Channel Data and Loopback enable register. Writing a logic one to RWB triggers an indirect read operation. Addressing of the RAM is the same as in an indirect write operation. The data read can be found in the PROV, and the CHAN[9:0] bits of the RCAS Indirect Channel Data register.

BUSY:

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when this register is written, to trigger an indirect access, and will stay high until the access is complete. At which point, BUSY will be set low. This register should be polled to determine when data from an indirect read operation is available in the RCAS Indirect Data register or to determine when a new indirect write operation may commence.

Register 0x110: RCAS Indirect Channel Data and Loopback enable

Bit	Type	Function	Default
Bit 31 To Bit 12		Unused	X
Bit 11	R/W	CDLBEN	0
Bit 10	R/W	PROV	0
Bit 9	R/W	CHAN [9]	0
Bit 8	R/W	CHAN [8]	0
Bit 7	R/W	CHAN [7]	0
Bit 6	R/W	CHAN [6]	0
Bit 5	R/W	CHAN [5]	0
Bit 4	R/W	CHAN [4]	0
Bit 3	R/W	CHAN [3]	0
Bit 2	R/W	CHAN [2]	0
Bit 1	R/W	CHAN [1]	0
Bit 0	R/W	CHAN [0]	0

This register contains the data read from the RCAS channel provision RAM after an indirect read operation or the data to be inserted into the RCAS channel provision RAM in an indirect write operation.

One channel must be reserved for timeslots that are unprovisioned in an active tributary.

CHAN[9:0]:

The indirect data bits (CHAN[9:0]) report the channel number read from the channel provision RAM after an indirect read operation has completed. Channel number to be written to the RCAS channel provision RAM in an indirect write operation must be set up in this register before triggering the write. CHAN[9:0] reflects the value written until the completion of a subsequent indirect read operation.

PROV:

The indirect provision enable bit (PROV) reports the channel provision enable flag read from the RCAS channel provision RAM after an indirect read operation has completed. The provision enable flag to be written to the RCAS channel provision RAM in an indirect write operation must be set up in this register before triggering the write. When PROV is set high, the current receive data byte is processed as part of the channel as indicated by CHAN[9:0]. When PROV is set low, the current timeslot does not belong to any channel and the received data byte ignored. PROV reflects the value written until the completion of a subsequent indirect read operation.

CDLBEN:

The indirect channel based diagnostic loopback enable bit (CDLBEN) indicates that for this channel, data is loopbacked from the Tx path (THDL-12) instead of being received from the receive links. If enabled, the channel can not be used for serial or SBI traffic. In addition, the equivalent bandwidth must be disabled in normal mode operation.

Register 0x114: RCAS Serial Link and Enable signal Register

Bit	Type	Function	Default
Bit 31 To Bit 9		Unused	X
Bit 8	R/W	SLINK[8]	0
Bit 7 to Bit 5		Unused	X
Bit 4	R/W	SLINK [4]	0
Bit 3 to Bit 1		Unused	X
Bit 0	R/W	SLINK [0]	0

This register allows the selection of the receive serial link to be enabled.

SLINK[0], SLINK[4], SLINK[8]:

The receive Serial Link selection (SLINK[8,4,0]) specify the serial link to be activated, and its data and clock to be received from the RCAS-12. When SLINK[0] for example is set high, the data and clock on the particular selected serial link will be received, otherwise the serial link is ignored. When a serial link is enabled, the corresponding SBI/SPE on the SBI bus must be disabled. Serial links map to SBI links according to the following table:

Table 16 - Serial Link to SBI Link Mapping

Serial Link	SPE No.	SBI Trib No.
0	1	1
4	2	1
8	3	1

Register 0x200 : RHDL Indirect Channel Select

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R	CBUSY	0
Bit 14	R/W	CRWB	0
Bit 13 To Bit 10		Unused	X
Bit 9	R/W	CHAN[9]	0
Bit 8	R/W	CHAN[8]	0
Bit 7	R/W	CHAN[7]	0
Bit 6	R/W	CHAN[6]	0
Bit 5	R/W	CHAN[5]	0
Bit 4	R/W	CHAN[4]	0
Bit 3	R/W	CHAN[3]	0
Bit 2	R/W	CHAN[2]	0
Bit 1	R/W	CHAN[1]	0
Bit 0	R/W	CHAN[0]	0

This register provides the channel number used to access the receive channel provision RAM. Writing to this register triggers an indirect channel register access. During indirect write operations, there must be no incoming data present on the HDLC channel being configured. Prior to commencing any indirect write operation to a particular HDLC channel, any timeslots mapped in the RCAS channel provision RAM (Register 0x110) to that HDLC channel must be re-mapped to the HDLC channel reserved for unused time slots.

CHAN[9:0]:

The indirect channel number bits (CHAN[9:0]) indicate the receive channel to be configured or interrogated in the indirect access.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the receive channel provision RAM. Writing a logic zero to CRWB triggers an indirect write operation. Data to be written is taken from the Indirect Channel Data registers. Writing a logic one to CRWB triggers an indirect read operation. The data read can be found in the Indirect Channel Data registers.

CBUSY:

The indirect access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set high when this register is written to trigger an indirect access, and will stay high until the access is complete. At which point, CBUSY will be set low. This register should be polled to determine when data from an indirect read operation is available in the RHDL Indirect Channel Data #1 and #2 registers or to determine when a new indirect write operation may commence.

Register 0x204 : RHDL Indirect Channel Data Register #1

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	W*	PROV	X
Bit 14	R/W	STRIP	X
Bit 13	W*	Reserved	X
Bit 12	R	TAVAIL	X
Bit 11	W	FPTR[11]	X
Bit 10	W	FPTR[10]	X
Bit 9	W	FPTR[9]	X
Bit 8	W	FPTR[8]	X
Bit 7	W	FPTR[7]	X
Bit 6	W	FPTR[6]	X
Bit 5	W	FPTR[5]	X
Bit 4	W	FPTR[4]	X
Bit 3	W	FPTR[3]	X
Bit 2	W	FPTR[2]	X
Bit 1	W	FPTR[1]	X
Bit 0	W	FPTR[0]	X

This register contains data read from the channel provision RAM after an indirect read operation or data to be inserted into the channel provision RAM in an indirect write operation.

* These register bits are also readable if no traffic is enabled in the device.

FPTR[11:0]:

The indirect FIFO block pointer (FPTR[11:0]) identifies one of the blocks of the circular linked list in the partial packet buffer used in the logical FIFO of the current channel. The FIFO pointer to be written to the channel provision RAM, in an indirect write operation, must be set up in this register before triggering the write. The FIFO pointer value can be any one of the blocks provisioned to form the circular buffer.

TAVAIL:

The indirect Transaction Available bit (TAVAIL) indicates whether the FIFO for the channel currently contains at least one transaction, defined as either a complete packet or a transaction sized number of blocks, available for transfer over the receive DMA interface. When TAVAIL is a logic 1, a transaction is available for transfer. When TAVAIL is a logic 0, a transaction is not available. TAVAIL is a read-only bit.

Reserved:

The Reserved bit must be set to 1 for correct operation of the FREEDM 84A1024 device.

STRIP:

The indirect frame check sequence discard bit (STRIP) configures the HDLC processor to remove the CRC from the incoming frame when writing the data to the channel FIFO. The FCS discard bit to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When STRIP is set high and CRC[1:0] is not equal to "00", the received CRC value is not written to the FIFO. When STRIP is set low, the received CRC value is written to the FIFO. The bytes in buffer field of the RPD correctly reflect the presence/absence of CRC bytes in the buffer. The value of STRIP is ignored when DELIN is low. STRIP reflects the value written until the completion of a subsequent indirect channel read operation.

PROV:

The indirect provision enable bit (PROV) reports the channel provision enable flag read from the channel provision RAM after an indirect channel read operation has completed. The provision enable flag to be written to the channel provision RAM, in an indirect write operation, must be set up in this register before triggering the write. When PROV is set high, the HDLC processor will process data on the channel specified by CHAN[9:0]. When PROV is set low, the HDLC processor will ignore data on the channel specified by CHAN[9:0]. PROV reflects the value written until the completion of a subsequent indirect channel read operation.

Register 0x208 : RHDL Indirect Channel Data Register #2

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	W*	7BIT	X
Bit 14	W*	PRIORITY	X
Bit 13	W*	INVERT	X
Bit 12		Unused	X
Bit 11	W*	CRC[1]	X
Bit 10	W*	CRC[0]	X
Bit 9	R/W	Reserved	X
Bit 8	R/W	Reserved	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register contains data read from the channel provision RAM after an indirect read operation or it contains data to be inserted into the channel provision RAM in an indirect write operation.

* These register bits are also readable if no traffic is enabled in the device.

Reserved:

The reserved bits must be set to the following values for correct operation of the FREEDM 84A1024 device.

Table 17 - Reserved bit Settings

Bit	Setting
9	0
8	0
3	0
2	0
1	0
0	1

CRC[1:0]:

The CRC algorithm bits (CRC[1:0]) configures the HDLC processor to perform CRC verification on the incoming data stream. The value of CRC[1:0] to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. CRC[1:0] is ignored when DELIN is low. CRC[1:0] reflects the value written until the completion of a subsequent indirect channel read operation.

Table 18 - CRC[1:0] Settings

CRC[1]	CRC[0]	Operation
0	0	No Verification
0	1	CRC-CCITT
1	0	CRC-32
1	1	Reserved

INVERT:

The HDLC data inversion bit (INVERT) configures the HDLC processor to logically invert the incoming HDLC stream from the RCAS-12 before processing it. The value of INVERT to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When INVERT is set to one, the HDLC stream is logically inverted before processing. When INVERT is set to zero, the HDLC stream is not inverted before processing. INVERT reflects the value written until the completion of a subsequent indirect channel read operation. Before tearing down a channel, this bit must be set to 0.

PRIORITY:

The channel FIFO priority bit (PRIORITY) informs the partial packet processor that the channel has precedence over other channels when being serviced by upstream blocks. The value of PRIORITY to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. Channel FIFOs with PRIORITY set to one are serviced before channel FIFOs with PRIORITY set to zero. Channels with an HDLC data rate to FIFO size ratio that is significantly higher than other channels should have PRIORITY set to one. PRIORITY reflects the value written until the completion of a subsequent indirect channel read operation.

7BIT:

The 7BIT enable bit (7BIT) configures the HDLC processor to ignore the least significant bit of each octet in the incoming channel stream. The value of 7BIT to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When 7BIT is set high, the least significant bit (last bit of each octet received), is ignored. When 7BIT is set low, the entire receive data stream is processed. 7BIT reflects the value written until the completion of a subsequent indirect channel read operation.

Register 0x210 : RHDL Indirect Block Select

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R	BBUSY	0
Bit 14	R/W	BRWB	0
Bit 13 To Bit 12		Unused	X
Bit 11	R/W	BLOCK[11]	0
Bit 10	R/W	BLOCK[10]	0
Bit 9	R/W	BLOCK[9]	0
Bit 8	R/W	BLOCK[8]	0
Bit 7	R/W	BLOCK[7]	0
Bit 6	R/W	BLOCK[6]	0
Bit 5	R/W	BLOCK[5]	0
Bit 4	R/W	BLOCK[4]	0
Bit 3	R/W	BLOCK[3]	0
Bit 2	R/W	BLOCK[2]	0
Bit 1	R/W	BLOCK[1]	0
Bit 0	R/W	BLOCK[0]	0

This register provides the block number used to access the block pointer RAM. Writing to this register triggers an indirect block register access.

BLOCK[11:0]:

The indirect block number (BLOCK[11:0]) indicates the block to be configured or interrogated in the indirect access.

BRWB:

The block indirect access control bit (BRWB) selects between a configure (write) or interrogate (read) access to the block pointer RAM. Writing a logic zero to BRWB triggers an indirect block write operation. Data to be written is taken from the Indirect Block Data register. Writing a logic one to BRWB triggers an indirect block read operation. The data read can be found in the Indirect Block Data register.

BBUSY:

The indirect access status bit (BBUSY) reports the progress of an indirect access. BBUSY is set high when this register is written to trigger an indirect access, and will stay high until the access is complete. At which point, BBUSY will be set low. This register should be polled to determine when data from an indirect read operation is available in the RHDL Indirect Block Data register or to determine when a new indirect write operation may commence.

Register 0x214 : RHDL Indirect Block Data

Bit	Type	Function	Default
Bit 31 To Bit 12		Unused	X
Bit 11	R/W	BPTR[11]	X
Bit 10	R/W	BPTR[10]	X
Bit 9	R/W	BPTR[9]	X
Bit 8	R/W	BPTR[8]	X
Bit 7	R/W	BPTR[7]	X
Bit 6	R/W	BPTR[6]	X
Bit 5	R/W	BPTR[5]	X
Bit 4	R/W	BPTR[4]	X
Bit 3	R/W	BPTR[3]	X
Bit 2	R/W	BPTR[2]	X
Bit 1	R/W	BPTR[1]	X
Bit 0	R/W	BPTR[0]	X

This register contains data read from the block pointer RAM after an indirect block read operation or data to be inserted into the block pointer RAM in an indirect block write operation.

BPTR[11:0]:

The indirect block pointer (BPTR[11:0]) configures the block pointer of the block specified by the Indirect Block Select register. The block pointer to be written to the block pointer RAM, in an indirect write operation, must be set up in this register before triggering the write. The block pointer value is the block number of the next block in the linked list. A circular list of blocks must be formed in order to use the block list as a receive channel FIFO buffer. BPTR[11:0] reflects the value written until the completion of a subsequent indirect block read operation. When provisioning a channel FIFO, all block pointers must be re-written to properly initialize the FIFO.

Register 0x220 : RHDL Configuration

Bit	Type	Function	Default
Bit 31 To Bit 10		Unused	X
Bit 9	R/W	LENCHK	0
Bit 8	R/W	TSTD	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register configures all provisioned receive channels.

TSTD:

The telecom standard bit (TSTD) controls the bit ordering of the HDLC data transferred across the receive APPI. When TSTD is set low, the least significant bit of each byte on the receive APPI bus (AD[0] and AD[8]) is the first HDLC bit received and the most significant bit of each byte (AD[7] and AD[15]) is the last HDLC bit received (datacom standard). When TSTD is set high, AD[0] and AD[8] are the last HDLC bits received and AD[7] and AD[15] are the first HDLC bits received (telecom standard).

LENCHK:

The packet length error check bit (LENCHK) controls the checking of receive packets that are longer than the maximum programmed length. When LENCHK is set high, receive packets are aborted and the remainder of the frame discarded when the packet exceeds the maximum packet length given by MAX[15:0]. When LENCHK is set low, receive packets are not checked for maximum size and MAX[15:0] must be set to ‘hFFFF.

Note: It is recommended to set this bit to 1. If not set, a string of all 0’s will be interpreted as an infinite length packet and will cause chunk buffer exhaustion.

Register 0x224 : RHDL Maximum Packet Length

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R/W	MAX[15]	1
Bit 14	R/W	MAX[14]	1
Bit 13	R/W	MAX[13]	1
Bit 12	R/W	MAX[12]	1
Bit 11	R/W	MAX[11]	1
Bit 10	R/W	MAX[10]	1
Bit 9	R/W	MAX[9]	1
Bit 8	R/W	MAX[8]	1
Bit 7	R/W	MAX[7]	1
Bit 6	R/W	MAX[6]	1
Bit 5	R/W	MAX[5]	1
Bit 4	R/W	MAX[4]	1
Bit 3	R/W	MAX[3]	1
Bit 2	R/W	MAX[2]	1
Bit 1	R/W	MAX[1]	1
Bit 0	R/W	MAX[0]	1

This register configures the maximum legal HDLC packet byte length.

MAX[15:0]:

The maximum HDLC packet length (MAX[15:0]) configures the FREEDM 84A1024 to reject HDLC packets longer than a maximum size when LENCHK is set high. Receive packets with total length, including address, control, information and FCS fields, greater than MAX[15:0] bytes are aborted. When LENCHK is set low, aborts are not generated regardless of packet length and MAX[15:0] must be set to ‘hFFFF.

Register 0x380 : THDL Indirect Channel Select

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R	CBUSY	0
Bit 14	R/W	CRWB	0
Bit 13 To Bit 10		Unused	X
Bit 9	R/W	CHAN[9]	0
Bit 8	R/W	CHAN[8]	0
Bit 7	R/W	CHAN[7]	0
Bit 6	R/W	CHAN[6]	0
Bit 5	R/W	CHAN[5]	0
Bit 4	R/W	CHAN[4]	0
Bit 3	R/W	CHAN[3]	0
Bit 2	R/W	CHAN[2]	0
Bit 1	R/W	CHAN[1]	0
Bit 0	R/W	CHAN[0]	0

This register provides the channel number used to access the transmit channel provision RAM. Writing to this register triggers an indirect channel register access.

CHAN[9:0]:

The indirect channel number bits (CHAN[9:0]) indicate the channel to be configured or interrogated in the indirect access.

CRWB:

The channel indirect access control bit (CRWB) selects between a configure (write) or interrogate (read) access to the channel provision RAM. Writing a logic zero to CRWB triggers an indirect write operation. Data to be written is taken from the Indirect Channel Data registers. Writing a logic one to CRWB triggers an indirect read operation. The data read can be found in the Indirect Channel Data registers.

CBUSY:

The indirect access status bit (CBUSY) reports the progress of an indirect access. CBUSY is set high when this register is written to trigger an indirect access, and will stay high until the access is complete. At which point, CBUSY will be set low. This register should be polled to determine when data from an indirect read operation is available in the THDL Indirect Channel Data #1, #2 and #3 registers or to determine when a new indirect write operation may commence.

Register 0x384 : THDL Indirect Channel Data #1

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R/W	PROV	X
Bit 14	R/W	CRC[1]	X
Bit 13	R/W	CRC[0]	X
Bit 12	R/W	DELIN	X
Bit 11	R/W	FPTR[11]	X
Bit 10	R/W	FPTR[10]	X
Bit 9	R/W	FPTR[9]	X
Bit 8	R/W	FPTR[8]	X
Bit 7	R/W	FPTR[7]	X
Bit 6	R/W	FPTR[6]	X
Bit 5	R/W	FPTR[5]	X
Bit 4	R/W	FPTR[4]	X
Bit 3	R/W	FPTR[3]	X
Bit 2	R/W	FPTR[2]	X
Bit 1	R/W	FPTR[1]	X
Bit 0	R/W	FPTR[0]	X

This register contains data read from the channel provision RAM after an indirect channel read operation or data to be inserted into the channel provision RAM in an indirect channel write operation.

FPTR[11:0]:

The indirect FIFO block pointer (FPTR[11:0]) informs the partial packet buffer processor about the circular linked list of blocks to use for a FIFO for the channel. The FIFO pointer to be written to the channel provision RAM, in an indirect write operation, must be set up in this register before triggering the write. The FIFO pointer value can be any one of the block numbers provisioned, by indirect block write operations, to form the circular buffer.

DELIN:

The indirect delineate enable bit (DELIN) configures the HDLC processor to perform flag sequence insertion and bit stuffing on the outgoing data stream. The delineate enable bit to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When DELIN is set high, flag sequence insertion, bit stuffing and ,optionally, CRC generation is performed on the outgoing HDLC data stream. When DELIN is set low, the HDLC processor does not perform any processing (flag sequence insertion, bit stuffing nor CRC generation) on the outgoing stream. DELIN reflects the value written until the completion of a subsequent indirect channel read operation.

CRC[1:0]:

The CRC algorithm (CRC[1:0]) configures the HDLC processor to perform CRC generation on the outgoing HDLC data stream. The value of CRC[1:0] to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. CRC[1:0] is ignored when DELIN is low. CRC[1:0] reflects the value written until the completion of a subsequent indirect channel read operation.

Table 19 - CRC[1:0] Settings

CRC[1]	CRC[0]	Operation
0	0	No CRC
0	1	CRC-CCITT
1	0	CRC-32
1	1	Reserved

PROV:

The indirect provision enable bit (PROV) reports the channel provision enable flag read from the channel provision RAM after an indirect channel read operation has completed. The provision enable flag to be written to the channel provision RAM, in an indirect write operation, must be set up in this register before triggering the write. When PROV is set high, the HDLC processor will service requests for data from the TCAS-12 block. When PROV is set low, the HDLC processor will ignore requests from the TCAS-12 block. PROV reflects the value written until the completion of a subsequent indirect channel read operation.

Register 0x388 : THDL Indirect Channel Data #2

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R/W	7BIT	X
Bit 14	R/W	INHIBIT	X
Bit 13	R/W	INVERT	X
Bit 12	R/W	DFCS	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	FLEN[10]	X
Bit 9	R/W	FLEN[9]	X
Bit 8	R/W	FLEN[8]	X
Bit 7	R/W	FLEN[7]	X
Bit 6	R/W	FLEN[6]	X
Bit 5	R/W	FLEN[5]	X
Bit 4	R/W	FLEN[4]	X
Bit 3	R/W	FLEN[3]	X
Bit 2	R/W	FLEN[2]	X
Bit 1	R/W	FLEN[1]	X
Bit 0	R/W	FLEN[0]	X

This register contains data to be inserted into the channel provision RAM in an indirect write operation.

FLEN[10:0]:

The indirect FIFO length (FLEN[10:0]) is the number of blocks, less one, that is provisioned to the circular channel FIFO specified by the FPTR[10:0] block pointer. The FIFO length to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write.

Reserved:

The reserved bits must be set low for correct operation of the FREEDM 84A1024 device.

DFCS:

The diagnose frame check sequence bit (DFCS) controls the inversion of the FCS field inserted into the transmit packet. The value of DFCS to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When DFCS is set to one, the FCS field in the outgoing HDLC stream is logically inverted allowing diagnosis of downstream FCS verification logic. The outgoing FCS field is not inverted when DFCS is set to zero. DFCS reflects the value written until the completion of a subsequent indirect channel read operation.

INVERT:

The HDLC data inversion bit (INVERT) configures the HDLC processor to logically invert the outgoing HDLC stream. The value of INVERT to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When INVERT is set to one, the outgoing HDLC stream is logically inverted. The outgoing HDLC stream is not inverted when INVERT is set to zero. INVERT reflects the value written until the completion of a subsequent indirect channel read operation.

INHIBIT:

The channel FIFO expedite inhibit bit (INHIBIT) informs the partial packet processor that the channel has less priority than other channels when requesting data from the EQM-12. The value of INHIBIT to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. Channel FIFOs with INHIBIT set to one cannot make expedited requests for data to the EQM-12. When INHIBIT is set to zero, both normal and expedited requests can be made to the EQM-12. Channels with HDLC data rates significantly slower than other channels should have INHIBIT set to one. INHIBIT reflects the value written until the completion of a subsequent indirect channel read operation.

7BIT:

The least significant stuff enable bit (7BIT) configures the HDLC processor to stuff the least significant bit of each octet in the outgoing channel stream. The value of 7BIT to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When 7BIT is set high, the least significant bit (last bit of each octet transmitted) does not contain channel data and is forced to the value configured by the BIT8 register bit. When 7BIT is set low, the entire octet contains valid data and BIT8 is ignored. 7BIT reflects the value written until the completion of a subsequent indirect channel read operation.

Register 0x38C : THDL Indirect Channel Data #3

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R/W	TRANS	X
Bit 14	R/W	IDLE	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	LEVEL[3]	X
Bit 10	R/W	LEVEL[2]	X
Bit 9	R/W	LEVEL[1]	X
Bit 8	R/W	LEVEL[0]	X
Bit 7	R/W	FLAG[2]	X
Bit 6	R/W	FLAG[1]	X
Bit 5	R/W	FLAG[0]	X
Bit 4		Unused	X
Bit 3	R/W	XFER[3]	X
Bit 2	R/W	XFER[2]	X
Bit 1	R/W	XFER[1]	X
Bit 0	R/W	XFER[0]	X

This register contains data read from the channel provision RAM after an indirect read operation or data to be inserted into the channel provision RAM in an indirect write operation.

XFER[3:0]:

The indirect channel transfer size (XFER[3:0]) specifies the minimum FIFO free space, less 1, before the partial packet processor begins requesting data from the DMA port. The channel transfer size to be written to the channel provision RAM, in an indirect write operation, must be set up in this register before triggering the write. When the channel FIFO free space reaches the limit specified by XFER[3:0], the partial packet processor will make a request to the DMA port for one XFER[3:0] amount of data. FIFO free space is measured in the number of blocks with each block being 16 bytes in size. XFER[3:0] reflects the value written until the completion of a subsequent indirect channel read operation.

XFER[3:0] must be less than or equal to the start transmission level specified by LEVEL[3:0] and TRANS.

FLAG[2:0]:

The flag insertion control (FLAG[2:0]) configures the minimum number of flags or bytes of idle bits the HDLC processor inserts between HDLC packets. The value of FLAG[2:0] to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. The minimum number of flags or bytes of idle (8 bits of 1's) inserted between HDLC packets is shown in the table below. FLAG[2:0] reflects the value written until the completion of a subsequent indirect channel read operation.

Table 20 - FLAG[2:0] Settings

FLAG[2:0]	Minimum Number of Flag/Idle Bytes
000	1 flag / 0 Idle byte
001	2 flags / 0 idle byte
010	4 flags / 2 idle bytes
011	8 flags / 6 idle bytes
100	16 flags / 14 idle bytes
101	32 flags / 30 idle bytes
110	64 flags / 62 idle bytes
111	128 flags / 126 idle bytes

LEVEL[3:0]:

The indirect channel FIFO trigger level (LEVEL[3:0]), in concert with the TRANS bit, configure the various channel FIFO free space levels which trigger the HDLC processor to start transmission of a HDLC packet as well as trigger the partial packet buffer to request data from the upstream device as shown in the following table. The channel FIFO trigger level to be written to the channel provision RAM, in an indirect write operation, must be set up in this register before triggering the write. LEVEL[3:0] reflects the value written until the completion of a subsequent indirect channel read operation.

The HDLC processor starts transmitting a packet when the channel FIFO free space is less than or equal to the level specified in the appropriate Start Transmission Level column of the following table or when an end of a packet is stored in the channel FIFO. When the channel FIFO free space is greater than or equal to the level specified in the Starving Trigger Level column of the following table and the HDLC processor is transmitting a packet and an end of a packet is not stored in the channel FIFO, the partial packet buffer makes expedited requests to the upstream device to retrieve XFER[3:0] + 1 blocks of data.

IDLE:

The interframe time fill bit (IDLE) configures the HDLC processor to use flag bytes or HDLC idle as the interframe time fill between HDLC packets. The value of IDLE to be written to the channel provision RAM, in an indirect channel write operation, must be set up in this register before triggering the write. When IDLE is set low, the HDLC processor uses flag bytes as the interframe time fill. When IDLE is set high, the HDLC processor uses HDLC idle (all one's bit with no bit-stuffing pattern is transmitted) as the interframe time fill. IDLE reflects the value written until the completion of a subsequent indirect channel read operation.

TRANS:

The indirect transmission start bit (TRANS), in concert with the LEVEL[3:0] bits, configure the various channel FIFO free space levels which trigger the HDLC processor to start transmission of a HDLC packet as well as trigger the partial packet buffer to request data from the upstream device as shown in the following table. The transmission start mode to be written to the channel provision RAM, in an indirect write operation, must be set up in this register before triggering the write. TRANS reflects the value written until the completion of a subsequent indirect channel read operation.

The HDLC processor starts transmitting a packet when the channel FIFO free space is less than or equal to the level specified in the appropriate Start Transmission Level column of the following table or when an end of a packet is stored in the channel FIFO. When the channel FIFO free space is greater than or equal to the level specified in the Starving Trigger Level column of the following table and the HDLC processor is transmitting a packet and an end of a packet is not stored in the channel FIFO, the partial packet buffer makes expedited requests to the upstream device to retrieve XFER[3:0] + 1 blocks of data.

To prevent lockup, the channel transfer size (XFER[3:0]) can be configured to be less than or equal to the start transmission level set by LEVEL[3:0] and TRANS. Alternatively, the channel transfer size can be set, such that, the total number of blocks in the logical channel FIFO minus the start transmission level is an integer multiple of the channel transfer size. The starving trigger level must always be set to a number of blocks greater than or equal to the channel transfer size.

Table 21 - Level[3:0]/TRANS Settings

LEVEL[3:0]	Starving Trigger Level	Start Transmission Level (TRANS=0)	Start Transmission Level (TRANS=1)
0010	4 Blocks (64 bytes free)	Invalid	2 Blocks (32 bytes free)
0011	6 Blocks (96 bytes free)	4 Blocks (64 bytes free)	Invalid
0100	8 Blocks (128 bytes free)	6 Blocks (96 bytes free)	4 Blocks (64 bytes free)
0101	12 Blocks (192 bytes free)	8 Blocks (128 bytes free)	6 Blocks (96 bytes free)
0110	16 Blocks (256 bytes free)	12 Blocks (192 bytes free)	8 Blocks (128 bytes free)
0111	24 Blocks (384 bytes free)	16 Blocks (256 bytes free)	12 Blocks (192 bytes free)
1000	32 Blocks (512 bytes free)	24 Blocks (384 bytes free)	16 Blocks (256 bytes free)
1001	48 Blocks (768 bytes free)	32 Blocks (512 bytes free)	24 Blocks (384 bytes free)
1010	64 Blocks (1 Kbytes free)	48 Blocks (768 bytes free)	32 Blocks (512 bytes free)
1011	96 Blocks (1.5 Kbytes free)	64 Blocks (1 Kbytes free)	48 Blocks (768 bytes free)

LEVEL[3:0]	Starving Trigger Level	Start Transmission Level (TRANS=0)	Start Transmission Level (TRANS=1)
1100	192 Blocks (3 Kbytes free)	128 Blocks (2 Kbytes free)	96 Blocks (1.5 Kbytes free)

Register 0x390 : THDL Indirect Channel Data Register #4

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R	DMAEXP	X
Bit 14	R	DMAREQ	X
Bit 13	R	AVAIL	X
Bit 12	R	EOP[12]	X
Bit 11	R	EOP[11]	X
Bit 10	R	EOP[10]	X
Bit 9	R	EOP[9]	X
Bit 8	R	EOP[8]	X
Bit 7	R	EOP[7]	X
Bit 6	R	EOP[6]	X
Bit 5	R	EOP[5]	X
Bit 4	R	EOP[4]	X
Bit 3	R	EOP[3]	X
Bit 2	R	EOP[2]	X
Bit 1	R	EOP[1]	X
Bit 0	R	EOP[0]	X

This register contains data read from the channel provision RAM after an indirect read operation.

EOP[12:0]:

The indirect channel FIFO end of packet count (EOP[12:0]) specifies the number of end of packets stored in the channel FIFO. The value of EOP[12:0] is expressed in a signed 2's complement form with EOP[12] as the sign bit. EOP[12:0] reflects the value of the last indirect channel read operation.

The EOP[12:0] register bits are used for test purposes only.

AVAIL:

The indirect channel data available flag (AVAIL) indicates when sufficient packet data is store in the channel FIFO for the HDLC processor to start transmission. When AVAIL is high, the channel FIFO free space is less than or equal to the level specified by the TRANS and LEVEL[3:0] register bits or at least one end of packet is store in the channel FIFO. In this case, the HDLC processor starts transmission when AVAIL is high and sufficient flags/idle specified by FLAG[2:0] have been transmitted. When AVAIL is low, the channel FIFO free space is greater than the level specified by the TRANS and LEVEL[3:0] register bits and no end of packets are store in the channel FIFO. In this case, the HDLC processor will not start transmitting a new packet or will finish transmitting the current packet. AVAIL reflects the value of the last indirect channel read operation.

The AVAIL register bit is used for test purposes only.

DMAREQ:

The indirect channel service request flag (DMAREQ) indicates when sufficient free space exists in the channel FIFO to perform a DMA operation. When DMAREQ is high, the channel free space is greater than or equal to 32 bytes. When DMAREQ is low, the channel free space is less than 32 bytes. DMAREQ reflects the value of the last indirect channel read operation.

The DMAREQ register bit is used for test purposes only.

DMAEXP:

The indirect channel expedite service request flag (DMAEXP) indicates when the channel FIFO requires an expedited DMA operation. When DMAEXP is high, the channel free space is greater than or equal to the level specified by LEVEL[3:0] and the HDLC processor is transmitting a packet and the end of a packet is not store in the channel FIFO. When DMAEXP is low, the channel free space is less than the level specified by LEVEL[3:0], or the HDLC processor is not transmitting or an end of a packet is store in the channel FIFO. DMAEXP reflects the value of the last indirect channel read operation.

The DMAEXP register bit is used for test purposes only.

Register 0x394 : THDL Indirect Channel Data Register #5

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R	FREE[12]	X
Bit 11	R	FREE[11]	X
Bit 10	R	FREE[10]	X
Bit 9	R	FREE[9]	X
Bit 8	R	FREE[8]	X
Bit 7	R	FREE[7]	X
Bit 6	R	FREE[6]	X
Bit 5	R	FREE[5]	X
Bit 4	R	FREE[4]	X
Bit 3	R	FREE[3]	X
Bit 2	R	FREE[2]	X
Bit 1	R	FREE[1]	X
Bit 0	R	FREE[0]	X

This register contains data read from the channel provision RAM after an indirect read operation.

FREE[12:0]:

The indirect channel FIFO free space (FREE[12:0]) indicates the number of empty or free blocks in the channel FIFO. The value of FREE[12:0] is expressed in a signed 2's complement form with FREE[12] as the sign bit. FREE[12:0] reflects the value of the last indirect channel read operation.

The FREE[12:0] register bits are used for test purposes only.

Register 0x398 : THDL Indirect Channel Data Register #6

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	WPTR[11]	X
Bit 10	R	WPTR[10]	X
Bit 9	R	WPTR[9]	X
Bit 8	R	WPTR[8]	X
Bit 7	R	WPTR[7]	X
Bit 6	R	WPTR[6]	X
Bit 5	R	WPTR[5]	X
Bit 4	R	WPTR[4]	X
Bit 3	R	WPTR[3]	X
Bit 2	R	WPTR[2]	X
Bit 1	R	WPTR[1]	X
Bit 0	R	WPTR[0]	X

This register contains data read from the channel provision RAM after an indirect read operation.

WPTR[11:0]:

The channel FIFO writer pointer (WPTR[11:0]) is the block number in the channel FIFO to which the write processor is storing packet data. WPTR[11:0] reflects the value of the last indirect channel read operation.

The WPTR[11:0] register bits are used for test purposes only.

Register 0x3A0 : THDL Indirect Block Select

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R	BBUSY	0
Bit 14	R/W	BRWB	0
Bit 13 To Bit 12		Unused	X
Bit 11	R/W	BLOCK[11]	0
Bit 10	R/W	BLOCK[10]	0
Bit 9	R/W	BLOCK[9]	0
Bit 8	R/W	BLOCK[8]	0
Bit 7	R/W	BLOCK[7]	0
Bit 6	R/W	BLOCK[6]	0
Bit 5	R/W	BLOCK[5]	0
Bit 4	R/W	BLOCK[4]	0
Bit 3	R/W	BLOCK[3]	0
Bit 2	R/W	BLOCK[2]	0
Bit 1	R/W	BLOCK[1]	0
Bit 0	R/W	BLOCK[0]	0

This register provides the block number used to access the block pointer RAM. Writing to this register triggers an indirect block register access.

BLOCK[11:0]:

The indirect block number (BLOCK[11:0]) indicate the block to be configured or interrogated in the indirect access.

BRWB:

The block indirect access control bit (BRWB) selects between a configure (write) or interrogate (read) access to the block pointer RAM. Writing a logic zero to BRWB triggers an indirect block write operation. Data to be written is taken from the Indirect Block Data register. Writing a logic one to BRWB triggers an indirect block read operation. The data read can be found in the Indirect Block Data register.

BBUSY:

The indirect access status bit (BBUSY) reports the progress of an indirect access. BBUSY is set high when this register is written to trigger an indirect access, and will stay high until the access is complete. At which point, BBUSY will be set low. This register should be polled to determine when data from an indirect read operation is available in the THDL Indirect Block Data register or to determine when a new indirect write operation may commence.

Register 0x3A4 : THDL Indirect Block Data

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R/W	Reserved	0
Bit 14 To Bit 12		Unused	X
Bit 11	R/W	BPTR[11]	0
Bit 10	R/W	BPTR[10]	0
Bit 9	R/W	BPTR[9]	0
Bit 8	R/W	BPTR[8]	0
Bit 7	R/W	BPTR[7]	0
Bit 6	R/W	BPTR[6]	0
Bit 5	R/W	BPTR[5]	0
Bit 4	R/W	BPTR[4]	0
Bit 3	R/W	BPTR[3]	0
Bit 2	R/W	BPTR[2]	0
Bit 1	R/W	BPTR[1]	0
Bit 0	R/W	BPTR[0]	0

This register contains data read from the transmit block pointer RAM after an indirect block read operation or data to be inserted into the transmit block pointer RAM in an indirect block write operation.

BPTR[11:0]:

The indirect block pointer (BPTR[11:0]) configures the block pointer of the block specified by the Indirect Block Select register. The block pointer to be written to the transmit block pointer RAM, in an indirect write operation, must be set up in this register before triggering the write. The block pointer value is the block number of the next block in the linked list. A circular list of blocks must be formed in order to use the block list as a channel FIFO buffer. FPTR[11:0] reflects the value written until the completion of a subsequent indirect block read operation.

When provisioning a channel FIFO, all blocks pointers must be re-written to properly initialize the FIFO.

Register 0x3B0 : THDL Configuration

Bit	Type	Function	Default
Bit 31 To Bit 10		Unused	X
Bit 9	R/W	BIT8	0
Bit 8	R/W	TSTD	0
Bit 7	R/W	Reserved	0
Bit 6 To Bit 4		Unused	X
Bit 3 To Bit 0	R/W	Reserved	0

This register configures all provisioned channels.

Reserved:

The reserved bits must be set low for correct operation of the FREEDM 84A1024 device.

TSTD:

The telecom standard bit (TSTD) controls the bit ordering of the HDLC data transferred on the transmit APPI. When TSTD is set low, the least significant bit of the each byte on the transmit APPI bus (AD[0] and AD[8]) is the first HDLC bit transmitted and the most significant bit of each byte (AD[7] and AD[15]) is the last HDLC bit transmitted (datacom standard). When TSTD is set high, AD[0] and AD[8] are the last HDLC bit transmitted and AD[7] and AD[15] are the first HDLC bit transmitted (telecom standard).

BIT8:

The least significant stuff control bit (BIT8) carries the value placed in the least significant bit of each octet when the HDLC processor is configured (7BIT set high) to stuff the least significant bit of each octet in the corresponding transmit link (TD[n]). When BIT8 is set high, the least significant bit (last bit of each octet transmitted) is forced high. When BIT8 is set low, the least significant bit is forced low. BIT8 is ignored when 7BIT is set low.

Register 0x400 : TCAS Indirect Context RAM Link Select

Bit	Type	Function	Default
Bit 31 To Bit 12		Unused	X
Bit 11	R	BUSY	X
Bit 10	R/W	RWB	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	SBI	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

This register provides the link number used to access the TCAS Context RAM. Writing to this register triggers an indirect register access.

Reserved:

The reserved bits must be set low for correct operation of the FREEDM 84A1024 device.

TRIB[4:0], SPE[1:0] and SBI:

The TRIB[4:0], SPE[1:0] and SBI fields are used to fully specify to which SBI tributary the context RAM write or read operation will apply.

TRIB[4:0] specifies the SBI tributary number within the SBI SPE as specified by the SPE[1:0] and SBI fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. SBI must be written to a logic one in the FREEDM 84A1024 device.

RWB:

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the context RAM. Writing a logic zero to RWB triggers an indirect write operation. Data to be written is taken from the LEN and SBI_MODE[2:0] bits of the TCAS Indirect Context RAM Data register. Writing a logic one to RWB triggers an indirect read operation. The data read can be found in the LEN and SBI_MODE[2:0] bits of the TCAS Indirect context RAM Data register.

BUSY:

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when this register is written, to trigger an indirect access, and will stay high until the access is complete. At which point, BUSY will be set low. This register should be polled to determine when data from an indirect read operation is available in the TCAS Indirect Data register or to determine when a new indirect write operation may commence.

Register 0x404 : TCAS Indirect Context RAM Data

Bit	Type	Function	Default
Bit 31 To Bit 5		Unused	X
Bit 4	R/W	SYNC	0
Bit 3	R/W	SBI_MODE[2]	0
Bit 2	R/W	SBI_MODE[1]	0
Bit 1	R/W	SBI_MODE[0]	0
Bit 0	R/W	LEN	0

This register provides the link enable bit and the frame mode or data type associated to this particular link in the TCAS context RAM.

SYNC:

The SYNC bit determines whether the link is operating in synchronous mode or asynchronous mode. When set low the link is set to asynchronous mode. When set high the TCAS will to synchronize the link output data according to the synchronous mode requirements of the SBI bus. This bit only applies to framed T1 or E1 links.

SBI_MODE[2:0]:

The Frame Mode bits (SBI_MODE [2:0]), report the type of data to a specific link to be configured accordingly according to the table below.

Table 22 - SBI Mode

SBI_MODE [2:0]	Configuration
000	Single unframed unchannelized DS-3/Serial Link
001	28 Unframed T1/J1 links
010	21 Unframed E1 links
011	Unused
100	Single framed unchannelized DS-3
101	28 Framed Channelized T1/J1 links
110	21 Framed Channelized E1 links
111	unused

LEN:

The Link Enable bit (LEN) when set Low disables the link. If enabled, the corresponding serial link must be disabled by clearing the appropriate SLINK[n] bit in register 0x414.

Register 0x408 : TCAS Channel Provision RAM Select

Bit	Type	Function	Default
Bit 31 To Bit 13		Unused	X
Bit 12	R/W	SBI_MODE[2]	0
Bit 11	R/W	SBI_MODE[1]	0
Bit 10	R/W	SBI_MODE[0]	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	SBI	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

This register provides the link number used to access the TCAS channel provision RAM.

Reserved:

The reserved bits must be set low for correct operation of the FREEDM 84A1024 device.

SBI_MODE[2:0]:

This field must be set to the same value as Bits3:1 in Register 0x404.

TRIB[4:0], SPE[1:0] and SBI:

The TRIB[4:0], SPE[1:0] and SBI fields are used to fully specify to which SBI tributary the context RAM write or read operation will apply.

TRIB[4:0] specifies the SBI tributary number within the SBI SPE as specified by the SPE[1:0] and SBI fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. SBI must be written to a logic one in the FREEDM 84A1024 device.

Register 0x40C : TCAS Indirect Channel Provision RAM Timeslot and Control Select

Bit	Type	Function	Default
Bit 31 To Bit 7		Unused	X
Bit 6	R	BUSY	0
Bit 5	R/W	RWB	0
Bit 4	R/W	TSLOT[4]	0
Bit 3	R/W	TSLOT[3]	0
Bit 2	R/W	TSLOT[2]	0
Bit 1	R/W	TSLOT[1]	0
Bit 0	R/W	TSLOT[0]	0

This register provides the link timeslot number and control bits used to access the TCAS channel provision RAM. Writing to this register triggers an indirect register access.

TSLOT[4:0]:

The indirect timeslot number bits (TSLOT[4:0]) indicate the timeslot to be configured or interrogated in the indirect access. For a channelized T1/J1 link, timeslots 0 to 23 are valid. For a channelized E1 link, timeslots 0 to 31 are valid. For unchannelized links, only timeslot 0 is valid.

RWB:

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the TCAS channel provision RAM. The address to the TCAS channel provision RAM is constructed by combining the TSLOT[4:0] and LINK[9:0] bits. Writing a logic zero to RWB triggers an indirect write operation. Data to be written is taken from the PROV, and the CHAN[9:0] bits of the TCAS Indirect Channel Data register. Writing a logic one to RWB triggers an indirect read operation. Addressing of the RAM is the same as in an indirect write operation. The data read can be found in the PROV, and the CHAN[9:0] bits of the TCAS Indirect Channel Data register.

BUSY:

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when this register is written, to trigger an indirect access, and will stay high until the access is complete. At which point, BUSY will be set low. This register should be polled to determine when data from an indirect read operation is available in the Indirect Data register or to determine when a new indirect write operation may commence.

Register 0x410: TCAS Indirect Channel Data enable

Bit	Type	Function	Default
Bit 31 To Bit 11		Unused	X
Bit 10	R/W	PROV	0
Bit 9	R/W	CHAN [9]	0
Bit 8	R/W	CHAN [8]	0
Bit 7	R/W	CHAN [7]	0
Bit 6	R/W	CHAN [6]	0
Bit 5	R/W	CHAN [5]	0
Bit 4	R/W	CHAN [4]	0
Bit 3	R/W	CHAN [3]	0
Bit 2	R/W	CHAN [2]	0
Bit 1	R/W	CHAN [1]	0
Bit 0	R/W	CHAN [0]	0

This register contains the data read from the TCAS channel provision RAM after an indirect read operation or the data to be inserted into the TCAS channel provision RAM in an indirect write operation.

CHAN[9:0]:

The indirect data bits (CHAN[9:0]) report the channel number read from the channel provision RAM after an indirect read operation has completed. Channel number to be written to the channel provision RAM in an indirect write operation must be set up in this register before triggering the write. CHAN[9:0] reflects the value written until the completion of a subsequent indirect read operation.

PROV:

The indirect provision enable bit (PROV) reports the channel provision enable flag read from the TCAS channel provision RAM after an indirect read operation has completed. The provision enable flag to be written to the TCAS channel provision RAM in an indirect write operation must be set up in this register before triggering the write. When PROV is set high, the current request is processed as part of the channel as indicated by CHAN[9:0]. When PROV is set low, the current timeslot does not belong to any channel and the request is ignored. PROV reflects the value written until the completion of a subsequent indirect read operation. For unchannelized links, a read of any TSLOT will report the value in TSLOT[4:0]=00000.

Register 0x414: TCAS Serial Link Enable Register

Bit	Type	Function	Default
Bit 15 to Bit 9		Unused	X
Bit 8	R/W	SLINK[8]	0
Bit 7 to Bit 5		Unused	X
Bit 4	R/W	SLINK [4]	0
Bit 3 to Bit 1		Unused	X
Bit 0	R/W	SLINK [0]	0

This register allows the selection of the serial link to be activated.

SLINK[0], SLINK[4], SLINK[8]:

The Tx Serial Link selection (SLINK[8,4,0]) bits specify the serial links to be activated. When SLINK[x] is set high, the data on the particular selected serial link will be transmitted, otherwise the serial link is ignored. When a serial link is enabled, the corresponding SBI/SPE on the SBI bus must be disabled. Serial links map to SBI links according to the following table:

Table 23 - Serial Link to SBI Link Mapping

Serial Link	SPE No.	SBI Trib No.
0	1	1
4	2	1
8	3	1

Register 0x418 : TCAS Idle Time-slot Fill Data

Bit	Type	Function	Default
Bit 31 To Bit 8		Unused	X
Bit 7	R/W	FDATA[7]	1
Bit 6	R/W	FDATA[6]	1
Bit 5	R/W	FDATA[5]	1
Bit 4	R/W	FDATA[4]	1
Bit 3	R/W	FDATA[3]	1
Bit 2	R/W	FDATA[2]	1
Bit 1	R/W	FDATA[1]	1
Bit 0	R/W	FDATA[0]	1

This register contains the data to be written to disabled time-slots of a channelized link.

FDATA[7:0]:

The fill data bits (FDATA[7:0]) are transmitted during disabled (PROV set low) time-slots of channelized links.

Register 0x580: RAPI Control Register

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R/W	ENABLE	0
Bit 14	R/W	STATEN	0
Bit 13	R/W	Reserved	0
Bit 12 To Bit 6		Unused	X
Bit 5		ANYPHYL	0
Bit 4		Unused	X
Bit 3	R/W	ALL1ENB	1
Bit 2 To Bit 0		Unused	X

The Control Register is used to set the operating mode of RAPI-12. It is used to configure the final word of a packet in APPI. It is also used to enable the RAPI-12.

ALL1ENB:

The All Ones Enable bit (ALL1ENB) is used to configure the device address space of the RAPI-12 in level-2 APPI. It is not used in level-3 APPI. When ALL1ENB is high in level-2 APPI, the all ones address (RXADDR[3:0] = “1111”) is reserved as null address to resolve contention for ANY-PHY bus, and it can not be assigned to any RAPI-12. When ALL1ENB is low in level-2 APPI, the all ones address is not treated as null address, and it can be assigned to one RAPI-12; contention for ANY-PHY bus must be resolved by external logic.

ANYPHYL:

The ANY PHY Level select bit allows selection between ANY PHY Level 2 and ANY PHY Level 3.

Table 24 - ANY-PHY Encoding

ANY-PHY	ANY-PHY Level
0	Level 2
1	Level 3

Reserved:

The reserved bits must be set low for correct operation of the FREEDM 84A1024 device.

STATEN:

The status enable bit (STATEN) enables the RAPI-12 to provide the status of an erred packet on RXDATA[7:0] during transfer of the final word of that packet on the receive APPI (REOP and RERR high). When STATEN is set high, the RAPI-12 overwrites RXDATA[7:0] of the final word of an erred packet with status information for that packet. When STATEN is set low, the RAPI-12 does not report detailed status information for an erred packet. The RXDATA[15:0] connector description details the erred packet status reporting when STATEN is set high.

ENABLE:

The Enable bit (ENABLE) enables normal operation of the RAPI-12. When ENABLE is set low, the RAPI-12 will complete the current data transfer and will respond to any further transactions on the APPI but will not send any new data. When ENABLE is set high, the RAPI-12 operates normally.

Register 0x584: RAPI Device Base Address Register

Bit	Type	Function	Default
Bit 31 To Bit 4		Unused	X
Bit 3	R/W	DBADDR[3]	0
Bit 2	R/W	DBADDR[2]	0
Bit 1	R/W	DBADDR[1]	0
Bit 0	R/W	DBADDR[0]	0

The Device Base Address Register is used to configure the address space occupied by the FREEDM 84A1024 device for device selection.

DBADDR[3:0]:

The Device Base Address bits (DBADDR[3:0]) configure the address space occupied by the FREEDM 84A1024 device for purposes of responding to receive polling and receive device selection. During polling in Level-2 APPI, the DBADDR[3:0] bits are used to respond to polling via the RXADDR[3:0] pins. Polling is not used in Level-3 APPI. During device selection, the DBADDR[3:0] bits are used to select a FREEDM 84A1024 device, enabling it to output data on the receive APPI.

Register 0x588: RAPI Channel Base Address Register

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R/W	CBADDR[15]	0
Bit 14	R/W	CBADDR[14]	0
Bit 13	R/W	CBADDR[13]	0
Bit 12	R/W	CBADDR[12]	0
Bit 11	R/W	CBADDR[11]	0
Bit 10	R/W	CBADDR[10]	0
Bit 9	R/W	CBADDR[9]	0
Bit 8	R/W	CBADDR[8]	0
Bit 7	R/W	CBADDR[7]	0
Bit 6	R/W	CBADDR[6]	0
Bit 5	R/W	CBADDR[5]	0
Bit 4	R/W	CBADDR[4]	0
Bit 3	R/W	CBADDR[3]	0
Bit 2	R/W	CBADDR[2]	0
Bit 1	R/W	CBADDR[1]	0
Bit 0	R/W	CBADDR[0]	0

The Channel Base Address Register is used to configure the address space occupied by the FREEDM 84A1024 device for receive polling.

CBADDR[15:0]:

The Channel Base Address bits (CBADDR[15:0]) configure the FREEDM 84A1024 to support channel numbers starting from the channel Base Address. The channel numbers used by the FREEDM 84A1024 will be CBADDR[15:0] to CBADDR[15:0]+1023.

Register 0x58C: RAPI Status Register

Bit	Type	Function	Default
Bit 31 To Bit 2		Unused	X
Bit 1	R	UDRUN	1
Bit 0	R	Reserved	0

The Status Register is used to record the status of RAPI-12.

UDRUN:

The underrun bit (UDRUN) is used to record events when the circular FIFO in RAPI-12 is empty.

Reserved:

The reserved bits must be set low for correct operation of the FREEDM 84A1024 device.

Register 0x5C0 : SBI EXTRACT Control

Bit	Type	Function	Default
Bit 31 To Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Unused	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	SBI_PAR_CTL	1

This register controls the operation of the SBI EXTRACT block.

SBI_PAR_CTL

The SBI_PAR_CTL bit is used to configure the Parity mode for checking of the SBI parity signal, DDP as follows: When SBI_PAR_CTL is '0' parity is even. When SBI_PAR_CTL is '1' parity is odd.

Reserved:

The reserved bits must be set according to the table below for correct operation of the FREEDM 84A1024 device.

Table 25 - Reserved/Unused bit Settings

Bit	Setting
3	1
2	0
1	0

Register 0x5D4 : SBI EXTRACT Tributary Indirect Access Address

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R	BUSY	0
Bit 14	R/W	RWB	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	SBI	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

This register provides the receive SBI, SPE and link number used to access the SBI EXTRACT tributary control configuration RAM.

TRIB[4:0], SPE[1:0] and SBI:

The TRIB[4:0], SPE[1:0] and SBI fields are used to fully specify to which SBI tributary the Control register write or read operation will apply.

TRIB[4:0] specifies the SBI tributary number within the SBI SPE as specified by the SPE[1:0] and SBI fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. SBI must be written to a logic one in the FREEDM 84A1024 device.

Reserved:

The reserved bits must be set low for correct operation of the FREEDM 84A1024 device.

RWB:

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the tributary control configuration RAM. Writing a '0' to RWB triggers an indirect write operation. Data to be written is taken from the SBI EXTRACT Tributary Indirect Access Data Register. Writing a '1' to RWB triggers an indirect read operation. The data read can be found in the SBI EXTRACT Tributary Indirect Access Data Register.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the Extract RAM Indirect Access Address Register triggers an indirect access and will stay high until the access is complete. This bit should be polled to determine when data from an indirect read operation is available in the Extract RAM Indirect Access Control Data Register. In a write access this bit should be polled to determine when a new operation may commence.

Register 0x5DC : SBI EXTRACT Tributary RAM Indirect Access Data

Bit	Type	Function	Default
Bit 31 To Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TRIB_TYP[1]	0
Bit 2	R/W	TRIB_TYP[0]	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	ENBL	0

This register contains data read from the SBI EXTRACT tributary control configuration RAM after an indirect read operation or data to be written to the tributary control configuration RAM in an indirect write operation.

ENBL

The ENBL bit is used to enable the EXSBI to take tributary data from an SBI tributary and transmit that data to the SBIIP link.

Reserved:

The reserved bits must be set low for correct operation of the FREEDM 84A1024 device.

TRIB_TYP[1:0]

The TRIB_TYP[1:0] field is used to specify the characteristics of the SBI tributary as shown in Table 26 below:

Table 26 - TRIB_TYP Encoding

TRIB_TYP[1:0]	Tributary type
00	Reserved
01	Framed
10	Unframed
11	Reserved

Register 0x5E0H: SBI EXTRACT SBI SPE Configuration Register

Bit	Type	Function	Default
Bit 31 To Bit 12	R	Unused	0
Bit 11	R/W	SPE3_EN	0
Bit 10	R/W	SPE3_TYP[2]	0
Bit 9	R/W	SPE3_TYP [1]	0
Bit 8	R/W	SPE3_TYP [0]	0
Bit 7	R/W	SPE2_EN	0
Bit 6	R/W	SPE2_TYP[2]	0
Bit 5	R/W	SPE2_TYP [1]	0
Bit 4	R/W	SPE2_TYP [0]	0
Bit 3	R/W	SPE1_EN	0
Bit 2	R/W	SPE1_TYP[2]	0
Bit 1	R/W	SPE1_TYP [1]	0
Bit 0	R/W	SPE1_TYP [0]	0

SPE1_EN, SPE2_EN, SPE3_EN:

Enables SPE1, SPE2 and SPE3 respectively. When these bits are set to 0 the respective SPE is disabled. When these bits are set to 1 the respective SPE is enabled. When an SPE is enabled each individual tributary within an SPE can be selectively enabled via the Extract Tributary RAM Indirect Access Control Data register. These bits must be written in a second write after the SPE*_TYP[2:0] bits have been set.

SPE1_TYP[2:0], SPE2_TYP[2:0], SPE3_TYP[2:0]:

SPE1_TYP[2:0], SPE2_TYP[2:0] and SPE3_TYP[2:0] select the SPE type for the three SPEs respectively. The types for each SPE are independently configured with possible types being T1, E1, DS3 or Fractional DS3. The setting for SPEx_TYP[2:0] are:

Table 27 - SBI EXTRACT SPE_TYP[2:0]

SPEx_TYP[2:0]	Payload Type
X00	28 T1/J1 links
X01	21 E1links
010	Single DS3 Link
011	Unused
11X	Fractional Rate

Register 0x600H: TAPI Control Register

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R/W	ENABLE	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12 To Bit 6		Unused	X
Bit 5	R/W	ANYPHYL	0
Bit 4	R/W	MODE	0
Bit 3 To Bit 1		Unused	X
Bit 0	R/W	Reserved.	0

The Control Register is used to set TAPI-12 mode. The Control Register is also used to enable the TAPI-12.

Reserved.

Reserved. The Reserved bit must be set low for correct operation of the FREEDM 84A1024 device.

MODE:

The mode bit (MODE) is used to configure operating modes of TAPI-12. When MODE is set high, TAPI-12 operates in non-blocking mode; that is, TAPI-12 will only deassert TRDY if it cannot accept 64 bytes (1 FIFO block) of data. When MODE is set low, TAPI-12 operates in blocking mode; that is, TAPI-12 will deassert TRDY if the free space in the circular FIFO is less than the data transfer burst length when TSX is sampled high. This bit should always be set to a 0 for guaranteed operation.

ANYPHYL:

The ANY PHY Level select bit allows selection between ANY PHY L2 and ANY PHY L3.

Table 28 - ANY-PHY Encoding

ANY-PHY	ANY-PHY Level
0	Level 2
1	Level 3

Reserved:

The reserved bits must be set low for correct operation of the FREEDM 84A1024 device.

ENABLE:

The Enable bit (ENABLE) enables normal operation of the TAPI-12. When ENABLE is set low, the TAPI-12 will complete the current data transfer and will respond to any further transactions on the APPI normally (by setting TRDY high), but will ignore any data. When ENABLE is set high, the TAPI-12 operates normally.

Register 0x604 : TAPI Indirect Channel Provisioning Register

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13 To Bit 10		Unused	X
Bit 9	R/W	CHAN[9]	0
Bit 8	R/W	CHAN[8]	0
Bit 7	R/W	CHAN[7]	0
Bit 6	R/W	CHAN[6]	0
Bit 5	R/W	CHAN[5]	0
Bit 4	R/W	CHAN[4]	0
Bit 3	R/W	CHAN[3]	0
Bit 2	R/W	CHAN[2]	0
Bit 1	R/W	CHAN[1]	0
Bit 0	R/W	CHAN[0]	0

The Indirect Channel Provisioning Register provides the channel number used to access the TAPI-12 channel provisioning RAM. Writing to this register triggers an indirect channel register access.

CHAN[9:0]:

The indirect channel number bits (CHAN[9:0]) indicate the channel to be configured or interrogated in the indirect access.

RWB:

The Read/Write Bar (RWB) bit selects between a provisioning/unprovisioning operation (write) or a query operation (read). Writing a logic 0 to RWB triggers the provisioning or unprovisioning of the channel specified by CHAN[9:0]. Writing a logic 1 to RWB triggers a query of the channel specified by CHAN[9:0].

BUSY:

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when this register is written to trigger an indirect access, and will stay high until the access is complete. At which point, BUSY will be set low. This register should be polled to determine when data from an indirect read operation is available or to determine when a new indirect write operation may commence.

Register 0x608 : TAPI Indirect Channel Data Register

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R/W	PROV	0
Bit 14 To Bit 8		Unused	X
Bit 7	R/W	BLEN[7]	X
Bit 6	R/W	BLEN[6]	X
Bit 5	R/W	BLEN[5]	X
Bit 4	R/W	BLEN[4]	X
Bit 3	R/W	BLEN[3]	X
Bit 2	R/W	BLEN[2]	X
Bit 1	R/W	BLEN[1]	X
Bit 0	R/W	BLEN[0]	X

The TAPI Indirect Channel Data Register contains data read from the TAPI-12 channel provision RAM after an indirect read operation or data to be written to channel provision RAM in an indirect write operation.

BLEN[7:0]:

The channel burst length (BLEN[7:0]) bits report the data transfer burst length read from the TAPI-12 channel provision RAM after an indirect read operation has completed. The data transfer burst length specifies the length (in bytes, less one) of burst data transfers on the transmit APPI which are not terminated by the assertion of TEOP. The data transfer burst length can be specified on a per-channel basis. The data transfer burst length to be written to the channel provision RAM in an indirect write operation must be set up in this register before triggering the write. BLEN[7:0] reflects the value written until the completion of a subsequent indirect read operation. The following values of BLEN[7:0] are valid:

Table 29 - Valid BLEN

BLEN[7:0]	APPI transfer burst length
00111111	64
01111111	128
11111111	256

PROV:

The indirect provision enable bit (PROV) reports the channel provision enable flag read from the TAPI-12 channel provision RAM after an indirect read operation has completed. The provision enable flag to be written to the TAPI-12 channel provision RAM, in an indirect write operation, must be set up in this register before triggering the write. When PROV is set high, the channel as indicated by CHAN[9:0] is provisioned. When PROV is set low, the channel indicated by CHAN[9:0] is unprovisioned. PROV reflects the value written until the completion of a subsequent indirect read operation. Traffic to the FREEDM 84A1024 must be stopped on that channel before that channel is unprovisioned.

Register 0x60C: TAPI Reserved Register

Bit	Type	Function	Default
Bit 31 To Bit 8		Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	1
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved:

The reserved bits must be left at their default value or set to 28H for correct operation of the FREEDM 84A1024 device.

Register 0x610: TAPI Status Register

Bit	Type	Function	Default
Bit 31 To Bit 2		Unused	X
Bit 1	R	Reserved	0
Bit 0	R	FULL	0

The Status Register contains flag bits reflecting the current status of TAPI-12. This register does not remain set when the condition is not present.

FULL:

The full bit (FULL) reports the instantaneous full status of the circular FIFO. It is set high when free space in the circular FIFO is smaller than a complete data segment and TSX is sampled high. It can only be cleared through the microprocessor interface. When full bit is high, it shows that the reader controller has not been able to empty the circular FIFO fast enough to keep pace with the writer controller. When TAPI-12 operates in non-blocking mode, the writer controller risks overflowing the circular FIFO when the full bit is set high.

Reserved:

This bit should be ignored.

Register 0x614: TAPI Base Address Register

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R/W	BADDR[15]	0
Bit 14	R/W	BADDR[14]	0
Bit 13	R/W	BADDR[13]	0
Bit 12	R/W	BADDR[12]	0
Bit 11	R/W	BADDR[11]	0
Bit 10	R/W	BADDR[10]	0
Bit 9	R/W	BADDR[9]	0
Bit 8	R/W	BADDR[8]	0
Bit 7	R/W	BADDR[7]	0
Bit 6	R/W	BADDR[6]	0
Bit 5	R/W	BADDR[5]	0
Bit 4	R/W	BADDR[4]	0
Bit 3	R/W	BADDR[3]	0
Bit 2	R/W	BADDR[2]	0
Bit 1	R/W	BADDR[1]	0
Bit 0	R/W	BADDR[0]	0

The Base Address Register specifies the minimum valid ANY-PHY channel address for TAPI-12.

BADDR[15:0]:

The base address bits (BADDR[15:0]) specifies the minimum valid ANY-PHY channel address residing in TAPI-12. A channel prepend address provided on TXDATA or a polling address provided on TXADDR is deemed out of range if it is greater than the sum of RADDR[15:0] and BADDR[15:0] or less than BADDR[15:0]. BADDR[15:0] must be a multiple of RADDR[15:0]+1 (see TAPI Range Address Register).

Register 0x618: TAPI Range Address Register

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R/W	RADDR[15]	0
Bit 14	R/W	RADDR[14]	0
Bit 13	R/W	RADDR[13]	0
Bit 12	R/W	RADDR[12]	0
Bit 11	R/W	RADDR[11]	0
Bit 10	R/W	RADDR[10]	0
Bit 9	R/W	RADDR[9]	0
Bit 8	R/W	RADDR[8]	0
Bit 7	R/W	RADDR[7]	0
Bit 6	R/W	RADDR[6]	0
Bit 5	R/W	RADDR[5]	0
Bit 4	R/W	RADDR[4]	0
Bit 3	R/W	RADDR[3]	0
Bit 2	R/W	RADDR[2]	0
Bit 1	R/W	RADDR[1]	0
Bit 0	R/W	RADDR[0]	0

The Range Address Register specifies the valid range of ANY-PHY channel address for TAPI-12.

RADDR[15:0]:

The range address bits (RADDR[15:0]) specifies the (valid range-1) of ANY-PHY channel address residing in TAPI-12. A channel prepend address provided on TXDATA or a polling address on TXADDR is deemed out of range if it is greater than the sum of RADDR[15:0] and BADDR[15:0] or less than BADDR[15:0] but must be rounded to a power of 2 – 1. I.e. For a range of 672 or 1024 channels, RADDR[15:0] must be set to the value 0000001111111111.

Register 0x680 : SBI INSERT Control

Bit	Type	Function	Default
Bit 31 To Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	SBI_PAR_CTL	1

This register controls the operation of the SBI INSERT block.

SBI_PAR_CTL:

The SBI_PAR_CTL bit is used to configure the Parity mode for generation of the SBI parity signal, ADP as follows: When SBI_PAR_CTL is '0' parity is even. When SBI_PAR_CTL is '1' parity is odd.

Reserved:

The reserved bits must be set low for correct operation of the FREEDM 84A1024 device.

Register 0x68C : SBI INSERT T1 Frame Pulse Offset Register

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R/W	Reserved	1
Bit 11	R/W	OFFSET_T1[11]	0
Bit 10	R/W	OFFSET_T1[10]	0
Bit 9	R/W	OFFSET_T1[9]	1
Bit 8	R/W	OFFSET_T1[8]	1
Bit 7	R/W	OFFSET_T1[7]	1
Bit 6	R/W	OFFSET_T1[6]	0
Bit 5	R/W	OFFSET_T1[5]	0
Bit 4	R/W	OFFSET_T1[4]	0
Bit 3	R/W	OFFSET_T1[3]	0
Bit 2	R/W	OFFSET_T1[2]	1
Bit 1	R/W	OFFSET_T1[1]	0
Bit 0	R/W	OFFSET_T1[0]	0

This register controls the T1 Frame pulse offset. This register is only required when operating in synchronous mode (SYNCH_TRIB=1).

OFFSET_T1[11:0]:

This parameter must be programmed to OFFSET T1[11:0] = 1400 (decimal) or 0101 0111 1000 (binary) for correct operation of the device.

Reserved:

The reserved bit must be set high for correct operation of the FREEDM 84A1024 device.

Register 0x690 : SBI INSERT E1 Frame Pulse Offset

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R	Unused	0
Bit 13	R	Unused	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	OFFSET_E1[11]	0
Bit 10	R/W	OFFSET_E1[10]	0
Bit 9	R/W	OFFSET_E1[9]	1
Bit 8	R/W	OFFSET_E1[8]	1
Bit 7	R/W	OFFSET_E1[7]	1
Bit 6	R/W	OFFSET_E1[6]	0
Bit 5	R/W	OFFSET_E1[5]	0
Bit 4	R/W	OFFSET_E1[4]	0
Bit 3	R/W	OFFSET_E1[3]	0
Bit 2	R/W	OFFSET_E1[2]	1
Bit 1	R/W	OFFSET_E1[1]	0
Bit 0	R/W	OFFSET_E1[0]	0

This register controls the E1 Frame pulse offset. This register is only required when operating in synchronous mode (SYNCH_TRIB=1).

OFFSET_E1[11:0]:

This parameter must be programmed to OFFSET_E1[11:0] = 1654 (decimal) or 0110 0111 0110 (binary) for correct operation of the device.

Reserved:

The reserved bit must be set low for correct operation of the FREEDM 84A1024 device.

Register 0x694 : SBI INSERT Tributary Indirect Access Address

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R	BUSY	0
Bit 14	R/W	RWB	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	SBI	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

This register provides the transmit SPE and link number used to access the SBI INSERT tributary control configuration RAM.

TRIB[4:0], SPE[1:0] and SBI:

The TRIB[4:0], SPE[1:0] and SBI fields are used to fully specify to which SBI tributary the Control register write or read operation will apply.

TRIB[4:0] specifies the SBI tributary number within the SBI/SPE as specified by the SPE[1:0] and SBI fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. SBI must be written to a logic one in the FREEDM 84A1024 device.

Reserved:

The reserved bits must be set low for correct operation of the FREEDM 84A1024 device.

RWB:

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the tributary control configuration RAM. Writing a '0' to RWB triggers an indirect write operation. Data to be written is taken from the SBI INSERT Tributary Indirect Access Data Register. Writing a '1' to RWB triggers an indirect read operation. The data read can be found in the SBI INSERT Control Tributary RAM Indirect Access Data Register.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the SBI INSERT Tributary Indirect Access Address Register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the SBI INSERT Tributary Indirect Access Data Register or to determine when a new indirect write operation may commence.

Register 0x69C : SBI INSERT Tributary Indirect Access Data

Bit	Type	Function	Default
Bit 31 To Bit 7		Unused	X
Bit 6	R/W	SBIIP_LB	0
Bit 5	R/W	SYNCH_TRIB	0
Bit 4	R/W	CLK_MSTR	0
Bit 3	R/W	TRIB_TYP[1]	0
Bit 2	R/W	TRIB_TYP[0]	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	ENBL	0

This register contains data read from the SBI INSERT tributary control configuration RAM after an indirect read operation or data to be written to the tributary control configuration RAM in an indirect write operation.

ENBL

The ENBL bit is used to enable the Tributary. Writing to an Insert Tributary Control and Status RAM location with the ENBL bit set enables the INSBI to take tributary data from an SBIIP link and transmit that data to the SBI tributary for that link.

Reserved:

The reserved bit must be set low for correct operation of the FREEDM 84A1024 device.

TRIB_TYP[1:0]

The TRIB_TYP[1:0] field is used to specify the characteristics of the SBI tributary as shown in Table 30 below:

Table 30 - TRIB_TYP Encoding

TRIB_TYP[1:0]	Tributary type
00	Reserved
01	Framed
10	Unframed
11	Reserved

CLK_MSTR:

The CLK_MSTR bit configures the SBI tributary to operate as a timing master or slave. Setting CLK_MSTR to 1 configures the tributary as a timing master (AJUST_REQ input ignored). Setting CLK_MSTR to 0 configures the tributary as a timing slave (requests on AJUST_REQ honored).

SYNCH_TRIB:

The SYNCH_TRIB bit is used to indicate whether the tributary is locked to the SBI SPE (i.e. is in synchronous mode). If this bit is set then the tributary is locked. If this bit is not set, then the tributary is free to float. This bit will default to off.

SBIIP_LB:

The SBIIP loopback bit selects the SBIIP extract loopback bus as the source for this tributary. When SBIIP_LB is set to 1 LB_EXT_DATA, LB_EXT_LINKRATE, etc. are used as the input data stream for the selected tributary. When SBIIP_LB is set to 0 the insert SBIIP bus is the source for the selected tributary. Loopbacks are only possible with floating tributaries, i.e. can not be used with synchronous T1 and E1 tributaries.

Note

Any write to a Tributary Control RAM location for a tributary will generate a configuration reset on that tributary, irrespective of whether the data written to the tributary control RAM location is unchanged from the previous value.

Register 0x6A0: SBI INSERT SBI SPE Configuration Register

Bit	Type	Function	Default
Bit 31 To Bit 12	R	Unused	0
Bit 11	R/W	SPE3_EN	0
Bit 10	R/W	SPE3_TYP[2]	0
Bit 9	R/W	SPE3_TYP [1]	0
Bit 8	R/W	SPE3_TYP [0]	0
Bit 7	R/W	SPE2_EN	0
Bit 6	R/W	SPE2_TYP[2]	0
Bit 5	R/W	SPE2_TYP [1]	0
Bit 4	R/W	SPE2_TYP [0]	0
Bit 3	R/W	SPE1_EN	0
Bit 2	R/W	SPE1_TYP[2]	0
Bit 1	R/W	SPE1_TYP [1]	0
Bit 0	R/W	SPE1_TYP [0]	0

SPE1_EN, SPE2_EN, SPE3_EN:

Enables SPE1, SPE2 and SPE3 respectively. When these bits are set to 0 the respective SPE is disabled. When these bits are set to 1 the respective SPE is enabled. When an SPE is enabled each individual tributary within an SPE can be selectively enabled via the Insert Tributary Control Indirect Access Data register.

SPE1_TYP[2:0], SPE2_TYP[2:0], SPE3_TYP[2:0]:

SPE1_TYP[2:0], SPE2_TYP[2:0] and SPE3_TYP[2:0] select the SPE type for the three SPEs respectively. The types for each SPE are independently configured with possible types being T1, E1, DS3 or Fractional Rate. The setting for SPEx_TYP[2:0] are:

Table 31 - SBI INSERT SPE_TYP[2:0]

SPEx_TYP[2:0]	Payload Type
X00	28 T1/J1 Links
X01	21 E1 Links
010	Single DS-3 Link
011	Reserved
11x	Fractional Rate

Register 0x800: Memory Port Control

Bit	Type	Function	Default
Bit 31	R	MPBusy	0
Bit 30 To Bit 29	R/W	MPCommand[1:0]	0
Bit 28 To Bit 27	R/W	MPBurstLength[1:0]	0
Bit 26 To Bit 24	R/W	MPMemSelect[2:0]	0
Bit 23 To Bit 0	R/W	MPQuadAddr[23:0]	0

Writes to this register will start a BUMP2 access to the internal aperture defined by MPMemSelect. The completion of one access is signaled by BUMP2 asserting MPBusy to state low. During an internal access, while MPBusy is high, all BUMP2 Control Registers are accessible by the microprocessor.

MPQuadAddr[23:0]

Indicates the beginning quad long word address for the operation in memory. Up to 96 megabytes of memory is supported in each aperture by this address (or 4M 16-byte or 24-byte regions).

For Chunk Buffer DRAM accesses, only even number addresses are valid.

MPMemSelect[2:0]

Selects the memory aperture. The aperture is chosen according to the following table.

Table 32 - MPMEMSelect Function

MPMemSelect[2:0]	Aperture Selected
000	Connection Context SRAM
001	Chunk Buffer DRAM
010	Resequencing DRAM
011	Statistics Counters
100	EQM-12 Memory
101	TFRAG Any Phy Channel RAM
110	RFRAG Memory
111	Unused

MPBurstLength[1:0]

Indicates how many long words of data will be written to or read from memory in one burst access. Data read from the memory goes to the Memory Read Data N registers. After a burst of 1 word only the Memory Read Data 1 register is updated, A burst of two words will update this register and Memory Read Data 2, and so on for bursts of 3 and 4 words. Similarly for write bursts when data from the Memory Write Data registers is written to the memory.

Table 33 - MPBurstLength Function

MPBurstLength[1:0]	Long Words Selected
00	1
01	2
10	3
11	4

For accesses to the Chunk Buffer DRAM, only the values 01 and 11 are valid. For accesses to the TFRAG Any Phy Channel RAM and the RFRAG RAM only the value of 00 is valid. For EQM write accesses, only the value of 11 is valid.

MPCommand[1:0]

Selects the type of access.

Table 34 - MPCommand functions

MPCommand[1:0]	Command Selected
00	Reserved
01	Write
10	Read
11	Unused

MPBusy

When a command is executed, this bit will automatically be set to a 1. When the command is complete, this bit will be cleared to zero. This signal is the inverse of MPISTATI found in the Interrupt Status Register.

Register 0x804-0x810: Memory Write Data N, N=0..3 (Burstable)

Bit	Type	Function	Default
Bit 31 To Bit 0	R/W	MPWrDataN[31:0]	0

Writes to these registers are not allowed while MPBusy is active high and MPCommand[1:0]=”01” (write).

MPWrDataN[31:0], N = 0..3

A 32 bit slice of the 128 bits of write data to be directed to the address and aperture as specified in the memory port control register. MPWrData0[31:0] corresponds to bits [31:0] of the write data. MPWrData1[31:0] corresponds to bits [63:32] of the write data. MPWrData2[31:0]corresponds to bits [95:64] of the write data. MPWrData0[31:0] corresponds to bits [127:96] of the write data.

Register 0x814: Memory Write Data Overflow 1 (Burstable)

Bit	Type	Function	Default
Bit 31 To Bit 16	R/W	MPWrData1[47:32]	0
Bit 15 To Bit 0	R/W	MPWrData0[47:32]	0

Writes to this register are not allowed while MPBusy is active high and MPCommand[1:0]=”01” (write).This register is only used for writes to the Chunk Buffer Memory.

MPWrData0[47:32]

The most significant 16 bits of MPWrData0.

MPWrData1[47:32]

The most significant 16 bits of MPWrData1.

Register 0x818: Memory Write Data Overflow 2 (Burstable)

Bit	Type	Function	Default
Bit 31 To Bit 16	R/W	MPWrData3[47:32]	0
Bit 15 To Bit 0	R/W	MPWrData2[47:32]	0

Writes to this register are not allowed while MPBusy is active high and MPCommand[1:0]=”01” (write).This register is only used for writes to the Chunk Buffer Memory.

MPWrData2[47:32]

The most significant 16 bits of MPWrData2.

MPWrData3[47:32]

The most significant 16 bits of MPWrData3.

Register 0x81C-0x828: Memory Read Data N, N=0..3 (Burstable)

Bit	Type	Function	Default
Bit 31 To Bit 0	R	MPRdDataN[31:0]	0

When a read command (MPCommand[1:0]=”10”) is asserted, the data in these registers will be valid after MPBusy goes low and will stay valid until the end of the next read command.

MPRdDataN[31:0], N = 0..3

The least significant 32 bits of read data from the address and aperture as specified in the memory port control register. MPRdDataN corresponds to MPLWordEn[N].

Register 0x82C: Memory Read Data Overflow 1 (Burstable)

Bit	Type	Function	Default
Bit 31 To Bit 16	R	MPRdData1[47:32]	0
Bit 15 To Bit 0	R	MPRdData0[47:32]	0

When a read command (MPCommand[1:0]=”10”) is asserted, the data in this register will be valid after MPBusy goes low and will stay valid until the end of the next read command. This register is only updated after reads from the Chunk buffer memory.

MPRdData0[47:32]

Indicates the most significant 16 bits of the first word of read data from memory.

MPRdData1[47:32]

Indicates the most significant 16 bits of the second word of read data from memory.

Register 0x830: Memory Read Data Overflow 2 (Burstable)

Bit	Type	Function	Default
Bit 31 To Bit 16	R	MPRdData3[47:32]	0
Bit 15 To Bit 0	R	MPRdData2[47:32]	0

When a read command (MPCommand[1:0]=”10”) is asserted, the data in this register will be valid after MPBusy goes low and will stay valid until the end of the next read command. This register is only updated after reads from the Chunk Buffer Memory.

MPRdData2[47:32]

Indicates the most significant 16 bits of the third word of read data from memory.

MPRdData3[47:32]

Indicates the most significant 16 bits of the fourth word of read data from memory.

Register 0x884: Unexpected SN CI (USNCI)

Bit	Type	Function	Default
Bit 31 To Bit 14		Unused	X
Bit 13 To Bit 0	R/W	CI	0

CI

The Connection Identifier (CI) of the connection that last experienced an unexpected SN.

Register 0x888: Lost SN CI (LSNCI)

Bit	Type	Function	Default
Bit 31 To Bit 14		Unused	X
Bit 13 To Bit 0	R/W	CI	0

CI

The Connection Identifier (CI) of the connection that last experienced a lost sequenced datagram.

Register 0x88C: SRAM Parity Error Address (SPERRADD)

Bit	Type	Function	Default
Bit 31 To Bit 18		Unused	X
Bit 17 To Bit 0	R/W	SPERRADD	0

SPERRADD

The last SRAM Address that was being accessed when a parity error occurred.

Register 0x890: Excessive number of Fragments CI (ENFCI)

Bit	Type	Function	Default
Bit 31 To Bit 14		Unused	X
Bit 13 To Bit 0	R/W	CI	0

CI

The Connection Identifier (CI) of the last connection on which a frame/packet was received with an excessive number of fragments. Maximum acceptable limit of fragments per packet is 82.

Register 0x900 CB_DRAMC Status and Control Register

Bit	Type	Function	Default
Bit 31 To Bit 7		UNUSED	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	DECC	0
Bit 4	R/W	ECC_OFF	0
Bit 3	R/W	FUNC_MODE	0
Bit 2	R/W	FPP_INIT	0
Bit 1	R/W	PROV_MODE	0
Bit 0	R	SDRAM_INIT	1

This register provides status information regarding the state of the CB_DRAMC. Only one of SDRAM_INIT, PROV_MODE or FUNC_MODE at any given time is allowed to be set “high” in this register. Unpredicted behavior may result otherwise. The ECC_OFF bit should be set to 1 prior to or at the same time FPP_INIT is set to 1 for hardware initialization of the FPP_FIFO. For microprocessor initialization, these bits should be set to 1 prior to the initialization process.

SDRAM _INIT:

Indicates that the initialization sequence of the Chunk Buffer SDRAMs is in progress. Since this sequence is executing immediately following power-up, this bit is set to “1” by default. This bit is automatically cleared when the SDRAM initialization procedure is completed.

PROV_MODE:

This bit is automatically set by the CB_DRAMC when it finishes executing the initialization sequence required by the SDRAMs. When set, this bit indicates that the CB_DRAMC is in “Provision” mode and only the microprocessor can perform memory transactions. This bit should be cleared by the microprocessor when all SDRAM transactions are complete. In addition, note that setting this bit while the CB_DRAMC is in “Functional Mode” (with FUNC_MODE set) will cause undetermined results.

FPP_INIT:

When set, this bit indicates that the DRAMC is in the process of initializing the Free Pool Pointer (FPP) FIFO residing in the Chunk Buffer. Two options exist for initializing the FPP FIFO: The first requires the microprocessor to set the FPP_INIT bit. This will prompt a CB_DRAMC based initialization procedure of the FIFO. The other method is to initialize the FPP FIFO by direct microprocessor accesses. In that case there is no need to set this bit.

FUNC_MODE:

When set, this bit indicates that the CB_DRAMC is in “Functional Mode”, i.e., it is ready to perform access to the Chunk Buffer on behalf of the various functional units of the chip. When the Free Pool Pointer (FPP) FIFO is initialized by the CB_DRAMC this bit will be automatically set by the CB_DRAMC at the end of the FPP FIFO initialization procedure. Otherwise this bit needs to be set by the microprocessor (when it finishes initializing the FPP FIFO).

ECC_OFF:

Setting this bit turns ECC off. ECC will not be added or corrected. When using the microprocessor interface to access the SDRAMs, this bit must be set to 1.

DECC:

The diagnostic ECC bit (DECC) configures TFRAG to logically invert the ECC for diagnostic purposes. When DECC is a logic one, ECC generated will be inverted. When DECC is a logic zero, a correct ECC will be generated.

Reserved:

The reserved bit must be set low for correct operation of the FREEDM 84A1024 device.

Register 0x904 : CB_DRAMC_COECCE Register

Bit	Type	Function	Default
Bit 31 To Bit 24		Unused	X
Bit 23 To Bit 0	R/W	COADDR[23:0]	0

Correctable ECC Error Register. This register stores the last address of the chunk or FPP which caused an ECC error that was corrected.

COADDR[23:0]:

It stores the address of the latest ECC error detected and corrected, (i.e., if two consecutive chunks read from the memory caused a correctable ECC error, only the address of the last chunk is kept).

Register 0x908 : CB_DRAMC_UNCOECCE Register

Bit	Type	Function	Default
Bit 31 To Bit 24		Unused	X
Bit 23 To Bit 0	R/W	UNCOADDR[23:0]	0

Uncorrectable ECC Error Register. This register stores the last address of the chunk or FPP which caused 2 ECC errors, one of which can not be corrected.

UNCOADDR[23:0]:

It stores the address of the latest uncorrectable ECC error, (i.e., if two consecutive chunks read from the memory caused an uncorrectable ECC error, only the address of the last chunk is kept).

Register 0x918 RS_DRAMC Status and Control Register

Bit	Type	Function	Default
Bit 31 To Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	DECC	0
Bit 4	R/W	ECC_OFF	0
Bit 3	R/W	FUNC_MODE	0
Bit 2	R/W	FPP_INIT	0
Bit 1	R/W	PROV_MODE	0
Bit 0	R	SDRAM_INIT	1

This register provides status information regarding the state of the RS_DRAMC. Only one of SDRAM_INIT, PROV_MODE or FUNC_MODE at any given time is allowed to be set "high" in this register. Unpredicted behavior may result otherwise. The ECC_OFF bit should be set to 1 prior to or at the same time FPP_INIT is set to 1 for hardware initialization of the FPP_FIFO. For microprocessor initialization, these bits should be set to 1 prior to the initialization process.

SDRAM _INIT:

Indicates that the initialization sequence of the Resequencing Buffer SDRAMs is in progress. Since this sequence is executing immediately following power-up, this bit is set to "1" by default. This bit is automatically cleared when the SDRAM initialization procedure is completed.

PROV_MODE:

This bit is automatically set by the RS_DRAMC when it finishes executing the initialization sequence required by the SDRAMs. When set, this bit indicates that the RS_DRAMC is in "Provision" mode and only the microprocessor can perform memory transactions. This bit should be cleared by the microprocessor when all SDRAM transactions are complete. In addition, note that setting this bit while the RS_DRAMC is in "Functional Mode" (with FUNC_MODE set) will cause undetermined results.

FPP_INIT:

When set, this bit indicates that the RS_DRAMC is in the process of initializing the Free Pool Pointer (FPP) FIFO used by the resequencing logic (realized in the Resequencing Buffer). Two options exist for initializing the FPP FIFO: The first requires the microprocessor to set the FPP_INIT bit. This will prompt a RS_DRAMC based initialization procedure of the FIFO. The other method is to initialize the FPP FIFO by direct microprocessor accesses. In that case there is no need to set this bit.

FUNC_MODE:

When set, this bit indicates that the RS_DRAMC is in “Functional Mode”, i.e., it is ready to perform accesses to the Resequencing Buffer. When the Free Pool Pointer (FPP) FIFO is initialized by the RS_DRAMC this bit will be automatically set by the RS_DRAMC at the end of the FPP FIFO initialization procedure. Otherwise this bit needs to be set by the microprocessor (when it finishes initializing the FPP FIFO).

ECC_OFF:

Setting this bit turns ECC off. ECC will not be added or corrected. When using the microprocessor interface to access the SDRAMs, this bit must be set to 1.

DECC:

The diagnostic ECC bit (DECC) configures DRAMC to logically invert the ECC for diagnostic purposes. When DECC is a logic one, ECC generated will be inverted. When DECC is a logic zero, a correct ECC will be generated.

Reserved:

The reserved bit must be set low for correct operation of the FREEDM 84A1024 device.

Register 0x91C : RS_DRAMC_COECCE Register

Bit	Type	Function	Default
Bit 31 To Bit 24		Unused	X
Bit 23 To Bit 0	R/W	COADDR[23:0]	0

Correctable ECC Error Register. This register stores the last address which caused an ECC error that was corrected.

COADDR[23:0]:

It stores the address of the latest ECC error detected and corrected, (i.e., if two consecutive memory transactions caused a correctable ECC error, only the last address is kept).

Register 0x920 : RS_DRAMC_UNCOECCE Register

Bit	Type	Function	Default
Bit 31 To Bit 24		Unused	X
Bit 23 To Bit 0	R/W	UNCOADDR[23:0]	0

Uncorrectable ECC Error Register. This register stores the last address which caused 2 ECC errors, one of which can not be corrected.

UNCOADDR[23:0]:

It stores the address of the latest uncorrectable ECC error, (i.e., if two consecutive memory transactions caused an uncorrectable ECC error, only the last address is kept).

Register 0x9A0 : BIST Controller

This control register is common to all BIST sequencers in the FREEDM 84A1024.

Bit	Type	Function	Default
Bit 31 To Bit 12		Unused	X
Bit 11	R/W	BISTPATTERN[7]	0
Bit 10	R/W	BISTPATTERN[6]	0
Bit 9	R/W	BISTPATTERN[5]	0
Bit 8	R/W	BISTPATTERN[4]	0
Bit 7	R/W	BISTPATTERN[3]	0
Bit 6	R/W	BISTPATTERN[2]	0
Bit 5	R/W	BISTPATTERN[1]	0
Bit 4	R/W	BISTPATTERN[0]	0
Bit 3	R/W	BISTMODE[2]	1
Bit 2	R/W	BISTMODE[1]	0
Bit 1	R/W	BISTMODE[0]	0
Bit 0	R/W	BISTSIDE	0

The BIST Enable register must be set up prior to setup of this register.

BISTSIDE:

The BIST sequencer input BISTSIDE determines which port of dual-port RAMs is tested when the BIST logic is operating.

BISTMODE[2:0]:

The BIST sequencer input BISTMODE should be set to “010” to run BIST. Other values are reserved for use during PMC production test.

BIST_PATTERN[7:0]:

The BIST test data pattern which is applied to the RAMs during BIST.

Register 0x9A4 : BIST Enable

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R/W	TAPI-12_EN	0
Bit 14	R/W	RAPI-12_EN	0
Bit 13	R/W	FRMBLD_EN	0
Bit 12	R/W	EQM-12_EN	0
Bit 11	R/W	IQM-12_EN	0
Bit 10	R/W	CB_DRAMC_EN	0
Bit 9	R/W	RS_DRAMC_EN	0
Bit 8	R/W	TFRAG_EN	0
Bit 7	R/W	RFRAG_EN	0
Bit 6	R/W	PM-12_EN	0
Bit 5	R/W	THDL-12_EN	0
Bit 4	R/W	RHDL-12_EN	0
Bit 3	R/W	TCAS-12_EN	0
Bit 2	R/W	RCAS-12_EN	0
Bit 1	R/W	INSBI_EN	0
Bit 0	R/W	EXSBI_EN	0

Each control bit in this register enables the BIST test of all memories controlled by the selected BIST sequencer. All memories in a selected block will be tested at the same time. It should be noted that for BIST to work, all clocks must be the same frequency (SYSCLK, RXCLK, TXCLK) and the maximum frequency of operation is 40MHz. Of the BIST sequencers above, TAPI-12 and RAPI-12 are run off TXCLK and RXCLK respectively. All other BIST sequencers are run off SYSCLK. This feature is intended for production testing as opposed to on board testing. If this feature is desired for on board testing, the simplest solution is to set TAPI-12_EN and RAPI-12_EN to 0 (ie don't BIST test these memories) and set SYSCLK=52MHz.

Register 0x9A8 : BIST Result

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R	TAPI-12_RE	X
Bit 14	R	RAPI-12_RE	X
Bit 13	R	FRMBLD_RE	0
Bit 12	R	EQM-12_RE	0
Bit 11	R	IQM-12_RE	0
Bit 10	R	CB_DRAMC_RE	0
Bit 9	R	RS_DRAMC_RE	0
Bit 8	R	TFRAG_RE	0
Bit 7	R	RFRAG_RE	0
Bit 6	R	PM-12_RE	0
Bit 5	R	THDL-12_RE	0
Bit 4	R	RHDL-12_RE	0
Bit 3	R	TCAS-12_RE	0
Bit 2	R	RCAS-12_RE	0
Bit 1	R	INSBI_RE	0
Bit 0	R	EXSBI_RE	0

Each control bit in this register informs the result of the BIST test of all memories controlled by the selected BIST sequencer. An active high bit means that at least one of the tested memories in the specified block has an error. The reported result is only valid for BIST sequencers that are enabled in the BIST Enable register, when the corresponding “End” bits in register 0x9AC become set.

Register 0x9AC : BIST End

Bit	Type	Function	Default
Bit 31 To Bit 16		Unused	X
Bit 15	R	TAPI-12_ED	0
Bit 14	R	RAPI-12_ED	0
Bit 13	R	FRMBLD_ED	0
Bit 12	R	EQM-12_ED	0
Bit 11	R	IQM-12_ED	0
Bit 10	R	CB_DRAMC_ED	0
Bit 9	R	RS_DRAMC_ED	0
Bit 8	R	TFRAG_ED	0
Bit 7	R	RFRAG_ED	0
Bit 6	R	PM-12_ED	0
Bit 5	R	THDL-12_ED	0
Bit 4	R	RHDL-12_ED	0
Bit 3	R	TCAS-12_ED	0
Bit 2	R	RCAS-12_ED	0
Bit 1	R	INSBI_ED	0
Bit 0	R	EXSBI_ED	0

Each control bit in this register informs the end of the BIST test of all memories controlled by the selected BIST sequencer.

Register 0x9B0: EXSBI BIST ERROR

Bit	Type	Function	Default
Bit 31 To Bit 8	X	Unused	X
Bit 7 To Bit 0	R	ERRORN[7:0]	0

Each of these bits reports a possible error in one of the internal RAMs in EXSBI TSB.

Register 0x9B4: INSBI BIST ERROR

Bit	Type	Function	Default
Bit 31 To Bit 10	X	Unused	X
Bit 9 To Bit 0	R	ERRORN[9:0]	0

Each of these bits reports a possible error in one of the internal RAMs in the INSBI TSB.

Register 0x9B8: RCAS-12 BIST ERROR

Bit	Type	Function	Default
Bit 31 To Bit 3	X	Unused	X
Bit 2 To Bit 0	R	ERRORN[2:0]	0

Each of these bits reports a possible error in one of the internal RAMs in the RCAS-12 TSB.

Register 0x9BC: TCAS-12 BIST ERROR

Bit	Type	Function	Default
Bit 31 To Bit 4	X	Unused	X
Bit 3 To Bit 0	R	ERRORN[3:0]	0

Each of these bits reports a possible error in one of the internal RAMs in the TCAS-12 TSB.

Register 0x9C0: RHDL-12 BIST ERROR

Bit	Type	Function	Default
Bit 31 To Bit 21	X	Unused	X
Bit 20 To Bit 0	R	ERRORN[20:0]	0

Each of these bits reports a possible error in one of the internal RAMs in the RHDL-12 TSB.

Register 0x9C4: THDL-12 BIST ERROR

Bit	Type	Function	Default
Bit 31 To Bit 22	X	Unused	X
Bit 21 To Bit 0	R	ERRORN[21:0]	0

Each of these bits reports a possible error in one of the internal RAMs in the THDL-12 TSB.

Register 0x9C8: PM-12 BIST ERROR

Bit	Type	Function	Default
Bit 31 To Bit 6	X	Unused	X
Bit 5 To Bit 0	R	ERRORN[5:0]	0

Each of these bits reports a possible error in one of the internal RAMs in the PM-12 TSB.

Register 0x9CC: RFRAG BIST ERROR

Bit	Type	Function	Default
Bit 31 To Bit 3	X	Unused	X
Bit 2 To Bit 0	R	ERRORN[2:0]	0

Each of these bits reports a possible error in one of the internal RAMs in the RFRAG TSB.

Register 0x9D0: TFRAG BIST ERROR

Bit	Type	Function	Default
Bit 31 To Bit 4	X	Unused	X
Bit 3 To Bit 0	R	ERRORN[3:0]	0

Each of these bits reports a possible error in one of the internal RAMs in the TFRAG TSB.

Register 0x9D4: RS_DRAMC BIST ERROR

Bit	Type	Function	Default
Bit 31 To Bit 1	X	Unused	X
Bit 0	R	ERRORN[0]	0

Each of these bits reports a possible error in one of the internal RAMs in the RS_DRAMC TSB.

Register 0x9D8: CB_DRAMC BIST ERROR

Bit	Type	Function	Default
Bit 31 To Bit 2	X	Unused	X
Bit 1 To Bit 0	R	ERRORN[1:0]	0

Each of these bits reports a possible error in one of the internal RAMs in the CB_DRAMC TSB.

Register 0x9DC: IQM-12 BIST ERROR

Bit	Type	Function	Default
Bit 31 To Bit 5	X	Unused	X
Bit 4 To Bit 0	R	ERRORN[4:0]	0

Each of these bits reports a possible error in one of the internal RAMs in the IQM-12 TSB.

Register 0x9E0: EQM-12 BIST ERROR

Bit	Type	Function	Default
Bit 31 To Bit 6	X	Unused	X
Bit 5 To Bit 0	R	ERRORN[5:0]	0

Each of these bits reports a possible error in one of the internal RAMs in the EQM-12 TSB.

Register 0x9E4: FRMBLD BIST ERROR

Bit	Type	Function	Default
Bit 31 To Bit 3	X	Unused	X
Bit 2 To Bit 0	R	ERRORN[2:0]	0

Each of these bits reports a possible error in one of the internal RAMs in the FRMBLD TSB.

Register 0x9E8: RAPI-12 BIST ERROR

Bit	Type	Function	Default
Bit 31 To Bit 2	X	Unused	X
Bit 1 To Bit 0	R	ERRORN[1:0]	X

Each of these bits reports a possible error in one of the internal RAMs in the RAPI-12 TSB.

Register 0x9EC: TAPI-12 BIST ERROR

Bit	Type	Function	Default
Bit 31 To Bit 3	X	Unused	X
Bit 2 To Bit 0	R	ERRORN[2:0]	X

Each of these bits reports a possible error in one of the internal RAMs in the TAPI-12 TSB.

11.2. Microprocessor accessible Memories

Certain regions of the internal and external memories are used to configure and monitor the operation of the FREEDM 84A1024.

Unlike the Normal Mode registers, these entries are not cleared upon read unless specified. Specified setups are required for correct operation of the chip. The default value for these memory bits is X unless specified.

11.2.1. PM-12 Memory Map

This internal memory is used for storing statistics counters. This memory is accessed through the Memory Port Control register and is burst accessible. This memory is initialized to 0 on reset although on start up, small erred packets may pass through the chip causing the counts to be non-zero. The contents of the memory must be read every 2 seconds in order to ensure counters do not overflow. Counters will be reset to 0 once read. If the counter is allowed to overflow, it will not rollover but will hold the maximum count value until read.

note1: Byte count includes 2-bytes per event for the CI prepend. Byte count (not including CI prepend) can be determined using corresponding event count.

note2: Byte count includes 2-bytes per frame/packet for the error CI prepend.

Table 35 - PM-12 Memory Map

Address	Record	Bits	Description
0000	Unused	31:26	X
RX_HDLC_CH (1K) 03FF	RX_BYTE_CNT	25:0	Rx byte count per HDLC channel
0400	Unused	31:26	X

Address	Record	Bits	Description
RX_HDLC_CH (1K) 07FF	RX_PKT_CNT	25:0	Rx packet count per HDLC channel
0800 RX_HDLC_CH (1K) 0BFF	Unused	31:26	X
	RX_FRM_ABRT	25:0	Rx framing aborts per HDLC channel
0C00 RX_HDLC_CH (1K) 0FFF	Unused	31:26	X
	RX_FCS_ERR_CNT	25:17	FCS error count per HDLC channel
	RX_PKTL_GMAX	16:8	Rx packet length greater than maximum allowed
	RX_NON_OA_FRM	7:0	Non-octet aligned frames per Rx HDLC channel
1000 RX_HDLC_CH (1K) 13FF	Unused	31:26	X
	RX_SDD_BYTE_CNT	25:0	Rx small datagrams discarded byte count per HDLC channel
1400 RX_HDLC_CH (1K) 17FF	Unused	31:26	X
	RX_CBE_BYTE_CNT	25:0	Rx Chunk Buffer allocation exceeded byte count per HDLC channel
1800 RX_HDLC_CH (1K) 1BFF	Unused	31:26	X
	RX_SDD_EV	25:0	Rx small datagrams discarded events per HDLC channel
1C00	Unused	31:26	X

Address	Record	Bits	Description
RX_HDLC_CH (1K) 1FFF	RX_CBE_EV	25:0	Rx Chunk Buffer allocation exceeded events per HDLC channel
2000 TX_HDLC_CH (1K) 23FF	Unused	31:26	X
	TX_BYTE_CNT	25:0	Tx byte count per HDLC channel
2400 TX_HDLC_CH (1K) 27FF	Unused	31:26	X
	TX_PKT_CNT	25:0	Tx packet count per HDLC channel
2800 TX_HDLC_CH (1K) 2BFF	Unused	31:26	X
	TX_FRM_ABRT	25:0	Tx framing aborts per HDLC channel
2C00	RX_FIFO_OF	31:0	Rx FIFO overflow
2C01	RX_UNEXP_SQNUM	31:0	Rx unexpected sequence number events
2C02	RX_FCS_BYTE_CNT	31:0	Rx byte count of datagrams with FCS errors *note1
2C03	RX_NOA_BYTE_CNT	31:0	Rx byte count of non-octet aligned datagrams *note1
2C04	Reserved	31:0	X
2C05	RX_GMX_BYTE_CNT	31:0	Rx byte count of datagrams with packet length greater than maximum allowed *note1
2C06	RX_FOR_BYTE_CNT	31:0	Rx byte count of datagrams with unexpected sequence number *note1
2C07	RX_ABR_BYTE_CNT	31:0	Rx byte count of datagrams with abort errors *note1

Address	Record	Bits	Description
2C08	RX_UHF_BYTE_CNT	31:0	Rx byte count of datagrams with unsupported header format *note2
2C09	RX_LOST_EV	31:0	Rx lost SN events
2C0A	RX_PKLT_LMIN	31:0	Rx packet length less than minimum allowed
2C0B	RX_EXC_FR_NBR	31:0	Rx excessive number of fragments events
2C0C	TX_FIFO_UF	31:0	Tx FIFO underflow
2C0D-2C13	Reserved	31:0	X

11.2.2. EQM-12 Memory

This internal memory is used to setup configuration and read status per Egress HDLC Channel and Multigroup. The default value of this memory is 0. All Reserved bits must be set to the value defined for correct operation. . For write accesses, only MPBurstLenght=11 is supported.

Table 36 - EQM-12 Memory Map

Address	Record	Word:Bits	Description
000 HDLC_CH (1024) each address = 4x32bits 3FF	Unused	127:122	X
	Reserved	121	Reserved. Must be set to 0 for correct operation.
	SPC_THR[18:0]	120:102	Space threshold. Must be setup to control HDLC Channel availability indications over the ANY PHY I/F. SPC_THR multiplied by 32 represents the maximum number of bytes below which and HDLC channel will indicate that it has space to accept a new datagram. SPC_THR should be set to: OV_THR – MTU(bytes)/32
	Reserved	101	Reserved. Must be set to 0 for correct operation.
	OV_THR[18:0]	100:82	Overflow Threshold. This value must be set larger than the SPC_THR value to indicate at which point and overflow interrupt is generated.
	MLG[7:0]	81:74	Multilink Group Number.
	AP_CHAN[9:0]	73:64	ANY-PHY Channel number.
	Reserved	63	Reserved. Must be set to 1 for correct operation.
	Reserved	62	Reserved. Must be set to 0 for correct operation.
	ML	61	Must be set for HDLC channels that belong to a multilink bundle.
	V_TP	60	Valid Tail Pointer. See note 1 below.
	SZ	59:40	Size. Must be set to 0 for correct operation.
	TP	39:20	Tail Pointer. See note 1 below.
	HP	19:0	Head Pointer. See note 1 below.
400 ML_GRP(84) Even Add= 4x32bits Odd Addresses= 2x32bits+8bits	Unused	199:195	X
	Round Robin	194	Sets lowest fill queue arbitration to round robin mode. The lowest fill queue is always selected as the next HDLC channel to be serviced. When multiple queues contain the same number of bytes and Round Robin is set, priority is given to the HDLC channel in the group following the one that was just serviced. When set to 0, priority is always given to the lowest channel in the group with lowest fill.

Address	Record	Word:Bits	Description
54F	RR Start Index	193:190	Round Robin starting index. This context indicates the channel in a ML group which will have highest priority if multiple channels have lowest fill. This index can be used to dictate which channel will first be used when a bundle is started up. Alternatively, this can be set to 0 and the first fragment will be sent down the first link in the bundle.
	Reserved	189	Reserved. Must be set to 0 for correct operation.
	ML_OV_THR[18:0]	188:170	Multilink Overflow Threshold. Defined as above. This value overrides the HDLC channel threshold value.
	Reserved	169	Reserved. Must be set to 0 for correct operation.
	ML_SPC_THR[18:0]	168:150	Multilink Space Threshold. Defined as above. This value overrides the HDLC channel threshold value.
	Reserved	149	Reserved. Must be set to 0 for correct operation.
	Reserved	148	Reserved. Must be set to 1 for correct operation.
	ML_SZ	147:128	Multilink Size. Must be set to 0 .
	Unused	127:124	X
	NUM_HCH[3:0]	123:120	Number of HDLC channels in ML group.
	HDLC_CHAN[119:0]	119:0	The multilink members (max of 12 HDLC channels). The first member is HDLC_CHAN[9:0] and the last member is HDLC_CHAN[119:110].

Note 1: These bits must be set to 0 after reset. For subsequent initializations of the HDLC channel, traffic must be stopped and when SZ[59:40]=0, a read modify write must be performed on the new configuration. V-TP, TP, and HP should retain their value.

11.2.3. TFRAG ANY-PHY Channel RAM Memory Map

This internal memory must be written to setup Egress ANY PHY Channel configuration. The default value of this memory is 0. MPBurstLength[1:0] must = 00 for access to this memory.

Table 37 - TFRAG ANY-PHY Channel RAM Memory Map

Address	Record	Bits	Description
000 ANY PHY CHANNEL # (1024)	Unused	31:24	X.
	PPP_PID_COMP	23	PID Compression enabled.
	PPP_ADDR_CTRL_COMP	22	Address/Control Compression enable.
	ML_GROUP[7:0]	21:14	Multilink Group. This must be set to the Multilink bundle number. Does not apply if in Single Link Mode.
	ML_CH	13	1 indicates that this channel is Multilink.

Address	Record	Bits	Description
3FF	DATA_TYPE[2:0]	12:10	Indicates data type as follows: 000 – PPP 001 -FR 010 – Transparent Mode 011 – Unused 1XX - Unused
	HDLC_CHAN[9:0]	9:0	The HDLC Channel for Single Link Mode. Does not apply if in Multilink Mode.
400	Unused	31:2	X
	DET_EOP_LOSS	1	1 – Enable detection of EOP Loss. If the ANY-PHY channel number changes before end-of-packet is received, the next segment will be interpreted as end-of-packet.
	Reserved	0	Reserved. Must be left at default or written to 0 for correct operation.
401	Reserved	31:0	X. Read only.
402	Reserved	31:0	X. Read only.
403	Reserved	31:0	X. Read only.

11.2.4. RFRAG Memory Map

This internal memory must be written to setup Ingress HDLC Channel configuration. The default value of this memory is 0. MPBurstLength[1:0] must = 00 for access to this memory.

Table 38 - RFRAG Memory Map

Address	Record	Bits	Description
000	Reserved	31:22	Must be written to 0 for correct operation.
	SDDSCRD_OVR	21	Small datagram discard threshold override. Set this bit to 1 to override the default 40-byte small datagram discard threshold with the value programmed into the SDDSCRD_THR[5:0] register.
	SDDSCRD_THR [5:0]	20:15	Small datagram discard threshold. When the SDDSCRD_OVR control bit is set to 1, program this register to the byte size (0 to 56) under which small datagrams will be discarded when an excessive number of datagrams are waiting to be processed by the resequencing engine.

Address	Record	Bits	Description
HDLC CHANNEL # (1024) 3FF	PTCL_PPP [1:0]	14:13	Protocol definition. 00 – PPP 01 – Frame Relay 10 – HDLC 11 – Unused
	ACF_CPRS	12	Address-and-Control field compression. Set this bit to 1 to allow the reception of Address-and-Control field compressed PPP headers. Uncompressed headers may also be received when this bit is set, but must carry the standard 0xFF and 0x03 values. This control bit is only used in PPP mode.
	PF_CPRS	11	Protocol field compression. Set this bit to 1 to allow the reception of Protocol field compressed PPP headers. Uncompressed headers may also be received when this bit is set. This control bit is only used in PPP mode.
	SEQFMT_12	10	Sequence number format. This control bit is only used in PPP mode. 0 – 12 bits 1 – 24 bits
	AP_CHAN [9:0]	9:0	ANY-PHY channel number. Program this register to the ANY-PHY channel number associated with this HDLC Channel. Prior to tearing down an ANY-PHY channel, all CI's associated with that ANY_PHY channel must first be torn down following the specified tear down procedure.
400 ANY-PHY CHANNEL	Reserved	31:23	Must be written to 0 for correct operation.
	AP_ALLOC_THR	22:4	ANY-PHY storage allocation threshold. Program this register to the allowed number of chunks of storage above which datagrams received for this ANY-PHY channel will be discarded. Note that this threshold will be verified only at the start of every datagram (i.e., no datagram will be discarded if its first chunk was accepted, even though subsequent chunks may cause the ANY-PHY storage allocation threshold to be exceeded). Care must therefore be taken when defining ANY-PHY storage allocation thresholds to reserve (subtract) enough headroom for storage of one additional datagram.
	OUTFMT_FRPK	3	Output format (frame/packet or fragment). 0 – Frame/Packet 1 – Fragment

Address	Record	Bits	Description
# (1024) 7FF	AP_CIOUT	2	ANY-PHY connection identifier output. Set this bit to 1 to indicate that the connection identifier is to be pre-pended to all datagram transfers across a downstream ANY-PHY interface. This bit will be overridden and forced to 1 when an erred datagram is received. This bit should never be cleared when sequenced datagrams are expected as this will cause an unexpected presence of sequence number error.
	AP_SEGSIZE[1:0]	1:0	Ingress ANY-PHY channel output segment size (64, 128, or 256 bytes). Each channel must be programmed with the same value. 00 – 64 bytes 01 – 128 bytes 10 – 256 bytes 11 – Unused
800 BFF		31:0	Reserved. Must be left at default or written to 0 for correct operation.
C00 FFF	AP_NCHNKS[18:0]	31:19 18:0	Unused Number of chunks stored in external chunk buffer

11.2.5. Re-Sequence Structures (RS) Memory Map

This external memory can be read or written with any value for test purposes before Functional Mode (FUNC_MODE) in RS_DRAMC Status and Control Register is enabled. The contents of the memory must be left in the state described below for correct operation.

ECC Protection can be enabled in RS_DRAMC Status and Control Register. If ECC is enabled, bits 31-24 are overwritten with the ECC value. If ECC is disabled, bits 31-24 are written with the data presented.

Table 39 - RS Memory Map

Address	Record	Bits	Description
000000 (HDLC# x 4096 = 4M) 3FFFFF	CI_LOOKUP	31:0	**Connection Identifier Lookup record**. This record must be populated according to the record description below. All unused locations must be set to a default connection identifier. Whenever a connection is de-commissioned , the location must be written with a default connection identifier. A Unique CI must be used for each ANY-PHY channel. All CI's in an ANY-PHY channel must be torn down before an ANY-PHY channel is torn down. The connection Identifier lookup address is generated as follows: Bits 23:22 – 0 Bits 21:12 – HDLC CH number Bits 11:10 – 00 – Sequenced or Transparent Mode 01 – Non-sequenced 10 – Control (ML_FR, ML_PPP, SL_PPP) 11 – Corrupt Bits 9:0 – 0 for Corrupt, Control or Transparent Mode DLCI or COS otherwise (although COS=0 if non-sequenced). Sequenced CI lookup record consists of 1024 entries per HDLC channel. In frame relay 1024 unique DLCI numbers can be mapped to 1-to-1024 CI numbers. In PPP 16 COS numbers can be mapped to 1-to-16 CI numbers. For each sequenced connection in an HDLC bundle, the same CI must be set up for each HDLC#. See Table 40 for details. This format is also used for transparent mode operation but the only valid instances for bits 11:10 are 00 or 11 and address bits 9:0 must be set to 0. Non-sequenced CI lookup record consists of 1024 entries per HDLC channel. In frame relay 1024 unique DLCI numbers can be mapped to 1-to-1024 CI numbers. In PPP each HDLC channel is mapped to 1 CI number. See Table 41 for details. Control CI lookup record consists of 1 entry per HDLC channel. In Multilink frame relay an active control bit in the frame header results in an index to the CI present in this record In Single or Multilink PPP an active NCP or LCP bit in the packet header results in an index to the CI present in this record. For Single Link FR, control packets are identified by DLCI and these packets must be identified by putting a unique CI in the non-sequenced table based on DLCI. See Table 42 for details. Corrupt CI lookup record consists of 1 entry per HDLC channel. A datagram marked as corrupted will result in an index to the corrupt CI lookup record. See Table 43 for details.

Address	Record	Bits	Description
400000 (256k) 43FFFF	Reserved	31:0	**LSB Record Status.** Upon initialization, S/W must write this field to 0 for correct operation of the chip. **Note –** ECC must be disabled when these locations are read from and written to by the microprocessor.
440000 (3.75M) 7FFFFF	Unused	31:0	X
800000 (2M) 9FFFFF	Reserved	31:0	**MSB Record.** Upon initialization, S/W must write this field to 0 for correct operation of the chip.
A00000 (512k entries x 2 locations per entry) AFFFFF	Reserved	31:0	Used by Hardware.
B00000 (32k) B07FBF	LSB_RCD _FREELIST	31:0	**LSB Record Freelist record**. Each entry points to the location an unoccupied LSB record with each LSB record comprising 128 address locations. When the RS_DRAMC status register bit FPP_INIT is set, internal logic writes a unique 15-bit pointer value to each of the 32k freelist locations (pointer values ranging from 40h to 7FFFh). If the RS_DRAMC status register bit FPP_INIT is not set, and has not been set since initialization of the device, then the microprocessor must populate the LSB record freelist as the internal logic will not have been invoked to do so. See Table 46 for details.
B07FC0 (.96875M) BFFFFF	Unused	31:0	X
C00000 (4M) FFFFFF	Reserved	31:0	Used by hardware.

Table 40 - Sequenced Connection Identifier Lookup Record

Relative Address	Record	bits	Description
000000 (1k) index via DLCI or COS number 0003FF	Reserved	31:24	These bits are ignored and overwritten with an ECC value via logic within the device.
	Unused	23:14	X
	CI_NUMBER	13:0	CI number ranging from 0d to 16,383d.

Table 41 - Non-sequenced Connection Identification Lookup Record

Relative Address	Record	bits	Description
000400 (1k) index via DLCI or COS number 0007FF	Reserved	31:24	These bits are ignored and overwritten with an ECC value via logic within the device.
	Unused	23:14	X
	CI_NUMBER	13:0	CI number ranging from 0d to 16,383d.

Table 42 - Control Connection Identifier lookup record

Relative Address	Record	bits	Description
000800 (1)	Reserved	31:24	These bits are ignored and overwritten with an ECC value via logic within the device.
	Unused	23:14	X
	CI_NUMBER	13:0	CI number ranging from 0d to 16,383d.

Table 43 - Corrupt Connection Identifier Lookup record

Relative Address	Record	Bits	Description
000C00 (1)	Reserved	31:24	These bits are ignored and overwritten with an ECC value via logic within the device.
	Unused	23:14	X
	CI_NUMBER	13:0	CI number ranging from 0d to 16,383d.

Table 44 -LSB Records Status record

Address	Record	Bits	Description
400000h	END_BIT/ OCP_BIT	31:2	A repetition of bits 0 and 1 pairs for fifteen other LSB record locations.

(256k) 43FFFFh	END_BIT	1	End bit. Valid only when the OCP_BIT is set. Holds the value of the End bit associated with the datagram information stored in the corresponding LSB record location.
	OCP_BIT	0	Occupied bit. Set to one when corresponding LSB record location is occupied with a valid datagram pointer and related information.

Table 45 -MSB Records record

Address	Record	Bits	Description
800000h	Reserved	31:24	ECC value
	Unused	23:16	X
(2M)	VAL_PTR	15	Pointer validation bit
9FFFFFh	LSB_PTR	14:0	15-bit pointer to one of the 32k LSB records

Table 46 - LSB Record Freelist record

Address	Record	Bits	Description
B00000	Reserved	31:24	These bits are ignored and overwritten with an ECC value via logic within the device.
	Unused	23:15	X
(32k-40h) B07FBF	LSB_RCD_PTR	14:0	15-bit LSB record pointer to one of the 32k LSB records. Prior to device operation each location is to be populated with a unique number ranging from 40h to 7FFFh.

11.2.6. Chunk Buffer Memory Map

This external memory can be read or written with any value for test purposes before Functional Mode (FUNC_MODE) is enabled in the CB_DRAMC Status and Control register. The contents of the memory must be left in the state described below for correct operation. Certain fields can be setup by H/W (also described below) if selected.

Table 47 - Chunk Buffer Memory Map (only even addresses are valid)

Address	Record	Bits	Description
000000 (4M) 3FFFFF	Reserved	95:0	X
400000 (256K) 43FFFF	IN_FPP _STORE	95:0	Ingress Free List Pointers. Each entry contains 2 x 48 bit words making up a 96 bit word. For S/W setup of the Free List Pointers, the record must be filled with the following data: 00400-7FFFF. I.e.. Address = 400000 Data = 000_2,0400_{16} ,000_2,0401_{16},00_2,8 bit ECC 000_2,0402_{16} ,000_2,0403_{16},00_2,8 bit ECC **Address = 400002 Data = 000_2,0404_{16} ,000_2,0405_{16},00_2,8 bit ECC 000_2,0406_{16} ,000_2,0407_{16},00_2,8 bit ECC **Address = 400004 Data = 000_2,0408_{16} ,000_2,0409_{16},00_2,8 bit ECC 000_2,$040A_{16}$,000_2,$040B_{16}$,00_2,8 bit ECC **Address = 400006 Data = 000_2,$040C_{16}$,000_2,$040D_{16}$,00_2,8 bit ECC 000_2,$040E_{16}$,000_2,$040F_{16}$,00_2,8 bit ECC . . . **Address = 43FDFC Data = 111_2,$FFF8_{16}$,111_2,$FFF9_{16}$,00_2,8 bit ECC 111_2,$FFFA_{16}$,111_2,$FFFB_{16}$,00_2,8 bit ECC **Address = 43FDFC Data = 111_2,$FFFC_{16}$,111_2,$FFFD_{16}$,00_2,8 bit ECC 111_2,$FFFE_{16}$,111_2,$FFFF_{16}$,00_2,8 bit ECC **Address = 43FE00-43FFFF Data = Leave at default value. This record can also be set up by h/w by setting the FPP_INIT bit in the CB_DRAM Status Register.
440000 7FFFFF	Unused	95:0	X

Address	Record	Bits	Description
800000 (4M) BFFFFF	Reserved	95:0	X
C00000 (256K) C3FFFF	EG_FPP _STORE	95:0	Egress Free List Pointers. Each entry contains 2 x 48 bit words making up a 96 bit word. For S/W setup of the Free List Pointers, the record must be filled with the following data: 00400-7FFFF. I.e. Address = C00000 Data = 000_2,0400_{16} ,000_2,0401_{16},00_2,8 bit ECC 000_2,0402_{16} ,000_2,0403_{16},00_2,8 bit ECC **Address = C00002 Data = 000_2,0404_{16} ,000_2,0405_{16},00_2,8 bit ECC 000_2,0406_{16} ,000_2,0407_{16},00_2,8 bit ECC Address = C00004 Data = 000_2,0408_{16} ,000_2,0409_{16},00_2,8 bit ECC 000_2,$040A_{16}$,000_2,$040B_{16}$,00_2,8 bit ECC **Address = C00006 Data = 000_2,$040C_{16}$,000_2,$040D_{16}$,00_2,8 bit ECC 000_2,$040E_{16}$,000_2,$040F_{16}$,00_2,8 bit ECC . . . Address = C3FDFC Data = 111_2,$FFF8_{16}$,111_2,$FFF9_{16}$,00_2,8 bit ECC 111_2,$FFFA_{16}$,111_2,$FFFB_{16}$,00_2,8 bit ECC *****Address = C3FDFC Data = 111_2,$FFFC_{16}$,111_2,$FFFD_{16}$,00_2,8 bit ECC 111_2,$FFFE_{16}$,111_2,$FFFF_{16}$,00_2,8 bit ECC Address = C3FE00-C3FFFF Data = Leave at default value. This record can also be set up by h/w by setting the FPP_INIT bit in the CB_DRAM Status Register.
C40000 FFFFFF	Unused	95:0	X

11.2.7. Connection Context (CC) Memory Map

This memory holds connection configuration for both Ingress (RX) and Egress (Tx). This external memory can be read or written with any value for test purposes before Traffic is enabled. The contents of the memory must be left in the state described below for correct operation. A connection's data may be read but not written to once traffic is present on the connection. Each connection contains 16 32-bit records (W15-W0). When writing to word 0 to set up a Rx connection, words 1-3 must also be written to the value 0. Addressing per CI is described as follows:

Table 48 - Connection Context Memory Addressing

Address	CI #	Word
00000	0000	W0
00001	0000	W1
…	…	…
0000F	0000	W15
00010	0001	W0
00011	0001	W1
…	…	…
0001F	0001	W15
3FFF0	3FFF	W0
3FFF1	3FFF	W1
…	…	…
3FFFF	3FFF	W15

Table 49 - CC Memory Map

Address	Record	Word:bits	Description
00000	Tx Unused	W15:31:10	X
	TX_HDR_SZ[1:0]	W15:9:8	Transmit Fragmentation Header 00 - Short sequence 01 - Short sequence with class(PPP) 10 - Long sequence (PPP) 11 - Long sequence with class (PPP)
	TX_FRAG_MODE[1:0]	W15:7:6	Tx Fragmentation Mode 00 – Add Fragment Header 01 – Add Sequence Number only 10 – Non sequenced 11 - Unused
	TX_FRAG_SIZE[1:0]	W15:5:4	Fragmentation size 00 – 128 01 – 256 10 – 512 11 – packet
Cin*16words (16x16K)	TX_SUB_CH_NUM[3:0]	W15:3:0	Tx Sub-channel number. Defines the offset/index of a member channel within a multilink group that is to be selected.
	TX_SEQ_NUM[23:0]	W14:31:8	Transmit Sequence Number.
	Unused	W14:7	X
	TX_ML_OVRD	W14:6	Transmit Multilink override 0 – No override 1 – Multilink override. The sub channel number is used to select from the multilink bundle.
	TX_COS[3:0]	W14:5:2	Tx Class of Service. Used only for PPP/ML_PPP.
	TX Reserved	W14:1:0	These bits must be set to 0 for correct operation.
Cin*16words (16x16K =256K)	Unused	W13:31:0	X
	Unused	W12:31:0	X
	Unused	W11:31:0	X
	Unused	W10:31:0	X
	Unused	W9:31:0	X
	Unused	W8:31:0	X
	Unused	W7:31:0	X
	Rx Reserved	W6:31:0	These bits must be set to 0 for correct operation.
	Rx Reserved	W5:31:0	These bits must be set to 0 for correct operation.

3FFFF	HEAD	W5:31:18	These bits must be initialised to 0 for correct operation. This field is used in conjunction with HOLE and TAIL_VALID to determine if resequencing is still in progress.
	HOLE	W5:17:4	These bits must be initialised to 0 for correct operation. This field is used in conjunction with HEAD and TAIL_VALID to determine if resequencing is still in progress.
	Rx Reserved	W5:3:0	These bits must be set to 0 for correct operation
	Rx Reserved	W3:31:13	These bits must be set to 0 for correct operation.
	FIFO_ACT	W3:12	FIFO Active. 1 – Active 0 - Inactive
	Rx Reserved	W3:11:0	These bits must be set to 0 for correct operation.
	Rx Reserved	W2:31:0	These bits must be set to 0 for correct operation.
	Rx Reserved	W1:31:16	These bits must be set to 0 for correct operation.
	TAIL_VALID	W1:15	Used in conjunction with HEAD and HOLE fields to determine if resequencing is still in progress.
	Rx Reserved	W1:14:0	These bits must be set to 0 for correct operation.
	Rx Reserved	W0:31:5	These bits must be set to 0 for correct operation.

	LOST_CNT	W0:4:1	Lost Timeout Period. The resolution of LOSTCNT is 10ms, so the actual timeout may be up to 10 ms later than the minimum values specified in the table below. When set to zero, lost declaration is turned off and no lost events are created. LOSTCNT TIMEOUT (min) 0 disabled 1 0 ms 2 10 ms 3 20 ms … … 15 140 ms ** NOTE: The timeout period should be chosen carefully to avoid sequence number wraparound when waiting for fragments that have become lost due to transmission errors. Bundle size, fragment size, serialization time, and differential delay are some of the factors to consider.
	RX_CLASS	W0:0	Receive Class 0 – High Priority 1 – Low Priority Note: When writing W0, W1-W3 must also be written to 0.

Resequencing is in progress if either the HEAD and HOLE fields are not equal to each other or the TAIL_VALID bit is 1.

12. Test Features Description

The FREEDM 84A1024 also supports a standard IEEE 1149.1 five signal JTAG boundary scan test port for use in board testing. All device inputs may be read and all device outputs may be forced via the JTAG test port.

12.1. Test Mode Registers

Test mode registers are used to apply test vectors to the DLL during production testing of the FREEDM 84A1024. Production testing is enabled by asserting the PMCTEST pin. During production tests, FREEDM 84A1024 registers are selected by the TA[12:0] pins. Read accesses are enabled by asserting TRDB low while write accesses are enabled by asserting TWRB low. Test mode register data is conveyed on the TDAT[15:0] pins. Test mode registers (as opposed to normal mode registers) are selected when TA[12]/TRS is set high.

Table 50 - Test Mode Register Memory Map

Address TA[12:0]	Register
0x0000 - 0x0EFF	Normal Mode Registers
0x0F00 - 0x0F1F	Reserved
0x1F20 - 0x1F2C	DLL Test Registers
0x1F2D - 0x1FFF	Reserved

Notes on Test Mode Register Bits

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused register bits should be masked off by software when read.
2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

12.2. JTAG Test Port

The FREEDM 84A1024 JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 51 - Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Code IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

12.2.1. Identification Register

Length - 32 bits

Version number - 3H

Part Number - 7388H

Manufacturer's identification code - 0CDH

Device identification - 373880CDH

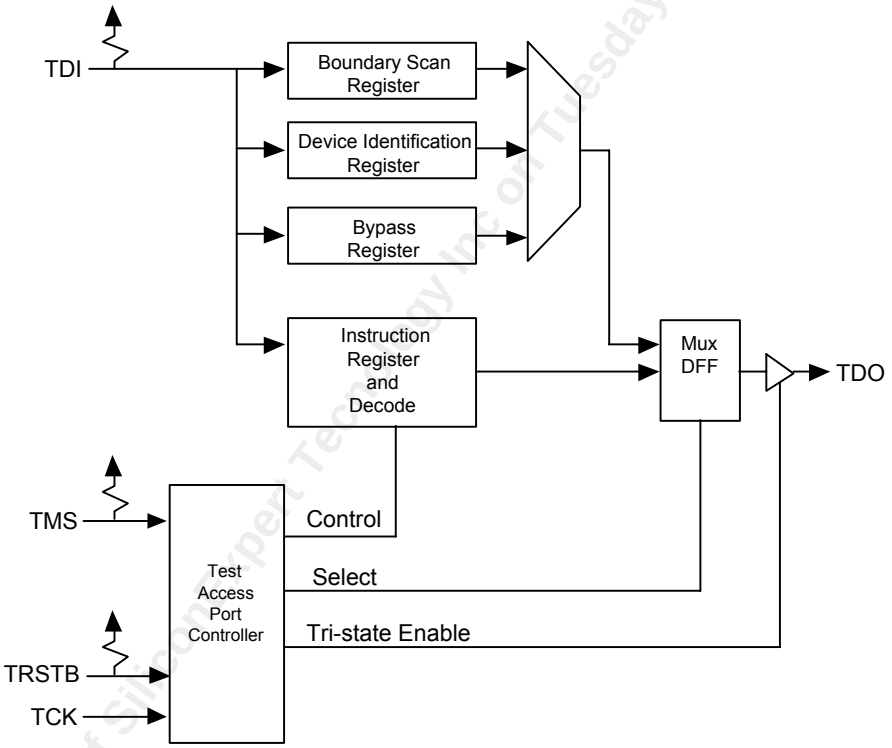
13. Operations

This section presents operating details for the JTAG boundary scan feature.

13.1. JTAG Support

The FREEDM 84A1024 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 32 - Boundary Scan Architecture



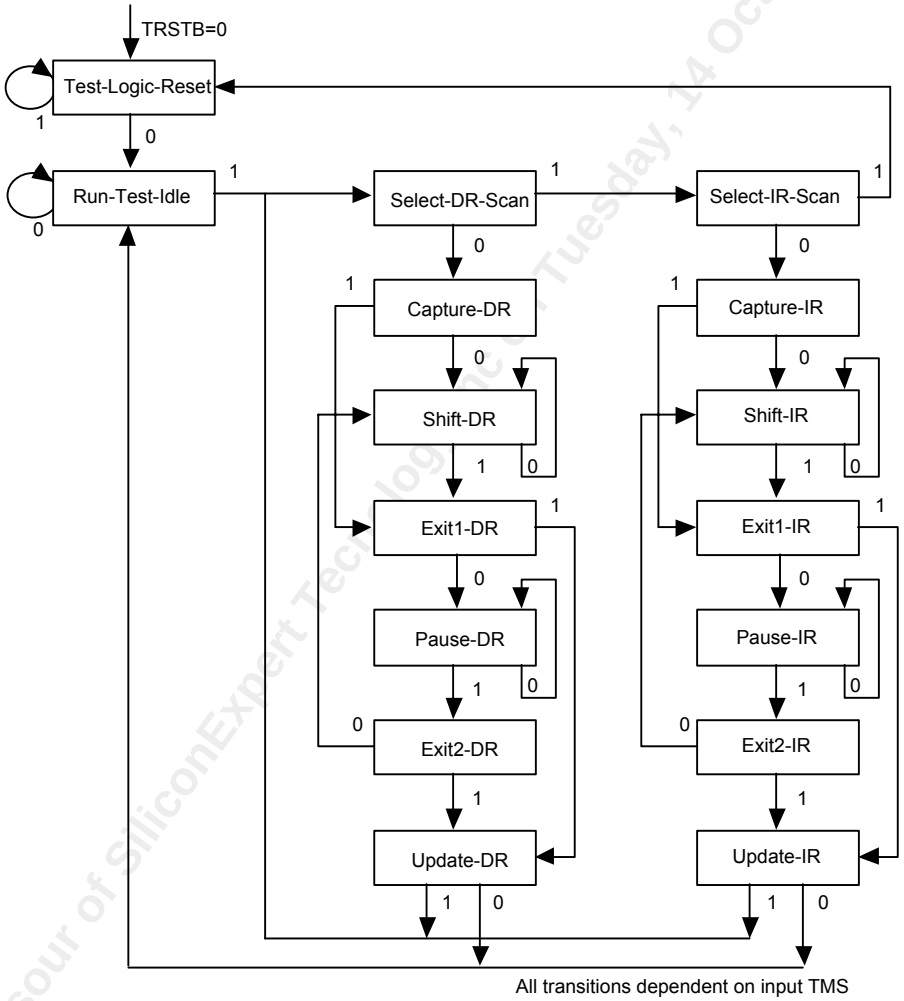
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decodes, and a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single bit delay from primary input, TDI to primary output , TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register placed in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 33 - TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

INTEST

The internal test instruction is used to exercise the device's internal core logic. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Update-DR state, patterns shifted in on input, TDI are used to drive primary inputs. During the Capture-DR state, primary outputs are sampled and loaded into the boundary scan register.

14. Functional Timing

14.1. SBI DROP BUS Interface Timing

Figure 34 - T1/E1 DROP BUS Functional Timing

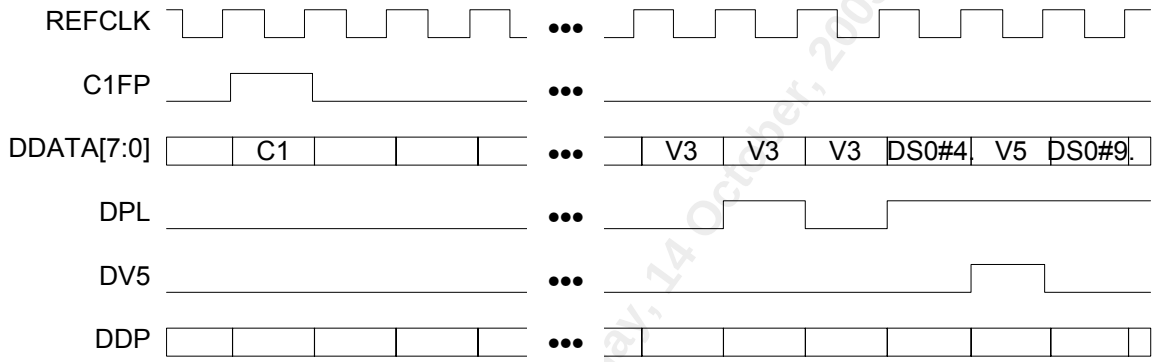


Figure 34 illustrates the operation of the SBI DROP BUS, using a negative justification on the second to last V3 octet as an example. The justification is indicated by asserting DPL high during the V3 octet. The timing diagram also shows the location of one of the tributaries by asserting DV5 high during the V5 octet.

Figure 35 - DS3 DROP BUS Functional Timing

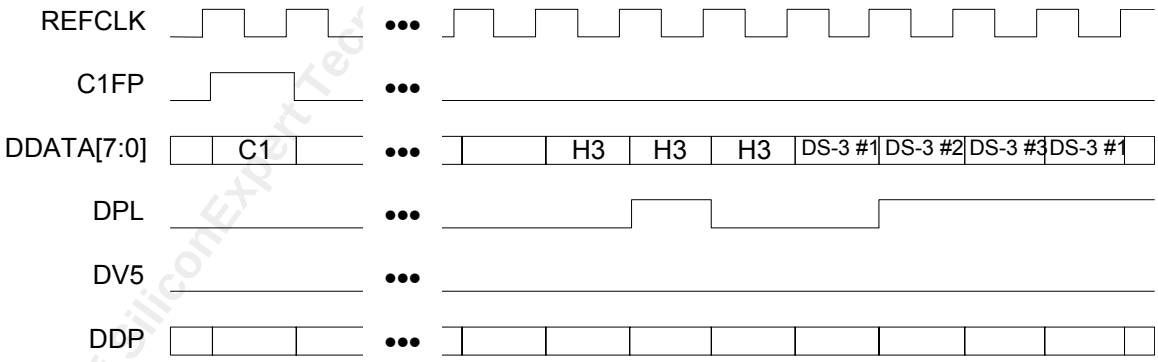


Figure 35 shows three DS-3 tributaries mapped onto the SBI bus. A negative justification is shown for DS-3 #2 during the H3 octet with DPL asserted high. A positive justification is shown for DS-3#1 during the first DS-3#1 octet after H3 which has DPL asserted low.

14.2. SBI ADD BUS Interface Timing

Figure 36 - DS3 Add Bus Adjustment Request Functional Timing

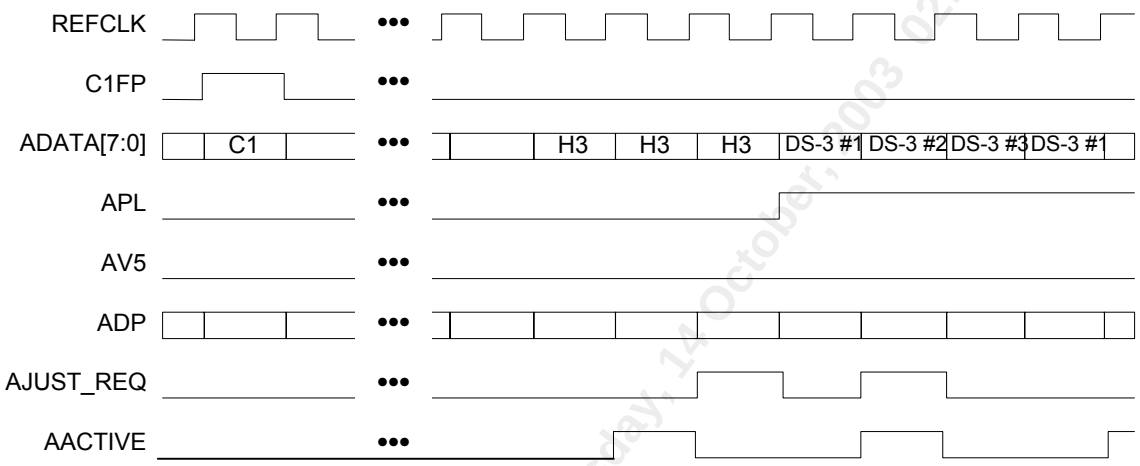
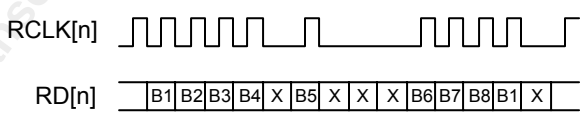


Figure 36 illustrates the operation of the SBI ADD BUS, using positive and negative justification requests as an example. (The responses to the justification requests would take effect during the next multi-frame.) The negative justification request occurs on the DS-3#3 tributary when AJUST_REQ is asserted high during the H3 octet. The positive justification occurs on the DS-3#2 tributary when AJUST_REQ is asserted high during the first DS-3#2 octet after the H3 octet. The AACTIVE signal is shown for the case in which FREEDM 84A1024 is only driving DS-3#2 onto the SBI ADD bus.

14.3. Receive Link Timing

The timing relationship of the receive clock (RCLK[n]) and data (RD[n]) signals is shown in Figure 37. The receive data is viewed as a contiguous serial stream. There is no concept of time-slots or framing. Every eight bits are grouped together into a byte with arbitrary alignment. The first bit received (B1 in Figure 37) is deemed the most significant bit of an octet. The last bit received (B8) is deemed the least significant bit. Bits that are to be processed by the FREEDM 84A1024 are clocked in on the rising edge of RCLK[n]. Bits that should be ignored (X in Figure 37) are squelched by holding RCLK[n] quiescent. In Figure 37, the quiescent period is shown to be a low level on RCLK[n]. A high level, effected by extending the high phase of the previous valid bit, is also acceptable. Selection of bits for processing is arbitrary and is not subject to any byte alignment or frame boundary considerations.

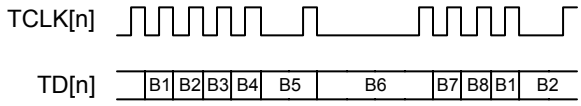
Figure 37 - Receive Link Timing



14.4. Transmit Link Timing

The timing relationship of the transmit clock (TCLK[n]) and data (TD[n]) signals is shown in Figure 38. The transmit data is viewed as a contiguous serial stream. There is no concept of time-slots or framing. Every eight bits are grouped together into a byte with arbitrary byte alignment. Octet data is transmitted from most significant bit (B1 in Figure 38) and ending with the least significant bit (B8 in Figure 38). Bits are updated on the falling edge of TCLK[n]. A transmit link may be stalled by holding the corresponding TCLK[n] quiescent. In Figure 38, bits B5 and B2 are shown to be stalled for one cycle while bit B6 is shown to be stalled for three cycles. In Figure 38, the quiescent period is shown to be a low level on TCLK[n]. A high level, effected by extending the high phase of the previous valid bit, is also acceptable. Gapping of TCLK[n] can occur arbitrarily without regard to byte nor frame boundaries.

Figure 38 - Transmit Link Timing



14.5. Receive APPI Timing (ANY-PHY Level 2)

The receive ANY-PHY packet interface (APPI) timing is shown in Figure 39 through Figure 42 when the ANY-PHY interface operates at 52 MHz, 16 bits of RXDATA are valid. The FREEDM 84A1024 device provides data to an external controller using the receive APPI. The following discussion surrounding the receive APPI functional timing assumes that multiple FREEDM 84A1024 devices share a single external controller. All Rx APPI signals are shared between the FREEDM 84A1024 devices

Figure 39 - Receive APPI Timing (Normal Transfer 16 bit 52 MHz)

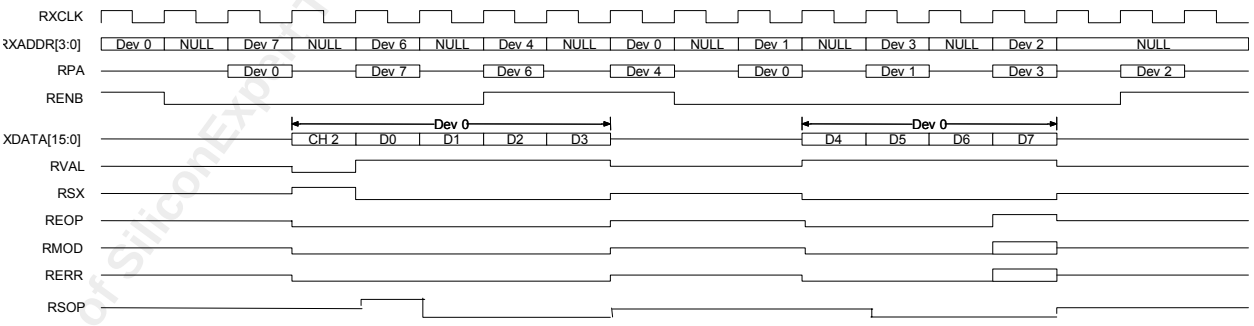


Figure 39 shows the transfer of an 8 word packet across the Rx APPI from FREEDM 84A1024 device 0, ANY-PHY channel 2. In this example, seven FREEDM 84A1024 devices are sharing the Rx APPI, with device 5 being the null address.

The data transfer begins when the external controller selects FREEDM 84A1024 device 0 by placing that address on the RXADDR[3:0] inputs and setting RENB high. The external controller sets RENB low in the next RXCLK cycle to commence data transfer across the Rx APPI. The FREEDM 84A1024 samples RENB low and responds by asserting RSX one RXCLK cycle later. The start of all burst data transfers is qualified with RSX and an in-band ANY-PHY channel address on RXDATA[15:0] to associate the data to follow with an ANY-PHY channel.

During the cycle when D2 is placed on RXDATA[15:0], the external controller is unable to accept any further data and sets RENB high. Two RXCLK cycles later, the FREEDM 84A1024 tristates the Rx APPI. The external controller may hold RENB high for an indeterminate number of RXCLK cycles. The FREEDM 84A1024 will wait until the external controller returns RENB low. Because the FREEDM 84A1024 does not support interrupted data transfers on the Rx APPI, the external controller must reselect FREEDM 84A1024 device 0 or output a null address during the clock cycle before it returns RENB low. However, while RENB remains high, the address on the RXADDR[3:0] signals may change. When the FREEDM 84A1024 device 0 samples RENB low, it continues data transfer by providing D4 on RXDATA[15:0]. Note that if D3 were the final word of the packet (Status), in response to sampling REOP high, the external controller does not have to reselect FREEDM 84A1024 device 0. This is shown in Figure 42.

The FREEDM 84A1024 will not pause burst data transfers across the Rx APPI.

The FREEDM 84A1024 automatically deselects at the end of all burst data transfers. The FREEDM 84A1024 must be reselected before any further data will be transferred across the Rx APPI.

The RVAL and REOP signals indicate the presence and end of valid packet data respectively. The RERR and RMOD signals are only valid at the end of a packet and are qualified with the REOP signal. When a packet is erred, the FREEDM 84A1024 may be programmed to overwrite RXDATA[15:0] in the final word of packet transfer with status information indicating the cause of the error. RXDATA[15:0] is not modified if a packet is error free.

The RXADDR[3:0] signals serve to poll FREEDM 84A1024 devices as well as for selection. During data transfer, the RXADDR[3:0] signals continue to poll the FREEDM 84A1024 devices sharing the Rx APPI. Polled results are returned on the RPA signal. Note that each poll address is separated by a NULL address to generate tristate turn-around cycle in order to prevent multiple FREEDM 84A1024 devices from briefly driving RPA. If RPA is a point-to-point signal for each FREEDM 84A1024 device on the board, then the tristate turn-around cycle is not required, thereby effectively doubling the polling bandwidth at the expense of extra signals.

Polled results reflect the status of the Rx APPI. Polled responses always refer to the next segment transfer. In other words, polled responses during or after the RXCLK cycle where RSX is set high refer to a segment which is not involved in the current data transfer. This allows the external controller to gather knowledge about the segment not involved in the current segment transfer so that it can anticipate reselecting that FREEDM 84A1024 device (via RENB) to maximize bandwidth on the Rx APPI (shown in Figure 41).

Figure 40 - Receive APPI Timing (Auto Deselection)

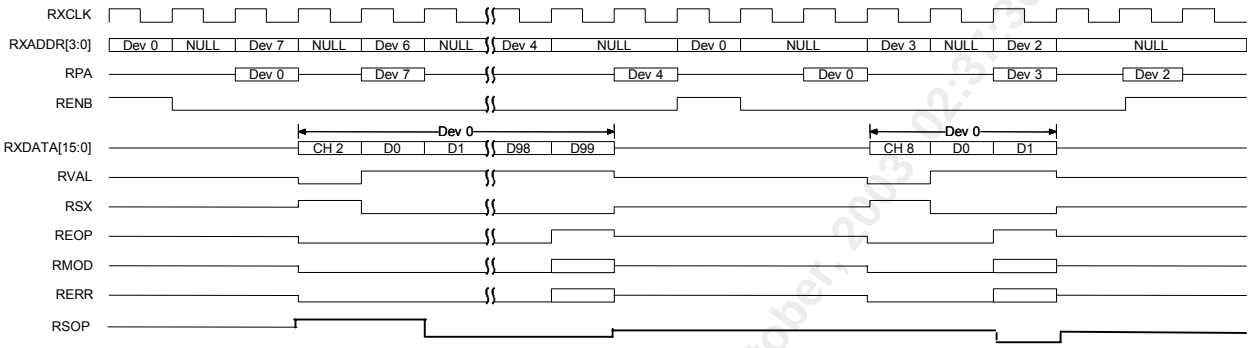


Figure 40 shows the transfer of a 100 word packet across the Rx APPI from FREEDM 84A1024 device 0, channel 2 followed by the transfer of a 2 word packet from FREEDM 84A1024 device 0, channel 8. More importantly, Figure 40 illustrates that, for back-to-back transfers from the same FREEDM 84A1024 (device 0), it must be reselected before any further data is provided on the Rx APPI.

At the end of the first 100 word packet transfer across the Rx APPI, the FREEDM 84A1024 automatically deselects and must be reselected before the second two word packet is transferred. When the external controller samples REOP high, it recognizes that the burst transfer has completed. Two RXCLK cycles later, the external controller reselects FREEDM 84A1024 device 0 by setting RENB high and placing address 0 on the RXADDR[3:0] signals. When the FREEDM 84A1024 samples RENB low, it begins the next data transfer as before.

Figure 41 - Receive APPI Timing (Optimal Reselection)

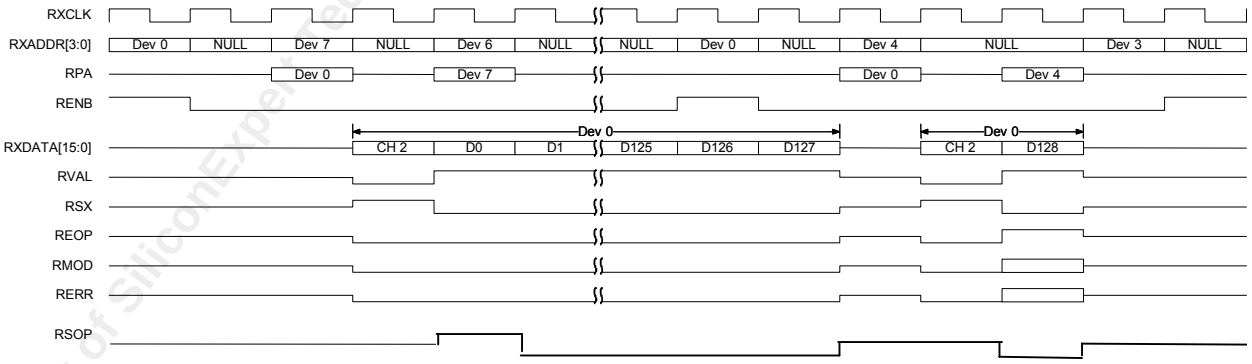


Figure 41 shows optimal bandwidth utilization across the Rx APPI.

With knowledge that the maximum burst data transfer (excluding ANY-PHY channel address prepend) is 256 bytes, i.e. 128 words, the external controller sets RENB high when the 127th word (D126) is placed on RXDATA[15:0] in anticipation of the end of a burst transfer. The FREEDM 84A1024 completes the burst data transfer and tristates the Rx APPI one RXCLK cycle after RENB is sampled high. Because the burst data transfer is complete and RENB is immediately returned low following selection, the FREEDM 84A1024 immediately begins the next data transfer following the single turn-around cycle.

The protocol dictates that at least one tristate turn-around cycle be inserted between data transfers, even if the external controller is reselecting the same FREEDM 84A1024 device. In other words, Figure 41 shows the earliest possible time that the external controller could have set RENB high to reselect FREEDM 84A1024 device 0.

Figure 42 - Receive APPI Timing (Boundary Condition)

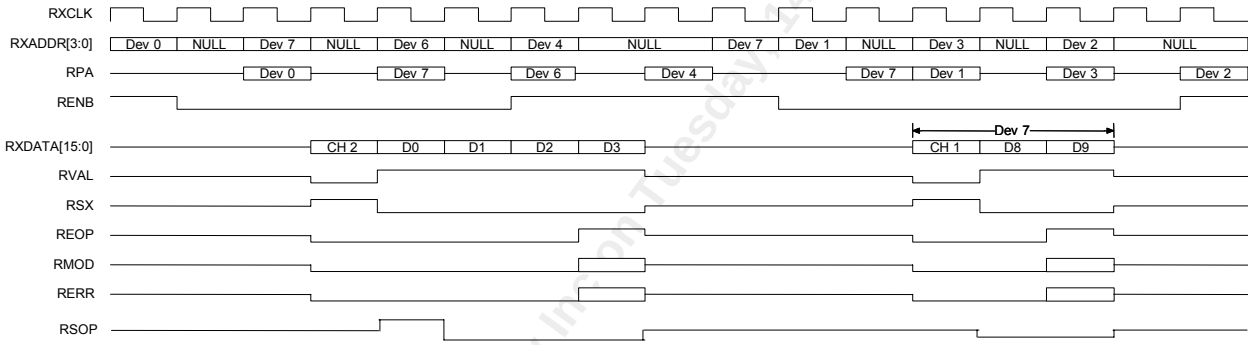


Figure 42 shows the boundary condition where a packet transfer completes shortly after the external controller has set RENB high to pause the FREEDM 84A1024 device. The second data transfer is the final two words of a packet for FREEDM 84A1024 device 7, channel 1.

When FREEDM 84A1024 device 0 places D2 on RXDATA[15:0], the external controller sets RENB high to pause the FREEDM 84A1024 device. In the following RXCLK cycle, the FREEDM 84A1024 provides D3 on RXDATA[15:0] and sets REOP high to conclude packet transfer. The external controller samples REOP high while RENB is high and recognizes that the packet transfer is complete. The external controller now knows that it doesn't need to reselect FREEDM 84A1024 device 0, but can select another FREEDM 84A1024 device sharing the Rx APPI. The external controller decides to select FREEDM 84A1024 device 7 by placing this address on the RXADDR[3:0] signals. The external controller sets RENB low to commence data transfer from FREEDM 84A1024 device 7.

14.6. Transmit APPI Timing (ANY-PHY Level 2)

The transmit ANY-PHY packet interface (APPI) timing is shown in Figure 43. An external controller provides data to the FREEDM 84A1024 device using the transmit APPI. The following discussion surrounding the transmit APPI functional timing assumes that multiple FREEDM 84A1024 devices share a single external controller. The FREEDM 84A1024 compares the TXADDR[15:0] to the base and range address registers to determine if the poll request is destined for the particular FREEDM 84A1024. All Tx APPI signals are shared between the FREEDM 84A1024 devices.

Figure 43 - Transmit APPI Timing (Normal Transfer)

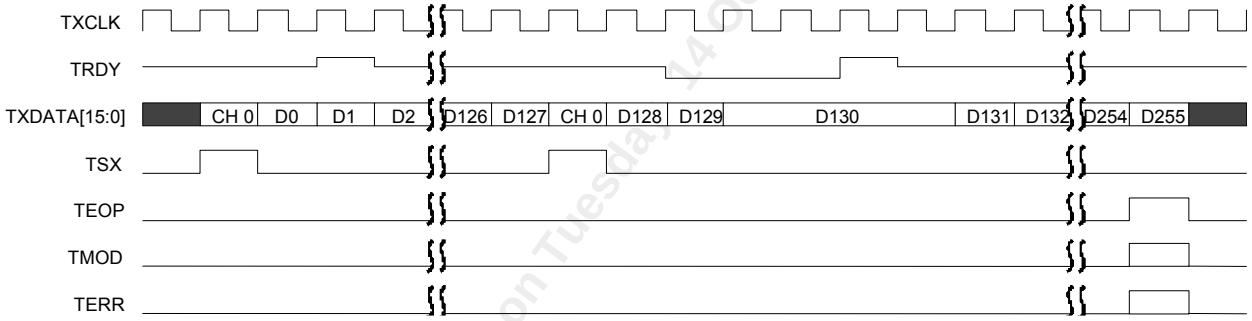


Figure 43 shows transfer of a 256 word packet on the Tx APPI for ANY-PHY channel 0. The maximum burst data transfer (excluding channel address prepend) is 128 words, so two data transfers are required to complete the transfer of the 256 word packet. The start of all burst data transfers is qualified with the TSX signal and an in-band channel address on TXDATA[15:0] to associate the data to follow with an ANY-PHY channel. The TEOP signal indicates the end of valid packet data. The TMOD and TERR signals are held low except at the end of a packet (TEOP set high).

The FREEDM 84A1024 starts driving the TRDY signal one TXCLK cycle after TSX is sampled high. Upon sampling the TRDY signal high, the external controller completes the current burst data transfer. The FREEDM 84A1024 tristates the TRDY signal one TXCLK cycle after it has been driven high. This is the case for the first burst data transfer in Figure 43. In the second burst data transfer, the FREEDM 84A1024 drives the TRDY signal low to indicate that the FIFO in the Tx APPI is full and no further data may be transferred. Upon sampling the TRDY signal low, the external controller must hold the last valid word of data on TXDATA[15:0]. The FREEDM 84A1024 may drive TRDY low for an indeterminate number of TXCLK cycles. During this time, the external controller must wait and is not permitted to begin another burst data transfer until TRDY is sampled high. When there is space in the Tx APPI FIFO, the FREEDM 84A1024 drives the TRDY signal high. Upon sampling the TRDY signal high, the external controller completes the current burst data transfer. The FREEDM 84A1024 tristates the TRDY signal one TXCLK cycle after it has been driven high.

The external controller must sample the TRDY signal high and must then wait 1 clock cycle before it can begin the next burst data transfer. This prevents the external controller from bombarding the FREEDM 84A1024 device with small packets and allows the FREEDM 84A1024 to perform the necessary housekeeping and clean up associated with the ending of burst data transfers. In addition, the rule that TSX must be a minimum of 4 clock cycles apart must be adhered to. This protocol also ensures that transitions between burst data transfers do not require any extra per ANY-PHY channel storage, thereby simplifying implementation of both the external controller and the FREEDM 84A1024 device. Figure 44 illustrates this condition.

Figure 44 - Transmit APPI Timing (Special Conditions)

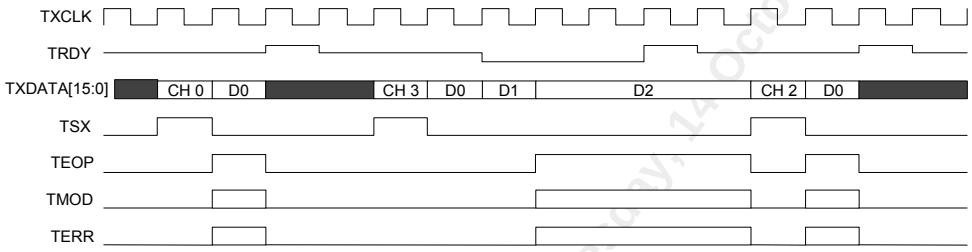
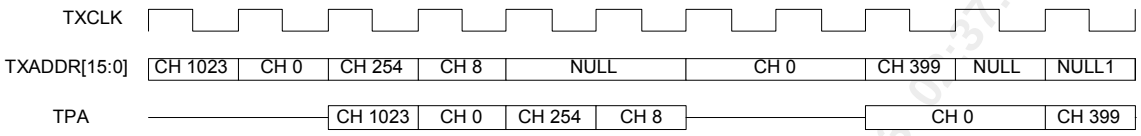


Figure 44 shows two special conditions – (1) the transfer of a one word packet illustrating how the external controller must wait until TRDY has been sampled high before the next data transfer can begin, and (2) the transfer of a packet which completes when TRDY is set low illustrating that although the packet has been completely transferred, the external controller must still wait until TRDY has been sampled high before the next data transfer can begin.

The first data transfer is a single word packet for ANY-PHY channel 0. The FREEDM 84A1024 asserts TRDY high one TXCLK cycle after TSX is sampled high. The Tx APPI protocol dictates that the external controller must wait until one clock after TRDY is sampled high before beginning the next data transfer for ANY-PHY channel 3. The external controller must hold the last valid word on TXDATA[15:0] until TRDY is sampled high. In this case, that data is a don't care. The FREEDM 84A1024 tristates the TRDY signal one TXCLK cycle after it has been driven high.

The second transfer is a three word packet, which completes transfer in the same TXCLK cycle that TRDY is sampled low by the external controller. Again, the external controller must hold the last valid word on TXDATA[15:0] until TRDY is sampled high. In this case, that data is D2, the last word of the packet. The FREEDM 84A1024 may drive TRDY low for an indeterminate number of TXCLK cycles. During this time, the external controller must wait and is not permitted to begin another burst data transfer until TRDY is sampled high. When the external controller samples TRDY high, the current burst transfer is deemed to be complete and the external controller may begin the next data transfer. The FREEDM 84A1024 tristates the TRDY signal one TXCLK cycle after it has been driven high.

Figure 45 - Transmit APPI Poll Timing



When supporting ANY-PHY Level 2 packet mode, polling is completely decoupled from device and ANY-PHY channel selection on the Tx APPI (Figure 45). Accordingly, the TXADDR[15:0] signals continue to provide only a poll address for any of the FREEDM 84A1024 devices sharing the Tx APPI. The FREEDM 84A1024 compares the TXADDR[15:0] to the base and range address registers to determine if the channel being polled resides within the device. Poll results are returned on the TPA signals. The TPA bit indicates whether or not space exists in the ANY-PHY channel FIFO for data (high means space to accept 9600 bytes in packet mode exists in the ANY-PHY channel FIFO).

14.7. Receive APPI Timing (ANY-PHY Level 3)

The receive ANY-PHY packet interface (APPI) timing is shown in Figure 46 when the ANY-PHY interface operates at 104 MHz, RXDATA[7:0] are valid. The FREEDM 84A1024 device provides data to an external controller using the receive APPI.

Figure 46 - Receive APPI Timing (Normal Transfer 8 bit 104 MHz)

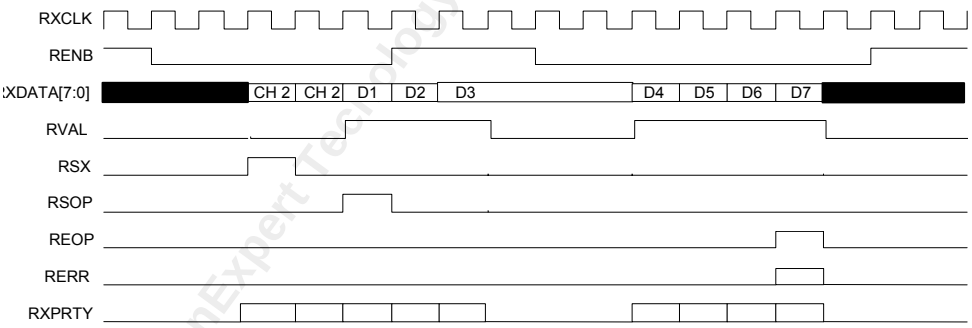


Figure 46 shows the transfer of an 8 byte packet across the Rx APPI from FREEDM 84A1024. The external controller sets RENB low to commence data transfer across the Rx APPI. The FREEDM 84A1024 samples RENB low and responds by asserting RSX one RXCLK cycle later. The start of all burst data transfers is qualified with RSX and an in-band ANY-PHY channel address on RXDATA[7:0] to associate the data to follow with an ANY-PHY channel. The RSOP signal is asserted 2 cycles after the RSX allowing the controller to identify the start of packet. The first two bytes indicate the ANY-PHY channel (CH 2) while the next two bytes contain either a connection identifier or the first two bytes of the packet.

During the cycle when D2 is placed on RXDATA[7:0], the external controller is unable to accept any further data and sets RENB high. Two RXCLK cycles later, the FREEDM 84A1024 pauses the Rx APPI. The external controller may hold RENB high for an indeterminate number of RXCLK cycles. The FREEDM 84A1024 will wait until the external controller returns RENB low.

The FREEDM 84A1024 will not pause burst data transfers across the Rx APPI.

The RVAL and REOP signals indicate the presence and end of valid packet data respectively. The RERR and RMOD signals are only valid at the end of a packet and are qualified with the REOP signal. When a packet is erred, the FREEDM 84A1024 may be programmed to overwrite RXDATA[7:0] in the final word of packet transfer with status information indicating the cause of the error. RXDATA[7:0] is not modified if a packet is error free

14.8. Transmit APPI Timing (ANY-PHY Level 3)

The transmit ANY-PHY packet interface (APPI) timing is shown in Figure 47 through Figure 49. An external controller provides data to the FREEDM 84A1024 device using the transmit APPI. The following discussion surrounding the transmit APPI functional timing assumes that point to point interfaces exist between FREEDM 84A1024 and the external controller. The FREEDM 84A1024 compares the TXADDR[15:0] to the base and range address registers to determine if the address is destined for the FREEDM 84A1024 .

Figure 47 - Transmit APPI Timing ANY-PHY Level 3 (Normal Transfer)

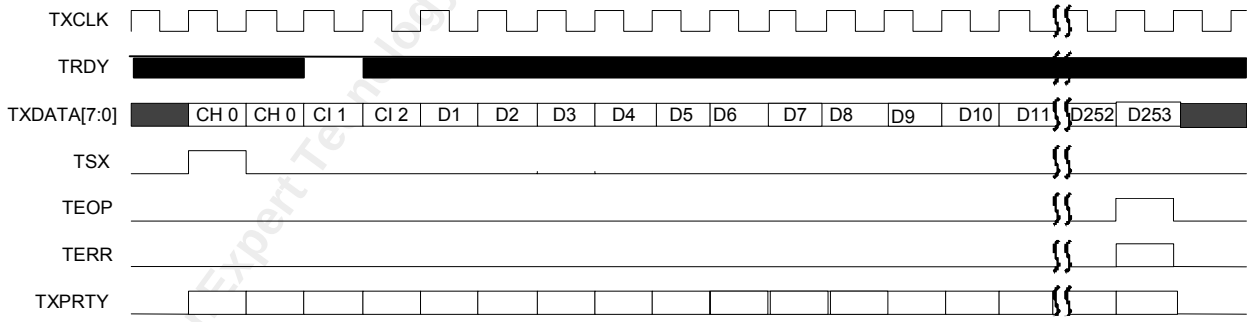


Figure 47 shows transfer of a 254 byte packet on the Tx APPI of FREEDM 84A1024 . The start of all burst data transfers is qualified with the TSX signal and an in-band ANY-PHY channel address on TXDATA[7:0] to associate the data to follow with an ANY-PHY channel. The TEOP signal indicates the end of valid packet data. The TERR signal is held low except at the end of a packet (TEOP set high).

The TRDY signal is valid one TXCLK cycle after TSX is sampled high. Upon sampling the TRDY signal high, the external controller completes the current burst data transfer. This is the case for the first burst data transfer in Figure 47. In Figure 48, the FREEDM 84A1024 drives the TRDY signal low to indicate that the FIFO in the Tx APPI are full and no further data may be transferred. Upon sampling the TRDY signal low, the external controller must hold the last valid word of data on TXDATA[7:0]. The FREEDM 84A1024 may drive TRDY low for an indeterminate number of TXCLK cycles. During this time, the external controller must wait and is not permitted to begin another burst data transfer until TRDY is sampled high. Upon sampling the TRDY signal high, the external controller completes the current burst data transfer.

The external controller can sample the TRDY signal high before it can begin the next burst data transfer. TRDY is provided to prevent the external controller from bombarding the FREEDM 84A1024 device with small packets and allows the FREEDM 84A1024 to perform the necessary housekeeping and clean up associated with the ending of burst data transfers. In addition, the rule that TSX must be a minimum of 4 clock cycles apart must be adhered. This protocol also ensures that transitions between burst data transfers do not require any extra per ANY-PHY channel storage, thereby simplifying implementation of both the external controller and the FREEDM 84A1024 device. Figure 48 illustrates this condition.

Figure 48 - Transmit APPI Timing ANY-PHY Level 3 (Special Condition)

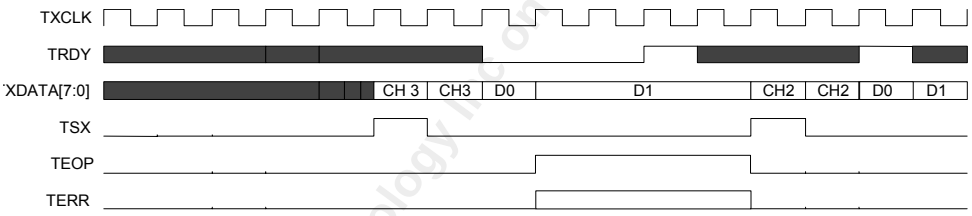
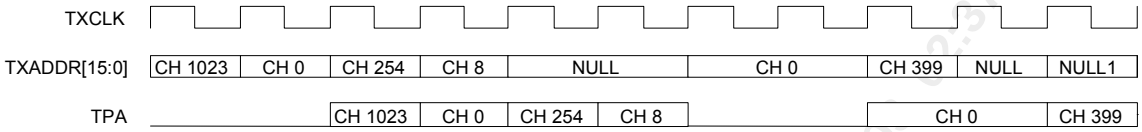


Figure 48 shows a special condition where the transfer of a packet that completes when TRDY is set low, illustrating that although the packet has been completely transferred, the external controller must still wait until TRDY has been sampled high before the next data transfer can begin.

The illustrated transfer is a two byte packet, which completes transfer in the same TXCLK cycle that TRDY is sampled low by the external controller. The external controller must hold the last valid byte on TXDATA[7:0] until TRDY is valid and sampled high. In this case, that data is D1, the last byte of the packet. The FREEDM 84A1024 may drive TRDY low for an indeterminate number of TXCLK cycles. During this time, the external controller must wait and is not permitted to begin another burst data transfer until TRDY is valid and sampled high. When the external controller samples TRDY high, the current burst transfer is deemed to be complete and the external controller may begin the next data transfer.

Figure 49 - Transmit APPI Polling Timing (ANY-PHY Level 3)



When supporting ANY-PHY Level 3 mode polling is completely decoupled from data transfer on the Tx APPI (Figure 49) with the restriction that the TPA poll result is invalid for all channels if it corresponds to a TXADDR poll coincident with the start of transfer (ie the cycle in which TSX is driven high). Accordingly, the TXADDR[15:0] signals continue to provide only a poll address for the FREEDM 84A1024 device The FREEDM 84A1024 compares the TXADDR[15:0] to the base and range address registers to determine if the ANY-PHY channel being polled resides within the device. Poll results are returned on the TPA signal. The TPA bit indicates whether or not space exists in the ANY-PHY channel FIFO for a 9600 byte packet (high means space exists in the ANY-PHY channel FIFO). For unprovisioned channels, TPA=0.

14.9. Re-Sequencing SDRAM Interface

The following two diagrams depict the timing for signals destined for the pins of the Re-sequencing SDRAM during the Activate-Read (with Auto-precharge), and Activate-Write (with Auto-precharge sequences.

Figure 50 - Read Timing for Re-Sequencing memory

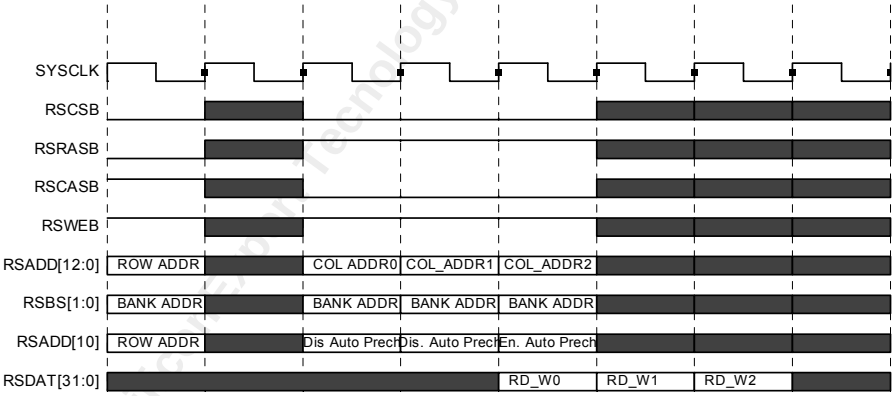
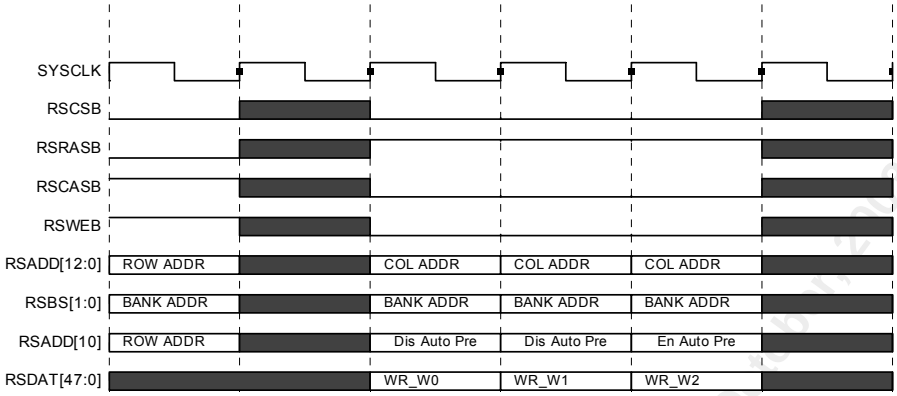


Figure 51 - Write Timing Re-Sequencing memory



14.10. Chunk Buffer SDRAM Interface

The following two diagrams depict the timing for signals destined for the pins of the Chunk Buffer SDRAM during the Activate-Read (with Auto-precharge), and Activate-Write (with Auto-precharge sequences.

Figure 52 - Read Timing for Chunk Buffer memory

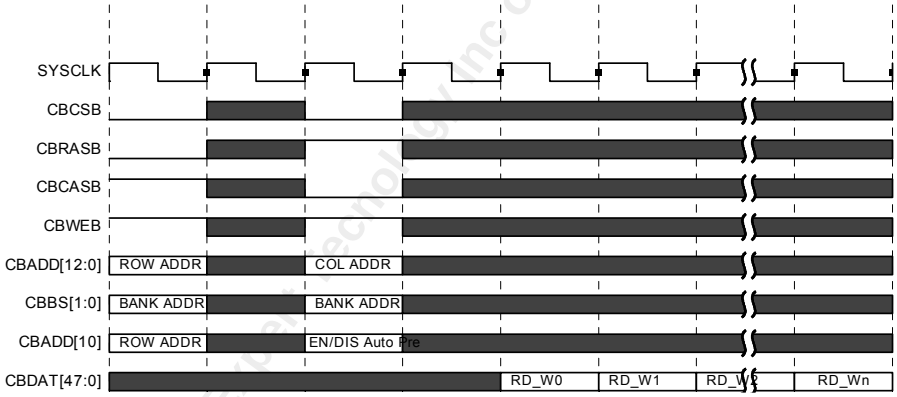
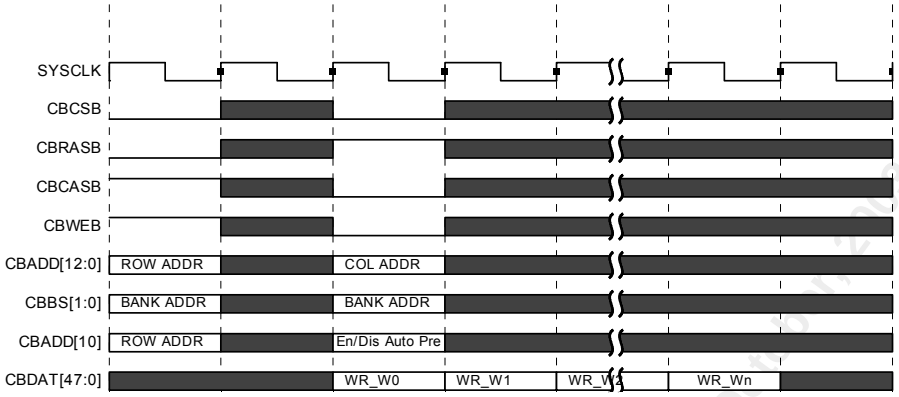


Figure 53 - Write Timing for Chunk Buffer memory



14.11. Context SSRAM Interface (ZBT SSRAM mode)

The following diagrams depict the timing for the pipelined ZBT SSRAM and Standard SSRAM during a read followed by a write cycle.

Figure 54 -Read followed by Write Timing for ZBT mode

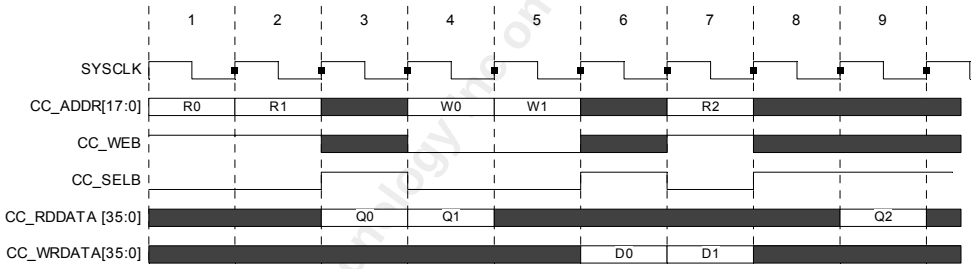
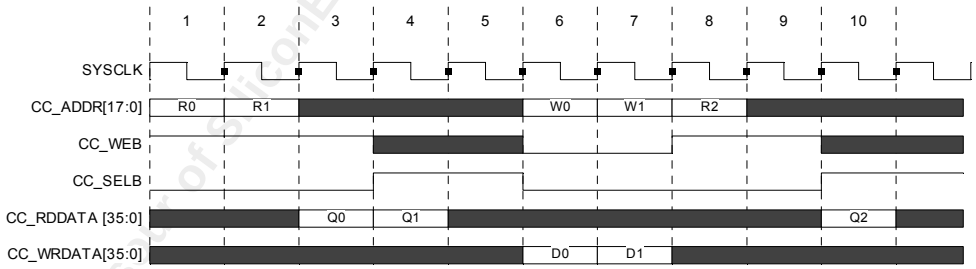


Figure 55 - Read followed by Write Timing for Standard SSRAM mode



14.12. Microprocessor Interface

The following diagrams illustrate the various handshaking required for microprocessor reads and writes.

Figure 56 shows a single read and write operation to the non-burstable register space with bus polarity set to 1. On the first cycle, BURSTB is sampled inactive; therefore, it is expected that the cycle is a single data transfer, and the BLAST signal is of no significance. The subsequent 2 cycles have BURSTB sampled active hence the transfer cycle is terminated when both BLAST and READYB are asserted. Note that between each transfer, there is a turn around cycle provided by the external interface to ensure that there is no bus contention on back to back transfers on the AD bus.

Figure 56 - Read and Write to non-burstable register space

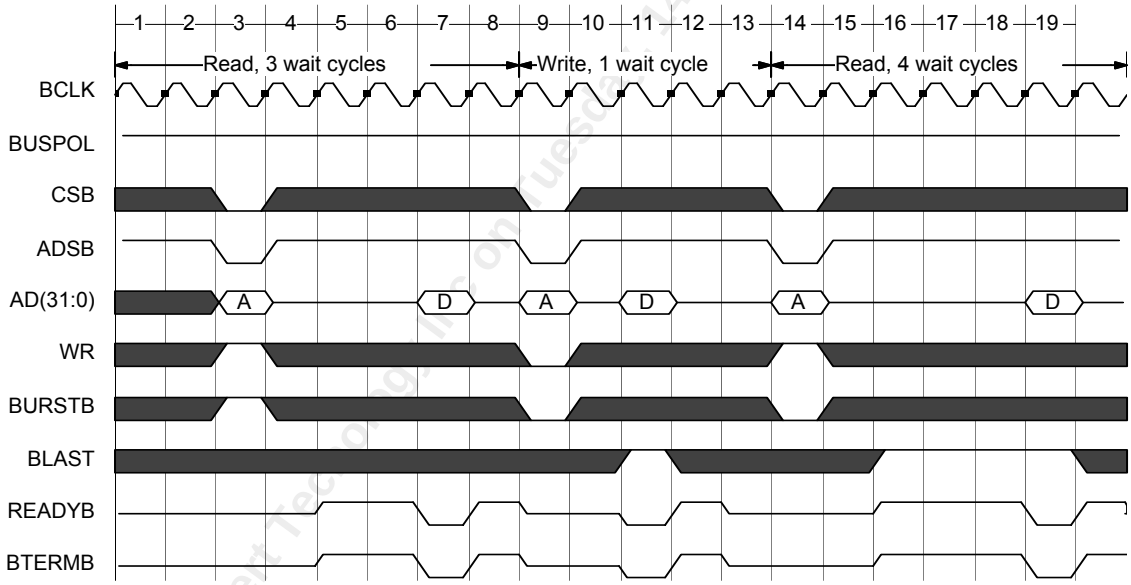


Figure 57 shows a burst read and write operation (only valid for burstable registers) with bus polarity set to 0. The first and third accesses illustrate transfers that are terminated by the FREEDM 84A1024 via the assertion of BTERMB. The second and fourth accesses illustrate transfers that are terminated by the external interface via the assertion of BLAST. Note that between each transfer, there is no turn around cycle. Care must be taken to examine the AC timing to ensure that there is no bus contention on the AD bus between a read followed by a write transfer. BTERMB is only asserted when the burst access is 4 cycles long. It is not asserted if the burst cycle is terminated by BLAST or for non-burst accesses (BURSTB=1).

Figure 57 Read and Write to burstable address space

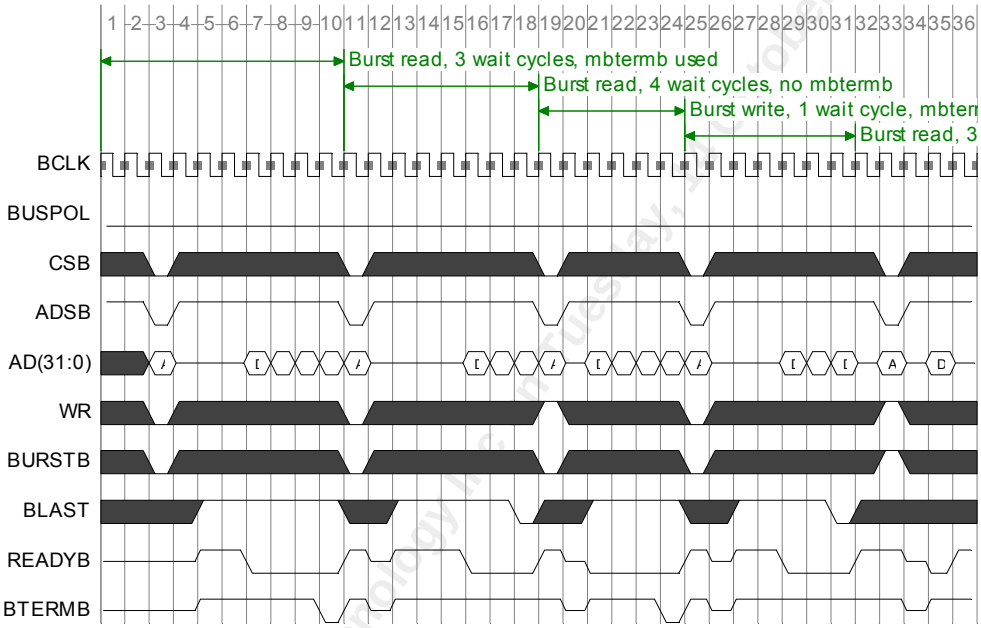
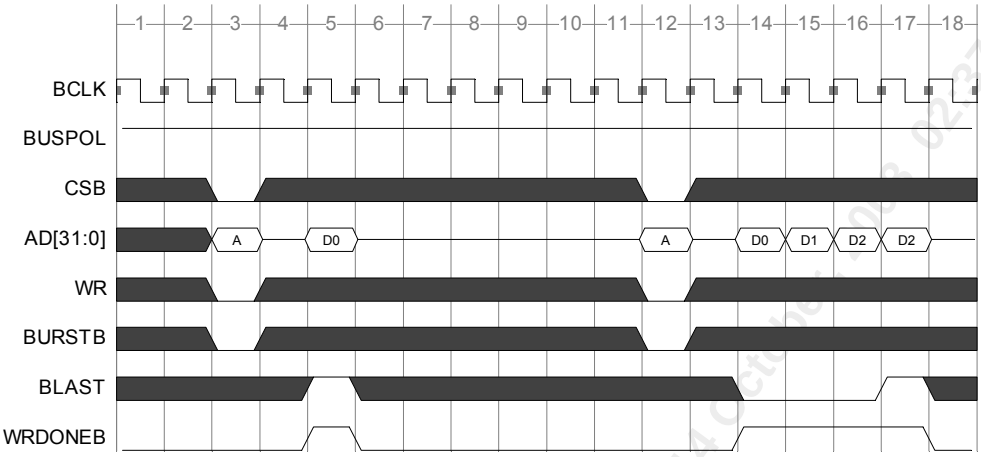


Figure 58 shows consecutive write operations using the WRDONEB signal without the READYB. Write operations may only begin when WRDONEB is sampled low by the external interface. On the first data transfer, the cycle is terminated normally. Subsequent access does not begin until WRDONEB is sampled low by the external interface. This interface is used when the external processor is incapable of dealing with wait states during write

Figure 58 - Consecutive Write Accesses Using WRDONEB



15. Absolute Maximum Ratings

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal operating conditions.

Table 52 - FREEDM 84A1024 Absolute Maximum Ratings

Ambient Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage (+3.3 Volt $V_{DD3.3}$)	-0.3V to +4.6V
Supply Voltage (+1.8 Volt $V_{DD1.8}$)	-0.3V to +2.5 V
Voltage on Any Pin	-0.3V to $V_{DD3.3}$ + 0.3V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+120° C

16. D.C. Characteristics

(T_A = -40°C to +85°C, $V_{DD3.3}$ = 3.0 to 3.6 V, $V_{DD1.8}$ = 1.71 to 1.94 V)

Table 53 - FREEDM 84A1024 D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{DD3.3}$	3.3V Power Supply	3.0	3.3	3.6	Volts	Note 5.
$V_{DD1.8}$	1.8V Power Supply	1.71	1.8	1.94	Volts	Note 5.
V_{IL}	Input Low Voltage	-0.3		0.8	Volts	
V_{IH}	Input High Voltage	2.0		$V_{DD3.3}$ + 0.3	Volts	
V_{OL}	Output or Bi-directional Low Voltage			0.4	Volts	I_{OL} = -9 mA for all outputs except TDO where I_{OL} = -6 mA, and AD[31:0], READYB, BTERMB, WRDONEB where I_{OL} = -12 mA. Note 3.
V_{OH}	Output or Bi-directional High Voltage	2.4			Volts	I_{OH} = 9 mA for all outputs except TDO where I_{OH} = 6 mA, and AD[31:0], READYB, BTERMB, WRDONEB where I_{OH} = 12 mA. Note 3.
I_{ILPU}	Input Low Current	+10	+150	+200	µA	V_{IL} = GND, Notes 1, 3, 5.
I_{IHPU}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}, Notes 1, 3
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND, Notes 2, 3
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}, Notes 2, 3
C_{IN}	Input Capacitance		5		pF	Excludes package. Package typically 2 pF. Note 5.
C_{OUT}	Output Capacitance		5		pF	All pins. Excludes package. Package typically 2 pF. Note 5.
C_{IO}	Bi-directional Capacitance		5		pF	All pins. Excludes package. Package typically 2 pF. Note 5.
L_{PIN}	Pin Inductance		2		nH	All pins. Note 5.
IDDOP1V8	Operating Current, core		0.78		A	VDD1.8 = 1.8V, Outputs with typical load. Full OC-3 operation.
IDDOP1V8	Operating Current, core		0.85		A	VDD1.8 = 1.94V, Outputs with typical load. Full OC-3 operation.
IDDOP3V3	Operating Current, I/O Ring		0.07		A	VDD3.3= 3.3V, Outputs with typical load. Full OC-3 operation.
IDDOP3V3	Operating Current, I/O Ring		0.08		A	VDD3.3= 3.6V, Outputs with typical load. Full OC-3 operation.

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor.
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. Input pin or bi-directional pin with internal pull-down resistor.
5. Typical values are given as a design aid. The product is not tested to the typical values given in the data sheet.

17. FREEDM 84A1024 Timing Characteristics

(T_A = -40°C to +85°C, $V_{DD3.3}$ = 3.0 to 3.6 V, $V_{DD1.8}$ = 1.71 to 1.94 V)

Notes on Input Timing

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Loads used to measure maximum output propagation delays are specified with each table.

3. 0pF load is used to measure minimum output propagation delays.

Output tristate delay is the time in nanoseconds from the 1.4 Volt point of the reference signal to the point where the total current delivered through the output is less than or equal to the leakage current transfer.

17.1. SBI Bus Interface Timing

Table 54 - REFCLK Timing

Symbol	Description	Min	Max	Units
f_{CLK}	Frequency, REFCLK =19.44MHz	-50	+50	ppm
	OR 77.76MHz	-20	+20	ppm
D_{CLK}	Duty Cycle, REFCLK	40	60	%

17.2. SBI Drop Bus Interface Timing

Figure 59 - SBI Drop Bus Input Interface Timing

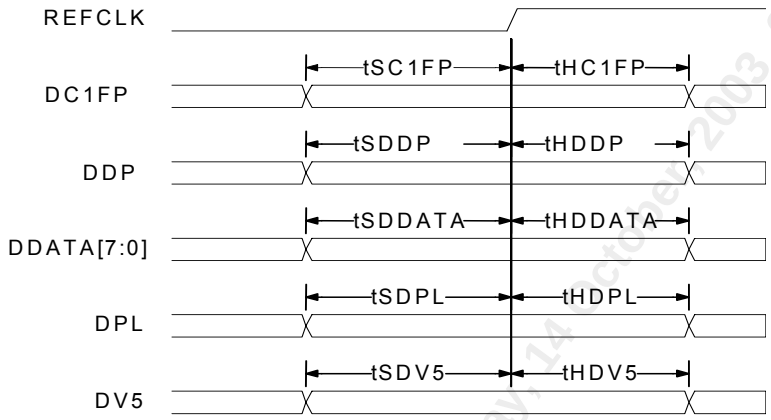


Table 55 - SBI/SBI336 Drop Bus Input Timing (referenced to (Figure 59))

Symbol	Parameter	Min	Max	Units
tSC1FP	REFCLK to Valid DC1FP Set-up Time	2		ns
tHC1FP	REFCLK to Valid DC1FP Hold Time	0		ns
tSDDATA	REFCLK to Valid DDATA Set-up Time	2		ns
tHDDATA	REFCLK to Valid DDATA Hold Time	0.3		ns
tSDPL	REFCLK to Valid DPL Set-up Time	2		ns
tHDPL	REFCLK to Valid DPL Hold Time	0.3		ns
tSDV5	REFCLK to Valid DV5 Set-up Time	2		ns
tHDV5	REFCLK to Valid DV5 Hold Time	0.3		ns
tSDDP	REFCLK to Valid DDP Set-up Time	2		ns
tHDDP	REFCLK to Valid DDP Hold Time	0.3		ns

17.3. SBI Add Bus Interface Timing

Figure 60 - SBI336 Add Bus Input Interface Timing

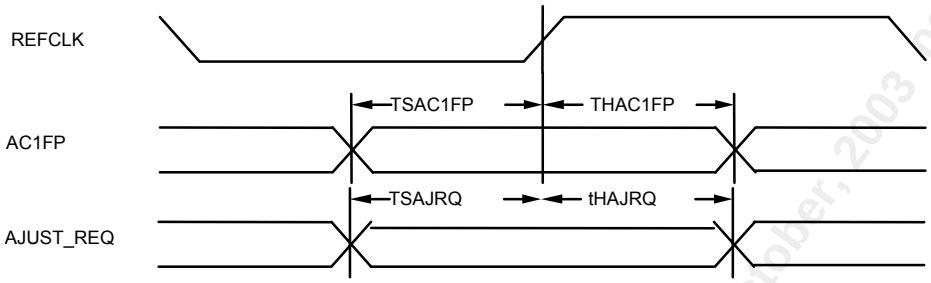


Table 56 - SBI/SBI336 Add Bus Input Timing (referenced to Figure 60)

Symbol	Parameter	Min	Max	Units
TSAC1FP	REFCLK to Valid AC1FP Set-up Time	2		ns
THAC1FP	REFCLK to Valid AC1FP Hold Time	0		ns
TSAJRQ	REFCLK to Valid AJUST_REQ Set-up Time	2		ns
THAJRQ	REFCLK to Valid AJUST_REQ Hold Time	0		ns

Notes

1. Input setup and hold times do not apply to ADETECT[1:0].

Figure 61 - SBI Add Bus Output Interface Timing

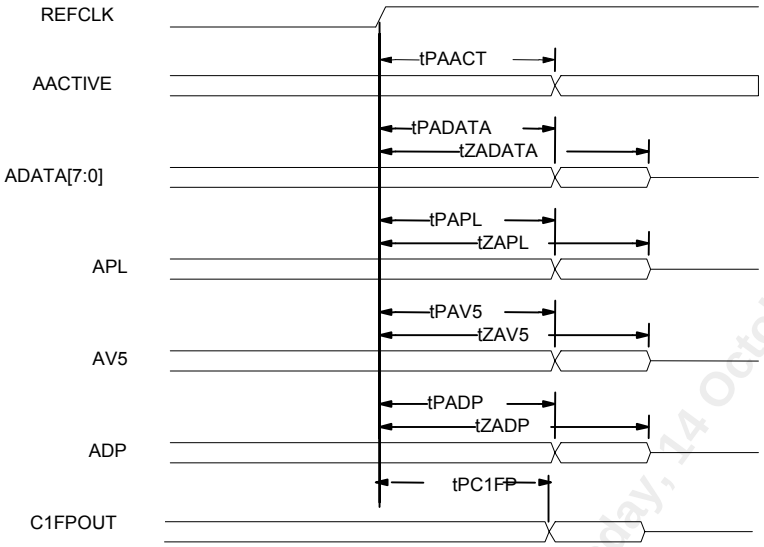


Figure 62 - SBI ADD BUS Collision Avoidance Timing

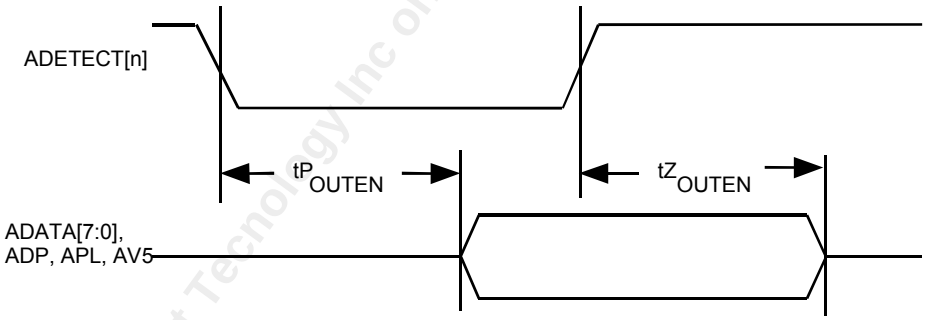


Table 57 - SBI/SBI336 Add Bus Output Timing (referenced to Figure 61 and Figure 62)

Symbol	Parameter	Min	Max	Units
tPAACT	REFCLK Edge to AACTIVE Prop Delay	1	8	ns
tPADATA	REFCLK Edge to ADATA Prop Delay	1	8.3	ns
tZADATA	REFCLK Edge to ADATA Output Tri-state	1	9	ns
tPAPL	REFCLK Edge to APL Prop Delay	1	8	ns
tZAPL	REFCLK Edge to APL Output Tri-state	1	9	ns
tPAV5	REFCLK Edge to AV5 Prop Delay	1	8.3	ns
tZAV5	REFCLK Edge to AV5 Output Tri-state	1	9	ns
tPADP	REFCLK Edge to ADP Prop Delay	1	8	ns
tZADP	REFCLK Edge to ADP Output Tri-state	1	9	ns

Symbol	Parameter	Min	Max	Units
TPC1FP	REFCLK Edge to C1FPOUT Prop Delay	1	9	ns
TPOUTEN	ADETECT[1] and ADETECT[0] low to All SBI ADD BUS Outputs (except AACTIVE) Valid	2	13	ns
TZOUTEN	ADETECT[1] or ADETECT[0] high to All SBI ADD BUS Outputs (except AACTIVE) Tristate	2	13	ns

Notes

1. Although the AJUST_REQ is referenced to the Drop bus DC1FP alignment the timing from REFCLK is independent of the Add or Drop side of the SBI bus.

2. Maximum output propagation delays are measured with a 50pF load on all outputs except C1FPOUT which is measured with a 100pF load.

17.4. Serial Clock and Data Timing

Table 58 - Clock/Data Input (Figure 63)

Symbol	Description	Min	Max	Units
	RCLK[0,4,8] Frequency		52	MHz
	RCLK[0,4,8] Duty Cycle	40	60	%
tS_{RD}	RD[0,4,8] Set-Up Time	2		ns
tH_{RD}	RD[0,4,8] Hold Time	1.5		ns

Figure 63 - Receive Data Timing

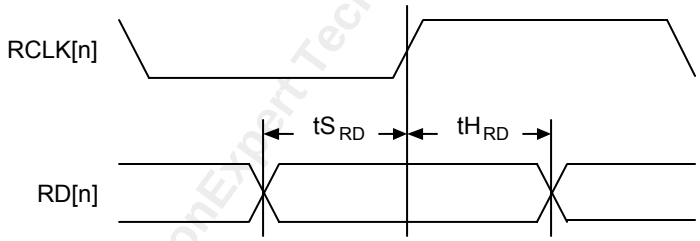


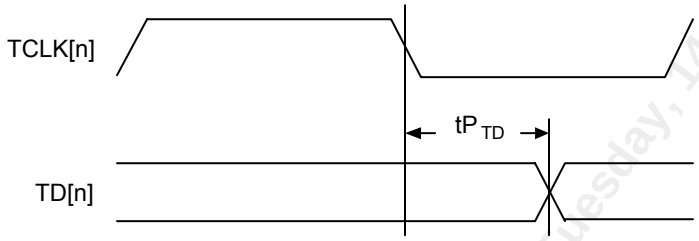
Table 59 - Clock/Data Output (Figure 64)

Symbol	Description	Min	Max	Units
	TCLK[0,4,8] Frequency		52	MHz
	TCLK[0,4,8] Duty Cycle	40	60	%
t_{PTD}	TCLK[0,4,8] Low to TD[0,4,8] Valid	3	12	ns

Notes:

1. Maximum output propagation delays are measured with a 50pF load on the output.

Figure 64 - Transmit Data Timing



17.5. ANY-PHY Timing

Table 60 - ANY-PHY Level 2 Interface (Figure 65 and Figure 66)

Symbol	Description	Min	Max	Units
	RXCLK Frequency	25	52	MHz
	RXCLK Duty Cycle	40	60	%
	TXCLK Frequency	25	52	MHz
	TXCLK Duty Cycle	40	60	%
t_{SAPPI}	All APPI Input Set-up time to RXCLK, TXCLK	4		ns
t_{HAPPI}	All APPI Input Hold time to RXCLK, TXCLK	1.1		ns
t_{PAPPI}	RXCLK, TXCLK to all APPI Outputs Valid	1	12	ns
t_{ZAPPI}	RXCLK, TXCLK to APPI Outputs Tristate	1	12	ns
t_{ZDAPPI}	RXCLK, TXCLK to APPI Outputs Driven	0		ns

Notes

1. Maximum output propagation delays are measured with a 50pF load on the output.

Table 61 - ANY-PHY Level 3 Interface (Figure 65 and Figure 66)

Symbol	Description	Min	Max	Units
	RXCLK Frequency	52	104	MHz

Symbol	Description	Min	Max	Units
	RXCLK Duty Cycle	40	60	%
	TXCLK Frequency	52	104	MHz
	TXCLK Duty Cycle	40	60	%
tS_{APPI}	All APPI Input Set-up time to RXCLK, TXCLK	2		ns
tH_{APPI}	All APPI Input Hold time to RXCLK, TXCLK	1.1		ns
tP_{APPI}	RXCLK, TXCLK to all APPI Outputs Valid	1.1	6.5	ns

Note:

Maximum output propagation delays are measured with a 20pF load on the output.

Figure 65 - Receive ANY-PHY Interface Timing

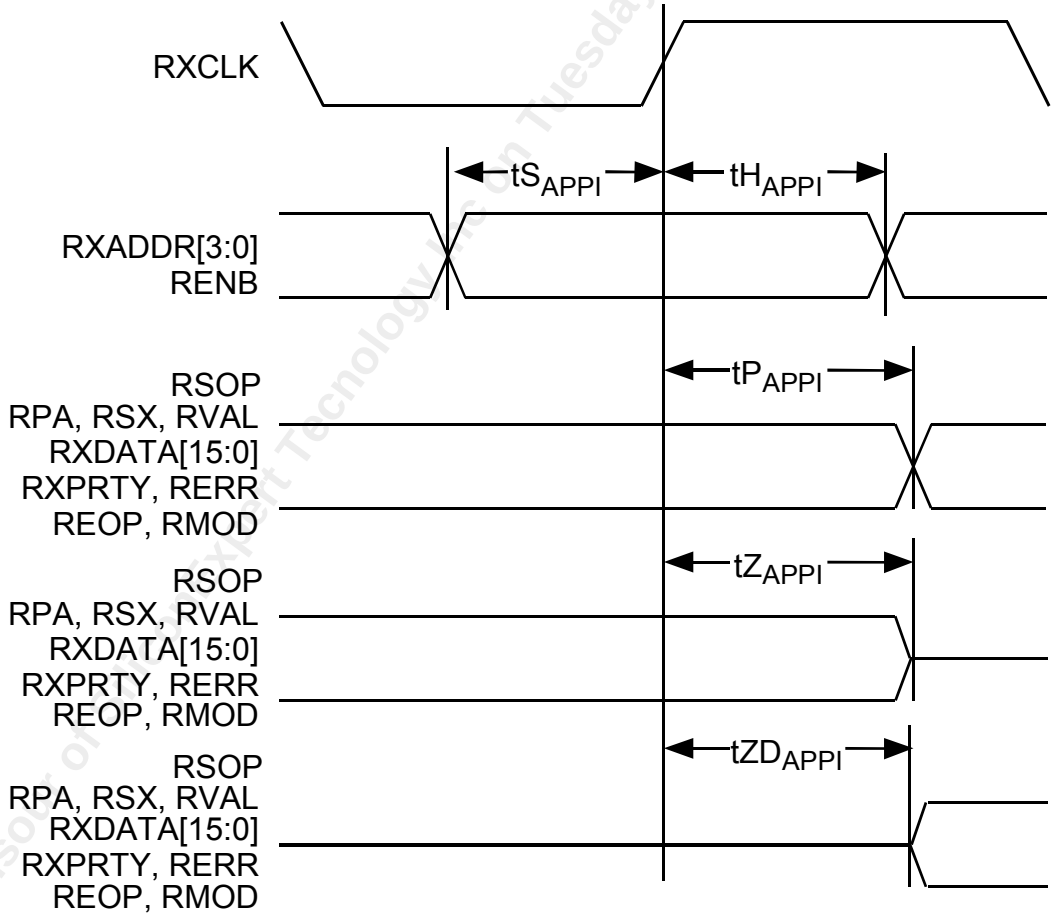
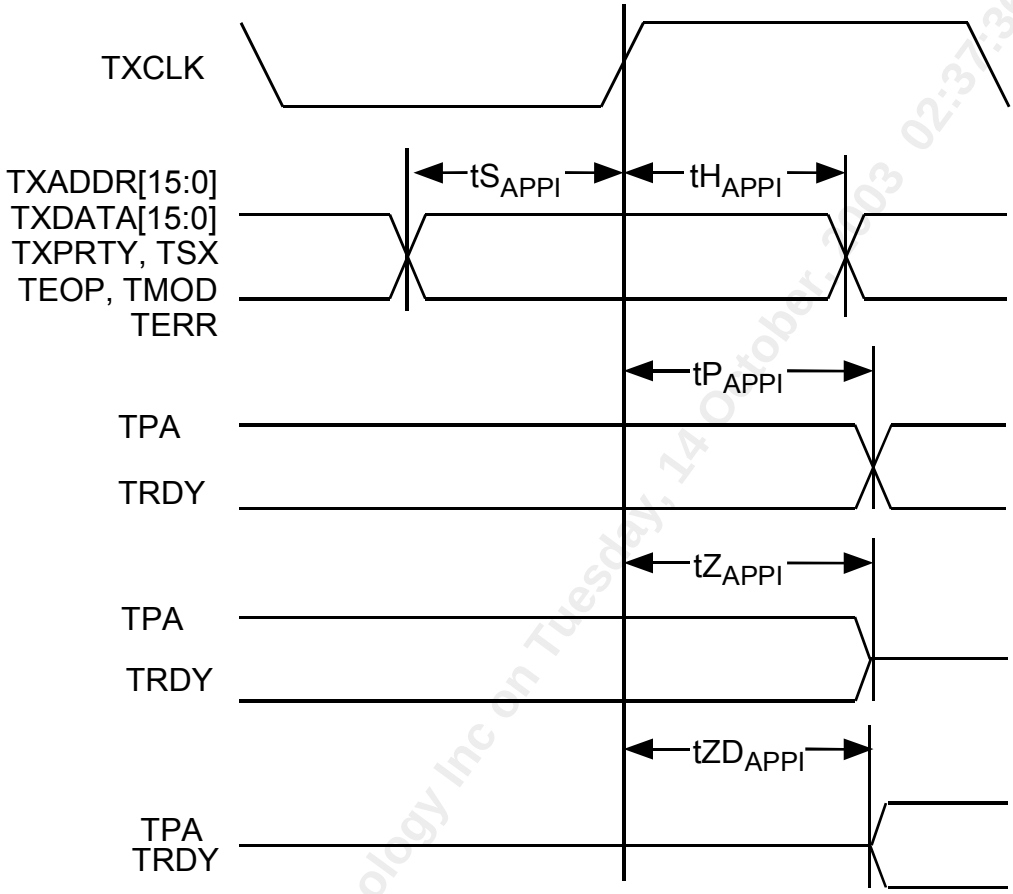


Figure 66 - Transmit ANY-PHY Interface Timing



17.6. Microprocessor Timing

Table 62 - Microprocessor Interface (Figure 67)

Symbol	Description	Min	Max	Units
f_{CLK}	Frequency, BCLK	33	66	MHz
D_{CLK}	Duty Cycle, BCLK	40	60	%
Ts	Input Set-up time to BCLK	4.0		ns
Th	Input Hold time to BCLK	1.1		ns
Tp	BCLK High to Output Valid	2.0	9.5	ns
Tz	BCLK High to Output High-Impedance	2.0	9.5	ns
Tzb	BCLK High to Output Driven	2.0		ns

Notes

1. Maximum output propagation delays are measured with a 50pF load on the output.

2. Input setup and hold times do not apply to BUSPOL.

3. Output Valid delays do not apply to INTHIB and INTLOB.

17.7. Memory Timing

Figure 67 - Synchronous I/O Timing

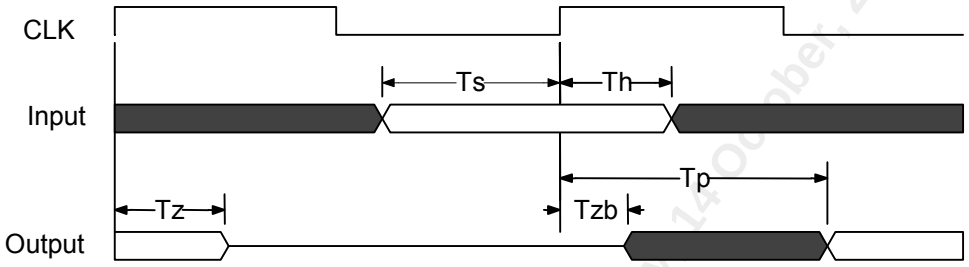


Table 63 - SYSCLK Timing

Symbol	Description	Min	Max	Units
f_{CLK}	Frequency, SYSCLK	90	100	MHz
D_{CLK}	Duty Cycle, SYSCLK	40	60	%

Table 64 - Resequencing SDRAM Interface (Figure 67)

Symbol	Description	Min	Max	Units
Ts	Input Set-up time to SYSCLK	2.5		ns
Th	Input Hold time to SYSCLK	0		ns
Tp	SYSCLK High to Output Valid	0.5	6.0	ns
Tz	SYSCLK High to Output High-Impedance	0.5	6.0	ns

Notes

1. Maximum output propagation delays are measured with a 30pF load on the output.

2. Output Valid delays do not apply to DQM.

Table 65 - Chunk Buffer SDRAM Interface (Figure 67)

Symbol	Description	Min	Max	Units
Ts	Input Set-up time to SYSCLK	2.5		ns
Th	Input Hold time to SYSCLK	0		ns
Tp	SYSCLK High to Output Valid	0.5	6.0	ns
Tz	SYSCLK High to Output High-Impedance	0.5	6.0	ns

Notes

1. Maximum output propagation delays are measured with a 30pF load on the output.

Table 66 - Connection Context Memory SSRAM Interface (Figure 67)

Symbol	Description	Min	Max	Units
Ts	Input Set-up time to SYSCLK	3.5		ns
Th	Input Hold time to SYSCLK	0		ns
Tp	SYSCLK High to Output Valid	0.5	6.5	ns
Tz	SYSCLK High to Output High-Impedance	0.5	6.5	ns
Tzb	SYSCLK High to Output Driven	0.5		ns

Notes

1. Maximum output propagation delays are measured with a 20pF load on the output.

17.8. JTAG Timing

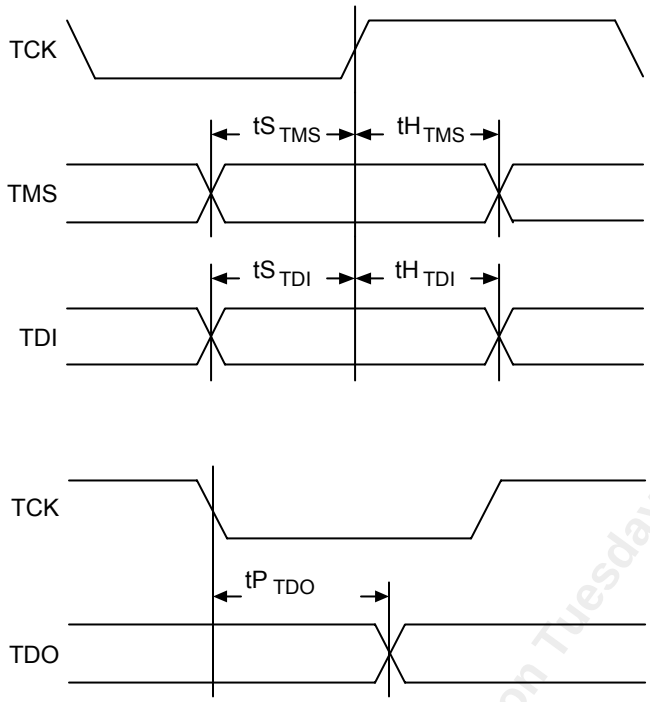
Table 67 - JTAG Port Interface (Figure 68)

Symbol	Description	Min	Max	Units
	TCK Frequency		1	MHz
	TCK Duty Cycle	40	60	%
t_{STMS}	TMS Set-up time to TCK	50		ns
t_{HTMS}	TMS Hold time to TCK	50		ns
t_{STDI}	TDI Set-up time to TCK	50		ns
t_{HTDI}	TDI Hold time to TCK	50		ns
t_{PTDO}	TCK Low to TDO Valid	2	50	ns

Notes

1. Maximum output propagation delays are measured with a 50pF load on the output.

Figure 68 - JTAG Port Interface Timing



18. Ordering and Thermal Information

Table 68 - FREEDM 84A1024 Ordering Information

PART NO.	DESCRIPTION
PM7389	520 Thermally Enhanced Ball Grid Array (TEBGA)

Table 69 - FREEDM 84A1024 Theta Jc

PART NO.	AMBIENT TEMPERATURE	Theta Jc
PM7389	-40°C to +85°C	1 °C/W

Table 70 - FREEDM 84A1024 Junction Temp

PM7389	Maximum Junction Temperature for Long Term Reliability	105 °C

Table 71 - FREEDM 84A1024 Theta Ja vs. Airflow

		Forced Air (Linear Feet per Minute)				
Theta Ja @ 2.6W	Conv	100	200	300	400	500
Dense Board	15.0	12.9	11.5	10.7	10.3	10.2
JEDEC Board	8.4	7.6	7.1	6.8	6.6	6.4

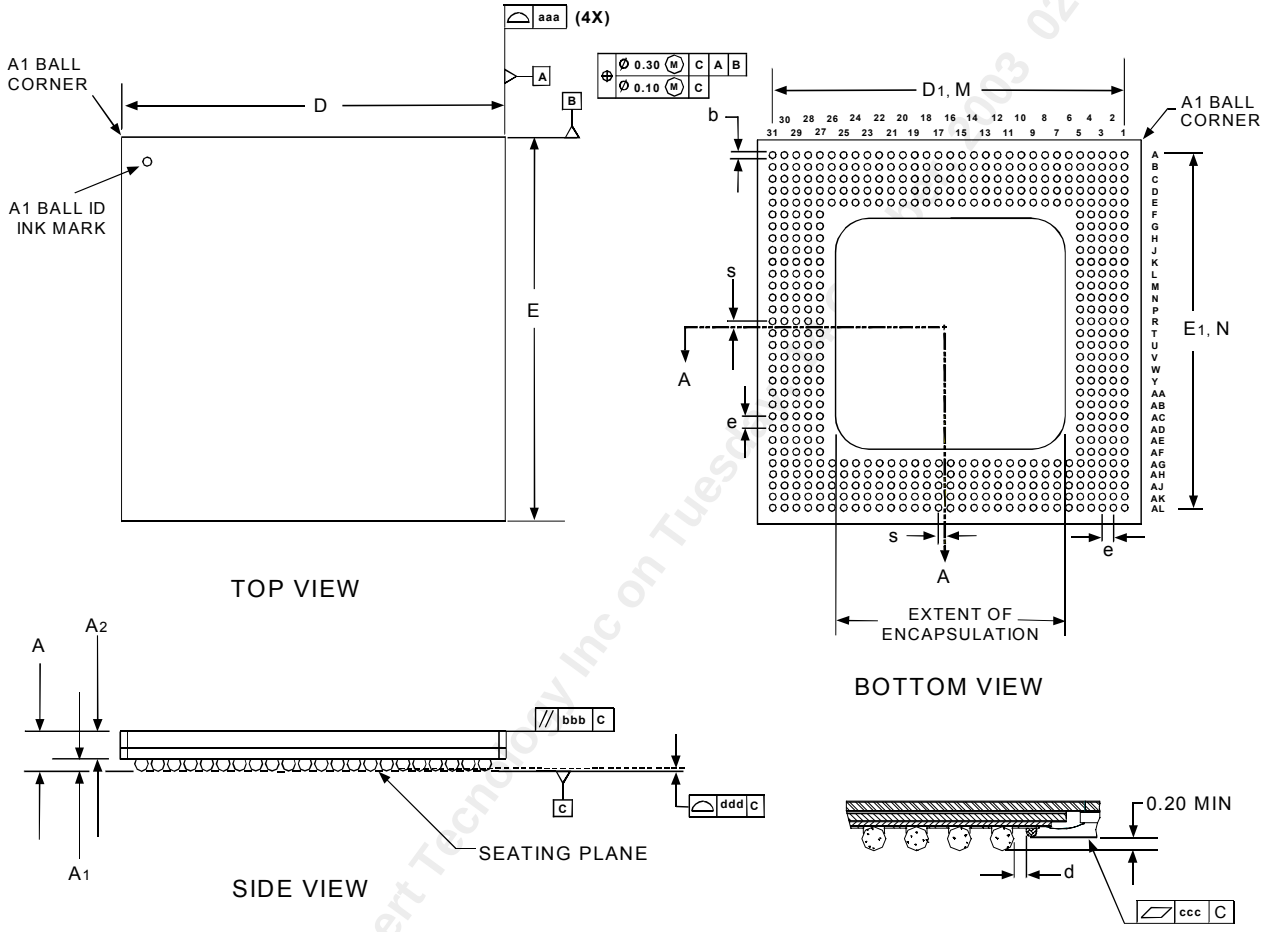
Notes on Theta Ja vs. Airflow

1. Dense Board – Board with 3x3 array of the same device with spacing of 4mm between device. 6 layer board (3 signal layers, 3 power layers). Chart represents device in the center of the array. Chart represents values obtained through simulation.

2. JEDEC Board – Single component on a board. 4 layer board (2 signal layers, 2 power layers), metallization length x width = 94 mm x 94 mm. Board dimension = 114mmx142mm. JEDEC Measurement as per EIA/GESD51

19. 520 PIN TEBGA – 40 x 40 MM BODY

Figure 69 - 520 Pin Enhanced Ball Grid Array (TEBGA)



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ccc DENOTES FLATNESS.
5) DIMENSION ddd DENOTES COPLANARITY.

PACKAGE TYPE : 520 THERMALLY ENHANCED BALL GRID ARRAY - SBGA																
BODY SIZE : 40 x 40 x 1.54 MM																
Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	d	e	aaa	bbb	ccc	ddd	S
Min.	1.30	0.50	0.80	39.90	38.00	39.90	38.00		0.60	0.5	-	-	-	-		-
Nom.	1.51	0.60	0.91	40.00	38.10	40.00	38.10	31x31	0.75	-	1.27	-	-	-		0.00
Max.	1.70	0.70	1.00	40.10	38.20	40.10	38.20		0.90	-	-	0.20	0.25	0.20	0.20	-