RL56CSMV/3 and RL56CSM/3

AnyPort™ Multi-Service Access Processor

Hardware Interface Description

Doc. No. 1137, Rev. 6
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CONEXANT™

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Document Revision Record

Changes Incorporated in Revision 6

1. Figure 1-1: Revised SDRAM box.
2. Table 1-3: Added SDRAM part numbers.
3. Figure 1-1: Revised SDRAM box.
4. Table 3-3: Revised x_SCLK I/O type.
5. Table 3-4: Added Itpu/Ot2 I/O type.
6. Table 3-5: Revised Output Voltage Low and Output Voltage High Test Conditions.
7. Section 3.4: Added.

Changes Incorporated in Revision 5

8. Throughout: Replaced VCC with VDD.
9. Throughout: Replaced VGG5V with VGG.
10. Figure 1-1: Corrected x_SCLK label.
11. Figure 3-1: Corrected RW# label and added CLK label.
12. Section 3.2: Added section headings and reorganized.
13. Table 3-1: Corrected RW# label.
14. Table 3-2: Corrected RW# label.
15. Table 3-3: Corrected MCU_TEST# I/O type to Itpu and corrected RW# label.
16. Table 3-4: Updated C_{IN} from 7 pF to 8pF.
17. Table 3-5: Added new table.
18. Table 3-8: Added power requirements for RL56CSMV/3.
19. Section 3.2.3: Revised thermal characteristics.
20. Section 3.3: Replaced Table 3-10 and Figure 3-3.
21. Table 3-11: Added notes.
22. Table 4-2: Added notes.
23. Table 3-3: Added notes.
24. Table 3-6: Revised.
25. Table 3-9: Replaced VDD in Limits with VGG, revised maximum Supply Voltage to 4.0 V, added Latch-up Current @ 125 °C.
26. Table 3-10: Revised.
27. Figure 3-3: Revised.
28. Section 3.2.3: Revised NOTES.
29. Table 4-2: Corrected t_{CS} Symbol.
30. Figure 4-3: Revised.
31. Figure 4-4: Revised.
32. Table 5-1: Revised.
33. Table 5-2: Revised.

Changes Incorporated in Revision 4

1. Added RL56CSMV/3 Voice enabled part to the AnyPort family.
2. Added Table 3-10, SDRAM Interface Timing and Figure 3-3. SDRAM Interface Timing
3. Added Figure 3-5, Oscillator Waveform Requirements.
4. Updated and corrected Figure 3-1, RL56CSMV/3 Hardware Interface Signals.
5. Renamed Channel Signal Names to match Logical Channels, as follows:

Old "A_name" changed to "C_name", old "B_name" changed to "A_name", old "C_name" changed to "B_name".

NOTE: This is a Signal Name change only. There is no functional change to device operation.

Ball	Old Name	New Name	Ball	Old Name	New Name	Ball	Old Name	New Name
AC26	A_SCLK	C_SCLK	G26	B_SCLK	A_SCLK	F01	C_SCLK	B_SCLK
AB25	A_FSYNC	C_FSYNC	H26	B_FSYNC	A_FSYNC	E01	C_FSYNC	B_FSYNC
AD25	A_RXDATA	C_RXDATA	K26	B_RXDATA	A_RXDATA	C01	C_RXDATA	B_RXDATA
AC25	A_TXDATA	C_TXDATA	L26	B_TXDATA	A_TXDATA	B01	C_TXDATA	B_TXDATA
V26	A_PLLVDD	C_PLLVDD	C16	B_PLLVDD	A_PLLVDD	G03	C_PLLVDD	B_PLLVDD
AD16	A_PLLGND	C_PLLGND	N25	B_PLLGND	A_PLLGND	C09	C_PLLGND	B_PLLGND
P26	A_EYEXY	C_EYEXY	A19	B_EYEXY	A_EYEXY	L03	C_EYEXY	B_EYEXY
AA25	A_EYESYNC	C_EYESYNC	F26	B_EYESYNC	A_EYESYNC	G01	C_EYESYNC	B_EYESYNC
Y24	A_EYECLK#	C_EYECLK#	E26	B_EYECLK#	A_EYECLK#	H01	C_EYECLK#	B_EYECLK#
U25	A_TSAEN#	C_TSAEN#	A23	B_TSAEN#	A_TSAEN#	J02	C_TSAEN#	B_TSAEN#
R26	A_XCLK	C_XCLK	A20	B_XCLK	A_XCLK	C07	C_XCLK	B_XCLK
R25	A_YCLK	C_YCLK	A21	B_YCLK	A_YCLK	C06	C_YCLK	B_YCLK

6. Updated Table 1-2, Logical Channel vs. Physical Channel.
7. Added Table 3-4, I/O Type Descriptions.
8. Updated Table 3-5, Digital Electrical Characteristics.
9. Updated Section 5.1.6, Clock Oscillator Circuit.

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1. INTRODUCTION

1.1 SUMMARY

The RL56CSMV/3 and RL56CSM/3 are members of the CONEXANT™ AnyPort™ family of multi-service access processors, and provide a complete solution to the transport of multiple media types between circuit-switched remote access and a variety of back-end networks. AnyPort processors are ideally suited for the network infrastructures resulting from the convergence of voice and data networking, addressing new requirements such as Voice and Fax over packet networks, ISDN and Cellular Data, while maintaining support of traditional PSTN Data/Fax needs.

Note: In this document, RL56CSMV/3 and CSMV/3 refer to both RL56CSMV/3 and RL56CSM/3 except as noted. Any reference to voice applies only to the RL56CSMV/3.

The CSMV/3 transcends existing modem solutions by providing a complete system solution for multi-service remote access. The combined DSP/RISC architecture provides an ideal engine to run CONEXANT's extensive suite of field-proven modulations, echo cancellers, voice coders, and communications protocols. In addition, performing functions such as T.38, V.120, async to sync HDLC conversion for PPP, V.110, and synchronous HDLC for PPP on ISDN connections, in the access processor allows system designers to reduce system overhead and increase scalability.

The CSMV/3 is a low-power system providing three communication channels in a single package. Powerful and downloadable DSP-based data pumps employ on-chip SRAM to allow upgrades to future voice and communication modulation schemes. An advanced RISC microcontroller manages three data pumps simultaneously. An innovative host interface to the Multi-Service Access Processor system uses a shared SDRAM memory to increase data throughput while reducing system cost and space. A programmable time slot selection feature provides direct digital connection to a T1/E1/PRI framing device.

A 35mm BGA package houses the CSMV/3 with extra balls available for thermal vias to minimize heat. A built-in phase lock loop (PLL) minimizes board noise while easing design. A quick-wake, sleep mode further reduces the power of this +3.3V access processor system.

This Hardware Interface Description describes the modem hardware capabilities. AT commands and S registers are defined in the AT Command Reference Manual (Order No. 1195). Additional information is described in the Software Interface Description (Order No. 1148) and the RL56DDP Modem Designer's Guide (Order No. 1141).

Table 1-1. RL56CSMV/3 and RL56CSM/3 Models and Functions

Model/Order/Part Numbers		Supported Functions		
Marketing Model Number	Part Number (340-Pin BGA)	Data	Fax	Voice
RL56CSM/3	R7138-94	Yes	Yes	No
RL56CSMV/3	R7178-24	Yes	Yes	Yes

1.2 FEATURES

Generic

- Three access channels in one package
- +3.3V operation with +5V tolerant inputs
- Downloadable controller firmware and data pump code
- Advanced RISC Machines (ARM) architecture
- Low-power sleep mode with quick wake
- Glueless interface to Bt8370 T1/E1/PRI framer with time slot selection
- Built-in phase lock loop (PLL)

Signaling

- DTMF detection and generation
- Multi frequency tone support for legacy network equipment (R1 and R2)

Data

- Data modem modes
  - PSTN: ITU-T V.90, K56flex, K56Plus, V.34 (33.6 kbps), V.FC, V.32 bis, V.32, V.22 bis, V.22A/B, V.23, and V.21; Bell 212A and 103
  - ISDN: 64/56 kbps ISDN Basic Rate Interface B Channel HDLC control, or data pass-through mode for HDLC processing elsewhere in the central site system
- Internal error correction and data compression (ECC)
  - V.42 LAPM, MNP 2-4, and MNP 10EC
  - V.42 bis and MNP 5 data compression
- Async/sync HDLC conversion
- V.120 ISDN data
- V.110 cellular data
- LAP-B X.75

Voice (RL56CSMV/3 only)

- Baseline configuration:
  - G.723.1 and G.723.1 Annex A
  - G.711 μ-law and A-law
  - G.729 Annex A and Annex B
  - G.168 128 ms Network Echo Canceller
- Patented robust jitter buffer
- Voice API using Mailbox Messages

FAX

- Fax modem send and receive rates up to 14400 bps
- V.17, V.33, V.29, V.27 ter, and V.21 channel 2
- Group 3, T.30 protocol and Class 1, 2 supported
- T.38 real-time fax protocol

Communications software-compatible AT command set

1.3 TECHNICAL OVERVIEW

1.3.1 General Description

The CSMV/3 provides the processing core for three channels of a central site Remote Access Server supporting high speed T1/E1/PRI digital lines. The OEM adds two oscillators, SDRAM, and discrete components to complete the Multi-Service Access Processor system.

The access processor includes a full-featured, self-contained data/fax/Voice modem solution shown in Figure 1-1. Data modem handshake, fax modem protocol, voice codecs, and ISDN data connection functions are supported and controlled through the AT command set.

1.3.2 Digital Data Pump (DDP)

The DDP is a +3.3V CONEXANT data pump supporting PSTN data/fax modem operation, ISDN B Channel call termination mode, and voice coding/decoding. The DDP executes internal code including downloadable modules from on-chip memory.

Digital data transfers serially between the T1/E1 framer device and the DDP at a data rate up to 8.192 Mbps. The T1/E1 framing device provides a strobe signal and the DDP TSA logic detects where the data for the channel starts in the serial TDM data stream using a programmable counter. The DDP performs PCM µ-law or A-law conversion and synchronizes with an external network clock.

1.3.3 ARM Microcontroller (MCU)

The ARM MCU performs the command processing and interfaces to the central site system controller via a 16-bit parallel host interface. Two 64-word deep FIFOs are used for improved data throughput between the access processor and system controller. This single powerful RISC processor controls three separate channels. A SDRAM loader is available to support download from the central site system controller on startup, if desired.

1.3.4 Access Processor Operation

In data modem modes, each channel can independently connect to PSTN data modems at rates up to 56 kbps or ISDN terminal adapters at rates up to 64 kbps. A downloadable architecture allows for software download. For PSTN modems, complete handshake and data rate negotiations are performed. By optimizing the modem configuration for line conditions, the DDP can connect at the highest data rate that the channel can support from 56 kbps to 300 bps with automatic fallback. Automode operation in V.34 is provided in accordance with PN3320 and in V.32 bis in accordance with PN2330. All tone and pattern detection functions required by the applicable ITU or Bell standard are supported. Asynchronous to synchronous conversion is supported inside the controller to ease PPP processing in PSTN data mode.

When the remote end is an ISDN terminal adapter, the CSMV/3 provides HDLC control including HDLC Flag generation/detection, bit stuffing/extraction, and CRC generation/checking. V.120, V.110, and LAP-B X.75 are also supported. V.120 is a standard for encapsulating asynchronous data communications traffic into ISDN data streams.

In fax modem mode, the CSMV/3 supports Group 3 facsimile send and receive speeds of 14400, 12000, 9600, 7200, 4800, and 2400 bps. Fax modem modes support T.30 fax requirements. Fax data transmission and reception performed by the access processor are controlled and monitored through the EIA-578 Class 1 and Class 2 command interface. Both transmit and receive fax data are buffered within the access processor.

In Voice mode, the CSMV/3 encodes PCM audio data from the line into Real-Time Protocol (RTP) packets for the Host, and decodes RTP packets from the Host, to output PCM audio data to the line. In Voice mode, DTMF digits can be detected and transmitted, and a Voice Activity Detector can be enabled.

1.3.5 Access Processor Firmware

Access processor firmware performs processing of general modem control, command sets, error correction and data compression, fax class 1 and class 2, voice coding and decoding (optional), and central site system controller interface functions.

The firmware is provided in object code form for executing from external SDRAM after download on startup using the ROM-coded Boot Loader. Equipment designers can add their own functions in firmware using commonly available development tools and the C programming language.

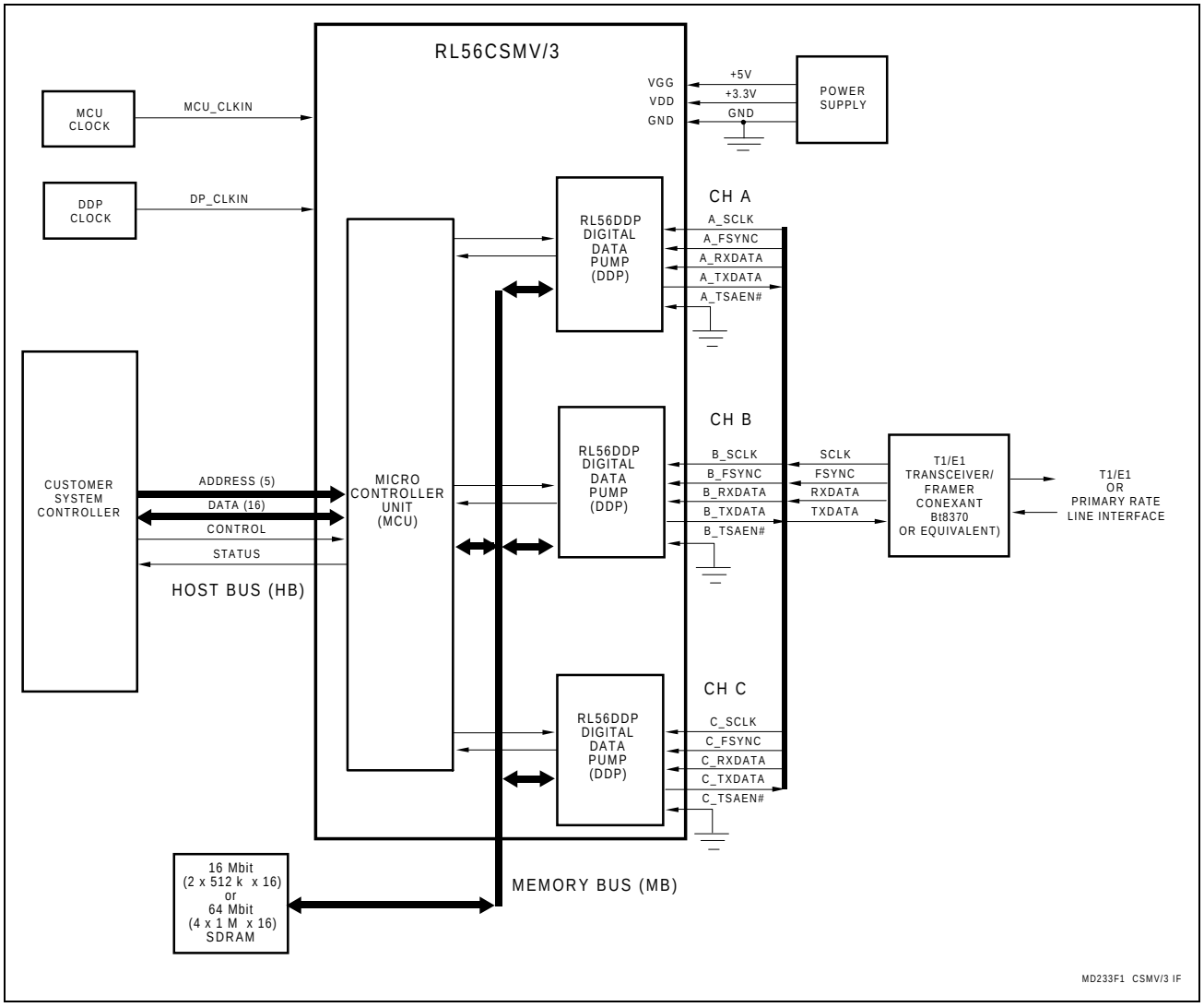

Figure 1-1. System Implementation Example Block Diagram

Note: Table 1-2 shows the DDP (physical) channel corresponding to the logical channel number programmed in the mailbox messages. The logical channel corresponds to the physical channel as follows: 0 = A, 1 = B, and 2 = C.

Table 1-2. Logical Channel vs. Physical Channel

Logical Channel	Corresponding Physical Channel
Logical Channel 0	Physical Channel A
Logical Channel 1	Physical Channel B
Logical Channel 2	Physical Channel C

1.3.6 Supported Interfaces

Parallel Host Bus Interface

The interface signals are: 16 bidirectional data lines (HBD0-HBD15), five address input lines (HBA1-HBA5), and six control lines (HBCS#, HBRD#, HBWR#, HBEN#, HBACKR#, and HBACKW#). Refer to the Software Interface Description (Order No. 1148) for FIFO and Mailbox description.

T1/E1 Transceiver Interface

The 4-line interface to the OEM-supplied T1/E1 Transceiver consists of the SCLK, FSYNC, and RXDATA inputs and the TXDATA output. The T1/E1 Transceiver interface timing is described in Section 3.2.3.

SDRAM Interface

The CSMV/3 provides address, data, and control lines to connect to a 16 Mbit (2 x 512 k x 16) or 64 Mbit (4 x 1 M x 16) Synchronous Dynamic RAM (SDRAM) meeting the Intel PC100 Specification. Typical SDRAMs that meet CSMV/3 requirements are listed in Table 1-3.

Table 1-3. Typical SDRAMs

Manufacturer	Part Number
16-Mbit SDRAMs	
NEC	UPD4516161AG5-A80 UPD4516161AG5-A10 UPD4516161AG5-A10B
Hyundai	HY57V161610CTC-8 HY57V161610CTC-10P HY57V161610CTC-10S
Fujitsu	MB81F161622B -60 MB81F161622B-70 MB81F161622B-80
Micron	MT48LC1M16A1-TG-7SE
64-Mbit SDRAMs	
NEC	UPD4564163G5-A10-9JF
Mitsubishi	M2V64S40BTP

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2. TECHNICAL SPECIFICATIONS

2.1 ESTABLISHING DATA MODEM CONNECTIONS

In a typical application, the “system controller” processes all aspects of PSTN connection call setup, including off-hook signaling, sending dial digits, call progress detection, and ring detection for both T1/E1 lines and ISDN D-Channel control.

After a PSTN connection is established by the system controller, the system controller issues the ATA command to the CSMV/3 to start the Answer Handshake Sequence, or the ATD command to start the Originate Handshake Sequence.

Modem Handshaking Protocol

If a handshake is not completed within the time specified in the S7 register after the ATD or ATA command is issued, the modem aborts the handshake attempt.

Answer Tone Detection

Answer tone can be detected over the frequency range of 2100 ± 40 Hz in ITU-T modes and 2225 ± 40 Hz in Bell modes.

Billing Protection

When the modem goes off-hook to answer an incoming call, both transmission and reception of data are prevented for 2 seconds (data modem) or 4 seconds (fax adaptive answer) to comply with the billing delay requirement.

Connection Speeds and CODEC Selection

The modem functions as a data modem when the +FCLASS=0 command is active.

Line connection can be selected using the +MS command in accordance with the draft PN-3320 standard presented to the TR30-4 committee (which is a candidate for the definition of V.25 ter at the ITU). The +MS command selects modulation, enables/disables automode, selects minimum and maximum line speeds, and selects μ-Law or A-Law codec.

The +MS command is described in the AT Command Reference Manual (Order No. 1195).

Multi-frequency (MF) Tone Generation and Detection

Multi-frequency (MF) tone generation and detection is supported by the +VTS, +CTD, +PTF, and +QTR commands.

The +VTS, +CTD, +PTF, and +QTR commands are described in the AT Command Reference Manual (Order No. 1195).

2.2 DATA MODE

Data mode exists when a connection has been established between modems and all handshaking has been completed.

Speed Buffering (Normal Mode)

Speed buffering allows a DTE to send data to, and receive data from, a modem at a speed different than the line speed. The modem supports speed buffering at all line speeds.

Flow Control

DTE-to-Modem Flow Control. Refer to the Software Interface Description (Order No. 1148).

Escape Sequence Detection

The “+++” escape sequence can be used to return control to the command mode from the data mode. Escape sequence detection is disabled by an S2 register value greater than 127, (or use &D2 and DTR drop - see S25 register, AT Command Reference Manual, Order No. 1195). Refer to the Software Interface Description (Order No. 1148).

BREAK Generation and Detection

Refer to the Software Interface Description (Order No. 1148).

Telephone Line Monitoring

GSTN Cleardown (V.90, K56flex, V.34, V.32 bis, V.32). Upon receiving GSTN Cleardown from the remote modem in a non-error correcting mode, the modem cleanly terminates the call.

Fall Forward/Fallback (V.34/V.32 bis/V.32)

During initial handshake, the modem will fallback to the optimal line connection within V.34/V.32 bis/V.32 mode depending upon signal quality if automode is enabled by the +MS or N1 command.

When connected in V.34/V.32 bis/V.32 mode, the modem will fall forward or fallback to the optimal line speed within the current modulation depending upon signal quality if fall forward/fallback is enabled by the %E2 command.

Retrain

The modem may lose synchronization with the received line signal under poor line conditions. If this occurs, retraining may be initiated to attempt recovery depending on the type of connection.

The modem initiates a retrain if line quality becomes unacceptable if enabled by the %E command. The modem continues to retrain until an acceptable connection is achieved, or until 30 seconds elapse resulting in line disconnect.

Programmable Inactivity Timer

The modem disconnects from the line if data is not sent or received for a specified length of time. In normal or error-correction mode, this inactivity timer is reset when data is received from either the DTE or from the line. This timer can be set to a value between 0 and 2550 seconds by using register S30. A value of 0 disables the inactivity timer.

2.3 ERROR CORRECTION AND DATA COMPRESSION

V.42 Error Correction

V.42 supports two methods of error correction: LAPM and, as a fallback, MNP 4. The modem provides a detection and negotiation technique for determining and establishing the best method of error correction between two modems.

MNP 2-4 Error Correction

MNP 2-4 is a data link protocol that uses error correction algorithms to ensure data integrity. Supporting stream mode, the modem sends data frames in varying lengths depending on the amount of time between characters coming from the DTE.

V.42 bis Data Compression

V.42 bis data compression mode, enabled by the %Cn command or S46 register, operates when a LAPM or MNP 10EC connection is established.

The V.42 bis data compression employs a “string learning” algorithm in which a string of characters from the DTE is encoded as a fixed length codeword. Two 2k-byte dictionaries are used to store the strings. These dictionaries are dynamically updated during normal operation.

MNP 5 Data Compression

MNP 5 data compression mode, enabled by the %Cn command, operates during an MNP connection.

In MNP 5, the modem increases its throughput by compressing data into tokens before transmitting it to the remote modem, and by decompressing encoded received data before sending it to the DTE.

2.4 FAX OPERATION

Facsimile functions operate in response to fax class 1 commands when +FCLASS=1 or in response to fax class 2 commands when +FCLASS=2.

In the fax mode, the on-line behavior of the modem is different from the data (non-fax) mode. After dialing, modem operation is controlled by fax commands. Other AT commands are still valid but may operate differently than in data modem mode.

Calling tone is generated in accordance with T.30.

2.5 DIAGNOSTICS

2.5.1 Commanded Tests

Diagnostics are performed in response to &T commands, per V.54.

Remote Digital Loopback (RDL) (&T6 Command). Data from the local DTE is sent to the remote modem which loops the data back to the local DTE.

Remote Digital Loopback with Self Test (&T7 Command). An internally generated pattern is sent from the local modem to the remote modem, which loops the data back to the local modem.

Local Digital Loopback (&T3 Command). When local digital loop is requested by the local DTE, two data paths are set up in the local modem. Data from the local DTE is looped back to the local DTE (path 1) and data received from the remote modem is looped back to the remote modem (path 2).

2.5.2 DDP Test

Following an SDRAM download, the ROM-coded Boot Loader jumps to the starting address of the MCU firmware, and the MCU firmware will try to configure the DDPs. If any DDP does not configure correctly, that channel is reported as "down", and AT commands that require access to the DDP (e.g., ATD, ATA, ATH, or ATZ) will respond with ERROR.

2.6 LOW POWER SLEEP MODE

Sleep Mode Entry. The DDPs enter the low power sleep mode when no line connection exists and no datapump activity occurs for the period of time specified in the S24 register. All DDP circuits are turned off in order to consume reduced power while being able to immediately wake up and resume normal operation.

Wake-up. When the Host requests a channel to be active, the MCU will wake-up the datapump for that channel. The wake-up process is transparent to the host.

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3. HARDWARE INTERFACE

3.1 HARDWARE SIGNALS

The RL56CSMV/3 interface is illustrated in Figure 3-1.

The RL56CSMV/3 BGA pin (ball) locations are shown in Figure 3-2.

The RL56CSMV/3 pin signals by pin location are listed in Table 3-1.

The RL56CSMV/3 pin signals by interface are listed in Table 3-2.

The RL56CSMV/3 hardware interface signals are defined in Table 3-3.

Hardware interface signal I/O types are described in Table 3-4.

Digital electrical characteristics for the hardware interface signals are listed in Table 3-5.

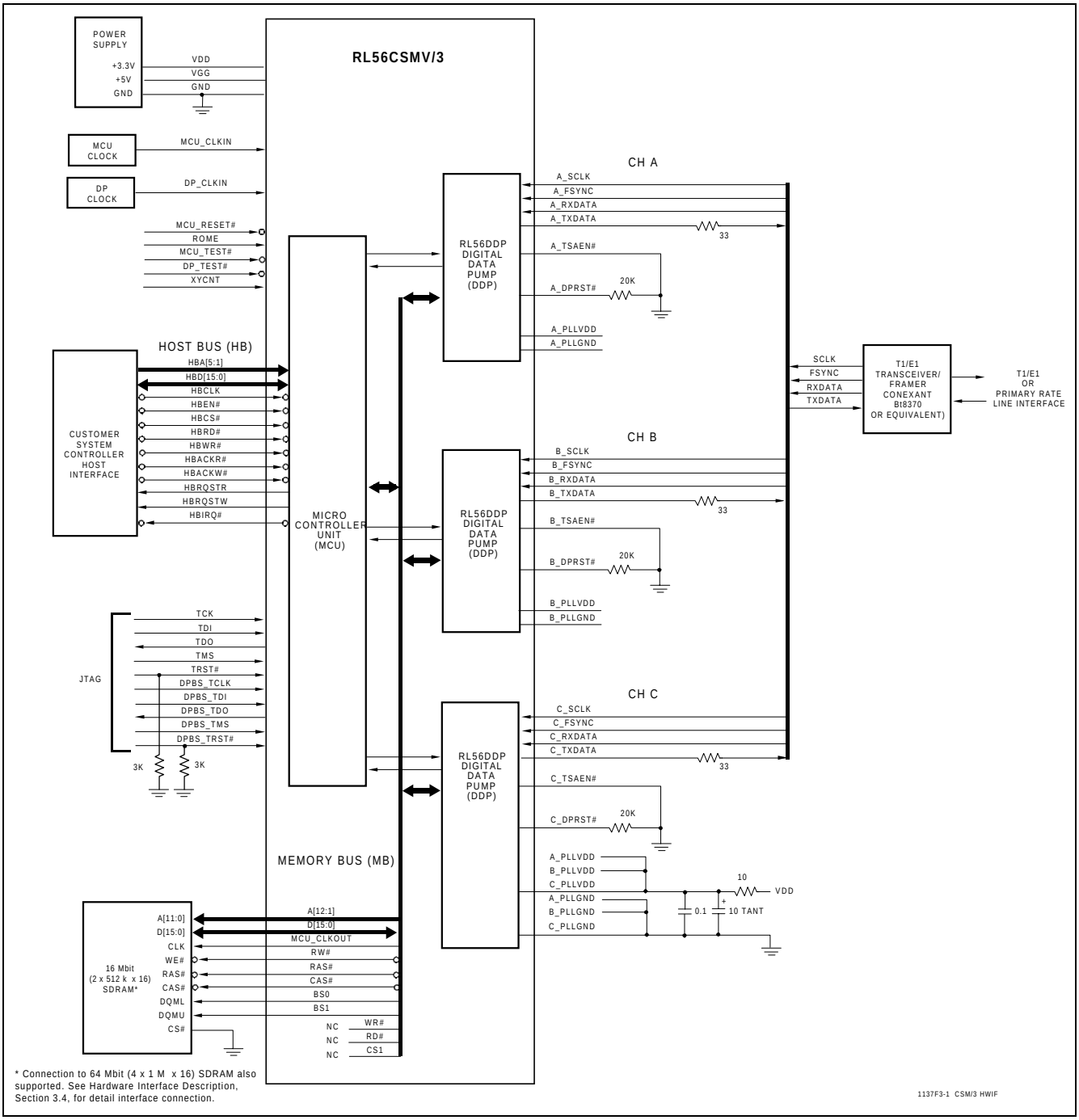

Figure 3-1. RL56CSMV/3 Hardware Interface Signals

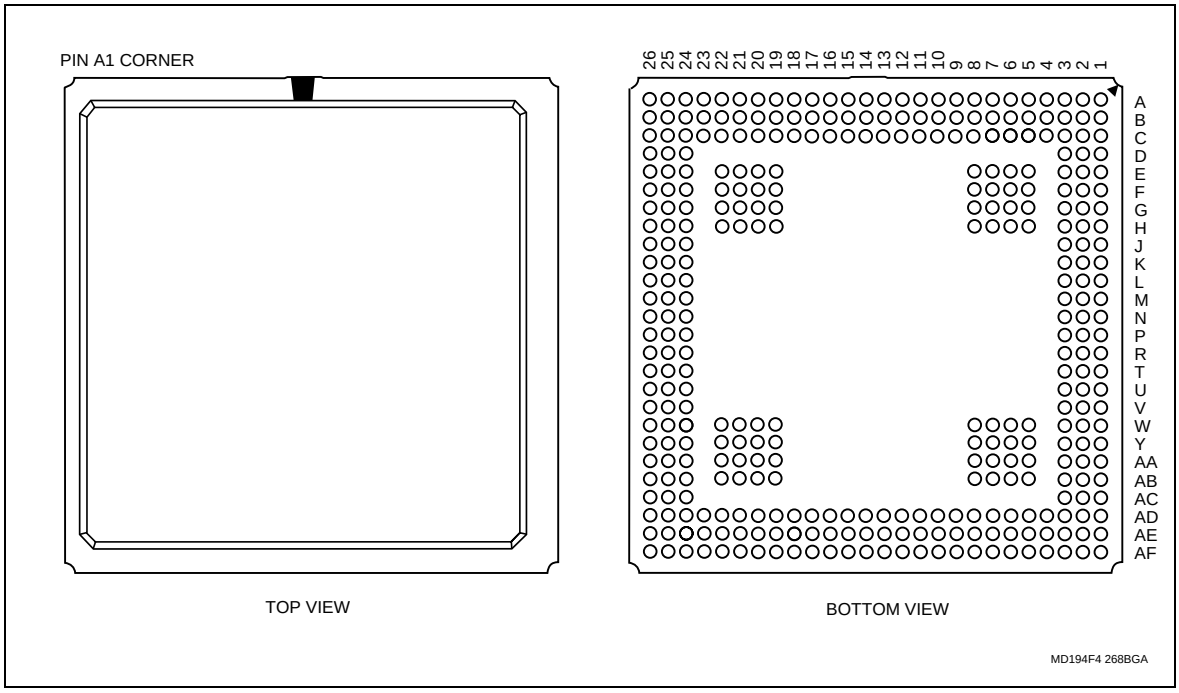

Figure 3-2. RL56CSMV/3 340-Pin BGA Package

Table 3-1. RL56CSMV/3 Pin Signals by Pin Location

Table Col.	1			2			3			4		
Table Row	Loc.	Signal	I/F	Loc.	Signal	I/F	Loc.	Signal	I/F	Loc.	Signal	I/F
1	A01	C_DPRST#	GND thru 20K	B25	B_DPRXCLK	TEST	F03	VDD	3.3V	K25	A_DPTXCLK	TEST
2	A02	A_DPRST#	GND thru 20K	B26	RESERVED		F05	RESERVED		K26	A_RXDATA	CH A
3	A03	B_DPRST#	GND thru 20K	C01	B_RXDATA	CH B	F06	GND	GND	L01	D9	MB
4	A04	VGG	5V	C02	RESERVED		F07	GND	GND	L02	D8	MB
5	A05	B_DPCS	TEST	C03	RESERVED		F08	GND	GND	L03	B_EYEXY	CH B
6	A06	A4	MB	C04	RESERVED		F19	GND	GND	L24	XYCNT	TEST
7	A07	A3	MB	C05	VDD	3.3V	F20	GND	GND	L25	RESERVED	
8	A08	A2	MB	C06	B_YCLK	CH B	F21	GND	GND	L26	A_TXDATA	CH A
9	A09	A1	MB	C07	B_XCLK	CH B	F22	RESERVED		M01	D12	MB
10	A10	A0	MB	C08	B_DSPRST	TEST	F24	DP_TEST#	TEST	M02	D11	MB
11	A11	D7	MB	C09	B_PLLGND	CH B	F25	RESERVED		M03	D10	MB
12	A12	D6	MB	C10	RESERVED		F26	A_EYESYNC	CH A	M24	VDD	3.3V
13	A13	D5	MB	C11	DPBS_TRST#	JTAG	G01	B_EYESYNC	CH B	M25	A_DPCS	TEST
14	A14	D0	MB	C12	VDD	3.3V	G02	RESERVED		M26	A_DSPRST	TEST
15	A15	DP_CLKIN	SYS	C13	B_DPINT	TEST	G03	B_PLLVDD	CH B	N01	D15	MB
16	A16	RESERVED		C14	RESERVED		G05	RESERVED		N02	D14	MB
17	A17	A_DPINT	TEST	C15	VDD	3.3V	G06	GND	GND	N03	D13	MB
18	A18	A_DSPINT	TEST	C16	A_PLLVDD	CH A	G07	GND	GND	N24	WR#	MB
19	A19	A_EYEXY	CH A	C17	RESERVED		G08	GND	GND	N25	A_PLLGND	CH A
20	A20	A_XCLK	CH A	C18	RESERVED		G19	GND	GND	N26	DPBS_TCLK	JTAG
21	A21	A_YCLK	CH A	C19	RESERVED		G20	GND	GND	P01	CAS#	MB
22	A22	RESERVED		C20	RESERVED		G21	GND	GND	P02	RAS#	MB
23	A23	A_TSAEN#	CH A	C21	RESERVED		G22	RESERVED		P03	MCU_CLKIN	SYS
24	A24	RESERVED		C22	RESERVED		G24	RESERVED		P24	C_DSPINT	TEST
25	A25	RESERVED		C23	A_DPTXD	TEST	G25	RESERVED		P25	RD#	MB
26	A26	RESERVED		C24	VDD	3.3V	G26	A_SCLK	CH A	P26	C_EYEXY	CH C
27	B01	B_TXDATA	CH B	C25	RESERVED		H01	B_EYECLK#	CH B	R01	PA5	NA
28	B02	RESERVED		C26	RESERVED		H02	RESERVED		R02	RESERVED	
29	B03	RESERVED		D01	RESERVED		H03	B_DSPINT	TEST	R03	MCU_CLKOUT	MB
30	B04	RESERVED		D02	RESERVED		H05	RESERVED		R24	C_DPTXCLK	TEST
31	B05	RESERVED		D03	RESERVED		H06	GND	GND	R25	C_YCLK	CH C
32	B06	RESERVED		D24	VDD	3.3V	H07	GND	GND	R26	C_XCLK	CH C
33	B07	C_DPEXRST	TEST	D25	A21	MB	H08	GND	GND	T01	PA3	NA
34	B08	A_DPEXRST	TEST	D26	RESERVED		H19	GND	GND	T02	PE4	NA
35	B09	B_DPEXRST	TEST	E01	B_FSYNC	CH B	H20	GND	GND	T03	VDD	3.3V
36	B10	D4	MB	E02	RESERVED		H21	GND	GND	T24	C_DPINT	TEST
37	B11	D3	MB	E03	RESERVED		H22	RESERVED		T25	VDD	3.3V
38	B12	D2	MB	E05	RESERVED		H24	VDD	3.3V	T26	VDD	3.3V
39	B13	D1	MB	E06	RESERVED		H25	RESERVED		U01	PA7	NA
40	B14	C_DPRXD	TEST	E07	RESERVED		H26	A_FSYNC	CH A	U02	PE0	NA
41	B15	RESERVED		E08	RESERVED		J01	RESERVED		U03	VDD	3.3V
42	B16	RESERVED		E19	RESERVED		J02	B_TSAEN#	CH B	U24	VGG	5V
43	B17	RESERVED		E20	RESERVED		J03	VDD	3.3V	U25	C_TSAEN#	CH C
44	B18	A_DPRXD	TEST	E21	RESERVED		J24	RESERVED		U26	RESERVED	
45	B19	RESERVED		E22	RESERVED		J25	RESERVED		V01	PE6	NA
46	B20	RESERVED		E24	RESERVED		J26	RESERVED		V02	PE2	NA
47	B21	RESERVED		E25	RESERVED		K01	BS1	MB	V03	RESERVED	
48	B22	B_DPRXD	TEST	E26	A_EYECLK#	CH A	K02	DPBS_TDO	JTAG	V24	C_DPRXCLK	TEST
49	B23	B_DPTXD	TEST	F01	B_SCLK	CH B	K03	VDD	3.3V	V25	C_DPTXD	TEST
50	B24	B_DPTXCLK	TEST	F02	RESERVED		K24	A_DPRXCLK	TEST	V26	C_PLLVDD	CH C

Notes: RESERVED = May have internal circuit connected, no external connection allowed.

Table 3-1. RL56CSMV/3 Pin Signals by Pin Location (Cont'd)

Table Col.	5			6			7			8		
Table Row	Loc.	Signal	I/F	Loc.	Signal	I/F	Loc.	Signal	I/F	Loc.	Signal	I/F
1	W01	PA4	NA	AB20	RESERVED		AE13	HBA1	HB			
2	W02	PA6	NA	AB21	RESERVED		AE14	HBCS#	HB			
3	W03	VDD	3.3V	AB22	RESERVED		AE15	HBWR#	HB			
4	W05	GND	GND	AB24	RESERVED		AE16	HBCLK	HB			
5	W06	GND	GND	AB25	C_FSYNC	CH C	AE17	HBEN#	HB			
6	W07	GND	GND	AB26	CS3	MB	AE18	A5	MB			
7	W08	GND	GND	AC01	TRST#	JTAG	AE19	A7	MB			
8	W19	GND	GND	AC02	PF3	NA	AE20	A9	MB			
9	W20	GND	GND	AC03	VDD	3.3V	AE21	A13	MB			
10	W21	GND	GND	AC24	CS0	MB	AE22	VDD	3.3V			
11	W22	RESERVED		AC25	C_TXDATA	CH C	AE23	RESERVED				
12	W24	MCU_RESET#	SYS	AC26	C_SCLK	CH C	AE24	A14	MB			
13	W25	ROME	SYS	AD01	PF7	NA	AE25	A22	MB			
14	W26	BS0	MB	AD02	TMS	JTAG	AE26	A24	MB			
15	Y01	PE1	NA	AD03	VDD	3.3V	AF01	PF4	NA			
16	Y02	PE3	NA	AD04	VDD	3.3V	AF02	PF6	NA			
17	Y03	VDD	3.3V	AD05	VDD	3.3V	AF03	TDI	JTAG			
18	Y05	GND	GND	AD06	VDD	3.3V	AF04	HBACKR#	HB			
19	Y06	GND	GND	AD07	VDD	3.3V	AF05	HBACKW#	HB			
20	Y07	GND	GND	AD08	VDD	3.3V	AF06	HBD0	HB			
21	Y08	GND	GND	AD09	VDD	3.3V	AF07	HBD2	HB			
22	Y19	GND	GND	AD10	VDD	3.3V	AF08	HBD3	HB			
23	Y20	GND	GND	AD11	VDD	3.3V	AF09	HBD10	HB			
24	Y21	GND	GND	AD12	HBD14	HB	AF10	HBD8	HB			
25	Y22	RESERVED		AD13	HBA2	HB	AF11	HBD5	HB			
26	Y24	C_EYECLK#	CH C	AD14	HBA5	HB	AF12	HBD13	HB			
27	Y25	MCU_TEST#	SYS	AD15	DPBS_TDI	JTAG	AF13	HBD11	HB			
28	Y26	CS4	MB	AD16	C_PLLGND	CH C	AF14	HBA3	HB			
29	AA01	PE5	NA	AD17	C_DSPRST	TEST	AF15	HBA4	HB			
30	AA02	PE7	NA	AD18	A12	MB	AF16	HBRD#	HB			
31	AA03	VDD	3.3V	AD19	C_DPCS	TEST	AF17	RESERVED				
32	AA05	GND	GND	AD20	A11	MB	AF18	HBIRQ#	HB			
33	AA06	GND	GND	AD21	A16	MB	AF19	A6	MB			
34	AA07	GND	GND	AD22	A15	MB	AF20	DPBS_TMS	JTAG			
35	AA08	GND	GND	AD23	A20	MB	AF21	A8	MB			
36	AA19	GND	GND	AD24	RW#	MB	AF22	A10	MB			
37	AA20	GND	GND	AD25	C_RXDATA	CH C	AF23	A17	MB			
38	AA21	GND	GND	AD26	CS1	MB	AF24	A19	MB			
39	AA22	RESERVED		AE01	PF5	NA	AF25	A18	MB			
40	AA24	VGG	5V	AE02	TDO	JTAG	AF26	A23	MB			
41	AA25	C_EYESYNC	CH C	AE03	TCK	JTAG						
42	AA26	CS2	MB	AE04	HBRQSTR	HB						
43	AB01	PF0	NA	AE05	HBRQSTW	HB						
44	AB02	PF2	NA	AE06	HBD1	HB						
45	AB03	PF1	NA	AE07	HBD9	HB						
46	AB05	GND	GND	AE08	HBD4	HB						
47	AB06	GND	GND	AE09	HBD6	HB						
48	AB07	GND	GND	AE10	HBD7	HB						
49	AB08	GND	GND	AE11	HBD12	HB						
50	AB19	RESERVED		AE12	HBD15	HB						

Notes: RESERVED = May have internal circuit connected, no external connection allowed.

Table 3-2. RL56CSMV/3 Pin Signals by Interface

Table Col.	1			2			3			4		
Table Row	Loc.	Signal	I/F	Loc.	Signal	I/F	Loc.	Signal	I/F	Loc.	Signal	I/F
1	AE13	HBA1	HB	G01	B_EYESYNC	CH B	L02	D8	MB	K25	A_DPTXCLK	TEST
2	AD13	HBA2	HB	H01	B_EYECLK#	CH B	L01	D9	MB	C23	A_DPTXD	TEST
3	AF14	HBA3	HB	J02	B_TSAEN#	CH B	M03	D10	MB	A18	A_DSPINT	TEST
4	AF15	HBA4	HB	C07	B_XCLK	CH B	M02	D11	MB	M26	A_DSPRST	TEST
5	AD14	HBA5	HB	C06	B_YCLK	CH B	M01	D12	MB	A05	B_DPCS	TEST
6	AF06	HBD0	HB	AC26	C_SCLK	CH C	N03	D13	MB	B09	B_DPEXRST	TEST
7	AE06	HBD1	HB	AB25	C_FSYNC	CH C	N02	D14	MB	C13	B_DPINT	TEST
8	AF07	HBD2	HB	AD25	C_RXDATA	CH C	N01	D15	MB	B25	B_DPRXCLK	TEST
9	AF08	HBD3	HB	AC25	C_TXDATA	CH C	W26	BS0	MB	B22	B_DPRXD	TEST
10	AE08	HBD4	HB	V26	C_PLLVDD	CH C	K01	BS1	MB	B24	B_DPTXCLK	TEST
11	AF11	HBD5	HB	AD16	C_PLLGND	CH C	AC24	CS0	MB	B23	B_DPTXD	TEST
12	AE09	HBD6	HB	P26	C_EYEXY	CH C	AD26	CS1	MB	H03	B_DSPINT	TEST
13	AE10	HBD7	HB	AA25	C_EYESYNC	CH C	AA26	CS2	MB	C08	B_DSPRST	TEST
14	AF10	HBD8	HB	Y24	C_EYECLK#	CH C	AB26	CS3	MB	F24	DP_TEST#	TEST
15	AE07	HBD9	HB	U25	C_TSAEN#	CH C	Y26	CS4	MB	L24	XYCNT	TEST
16	AF09	HBD10	HB	R26	C_XCLK	CH C	P25	RD#	MB	A01	C_DPRST#	GND thru 20K
17	AF13	HBD11	HB	R25	C_YCLK	CH C	AD24	RW#	MB	A02	A_DPRST#	GND thru 20K
18	AE11	HBD12	HB	A10	A0	MB	N24	WR#	MB	A03	B_DPRST#	GND thru 20K
19	AF12	HBD13	HB	A09	A1	MB	P02	RAS#	MB	T01	PA3	NA
20	AD12	HBD14	HB	A08	A2	MB	P01	CAS#	MB	W01	PA4	NA
21	AE12	HBD15	HB	A07	A3	MB	R03	MCU_CLKOUT	MB	R01	PA5	NA
22	AE16	HBCLK	HB	A06	A4	MB	P03	MCU_CLKIN	SYS	W02	PA6	NA
23	AE17	HBEN#	HB	AE18	A5	MB	A15	DP_CLKIN	SYS	U01	PA7	NA
24	AE14	HBCS#	HB	AF19	A6	MB	W24	MCU_RESET#	SYS	U02	PE0	NA
25	AF16	HBRD#	HB	AE19	A7	MB	W25	ROME	SYS	Y01	PE1	NA
26	AE15	HBWR#	HB	AF21	A8	MB	Y25	MCU_TEST#	SYS	V02	PE2	NA
27	AF04	HBACKR#	HB	AE20	A9	MB	AE03	TCK	JTAG	Y02	PE3	NA
28	AF05	HBACKW#	HB	AF22	A10	MB	AF03	TDI	JTAG	T02	PE4	NA
29	AE04	HBRQSTR	HB	AD20	A11	MB	AE02	TDO	JTAG	AA01	PE5	NA
30	AE05	HBRQSTW	HB	AD18	A12	MB	AD02	TMS	JTAG	V01	PE6	NA
31	AF18	HBIRQ#	HB	AE21	A13	MB	AC01	TRST#	JTAG	AA02	PE7	NA
32	G26	A_SCLK	CH A	AE24	A14	MB	N26	DPBS_TCLK	JTAG	AB01	PF0	NA
33	H26	A_FSYNC	CH A	AD22	A15	MB	AD15	DPBS_TDI	JTAG	AB03	PF1	NA
34	K26	A_RXDATA	CH A	AD21	A16	MB	K02	DPBS_TDO	JTAG	AB02	PF2	NA
35	L26	A_TXDATA	CH A	AF23	A17	MB	AF20	DPBS_TMS	JTAG	AC02	PF3	NA
36	C16	A_PLLVDD	CH A	AF25	A18	MB	C11	DPBS_TRST#	JTAG	AF01	PF4	NA
37	N25	A_PLLGND	CH A	AF24	A19	MB	AD19	C_DPCS	TEST	AE01	PF5	NA
38	A19	A_EYEXY	CH A	AD23	A20	MB	B07	C_DPEXRST	TEST	AF02	PF6	NA
39	F26	A_EYESYNC	CH A	D25	A21	MB	T24	C_DPINT	TEST	AD01	PF7	NA
40	E26	A_EYECLK#	CH A	AE25	A22	MB	V24	C_DPRXCLK	TEST	C05	VDD	3.3V
41	A23	A_TSAEN#	CH A	AF26	A23	MB	B14	C_DPRXD	TEST	C12	VDD	3.3V
42	A20	A_XCLK	CH A	AE26	A24	MB	R24	C_DPTXCLK	TEST	C15	VDD	3.3V
43	A21	A_YCLK	CH A	A14	D0	MB	V25	C_DPTXD	TEST	C24	VDD	3.3V
44	F01	B_SCLK	CH B	B13	D1	MB	P24	C_DSPINT	TEST	D24	VDD	3.3V
45	E01	B_FSYNC	CH B	B12	D2	MB	AD17	C_DSPRST	TEST	F03	VDD	3.3V
46	C01	B_RXDATA	CH B	B11	D3	MB	M25	A_DPCS	TEST	H24	VDD	3.3V
47	B01	B_TXDATA	CH B	B10	D4	MB	B08	A_DPEXRST	TEST	J03	VDD	3.3V
48	G03	B_PLLVDD	CH B	A13	D5	MB	A17	A_DPINT	TEST	K03	VDD	3.3V
49	C09	B_PLLGND	CH B	A12	D6	MB	K24	A_DPRXCLK	TEST	M24	VDD	3.3V
50	L03	B_EYEXY	CH B	A11	D7	MB	B18	A_DPRXD	TEST	T03	VDD	3.3V

Notes: RESERVED = May have internal circuit connected, no external connection allowed.

Table 3-2. RL56CSMV/3 Pin Signals by Interface (Continued)

Table Col.	5			6			7			8		
Table Row	Loc.	Signal	I/F	Loc.	Signal	I/F	Loc.	Signal	I/F	Loc.	Signal	I/F
1	T25	VDD	3.3V	Y20	GND	GND	C26	RESERVED				
2	T26	VDD	3.3V	Y21	GND	GND	D01	RESERVED				
3	U03	VDD	3.3V	AA05	GND	GND	D02	RESERVED				
4	W03	VDD	3.3V	AA06	GND	GND	D03	RESERVED				
5	Y03	VDD	3.3V	AA07	GND	GND	D26	RESERVED				
6	AA03	VDD	3.3V	AA08	GND	GND	E02	RESERVED				
7	AC03	VDD	3.3V	AA19	GND	GND	E03	RESERVED				
8	AD03	VDD	3.3V	AA20	GND	GND	E05	RESERVED				
9	AD04	VDD	3.3V	AA21	GND	GND	E06	RESERVED				
10	AD05	VDD	3.3V	AB05	GND	GND	E07	RESERVED				
11	AD06	VDD	3.3V	AB06	GND	GND	E08	RESERVED				
12	AD07	VDD	3.3V	AB07	GND	GND	E19	RESERVED				
13	AD08	VDD	3.3V	AB08	GND	GND	E20	RESERVED				
14	AD09	VDD	3.3V	A16	RESERVED		E21	RESERVED				
15	AD10	VDD	3.3V	A22	RESERVED		E22	RESERVED				
16	AD11	VDD	3.3V	A24	RESERVED		E24	RESERVED				
17	AE22	VDD	3.3V	A25	RESERVED		E25	RESERVED				
18	A04	VGG	5V	A26	RESERVED		F02	RESERVED				
19	U24	VGG	5V	AA22	RESERVED		F05	RESERVED				
20	AA24	VGG	5V	AB19	RESERVED		F22	RESERVED				
21	F06	GND	GND	AB20	RESERVED		F25	RESERVED				
22	F07	GND	GND	AB21	RESERVED		G02	RESERVED				
23	F08	GND	GND	AB22	RESERVED		G05	RESERVED				
24	F19	GND	GND	AB24	RESERVED		G22	RESERVED				
25	F20	GND	GND	AE23	RESERVED		G24	RESERVED				
26	F21	GND	GND	AF17	RESERVED		G25	RESERVED				
27	G06	GND	GND	B02	RESERVED		H02	RESERVED				
28	G07	GND	GND	B03	RESERVED		H05	RESERVED				
29	G08	GND	GND	B04	RESERVED		H22	RESERVED				
30	G19	GND	GND	B05	RESERVED		H25	RESERVED				
31	G20	GND	GND	B06	RESERVED		J01	RESERVED				
32	G21	GND	GND	B15	RESERVED		J24	RESERVED				
33	H06	GND	GND	B16	RESERVED		J25	RESERVED				
34	H07	GND	GND	B17	RESERVED		J26	RESERVED				
35	H08	GND	GND	B19	RESERVED		L25	RESERVED				
36	H19	GND	GND	B20	RESERVED		R02	RESERVED				
37	H20	GND	GND	B21	RESERVED		U26	RESERVED				
38	H21	GND	GND	B26	RESERVED		V03	RESERVED				
39	W05	GND	GND	C02	RESERVED		W22	RESERVED				
40	W06	GND	GND	C03	RESERVED		Y22	RESERVED				
41	W07	GND	GND	C04	RESERVED							
42	W08	GND	GND	C10	RESERVED							
43	W19	GND	GND	C14	RESERVED							
44	W20	GND	GND	C17	RESERVED							
45	W21	GND	GND	C18	RESERVED							
46	Y05	GND	GND	C19	RESERVED							
47	Y06	GND	GND	C20	RESERVED							
48	Y07	GND	GND	C21	RESERVED							
49	Y08	GND	GND	C22	RESERVED							
50	Y19	GND	GND	C25	RESERVED							

Notes: RESERVED = May have internal circuit connected, no external connection allowed.

Table 3-3. RL56CSMV/3 Signal Definitions

Label	I/O Type	Signal Name/Description
SYSTEM OVERHEAD		
MCU_CLKIN	It	**MCU Clock In.** Connect to an external 40.0 MHz clock.
DP_CLKIN	Itclk	**Data Pump Clock In**. Connect to an external 28.224 MHz clock.
MCU_RESET#	It/Ot8	**MCU Reset.** This active low input resets the modem to factory default values. After application of VDD, MCU_RESET# must be held low for at least 2 ms after the VDD reaches operating range. The CSMV/3 is ready to use 2 ms after the low-to-high transition of MCU_RESET#.
ROME	It	**MCU Internal ROM Enable.** Active high input enables MCU internal ROM access; low disables internal ROM access.
MCU_TEST#	Itpu	**MCU Test Mode.** Active low input enables test mode (factory test only). Leave open for normal operation.
VDD	PWR	**Digital Supply Voltage.** Connect to +3.3V.
VGG	PWR	**5V Reference Voltage.** VGG is the reference voltage for +5V tolerant inputs. Connect to +5V if +5V tolerant inputs are required, otherwise, connect to VDD.
GND	GND	**Digital Ground.** Connect to digital ground.
PARALLEL HOST INTERFACE		
HBA[5:1]	It	**Host Bus Address Lines 1-5.** During a host read or write operation with HBCS# low, HBA[5:1] select one of 32 Host Bus registers.
HBD[15:0]	It/Ot8	**Host Bus Data Lines 0-15**. HBD[15:0] comprise 16 three-state input/output lines providing bidirectional communication between the host and the modem. Data, control words, and status information are transferred over HBD[15:0].
HBCLK	Itpu	**Host Bus Clock.** Bus clock used to synchronize host bus accesses.
HBEN#	Itpu	**Host Bus Data Output Enable.** When HBRD# low and HBEN# is low, the Host Data Bus lines (HBD0-HBD15) are active; when HBRD# high and HBEN# high, the HBD0-HBD15 lines are tri-stated. HBRD# and HBEN# can be tied together.
HBCS#	Itpu	**Host Bus Chip Select.** HBCS# input low enables the host bus interface.
HBRD#	Itpu	**Host Bus Read.** HBRD# is an active low read control input. When HBCS# is low, HBRD# low allows the host to read status information or data from the selected Host Bus register.
HBWR#	Itpu	**Host Bus Write.** HBWR# is an active low write control input. When HBCS# is low, HBWR# low allows the host to write data or control words into the selected Host Bus register.
HBACKR#	Itpu	**Host Bus Receive DMA Acknowledge.** HBACKR# is an active low input asserted to acknowledge receipt of HBRQSTR by the host.
HBACKW#	Itpu	**Host Bus Transmit DMA Acknowledge.** HBACKW# is an active low input asserted to acknowledge receipt of HBRQSTW by the host.
HBRQSTR	Otts8	**Host Bus Receive DMA Request.** HBRQSTR is an active high output asserted to request DMA transfer of received data.
HBRQSTW	Otts8	**Host Bus Transmit DMA Request.** HBRQSTW is an active high output asserted to request DMA transfer of transmit data.
HBIRQ#	Otts8	**Host Bus Interrupt Request**. HBIRQ# is an active low open drain output asserted to request host interrupt service.

Table 3-3. RL56CSMV/3 Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
MEMORY BUS INTERFACE		
A0-A24	It/Ot8	**Memory Address Lines 0-24.** A0-A24 are the external memory bus address lines. Connect A1-A12 to the SDRAM A0-A11 pins, respectively.
D0-D15	It/Ot8	**Memory Data Lines 0-15.** D0-D15 are the external memory bus data lines. Connect D0-D15 to the SDRAM D0-D15 pins, respectively.
MCU_CLKOUT	Otts8	**MCU Clock Out.** MCU_CLKOUT is an output clock at MCU_CLKIN frequency. Connect to the SDRAM CLK pin.
RD#	Otts8	**Read Enable.** RD# is an active low output used to enable data transfer from the selected device to the D0-D15 lines. Not used with SDRAM.
WR#	Otts8	**Write Enable.** WR# is an active low output used to enable data transfer from the D0-D15 lines to the selected device. Not used with SDRAM.
CS0-CS4	Otts8	**Chip Select Line 0, 1, 2, 3, and 4.** CS0-CS4 are active low chip select output lines used to select external memory. Not used with SDRAM.
BS[1:0]	Otts8	**Byte Select Lines 0 - 1.** The BS output is used by the SDRAM to select the upper and lower bytes for 16-bit SDRAM access. Connect BS0 to SDRAM DGML pin and BS1 to SDRAM DGMU pin.
RAS#	Otts8	**Row Address Strobe.** RAS# is an active low output used by the SDRAM to define the SDRAM operation commands in conjunction with the CAS# and WR# signals and is latched by the SDRAM at the positive edge of CLK. Connect to SDRAM RAS# pin.
CAS#	Otts8	**Column Address Strobe.** CAS# is an active low output to used by the SDRAM to define the SDRAM operation commands in conjunction with the RAS# and WR# signals and is latched at the positive edge of CLK. Connect to SDRAM CAS# pin.
RW#	Itpu/Ot8	**Read Not Write Pulse.** Connect to WE# of SDRAM.

Table 3-3. RL56CSMV/3 Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
T1/E1 TRANSCEIVER INTERFACE		
A_RXDATA B_RXDATA C_RXDATA	Itk	**Receive Serial Data.** A-Law/μ-Law PCM receive data sample from the T1/E1 Transceiver.
A_TXDATA B_TXDATA C_TXDATA	It/Ot8	**Transmit Serial Data.** A-Law/μ-Law PCM transmit data sample to the T1/E1 Transceiver. Tri-states when not shifting (Figure 3-8). TXDATA requires a 33 ohm series resistor, to avoid problems caused by one driver turning off, while another driver is turning on.
A_SCLK B_SCLK C_SCLK	Itpu/Ot2	**Clock.** Shift clock (1.544 MHz - 8.192 MHz) input from the T1/E1 Transceiver. **NOTE:** FSYNC and SCLK must be operating whenever the device is not in Reset.
A_FSYNC B_FSYNC C_FSYNC	Itpu	**Frame Sync.** 8 kHz frame sync input from the T1/E1 Transceiver. **NOTE:** FSYNC and SCLK must be operating whenever the device is not in Reset.
A_EYEXY B_EYEXY C_EYEXY	Otts2	**Eye Pattern X/Y Data Output.** Not supported. No external connection.
A_EYECLK# B_EYECLK# C_EYECLK#	Otts2	**Eye Pattern Clock Output.** Not supported. No external connection.
A_EYESYNC B_EYESYNC C_EYESYNC	Otts2	**Eye Pattern Sync Output.** Not supported. No external connection.
A_XCLK B_XCLK C_XCLK	It/Ot2	**XCLK Output.** Clock output at the data pump input frequency (DP_CLKIN). No external connection.
A_YCLK B_YCLK C_YCLK	It/Ot2	**YCLK Output.** Clock output at one-half the data pump input frequency (DP_CLKIN) divided by two.
A_PLLVDD B_PLLVDD C_PLLVDD,	PLL	**PLLVDD Connection.** Connect to VDD through a 10 Ω resistor and to PLLGND through 0.1 μF and 10 μF capacitors in parallel.
A_PLLGND B_PLLGND C_PLLGND	PLL	**PLLGND Connection.** Connect to GND.
A_TSAEN# B_TSAEN# C_TSAEN#	Itpu	**Time Slot Assigner Enable.** These pins must be tied to ground to enable the Time Slot Assigner.

Table 3-3. RL56CSMV/3 Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
TEST/NOT USED		
DP_TEST#	Itpu	**Data Pump Test.** Factory test only. Internal pull-up. Leave open
XYCNT	Itpu	**XY Control.** Factory test only. Internal pull-up. Leave open
A_DPCS B_DPCS C_DPCS	Itpu	**Data Pump Chip Select.** Factory test only. Internal pull-up. Leave open
A_DPEXRST B_DPEXRST C_DPEXRST	Ith	**Data Pump External Reset.** Factory test only; leave open.
A_DPINT B_DPINT C_DPINT	Itpu	**Data Pump Interrupt.** Factory test only. Internal pull-up. Leave open
A_DPRST# B_DPRST# C_DPRST#	Ith	**Data Pump Reset.** Connect to GND through a 20K Ω resistor.
A_DPRXCLK B_DPRXCLK C_DPRXCLK	Otts2	**Data Pump Receive Data Clock.** Factory test only; leave open.
A_DPRXD B_DPRXD C_DPRXD	Otts2	**Data Pump Receive Data.** Factory test only; leave open.
A_DPTXCLK B_DPTXCLK C_DPTXCLK	Otts2	**Data Pump Transmit Data Clock.** Factory test only; leave open.
A_DPTXD B_DPTXD C_DPTXD	Itpu	**Data Pump Transmit Data.** Factory test only; leave open.
A_DSPINT B_DSPINT C_DSPINT	It	**Data Pump DSP Interrupt.** Factory test only. Internal pull-up. Leave open
A_DSPRST B_DSPRST C_DSPRST	Ith	**Data Pump DSP Reset.** Factory test only; leave open.
JTAG TEST		
TCK	Ij	**MCU Test Clock.** This is the boundary scan clock signal of the microcontroller. This pin has an internal pulldown, and it conforms to IEEE 1149.1 JTAG specification.
TDI	Ijpu	**MCU Test Input.** This is the boundary scan serial input signal of the microcontroller, and it is shifted in on the rising edge of TCK. The pin has an internal pullup, and it conforms to IEEE 1149.1 JTAG specification.
TDO	Ojts4	**MCU Test Output.** This is the tristateable boundary scan data output signal from the microcontroller, and it is shifted out on the falling edge of TCK. It conforms to IEEE 1149.1 JTAG specification.
TMS	Ijpu	**MCU Test Mode Select.** This is the control signal to the microcontroller TAP controller. This pin has an internal pull-up, and it conforms to IEEE 1149.1 JTAG specification.
TRST#	Ijpu	**MCU Test Reset**. A high to low signal forces the microcontroller TAP controller into a logic reset state. It must be held low during normal (non-test) operation. This pin has an internal pull-up, and it conforms to IEEE 1149.1 JTAG specification. TRST# requires a 3K ohm pull-down resistor to GND.
DPBS_TCLK	Ij	**Data Pump Test Clock.** This is the boundary scan clock signal for the internal data pumps. This pin does not have an internal pulldown. In an application design, connect to an external 50KΩ pulldown. It conforms to IEEE 1149.1 JTAG specification.
DPBS_TDI	Ijpu	**Data Pump Test Input.** This is the boundary scan serial input data for the internal data pumps. It is shifted in on the rising edge of DPBS_TCK, and then daisy chained to all the data pumps. This pin has an internal pullup. It conforms to IEEE 1149.1 JTAG specification.
DPBS_TDO	Ojts4	**Data Pump Test Output.** This tristateable boundary scan data output signal from the last daisy chained data pump. It is shifted out on the falling edge of DPBS_TCK. It conforms to IEEE 1149.1 JTAG specification.

Table 3-3. RL56CSMV/3 Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
DPBS_TMS	Ijpu	**Data Pump Test Mode Select.** This is the control signal to the data pump TAP controllers. This pin has an internal pullup. It conforms to IEEE 1149.1 JTAG specification.
DPBS_TRST#	Ijpu	**Data Pump Test Reset**. A high to low signal forces the data pump TAP controller into a logic reset state. This pin has an internal pullup and must be held low during normal (non-test) operation. It conforms to IEEE 1149.1 JTAG specification. DPBS_TRST# requires a 3K ohm pull-down resistor to GND.
UNASSIGNED		
PA3	It/Ot8	**Port PA3.** Not used; leave open.
PA4	It/Ot8	**Port PA4.** Not used; leave open.
PA5	It/Ot8	**Port PA5.** Not used; leave open.
PA6	It/Ot8	**Port PA6.** Not used; leave open.
PA7	It/Ot8	**Port PA7.** Not used; leave open.
PE0	It/Ot8	**Port PE0.** Not used; leave open.
PE1	It/Ot8	**Port PE1.** Not used; leave open.
PE2	It/Ot8	**Port PE2.** Not used; leave open.
PE3	It/Ot8	**Port PE3.** Not used; leave open.
PE4	It/Ot8	**Port PE4.** Not used; leave open.
PE5	It/Ot8	**Port PE5.** Not used; leave open.
PE6	It/Ot8	**Port PE6.** Not used; leave open.
PE7	It/Ot8	**Port PE7.** Not used; leave open.
PF0	It/Ot8	**Port PF0.** Not used; leave open.
PF1	It/Ot8	**Port PF1.** Not used; leave open.
PF2	It/Ot8	**Port PF2.** Not used; leave open.
PF3	It/Ot8	**Port PF3.** Not used; leave open.
PF4	It/Ot8	**Port PF4.** Not used; leave open.
PF5	It/Ot8	**Port PF5.** Not used; leave open.
PF6	It/Ot8	**Port PF6.** Not used; leave open.
PF7	It/Ot8	**Port PF7.** Not used; leave open.

Note: See I/O Type Descriptions in Table 3-4.

Table 3-4. I/O Type Descriptions

I/O Type	Description	Reference
Ij	+5V Tolerant JTAG Input, C_{IN} = 8 pF	pjd00n
Ijpu	+5V Tolerant JTAG Input, internal 75k ± 25k ohm pull-up, C_{IN} = 8 pF	pjd00u
It	+5V Tolerant TTL Input, C_{IN} = 8 pF	ptd00n
It/Ot2	+5V Tolerant TTL Input/TTL Output, 2 mA into 120 ohm load, C_{IN} = 9 pF	ptb01n
It/Ot8	+5V Tolerant TTL Input/TTL Output, 8 mA into 50 ohm load, C_{IN} = 9 pF	ptb03n
Itclk	+5V Tolerant TTL Input, clock, internal keeper, C_{IN} = 22 pF	
Ith	+5V Tolerant TTL Input, hysterisis, C_{IN} = 8 pF	ptd10n
Itk	+5V Tolerant TTL Input, internal keeper, C_{IN} = 8 pF	ptd00r
Itpd	+5V Tolerant TTL Input, internal 75k ± 25k ohm pull-down, C_{IN} = 8 pF	ptd00d
Itpu	+5V Tolerant TTL Input, internal 75k ± 25k ohm pull-up, C_{IN} = 8 pF	ptd00u
Itpu/Ot2	+5V Tolerant TTL-compatible Input/TTL-compatible Output (Bidirectional), 2 mA into 120 ohm load, with 75k ± 25k ohm pull-up, C_{IN} = 9 pF	ptb01ud
Itpu/Ot8	+5V Tolerant TTL Input/TTL Output (Bidirectional), 8 mA into 50 ohm load, with 75k ± 25k ohm pull-up, C_{IN} = 9 pF	ptb03u
Ojts4	+5V Tolerant JTAG 3-State Output, 4 mA into 80 ohm load, C_{IN} = 10 pF	pjt02n
Otts2	+5V Tolerant TTL 3-State Output, 2 mA into 120 ohm load, C_{IN} = 10 pF	ptt01n
Otts8	+5V Tolerant TTL 3-State Output, 8 mA into 50 ohm load, C_{IN} = 10 pF	ptt03n

Note: See Digital Electrical Characteristics in Table 3-5.

Table 3-5. Digital Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage Low	V_{IL}	-0.3	–	0.8	VDC	
Input Voltage High	V_{IH}	2.0	–	5.25	VDC	VGG = 5V
		2.0	–	3.6	VDC	VGG = 3.3V
Input Current Low (See Note 2)	I_{IL}	–	–	-10	µA	V_{IN} = 0
Input Current High (See Note 2)	I_{IH}	–	–	+10	µA	V_{IN} = 5.25V
Input Current Low (with internal pull-downs) (See Note 2)	I_{IL}	–	–	-10	µA	V_{IN} = 0
Input Current High (with internal pull-downs) (See Note 2)	I_{IH}	–	–	+100	µA	V_{IN} = 5.25V
Input Current Low (with internal pull-ups) (See Note 2)	I_{IL}	-15	–	-100	µA	V_{IN} = 0
Input Current High (with internal pull-ups) (See Note 2)	I_{IH}	–	–	+10	µA	V_{IN} = 5.25V
Output Voltage Low	V_{OL}	–	–	0.4	VDC	See Note 3
Output Voltage High	V_{OH}	2.4	–	VDD	VDC	See Note 4
Three-State (Off) Current Low	I_{OZL}	–	–	-10	µA	V_{IN} = 0
Three-State (Off) Current High	I_{OZH}	–	–	+10	µA	V_{IN} = 5.25V

Notes:

1. Test Conditions: VDD = +3.3V ± 0.3V, TA = 0°C to 70°C, (unless otherwise stated).
2. Current flow out of the device is shown as minus.
3. I_{OL} = 8 mA for I/O types It/Ot8, Ot8, Otts8, and Itpu/Ot8.
   I_{OL} = 4 mA for I/O type It/Ot4.
   I_{OL} = 2 mA for I/O types It/Ot2 and Otts2.
4. I_{OH} = -8 mA for I/O types It/Ot8, Ot8, Otts8, and Itpu/Ot8.
   I_{OH} = -4 mA for I/O type It/Ot4.
   I_{OH} = -2 mA for I/O types It/Ot2 and Otts2.

3.2 ELECTRICAL AND ENVIRONMENTAL SPECIFICATIONS

3.2.1 Operating Conditions and Absolute Maximum Ratings

Operating conditions are stated in Table 3-6.

The absolute maximum ratings are listed in Table 3-7.

3.2.2 Current and Power Requirements

The current and power requirements are listed in Table 3-8.

Table 3-6. Operating Conditions

Parameter	Min.	Max.	Units
VDD	+3.0	+3.6	VDC
VGG	+4.75	+5.25	VDC
Ambient Temperature (TA)	0	70	0°C

Table 3-7. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	VDD	-0.5 to +4.0	V
Input Voltage	V_{IN}	-0.5 to (VGG +0.5)	V
Operating Temperature Range	T_A	-0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (VGG + 0.5)	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	V
Latch-up Current (25°C)	I_{TRIG}	±300	mA
Latch-up Current (125°C)	I_{TRIG}	±150	mA
Latch-up Current (25°C)	I_{TRIG}	±400	mA
Maximum Junction Temperature	T_J	125	°C

Table 3-8. Current and Power Requirements

Mode	DDP Clock at 28.224 MHz				DDP Clock at 45 MHz			
	Typ. Current (mA)	Max. Current (mA)	Typ. Power (mW)	Max. Power (mW)	Typ. Current (mA)	Max. Current (mA)	Typ. Power (mW)	Max. Power (mW)
RL56CSM/3 (R7138)								
Normal mode	300	305	990	1100	NA	NA	NA	NA
Sleep mode	163		540					
RL56CSMV/3 (R7178)								
Normal mode	275	280	910	1010	330	333	1090	1200
Sleep mode	152		500		152		500	

Notes:

1. Current and power figures represent entire device (3 channels).
2. Test Conditions: VDD = 3.3 VDC for typical values; VDD = 3.6 VDC for maximum values.
   TA = 0°C to 70°C
3. f = internal operating frequency: MCU = 40 MHz; DDP = 28.224 MHz (during non-G.728 modes) or 45 MHz (during G.728 mode).

The BGA thermal characteristics are listed in Table 3-9.

Table 3-9. Thermal Characteristics

Die Name	Die Number	T_{diff} (°C)	Natural Convection Cooling			Forced Convection Cooling at 1 m/s		
			Trise (°C)	Tmax (°C)	Tcase (°C)	Trise (°C)	Tmax (°C)	Tcase (°C)
MCU	1	2.0 °C	27	97	95	23	93	91
DDP	2, 3, and 4	2.0 °C	22	92	90	17.5	87.5	85.5

Notes:

1. The thermal performance of multi die BGA packages is shown by temperature rise over the ambient temperature [°C] for different devices inside the package. The maximum operating junction temperature and case temperature can be estimated as follows:

   Where:

   Tambient = Ambient temperature (specified at 70 °C) measured 2 inches above the center of the package.

   Tdiff = Temperature difference between junction and case (specified for a given die).

   Trise = Temperature rise (specified for a given die for Natural Convection and Forced Convection at 1 m/s conditions).

   Tmax = Maximum operating junction temperature = Tambient + Trise [°C].

   Tcase = Case temperature = Tmax - Tdiff.[°C].

   Example: Hottest Die; natural convection case with maximum Tambient = 70 °C:

   Tdiff = 2.0 °C (the case temperature for the hottest die is ~2.0 °C lower than the maximum junction temperature).

   Tmax = Tambient + Trise [°C] = 70 +27 = 97 °C.

   Tcase = Tmax – Tdiff [°C] = 97 - 2.0 = 95 °C.

2. Maximum allowable junction temperature = 125 °C.

3.2.3 Thermal Characteristics

Package Thermal Design and Test Structure

Figure 3-3 shows the internal structure of the multi-die Ball Grid Array [BGA] package. Four die are mounted on a laminate substrate and over-molded for mechanical protection. The internal heat path transfers the heat from the top surface of the die to the bottom surface of the package through thermal vias and voltage planes.

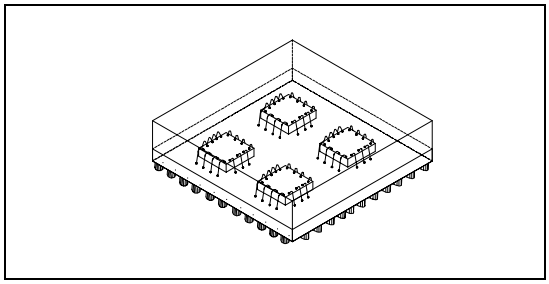

Figure 3-3. Multi Die Ball Grid Array Package

Figure 3-3 and Figure 3-4 show the primary heat flow path in a multi-die BGA package.

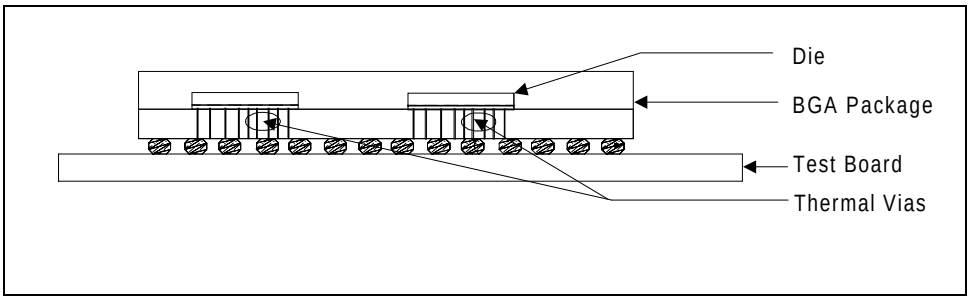

Figure 3-4. Package Internal Heat Removal Path

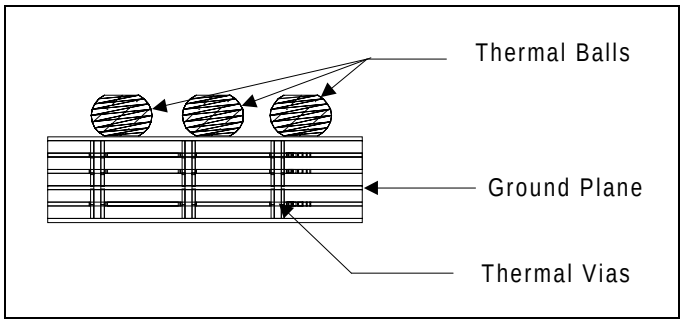

Figure 3-5. Connecting BGA Thermal Balls to Motherboard Ground Plane by Using Thermal Vias

To obtain the best package thermal performance, connect the thermal balls to the motherboard ground plane, using thermal vias shown in Figure 3-5.

Product Thermal Performance

For multi-die packages, an equivalent thermal resistance is used to represent thermal performance. This definition is used to evaluate thermal performance of the package directly in a system level situation. The defined equivalent thermal resistance is only valid at the stated power conditions.

Junction Temperature Calculation for Package Type: 35 mm BGA, Size = 35.0 mm * 35.0 mm * 2.27 mm

Maximum junction temperature can be calculated as:

$$T_j = P \times \theta_{ja} + T_a \quad (1)$$

Where:

θ_{ja} = Equivalent Package Thermal Resistance (°C/W)

T_j = Maximum Junction Temperature(°C)

T_a = Ambient Temperature (°C)

P = Package Total Power Dissipation Value (W)

For the RL56CSM/3 (R7138)

P = 1.190 (W)

θ_{ja} = 19.55 °C/W (natural convection)

θ_{ja} = 15.20 °C/W (1 m/s air flow)

From equation (1) and assuming maximum ambient temperature of 70 °C, maximum junction temperature for the natural convection case is calculated as:

$$T_j = 1.190 \times 19.55 + 70 = 93.25 \text{ °C}$$

For the RL56CSMV/3 (R7178):

P = 1.310 (W)

θ_{ja} = 19.48 °C/W (natural convection)

θ_{ja} = 14.85 °C/W (1 m/s air flow)

From equation (1) and assuming maximum ambient temperature of 70 °C, maximum junction temperature for the natural convection case is calculated as:

$$T_j = 1.310 \times 19.48 + 70 = 95.50 \text{ °C}$$

Test Structure

Package thermal performance has been tested following JEDEC standards. The BGA package has been mounted at the center of a 100 mm x 100 mm 6-layer test board and has been tested under different air flow velocities. Figure 3-6 shows the system configuration.

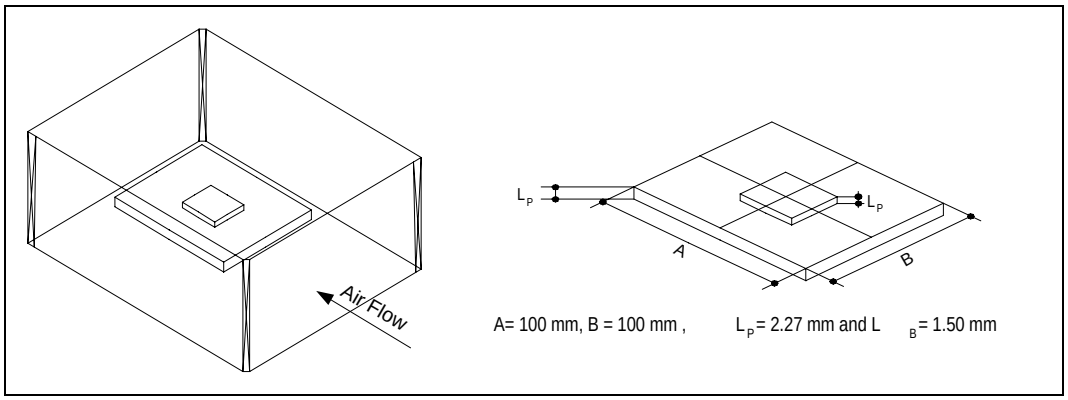

Figure 3-6. Test Performance Structure

3.3 INTERFACE TIMING AND WAVEFORMS

3.3.1 External SDRAM

The CSMV/3 requires connection to a 2 x 512k x 16-bit Synchronous Dynamic RAM (SDRAM) meeting the Intel PC100 Spec.

Note: Address A0-A11 of SDRAM connects to A1-A12 of RL56CSM/3.

The SDRAM interface waveforms are shown in Figure 3-7 and interface timing is listed in Table 3-10.

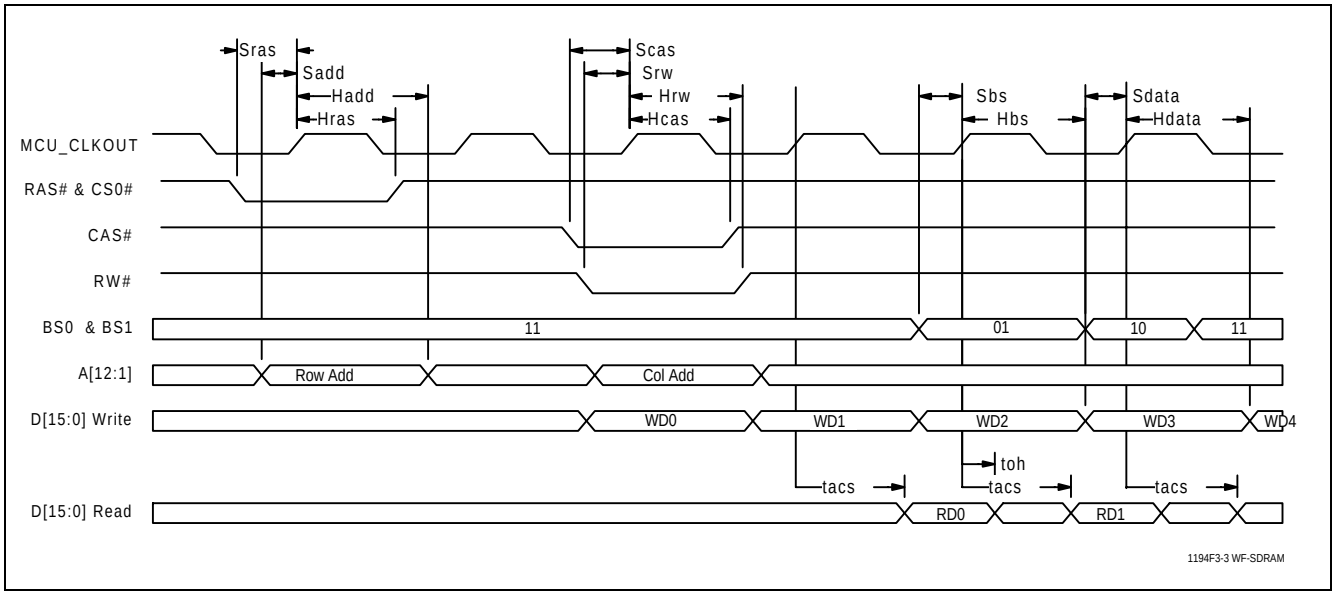

Figure 3-7. SDRAM Interface Timing

Table 3-10. SDRAM Interface Timing

Symbol	Parameter	Min.	Max.	Unit
Scas	CAS Setup time	2.5	-	ns
Hcas	CAS Hold time	4	-	ns
Sras	RAS Setup time	2.5	-	ns
Hras	RAS Hold time	4	-	ns
Srw	RW Setup time	2.5	-	ns
Hrw	RW Hold time	4	-	ns
Sbs	BS Setup time	2.5	-	ns
Hbs	BS Hold time	4	-	ns
Sadd	Address Setup time	4.5	-	ns
Hadd	Address Hold time	4	-	ns
Sdata	Data Setup time	6.25	-	ns
Hdata	Data Hold time	4	-	ns
tacs	SDRAM Access time	-	9	ns
toh	SDRAM Output Hold time	3	-	ns

3.3.2 T1/E1 Transceiver Interface Timing

The T1/E1 Transceiver interface timing is listed in Table 3-11 and waveforms are shown in Figure 3-8.

Table 3-11. Timing – T1/E1 Transceiver

Parameter	Symbol	Min.	Max.	Unit
SCLK frequency	fSCK	1.0	12.0	MHz
SCLK duty cycle @ above 8 MHz		40	60	%
@ equal or below 8 MHz		30	70	%
FSYNC low time	Tf0	900		ns
FSYNC high time	Tf1	900		ns
FSYNC setup time relative to SCLK falling edge	Tfs	10		ns
FSYNC hold time relative to SCLK falling edge	Tfh	10		ns
TXDATA delay from SCLK rising edge @ 50 pF	Tckdv		20	ns
@ 200 pF			28	ns
@500 pF			50	ns
First TXDATA bit delay from FSYNC rising edge @ 50 pF	Tfsdv		20	ns
@ 200 pF			28	ns
@ 500 pF			50	ns
RXDATA setup time relative to SCLK falling edge	Trs	10		ns
RXDATA hold time relative to SCLK falling edge	Trh	10		ns
TXDATA High-Z output delay	Ttxhz	4	10	ns
TXDATA Low-Z output delay	Ttxlz	4	10	ns
Test Conditions: VDD = 3.3 ± 0.3 VDC, TA = 0°C to 70°C.				

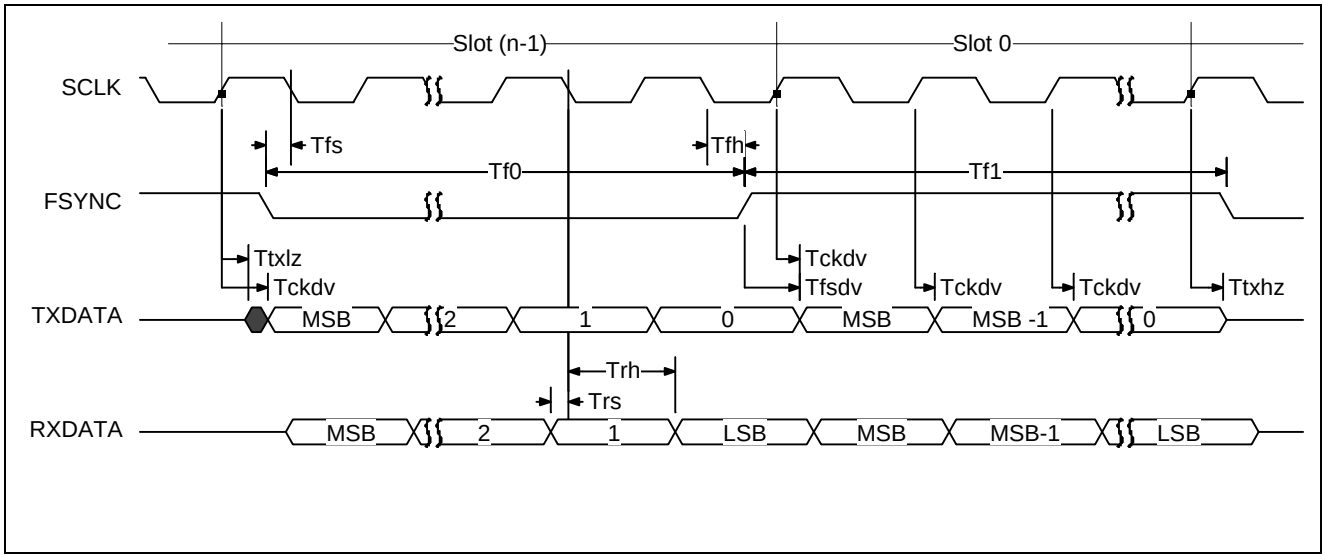

Figure 3-8. TDM Bus Timing Diagram

To detect the rising edge of FSYNC, the DDP uses the falling edge of SCLK (with Tfs and Tfh) to first sample FSYNC low. Once FSYNC is detected low, the DDP looks for the rising edge of FSYNC. The next rising edges of FSYNC and SCLK (with Tckdv and Tfsdv) determine the output of the first TXDATA data. After the first TXDATA bit of the first time slot, all subsequent TXDATA bits depend on the rising edge of SCLK (and Tckdv) only. Note that the rising edge of FSYNC may occur earlier or later than the rising edge of the SCLK.

3.3.3 Oscillator Waveform Requirements

The oscillator waveform requirements are shown in Figure 3-9.

NOTES:

1. Use care in PCB routing of MCU_CLKIN and MCU_CLKOUT signals. Minimize trace length, add terminations as required, and avoid impedance discontinuities to retain waveform integrity, i.e., maintain duty cycle, rise and fall times, and minimize undershoot and overshoot.
2. Keep all traces and component leads connected to clock input and output pins short in order to reduce induced noise levels and minimize any stray capacitance that could affect the clock oscillator.
3. Allow for a series impedance matching resistor at the clock source, and a parallel terminating resistor at the clock inputs.
4. Use of a Clock Buffer Driver is strongly recommended in order to meet rise and fall time requirements.

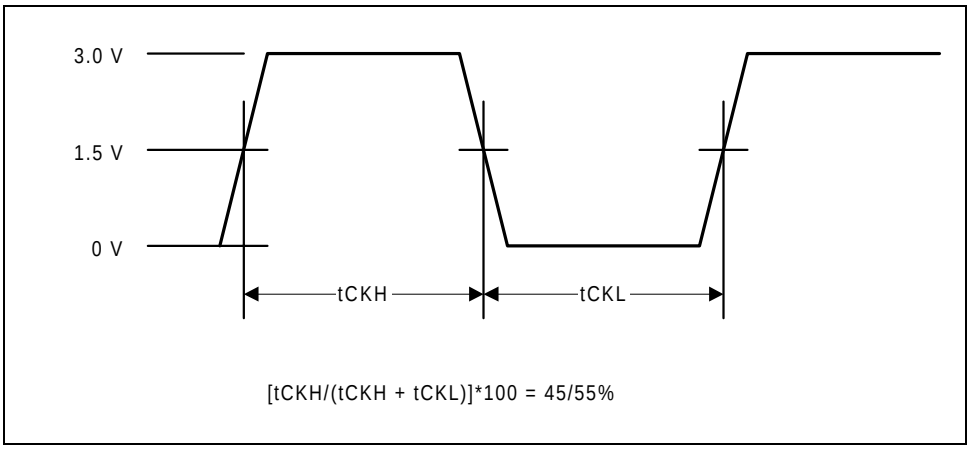

Figure 3-9. Oscillator Waveform Requirements

3.4 SDRAM INTERFACE CONNECTIONS

3.4.1 16-Mbit SDRAM Interface

The interface connections to a 16-Mbit SDRAM are shown in Figure 3-10.

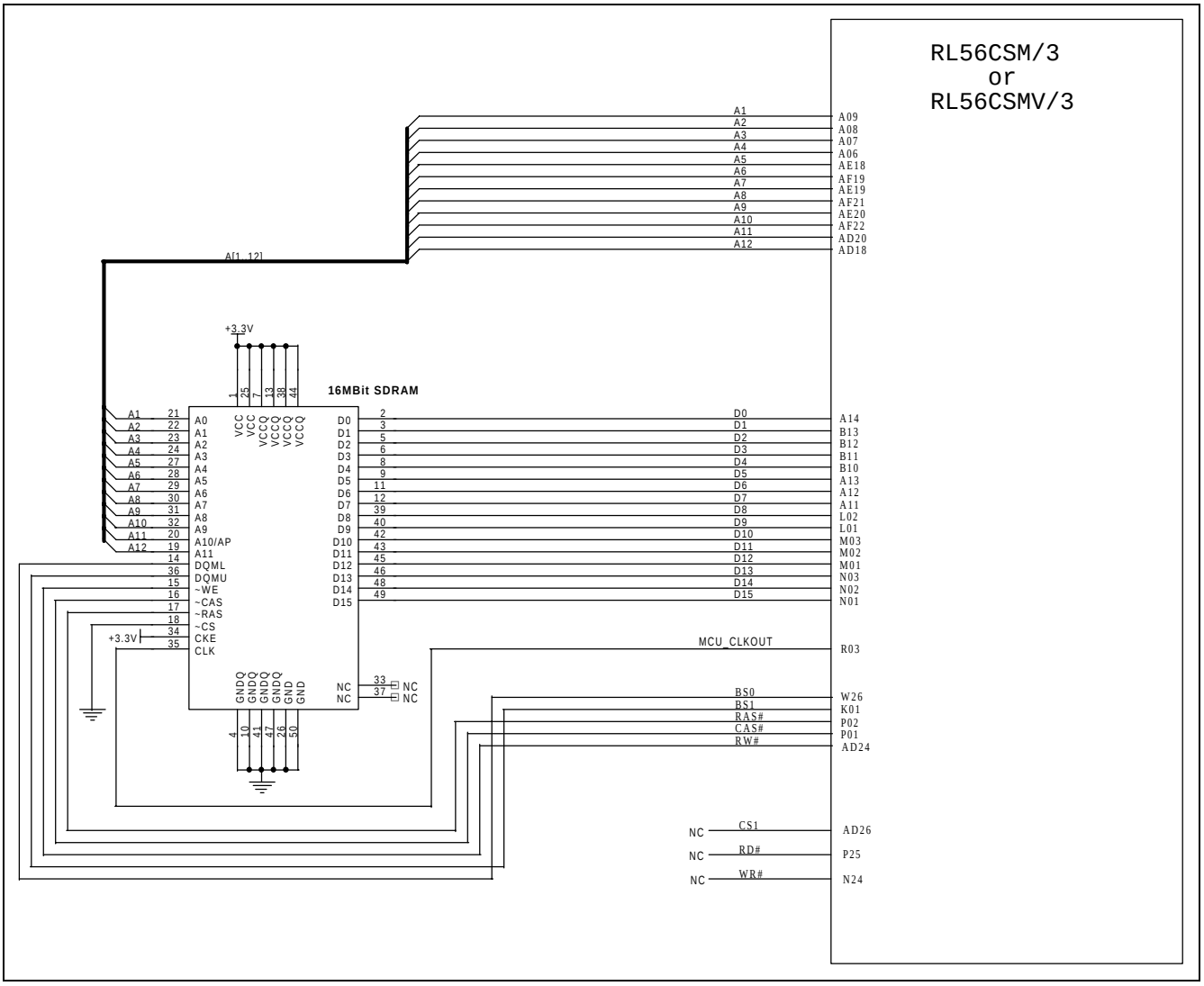

Figure 3-10. 16-Mbit SDRAM Interface Connections

3.4.2 64-Mbit SDRAM Interface

The interface connections to a 64-Mbit SDRAM are shown in Figure 3-11.

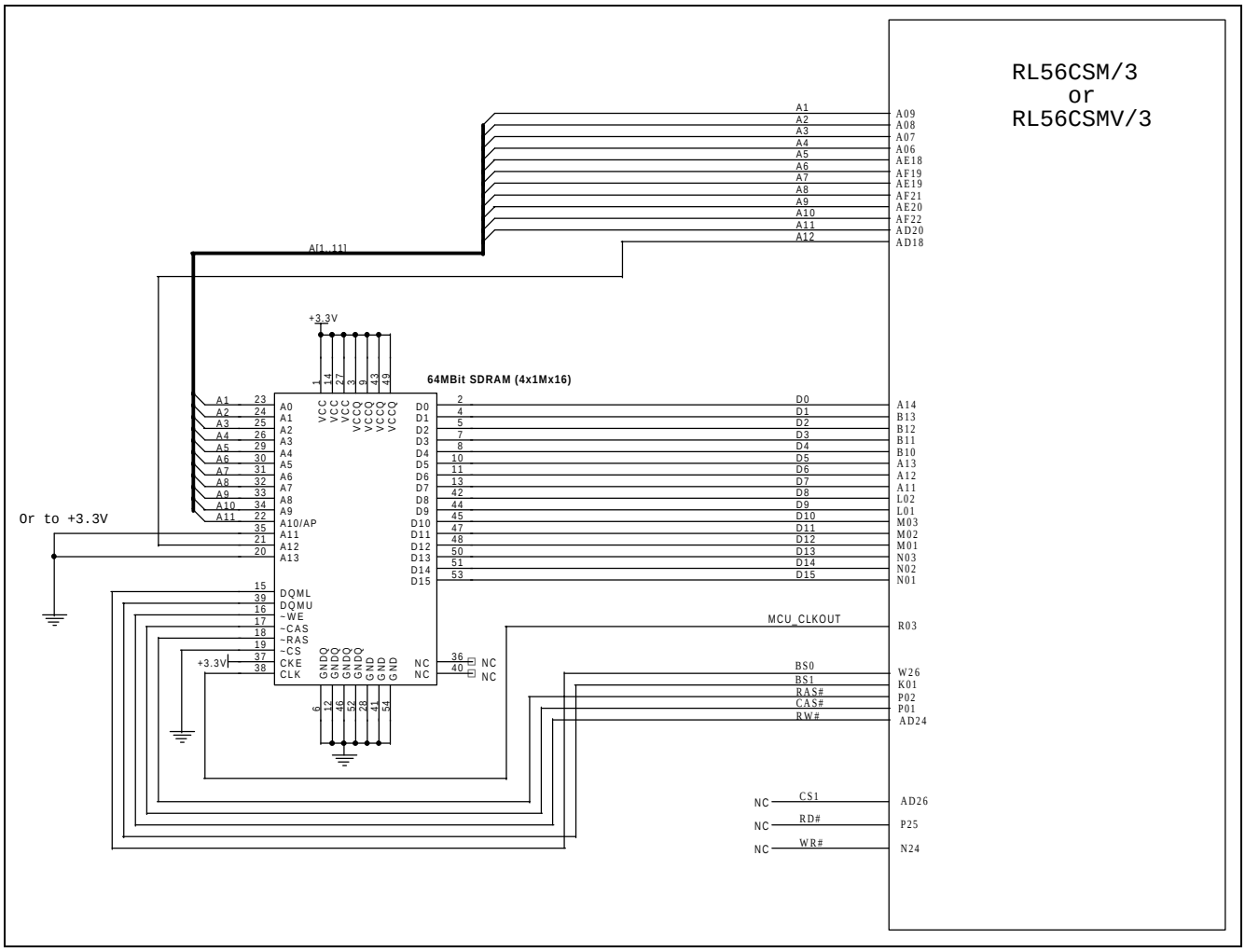

Figure 3-11. 64-Mbit SDRAM Interface Connections

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4. HOST INTERFACE

4.1 REGISTERS AND FIFO

The Host interface (Figure 4-1) is served by two FIFOs, one for transmitted data (outbound) from the Host and one for received data (inbound) to the Host. In addition to the FIFOs, there are four transmit and four receive “mailbox” registers that serve for out-of-band control data between the Host and the microcontroller. Status and interrupt control registers are also provided.

Each FIFO is 128 bytes deep. The Host interface is 16-bits wide, thus only 64 operations are required to read or write the entire FIFO. The design of the FIFOs and associated registers allows simultaneous access by both the Host and the microcontroller without the loss or modification of any data being exchanged.

Five Host bus address inputs select one of 32 possible registers, 16 of which are reserved (Table 4-1).

Host bus READ, WRITE and Chip Select signals are also input for control. External DMA request and acknowledge signals are provided. The RX DMA Request is invoked when the FIFO threshold has been reached. RX DMA Requests cease once the FIFO has been emptied. Receipt of a DMA acknowledge signal forces assertion of the Host chip select and the FIFO address. When the DMA acknowledge signal is active, the presence of the Host READ or WRITE will transfer FIFO data to or from the bus, respectively. Similarly, the TX DMA Request is invoked when the TX_FIFO is empty and continues until the FIFO threshold has been reached. The Request signals are active high and the acknowledge signals active low.

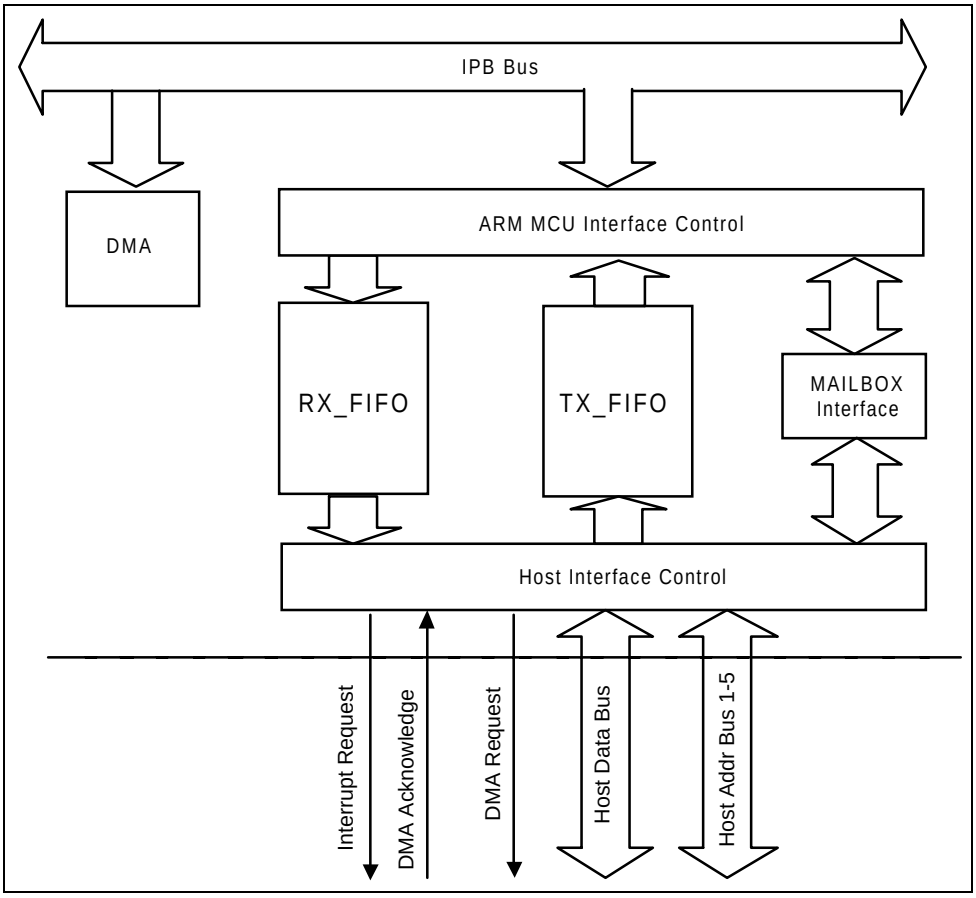

Figure 4-1. Host Interface Block Diagram

Table 4-1. Host Control, Status and I/O Registers

Host Bus Address	Register (READ)	Register (WRITE)
0x00	Host TX_FIFO Data	Host TX_FIFO Data
0x01	Host TX_FIFO Size	Host TX_FIFO Size
0x02	Host TX_FIFO Threshold (Low)	Host TX_FIFO Threshold (Low)
0x03	Host RX_FIFO Data	Host RX_FIFO Data
0x04	Host RX_FIFO Size	Reserved
0x05	Host RX_FIFO Threshold (High)	Host RX_FIFO Threshold (High)
0x06	Host FIFO Control [15:0]	Host FIFO Control [15:0]
0x07	Host FIFO Interrupt/Acknowledge [15:0]	Host FIFO Interrupt/Acknowledge [15:0]
0x08	Txmail0 [15:0]	Txmail0 [15:0]
0x09	Txmail1 [15:0]	Txmail1 [15:0]
0x0A	Txmail2 [15:0]	Txmail2 [15:0]
0x0B	Txmail3 [15:0]	Txmail3 [15:0] Host write to this register will cause an interrupt to the CSMV/3. CSMV/3 acknowledge of this interrupt will cause a corresponding interrupt to the Host
0x0C	Rxmail0 [15:0]	Reserved
0x0D	Rxmail1 [15:0]	Reserved
0x0E	Rxmail2 [15:0]	Reserved
0x0F	Rxmail3 [15:0] CSMV/3 write to this register (CSMV/3 address 0x10001DE) will cause an interrupt to the Host. The Host acknowledge of this interrupt will cause a corresponding interrupt to the CSMV/3.	Reserved

4.2 HOST INTERFACE DESCRIPTION

The CSMV/3 Host interface consists of two unidirectional 64x16 FIFOs, which allow the core processor in the CSMV/3 and an external processor (Host) to efficiently transfer data. The Host interface has the following features:

- Supports one wait state access on Host side.
- Supports 50 ns access speed on Host side.
- Supports DMA Request and Acknowledge signals on both the CSMV/3 and Host interfaces.
- Supports 8 bi-directional halfword mailboxes.
- Supports threshold and time-out features on DMA interface.

The interface consists of four major blocks:

- CSMV/3 interface control
- Host interface control
- Two FIFO blocks
- Mailbox interface.

For consistent orientation purposes, the transmit (TX) direction is from a Host computer to the PSTN (Public Switched Telephone Network) and the receive (RX) direction is from the PSTN to the Host computer (Figure 4-2). Relative to the RL56CSMV/3, TX data is received (read) from the Host and transmitted (written) to the data pump and RX data is received (read) from the data pump and transmitted (written) to the Host.

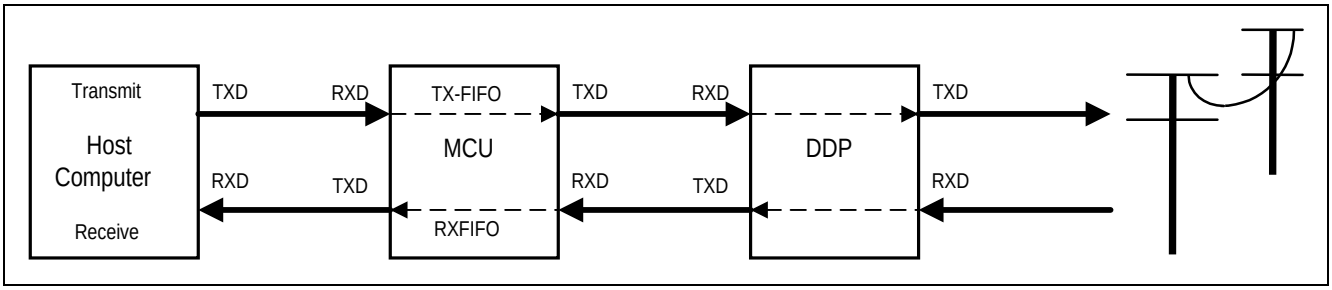

Figure 4-2. Reference Direction For Modem Data

4.2.1 Mailbox Interface

The mailbox interface consists of eight registers, all of which can be read or written by either the Host or the CSMV/3. The first four are TXMAIL0-TXMAIL3 and the second four are RXMAIL0-RXMAIL3. Normally, the TXMAIL registers are written by the Host and read by the CSMV/3, and the RXMAIL registers are written by the CSMV/3 and read by the Host. TXMAIL3 has a special feature such that a mailbox write interrupt request is triggered to the CSMV/3 processor when the Host writes to TXMAIL3. A mailbox acknowledge interrupt is asserted to the Host processor when the CSMV/3 acknowledges the TXMAIL3 interrupt, Similarly, the CSMV/3 writing to RXMAIL3 will interrupt the Host, and the Host acknowledge of that interrupt will trigger an interrupt to the CSMV/3.

4.2.2 Host FIFO Interface

The Host FIFO interface control section is used to control the access to the FIFO by the Host processor.

TX_FIFO Host Interface

The TX_FIFO Host interface consists of the following registers which are accessible by the Host:

TXFIFO DATA[15:0]	Used to write data into the FIFO. Reading this register returns last value written.
TXFIFO SIZE[15:0]	The current depth of the FIFO.
TXFIFO THRESHOLD	The low threshold value of the TX_FIFO. A TX_FIFO depth less than this value will cause an interrupt to occur to the Host if enabled. This value can also be used to control the external DMA request line. The DMA can be used to fill the FIFO. Once the FIFO is full the DMA request signal is de-asserted. If the DMA threshold feature is active, then the DMA request signal will not be reasserted until the CSMV/3 has removed enough data so that the depth of the FIFO is less than the low threshold. Once the DMA request is asserted, the DMA will completely fill the FIFO or empty the DMA buffer, whichever occurs first. Once the TX_FIFO is full the DMA request line will again be de-asserted.

RX_FIFO Host Interface

The RX_FIFO Host interface consists of the following registers:

RXFIFO DATA[15:0]	Used to read data from the FIFO. This register cannot be written.
RXFIFO SIZE[15:0]	The current depth of the receive FIFO.
RXFIFO THRESHOLD	The high threshold value of the RX_FIFO. Exceeding this value will cause an interrupt to occur to the Host if enabled. The interrupt cannot be cleared until sufficient data has been removed from the FIFO by the Host to cause the size to be less than the threshold. This value can also be used to control the external DMA request line. The DMA can be used to empty the RX_FIFO. Once the FIFO is empty the DMA request signal is de-asserted. If the DMA threshold feature is active, then the DMA request signal will not be re-asserted until the CSMV/3 has written enough data so that the depth of the FIFO is greater than the high threshold.

HOST FIFO CONTROL The Host FIFO control register contains control (enable) bits for the Host transmit and receive FIFO and the mailbox interface.

7	6	5	4	3	2	1	0
DMAMODE	RXDHE	HBRXRQ_EN	RXFF_EN	Reserved	TXDHE	HBTXRQ_EN	TXFF_EN

15	14	13	12	11	10	9	8
Reserved	RXM3IE	RXTHIE	RXFIE	DMABEIE	TXM3IE	TXTHIE	TXEIE

Bit 0	TXFF_EN	Enables TX_FIFO operation. The FIFOs are disabled on reset.
Bit 1	HBTXRQ_EN	Enables operation of HBRQSTW.
Bit 2	TXDHE	TX_FIFO DMA Hysteresis Enable.
Bit 3	Reserved	
Bit 4	RXFF_EN	Enables RX_FIFO operation. The FIFOs are disabled on reset.
Bit 5	HBRXRQ_EN	Enables operation of HBRQSTR. When disabled the output is low.
Bit 6	RXDHE	RX_FIFO DMA Hysteresis Enable.
Bit 7	DMAMODE	Enables one of two DMA modes. See following explanation.
Bit 8	TXEIE	TX_FIFO Empty Interrupt Enable.
Bit 9	TXTHIE	TX_FIFO Threshold Interrupt Enable.
Bit 10	TXM3IE	TXMAIL3 Interrupt Enable.
Bit 11	DMABEIE	Internal RX DMA Buffer Empty Interrupt Enable. Also, this condition will trigger the HBRQSTR signal without reaching the threshold.
Bit 12	RXFIE	RX_FIFO Full Interrupt Enable.
Bit 13	RXTHIE	RX_FIFO Threshold Interrupt Enable.
Bit 14	RXM3IE	RXMAIL3 Interrupt Enable.
Bit 15	Reserved	

DMAMODE = 0 (bit 7)

1. HBRQSTR is deasserted when the last word read by the Host empties the RX_FIFO.
2. HBRQSTW is deasserted when the last word written by the Host causes the TX_FIFO level to exceed the CSMV/3 TX_FIFO threshold(high) when hysteresis is enabled.
3. In this mode the action required to read or write the FIFOs is a toggle of the corresponding HBACKR#/HBACKW# signals.
4. Data may be read (or written) by toggling, at least one cycle on and one cycle off, the HBRD# (or HBWRP). Data may also be transferred by toggling the appropriate acknowledge signal.

DMAMODE = 1 (bit 7)

1. HBRQSTR is deasserted when two words remain to be read from the RX_FIFO.
2. HBRQSTW is deasserted when the last word written by the Host causes the TX FIFO level to equal two words less than the CSMV/3 TX_FIFO threshold(high) when hysteresis is enabled.
3. The CSMV/3 device will read or write one word of Host data every two HBCLK clock cycles as long as the associated acknowledge signal is active (low). The HBCS# and HBRD# or HBWR# are not required during the period the acknowledge signal is asserted. In this mode when reading the RX_FIFO, HBACKR# asserted, it is required that the HBEN# signal be asserted to enable the output drivers. HBEN# should be high during periods when HBACKW# is asserted.

HOST FIFO INT/ACK

This register contains FIFO status indicator bits as well as corresponding “acknowledge” bits. The Host writing to bits 8-15 will have no affect since these bits are set by FIFO logic. The FIFO interrupt acknowledge bits, 0-6, are used to clear the corresponding interrupt. Any or all bits may be acknowledged simultaneously. Writing a one to the corresponding interrupt acknowledge bit causes the status bit to be cleared and the corresponding interrupt deasserted if currently active. Writing a zero to any bit has no effect. Bit 7 is provided as an optional means of the Host causing the CSMV/3’s internal DMA to read the TX_FIFO. If the data level in the FIFO has not reached the CSMV/3 TX_FIFO Threshold, then setting this bit will cause the CSMV/3 internal DMA request signal to be asserted.

7	6	5	4	3	2	1	0
TXCMPLT	RXM3IAK	RXTHIAK	RXFIAK	DMABEAK	TXM3IAK	TXTHIAK	TXEIAK

15	14	13	12	11	10	9	8
Reserved	RXM3I	RXTH	RXF	DMABEI	TXM3I	TXTH	TXE

Bit 0	TXEIAK	Writing a “1” clears the corresponding interrupt status bit.
Bit 1	TXTHIAK	Writing a “1” clears the corresponding interrupt status bit.
Bit 2	TXM3IAK	Writing a “1” clears the corresponding interrupt status bit.
Bit 3	DMABEIAK	Writing a “1” clears the corresponding interrupt status bit.
Bit 4	RXFIAK	Writing a “1” clears the corresponding interrupt status bit.
Bit 5	RXTHIAK	Writing a “1” clears the corresponding interrupt status bit.
Bit 6	RXM3IAK	Writing a “1” clears the corresponding interrupt status bit.
Bit 7	TXCMPLT	Writing a “1” will set the CSMV/3 “threshold interrupt” status.
Bit 8	TXE	The TX_FIFO is empty.
Bit 9	TXTH	The TX_FIFO depth is less than the threshold value.
Bit 10	TXM3I	The CSMV/3 has acknowledged a TXM3 FULL Interrupt.
Bit 11	DMABEI	The DMA Buffer is empty.
Bit 12	RXF	The RX_FIFO is full.
Bit 13	RXTH	The RX_FIFO depth is greater than the threshold value.
Bit 14	RXM3I	The CSMV/3 has written data to the RXMAIL3 Register.
Bit 15	Reserved	

4.2.3 Host Bus Timing

Host Read

The host bus read timing is listed in Table 4-2 and illustrated in Figure 4-3.

To read, the Host first asserts the chip select HBCS#, HBA[5:1] and HBEN# to request the CSMV/3 Host bus. HBEN# must be asserted at least one cycle before the end of the HBRD# signal to turn on the data output drivers. The CSMV/3 will then output data on HBD[15:0]. The HBCS# or HBRD# must be deasserted for one cycle following a read operation before a subsequent read or write may occur.

Table 4-2. Timing - Host Read

Parameter	Symbol	Min	Max	Units
Clock Period	t_{CYC}	25		ns
Address to Data Valid	t_{AS}		20	ns
Address Hold	t_{AH}	2		ns
Chip Select to Data Valid	t_{CS}		20	ns
Chip Select Hold	t_{CH}	2		ns
Chip Select Pulse Width	t_{CSW}	t_{CYC}		ns
Bus Enable to Low Impedance	t_{EN}		14	ns
Bus Enable Hold	t_{ENH}	2		ns
Read Pulse to Data Valid	t_{DD}		20	ns
Read Pulse Hold	t_{RDH}	2		ns
Read Pulse Width	t_{RDW}	t_{CYC}		ns
Data Tristate Delay	t_{DZ}		5	ns
Test Conditions: VDD = 3.3 ± 0.3 VDC, TA = 0°C to 70°C, output load = 45 pF.				

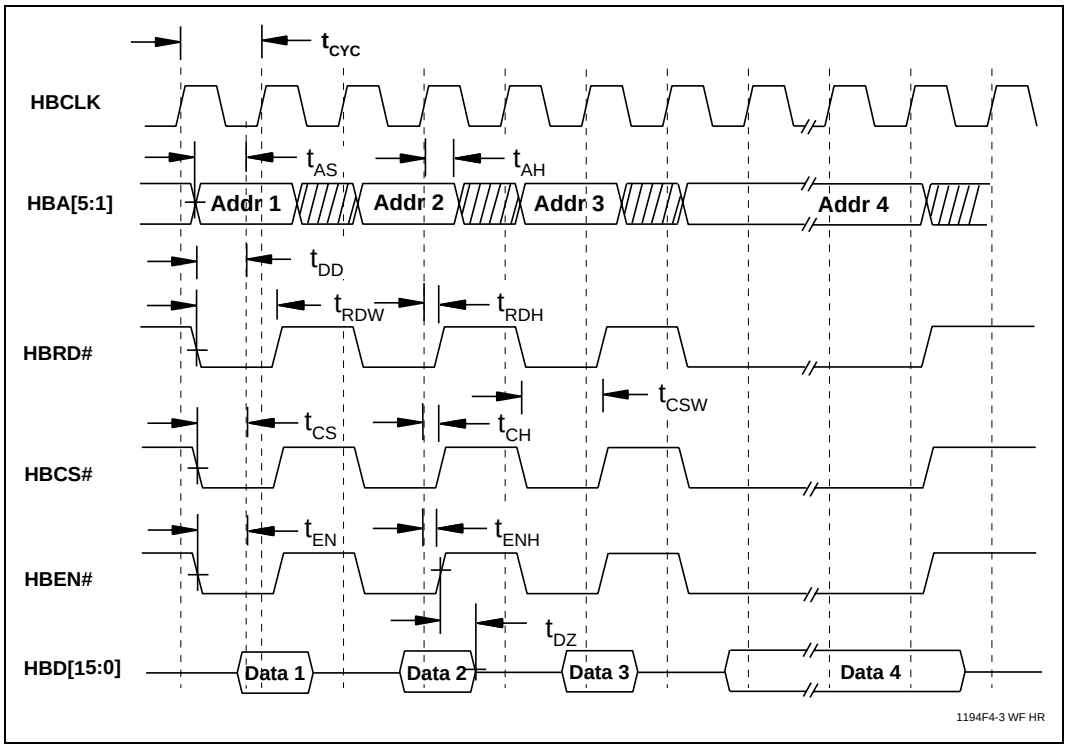

Figure 4-3. Waveforms - Host Read

Host Write

Host write timing is listed in Table 4-3 and illustrated in Figure 4-4.

Host writes are similar to the reads except that HBWR# is taken low, and the HBD[15:0] data is supplied by the Host. Data will be clocked into the CSMV/3 on the rising edge of the HBCLK. HBCS# or HBWR# must be deasserted for one cycle before a subsequent read or write can occur.

Table 4-3. Timing - Host Write

Parameter	Symbol	Min	Max	Units
Clock Period	t_{CYC}	25		ns
Address Valid to Clock Rising Edge	t_{AS}	20		ns
Address Hold	t_{AH}	2		ns
Chip Select to Clock Rising Edge	t_{CS}	20	t_{CYC} *	ns
Chip Select Hold	t_{CH}	2		ns
Write Pulse to Clock Rising Edge	t_{WR}	20	t_{CYC} *	ns
Write Pulse Hold	t_{WH}	2		ns
Data Valid to Clock Rising Edge	t_{DS}	18		ns
Data Write Hold	t_{DH}	2		ns

*The Host Chip Select or Write Pulse must be deactivated prior to the second rising edge of the clock to prevent latching the data bus a second time.

Test Conditions: VDD = 3.3 ± 0.3 VDC, TA = 0°C to 70°C, output load = 45 pF.

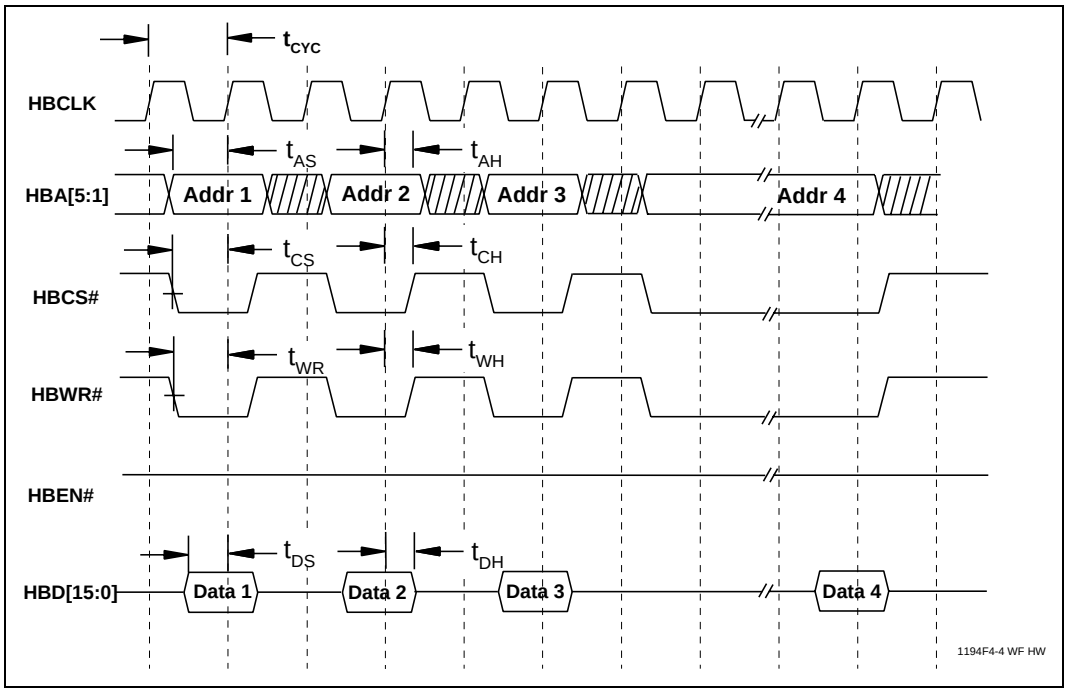

Figure 4-4. Waveforms - Host Write

4.2.4 Host Interface - DMA Demand Mode Timing

DMA Demand Mode is entered when the control bit DMAMODE is set. The DMAMODE = 1 setting selects a burst type of data transfer controlled by the host acknowledge signal. For this activity to occur it is necessary that the associated HBTXRQ_EN or HBRXRQ_EN be set (enabled). In this mode the action of asserting the HBACKR# (or HBACKW#) will:

1. Ignore the setting of the control and address signals, HBA[5:1], HBCS#, HBRD# (or HBWR#).
2. Data from the FIFO will be output on every other HBCLK cycle (note: the host data bus transfer rate cannot exceed 50 ns per word. Therefor the minimum HBCLK period cannot be less than 25 ns.
3. During the period when HBACKR# (or HBACKW#) is active, no other host registers may be accessed.

In systems with multiple CSMV/3s, the HBACKR#(or HBACKW#) signal can be bussed to all devices as long as only one device has its HBTXRQ_EN or HBRXRQ_EN enabled at any one time. Also, in DMAMODE = 1, the host should set the FIFO threshold value at the desired level and the “FIFO hysteresis mode” must be enabled.

Host DMA Demand Mode Read

The Host DMA Demand Mode read timing is shown in Figure 4-5.

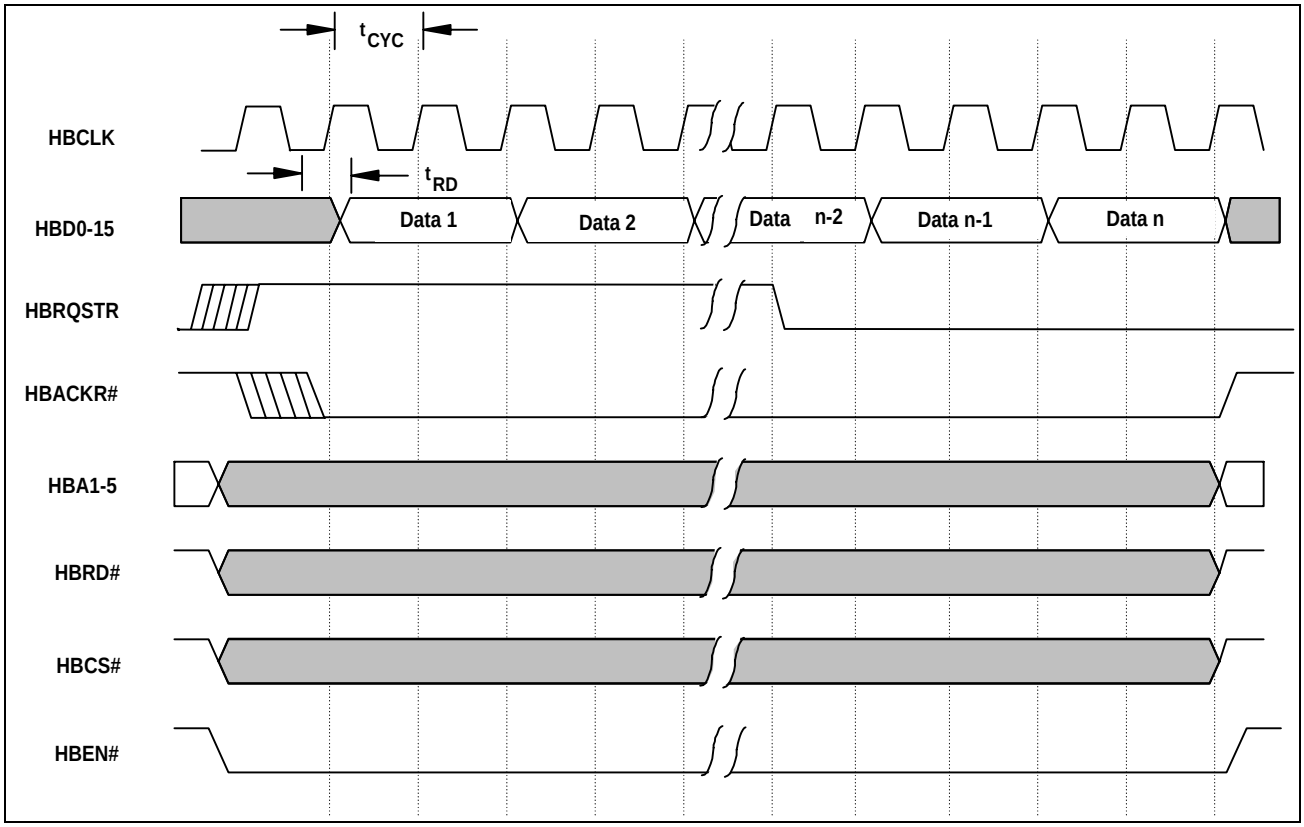

Figure 4-5. Host DMA Demand Mode Read, DMAMODE = 1

Host DMA Demand Mode Write

The Host DMA Demand Mode write timing is shown in Figure 4-6.

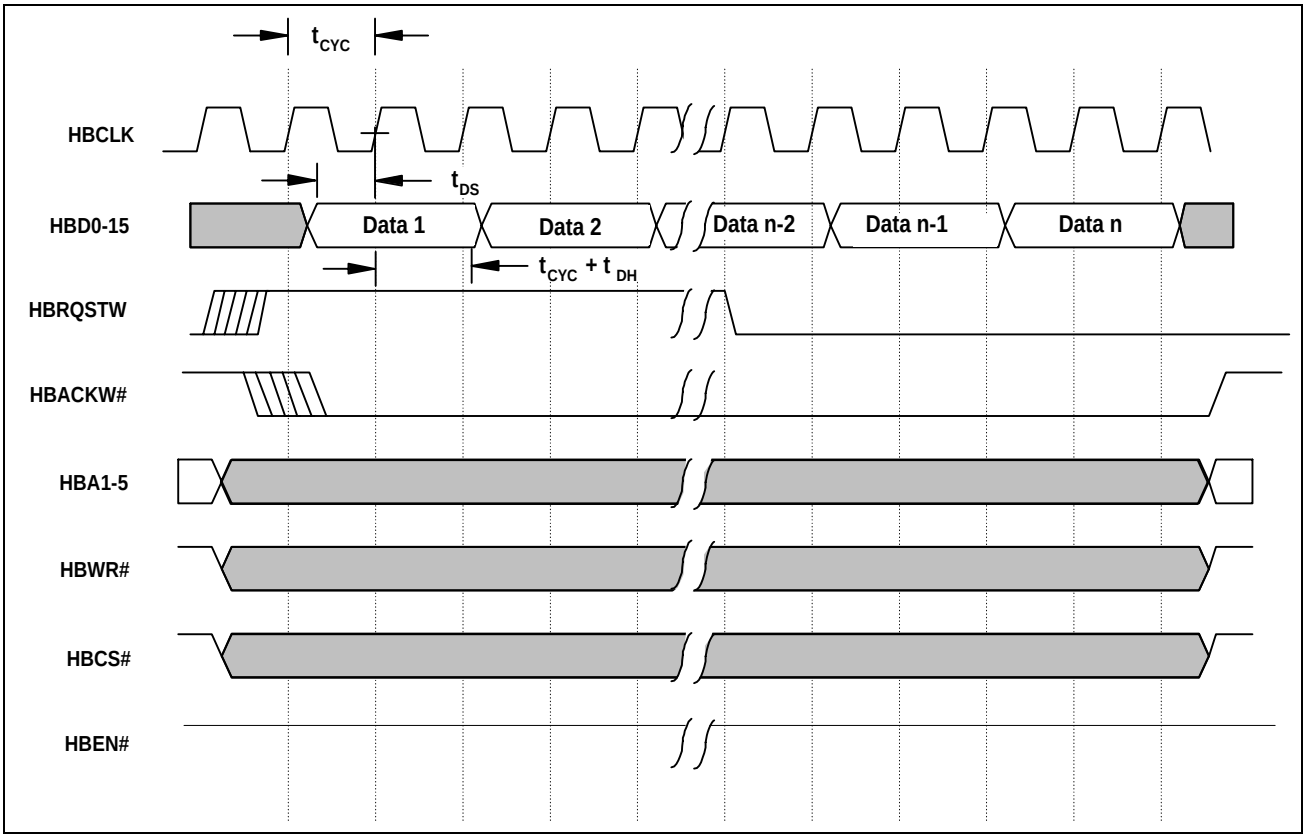

Figure 4-6. Host DMA Demand Mode Write, DMAMODE = 1

4.2.5 Host Interface Pin Summary

A summary of the CSMV/3 Host Interface inputs and outputs is shown in Table 4-4.

Table 4-4. Host Bus Interface Pin Description

Pin	Description	Function
HBA[5:1]	Host Bus Address	Input
HBD[15:0]	Host Bus Data	I/O
HBRD#	Host Bus Read Not - When low, the Host is reading data from the CSMV/3.	I
HBWR#	Host Bus Write Not - When low, the Host is writing data to the CSMV/3.	I
HBCS#	Host Bus Chip Select Not	I
HBCLK	Host Bus Clock	I
HBEN#	Host Bus Data Output Enable Not - Used in conjunction with HBRD# low or HBACKR# low. If HBEN# is low then HBD is active, if high then HBD is tri-stated.	I
HBIRQ#	Host Bus Interrupt Request - Interrupt from the CSMV/3 to the Host.	O
HBRQSTW	Host Bus Transmit DMA Request	O
HBACKW#	Host Bus Transmit DMA Acknowledge	I
HBRQSTR	Host Bus Receive DMA Request	O
HBACKR#	Host Bus Receive DMA Acknowledge	I

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5. DESIGN CONSIDERATIONS

Good engineering practices must be followed when designing a printed circuit board (PCB) containing the modem device. This is especially important considering the high data bit rate and high fax rate. Suppression of noise is essential to the proper operation and performance of the modem.

Two aspects of noise in an OEM board design containing the modem device set must be considered: on-board/off-board generated noise that can affect modem operation and on-board generated noise that can radiate off-board. Both on-board and off-board generated noise that is coupled on-board can affect interfacing signal levels and quality. Of particular concern is noise in frequency ranges affecting modem performance.

On-board generated electromagnetic interference (EMI) noise that can be radiated or conducted off-board is a separate, but equally important, concern. This noise can affect the operation of surrounding equipment. Most local governing agencies have stringent certification requirements that must be met for use in specific environments. In order to minimize the contribution of the circuit design and PCB layout to EMI, the designer must understand the major sources of EMI and how to reduce them to acceptable levels.

Proper PC board layout (component placement and orientation, signal routing, trace thickness and geometry, etc.), component selection (composition, value, and tolerance), interface connections, and shielding are required for the board design to achieve desired modem performance and to attain EMI certification.

All the aspects of proper engineering practices are beyond the scope of this designer's guide. The designer should consult noise suppression techniques described in technical publications and journals, electronics and electrical engineering text books, and component supplier application notes. Seminars addressing noise suppression techniques are often offered by technical and professional associations as well as component suppliers.

The following guidelines are offered to specifically help achieve stated modem performance and to minimize EMI generation.

5.1 PC BOARD LAYOUT GUIDELINES

5.1.1 General Principles

1. Keep high speed digital traces as short as possible.
2. Provide proper power supply distribution, grounding, and decoupling.
3. Provide separate digital ground and chassis ground (if appropriate) planes.
4. Provide wide traces for power and critical signals.
5. Position interface digital circuits near the corresponding host bus connection.

5.1.2 Component Placement

1. From the system circuit schematic,
   a) Identify the high speed digital circuits and their components, as well as external signal and power connections.
   b) Note the location of power and signals pins for each device (IC).
2. Once sections have been roughly defined, place the components starting with the connectors and jacks.
   a) Allow sufficient clearance around connectors and jacks for mating connectors and plugs.
   b) Allow sufficient clearance around components for power and ground traces.
   c) Allow sufficient clearance around sockets to allow the use of component extractors.
3. Place active digital components/circuits and decoupling capacitors.
   a) Place digital components close together in order to minimize signal trace length.
   b) Place 0.1 µF decoupling (bypass) capacitors close to the pins (usually power and ground) of the IC they are decoupling. Make the smallest loop area possible between the capacitor and power/ground pins to reduce EMI.
   c) Place crystal/clock circuits as close as possible to the devices they drive.

5.1.3 Signal Routing

1. Keep host interface signals (e.g., HBCS#, HBRD#, HBWR#, and RESET#) traces at least 10 mil thick (preferably 12 - 15 mil).

2. Keep all other signal traces as wide as possible, at least 5 mil (preferably 10 mil).Route the signals between components by the shortest possible path (the components should have been previously placed to allow this).
3. Route the traces between bypass capacitors to IC pins, at least 25 mil wide; avoid vias if possible.
4. Avoid right angle (90 degree) turns on high frequency traces. Use smoothed radiuses or 45 degree corners.
5. Minimize the number of through-hole connections (feedthroughs/vias) on traces carrying high frequency signals.
6. Keep all signal traces away from crystal/clock circuits.
7. Distribute high frequency signals continuously on a single trace rather than several traces radiating from one point.
8. Provide adequate clearance (e.g., 60 mil minimum) around feedthroughs in any internal planes.
9. Eliminate ground loops, which are unexpected current return paths to the power source.

5.1.4 Power

1. Identify digital power (VDD) supply connections.
2. Place a 10 µF electrolytic or tantalum capacitor in parallel with a ceramic 0.1 µF capacitor between power and ground at one or more points in the digital section. Place one set nearest to where power enters the PCB (edge connector or power connector) and place another set at the furthest distance from where power enters the PCB. These capacitors help to supply current surge demands by the digital circuits and prevent those surges from generating noise on the power lines that may affect other circuits.
3. For 2-layer boards, route a 200-mil wide power trace on two edges of the same side of the PCB around the border of the circuits using the power. (Note that a digital ground trace should likewise be routed on the other side of the board.)
4. Generally, route all power traces before signal traces.

5.1.5 Ground Planes

1. In a 2-layer design, provide digital ground plane areas in all unused space around and under digital circuit components on both sides of the board and connect them such a manner as to avoid small islands. Connect each ground plane area to like ground plane areas on the same side at several points and to like ground plane areas on the opposite side through the board at several points. Connect all modem DGND pins to the digital ground plane area.
2. In a 4-layer design, provide a digital ground plane covering the corresponding digital circuits. Connect all modem GND pins to the digital ground plane.
3. In a design which needs EMI filtering, define an additional “chassis” section adjacent to the bracket end of a plug-in card. Most EMI components (usually ferrite beads/capacitor combinations) can be positioned in this section. Fill the unused space with a chassis ground plane, and connect it to the metal card bracket and any connector shields/grounds.
4. Keep the current paths of separate board functions isolated, thereby reducing the current's travel distance. Separate board functions are: host interface, display, and digital (SRAM, EPROM, modem). Power and ground for each of these functions should be separate islands connected together at the power and ground source points only.
5. Connect grounds together at only one point, if possible, using a ferrite bead. Allow other points for grounds to be connected together if necessary for EMI suppression.
6. Keep all ground traces as wide as possible, at least 25 mil to 50 mil.
7. Keep the traces connecting all decoupling capacitors to power and ground at their respective ICs as short and as direct (i.e., not going through vias) as possible.

5.1.6 Clock Oscillator Circuit

1. Use +3.3 V oscillators with specified 45/55% duty cycle limits **– this is critical for MCU_CLKIN.**
2. Use care in PCB routing of MCU_CLKIN and MCU_CLKOUT signals. Minimize trace length, add terminations as required, and avoid impedance discontinuities to retain waveform integrity, i.e., maintain duty cycle, rise and fall times, and minimize undershoot and overshoot.
3. Maintain +3.3V supply within ± 10%.
4. Keep all traces and component leads connected to clock input and output pins short in order to reduce induced noise levels and minimize any stray capacitance that could affect the clock oscillator.
5. Allow for a series impedance matching resistor at the clock source, and a parallel terminating resistor at the clock inputs.

5.1.7 EMI Considerations for Standalone Modem Design

1. Use a metal enclosure.
2. If a plastic enclosure is required, internal metal foil lining the enclosure or conductive spray applied to the top and bottom covers may reduce emissions.

5.1.8 Optional Configurations

Because fixed requirements of a design may alter EMI performance, guidelines that work in one case may deliver little or no performance enhancement in another. Initial board design should, therefore, include flexibility to allow evaluation of optional configurations. These optional configurations may include:

1. Chokes that can replaced with jumper wires as a cost reduction if the design has sufficient EMI margin.
2. Various grounding areas connected by tie points (these tie points can be short jumper wires, solder bridges between close traces, etc.).
3. Cable ground wires or cable shielding connected on the board or floated.
4. Develop two designs in parallel; one based on a 2-layer board and the other based on a 4-layer board. During the evaluation phase, better performance of one design over another may result in quicker time to market.

5.1.9 DDP Specific

1. Provide a 0.1 µF ceramic decoupling capacitor to ground between the power supply and the VDD pins.

5.2 OSCILLATOR SPECIFICATIONS

Recommended surface-mount clock oscillator specifications are listed in Table 5-1.

Recommended through-hole clock oscillator specifications are listed in Table 5-2.

Table 5-1. Clock Oscillator Specifications - Surface Mount

Characteristic	Value	Value
Electrical		
Output Frequency	28.224 MHz	40.000 MHz nom.
Frequency Stability (Note 1)	±100 ppm (0°C to 70°C)	±100 ppm (0°C to 70°C)
Symmetry	45 / 55%	45 / 55%
Output Voltage	VDD max.	VDD max.
	2.4V min.	2.4V min.
Rise/Fall Time (Note 2)	6 ns max.	6 ns max. (Note 3)
Driving Ability	10 TTL load or 50 pF HCMOS load	10 TTL load or 50 pF HCMOS load
Start up Time	3 ms typ.	3 ms typ.
Supply Voltage	3.3V ± 0.3V	3.3V ± 0.3V
Supply Current (Note 4)	45 mA max.	50 mA max.
Storage Temperature	–55°C to 125°C	–55°C to 125°C
Mechanical		
Dimensions (L x W x H)	7.64 x 5.23 x 1.95 mm max.	7.64 x 5.23 x 1.95 mm max.
Mounting	SMT	SMT
Package	Ceramic (Leadless Chip Carrier)	Ceramic (Leadless Chip Carrier)
Suggested Suppliers		
	KDS America	KDS America
	ILSI America	ILSI America
	Vectron Technologies, Inc.	Vectron Technologies, Inc.

Notes:

1. Inclusive of calibration tolerance @ 25°C, over the operating temperature range, and aging.
2. Transition times are measured between 10% and 90% of Supply Voltage.
3. A transition time of 6 ns is acceptable if the clock buffer can supply the waveform shown in Figure 3-9.
4. Current consumption is typically 0.4 mA/MHz above 20 MHz frequencies.
5. Suggested suppliers:

   KDS America
   Fountain Valley, CA 92626
   (714) 557-7833

   ILSI America
   Kirkland, WA 98033
   (206) 828 - 4886

   Vectron Technologies, Inc.
   Lowell, NH 03051
   (603) 598-0074

Table 5-2. Clock Oscillator Specifications - Through Hole

Characteristic	Value	Value
Electrical		
Output Frequency	28.224 MHz	40.000 MHz nom.
Frequency Stability (Note 1)	±100 ppm (0°C to 70°C)	±100 ppm (0°C to 70°C)
Symmetry	45 / 55% max.	45 / 55% max.
Output Voltage	VDD max.	VDD max.
	2.4V min.	2.4V min.
Rise/Fall Time (Note 2)	6 ns max.	6 ns max. (Note 3)
Driving Ability	10 TTL load or 50 pF HCMOS load	10 TTL load or 50 pF HCMOS load
Start up Time	3 ms typ.	3 ms typ.
Supply Voltage	3.3V ± 0.3V	3.3V ± 0.3V
Supply Current (Note 4)	45 mA max.	45 mA max.
Storage Temperature	–55°C to 125°C	–55°C to 125°C
Mechanical		
Dimensions (L x W x H)	13.2 x 13.2 x 5.0 mm max.	13.2 x 13.2 x 5.0 mm max.
Mounting	Through Hole	Through Hole
Package	Half Size 8-Pin DIP	Half Size 8-Pin DIP

Notes:

1. Inclusive of calibration tolerance @ 25°C, over the operating temperature range, and aging.
2. Transition times are measured between 10% and 90% of Supply Voltage.
3. A transition time of 6 ns is acceptable if the clock buffer can supply the waveform shown in Figure 3-9.
4. Current consumption is typically 0.4 mA/MHz above 20 MHz frequencies.
5. Suggested suppliers:

   KDS America
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   ILSI America
   Kirkland, WA 98033
   (206) 828 - 4886

   Vectron Technologies, Inc.
   Lowell, NH 03051
   (603) 598-0074

5.3 PACKAGE DIMENSIONS

Package dimensions are shown in Figure 5-1.

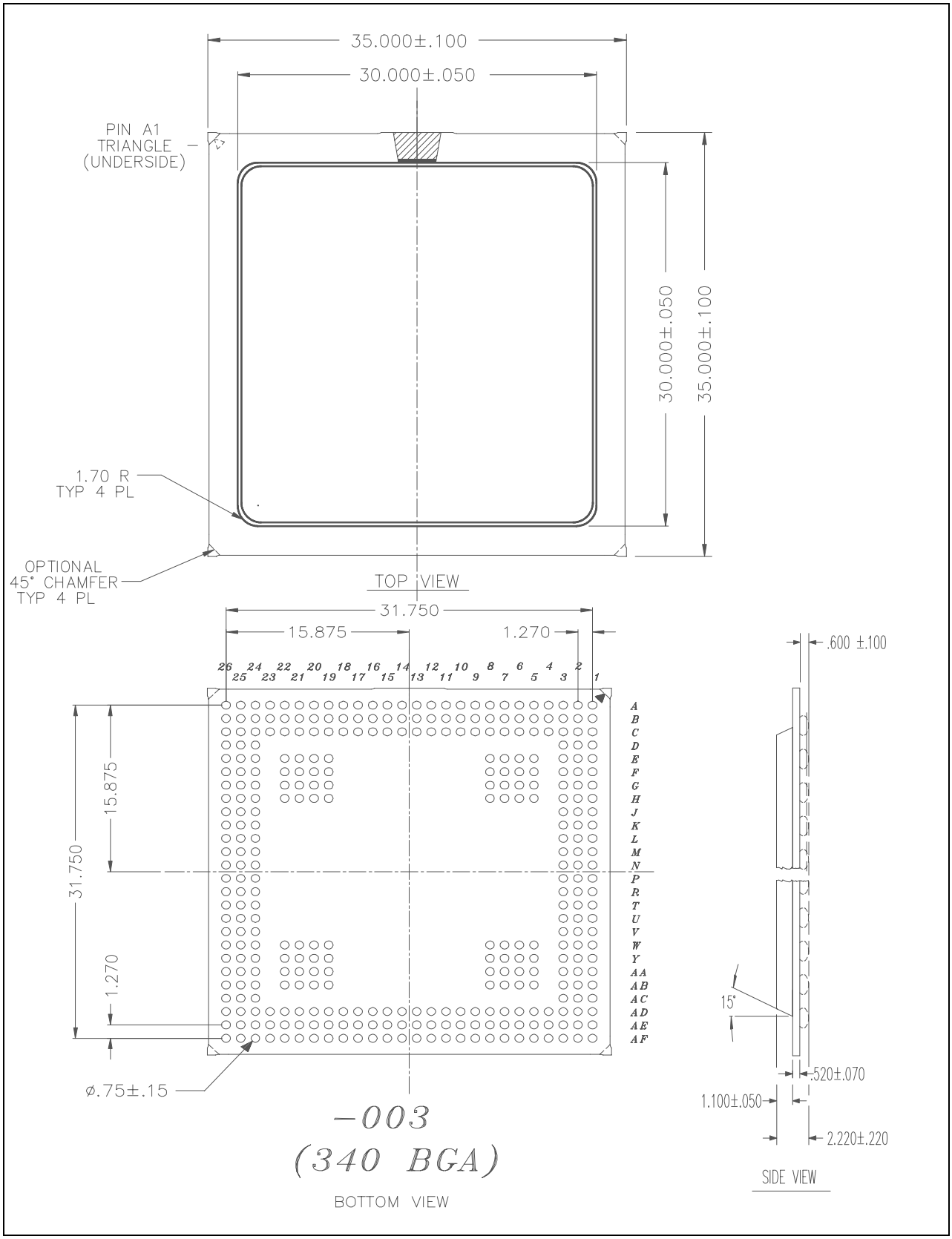

Figure 5-1. Package Dimensions - 340-Pin BGA

5.4 PLASTIC BGA HANDLING AND USE

5.4.1 Handling

Plastic BGA (PBGA) packages are more robust than quad flat pack (QFP) packages. Touching or knocking the solder ball will not cause a bent solder ball. As with all packages, the devices should be treated as electrostatic damage (ESD) sensitive and the solder contacts shall be kept clean from dirt or oils. PBGAs are typically transported and protected in trays and dry packed for moisture protection

5.4.2 Circuit Card Design

Circuit boards designed for PBGA packages should adhere to the following guidelines.

Solder Pad Design

Plated through holes must not be placed in the pad which is intended to attach a solder ball. This will cause the solder to wick inside the hole and produce misformed balls and electrical opens. Instead any plated through holes should be placed away from the attach pad. Tenting the via will prevent misaligned balls from wicking into the via. Plugging the vias further prevents solder ball wicking as well as trapped flux contamination.

Solder mask defined (SMD) pads or non-solder mask defined (NSMD) pads are both suitable pad designs (see Figure 5-2). Typical SMD design has a copper pad 30 mils (0.76 mm) diameter with a solder mask opening of 25 mils (0.63 mm). For routing escape, NSMD designs have a copper pad of 25 mils (0.63 mm) down to 20 mils (0.51 mm) with the solder mask opening 5 mils (0.13 mm) larger than the copper pad. NSMD pads provide easy X-ray inspection of the solder ball wetting to the pad tail and have excellent thermal cycle fatigue life. NSMD pads, however, have less strength than SMD pads and may not be suitable for boards which undergo significant bending or twisting.().

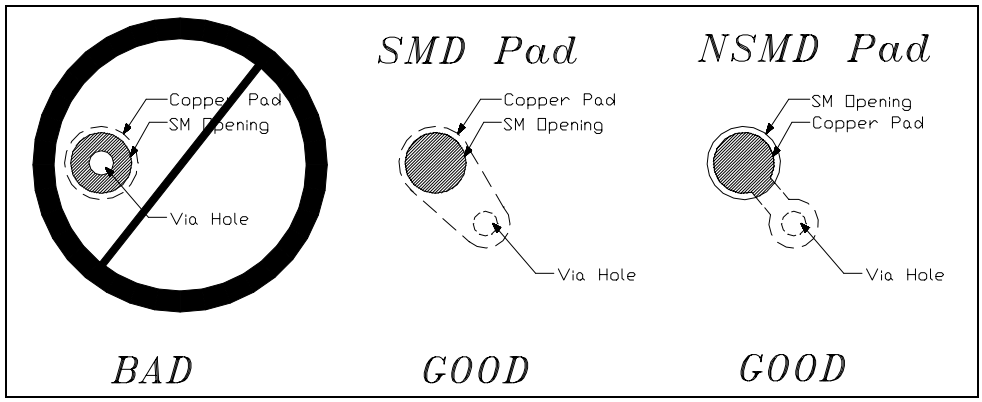

Figure 5-2. Plated Hole Placement Guideline for Connection to BGA Ball

PBGA Placement Design

PBGA packages should be placed on the printed circuit board with manufacturability in mind. If a PBGA is to be removed, it is usually done with a hot air nozzle. Some spacing (50 mils minimum) should be allowed between adjacent devices. If components are wave soldered, these devices should be placed away from the PBGA to prevent the wave from reflowing or washing away the solder balls. If the PBGA is mount on top, plated-through-holes under the PBGA should be tented or plugged before bottom side wave soldering.

5.4.3 Solder Reflowing

Solder Pad Preparation

Ball attach pads most often have solder paste screen printed or stenciled for reflow preparation. Paste application is most popular using stencils with 6 mil to 8 mil thicknesses and 20 to 25 mil openings. In addition, PBGAs can be assembled with flux only (no solder paste is required). No-clean paste or flux is most popular, although rosin and water soluble fluxes are also usable.

Temperature Profiling

When establishing a reflow profile, it is necessary to monitor the temperature of each PBGA location on the circuit board as well as across the individual PBGAs. A good technique for measuring PBGA temperature is to drill several small holes

through the top of the package just to the solder balls. Insert thermocouples into these hole. Then, fill the holes and tack down the wires with epoxy. Thermocouples should be placed above outer corner balls (typically the hottest) and the most inner balls (typically the coolest).

Ideal reflow profiles should be developed around the solder paste or flux. Typically profiles elevate the PBGA above the tin-lead liquidus temperature of 183°C for 60 seconds and a peak temperature between 205°C and 220°C. Solder ball temperatures above 230°C create higher risks for popcorn delamination.

Full convection forced air furnaces provide the most uniform temperature, however, infrared or vapor phase systems can be used. Nitrogen gas is not required but can be used to improve yields in cases of poor printed circuit board wettability or process enhancement. If a hot air nozzle is used to attach the PBGA, heat the entire circuit board with a secondary hot plate or hot air during the reflow process. Preheating the entire board will make the PBGA attach process much faster and minimize thermal shock to the package and circuit board.

Placement

Due to the "self alignment" nature of PBGAs, placement accuracy can be as coarse as $\pm$ 12 mils or greater and still have the package reflow into position. For greatest accuracy, package placement should be referenced off of the solder balls. This can be performed with standard bottom side vision systems which align the solder balls to the pads or with a simple nesting plate which keys off the solder balls. Referencing off of the PBGA body is also suitable.

5.4.4 Inspection

Due to the robust nature of PBGA solder reflow, in-line inspection is not required for production assembly. If uniform reflow temperature is maintained and outer solder joints look good, the internal joints will be good. Standard two-dimensional X-rays are extremely useful when initially characterizing a soldering process or trouble shooting electrical failures. X-rays often determine that electrical failures blamed on the PBGA are really caused by other components.

5.4.5 Rework and Removal

Precaution must be used when removing moisture sensitive PBGA packages or non BGA packages close to the rework site. If the board contains moisture sensitive packages near the rework location, the entire board should be baked at least 12 hours at 125°C prior to any rework.

PBGA rework is most commonly performed with hot air rework stations. The most effective stations provide bottom side preheating (for the entire circuit board) and a programmable temperature/time profile. After a PBGA is removed, excess solder will remain on the circuit board and the package balls will be destroyed. This excess solder on the board must be removed to prepare the solder pads. A solder vacuum tool works best to prevent damaged pads usually caused with solder wicks or excessively hot soldering irons. After the pads are cleaned, the same flux as was used during the initial soldering should be applied to the pads. The new PBGA should then be aligned on the pads and reflowed using the same hot air profile.

As with any PBGA, care must be take never to touch or push down of the package while the solder balls are molten. This action will cause the balls to squash and bridge with adjacent balls. Removed PBGAs may either be reballed for reuse (if determined good) or scrapped.

5.4.6 Moisture

PBGAs are considered to be moisture sensitive and require baking and sealing in a bag called “dry pack”. If packages are allowed to absorb moisture, then they risk “popcorning” or cracking during solder reflow. Standard moisture ratings for PBGA packages (“Level 4”) recommend devices be assembled within 72 hours after they are removed from the dry pack bag. If this time is exceeded, then the parts should be baked at least 12 hours at 125°C prior to assembly.

5.4.7 References

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INSIDE BACK COVER NOTES

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