HD63485

Graphic Memory Interface Controller (GMIC)

Description

The HD63485 LSI belongs to the ACRTC (advanced CRT controller) family. It provides memory access control to frame buffers for graphic display and drawing. Incorporating bus driver circuits and a DRAM (dynamic RAM) interface, the GMIC allows direct connection to DRAM with no external circuits. Its main function include address data latch, DRAM row and column address multiplexing, supplying $\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$, $\overline{WE}$, and other signals, and generating the 2CLK signal for the ACRTC. Using the Hi-BiCMOS process, the HD63485 achieves high speed memory access with low power dissipation.

Features

- Drives frame buffer memory directly ($I_{OL} = 24$ mA max)
- Generates DRAM signal : row and column addresses, $\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$, $\overline{WE}$, etc
- High-speed dot rate input (64 MHz max)
- Direct ACRTC interface
- Generates horizontal scrolling control signals
- Generates load signals for horizontal smooth scrolling
- Programmable address incerment mode
- Generates 2CLK signal
- TTL-compatible input output
- Single + 5 V power supply
- Low power dissipation

Type of Products

Part No.	Speed	Package
HD63485PS32	32MHz	64-pin Plastic Shrink DIP
HD63485PS48	48MHz	(DP-64S)
HD63485PS64	64MHz	
HD63485CP32	32MHz	68-pin PLCC
HD63485CP48	48MHz	(CP-68)
HD63485CP64	64MHz	

Pin Description

Figure 1 shows the pin arrangement for the 64-pin shrink-type DIP and the 68-pin PLCC packages. Pins marked with * are bus drivers, which can handle a maximum output current I_{OL} of 24mA. Table 1 describes the pins.
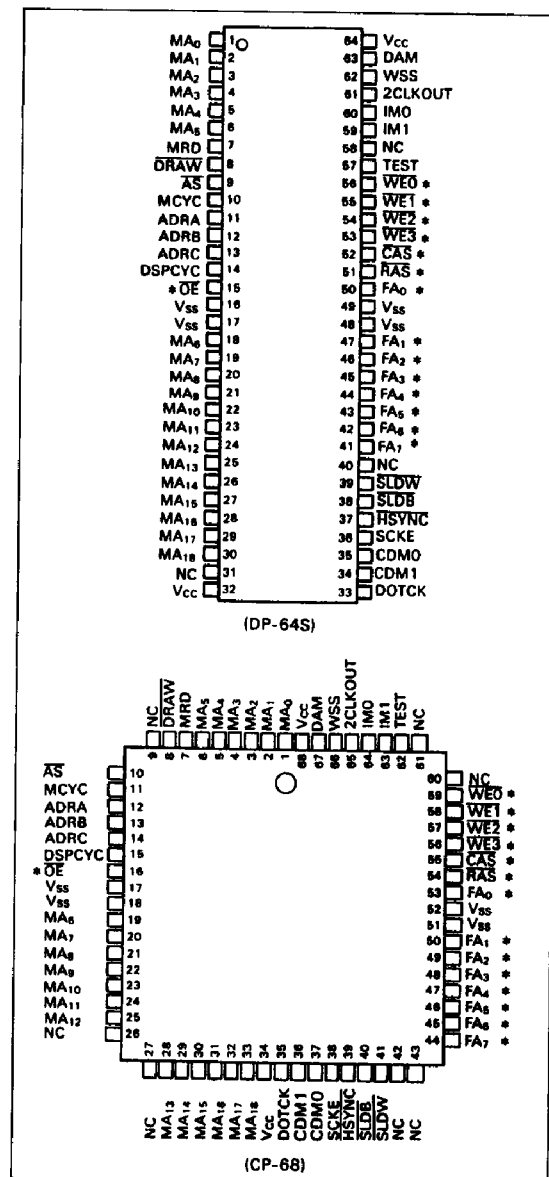

Figure 1. Pin Arrangement

Memory Cycle (MCYC): The MCYC input indicates the ACRTC's frame buffer access timing. MCYC is low when the ACRTC is in the address cycle, and high when the ACRTC is in the data cycle.

Draw ($\overline{\text{DRAW}}$): The $\overline{\text{DRAW}}$ input indicates whether the ACRTC memory cycle is a drawing cycle. $\overline{\text{DRAW}}$ is low during drawing cycle, and high otherwise. The GMIC uses $\overline{\text{DRAW}}$ to recognize display cycles, and also to generate DRAM control signals ($\overline{\text{WE 3}}$-$\overline{\text{WE 0}}$).

Memory Read (MRD): The MRD input controls data transfer between frame buffers and the ACRTC. The ACRTC pulls MRD high when it reads data from the frame buffer, and low when it writes data.

The only exception is when the ACRTC is in superimpose display mode (dual access mode 1). In superimpose display mode, the ACRTC inputs a low level and reads data from a frame buffer in order to indicate that the display cycle is for a superimposed screen (window screen).

Address Storbe ($\overline{\text{AS}}$): The $\overline{\text{AS}}$ input is a latch timing signal for the memory address sent from the ACRTC. Additionally, $\overline{\text{AS}}$ indicates whether memory is begin accessed. For example, for horizontal zooming, the $\overline{\text{SLDB}}$ signal is provided at a lower frequency, corresponding to the lower frequency of $\overline{\text{AS}}$.

Memory Address Bus (MA_{18}-MA_0): The MA_{18}-MA_0 inputs are address signals for frame buffer access, provided by the ACRTC.

Horizontal Sync ($\overline{\text{HSYNC}}$): The $\overline{\text{HSYNC}}$ input is a DRAM refresh cycle control signal to horizontally synchronize CRT displays. The GMIC performs $\overline{\text{RAS}}$ only refresh when $\overline{\text{HSYNC}}$ is low and $\overline{\text{DRAW}}$ is high when $\overline{\text{AS}}$ pulses are input.

Setting $\overline{\text{HSYNC}}$ low informs the GMIC of the end of a raster display. Usually, the ACRTC's $\overline{\text{HSYNC}}$ output supplies this input.

Frame Buffer Access Signals

Row Address Strobe ($\overline{\text{RAS}}$): The GMIC outputs the DRAMs' $\overline{\text{RAS}}$ timing signal on the $\overline{\text{RAS}}$ output.

Column Address Strobe ($\overline{\text{CAS}}$): The GMIC outputs the DRAMs' $\overline{\text{CAS}}$ timing signal on the $\overline{\text{CAS}}$ output.

Write Enable ($\overline{\text{WE 3}}$-$\overline{\text{WE 0}}$): The GMIC outputs the DRAM's $\overline{\text{WE}}$ timing signals on the $\overline{\text{WE}}$ outputs. Since $\overline{\text{WE 3}}$-$\overline{\text{WE 0}}$ are controlled by the incerment mode (IM 1, IM 0) and by the lower two bits of the

address (MA 1, MA 0), the GMIC can directly control up to four memory banks. Up to eight memory banks can be controlled by externally decoding the address (ADRC) and $\overline{\text{WE 3}}$-$\overline{\text{WE 0}}$.

$\overline{\text{WE 3}}$-$\overline{\text{WE 0}}$ are bus driver that can handle a maximum output current I_{OL} of 24 mA.

Output Enable ($\overline{\text{OE}}$): The GMIC outputs the DRAMs' output timing signal on the $\overline{\text{OE}}$ output. $\overline{\text{OE}}$ is a bus driver that can handle a maximum output current I_{OL} of 24 mA.

Frame Buffer Address (FA 7-FA 0): The GMIC outputs the multiplexed DRAM address on FA 7-FA 0. How the address is multiplexed depends on the incerment mode (table 4). FA 7-FA 0 are bus drivers that can handle a maximum output current I_{OL} of 24 mA.

Address (ADRA-ADRC): The GMIC latches three address bits other than those delivered on the FA 7-FA 0 bits and outputs them on ADRA-ADRC in one memory cycle.

GVAC Control Signals

Shift Clock Enable (SCKE): The SCKE output controls the GVACs' video signal generation shift register. It outputs a control signal for zooming according to the horizontal zoom signal (attribute control signal) from the ACRTC. The GVAC performs horizontal zoom by halting the clock when SCKE is low.

Shift Load Signals ($\overline{\text{SLDB}}$, $\overline{\text{SLDW}}$): The $\overline{\text{SLDB}}$ and $\overline{\text{SLDW}}$ outputs are load signals for the display data of the video signal generation shift register. The $\overline{\text{SLDB}}$ output is used for single access mode, dual access mode 0, and dual access mode 1. The $\overline{\text{SLDW}}$ output controls the window screen in dual access mode 1.

Display Cycle (DSPCYC): The DSPCYC output indicates whether a memory cycle is a display cycle.

DSPCYC is high during display cycle, and low otherwise.

$\overline{\text{AS}}$	$\overline{\text{DRAW}}$	MRD	cycle mode	memory cycle	DSPCYC
	L	L	Drawing Write	Memory Write	L
⊓⌐	L	H	Drawing Read	Memory Read	L
Low	H	L	Window Screen Display	Memory Read	H
pulse	H	H	Backscreen Display	Memory Read	H
H	x	x	—	No Access	L

HD63485

Functional Description

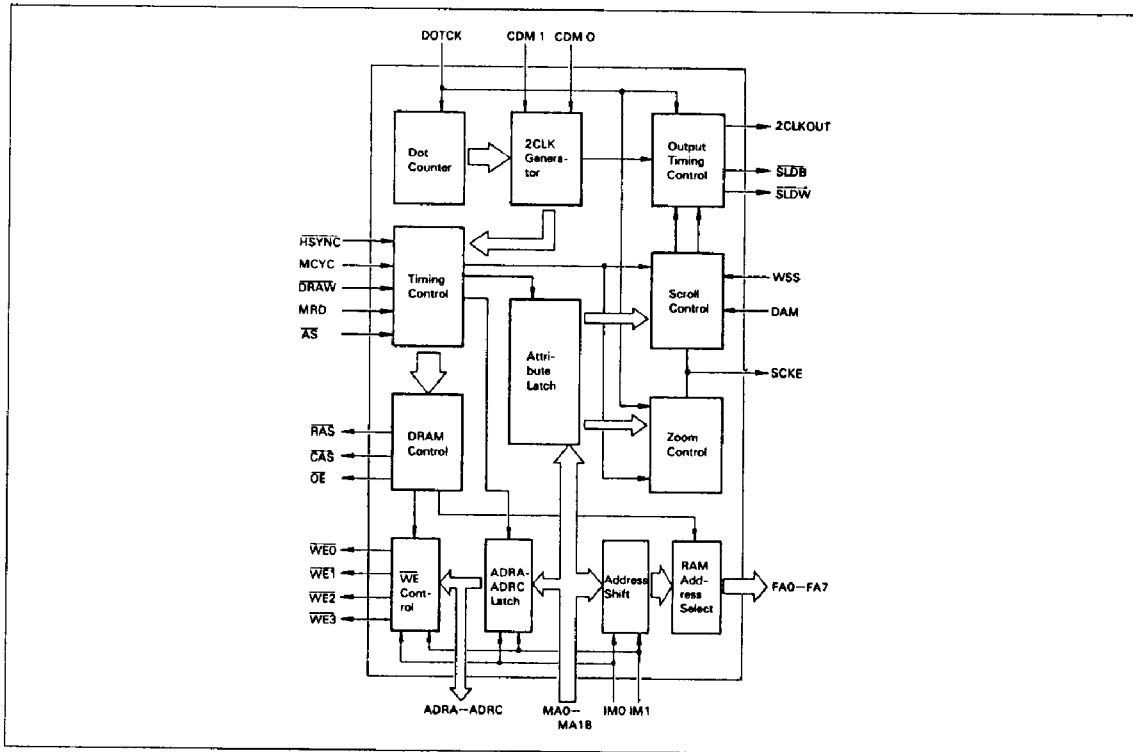Figure 2 is a block diagram of the HD63485.

Figure 2.   GMIC Block Diagram

2CLK Generator

The 2CLK generator generates 2CLKOUT for the ACRTC and itself by dividing the external DOTCK signal. The ratio of DOTCK to 2CLKOUT is set externally by the CDM 1 and CDM 0 inputs.

Attribute Latch

The attribute latch temporarily stores the attribute codes input from the ACRTC on MA 18-MA 0 used for horizontal zoom (HZ 3-HZ 0) and horizontal scroll dot (HSD 3-HSD 0).

Zoom Control

Zoom control generates the SCKE signal from DOTCK to control the GVAC clock for horizontal display zooming.

Scroll Control

Scroll control generates shift load signals (SLDB, SLDW) which control video signal generation for the GVAC.

Address Shifter

The address shifter stores memory addresses (MA 18-MA 0) sent from the ACRTC. It supplies them to the RAM address section according to the timesharing mode selected by the graphic increment mode (IM 1, IM0).

ADRA-ADRC Latches

The ADRA-ADRC latches store the lower or upper address bits which are not supplied to FA 7-FA 0 from the memory address sent from the ACRTC. It outputs them for the whole memory cycle.

RAM Address Selection

The RAM address selection circuits output the timeshared row and column addresses to the frame buffers according to the $\overline{RAS}$ and $\overline{CAS}$ timing.

DRAM Control and $\overline{WE}$ Control

The DRAM and $\overline{WE}$ control circuits generate $\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$, and $\overline{WE}$ signals for frame buffer access from the ACRTC output signals.

System Description

Applications

The GMIC provides communications between the ACRTC and frame buffers. It contains control circuits for generating signals necessary for the ACRTC to access a frame buffer. In addition it generates basic signals for operating the ACRTC and control signals for the GVAC (graphic video attribute controller), which generates the video signals for a CRT display.

The GMIC's operation mode can be controlled by it program pins. This makes the GMIC suitable for a wide range of operations, from small, low-speed systems to large, high-speed systems, and it allows it to flexibly change to suit system specification changes.

Figure 3 shows a graphic system configuration using an ACRTC, GMIC, and GVACs. Using a GMIC for interface to the frame buffers and a GAVCs for CRT video signal generation creates a flexible, high-performance graphic system with a minimum component count.

System Configuration

The typical graphic system application for the GMIC and GVAC shown in figure 3 uses two GVACs, but the number of GVACs used can be changed to accommodate CRT resolution and colorigrey scale per pixels for various applications.

The GMIC receives memory addresses (MAD$_{15}$-MAD$_0$, MA$_{18}$-MA$_{16}$), address strobe ($\overline{AS}$), memory cycle (MCYC), draw ($\overline{DRAW}$), memory read ($\overline{MRD}$), and other ACRTC outputs, and generates control signals for the frame buffers. The frame buffers are generally constructed from DRAM, since graphic systems require large memory capacity frame buffers. The GMIC therefore uses a DRAM-compatible multiplexing system. Through this multiplexing, the GMIC delivers address outputs and control signals such as $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and $\overline{OE}$, acting as a direct interface between the ACRTC and the frame buffers. Furthermore, the GMIC generates a basic clock signal for the ACRTC (2CLK) by dividing the high-speed dot clock. It also generates control signals for the GVAC.
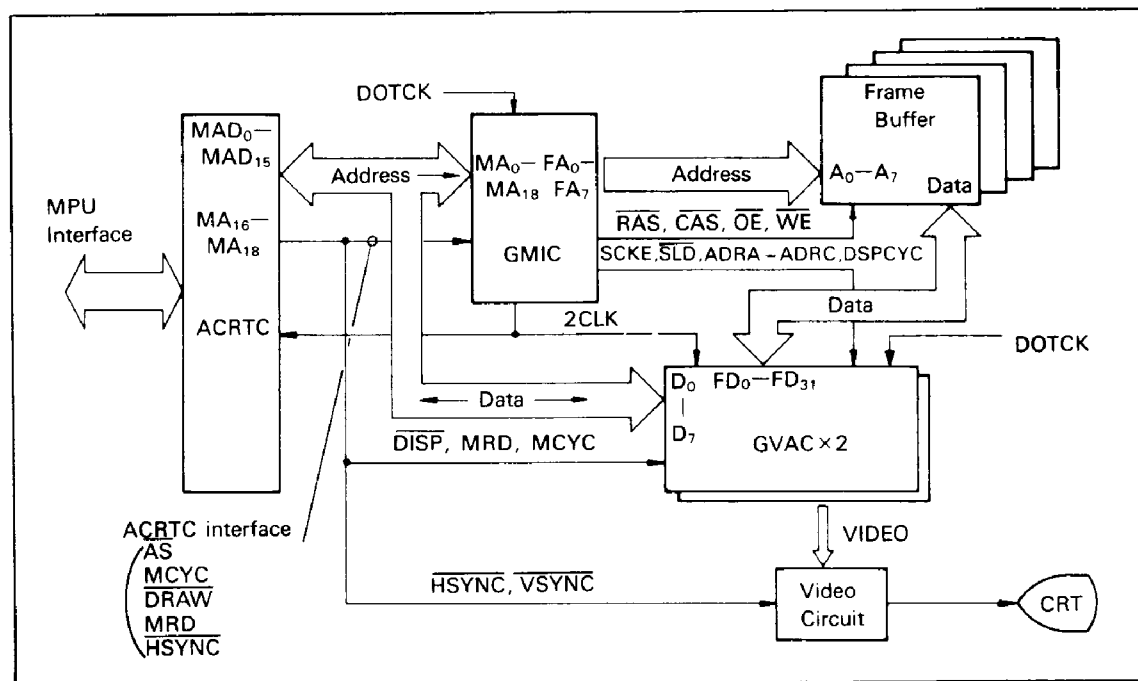
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Figure 3.   System Application Example

Operation

Basic Clock

Timing for signals to and from the GMIC is based on the dot clock (DOTCK) supplied to the GMIC and the clock output (2CLKOUT) generated by the GMIC. 2CLKOUT is generated by dividing the DOTCK input by the ratio selected by the CDM 1 and CDM 0 inputs. Figure 4 shows the relation between DOTCK and 2CLKOUT. The frequency of DOTCK depends on the speed and resolution of the CRT display. DOTCK (in MHz) equals the horizontal resolution (pixels/raster line) by the horizontal display raster scan period (μs per raster).

$f_{DOTCK} = [\text{Horizontal resolution (pixels/raster)}]/[\text{Horizontal display period}(\mu\text{s})]$ (MHz)

The dot clock dividing mode should be chosen considering the frame buffer cycle time and the speed of the ACRTC used. For high-speed drawing, a smaller division ratio should be used to supply a higher frequency chock to the ACRTC. For applications using low-speed frame buffers and extermal circuits, larger division rations should be selected to supply a lower frequency clock to the ACRTC.

Note : The maximum DOTCK frequency is sometimes limited by the DOTCK division ratio. If the division ratio is 8 or 16, the maximum frequency is allowed, but if a division ratio of 4 is used, the DOTCK frequency is limited to 32 MHz.

Frame Buffer Control

The GMIC is designed for use with DRAM frame buffer memories. Therefore, the GMIC generates DRAM access signals $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, and $\overline{\text{OE}}$. Also, it outputs row and column addresses to the RAM, timeshared according to $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.

Table 5 shows the GMIC frame buffer access modes. The memory cycles are roughly divided into six types. They are distinguished by the ACRTC's
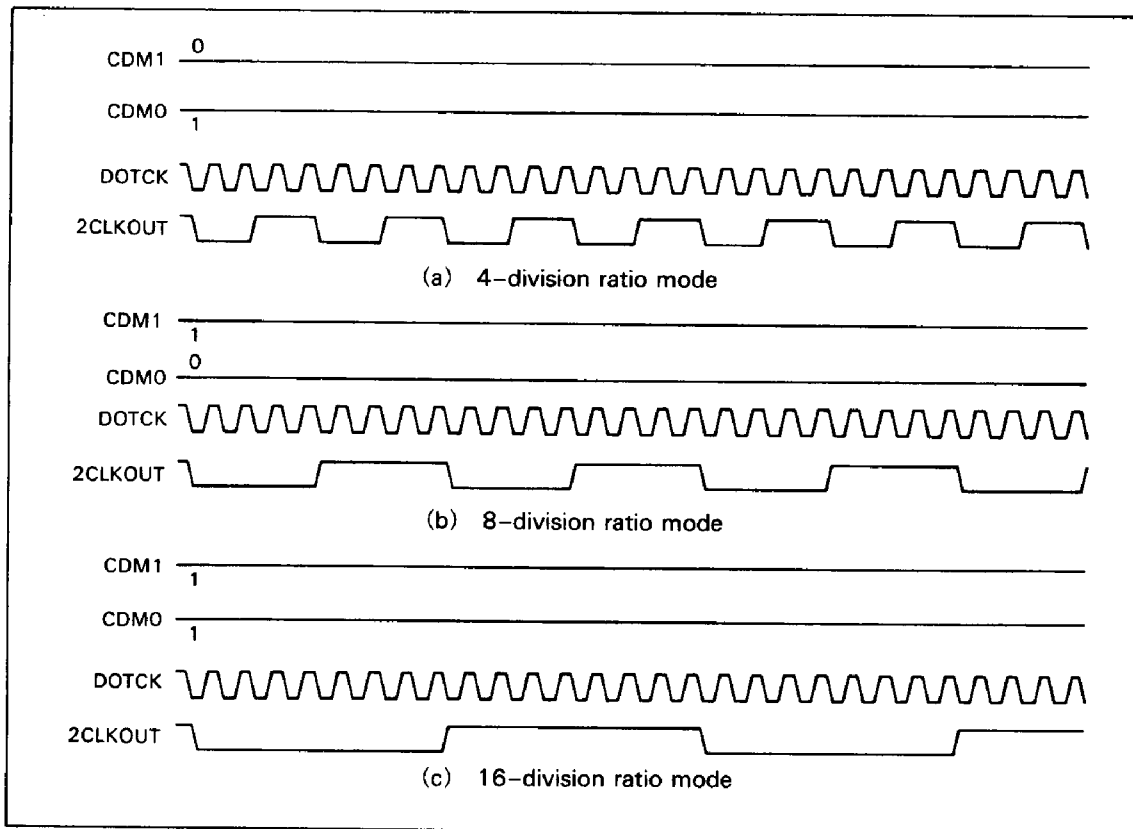

(a) 4-division ratio mode

(b) 8-division ratio mode

(c) 16-division ratio mode

Figure 4. DOTCK Division

output signals (AS, HSYNC, DRAW, MRD).
Figure 5 shows RAS only refresh cycle timing.

Figure 6 and 7 show read and write cycle timing, respectively.

Table 5. Memory Cycles

AS	HSYNC	DRAW	MRD	Cycle Mode	Memory Cycle
Low pulse	Low	High	High	Refresh cycle	RAS only refresh
		Low	Low	Drawing write cycle	Memory write
		Low	High	Drawing read cycle	Memory read
	High	High	Low	Window screen cycle	Memory read
		High	High	Background screen display	Memory read
High		High	High		No access

Note : The GMIC performs a frame buffer refresh during a horizontal sync period (HSYNC=low), with DRAW high and AS pulse applied. During a refresh cycle, only RAS is output. CAS and OE are not output.
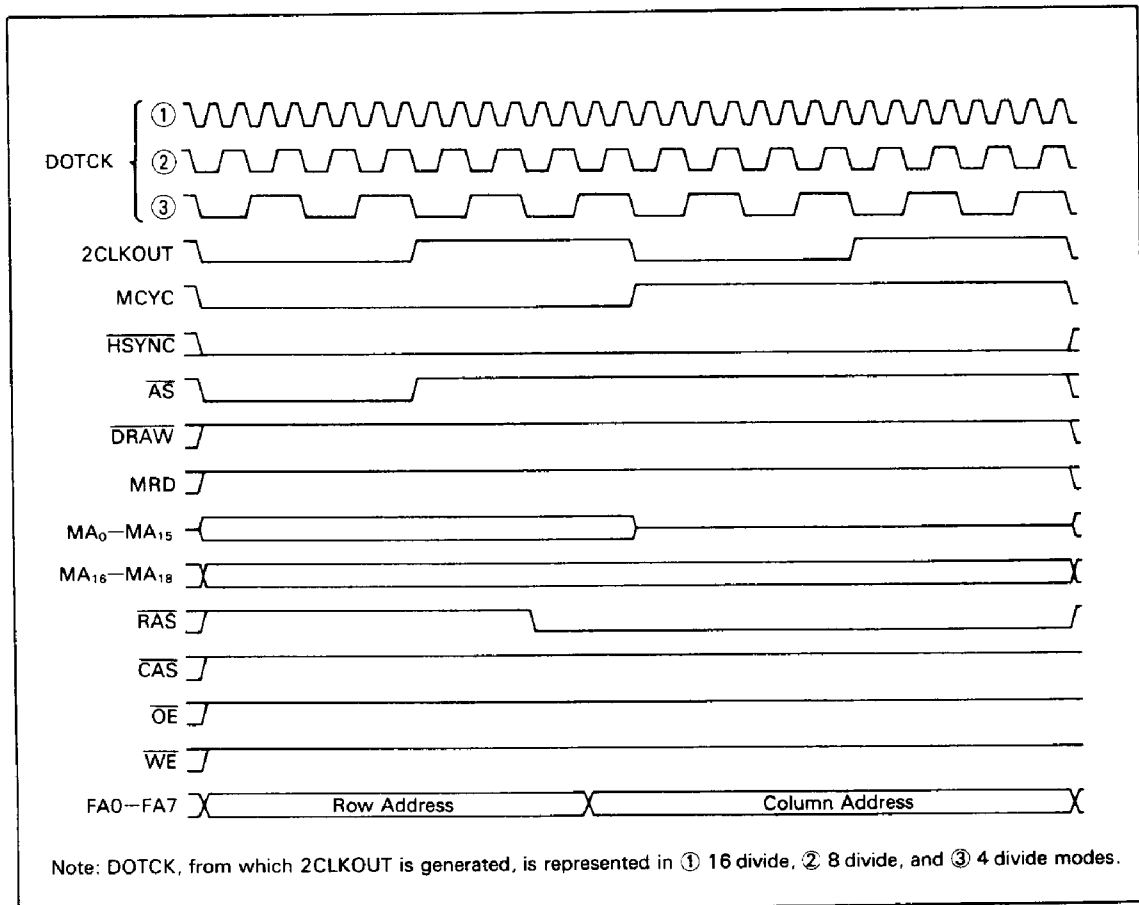
Figure 5. RAS Only Refresh Timing

Note: DOTCK, from which 2CLKOUT is generated, is represented in ① 16 divide, ② 8 divide, and ③ 4 divide modes.

Figure 6. Read Cycle Timing

Note: DOTCK, from which 2CLKOUT is generated, is represented in ① 16 divide, ② 8 divide, and ③ 4 divide modes.
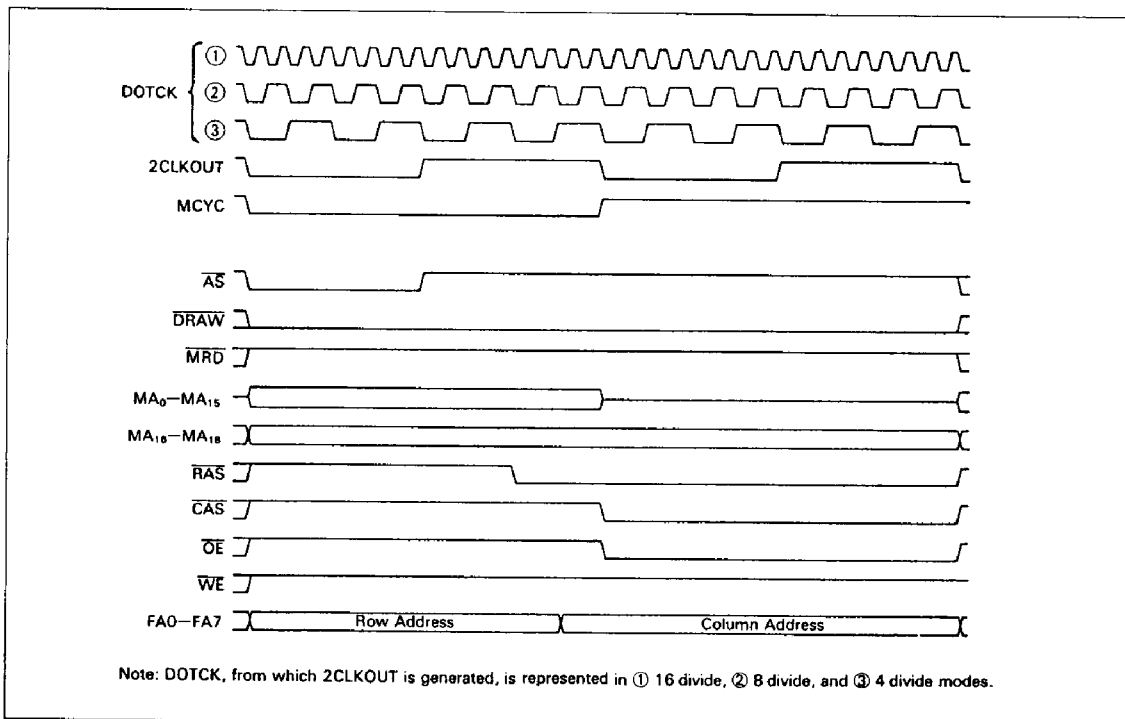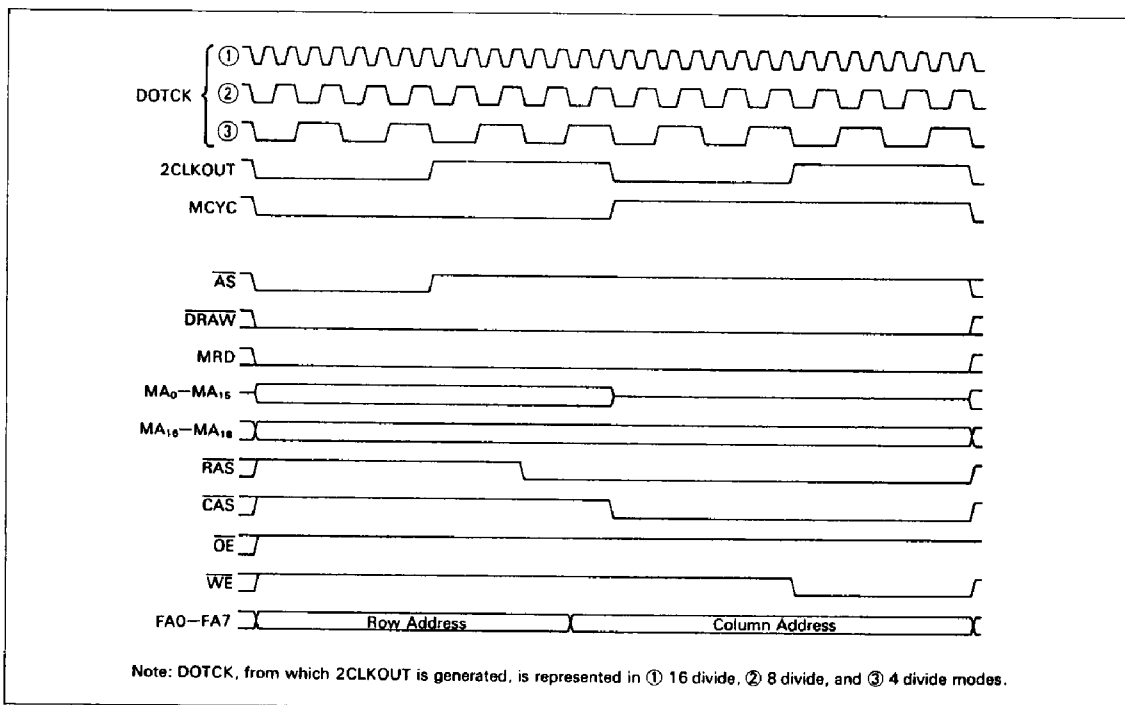
Figure 7. Write Cycle Timing

respectively.

Table 7 shows the output condition of the write enable signals $\overline{WE3}$-$\overline{WE0}$. The four write enable signals can directly control up to four memory banks. The $\overline{WE}$ output is determined by $\overline{DRAW}$, MA0, IM1, and IM0.

Video Shifter Shift Load Signals ($\overline{SLDB}$, $\overline{SLDW}$)

$\overline{SLDB}$ and $\overline{SLDW}$ load timing signals control the timing of display data input from a frame buffer to the video signal generation shift register (parallel-to-serial conversion circuit). $\overline{SLDB}$ is used for base screen in single access mode, dual access mode 0, and dual access mode 1. $\overline{SLDW}$ is used for window screens in dual access mode 1.

Relation of Access Mode and WSS to $\overline{SLDB}$ and $\overline{SLDW}$:
Table 8 shows the relationship between access modes, WSS, and $\overline{SLDB}$ and $\overline{SLDW}$. When WSS=0 in single access or dual access mode 0, $\overline{SLDB}$ output timing can be varied according to the amount of scrolling for one display cycle. $\overline{SLDW}$ is not output.

When WSS=0 in dual access mode 1 for the bese screen, $\overline{SLDB}$ output timing can be varied to accommodate smooth scrolling according to the horizontal scroll dot attribute control signals HSD3-HSD0 supplied by the ACRTC. The

$\overline{SLDW}$ signal is asserted for one period of the last dot clock during a display cycle. Its output cannot be varied for scrolling.

When WSS=1, for the window in dual access mode 1, $\overline{SLDB}$ signal is asserted and fixed for one period of the last dot clock of one display cycle, where as $\overline{SLDW}$ timing can be varied according to scrolling amount in one display cycle.

Amount of Scrolling and Output Timing :
Figure 8 shows the output timing of the shift load signals ($\overline{SLDB}$, $\overline{SLDW}$) for different amounts of scrolling. With increased scrolling, the load signal is output earlier by one dot clock.

Figure 9, 10, and 11 show $\overline{SLDB}$ and $\overline{SLDW}$ timing for single access, dual access mode 0, and dual access mode 1, respectively. Figure 12, 13, and 14 show $\overline{SLDB}$ timing for double and triple zooming.

Table 9 shows the attribute codes set for the ACRTC and the corresponding scrolling amounts. Table 10 shows the relationship between the GMIC dot clock division ratios and GVAC shift register lengths in corresponding access modes. Display colors are determined by the shift register length and amount of display data simultaneously read set in the ACRTC's GAI. The single and dual access modes are described in the ACRTC User's Manual, 3.2 CRT Interface.

Table 8. WSS, Access Mode, Shift Load Signals

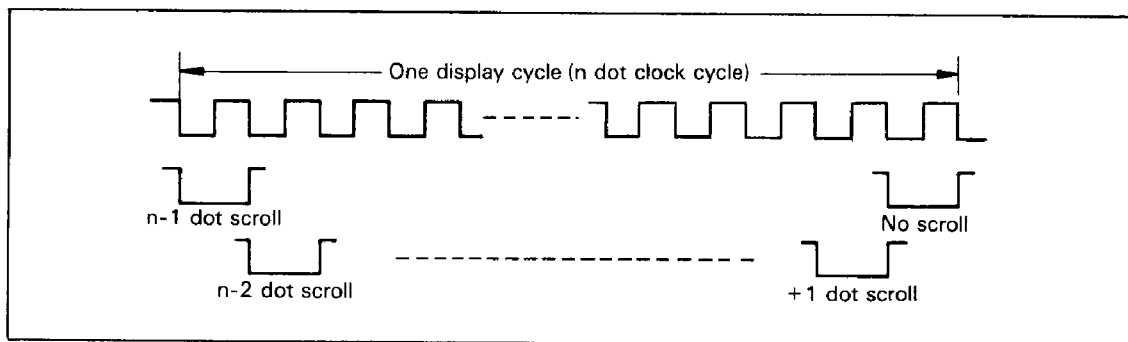| WSS	Access Mode	$\overline{SLDB}$	$\overline{SLDW}$
0	Single access, Dual access 0	Scrolling amount is permitted	No output
	Dual access 1, Base screen	Scrolling amount is permitted	Scrolling impossible
1	Dual access 1, Base screen	Scrolling impossible	Scrolling amount is permitted

Figure 8. Shift Load ($\overline{SLDB}$, $\overline{SLDW}$) Output Timing

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Table 9. ACRTC Attribute Codes and Scrolling Amounts

Shift Bit Length	HSD5	HSD4	HSD3	HSD2	HSD1	HSD0	Scroll Dot Count
16 bits	x	x	0	0	0	0	0
	x	x	0	0	0	1	1
	x	x	0	0	1	0	2
			⋮				
	x	x	1	1	1	0	14
	x	x	1	1	1	1	15
32 bits	x	0	0	0	0	0	0
	x	0	0	0	0	1	1
	x	0	0	0	1	0	2
			⋮				
	x	1	1	1	1	0	30
	x	1	1	1	1	1	31
64 bits	0	0	0	0	0	0	0
	0	0	0	0	0	1	1
	0	0	0	0	1	0	2
			⋮				
	1	1	1	1	1	0	62
	1	1	1	1	1	1	63

Note: The attribute code from the ACRTC supplies HSD3-HSD0, and memory address MA1 and MA0 supply HSD5 and HSD4. If these memory address bits are used (MA1 for 64-bit shifts, MA0 for 32-bit shifts), they must not be changed during one horizontal period.

Table 10. GMIC Division Ratio and GVAC Shift Lengths

Division Ratio	Single Access	Dual Access
Divide by 4	8 dot shift	16 dot shift
Divide by 8	16 dot shift	32 dot shift
Divide by 16	32 dot shift	64 dot shift (note)

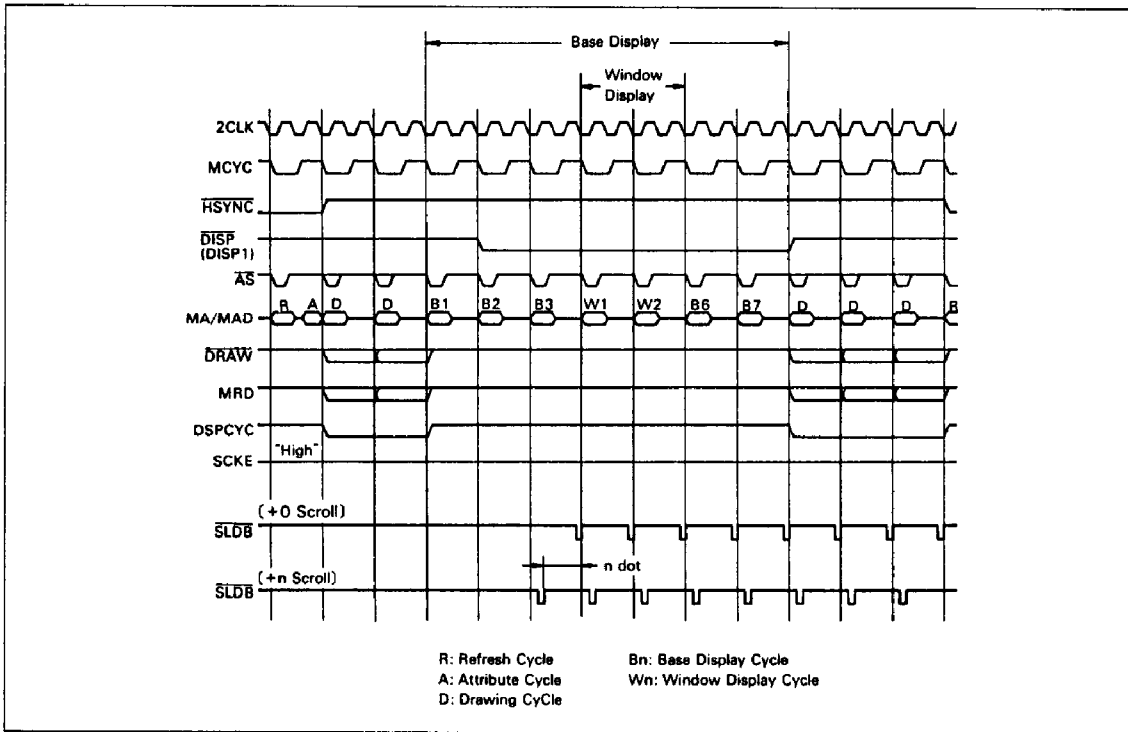Note: This mode cannot be used directly because the maximum shift register length is 32 dots.

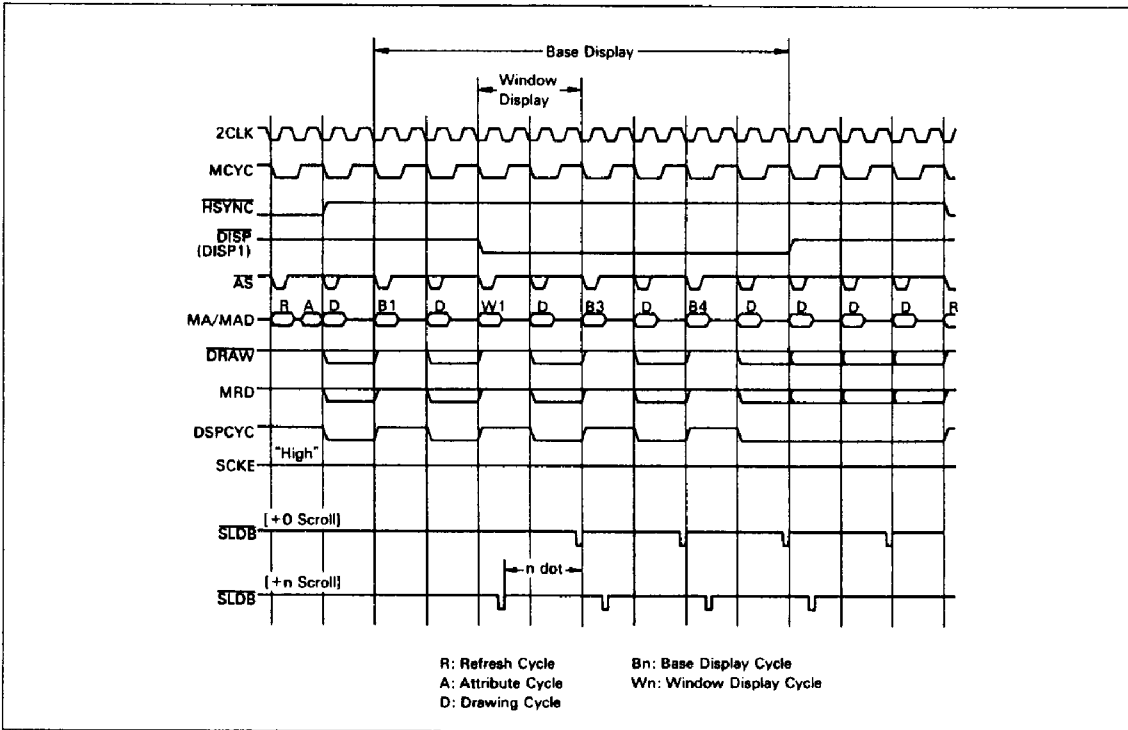Figure 9. $\overline{\text{SLDB}}$ Timing (Single Access Mode)

Figure 10. $\overline{\text{SLDB}}$ Timing (Dual Access Mode 0)
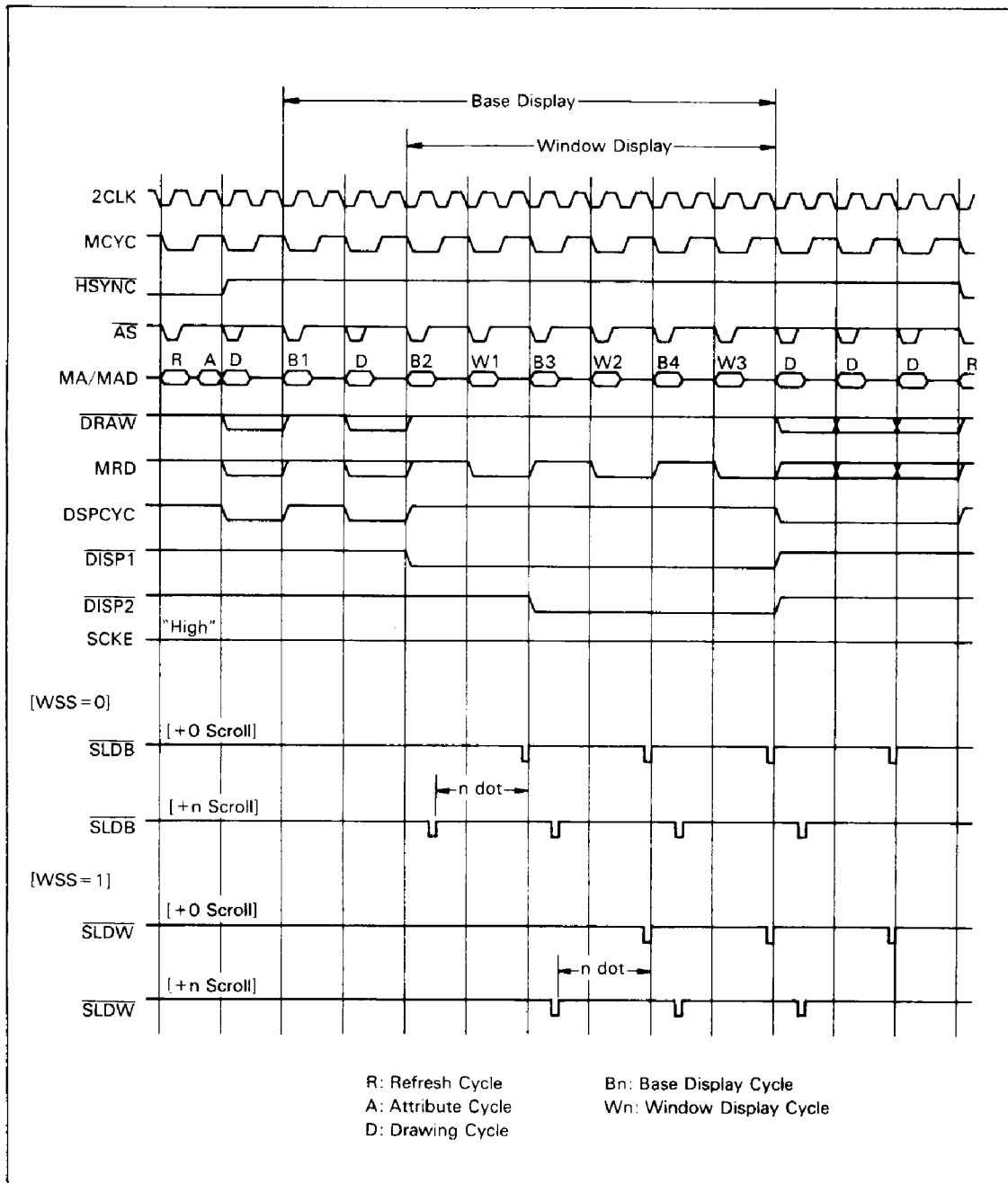
Figure 11. SLDB and SLDW Timing (Dual Access Mode 1)

R: Refresh Cycle   D: Drawing Cycle
A: Attribute Cycle   Bn: Base Display Cycle
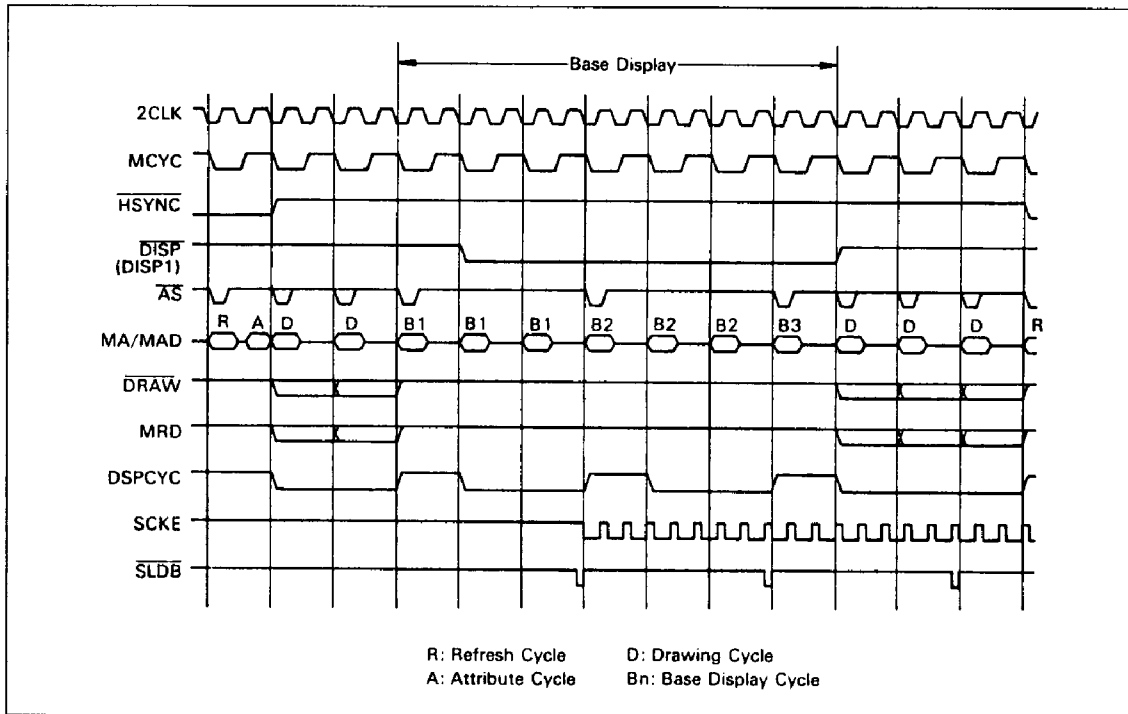
Figure 12.   Zoom Display Timing (Single Access Mode, Triple Zoom)

R: Refresh Cycle   D: Drawing Cycle
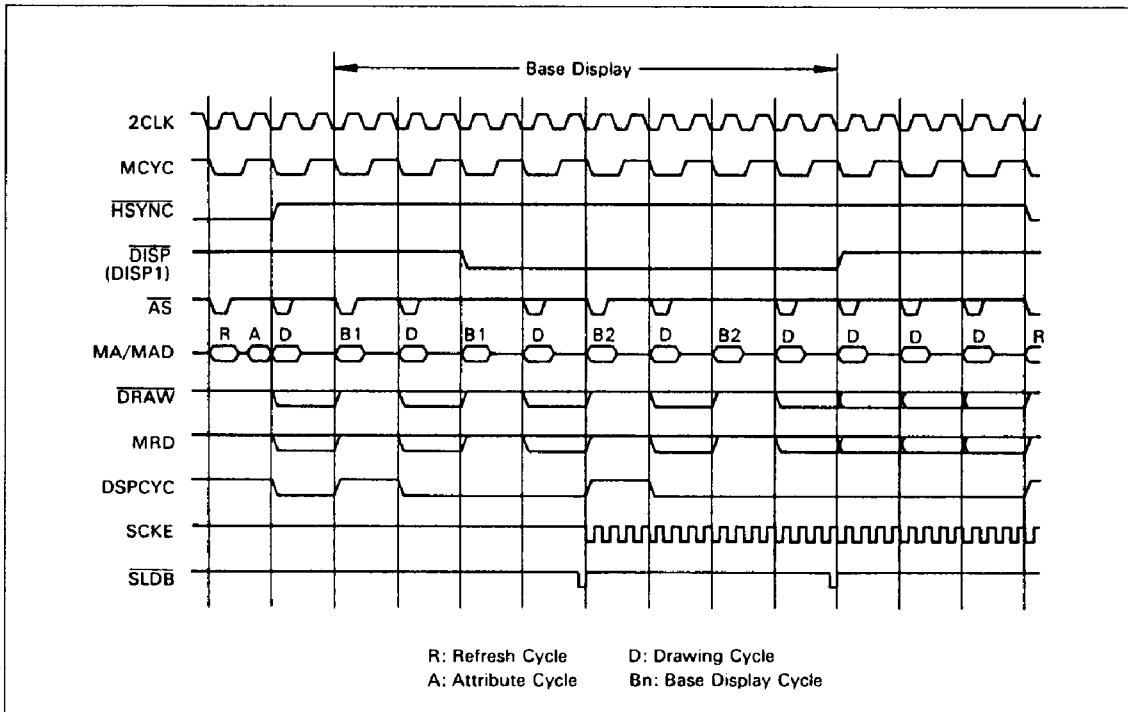A: Attribute Cycle   Bn: Base Display Cycle

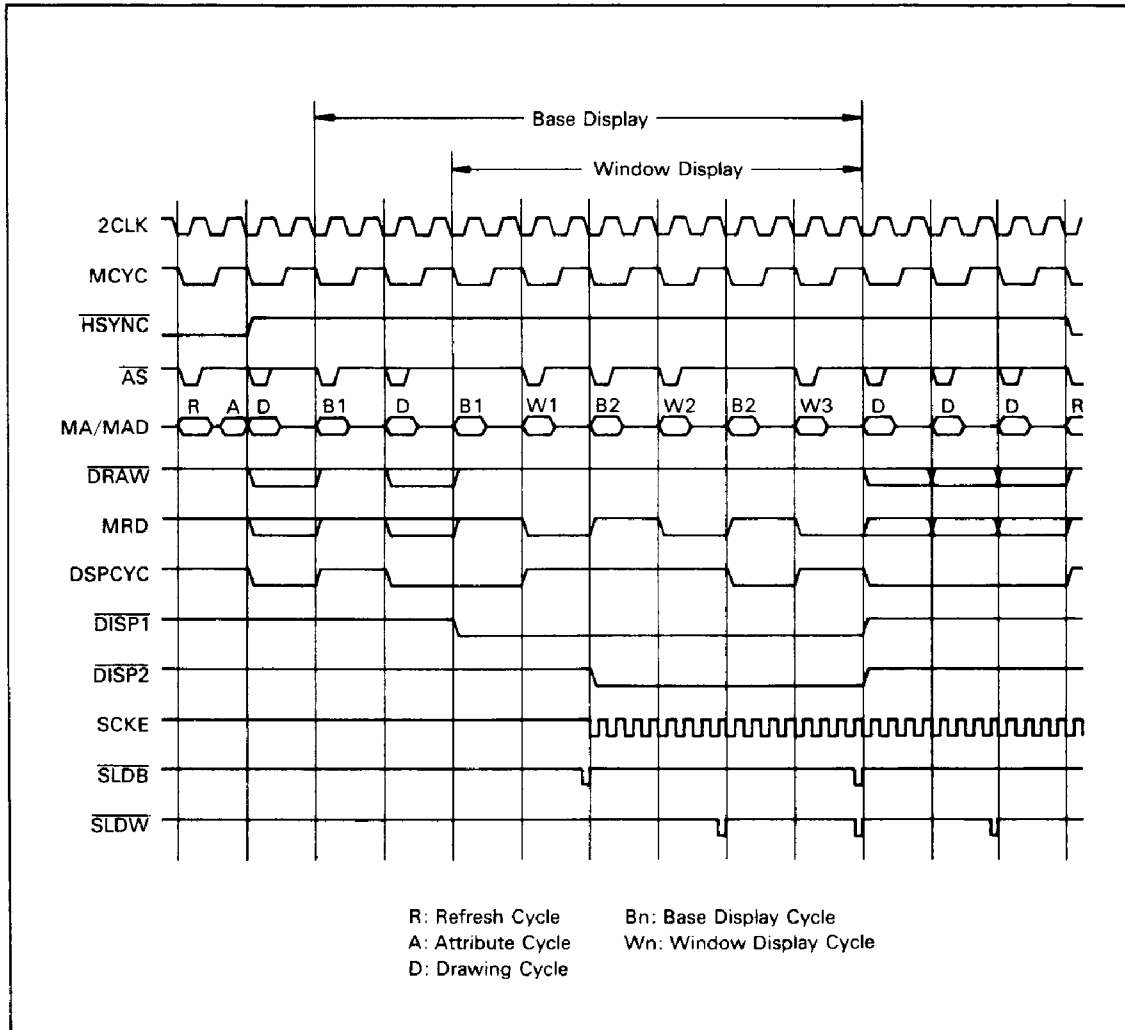**Figure 13.   Zoom Display Timing (Dual Access Mode 0, Double Zoom)**

Figure 14. Zoom Display Timing (Dual Access Mode 1,Double Zoom)

Driving Priority Mode : In the ACRTC drawing priority mode, drawing memory access takes priority over display memory access. In this mode, when display data is provided in the same manner as in the 32-bit shift mode but the system does not enter a display cycle, and a total output of 32 bits is completed, low-level output are provided until the next display cycle.

Shift Clock Enable (SCKE)

Shift clock enable (SCKE) is a control signal for the GVAC video signal generation shift register. GVAC drives the shift register on the falling edge of the dot clock. The SCKE control signal decreases the dot clock frequency to set the zoom scale. Figure 15 shows triple zoom (HZ=0011) timing. Table 11 shows attribute codes and corresponding zoom scales.

Table 11. Attribute Codes and Zoom Scales

| HZ3	HZ2	HZ1	HZ0	Zoom scale
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16
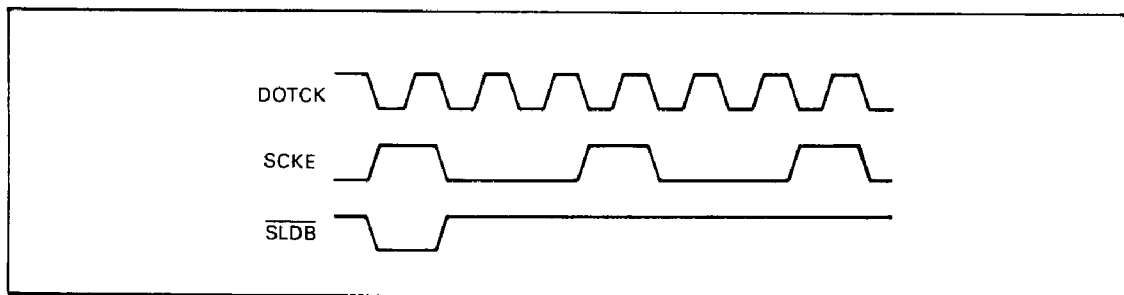
Figure 15. Triple Zoom Timing

Attribute Control Signals

The GMIC receives attribute code control signals for horizontal zooming and horizontal smooth scrolling from the ACRTC. Figure 16 shows attribute control output timing, and figure 17 shows the corresponding output pins.

The GMIC can control horizontal smooth scrolling of up to a 63-dot shift. However, the ACRTC outputs a 4-bit code (HSD3-HSD0), directly supporting up to a 15-dot shift. Therefore, the GMIC latches the lower 2 bits of the display adddress (MA0, MA1) output every display cycle into its internal register in order to control a 63-dot shift.
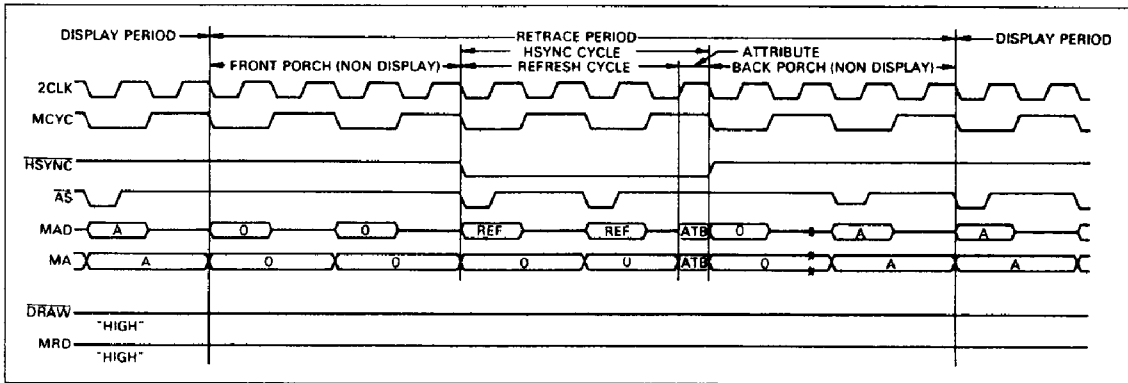
Figure 16. DRAM Refresh and Attribute Control Data Output (Single Access Mode)
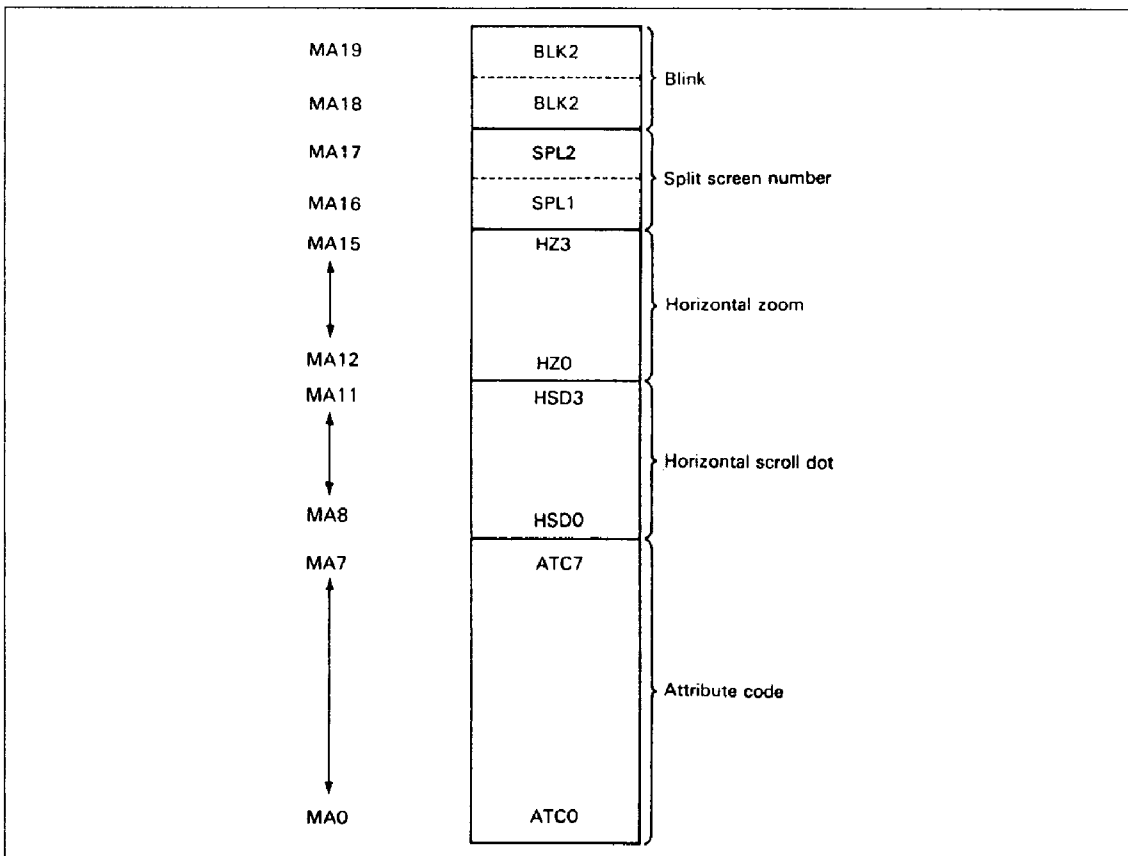
Figure 17. Attribute Control Signal Output Pins

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Absolute Maximum Ratings (All voltages referenced to Vss = 0 V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	− 0.3 to + 7.0	V
Input voltage	V_{in}	− 0.3 to V_{CC} + 0.3	V
Output voltage	V_{out}	5.5	V
Operating temperature	T_{opr}	0 to + 70	°C
Storage temperature	T_{str}	− 55 to + 150	°C

Notes : Using an LSI beyond in maximum ratings may result in its permanent destruction. LSIs should usually be operated under the recommended operating conditions. Exceeding any of these conditions may adversely affect its reliability.

Recommended Operating Conditions (All voltages referenced to Vss = 0 V)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Input voltage low	V_{IL}	0	—	0.7	V
Input voltage high	V_{IH}	2.2	—	V_{CC}	V
Operating temperature	T_{opr}	0	25	70	°C

Electrical Characteristics

DC Characteristics (V$_{CC}$ = 5.0 V ± 5%, V$_{SS}$ = 0 V, T$_a$ = 0°C to 70°C unless otherwise noted)

Item		Symbol	Min	Max	Unit	Test Condition
Input voltage high		V_{IH}	2.2	V_{CC}	V	
Input voltage low		V_{IL}	−0.3	0.7	V	
Input clamp voltage		V_I		−1.5	V	V_{CC} = 4.75 V, I_{in} = −18 mA
Output voltage high	ADRA-ADRC, $\overline{SLDB}$, $\overline{SLDW}$, DSPCYC, SCKE, 2CLKOUT	V_{OH}	2.7		V	V_{CC} = 4.75V, I_{OH} = −400 mA
	$\overline{WE3}$-$\overline{WE0}$. FA7-FA0, $\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$	V_{OH}	2.0		V	V_{CC} = 4.75 V, I_{OH} = −15 mA
Output voltage low	ADRA-ADRC, $\overline{SLDB}$, $\overline{SLDW}$, DSPCYC, SCKE 2CLKOUT	V_{OL}		0.5	V	V_{CC} = 4.75 V, I_{OL} = 8 mA
	$\overline{WE3}$-$\overline{WE0}$, FA7-FA0, $\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$	V_{OL}		0.5	V	V_{CC} = 4.75 V, I_{OL} = 24 mA
Input current high		I_{IH}		20	µA	V_{CC} = 5.25 V, V_I = 2.7 V
Input current low		I_{IL}		−400	µA	V_{CC} = 5.25 V, V_I = 0.4 V
Output short circuit current		I_{OS}	−40	−120	mA	V_{CC} = 5.25 V
Current consumption		I_{CC}		160	mA	V_{CC} = 5.25 V
Input capacitance		C_{in}		10	pF	

AC Characteristics (V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V, T_a = 0℃ to + 70℃)

No	Item	Symbol	32 MHz Min	32 MHz Max	48 MHz Min	48 MHz Max	64 MHz Min	64 MHz Max	Unit	Figure
	DOTCK operation frequence	f		32		48		64	MHz	
①	DOTCK cycle time	t_C	31.3		20.8		15.6		ns	18
②	DOTCK high level pulse width	t_{HW}	12		9		6		ns	
③	DOTCK low level pulse width	t_{LW}	12		9		6		ns	
④	DOTCK rise time	t_R		5		5		5	ns	
⑤	DOTCK fall time	t_F		5		5		5	ns	
⑥	2CLKOUT delay	t_{2CLKD}		24		17		14	ns	19
⑦	MCYC setup time	t_{MCYCS}	t_C + 20		t_C + 20		t_C + 20		ns	20-23
⑧	MCYC hold time	t_{MCYCH}	0		0		0		ns	
⑨	HSYNC setup time	H_{HSS}	t_C + 20		t_C + 20		t_C + 20		ns	20-22
⑩	HSYNC hold time	t_{HSH}	0		0		0		ns	23
⑪	MRD setup time	t_{MRDS}	t_C + 20		t_C + 20		t_C + 20		ns	20-22
⑫	MRD hold time	t_{MRDH}	5		5		5		ns	20, 21, 23
⑬	DRAW setup time	t_{DRAWS}	t_C + 20		t_C + 20		t_C + 20		ns	20-22
⑭	DRAW hold time	t_{DRAWH}	5		5		5		ns	20, 21, 23
⑮	AS setup time (CDM = 01)	t_{ASS}	t_C + 25		t_C + 25		t_C + 25		ns	20-23
	AS setup time (CMD = 10)	t_{ASS}	$2t_C$ + 25		$2t_C$ + 25		$2t_C$ + 25		ns	
	AS setup time (CDM = 11)	t_{ASS}	$4t_C$ + 25		$4t_C$ + 25		$4t_C$ + 25		ns	
⑯	AS pulse width	t_{ASW}	25		25		25		ns	
⑰	Memory address setup time	t_{MAS}	10		10		10		ns	20-23
⑱	Memory address hold time	t_{MAH}	5		5		5		ns	
⑲	Attribute code setup time	t_{ACS}	20		20		20		ns	23
⑳	Attribute code hold time	t_{ACH}	5		5		5		ns	
㉑	RAS setup time (CDM = 01)	t_{RSS}	t_C − 20		t_C − 20		t_C − 20		ns	20-23
	RAS setup time (CDM = 10)	t_{RSS}	$2t_C$ − 20		$2t_C$ − 20		$2t_C$ − 20		ns	
	RAS setup time (CDM = 11)	t_{RSS}	$4t_C$ − 20		$4t_C$ − 20		$4t_C$ − 20		ns	
㉒	RAS hold time	t_{RSH}	3		3		3		ns	

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AC Characteristics (cont)

| No	Item	Symbol	32 MHz		48 MHz		64 MHz		Unit	Figure
			Min	Max	Min	Max	Min	Max		
㉓	$\overline{CAS}$ delay time (CDM = 01)	t_{CASD}	$t_C - 7$		$t_C - 7$		$t_C - 7$		ns	20, 21
	$\overline{CAS}$ delay time (CDM = 10)	t_{CASD}	$2t_C - 7$		$2t_C - 7$		$2t_C - 7$		ns	
	$\overline{CAS}$ delay time (CDM = 11)	t_{CASD}	$4t_C - 7$		$4t_C - 7$		$4t_C - 7$		ns	
㉓A	$\overline{CAS}$ delay time from 2CLK	t_{CASDH}		20		20		15	ns	
㉔	$\overline{CAS}$ hold time	t_{CASH}	5		5		5		ns	
㉕	Memory address setup time (CDM = 01)	t_{MASC}	$t_C + 25$		$t_C + 25$		$t_C + 25$		ns	20-23
	Memory address setup time (CDM = 10)	t_{MASC}	$2t_C + 25$		$2t_C + 25$		$2t_C + 25$		ns	
	Memory address setup time (CDM = 11)	t_{MASC}	$4t_C + 25$		$4t_C + 25$		$4t_C + 25$		ns	
㉖	Row address setup time	t_{RAS}	0		0		0		ns	
㉗	Row address hold time (CDM = 01)	t_{RAH}	$t_C/2 - 2$		$t_C/2 - 2$		$t_C/2 - 2$		ns	
	Row address hold time (CDM = 10)	t_{RAH}	$t_C - 2$		$t_C - 2$		$t_C - 2$		ns	
	Row address hold time (CDM = 11)	t_{RAH}	$2t_C - 2$		$2t_C - 2$		$2t_C - 2$		ns	
㉘	Column address setup time	t_{CAS}	0		0		0		ns	20, 21
㉙	Column address hold time	t_{CAH}	0		0		0		ns	
㉚	$\overline{OE}$ delay time	t_{OED}		20		20		20	ns	20
㉛	$\overline{OE}$ hold time	t_{OEH}	3		3		3		ns	
㉜	$\overline{WE}$ delay time	t_{WED}	5	30	5	30	5	30	ns	21
㉝	$\overline{WE}$ hold time	t_{WEH}	3		3		3		ns	
㉞	Address delay time	t_{AD}		30		30		30	ns	
㉟	Address hold time	t_{AH}	0		0		0		ns	
㊱	SCKE delay time	t_{SCKD}	5	24	5	17	5	14	ns	18
㊲	$\overline{SLD}$ delay time	t_{SLDD}	5	24	5	17	5	14	ns	
㊳	DSPCYC delay time from $\overline{AS}$	t_{DSPDA}		40		40		40	ns	20
㊳A	DSPCYC delay time from $\overline{DRAW}$	t_{DSPDD}		20		20		20	ns	
㊴	DSPCYC hold time	t_{DSPH}	5		5		5		ns	
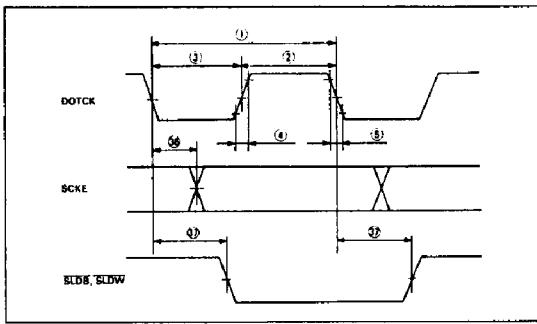
Figure 18.   Clock

Figure 19.   2CLKOUT

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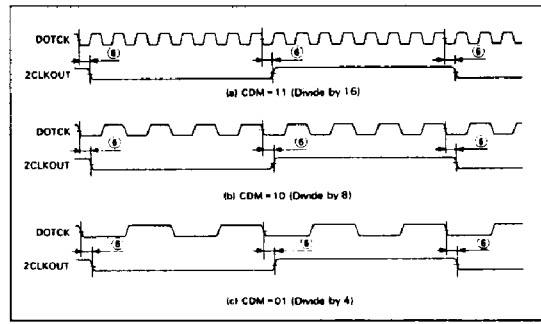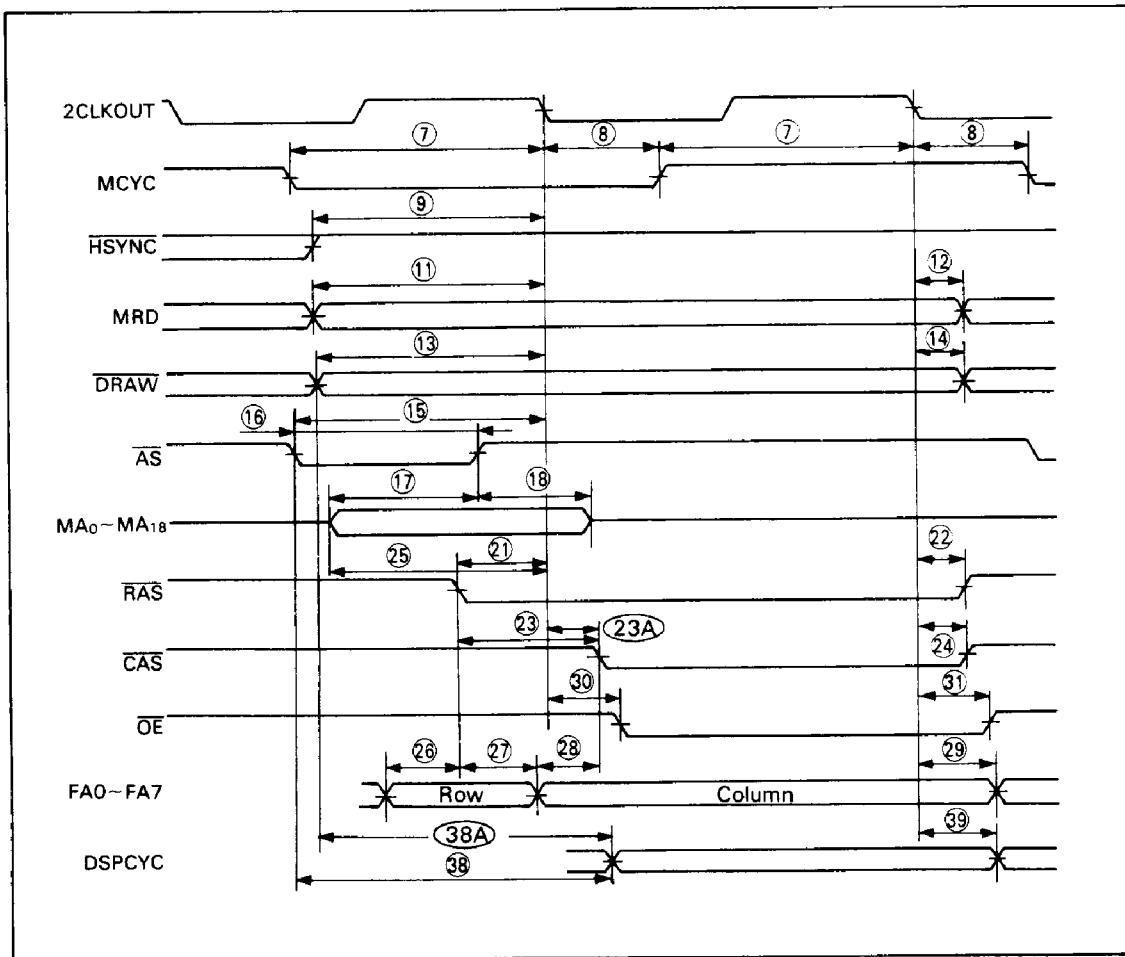
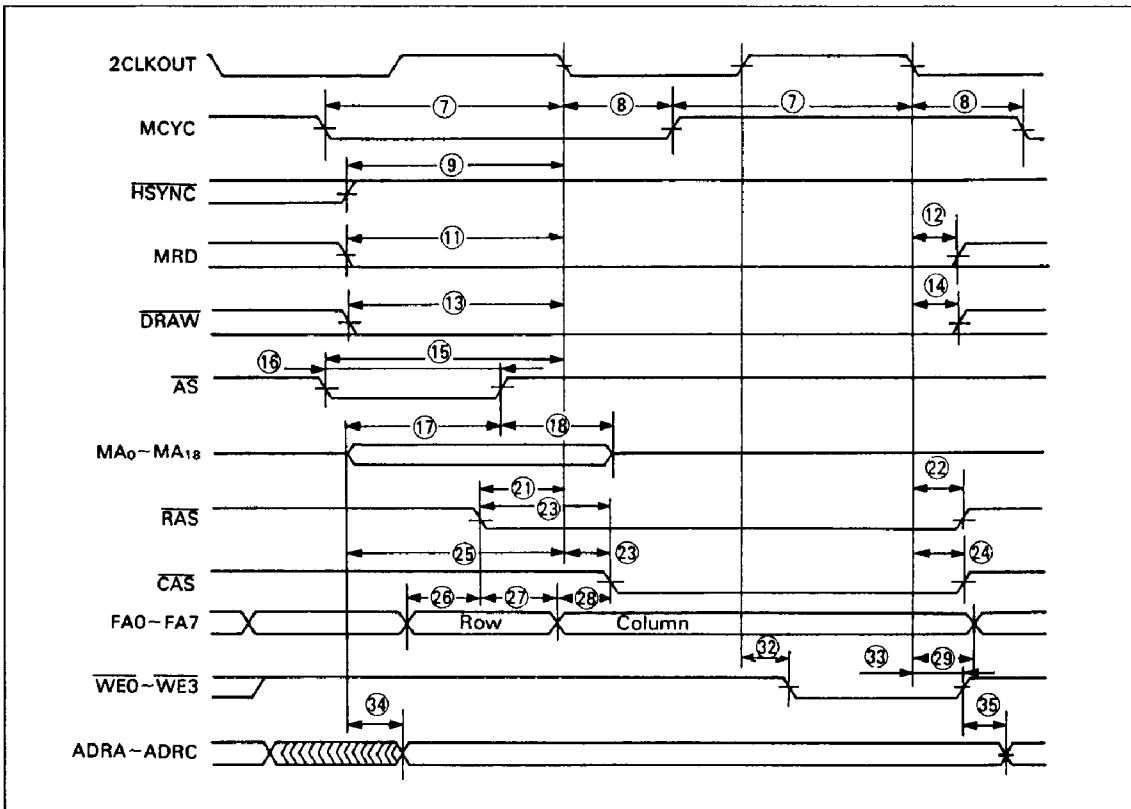**Figure 20.   Memory Read Cycle (Drawing Read and Display)**

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Figure 21.   Memory Write Cycle

Figure 22.   Refresh Cycle