SMSC™

STANDARD
MICROSYSTEMS
CORPORATION

FDC37C93x

Plug and Play Compatible Ultra I/O™ Controller

FEATURES

- 5 Volt Operation
- ISA Plug-and-Play Standard (Version 1.0a) Compatible Register Set
- 8042 Keyboard Controller
  - 2K Program ROM
  - 256 Bytes Data RAM
  - Asynchronous Access to Two Data Registers and One Status Register
  - Supports Interrupt and Polling Access
  - 8 Bit Timer/Counter
- Real Time Clock
  - MC146818 and DS1287 Compatible
  - 256 Bytes of Battery Backed CMOS in Two Banks of 128 Bytes
  - 128 Bytes of CMOS RAM Lockable in 4x32 Byte Blocks
  - 12 and 24 Hour Time Format
  - Binary and BCD Format
  - 1µa Standby Current (typ)
- Intelligent Auto Power Management
- 2.88MB Super I/O Floppy Disk Controller
  - Relocatable to 480 Different Addresses
  - 13 IRQ Options
  - 4 DMA Options
  - Licensed CMOS 765B Floppy Disk Controller
  - Advanced Digital Data Separator
  - Software and Register Compatible with SMSC's Proprietary 82077AA Compatible Core
  - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
  - Game Port Select Logic
  - Supports Two Floppy Drives Directly
  - 24 mA AT Bus Drivers
  - Low Power CMOS Design
- Licensed CMOS 765B Floppy Disk Controller Core
  - Supports Vertical Recording Format
  - 16 Byte Data FIFO
  - 100% IBM® Compatibility
  - Detects All Overrun and Underrun Conditions
  - 48 mA Drivers and Schmitt Trigger Inputs
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
- Enhanced Digital Data Separator
  - Low Cost Implementation
  - No Filter Components Required
  - 2 Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - Programmable Precompensation Modes
- Serial Ports
  - Relocatable to 480 Different Addresses
  - 13 IRQ Options
  - Two High Speed NS16C550 Compatible UARTs with Send/Receive 16 Byte FIFOs
  - Programmable Baud Rate Generator
  - Modem Control Circuitry Including 230K and 460K Baud
  - IrDA, HP-SIR, ASK-IR Support
- IDE Interface
  - Relocatable to 480 Different Addresses
  - 13 IRQ Options (*IRQ Steering through chip)*
  - Two Channel/Four Drive Support
  - On-Chip Decode and Select Logic Compatible with IBM PC/XT® and PC/AT® Embedded Hard Disk Drives
- Serial EEPROM Interface
- Multi-Mode™ Parallel Port with ChiProtect™

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80 Arkay Dr.
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- Relocatable to 480 Different Addresses
- 13 IRQ Options
- 4 DMA Options
- Enhanced Mode
- Standard Mode:
  - IBM PC/XT, PC/AT, and PS/2™ Compatible Bidirectional Parallel Port
  - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - High Speed Mode
  - Microsoft and Hewlett Packard Extended Capabilities Port (ECP) Compatible (IEEE 1284 Compliant)
- Incorporates ChiProtect™ Circuitry for Protection Against Damage Due to Printer Power-On
- 12 mA Output Drivers

- ISA Host Interface
- 16 Bit Address Qualification
- 160 Pin QFP Package

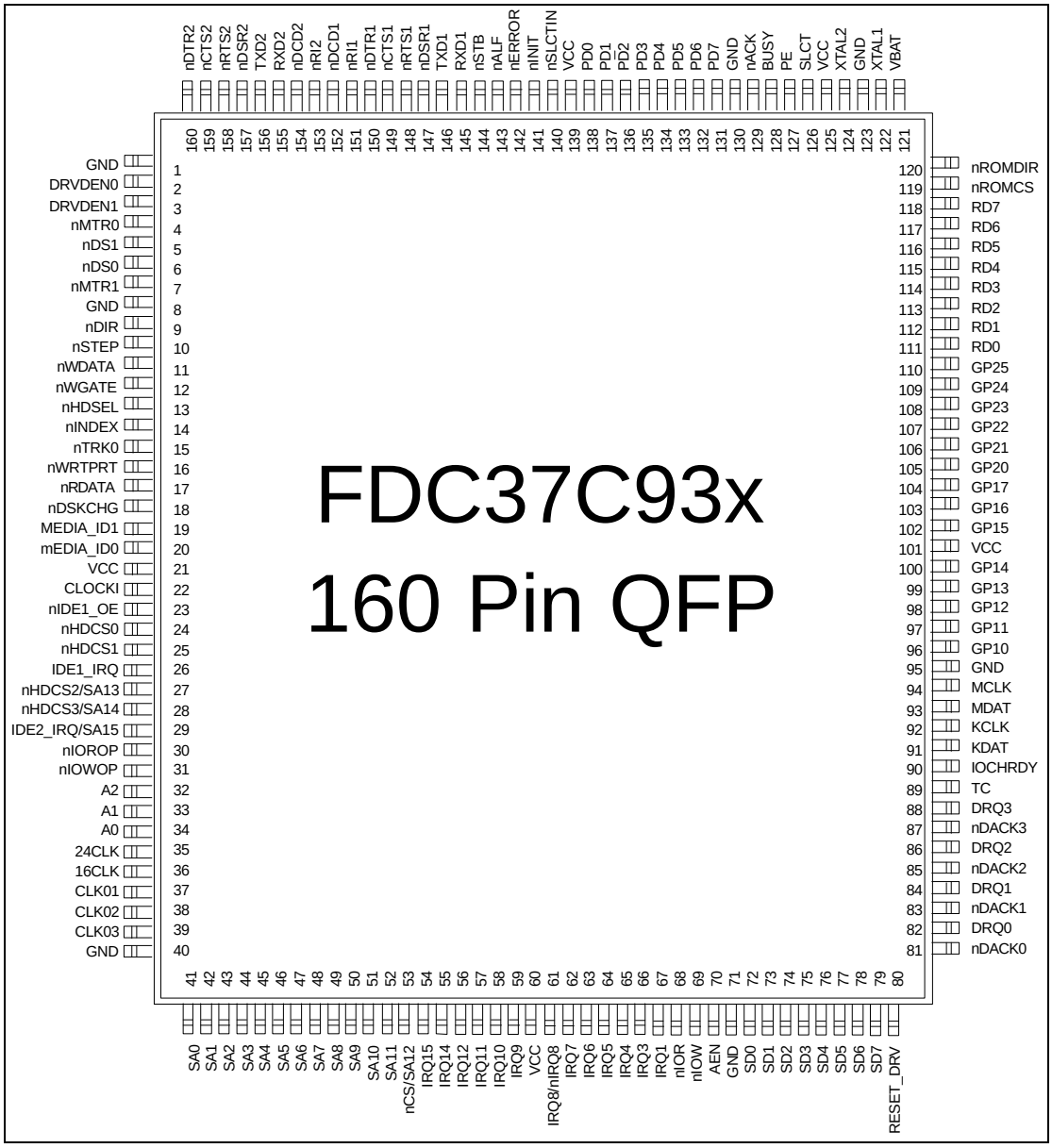
GENERAL DESCRIPTION

The FDC37C93x incorporates a keyboard interface, real-time clock, SMSC's true CMOS 765B floppy disk controller, advanced digital data separator, 16 byte data FIFO, two 16C550 compatible UARTs, one Multi-Mode parallel port which includes ChiProtect circuitry plus EPP and ECP support, IDE interface, on-chip 24 mA AT bus drivers, game port chip select and two floppy direct drive support. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures in addition to providing data overflow and underflow protection. The SMSC advanced digital data separator incorporates SMSC's patented data separator technology, allowing for ease of testing and use. Both on-chip UARTs are compatible with the NS16C550. The parallel port, the IDE interface, and the game port select logic are compatible with IBM PC/AT architecture, as well as EPP and ECP. The FDC37C93x incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes.

The FDC37C93x provides support for the ISA Plug-and-Play Standard (Version 1.0a) and provides for the recommended functionality to support Windows '95. Through internal configuration registers, each of the FDC37C93x's logical device's I/O address, DMA channel and IRQ channel may be programmed. There are 480 I/O address location options, 13 IRQ options, and three DMA channel options for each logical device.

The FDC37C93x does not require any external filter components and is, therefore, easy to use and offers lower system cost and reduced board area. The FDC37C93x is software and register compatible with SMSC's proprietary 82077AA core.

PIN CONFIGURATION



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE
PROCESSOR/HOST INTERFACE			
72:79	System Data Bus	SD[0:7]	I/O24
41:52	System Address Bus	SA[0:11]	I
53	Chip Select/SA12 (Active Low)(Note 1)	nCS	I
70	Address Enable (DMA master has bus control)	AEN	I
90	I/O Channel Ready	IOCHRDY	OD24
80	Reset Drive	RESET_DRV	IS
67:61, 59:54	Interrupt Requests [1,3:12,14,15] (Polarity control for IRQ8)	IRQ[1,3:12, 14,15]	OD24
82,84, 86,88	DMA Requests	DRQ[0:3]	O24
81,83, 85,87	DMA Acknowledge	nDACK[0:3]	I
89	Terminal Count	TC	I
68	I/O Read	nIOR	I
69	I/O Write	nIOW	I
35	Serial Clock Out (24 MHz)	24CLK	08SR
36	16 MHz Out	16CLK	08SR
22	14.318MHz Clock Input	CLOCKI	ICLK
37	14.318MHz Clock Output 1	CLKO1	O16SR
38	14.318MHz Clock Output 2	CLKO2	08SR
39	14.318MHz Clock Output 3	CLKO3	08SR
POWER PINS			
21, 60, 101, 125, 139	+5V Supply Voltage	VCC	
1, 8, 40, 71, 95, 123, 130	Ground	GND	
FDD INTERFACE			
17	Read Disk Data	nRDATA	IS
12	Write Gate	nWGATE	OD48
11	Write Disk Data	nWDATA	OD48

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE
13	Head Select (1 = side 0)	nHDSEL	OD48
9	Step Direction (1 = out)	nDIR	OD48
10	Step Pulse	nSTEP	OD48
18	Disk Change	nDSKCHG	IS
5,6	Drive Select Lines	nDS[1:0]	OD48
7,4	Motor On Lines	nMTR[1:0]	OD48
16	Write Protected	nWPROT	IS
15	Track 0	nTR0	IS
14	Index Pulse Input	nINDEX	IS
3,2	Drive Density Select [1:0]	DRVDEN [1:0]	OD48
19,20	Media ID inputs. In floppy enhanced mode 2 these inputs are the media ID [1:0] inputs.	MID[1:0]	IS
SERIAL PORT 1 INTERFACE			
145	Receive Serial Data 1	RXD1	I
146	Transmit Serial Data 1	TXD1	O4
148	Request to Send 1	nRTS1	O4
149	Clear to Send 1	nCTS1	I
150	Data Terminal Ready 1	nDTR1	O4
147	Data Set Ready 1	nDSR1	I
152	Data Carrier Detect 1	nDCD1	I
151	Ring Indicator 1	nRI1	I
SERIAL PORT 2 INTERFACE			
155	Receive Serial Data 2	RXD2	I
156	Transmit Serial Data 2	TXD2	O4
158	Request to Send 2	nRTS2	O4
159	Clear to Send 2	nCTS2	I
160	Data Terminal Ready 2	nDTR2	O4
157	Data Set Ready 2	nDSR2	I
154	Data Carrier Detect 2	nDCD2	I
153	Ring Indicator 2	nRI2	I
IDE1 INTERFACE			

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE
23	IDE1 Enable	nIDE1_OE	O4
24	IDE1 Chip Select 0	nHDCS0	O24
25	IDE1 Chip Select 1	nHDCS1	O24
30	IOR Output	nIOROP	024
31	IOW Output	nIOWOP	024
32:34	Address [2:0] Output	A[2:0]	024
26	IDE1 Interrupt Request	IDE1_IRQ	I
IDE2 INTERFACE			
27	IDE2 Chip Select 2/SA13 (Note 3)	nHDCS2	I/O24
28	IDE2 Chip Select 3/SA14 (Note 3)	nHDCS3	I/O24
29	IDE2 Interrupt Request/SA15	IDE2_IRQ	I
PARALLEL PORT INTERFACE			
138:131	Parallel Port Data Bus	PD[0:7]	I/OP24
140	Printer Select	nSLCTIN	OD24/OP24
141	Initiate Output	nINIT	OD24/OP24
143	Auto Line Feed	nALF	OD24/OP24
144	Strobe Signal	nSTB	OD24/OP24
128	Busy Signal	BUSY	I
129	Acknowledge Handshake	nACK	I
127	Paper End	PE	I
126	Printer Selected	SLCT	I
142	Error at Printer	nERROR	I
REAL-TIME CLOCK			
122	32Khz Crystal Input	XTAL1	ICLK2
124	32Khz Crystal Output	XTAL2	OCLK2
121	Battery Voltage	Vbat	
KEYBOARD/MOUSE			
91	Keyboard Data	KDAT	I/OD16P
92	Keyboard Clock	KCLK	I/OD16P
93	Mouse Data	MDAT	I/OD16P

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE
94	Mouse Clock	MCLK	I/OD16P
GENERAL PURPOSE I/O			
96	GP I/O; IRQ in	GP10	I/O4
97	GP I/O; IRQ in	GP11	I/O4
98	GP I/O; WD Timer Output /IRRX	GP12	I/O4
99	GP I/O; Power Led output /IRTX	GP13	I/O24
100	GP I/O; GP Address Decode	GP14	I/O4
102	GP I/O; GP Write Strobe	GP15	I/O4
103	GP I/O; JOY Read Strobe/JOYCS	GP16	I/O4
104	GP I/O; Joy Write Strobe	GP17	I/O4
105	GP I/O; IDE2 Output Enable/8042 P20	GP20	I/O4
106	GP I/O; Serial EEPROM Data In	GP21	I/O4
107	GP I/O; Serial EEPROM Data Out	GP22	I/O4
108	GP I/O; Serial EEPROM Clock	GP23	I/O4
109	GP I/O; Serial EEPROM Enable	GP24	I/O4
110	GP I/O; 8042 P21	GP25	I/O4
BIOS BUFFERS			
111:118	ROM Bus (I/O to the SD Bus)	RD[0:7]	I/O4
119	ROM Chip Select (only used for ROM)	nROMCS	I
120	ROM Output Enable (DIR) (only used for ROM)	nROM*DIR*	I

Note 1: nCS -This pin is the active low chip select, it must be low for all chip accesses. For 12 bit addressing, SA0:SA11, this input should be tied to GND. For 16 bit address qualification, address bits SA12:SA15 can be "ORed" together and applied to this pin. If IDE2 is not used, SA12 can be connected to nCS, pin 27 to SA13, pin 28 to SA14 and pin 29 to SA15.
Note 2: nYY - The "n" as the first letter of a signal name indicates an "Active Low" signal.
Note 3: nHDCS2 and nHDCS3 require a pull-up to ensure a logic high at power-up when used for IDE2 until the Active Bit is set to 1.

Buffer Type Descriptions

I	Input, TTL compatible.
IS	Input with Schmitt trigger.
I/OD16P	Input/Output, 16mA sink, 90uA pull-up.
I/O24	Input/Output, 24mA sink, 12mA source.
I/O4	Input/Output, 4mA sink, 2mA source
O4	Output, 4mA sink, 2mA source.
O8SR	Output, 8mA sink, 4mA source with Slew Rate Limiting
O16SR	Output, 16mA sink, 8mA source with Slew Rate Limiting
O24	Output, 24mA sink, 12mA source.
OD24	Output, Open Drain, 24mA sink.
OD48	Output, Open Drain, 48mA sink.
OP24	Output, 24mA sink, 12mA source.
I/OP24	Input/Output, 24mA sink, 12mA source, 90µA pull-up
ICLK	Clock Input
ICLK2	Clock Input
OCLK2	Clock Output

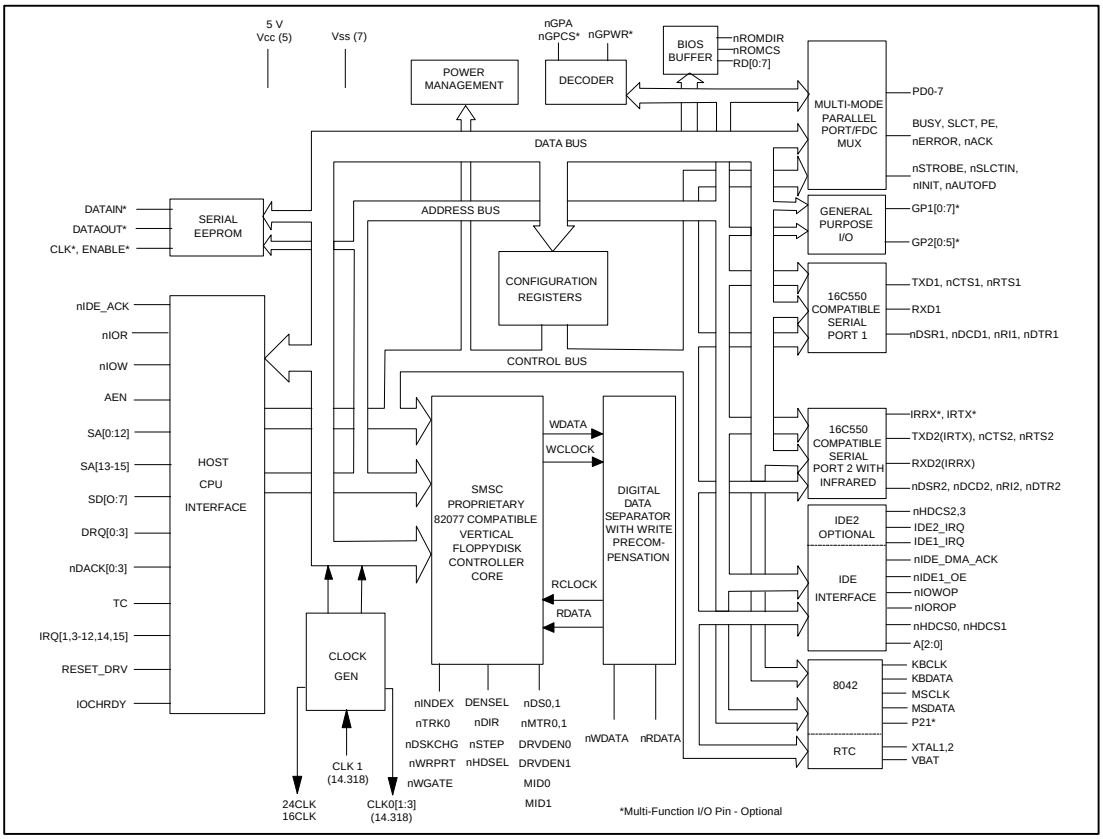


FIGURE 1 - FDC37C93x BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

SUPER I/O REGISTERS

The address map, shown below in Table 1, shows the addresses of the different blocks of the Super I/O immediately after power up. The base addresses of the FDC, IDE, serial and parallel ports can be moved via the configuration registers. Some addresses are used to access more than one register.

HOST PROCESSOR INTERFACE

The host processor communicates with the FDC37C93x through a series of read/write registers. The port addresses for these registers are shown in Table 1. Register access is accomplished through programmed I/O or DMA transfers. All registers are 8 bits wide except the IDE data register at port 1F0H which is 16 bits wide. All host interface output buffers are capable of sinking a minimum of 12 mA.

Table 1 - Super I/O Block Addresses

ADDRESS	BLOCK NAME	LOGICAL DEVICE	NOTES
Base+(0-5) and +(7)	Floppy Disk	0	
Base+(0-7)	Serial Port Com 1	4	
Base+(0-7)	Serial Port Com 2	5	IR Support
Base+(0-3) Base+(0-7) Base+(0-3), +(400-402) Base+(0-7), +(400-402)	Parallel Port SPP EPP ECP ECP+EPP+SPP	3	
Base1+(0-7), Base2+(0)	IDE 1	1	
Base1+(0-7), Base2+(0)	IDE 2	2	

Note 1: Refer to the configuration register descriptions for setting the base address

FLOPPY DISK CONTROLLER

The Floppy Disk Controller (FDC) provides the interface between a host microprocessor and the floppy disk drives. The FDC integrates the functions of the Formatter/Controller, Digital Data Separator, Write Precompensation and Data Rate Selection logic for an IBM XT/AT compatible FDC. The true CMOS 765B core guarantees 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection.

The FDC is compatible to the 82077AA using SMSC's proprietary floppy disk controller core.

FDC INTERNAL REGISTERS

The Floppy Disk Controller contains eight internal registers which facilitate the interfacing between the host microprocessor and the disk drive. Table 2 shows the addresses required to access these registers. Registers other than the ones shown are not supported. The rest of the description assumes that the primary addresses have been selected.

Table 2 - Status, Data and Control Registers
(Shown with base addresses of 3F0 and 370)

PRIMARY ADDRESS	SECONDARY ADDRESS		REGISTER	
3F0	370	R	Status Register A	SRA
3F1	371	R	Status Register B	SRB
3F2	372	R/W	Digital Output Register	DOR
3F3	373	R/W	Tape Drive Register	TSR
3F4	374	R	Main Status Register	MSR
3F4	374	W	Data Rate Select Register	DSR
3F5	375	R/W	Data (FIFO)	FIFO
3F6	376		Reserved	
3F7	377	R	Digital Input Register	DIR
3F7	377	W	Configuration Control Register	CCR

STATUS REGISTER A (SRA)

Address 3F0 READ ONLY
This register is read-only and monitors the state of the FINTR pin and several disk interface pins in PS/2 and Model 30 modes. The SRA can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F0.

PS/2 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	nDRV2	STEP	nTRK0	HDSEL	nINDX	nWP	DIR
RESET COND.	0	N/A	0	N/A	0	N/A	N/A	0

BIT 0 DIRECTION
Active high status indicating the direction of head movement. A logic "1" indicates inward direction; a logic "0" indicates outward direction.

BIT 1 nWRITE PROTECT
Active low status of the WRITE PROTECT disk interface input. A logic "0" indicates that the disk is write protected.

BIT 2 nINDEX
Active low status of the INDEX disk interface input.

BIT 3 HEAD SELECT
Active high status of the HDSEL disk interface input. A logic "1" selects side 1 and a logic "0" selects side 0.

BIT 4 nTRACK 0
Active low status of the TRK0 disk interface input.

BIT 5 STEP
Active high status of the STEP output disk interface output pin.

BIT 6 nDRV2
Active low status of the DRV2 disk interface input pin, indicating that a second drive has been installed.

BIT 7 INTERRUPT PENDING
Active high bit indicating the state of the Floppy Disk Interrupt output.

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	DRQ	STEP F/F	TRK0	nHDSEL	INDX	WP	nDIR
RESET COND.	0	0	0	N/A	1	N/A	N/A	1

BIT 0 nDIRECTION
Active low status indicating the direction of head movement. A logic "0" indicates inward direction; a logic "1" indicates outward direction.

BIT 1 WRITE PROTECT
Active high status of the WRITE PROTECT disk interface input. A logic "1" indicates that the disk is write protected.

BIT 2 INDEX
Active high status of the INDEX disk interface input.

BIT 3 nHEAD SELECT
Active low status of the HDSEL disk interface input. A logic "0" selects side 1 and a logic "1" selects side 0.

BIT 4 TRACK 0
Active high status of the TRK0 disk interface input.

BIT 5 STEP
Active high status of the latched STEP disk interface output pin. This bit is latched with the STEP output going active, and is cleared with a read from the DIR register, or with a hardware or software reset.

BIT 6 DMA REQUEST
Active high status of the DRQ output pin.

BIT 7 INTERRUPT PENDING
Active high bit indicating the state of the Floppy Disk Interrupt output.

STATUS REGISTER B (SRB)

Address F1 READ ONLY
This register is read-only and monitors the state of several disk interface pins in PS/2 and Model 30 modes. The SRB can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F1.

PS/2 Mode

	7	6	5	4	3	2	1	0
	1	1	DRIVE SEL0	WDATA TOGGLE	RDATA TOGGLE	WGATE	MOT EN1	MOT EN0
RESET COND.	1	1	0	0	0	0	0	0

BIT 0 MOTOR ENABLE 0
Active high status of the MTR0 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 1 MOTOR ENABLE 1
Active high status of the MTR1 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 2 WRITE GATE
Active high status of the WGATE disk interface output.

BIT 3 READ DATA TOGGLE
Every inactive edge of the RDATA input causes this bit to change state.

BIT 4 WRITE DATA TOGGLE
Every inactive edge of the WDATA input causes this bit to change state.

BIT 5 DRIVE SELECT 0
Reflects the status of the Drive Select 0 bit of the DOR (address 3F2 bit 0). This bit is cleared after a hardware reset and it is unaffected by a software reset.

BIT 6 RESERVED
Always read as a logic "1".

BIT 7 RESERVED
Always read as a logic "1".

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	nDRV2	nDS1	nDS0	WDATA F/F	RDATA F/F	WGATE F/F	nDS3	nDS2
RESET COND.	N/A	1	1	0	0	0	1	1

BIT 0 nDRIVE SELECT 2
Active low status of the DS2 disk interface output.

BIT 1 nDRIVE SELECT 3
Active low status of the DS3 disk interface output.

BIT 2 WRITE GATE
Active high status of the latched WGATE output signal. This bit is latched by the active going edge of WGATE and is cleared by the read of the DIR register.

BIT 3 READ DATA
Active high status of the latched RDATA output signal. This bit is latched by the inactive going edge of RDATA and is cleared by the read of the DIR register.

BIT 4 WRITE DATA
Active high status of the latched WDATA output signal. This bit is latched by the inactive going edge of WDATA and is cleared by the read of the DIR register. This bit is not gated with WGATE.

BIT 5 nDRIVE SELECT 0
Active low status of the DS0 disk interface output.

BIT 6 nDRIVE SELECT 1
Active low status of the DS1 disk interface output.

BIT 7 nDRV2
Active low status of the DRV2 disk interface input.

DIGITAL OUTPUT REGISTER (DOR)

Address 3F2 READ/WRITE

The DOR controls the drive select and motor enables of the disk interface outputs. It also contains the enable for the DMA logic and a software reset bit. The contents of the DOR are unaffected by a software reset. The DOR can be written to at any time.

	7	6	5	4	3	2	1	0
	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMAEN	nRESET	DRIVE SEL1	DRIVE SEL0
RESET COND.	0	0	0	0	0	0	0	0

BIT 0 and 1 DRIVE SELECT

These two bits are binary encoded for the four drive selects DS0 -DS3, thereby allowing only one drive to be selected at one time.

BIT 2 nRESET

A logic "0" written to this bit resets the Floppy disk controller. This reset will remain active until a logic "1" is written to this bit. This software reset does not affect the DSR and CCR registers, nor does it affect the other bits of the DOR register. The minimum reset duration required is 100ns, therefore toggling this bit by consecutive writes to this register is a valid method of issuing a software reset.

BIT 3 DMAEN

PC/AT and Model 30 Mode:

Writing this bit to logic "1" will enable the DRQ, nDACK, TC and FINTR outputs. This bit being a logic "0" will disable the nDACK and TC inputs, and hold the DRQ and FINTR outputs in a high impedance state. This bit is a logic "0" after a reset and in these modes.

PS/2 Mode: In this mode the DRQ, nDACK, TC and FINTR pins are always enabled. During a reset, the DRQ, nDACK, TC, and FINTR pins will remain enabled, but this bit will be cleared to a logic "0".

BIT 4 MOTOR ENABLE 0

This bit controls the MTR0 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 5 MOTOR ENABLE 1

This bit controls the MTR1 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 6 MOTOR ENABLE 2

This bit controls the MTR2 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 7 MOTOR ENABLE 3

This bit controls the MTR3 disk interface output. A logic "1" in this bit causes the output to go active.

Table 3 - Drive Activation Values

DRIVE	DOR VALUE
0	1CH
1	2DH
2	4EH
3	8FH

TAPE DRIVE REGISTER (TDR)

Address 3F3 READ/WRITE

This register is included for 82077 software compatability. The robust digital data separator used in the FDC does not require its characteristics modified for tape support. The contents of this register are not used internal to the device. The TDR is unaffected by a software reset. Bits 2-7 are tri-stated when read in this mode.

Table 4- Tape Select Bits

TAPE SEL1	TAPE SEL2	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

Table 5 - Internal 2 Drive Decode - Normal

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	X	X	1	0	0	1	0	nBIT 5	nBIT 4
X	X	1	X	0	1	0	1	nBIT 5	nBIT 4
X	1	X	X	1	0	1	1	nBIT 5	nBIT 4
1	X	X	X	1	1	1	1	nBIT 5	nBIT 4
0	0	0	0	X	X	1	1	nBIT 5	nBIT 4

Table 6 - Internal 2 Drive Decode - Drives 0 and 1 Swapped

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	X	X	1	0	0	0	1	nBIT 4	nBIT 5
X	X	1	X	0	1	1	0	nBIT 4	nBIT 5
X	1	X	X	1	0	1	1	nBIT 4	nBIT 5
1	X	X	X	1	1	1	1	nBIT 4	nBIT 5
0	0	0	0	X	X	1	1	nBIT 4	nBIT 5

Normal Floppy Mode

Normal mode. Register 3F3 contains only bits 0 and 1. When this register is read, bits 2 - 7 are a high impedance.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	tape sel1	tape sel0

Enhanced Floppy Mode 2 (OS2)

Register 3F3 for Enhanced Floppy Mode 2 operation.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Media ID1	Media ID0	Drive Type ID		Floppy Boot Drive		tape sel1	tape sel0

For this mode, MEDIA_ID[1:0] pins are gated into bits 6 and 7 of the 3F3 register. These two bits are not affected by a hard or soft reset.

BIT 7 MEDIA ID 1 READ ONLY (Pin 19) (See Table 7)

BIT 6 MEDIA ID 0 READ ONLY (Pin 20) (See Table 8)

BITS 5 and 4 Drive Type ID - These bits reflect two of the bits of L0-CRF1. Which two bits these are depends on the last drive selected in the Digital Output Register (3F2). (See Table 9)

Note: L0-CRF1-B5 = Logical Device 0, Configuration Register F1, Bit 5

BITS 3 and 2 Floppy Boot Drive - These bits reflect the value of L0-CRF1. Bit 3 = L0-CRF1-B7. Bit 2 = L0-CRF1-B6.

Bits 1 and 0 - Tape Drive Select (READ/WRITE). Same as in Normal and Enhanced Floppy Mode. 1.

Table 9 - Drive Type ID

Table 7 - Media ID1

Input	**MEDIA ID1**	
	BIT 7	
Pin 19	L0-CRF1-B5 = 0	L0-CRF1-B5 = 1
0	0	1
1	1	0

Table 8 - Media ID0

Input	**MEDIA ID0**	
	BIT 6	
Pin 20	CRF1-B4 = 0	CRF1-B4 = 1
0	0	1
1	1	0

Digital Output Register		Register 3F3 - Drive Type ID	
Bit 1	Bit 0	Bit 5	Bit 4
0	0	L0-CRF2 - B1	L0-CRF2 - B0
0	1	L0-CRF2 - B3	L0-CRF2 - B2
1	0	L0-CRF2 - B5	L0-CRF2 - B4
1	1	L0-CRF2 - B7	L0-CRF2 - B6

Note: L0-CRF2-Bx = Logical Device 0, Configuration Register F2, Bit x.

DATA RATE SELECT REGISTER (DSR)

Address 3F4 WRITE ONLY

This register is write only. It is used to program the data rate, amount of write precompensation, power down status, and software reset. The data rate is programmed using the Configuration Control Register (CCR) not the DSR, for PC/AT and PS/2 Model 30 and Microchannel applications. Other applications can set the data rate in the DSR. The data rate of the floppy controller is the most recent write of either the DSR or CCR. The DSR is unaffected by a software reset. A hardware reset will set the DSR to 02H, which corresponds to the default precompensation setting and 250 Kbps.

	7	6	5	4	3	2	1	0
	S/W RESET	POWER DOWN	0	PRE-COMP2	PRE-COMP1	PRE-COMP0	DRATE SEL1	DRATE SEL0
RESET COND.	0	0	0	0	0	0	1	0

BIT 0 and 1 DATA RATE SELECT

These bits control the data rate of the floppy controller. See Table 11 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BIT 2 through 4 PRECOMPENSATION SELECT

These three bits select the value of write precompensation that will be applied to the WDATA output signal. Table 10 shows the precompensation values for the combination of these bits settings. Track 0 is the default starting track number to start precompensation. this starting track number can be changed by the configure command.

BIT 5 UNDEFINED

Should be written as a logic "0".

BIT 6 LOW POWER

A logic "1" written to this bit will put the floppy controller into manual low power mode. The floppy controller clock and data separator circuits will be turned off. The controller will come out of manual low power mode after a software reset or access to the Data Register or Main Status Register.

BIT 7 SOFTWARE RESET

This active high bit has the same function as the DOR RESET (DOR bit 2) except that this bit is self clearing.

Table 10 - Precompensation Delays

PRECOMP 432	**PRECOMPENSATION DELAY** (nsec)	
	<2Mbps	2Mbps
111	0.00	0
001	41.67	20.8
010	83.34	41.7
011	125.00	62.5
100	166.67	83.3
101	208.33	104.2
110	250.00	125
000	Default	Default

Default: See Table 12

Table 11 - Data Rates

DRIVE RATE		DATA RATE		DATA RATE		DENSEL	DRATE(1)	
DRT1	DRT0	SEL1	SEL0	MFM	FM		1	0
0	0	1	1	1Meg	---	1	1	1
0	0	0	0	500	250	1	0	0
0	0	0	1	300	150	0	0	1
0	0	1	0	250	125	0	1	0
0	1	1	1	1Meg	---	1	1	1
0	1	0	0	500	250	1	0	0
0	1	0	1	500	250	0	0	1
0	1	1	0	250	125	0	1	0
1	0	1	1	1Meg	---	1	1	1
1	0	0	0	500	250	1	0	0
1	0	0	1	2Meg	---	0	0	1
1	0	1	0	250	125	0	1	0

Drive Rate Table (Recommended) 00 = 360K, 1.2M, 720K, 1.44M and 2.88M Vertical Format
01 = 3-Mode Drive
10 = 2 Meg Tape

Note 1: The DRATE and DENSEL values are mapped onto the DRIVEDEN pins.

Table 12 - DRVDEN Mapping

DT1	DT0	DRVDEN1 (1)	DRVDEN0 (1)	DRIVE TYPE
0	0	DRATE0	DENSEL	4/2/1 MB 3.5" 2/1 MB 5.25" FDDS 2/1.6/1 MB 3.5" (3-MODE)
1	0	DRATE0	DRATE1	
0	1	DRATE0	nDENSEL	PS/2
1	1	DRATE1	DRATE0	

Table 13 - Default Precompensation Delays

DATA RATE	PRECOMPENSATION DELAYS
2 Mbps	20.8 ns
1 Mbps	41.67 ns
500 Kbps	125 ns
300 Kbps	125 ns
250 Kbps	125 ns

*The 2 Mbps data rate is only available if V_{CC} = 5V.

MAIN STATUS REGISTER

Address 3F4 READ ONLY

The Main Status Register is a read-only register and indicates the status of the disk controller. The Main Status Register can be read at any time. The MSR indicates when the disk controller is ready to receive data via the Data Register. It should be read before each byte transferring to or from the data register except in DMA mode. No delay is required when reading the MSR after a data transfer.

7	6	5	4	3	2	1	0
RQM	DIO	NON DMA	CMD BUSY	DRV3 BUSY	DRV2 BUSY	DRV1 BUSY	DRV0 BUSY

BIT 0 - 3 DRV x BUSY

These bits are set to 1s when a drive is in the seek portion of a command, including implied and overlapped seeks and recalibrates.

BIT 4 COMMAND BUSY

This bit is set to a 1 when a command is in progress. This bit will go active after the command byte has been accepted and goes inactive at the end of the results phase. If there is no result phase (Seek, Recalibrate commands), this bit is returned to a 0 after the last command byte.

BIT 5 NON-DMA

This mode is selected in the SPECIFY command and will be set to a 1 during the execution phase of a command. This is for polled data transfers and helps differentiate between the data transfer phase and the reading of result bytes.

BIT 6 DIO

Indicates the direction of a data transfer once a RQM is set. A 1 indicates a read and a 0 indicates a write is required.

BIT 7 RQM

Indicates that the host can transfer data if set to a 1. No access is permitted if set to a 0.

DATA REGISTER (FIFO)

Address 3F5 READ/WRITE

All command parameter information, disk data and result status are transferred between the host processor and the floppy disk controller through the Data Register. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The Data Register defaults to FIFO disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the Configure command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. Table 14 gives several examples of the delays with a FIFO. The data is based upon the following formula:

$$\text{Threshold \#} \times \left| \frac{1 \times 8}{\text{DATA RATE}} \right| - 1.5\mu s = \text{DELAY}$$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the command execution phase is entered, the FIFO is cleared of any data to ensure that invalid data is not transferred.

An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

Table 14 - FIFO Service Delay

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 2 Mbps* DATA RATE
1 byte	1 x 4 µs - 1.5 µs = 2.5 µs
2 bytes	2 x 4 µs - 1.5 µs = 6.5 µs
8 bytes	8 x 4 µs - 1.5 µs = 30.5 µs
15 bytes	15 x 4 µs - 1.5 µs = 58.5 µs

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 1 Mbps DATA RATE
1 byte	1 x 8 µs - 1.5 µs = 6.5 µs
2 bytes	2 x 8 µs - 1.5 µs = 14.5 µs
8 bytes	8 x 8 µs - 1.5 µs = 62.5 µs
15 bytes	15 x 8 µs - 1.5 µs = 118.5 µs

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 500 Kbps DATA RATE
1 byte	1 x 16 µs - 1.5 µs = 14.5 µs
2 bytes	2 x 16 µs - 1.5 µs = 30.5 µs
8 bytes	8 x 16 µs - 1.5 µs = 126.5 µs
15 bytes	15 x 16 µs - 1.5 µs = 238.5 µs

*The 2 Mbps data rate is only available if V_{CC} = 5V.

DIGITAL INPUT REGISTER (DIR)

Address 3F7 READ ONLY
This register is read-only in all modes.

PC-AT Mode

	7	6	5	4	3	2	1	0
	DSK CHG							
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

BIT 0 - 6 UNDEFINED
The data bus outputs D0 - 6 will remain in a high impedance state during a read of this register.

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable.

PS/2 Mode

	7	6	5	4	3	2	1	0
	DSK CHG	1	1	1	1	DRATE SEL1	DRATE SEL0	nHIGH nDENS
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1

BIT 0 nHIGH DENS
This bit is low whenever the 500 Kbps or 1 Mbps data rates are selected, and high when 250 Kbps and 300 Kbps are selected.

BITS 1 - 2 DATA RATE SELECT
These bits control the data rate of the floppy controller. See Table 11 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BITS 3 - 6 UNDEFINED
Always read as a logic "1"

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable.

Model 30 Mode

	7	6	5	4	3	2	1	0
	DSK CHG	0	0	0	DMAEN	NOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	0	0	0	0	0	1	0

BITS 0 - 1 DATA RATE SELECT
These bits control the data rate of the floppy controller. See Table 11 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BIT 2 NOPREC
This bit reflects the value of NOPREC bit set in the CCR register.

BIT 3 DMAEN
This bit reflects the value of DMAEN bit set in the DOR register bit 3.

BITS 4 - 6 UNDEFINED
Always read as a logic "0"

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the pin.

CONFIGURATION CONTROL REGISTER (CCR)

Address 3F7 WRITE ONLY
PC/AT and PS/2 Modes

	7	6	5	4	3	2	1	0
							DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

BIT 0 and 1 DATA RATE SELECT 0 and 1
These bits determine the data rate of the floppy controller. See Table 11 for the appropriate values.

BIT 2 - 7 RESERVED
Should be set to a logical "0"

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
						NOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

BIT 0 and 1 DATA RATE SELECT 0 and 1
These bits determine the data rate of the floppy controller. See Table 11 for the appropriate values.

BIT 2 NO PRECOMPENSATION
This bit can be set by software, but it has no functionality. It can be read by bit 2 of the DSR when in Model 30 register mode. Unaffected by software reset.

BIT 3 - 7 RESERVED
Should be set to a logical "0"

Table 12 shows the state of the DENSEL pin. The DENSEL pin is set high after a hardware reset and is unaffected by the DOR and the DSR resets.

STATUS REGISTER ENCODING

During the Result Phase of certain commands, the Data Register contains data bytes that give the status of the command just executed.

Table 15 - Status Register 0

BIT NO.	SYMBOL	NAME	DESCRIPTION
7,6	IC	Interrupt Code	00 - Normal termination of command. The specified command was properly executed and completed without error. 01 - Abnormal termination of command. Command execution was started, but was not successfully completed. 10 - Invalid command. The requested command could not be executed. 11 - Abnormal termination caused by Polling.
5	SE	Seek End	The FDC completed a Seek, Relative Seek or Recalibrate command (used during a Sense Interrupt Command).
4	EC	Equipment Check	The TRK0 pin failed to become a "1" after: 1. 80 step pulses in the Recalibrate command. 2. The Relative Seek command caused the FDC to step outward beyond Track 0.
3			Unused. This bit is always "0".
2	H	Head Address	The current head address.
1,0	DS1,0	Drive Select	The current selected drive.

Table 16 - Status Register 1

BIT NO.	SYMBOL	NAME	DESCRIPTION
7	EN	End of Cylinder	The FDC tried to access a sector beyond the final sector of the track (255D). Will be set if TC is not issued after Read or Write Data command.
6			Unused. This bit is always "0".
5	DE	Data Error	The FDC detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overrun/ Underrun	Becomes set if the FDC does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3			Unused. This bit is always "0".
2	ND	No Data	Any one of the following: 1. Read Data, Read Deleted Data command - the FDC did not find the specified sector. 2. Read ID command - the FDC cannot read the ID field without an error. 3. Read A Track command - the FDC cannot find the proper sector sequence.
1	NW	Not Writable	WP pin became a "1" while the FDC is executing a Write Data, Write Deleted Data, or Format A Track command.
0	MA	Missing Address Mark	Any one of the following: 1. The FDC did not detect an ID address mark at the specified track after encountering the index pulse from the IDX pin twice. 2. The FDC cannot detect a data address mark or a deleted data address mark on the specified track.

Table 17 - Status Register 2

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	CM	Control Mark	Any one of the following: 1. Read Data command - the FDC encountered a deleted data address mark. 2. Read Deleted Data command - the FDC encountered a data address mark.
5	DD	Data Error in Data Field	The FDC detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC.
3			Unused. This bit is always "0".
2			Unused. This bit is always "0".
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FF hex, which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The FDC cannot detect a data address mark or a deleted data address mark.

Table 18- Status Register 3

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	WP	Write Protected	Indicates the status of the WP pin.
5			Unused. This bit is always "1".
4	T0	Track 0	Indicates the status of the TRK0 pin.
3			Unused. This bit is always "1".
2	HD	Head Address	Indicates the status of the HDSEL pin.
1,0	DS1,0	Drive Select	Indicates the status of the DS1, DS0 pins.

RESET

There are three sources of system reset on the FDC: the RESET pin of the FDC, a reset generated via a bit in the DOR, and a reset generated via a bit in the DSR. At power on, a Power On Reset initializes the FDC. All resets take the FDC out of the power down state.

All operations are terminated upon a RESET, and the FDC enters an idle state. A reset while a disk write is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, including the Configure command information, and the FDC waits for a new command. Drive polling will start unless disabled by a new Configure command.

RESET Pin (Hardware Reset)

The RESET pin is a global reset and clears all registers except those programmed by the Specify command. The DOR reset bit is enabled and must be cleared by the host to exit the reset state.

DOR Reset vs. DSR Reset (Software Reset)

These two resets are functionally the same. Both will reset the FDC core, which affects drive status information and the FIFO circuits. The DSR reset clears itself automatically while the DOR reset requires the host to manually clear it. DOR reset has precedence over the DSR reset. The DOR reset is set automatically upon a pin reset. The user must manually clear this reset bit in the DOR to exit the reset state.

MODES OF OPERATION

The FDC has three modes of operation, PC/AT mode, PS/2 mode and Model 30 mode. These are determined by the state of the IDENT and MFM bits 6 and 5 respectively of CRxx.

PC/AT mode - (IDENT high, MFM a "don't care")
The PC/AT register set is enabled, the DMA enable bit of the DOR becomes valid (FINTR and DRQ can be hi Z), and TC and DENSEL become active high signals.

PS/2 mode - (IDENT low, MFM high)
This mode supports the PS/2 models 50/60/80 configuration and register set. The DMA bit of the DOR becomes a "don't care", (FINTR and DRQ are always valid), TC and DENSEL become active low.

Model 30 mode - (IDENT low, MFM low)
This mode supports PS/2 Model 30 configuration and register set. The DMA enable bit of ther DOR becomes valid (FINTR and DRQ can be hi Z), TC is active high and DENSEL is active low.

DMA TRANSFERS

DMA transfers are enabled with the Specify command and are initiated by the FDC by activating the FDRQ pin during a data transfer command. The FIFO is enabled directly by asserting nDACK and addresses need not be valid.

Note that if the DMA controller (i.e. 8237A) is programmed to function in verify mode, a pseudo read is performed by the FDC based only on nDACK. This mode is only available when the FDC has been configured into byte mode (FIFO disabled) and is programmed to do a read. With the FIFO enabled, the FDC can perform the above operation by using the new Verify command; no DMA operation is needed.

CONTROLLER PHASES

For simplicity, command handling in the FDC can be divided into three phases: Command, Execution, and Result. Each phase is described in the following sections.

Command Phase

After a reset, the FDC enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the FDC before the command phase is complete. (Please refer to Table 19 for the command set descriptions.) These bytes of data must be transferred in the order prescribed.

Before writing to the FDC, the host must examine the RQM and DIO bits of the Main Status Register. RQM and DIO must be equal to "1" and "0" respectively before command bytes may be written. RQM is set false by the FDC after each write cycle until the received byte is processed. The FDC asserts RQM again to request each parameter byte of the command unless an illegal command condition is detected. After the last parameter byte is received, RQM remains "0" and the FDC automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to provide for the proper handling of the "Invalid Command" condition.

Execution Phase

All data transfers to or from the FDC occur during the execution phase, which can proceed in DMA or non-DMA mode as indicated in the Specify command.

After a reset, the FIFO is disabled. Each data byte is transferred by an FINT or FDRQ depending on the DMA mode. The Configure command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> is defined as the number of bytes available to the FDC when service is requested from the host and ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

Non-DMA Mode - Transfers from the FIFO to the Host

The FINT pin and RQM bits in the Main Status Register are activated when the FIFO contains (16-<threshold>) bytes or the last bytes of a full sector have been placed in the FIFO. The FINT pin can be used for interrupt-driven systems, and RQM can be used for polled systems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. The FDC will deactivate the FINT pin and RQM bit when the FIFO becomes empty.

Non-DMA Mode - Transfers from the Host to the FIFO

The FINT pin and RQM bit in the Main Status Register are activated upon entering the execution phase of data transfer commands. The host must respond to the request by writing data into the FIFO. The FINT pin and RQM bit remain true until the FIFO becomes full. They are set true again when the FIFO has <threshold> bytes remaining in the FIFO. The FINT pin will also be deactivated if TC and nDACK both go inactive. The FDC enters the result phase after the last byte is taken by the FDC from the FIFO (i.e. FIFO empty condition).

DMA Mode - Transfers from the FIFO to the Host

The FDC activates the DDRQ pin when the FIFO contains (16 - <threshold>) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The FDC will deactivate the DDRQ pin when the FIFO becomes empty. FDRQ goes inactive after nDACK goes active for the last byte of a data transfer (or on the active edge of nIOR, on the last byte, if no edge is present on nDACK). A data underrun may occur if FDRQ is not removed in time to prevent an unwanted cycle.

DMA Mode - Transfers from the Host to the FIFO

The FDC activates the FDRQ pin when entering the execution phase of the data transfer commands. The DMA controller must respond by activating the nDACK and nIOW pins and placing data in the FIFO. FDRQ remains active until the FIFO becomes full. FDRQ is again set true when the FIFO has <threshold> bytes remaining in the FIFO. The FDC will also deactivate the FDRQ pin when TC becomes true (qualified by nDACK), indicating that no more data is required. FDRQ goes inactive after nDACK goes active for the last byte of a data transfer (or on the active edge of nIOW of the last byte, if no edge is present on nDACK). A data overrun may occur if FDRQ is not removed in time to prevent an unwanted cycle.

Data Transfer Termination

The FDC supports terminal count explicitly through the TC pin and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multi-sector transfer.

If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the FDC will continue to complete the sector as if a hardware TC was received. The only difference between these implicit functions and TC is that they return "abnormal termination" result status. Such status indications can be ignored if they were expected.

Note that when the host is sending data to the FIFO of the FDC, the internal sector count will be complete when the FDC reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the FDC to read the last 16 bytes from the FIFO. The host must tolerate this delay.

Result Phase

The generation of FINT determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the FDC before the result phase is complete. These bytes of data must be read out for another command to start.

RQM and DIO must both equal "1" before the result bytes may be read. After all the result bytes have been read, the RQM and DIO bits switch to "1" and "0" respectively, and the CB bit is cleared, indicating that the FDC is ready to accept the next command.

COMMAND SET/DESCRIPTIONS

Commands can be written whenever the FDC is in the command phase. Each command has a unique set of needed parameters and status results. The FDC checks to see that the first byte is a valid command and, if valid, proceeds with the command. If it is invalid, an interrupt is issued. The user sends a Sense Interrupt Status command which returns an invalid command error. Refer to Table 19 for explanations of the various symbols used. Table 20 lists the required parameters and the results associated with each command that the FDC is capable of performing.

Table 19 - Description of Command Symbols

<table>
<tr><th>SYMBOL</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>C</td><td>Cylinder Address</td><td>The currently selected address; 0 to 255.</td></tr>
<tr><td>D</td><td>Data Pattern</td><td>The pattern to be written in each sector data field during formatting.</td></tr>
<tr><td>D0, D1, D2, D3</td><td>Drive Select 0-3</td><td>Designates which drives are perpendicular drives on the Perpendicular Mode Command. A "1" indicates a perpendicular drive.</td></tr>
<tr><td>DIR</td><td>Direction Control</td><td>If this bit is 0, then the head will step out from the spindle during a relative seek. If set to a 1, the head will step in toward the spindle.</td></tr>
<tr><td>DS0, DS1</td><td>Disk Drive Select</td><td><table><tr><th>DS1</th><th>DS0</th><th>DRIVE</th></tr><tr><td>0</td><td>0</td><td>drive 0</td></tr><tr><td>0</td><td>1</td><td>drive 1</td></tr><tr><td>1</td><td>0</td><td>drive 2</td></tr><tr><td>1</td><td>1</td><td>drive 3</td></tr></table></td></tr>
<tr><td>DTL</td><td>Special Sector Size</td><td>By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.</td></tr>
<tr><td>EC</td><td>Enable Count</td><td>When this bit is "1" the "DTL" parameter of the Verify command becomes SC (number of sectors per track).</td></tr>
<tr><td>EFIFO</td><td>Enable FIFO</td><td>This active low bit when a 0, enables the FIFO. A "1" disables the FIFO (default).</td></tr>
<tr><td>EIS</td><td>Enable Implied Seek</td><td>When set, a seek operation will be performed before executing any read or write command that requires the C parameter in the command phase. A "0" disables the implied seek.</td></tr>
<tr><td>EOT</td><td>End of Track</td><td>The final sector number of the current track.</td></tr>
</table>

Table 19 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
GAP		Alters Gap 2 length when using Perpendicular Mode.
GPL	Gap Length	The Gap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field).
H/HDS	Head Address	Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.
HLT	Head Load Time	The time interval that FDC waits after loading the head and before initializing a read or write operation. Refer to the Specify command for actual delays.
HUT	Head Unload Time	The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the Specify command for actual delays.
LOCK		Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE COMMAND can be reset to their default values by a "software Reset". (A reset caused by writing to the appropriate bits of either tha DSR or DOR)
MFM	MFM/FM Mode Selector	A one selects the double density (MFM) mode. A zero selects single density (FM) mode.
MT	Multi-Track Selector	When set, this flag selects the multi-track operating mode. In this mode, the FDC treats a complete cylinder under head 0 and 1 as a single track. The FDC operates as this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector under head 1 when the FDC finishes operating on the last sector under head 0.

Table 19 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
N	Sector Size Code	This specifies the number of bytes in a sector. If this parameter is "00", then the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the "N'th" power) times 128. All values up to "07" hex are allowable. "07"h would equal a sector size of 16k. It is the user's responsibility to not select combinations that are not possible with the drive. **N** **SECTOR SIZE** 00 128 bytes 01 256 bytes 02 512 bytes 03 1024 bytes .. ... 07 16 Kbytes
NCN	New Cylinder Number	The desired cylinder number.
ND	Non-DMA Mode Flag	When set to 1, indicates that the FDC is to operate in the non-DMA mode. In this mode, the host is interrupted for each data transfer. When set to 0, the FDC operates in DMA mode, interfacing to a DMA controller by means of the DRQ and nDACK signals.
OW	Overwrite	The bits D0-D3 of the Perpendicular Mode Command can only be modified if OW is set to 1. OW id defined in the Lock command.
PCN	Present Cylinder Number	The current position of the head at the completion of Sense Interrupt Status command.
POLL	Polling Disable	When set, the internal polling routine is disabled. When clear, polling is enabled.
PRETRK	Precompensation Start Track Number	Programmable from track 00 to FFH.
R	Sector Address	The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.
RCN	Relative Cylinder Number	Relative cylinder offset from present cylinder as used by the Relative Seek command.
SC	Number of Sectors Per Track	The number of sectors per track to be initialized by the Format command. The number of sectors per track to be verified during a

Table 19 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
		Verify command when EC is set.
SK	Skip Flag	When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of Read Data. If Read Deleted is executed, only sectors with a deleted address mark will be accessed. When set to "0", the sector is read or written the same as the read and write commands.
SRT	Step Rate Interval	The time interval between step pulses issued by the FDC. Programmable from 0.5 to 8 milliseconds in increments of 0.5 ms at the 1 Mbit data rate. Refer to the SPECIFY command for actual delays.
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Registers within the FDC which store status information after a command has been executed. This status information is available to the host during the result phase after command execution.
WGATE	Write Gate	Alters timing of WE to allow for pre-erase loads in perpendicular drives.

INSTRUCTION SET

Table 20 - Instruction Set

READ DATA										
PHASE	**R/W**	**DATA BUS**								**REMARKS**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	-------- C --------								Sector ID information prior to Command execution.
	W	-------- H --------								
	W	-------- R --------								
	W	-------- N --------								
	W	------- EOT -------								
	W	------- GPL -------								
	W	------- DTL -------								
Execution										Data transfer between the FDD and system.
Result	R	------- ST0 -------								Status information after Command execution.
	R	------- ST1 -------								
	R	------- ST2 -------								
	R	-------- C --------								Sector ID information after Command execution.
	R	-------- H --------								
	R	-------- R --------								
	R	-------- N --------								

READ DELETED DATA										
PHASE	**R/W**	**DATA BUS**								**REMARKS**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	-------- C --------								Sector ID information prior to Command execution.
	W	-------- H --------								
	W	-------- R --------								
	W	-------- N --------								
	W	------- EOT -------								
	W	------- GPL -------								
	W	------- DTL -------								
Execution										Data transfer between the FDD and system.
Result	R	------- ST0 -------								Status information after Command execution.
	R	------- ST1 -------								
	R	------- ST2 -------								
	R	-------- C --------								Sector ID information after Command execution.
	R	-------- H --------								
	R	-------- R --------								
	R	-------- N --------								

WRITE DATA										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	-------- C --------								Sector ID information prior to Command execution.
	W	-------- H --------								
	W	-------- R --------								
	W	-------- N --------								
	W	------- EOT -------								
	W	------- GPL -------								
	W	------- DTL -------								
Execution										Data transfer between the FDD and system.
Result	R	------- ST0 -------								Status information after Command execution.
	R	------- ST1 -------								
	R	------- ST2 -------								
	R	-------- C --------								Sector ID information after Command execution.
	R	-------- H --------								
	R	-------- R --------								
	R	-------- N --------								

WRITE DELETED DATA									
PHASE	**R/W**	**DATA BUS**							**REMARKS**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	- - - - - - - - C - - - - - - - -								Sector ID information prior to Command execution.
	W	- - - - - - - - H - - - - - - - -								
	W	- - - - - - - - R - - - - - - - -								
	W	- - - - - - - - N - - - - - - - -								
	W	- - - - - - - EOT - - - - - - -								
	W	- - - - - - - GPL - - - - - - -								
	W	- - - - - - - DTL - - - - - - -								
Execution										Data transfer between the FDD and system.
Result	R	- - - - - - - ST0 - - - - - - -								Status information after Command execution.
	R	- - - - - - - ST1 - - - - - - -								
	R	- - - - - - - ST2 - - - - - - -								
	R	- - - - - - - - C - - - - - - - -								Sector ID information after Command execution.
	R	- - - - - - - - H - - - - - - - -								
	R	- - - - - - - - R - - - - - - - -								
	R	- - - - - - - - N - - - - - - - -								

READ A TRACK									
PHASE	**R/W**	**DATA BUS**							**REMARKS**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	-------- C --------								Sector ID information prior to Command execution.
	W	-------- H --------								
	W	-------- R --------								
	W	-------- N --------								
	W	-------- EOT --------								
	W	-------- GPL --------								
	W	-------- DTL --------								
Execution										Data transfer between the FDD and system. FDC reads all of cylinders' contents from index hole to EOT.
Result	R	-------- ST0 --------								Status information after Command execution.
	R	-------- ST1 --------								
	R	-------- ST2 --------								
	R	-------- C --------								Sector ID information after Command execution.
	R	-------- H --------								
	R	-------- R --------								
	R	-------- N --------								

VERIFY									
PHASE	**R/W**	**DATA BUS**							**REMARKS**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	- - - - - - - - C - - - - - - - -								Sector ID information prior to Command execution.
	W	- - - - - - - - H - - - - - - - -								
	W	- - - - - - - - R - - - - - - - -								
	W	- - - - - - - - N - - - - - - - -								
	W	- - - - - - - EOT - - - - - - -								
	W	- - - - - - - GPL - - - - - - -								
	W	- - - - - - DTL/SC - - - - - -								
Execution										No data transfer takes place.
Result	R	- - - - - - - ST0 - - - - - - -								Status information after Command execution.
	R	- - - - - - - ST1 - - - - - - -								
	R	- - - - - - - ST2 - - - - - - -								
	R	- - - - - - - - C - - - - - - - -								Sector ID information after Command execution.
	R	- - - - - - - - H - - - - - - - -								
	R	- - - - - - - - R - - - - - - - -								
	R	- - - - - - - - N - - - - - - - -								

VERSION									
PHASE	**R/W**	**DATA BUS**							**REMARKS**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	W	0	0	0	1	0	0	0	0	Command Code
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

FORMAT A TRACK									
PHASE	**R/W**	**DATA BUS**							**REMARKS**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	-------- N --------								Bytes/Sector
	W	-------- SC --------								Sectors/Cylinder
	W	------- GPL -------								Gap 3
	W	-------- D --------								Filler Byte
Execution for Each Sector Repeat:	W	-------- C --------								Input Sector Parameters
	W	-------- H --------								
	W	-------- R --------								
	W	-------- N --------								
										FDC formats an entire cylinder
Result	R	------- ST0 -------								Status information after Command execution
	R	------- ST1 -------								
	R	------- ST2 -------								
	R	------ Undefined ------								
	R	------ Undefined ------								
	R	------ Undefined ------								
	R	------ Undefined ------								

RECALIBRATE										
PHASE	**R/W**	**DATA BUS**								**REMARKS**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt.

SENSE INTERRUPT STATUS										
PHASE	**R/W**	**DATA BUS**								**REMARKS**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	- - - - - - - ST0 - - - - - - -								Status information at the end of each seek operation.
	R	- - - - - - - PCN - - - - - - -								

SPECIFY										
PHASE	**R/W**	**DATA BUS**								**REMARKS**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	- - - SRT - - -				- - - HUT - - -				
	W	- - - - - - HLT - - - - - -							ND	

SENSE DRIVE STATUS										
PHASE	**R/W**	**DATA BUS**								**REMARKS**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	- - - - - - - ST3 - - - - - - -								Status information about FDD

SEEK										
PHASE	**R/W**	**DATA BUS**								**REMARKS**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	- - - - - - - NCN - - - - - - -								
Execution										Head positioned over proper cylinder on diskette.

CONFIGURE										
PHASE	**R/W**	**DATA BUS**								**REMARKS**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	0	0	1	0	0	1	1	Configure Information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL	- - - FIFOTHR - - -				
Execution	W	- - - - - - - - - PRETRK - - - - - - - - -								

RELATIVE SEEK									
PHASE	R/W	DATA BUS							REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	------- RCN -------								

DUMPREG									
PHASE	R/W	DATA BUS							REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	1	1	1	0	*Note: Registers placed in FIFO
Execution										
Result	R	------ PCN-Drive 0 -------								
	R	------ PCN-Drive 1 -------								
	R	------ PCN-Drive 2 -------								
	R	------ PCN-Drive 3 -------								
	R	---- SRT ---- | --- HUT ---								
	R	------- HLT ------- | ND								
	R	------- SC/EOT -------								
	R	LOCK	0	D3	D2	D1	D0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL	| -- FIFOTHR --				
	R	-------- PRETRK --------								

READ ID									
PHASE	**R/W**	**DATA BUS**							**REMARKS**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	- - - - - - - - ST0 - - - - - - - -								Status information after Command execution.
										Disk status after the Command has completed
	R	- - - - - - - - ST1 - - - - - - - -								
	R	- - - - - - - - ST2 - - - - - - - -								
	R	- - - - - - - - C - - - - - - - -								
	R	- - - - - - - - H - - - - - - - -								
	R	- - - - - - - - R - - - - - - - -								
	R	- - - - - - - - N - - - - - - - -								

PERPENDICULAR MODE										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	1	0	0	1	0	Command Codes
		OW	0	D3	D2	D1	D0	GAP	WGATE	

INVALID CODES										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	- - - - - Invalid Codes - - - - -								Invalid Command Codes (NoOp - FDC goes into Standby State)
Result	R	- - - - - - - ST0 - - - - - - -								ST0 = 80H

LOCK										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	

SC is returned if the last command that was issued was the Format command. EOT is returned if the last command was a Read or Write.

NOTE: These bits are used internally only. They are not reflected in the Drive Select pins. It is the user's responsibility to maintain correspondence between these bits and the Drive Select pins (DOR).

DATA TRANSFER COMMANDS

All of the Read Data, Write Data and Verify type commands use the same parameter bytes and return the same results information, the only difference being the coding of bits 0-4 in the first byte.

An implied seek will be executed if the feature was enabled by the Configure command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. If the seek portion fails, it will be reflected in the results status normally returned for a Read/Write Data command. Status Register 0 (ST0) would contain the error code and C would contain the cylinder on which the seek failed.

Read Data

A set of nine (9) bytes is required to place the FDC in the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the FDC reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one and the data from the next logical sector is read and output via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of TC, or an implied TC (FIFO overrun/underrun), the FDC stops sending data but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector, terminate the Read Data Command.

N determines the number of bytes per sector (see Table 21 below). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the FDC transfers the specified number of bytes to the host. For reads, it continues to read the entire 128-byte sector and checks for CRC errors. For writes, it completes the 128-byte sector by filling in zeros. If N is not set to 00 Hex, DTL should be set to FF Hex and has no impact on the number of bytes transferred.

Table 21 - Sector Sizes

N	SECTOR SIZE
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	...
07	16 Kbytes

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track) and N (number of bytes/sector).

The Multi-Track function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing the last sector of the same track at Side 1.

If the host terminates a read or write operation in the FDC, the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Refer to Table 22.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify command) has elapsed. If the host issues another command before the head unloads,

then the head settling time may be saved between subsequent reads.

If the FDC detects a pulse on the nINDEX pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the ND bit in Status Register 1 to "1" indicating a sector not found, and terminates the Read Data Command.

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a CRC error occurs in the ID or data field, the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the DE bit flag in Status Register 1 to "1", sets the DD bit in Status Register 2 to "1" if CRC is incorrect in the ID field, and terminates the Read Data Command. Table 23 describes the effect of the SK bit on the Read Data command execution and results. Except where noted in Table 23, the C or R value of the sector address is automatically incremented (see Table 25).

Table 22 - Effects of MT and N Bits

MT	N	MAXIMUM TRANSFER CAPACITY	FINAL SECTOR READ FROM DISK
0	1	256 x 26 = 6,656	26 at side 0 or 1
1	1	256 x 52 = 13,312	26 at side 1
0	2	512 x 15 = 7,680	15 at side 0 or 1
1	2	512 x 30 = 15,360	15 at side 1
0	3	1024 x 8 = 8,192	8 at side 0 or 1
1	3	1024 x 16 = 16,384	16 at side 1

Table 23 - Skip Bit vs Read Data Command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	No	Normal termination.
0	Deleted Data	Yes	Yes	Address not incremented. Next sector not searched for.
1	Normal Data	Yes	No	Normal termination.
1	Deleted Data	No	Yes	Normal termination. Sector not read ("skipped").

Read Deleted Data

This command is the same as the Read Data command, only it operates on sectors that contain a Deleted Data Address Mark at the beginning of a Data Field.

Table 24 describes the effect of the SK bit on the Read Deleted Data command execution and results.

Except where noted in Table 24, the C or R value of the sector address is automatically incremented (see Table 25).

Table 24 - Skip Bit vs. Read Deleted Data Command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	Yes	Address not incremented. Next sector not searched for.
0	Deleted Data	Yes	No	Normal termination.
1	Normal Data	No	Yes	Normal termination. Sector not read ("skipped").
1	Deleted Data	Yes	No	Normal termination.

Read A Track

This command is similar to the Read Data command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the nINDEX pin, the FDC starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The FDC compares the ID information read from each sector with the specified value in the command and sets the ND flag of Status Register 1 to a "1" if there is no comparison. Multi-track or skip operations are not allowed with this command. The MT and SK bits (bits D7 and D5 of the first command byte respectively) should always be set to "0".

This command terminates when the EOT specified number of sectors has not been read. If the FDC does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the IDX pin, then it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

Table 25 - Result Phase Table

MT	HEAD	FINAL SECTOR TRANSFERRED TO HOST	ID INFORMATION AT RESULT PHASE			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	LSB	01	NC

NC: No Change, the same value as the one at the beginning of command execution.
LSB: Least Significant Bit, the LSB of H is complemented.

Write Data

After the Write Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the Specify command), and begins reading ID fields. When the sector address read from the diskette matches the sector address specified in the command, the FDC reads the data from the host via the FIFO and writes it to the sector's data field.

After writing data into the current sector, the FDC computes the CRC value and writes it into the CRC field at the end of the sector transfer. The Sector Number stored in "R" is incremented by one, and the FDC continues writing to the next data field. The FDC continues this "Multi-Sector Write Operation". Upon receipt of a terminal count signal or if a FIFO over/under run occurs while a data field is being written, then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID fields, it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the DE bit of Status Register 1 to "1", and terminates the Write Data command.

The Write Data command operates in much the same manner as the Read Data command. The following items are the same. Please refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) bit
- ND (No Data) bit
- Head Load, Unload Time Interval
- ID information when the host terminates the command
- Definition of DTL when N = 0 and when N does not = 0

Write Deleted Data

This command is almost the same as the Write Data command except that a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

Verify

The Verify command is used to verify the data stored on a disk. This command acts exactly like a Read Data command except that no data is transferred to the host. Data is read from the disk and CRC is computed and checked against the previously-stored value.

Because data is not transferred to the host, TC (pin 89) cannot be used to terminate this command. By setting the EC bit to "1", an implicit TC will be issued to the FDC. This implicit TC will occur when the SC value has decremented to 0 (an SC value of 0 will verify 256 sectors). This command can also be terminated by setting the EC bit to "0" and the EOT value equal to the final sector to be checked. If EC is set to "0", DTL/SC should be programmed to 0FFH. Refer to Table 25 and Table 26 for information concerning the values of MT and EC versus SC and EOT value.

Definitions:

Sectors Per Side = Number of formatted sectors per each side of the disk.

Sectors Remaining = Number of formatted sectors left which can be read, including side 1 of the disk if MT is set to "1".

Table 26 - Verify Command Result Phase Table

MT	EC	SC/EOT VALUE	TERMINATION RESULT
0	0	SC = DTL EOT ≤ # Sectors Per Side	Success Termination Result Phase Valid
0	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
0	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
0	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	0	SC = DTL EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid

NOTE: If MT is set to "1" and the SC value is greater than the number of remaining formatted sectors on Side 0, verifying will continue on Side 1 of the disk.

Format A Track

The Format command allows an entire track to be formatted. After a pulse from the IDX pin is detected, the FDC starts writing data on the disk including gaps, address marks, ID fields, and data fields per the IBM System 34 or 3740 format (MFM or FM respectively). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID field for each sector is supplied by the host; that is, four data bytes per sector are needed by the FDC for C, H, R, and N (cylinder, head, sector number and sector size respectively).

After formatting each sector, the host must send new values for C, H, R and N to the FDC for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the FDC encounters a pulse on the IDX pin again and it terminates the command.

Table 27 contains typical values for gap fields which are dependent upon the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

FORMAT FIELDS

SYSTEM 34 (DOUBLE DENSITY) FORMAT

GAP4a	SYNC	IAM		GAP1	SYNC	IDAM		C	H	S	N	C	GAP2	SYNC	DATA AM		DATA	C	GAP3	GAP 4b
80x 4E	12x 00	3x C2	FC	50x 4E	12x 00	3x A1	FE	Y L	D	E C	O	R C	22x 4E	12x 00	3x A1	FB F8		R C		

SYSTEM 3740 (SINGLE DENSITY) FORMAT

GAP4a	SYNC	IAM	GAP1	SYNC	IDAM	C	H	S	N	C	GAP2	SYNC	DATA AM	DATA	C	GAP3	GAP 4b
40x FF	6x 00	FC	26x FF	6x 00	FE	Y L	D	E C	O	R C	11x FF	6x 00	FB or F8		R C		

PERPENDICULAR FORMAT

GAP4a	SYNC	IAM		GAP1	SYNC	IDAM		C	H	S	N	C	GAP2	SYNC	DATA AM		DATA	C	GAP3	GAP 4b
80x 4E	12x 00	3x C2	FC	50x 4E	12x 00	3x A1	FE	Y L	D	E C	O	R C	41x 4E	12x 00	3x A1	FB F8		R C		

Table 27 - Typical Values for Formatting

	FORMAT	SECTOR SIZE	N	SC	GPL1	GPL2
5.25" Drives	FM	128	00	12	07	09
		128	00	10	10	19
		512	02	08	18	30
		1024	03	04	46	87
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
	MFM	256	01	12	0A	0C
		256	01	10	20	32
		512*	02	09	2A	50
		1024	03	04	80	F0
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
3.5" Drives	FM	128	0	0F	07	1B
		256	1	09	0F	2A
		512	2	05	1B	3A
	MFM	256	1	0F	0E	36
		512**	2	09	1B	54
		1024	3	05	35	74

GPL1 = suggested GPL values in Read and Write commands to avoid splice point between data field and ID field of contiguous sections.
GPL2 = suggested GPL value in Format A Track command.
*PC/AT values (typical)
**PS/2 values (typical). Applies with 1.0 MB and 2.0 MB drives.
NOTE: All values except sector size are in hex.

CONTROL COMMANDS

Control commands differ from the other commands in that no data transfer takes place. Three commands generate an interrupt when complete: Read ID, Recalibrate, and Seek. The other control commands do not generate an interrupt.

Read ID

The Read ID command is used to find the present position of the recording heads. The FDC stores the values from the first ID field it is able to read into its registers. If the FDC does not find an ID address mark on the diskette after the second occurrence of a pulse on the nINDEX pin, it then sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

The following commands will generate an interrupt upon completion. They do not return any result bytes. It is highly recommended that control commands be followed by the Sense Interrupt Status command. Otherwise, valuable interrupt status information will be lost.

Recalibrate

This command causes the read/write head within the FDC to retract to the track 0 position. The FDC clears the contents of the PCN counter and checks the status of the nTR0 pin from the FDD. As long as the nTR0 pin is low, the DIR pin remains 0 and step pulses are issued. When the nTR0 pin goes high, the SE bit in Status Register 0 is set to "1" and the command is terminated. If the nTR0 pin is still low after 79 step pulses have been issued, the FDC sets the SE and the EC bits of Status Register 0 to "1" and terminates the command. Disks capable of handling more than 80 tracks per side may require more than one Recalibrate command to return the head back to physical Track 0.

The Recalibrate command does not have a result phase. The Sense Interrupt Status command must be issued after the Recalibrate command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in a NON-BUSY state. At this time, another Recalibrate command may be issued, and in this manner parallel Recalibrate operations may be done on up to four drives at once.

Upon power up, the software must issue a Recalibrate command to properly initialize all drives and the controller.

Seek

The read/write head within the drive is moved from track to track under the control of the Seek command. The FDC compares the PCN, which is the current head position, with the NCN and performs the following operation if there is a difference:

PCN < NCN: Direction signal to drive set to "1" (step in) and issues step pulses.
PCN > NCN: Direction signal to drive set to "0" (step out) and issues step pulses.

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN the SE bit in Status Register 0 is set to "1" and the command is terminated.

During the command phase of the seek or recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in the NON-BUSY state. At this time, another Seek or Recalibrate command may be issued, and in this manner, parallel seek operations may be done on up to four drives at once.

Note that if implied seek is not enabled, the read and write commands should be preceded by:

1) Seek command - Step to the proper track
2) Sense Interrupt Status command - Terminate the Seek command
3) Read ID - Verify head is on proper track
4) Issue Read/Write command.

The Seek command does not have a result phase. Therefore, it is highly recommended that the Sense Interrupt Status command be issued after the Seek command to terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return to a "0". When exiting POWERDOWN mode, the FDC clears the PCN value and the status information to zero. Prior to issuing the POWERDOWN command, it is highly recommended that the user service all pending interrupts through the Sense Interrupt Status command.

Sense Interrupt Status

An interrupt signal on FINT pin is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data command
   b. Read A Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format A Track command
   g. Write Deleted Data command
   h. Verify command
2. End of Seek, Relative Seek, or Recalibrate command

3. FDC requires a data transfer during the execution phase in the non-DMA mode

The Sense Interrupt Status command resets the interrupt signal and, via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt.

Table 28 - Interrupt Identification

SE	IC	INTERRUPT DUE TO
0	11	Polling
1	00	Normal termination of Seek or Recalibrate command
1	01	Abnormal termination of Seek or Recalibrate command

The Seek, Relative Seek, and Recalibrate commands have no result phase. The Sense Interrupt Status command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in ST0 will always return a "0". If a Sense Interrupt Status is not issued, the drive will continue to be BUSY and may affect the operation of the next command.

Sense Drive Status

Sense Drive Status obtains drive status information. It has not execution phase and goes directly to the result phase from the command phase. Status Register 3 contains the drive status information.

Specify

The Specify command sets the initial values for each of the three internal times. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the

remaining step pulses. The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the read/write operation starts. The values change with the data rate speed selection and are documented in Table 29. The values are the same for MFM and FM.

Table 29 - Drive Control Delays (ms)

	HUT					SRT				
	2M	**1M**	**500K**	**300K**	**250K**	**2M**	**1M**	**500K**	**300K**	**250K**
0	64	128	256	426	512	4	8	16	26.7	32
1	4	8	16	26.7	32	3.75	7.5	15	25	30
..	..	..	..	..	..	..	..	..	..	..
E	56	112	224	373	448	0.5	1	2	3.33	4
F	60	120	240	400	480	0.25	0.5	1	1.67	2

	HLT				
	2M	**1M**	**500K**	**300K**	**250K**
00	64	128	256	426	512
01	0.5	1	2	3.3	4
02	1	2	4	6.7	8
..	..	..	..	..	.
7F	63	126	252	420	504
7F	63.5	127	254	423	508

The choice of DMA or non-DMA operations is made by the ND bit. When this bit is "1", the non-DMA mode is selected, and when ND is "0", the DMA mode is selected. In DMA mode, data transfers are signalled by the FDRQ pin. Non-DMA mode uses the RQM bit and the FINT pin to signal data transfers.

Configure

The Configure command is issued to select the special features of the FDC. A Configure command need not be issued if the default values of the FDC meet the system requirements.

Configure Default Values:
EIS - No Implied Seeks
EFIFO - FIFO Disabled
POLL - Polling Enabled
FIFOTHR - FIFO Threshold Set to 1 Byte
PRETRK - Pre-Compensation Set to Track 0

EIS - Enable Implied Seek. When set to "1", the FDC will perform a Seek operation before executing a read or write command. Defaults to no implied seek.

EFIFO - A "1" disables the FIFO (default). This means data transfers are asked for on a byte-by-byte basis. Defaults to "1", FIFO disabled. The threshold defaults to "1".

POLL - Disable polling of the drives. Defaults to "0", polling enabled. When enabled, a single interrupt is generated after a reset. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR - The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 to 16 bytes. Defaults to

one byte. A "00" selects one byte; "0F" selects 16 bytes.

PRETRK - Pre-Compensation Start Track Number. Programmable from track 0 to 255. Defaults to track 0. A "00" selects track 0; "FF" selects track 255.

Version

The Version command checks to see if the controller is an enhanced type or the older type (765A). A value of 90 H is returned as the result byte.

Relative Seek

The command is coded the same as for Seek, except for the MSB of the first byte and the DIR bit.

DIR Head Step Direction Control

DIR	ACTION
0	Step Head Out
1	Step Head In

RCN Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

The Relative Seek command differs from the Seek command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The Seek command is good for drives that support a maximum of 256 tracks. Relative Seeks cannot be overlapped with other Relative Seeks. Only one Relative Seek can be active at a time. Relative Seeks may be overlapped with Seeks and Recalibrates. Bit 4 of Status Register 0 (EC) will be set if Relative Seek attempts to step outward beyond Track 0.

As an example, assume that a floppy drive has 300 useable tracks. The host needs to read track 300 and the head is on any track (0-255). If a Seek command is issued, the head will stop at track 255. If a Relative Seek command is issued, the FDC will move the head the specified number of tracks, regardless of the internal cylinder position register (but will increment the register). If the head was on track 40 (d), the maximum track that the FDC could position the head on using Relative Seek will be 295 (D), the initial track + 255 (D). The maximum count that the head can be moved with a single Relative Seek command is 255 (D).

The internal register, PCN, will overflow as the cylinder number crosses track 255 and will contain 39 (D). The resulting PCN value is thus (RCN + PCN) mod 256. Functionally, the FDC starts counting from 0 again as the track number goes above 255 (D). It is the user's responsibility to compensate FDC functions (precompensation track number) when accessing tracks greater than 255. The FDC does not keep track that it is working in an "extended track area" (greater than 255). Any command issued will use the current PCN value except for the Recalibrate command, which only looks for the TRACK0 signal. Recalibrate will return an error if the head is farther than 79 due to its limitation of issuing a maximum of 80 step pulses. The user simply needs to issue a second Recalibrate command. The Seek command and implied seeks will function correctly within the 44 (D) track (299-255) area of the "extended track area". It is the user's responsibility not to issue a new track position that will exceed the maximum track that is present in the extended area.

To return to the standard floppy range (0-255) of tracks, a Relative Seek should be issued to cross the track 255 boundary.

A Relative Seek can be used instead of the normal Seek, but the host is required to calculate the difference between the current head location and the new (target) head location. This may require the host to issue a Read ID command to ensure that the head is physically on the track that software assumes it to be. Different FDC commands will return different cylinder results which may be difficult to keep track of with software without the Read ID command.

Perpendicular Mode

The Perpendicular Mode command should be issued prior to executing Read/Write/Format commands that access a disk drive with perpendicular recording capability. With this command, the length of the Gap2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives. Table 30 describes the effects of the WGATE and GAP bits for the Perpendicular Mode command. Upon a reset, the FDC will default to the conventional mode (WGATE = 0, GAP = 0).

Selection of the 500 Kbps and 1 Mbps perpendicular modes is independent of the actual data rate selected in the Data Rate Select Register. The user must ensure that these two data rates remain consistent.

The Gap2 and VCO timing requirements for perpendicular recording type drives are dictated by the design of the read/write head. In the design of this head, a pre-erase head precedes the normal read/write head by a distance of 200 micrometers. This works out to about 38 bytes at a 1 Mbps recording density. Whenever the write head is enabled by the Write Gate signal, the pre-erase head is also activated at the same time. Thus, when the write head is initially turned on, flux transitions recorded on the media for the first 38 bytes will not be preconditioned with the pre-erase head since it has not yet been activated. To accommodate this head activation and deactivation time, the Gap2 field is expanded to a length of 41 bytes. The format field shown on Page 57 illustrates the change in the Gap2 field size for the perpendicular format.

On the read back by the FDC, the controller must begin synchronization at the beginning of the sync field. For the conventional mode, the internal PLL VCO is enabled (VCOEN) approximately 24 bytes from the start of the Gap2 field. But, when the controller operates in the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), VCOEN goes active after 43 bytes to accommodate the increased Gap2 field size. For both cases, and approximate two-byte cushion is maintained from the beginning of the sync field for the purposes of avoiding write splices in the presence of motor speed variation.

For the Write Data case, the FDC activates Write Gate at the beginning of the sync field under the conventional mode. The controller then writes a new sync field, data address mark, data field, and CRC as shown on page 57. With the pre-erase head of the perpendicular drive, the write head must be activated in the Gap2 field to insure a proper write of the new sync field. For the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), 38 bytes will be written in the Gap2 space. Since the bit density is proportional to the data rate, 19 bytes will be written in the Gap2 field for the 500 Kbps perpendicular mode (WGATE = 1, GAP =0).

It should be noted that none of the alterations in Gap2 size, VCO timing, or Write Gate timing affect normal program flow. The information provided here is just for background purposes and is not needed for normal operation. Once the Perpendicular Mode command is invoked, FDC software behavior from the user standpoint is unchanged.

The perpendicular mode command is enhanced to allow specific drives to be designated Perpendicular recording drives. This enhancement allows data transfers between Conventional and Perpendicular drives without

having to issue Perpendicular mode commnds between the accesses of the different drive types, nor having to change write pre-compensation values.

When both GAP and WGATE bits of the PERPENDICULAR MODE COMMAND are both programmed to "0" (Conventional mode), then D0, D1, D2, D3, and D4 can be programmed independently to "1" for that drive to be set automatically to Perpendicular mode. In this mode the following set of conditions also apply:

1. The GAP2 written to a perpendicular drive during a write operation will depend upon the programmed data rate.
2. The write pre-compensation given to a perpendicular mode drive will be 0ns.
3. For D0-D3 programmed to "0" for conventional mode drives any data written will be at the currently programmed write pre-compensation.

Note: Bits D0-D3 can only be overwritten when OW is programmed as a "1".If either GAP or WGATE is a "1" then D0-D3 are ignored.

Software and hardware resets have the following effect on the PERPENDICULAR MODE COMMAND:

1. "Software" resets (via the DOR or DSR registers) will only clear GAP and WGATE bits to "0". D0-D3 are unaffected and retain their previous value.
2. "Hardware" resets will clear all bits (GAP, WGATE and D0-D3) to "0", i.e all conventional mode.

Table 30 - Effects of WGATE and GAP Bits

WGATE	GAP	MODE	LENGTH OF GAP2 FORMAT FIELD	PORTION OF GAP 2 WRITTEN BY WRITE DATA OPERATION
0	0	Conventional	22 Bytes	0 Bytes
0	1	Perpendicular (500 Kbps)	22 Bytes	19 Bytes
1	0	Reserved (Conventional)	22 Bytes	0 Bytes
1	1	Perpendicular (1 Mbps)	41 Bytes	38 Bytes

LOCK

In order to protect systems with long DMA latencies against older application software that can disable the FIFO the LOCK Command has been added. This command should only be used by the FDC routines, and application software should refrain from using it. If an application calls for the FIFO to be disabled then the CONFIGURE command should be used.

The LOCK command defines whether the EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be RESET by the DOR and DSR registers. When the LOCK bit is set to logic "1" all subsequent "software RESETS by the DOR and DSR registers will not change the previously set parameters to their default values. All "hardware" RESET from the RESET pin will set the LOCK bit to logic "0" and return the EFIFO, FIFOTHR, and PRETRK to their default values. A status byte is returned immediately after issuing a a LOCK command. This byte reflects the value of the LOCK bit set by the command byte.

ENHANCED DUMPREG

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug. To accommodate the LOCK command and the enhanced PERPENDICULAR MODE command the eighth byte of the DUMPREG command has been modified to contain the additional data from these two commands.

COMPATIBILITY

The FDC37C93x was designed with software compatibility in mind. It is a fully backwards-compatible solution with the older generation 765A/B disk controllers. The FDC also implements on-board registers for compatibility with the PS/2, as well as PC/AT and PC/XT, floppy disk controller subsystems. After a hardware reset of the FDC, all registers, functions and enhancements default to a PC/AT, PS/2 or PS/2 Model 30 compatible operating mode, depending on how the IDENT and MFM bits are configured by the system BIOS.

SERIAL PORT (UART)

The FDC37C93x incorporates two full function UARTs. They are compatible with the NS16450, the 16450 ACE registers and the NS16550A. The UARTS perform serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 460.8K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UARTs each contain a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. The UARTs are also capable of supporting the MIDI data rate. Refer to the Configuration Registers for information on disabling, power down and changing the base address of the UARTs. The interrupt from a UART is enabled by programming OUT2 of that UART to a logic "1". OUT2 being a logic "0" disables that UART's interrupt. The second UART also supports IrDA, HP-SIR and ASK-IR infrared modes of operation.

REGISTER DESCRIPTION

Addressing of the accessible registers of the Serial Port is shown below. The base addresses of the serial ports are defined by the configuration registers (see Configuration section). The Serial Port registers are located at sequentially increasing addresses above these base addresses. The FDC37C93x contains two serial ports, each of which contain a register set as described below.

Table 31 - Addressing the Serial Port

DLAB*	A2	A1	A0	REGISTER NAME
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control (read/write)
X	1	0	0	Modem Control (read/write)
X	1	0	1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1	1	1	Scratchpad (read/write)
1	0	0	0	Divisor LSB (read/write)
1	0	0	1	Divisor MSB (read/write

*NOTE: DLAB is Bit 7 of the Line Control Register

The following section describes the operation of the registers.

RECEIVE BUFFER REGISTER (RB)
Address Offset = 0H, DLAB = 0, READ ONLY

This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

TRANSMIT BUFFER REGISTER (TB)
Address Offset = 0H, DLAB = 0, WRITE ONLY

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

INTERRUPT ENABLE REGISTER (IER)
Address Offset = 1H, DLAB = 0, READ/WRITE

The lower four bits of this register control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the FDC37C93x. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

Bit 0
This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic "1".

Bit 1
This bit enables the Transmitter Holding Register Empty Interrupt when set to logic "1".

Bit 2
This bit enables the Received Line Status Interrupt when set to logic "1". The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

Bit 3
This bit enables the MODEM Status Interrupt when set to logic "1". This is caused when one of the Modem Status Register bits changes state.

Bits 4 through 7
These bits are always logic "0".

FIFO CONTROL REGISTER (FCR)
Address Offset = 2H, DLAB = X, WRITE

This is a write only register at the same location as the IIR. This register is used to enable and clear the FIFOs, set the RCVR FIFO trigger level. Note: DMA is not supported.

Bit 0
Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic "0" disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

Bit 1
Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0.

The shift register is not cleared. This bit is self-clearing.

Bit 2
Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 3
Writting to this bit has no effect on the operation of the UART. The RXRDY and TXRDY pins are not available on this chip.

Bit 7	Bit 6	RCVR FIFO Trigger Level (BYTES)
0	0	1
0	1	4
1	0	8
1	1	14

Bit 4,5
Reserved

Bit 6,7
These bits are used to set the trigger level for the RCVR FIFO interrupt.

INTERRUPT IDENTIFICATION REGISTER (IIR)
Address Offset = 2H, DLAB = X, READ

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Interrupt Control Table). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

Bit 0
This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic "0", an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic "1", no interrupt is pending.

Bits 1 and 2
These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table.

Bit 3

In non-FIFO mode, this bit is a logic "0". In FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5
These bits of the IIR are always logic "0".

Bits 6 and 7
These two bits are set when the FIFO CONTROL Register bit 0 equals 1.

Table 32 - Interrupt Control Table

FIFO MODE ONLY	INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	**BIT 2**	**BIT 1**	**BIT 0**	**PRIORITY LEVEL**	**INTERRUPT TYPE**	**INTERRUPT SOURCE**	**INTERRUPT RESET CONTROL**
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

LINE CONTROL REGISTER (LCR)
Address Offset = 3H, DLAB = 0, READ/WRITE

This register contains the format information of the serial line. The bit definitions are:

Bits 0 and 1
These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

BIT 1	BIT 0	WORD LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

The Start, Stop and Parity bits are not included in the word length.

Bit 2
This bit specifies the number of stop bits in each transmitted or received serial character. The following table summarizes the information.

Bit 2	WORD LENGTH	NUMBER OF STOP BITS
0	--	1
1	5 Bits	1.5
1	6 Bits	2
1	7 Bits	2
1	8 BIts	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.

Bit 3
Parity Enable bit. When bit 3 is a logic "1", a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).

Bit 4
Even Parity Select bit. When bit 3 is a logic "1" and bit 4 is a logic "0", an odd number of logic "1"'s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic "1" and bit 4 is a logic "1" an even number of bits is transmitted and checked.

Bit 5
Stick Parity bit. When bit 3 is a logic "1" and bit 5 is a logic "1", the parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6
Set Break Control bit. When bit 6 is a logic "1", the transmit data output (TXD) is forced to the Spacing or logic "0" state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

Bit 7
Divisor Latch Access bit (DLAB). It must be set high (logic "1") to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic "0") to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

MODEM CONTROL REGISTER (MCR)
Address Offset = 4H, DLAB = X, READ/WRITE

This 8 bit register controls the interface with the MODEM or data set (or device emulating a MODEM). The contents of the MODEM control register are described on the following page.

Bit 0
This bit controls the Data Terminal Ready (nDTR) output. When bit 0 is set to a logic "1", the nDTR output is forced to a logic "0". When bit 0 is a logic "0", the nDTR output is forced to a logic "1".

Bit 1
This bit controls the Request To Send (nRTS) output. Bit 1 affects the nRTS output in a manner identical to that described above for bit 0.

Bit 2
This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

Bit 3
Output 2 (OUT2). This bit is used to enable an UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

Bit 4
This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic "1", the following occur:

1. The TXD is set to the Marking State (logic "1").
2. The receiver Serial Input (RXD) is disconnected.
3. The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.
4. All MODEM Control inputs (nCTS, nDSR, nRI and nDCD) are disconnected.
5. The four MODEM Control outputs (nDTR, nRTS, OUT1 and OUT2) are internally connected to the four MODEM Control inputs (nDSR, nCTS, RI, DCD).
6. The Modem Control output pins are forced inactive high.
7. Data that is transmitted is immediately received.

This feature allows the processor to verify the transmit and receive data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7
These bits are permanently set to logic zero.

LINE STATUS REGISTER (LSR)
Address Offset = 5H, DLAB = X, READ/WRITE

Bit 0
Data Ready (DR). It is set to a logic "1" whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic "0" by reading all of the data in the Receive Buffer Register or the FIFO.

Bit 1
Overrun Error (OE). Bit 1 indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrunn error will occur only when the FIFO is full and the next character has been completely received in the shift register, the character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a logic "1" immediately upon detection of an overrun condition, and reset whenever the Line Status Register is read.

Bit 2
Parity Error (PE). Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register

is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.

Bit 3
Framing Error (FE). Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

Bit 4
Break Interrupt (BI). Bit 4 is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. Restarting after a break is received, requires the serial data (RXD) to be logic "1" for at least 1/2 bit time.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5
Transmitter Holding Register Empty (THRE). Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is a read only bit.

Bit 6
Transmitter Empty (TEMT). Bit 6 is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is a read only bit. In the FIFO mode this bit is set whenever the THR and TSR are both empty,

Bit 7
This bit is permanently set to logic "0" in the 450 mode. In the FIFO mode, this bit is set to a logic "1" when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.

MODEM STATUS REGISTER (MSR)
Address Offset = 6H, DLAB = X, READ/WRITE

This 8 bit register provides the current state of the control lines from the MODEM (or peripheral device). In addition to this current state information, four bits of the MODEM Status Register (MSR) provide change information. These bits are set to logic "1" whenever a control input from the MODEM changes state. They are reset to logic "0" whenever the MODEM Status Register is read.

Bit 0
Delta Clear To Send (DCTS). Bit 0 indicates that the nCTS input to the chip has changed state since the last time the MSR was read.

Bit 1
Delta Data Set Ready (DDSR). Bit 1 indicates that the nDSR input has changed state since the last time the MSR was read.

Bit 2
Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the nRI input has changed from logic "0" to logic "1".

Bit 3
Delta Data Carrier Detect (DDCD). Bit 3 indicates that the nDCD input to the chip has changed state.
NOTE: Whenever bit 0, 1, 2, or 3 is set to a logic "1", a MODEM Status Interrupt is generated.

Bit 4
This bit is the complement of the Clear To Send (nCTS) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to nRTS in the MCR.

Bit 5
This bit is the complement of the Data Set Ready (nDSR) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to DTR in the MCR.

Bit 6
This bit is the complement of the Ring Indicator (nRI) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT1 in the MCR.

Bit 7
This bit is the complement of the Data Carrier Detect (nDCD) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT2 in the MCR.

SCRATCHPAD REGISTER (SCR)
Address Offset =7H, DLAB =X, READ/WRITE

This 8 bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

PROGRAMMABLE BAUD RATE GENERATOR (AND DIVISOR LATCHES DLH, DLL)

The Serial Port contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3 MHz) and dividing it by any divisor from 1 to 65535. This output frequency of the Baud Rate Generator is 16x the Baud rate. Two 8 bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers the output divides the clock by the number 3. If a 1 is loaded the output is the inverse of the input oscillator. If a two is loaded the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is the 24 MHz crystal divided by 13, giving a 1.8462 MHz clock.

Table 33 shows the baud rates possible with a 1.8462 MHz crystal.

Effect Of The Reset on Register File

The Reset Function Table (Table 34) details the effect of the Reset input on each of the registers of the Serial Port.

FIFO INTERRUPT MODE OPERATION

When the RCVR FIFO and receiver interrupts are enabled (FCR bit 0 = "1", IER bit 0 = "1"), RCVR interrupts occur as follows:

A. The receive data available interrupt will be issued when the FIFO has reached its programmed trigger level; it is cleared as soon as the FIFO drops below its programmed trigger level.
B. The IIR receive data available indication also occurs when the FIFO trigger level is reached. It is cleared when the FIFO drops below the trigger level.
C. The receiver line status interrupt (IIR=06H), has higher priority than the received data available (IIR=04H) interrupt.
D. The data ready bit (LSR bit 0)is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts occur as follows:

A. A FIFO timeout interrupt occurs if all the following conditions exist:

- at least one character is in the FIFO
- The most recent serial character received was longer than 4 continuous character times ago. (If 2 stop bits are programmed, the second one is included in this time delay.)
- The most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 160 msec at 300 BAUD with a 12 bit character.

B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baudrate).

C. When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.

D. When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = "1", IER bit 1 = "1"), XMIT interrupts occur as follows:

A. The transmitter holding register interrupt (02H) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 of 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmitter FIFO since the last THRE=1. The transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO POLLED MODE OPERATION

With FCR bit 0 = "1" resetting IER bits 0, 1, 2 or 3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation.

In this mode, the user's program will check RCVR and XMITTER status via the LSR. LSR

definitions for the FIFO Polled Mode are as follows:

- Bit 0=1 as long as there is one byte in the RCVR FIFO.
- Bits 1 to 4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since EIR bit 2=0.
- Bit 5 indicates when the XMIT FIFO is empty.
- Bit 6 indicates that both the XMIT FIFO and shift register are empty.
- Bit 7 indicates whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

Table 33 - Baud Rates Using 1.8462 MHz Clock for <= 38.4K; Using 1.8432MHz Clock for 115.2k ; Using 3.6864MHz Clock for 230.4k; Using 7.3728 MHz Clock for 460.8k

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL*	CRxx: BIT 7 OR 6
50	2304	0.001	X
75	1536	-	X
110	1047	-	X
134.5	857	0.004	X
150	768	-	X
300	384	-	X
600	192	-	X
1200	96	-	X
1800	64	-	X
2000	58	0.005	X
2400	48	-	X
3600	32	-	X
4800	24	-	X
7200	16	-	X
9600	12	-	X
19200	6	-	X
38400	3	0.030	X
57600	2	0.16	X
115200	1	0.16	X
230400	32770	0.16	1
460800	32769	0.16	1

*Note: The percentage error for all baud rates, except where indicated otherwise, is 0.2%.

Table 34 - Reset Function Table

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	RESET	All bits low
Interrupt Identification Reg.	RESET	Bit 0 is high; Bits 1 - 7 low
FIFO Control	RESET	All bits low
Line Control Reg.	RESET	All bits low
MODEM Control Reg.	RESET	All bits low
Line Status Reg.	RESET	All bits low except 5, 6 high
MODEM Status Reg.	RESET	Bits 0 - 3 low; Bits 4 - 7 input
TXD1, TXD2	RESET	High
INTRPT (RCVR errs)	RESET/Read LSR	Low
INTRPT (RCVR Data Ready)	RESET/Read RBR	Low
INTRPT (THRE)	RESET/ReadIIR/Write THR	Low
OUT2B	RESET	High
RTSB	RESET	High
DTRB	RESET	High
OUT1B	RESET	High
RCVR FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low
XMIT FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low

Table 35 - Register Summary for an Individual UART Channel

REGISTER ADDRESS*	REGISTER NAME	REGISTER SYMBOL	BIT 0	BIT 1
ADDR = 0 DLAB = 0	Receive Buffer Register (Read Only)	RBR	Data Bit 0 (Note 1)	Data Bit 1
ADDR = 0 DLAB = 0	Transmitter Holding Register (Write Only)	THR	Data Bit 0	Data Bit 1
ADDR = 1 DLAB = 0	Interrupt Enable Register	IER	Enable Received Data Available Interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)
ADDR = 2	Interrupt Ident. Register (Read Only)	IIR	"0" if Interrupt Pending	Interrupt ID Bit
ADDR = 2	FIFO Control Register (Write Only)	FCR	FIFO Enable	RCVR FIFO Reset
ADDR = 3	Line Control Register	LCR	Word Length Select Bit 0 (WLS0)	Word Length Select Bit 1 (WLS1)
ADDR = 4	MODEM Control Register	MCR	Data Terminal Ready (DTR)	Request to Send (RTS)
ADDR = 5	Line Status Register	LSR	Data Ready (DR)	Overrun Error (OE)
ADDR = 6	MODEM Status Register	MSR	Delta Clear to Send (DCTS)	Delta Data Set Ready (DDSR)
ADDR = 7	Scratch Register (Note 4)	SCR	Bit 0	Bit 1
ADDR = 0 DLAB = 1	Divisor Latch (LS)	DDL	Bit 0	Bit 1
ADDR = 1 DLAB = 1	Divisor Latch (MS)	DLM	Bit 8	Bit 9

*DLAB is Bit 7 of the Line Control Register (ADDR = 3).

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
Note 2: When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.

Table 35 - Register Summary for an Individual UART Channel (continued)

BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Enable Receiver Line Status Interrupt (ELSI)	Enable MODEM Status Interrupt (EMSI)	0	0	0	0
Interrupt ID Bit	Interrupt ID Bit (Note 5)	0	0	FIFOs Enabled (Note 5)	FIFOs Enabled (Note 5)
XMIT FIFO Reset	DMA Mode Select (Note 6)	Reserved	Reserved	RCVR Trigger LSB	RCVR Trigger MSB
Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
OUT1 (Note 3)	OUT2 (Note 3)	Loop	0	0	0
Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register (THRE)	Transmitter Empty (TEMT) (Note 2)	Error in RCVR FIFO (Note 5)
Trailing Edge Ring Indicator (TERI)	Delta Data Carrier Detect (DDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

Note 3: This bit no longer has a pin associated with it.
Note 4: When operating in the XT mode, this register is not available.
Note 5: These bits are always zero in the non-FIFO mode.
Note 6: Writing a one to this bit has no effect. DMA modes are not supported in this chip.

NOTES ON SERIAL PORT OPERATION
FIFO MODE OPERATION:

GENERAL

The RCVR FIFO will hold up to 16 bytes regardless of which trigger level is selected.

TX AND RX FIFO OPERATION

The Tx portion of the UART transmits data through TXD as soon as the CPU loads a byte into the Tx FIFO. **The UART will prevent loads to the Tx FIFO if it currently holds 16 characters.** Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The chip issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO the Tx FIFO empty interrupt will transition from active to inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UART's interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. **Therefore, after the first byte has been loaded into the FIFO the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt. This one character Tx interrupt delay will remain active until at least two bytes have been loaded into the FIFO, concurrently. When the Tx FIFO empties after this condition, the Tx interrupt will be activated without a one character delay.**

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the Overrun Error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side-effect of having a Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. **To prevent the software from having to check for this situation the chip incorporates a timeout interrupt.**

The timeout interrupt is activated when there is a least one byte in the Rx FIFO, and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The timeout interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it. These FIFO related features allow optimization of CPU/UART transactions and are especially useful given the higer baud rate capability (256 kbaud).

INFRARED INTERFACE

The infrared interface provides a two-way wireless communications port using infrared as a transmission medium. Two IR implementations have been provided for the second UART in this chip (logical device 5), IrDA and Amplitude Shift Keyed IR. The IR transmission can use the standard UART2 TX and RX pins or optional IRTX2 and IRRX2 pins. These can be selected through the configuration registers.

IrDA allows serial communication at baud rates up to 115K Baud. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a single IR pulse at the beginning of the serial bit time. A one is signaled by sending no IR pulse during the bit time. Please refer to the AC timing for the parameters of these pulses and the IrDA waveform.

The Amplitude Shift Keyed IR allows serial communication at baud rates up to 19.2K Baud. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a 500KHz waveform for the duration of the serial bit time. A one is signaled by sending no transmission the bit time. Please refer to the AC timing for the parameters of the ASK-IR waveform.

If the Half Duplex option is chosen, there is a time-out when the direction of the transmission is changed. This time-out starts at the last bit transfered during a transmission and blocks the receiver input until the time-out expires. If the transmit buffer is loaded with more data before the time-out expires, the timer is restarted after the new byte is transmitted. If data is loaded into the transmit buffer while a character is being received, the transmission will not start until the time-out expires after the last receive bit has been received. If the start bit of another character is received during this time-out, the timer is restarted after the new character is received. The time-out is four character times. A character time is defined as 10 bit times regardless of the actual word length being used.

PARALLEL PORT

The FDC37C93x incorporates an IBM XT/AT compatible parallel port. This supports the optional PS/2 type bi-directional parallel port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP) parallel port modes. Refer to the Configuration Registers for information on disabling, power down, changing the base address of the parallel port, and selecting the mode of operation.

The parallel port also incorporates SMSC's ChiProtect circuitry, which prevents possible damage to the parallel port due to printer power-up.

The functionality of the Parallel Port is achieved through the use of eight addressable ports, with their associated registers and control gating. The control and data port are read/write by the CPU, the status port is read/write in the EPP mode. The address map of the Parallel Port is shown below:

DATA PORT	BASE ADDRESS + 00H	EPP DATA PORT 0	BASE ADDRESS + 04H
STATUS PORT	BASE ADDRESS + 01H	EPP DATA PORT 1	BASE ADDRESS + 05H
CONTROL PORT	BASE ADDRESS + 02H	EPP DATA PORT 2	BASE ADDRESS + 06H
EPP ADDR PORT	BASE ADDRESS + 03H	EPP DATA PORT 3	BASE ADDRESS + 07H

The bit map of these registers is:

	D0	D1	D2	D3	D4	D5	D6	D7	Note
DATA PORT	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	1
STATUS PORT	TMOUT	0	0	nERR	SLCT	PE	nACK	nBUSY	1
CONTROL PORT	STROBE	AUTOFD	nINIT	SLC	IRQE	PCD	0	0	1
EPP ADDR PORT	PD0	PD1	PD2	PD3	PD4	PD5	PD6	AD7	2,3
EPP DATA PORT 0	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2,3
EPP DATA PORT 1	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2,3
EPP DATA PORT 2	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2,3
EPP DATA PORT 3	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2,3

Note 1: These registers are available in all modes.
Note 2: These registers are only available in EPP mode.
Note 3 : For EPP mode, IOCHRDY must be connected to the ISA bus.

Table 36 - Parallel Port Connector

HOST CONNECTOR	PIN NUMBER	STANDARD	EPP	ECP
1		nStrobe	nWrite	nStrobe
2-9		PData<0:7>	PData<0:7>	PData<0:7>
10		nAck	Intr	nAck
11		Busy	nWait	Busy, PeriphAck(3)
12		PE	(NU)	PError, nAckReverse(3)
13		Select	(NU)	Select
14		nAutofd	nDatastb	nAutoFd, HostAck(3)
15		nError	(NU)	nFault(1) nPeriphRequest(3)
16		nInit	(NU)	nInit(1) nReverseRqst(3)
17		nSelectin	nAddrstrb	nSelectIn(1,3)

(1) = Compatible Mode
(3) = High Speed Mode

Note: For the cable interconnection required for ECP support and the Slave Connector pin numbers, refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.09, Jan. 7, 1993. This document is available from Microsoft.

IBM XT/AT COMPATIBLE, BI-DIRECTIONAL AND EPP MODES

DATA PORT
ADDRESS OFFSET = 00H

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus with the rising edge of the nIOW input. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation in SPP mode, PD0 - PD7 ports are buffered (not latched) and output to the host CPU.

STATUS PORT
ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. The contents of this register are latched for the duration of an nIOR read cycle. The bits of the Status Port are defined as follows:

BIT 0 TMOUT - TIME OUT
This bit is valid in EPP mode only and indicates that a 10 usec time out has occured on the EPP bus. A logic O means that no time out error has occured; a logic 1 means that a time out error has been detected. This bit is cleared by a RESET. Writing a one to this bit clears the time out status bit. On a write, this bit is self clearing and does not require a write of a zero. Writing a zero to this bit has no effect.

BITS 1, 2 - are not implemented as register bits, during a read of the Printer Status Register these bits are a low level.

BIT 3 nERR - nERROR
The level on the nERROR input is read by the CPU as bit 3 of the Printer Status Register. A logic 0 means an error has been detected; a logic 1 means no error has been detected.

BIT 4 SLCT - PRINTER SELECTED STATUS
The level on the SLCT input is read by the CPU as bit 4 of the Printer Status Register. A logic 1 means the printer is on line; a logic 0 means it is not selected.

BIT 5 PE - PAPER END
The level on the PE input is read by the CPU as bit 5 of the Printer Status Register. A logic 1 indicates a paper end; a logic 0 indicates the presence of paper.

BIT 6 nACK - nACKNOWLEDGE
The level on the nACK input is read by the CPU as bit 6 of the Printer Status Register. A logic 0 means that the printer has received a character and can now accept another. A logic 1 means that it is still processing the last character or has not received the data.

BIT 7 nBUSY - nBUSY
The complement of the level on the BUSY input is read by the CPU as bit 7 of the Printer Status Register. A logic 0 in this bit means that the printer is busy and cannot accept a new character. A logic 1 means that it is ready to accept the next character.

CONTROL PORT
ADDRESS OFFSET = 02H

The Control Port is located at an offset of '02H' from the base address. The Control Register is initialized by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE
This bit is inverted and output onto the nSTROBE output.

BIT 1 AUTOFD - AUTOFEED
This bit is inverted and output onto the nAUTOFD output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 nINIT - nINITIATE OUTPUT
This bit is output onto the nINIT output without inversion.

BIT 3 SLCTIN - PRINTER SELECT INPUT
This bit is inverted and output onto the nSLCTIN output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

BIT 4 IRQE - INTERRUPT REQUEST ENABLE
The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU. An interrupt request is generated on the IRQ port by a positive going nACK input. When the IRQE bit is programmed low the IRQ is disabled.

BIT 5 PCD - PARALLEL CONTROL DIRECTION
Parallel Control Direction is not valid in printer mode. In printer mode, the direction is always out regardless of the state of this bit. In bi-directional, EPP or ECP mode, a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read). Bits 6 and 7 during a read are a low level, and cannot be written.

EPP ADDRESS PORT
ADDRESS OFFSET = 03H

The EPP Address Port is located at an offset of '03H' from the base address. The address register is cleared at initialization by RESET. During a WRITE operation, the contents of DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports, the leading edge of nIOW causes an EPP ADDRESS WRITE cycle to be performed, the trailing edge of IOW latches the data for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read, the leading edge of IOR causes an EPP ADDRESS READ cycle to be performed and the data output to the host CPU, the deassertion of ADDRSTB latches the PData for the duration of the IOR cycle. This register is only available in EPP mode.

EPP DATA PORT 0
ADDRESS OFFSET = 04H

The EPP Data Port 0 is located at an offset of '04H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the contents of DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports, the leading edge of nIOW causes an EPP DATA WRITE cycle to be performed, the trailing edge of IOW latches the data for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read, the leading edge of IOR causes an EPP READ cycle to be performed and the data output to the host CPU, the deassertion of DATASTB latches the PData for the duration of the IOR cycle. This register is only available in EPP mode.

EPP DATA PORT 1
ADDRESS OFFSET = 05H

The EPP Data Port 1 is located at an offset of '05H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP DATA PORT 2
ADDRESS OFFSET = 06H

The EPP Data Port 2 is located at an offset of '06H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP DATA PORT 3
ADDRESS OFFSET = 07H

The EPP Data Port 3 is located at an offset of '07H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP 1.9 OPERATION

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from the start of the EPP cycle (nIOR or nIOW asserted) to nWAIT being deasserted (after command). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

During an EPP cycle, if STROBE is active, it overrides the EPP write signal forcing the PDx bus to always be in a write mode and the nWRITE signal to always be asserted.

Software Constraints

Before an EPP cycle is executed, the software must ensure that the control register bit PCD is a logic "0" (ie a 04H or 05H should be written to the Control port). If the user leaves PCD as a logic "1", and attempts to perform an EPP write, the chip is unable to perform the write (because PCD is a logic "1") and will appear to perform an EPP read on the parallel bus, no error is indicated.

EPP 1.9 Write

The timing for a write operation (address or data) is shown in timing diagram EPP Write Data or Address cycle. IOCHRDY is driven active low at the start of each EPP write and is released when it has been determined that the write cycle can complete. The write cycle can complete under the following circumstances:

1. If the EPP bus is not ready (nWAIT is active low) when nDATASTB or nADDRSTB goes active then the write can complete when nWAIT goes inactive high.

2. If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of nDATASTB, nWRITE or nADDRSTB. The write can complete once nWAIT is determined inactive.

Write Sequence of operation

1. The host selects an EPP register, places data on the SData bus and drives nIOW active.
2. The chip drives IOCHRDY inactive (low).
3. If WAIT is not asserted, the chip must wait until WAIT is asserted.
4. The chip places address or data on PData bus, clears PDIR, and asserts nWRITE.

5. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.
6. Peripheral deasserts nWAIT, indicating that any setup requirements have been satisfied and the chip may begin the termination phase of the cycle.
7. a) The chip deasserts nDATASTB or nADDRSTRB, this marks the beginning of the termination phase. If it has not already done so, the peripheral should latch the information byte now.
   b) The chip latches the data from the SData bus for the PData bus and asserts (releases) IOCHRDY allowing the host to complete the write cycle.
8. Peripheral asserts nWAIT, indicating to the host that any hold time requirements have been satisfied and acknowledging the termination of the cycle.
9. Chip may modify nWRITE and nPDATA in preparation for the next cycle.

EPP 1.9 Read

The timing for a read operation (data) is shown in timing diagram EPP Read Data cycle. IOCHRDY is driven active low at the start of each EPP read and is released when it has been determined that the read cycle can complete. The read cycle can complete under the following circumstances:

1. If the EPP bus is not ready (nWAIT is active low) when nDATASTB goes active then the read can complete when nWAIT goes inactive high.

2. If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of WRITE or before nDATASTB goes active. The read can complete once nWAIT is determined inactive.

Read Sequence of Operation

1. The host selects an EPP register and drives nIOR active.
2. The chip drives IOCHRDY inactive (low).
3. If WAIT is not asserted, the chip must wait until WAIT is asserted.
4. The chip tri-states the PData bus and deasserts nWRITE.
5. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.
6. Peripheral drives PData bus valid.
7. Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.
8. a) The chip latches the data from the PData bus for the SData bus and deasserts nDATASTB or nADDRSTRB. This marks the beginning of the termination phase.
   b) The chip drives the valid data onto the SData bus and asserts (releases) IOCHRDY allowing the host to complete the read cycle.
9. Peripheral tri-states the PData bus and asserts nWAIT, indicating to the host that the PData bus is tri-stated.
10. Chip may modify nWRITE, PDIR and nPDATA in preparation for the next cycle.

EPP 1.7 OPERATION

When the EPP 1.7 mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a

watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from the start of the EPP cycle (nIOR or nIOW asserted) to the end of the cycle nIOR or nIOW deasserted). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

Software Constraints

Before an EPP cycle is executed, the software must ensure that the control register bits D0, D1 and D3 are set to zero. Also, bit D5 (PCD) is a logic "0" for an EPP write or a logic "1" for and EPP read.

EPP 1.7 Write

The timing for a write operation (address or data) is shown in timing diagram EPP 1.7 Write Data or Address cycle. IOCHRDY is driven active low when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The write cycle can complete when nWAIT is inactive high.

Write Sequence of Operation

1. The host sets PDIR bit in the control register to a logic "0". This asserts nWRITE.
2. The host selects an EPP register, places data on the SData bus and drives nIOW active.
3. The chip places address or data on PData bus.
4. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.
5. If nWAIT is asserted, IOCHRDY is deasserted until the peripheral deasserts nWAIT or a time-out occurs.
6. When the host deasserts nIOW the chip deasserts nDATASTB or nADDRSTRB and latches the data from the SData bus for the PData bus.
7. Chip may modify nWRITE, PDIR and nPDATA in preparation of the next cycle.

EPP 1.7 Read

The timing for a read operation (data) is shown in timing diagram EPP 1.7 Read Data cycle. IOCHRDY is driven active low when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The read cycle can complete when nWAIT is inactive high.

Read Sequence of Operation

1. The host sets PDIR bit in the control register to a logic "1". This deasserts nWRITE and tri-states the PData bus.
2. The host selects an EPP register and drives nIOR active.
3. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.
4. If nWAIT is asserted, IOCHRDY is deasserted until the peripheral deasserts nWAIT or a time-out occurs.
5. The Peripheral drives PData bus valid.
6. The Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.
7. When the host deasserts nIOR the chip deasserts nDATASTB or nADDRSTRB.
8. Peripheral tri-states the PData bus.
9. Chip may modify nWRITE, PDIR and nPDATA in preparation of the next cycle.

Table 37 - EPP Pin Descriptions

EPP SIGNAL	EPP NAME	TYPE	EPP DESCRIPTION
nWRITE	nWrite	O	This signal is active low. It denotes a write operation.
PD<0:7>	Address/Data	I/O	Bi-directional EPP byte wide address and data bus.
INTR	Interrupt	I	This signal is active high and positive edge triggered. (Pass through with no inversion, Same as SPP.)
WAIT	nWait	I	This signal is active low. It is driven inactive as a positive acknowledgement from the device that the transfer of data is completed. It is driven active as an indication that the device is ready for the next transfer.
DATASTB	nData Strobe	O	This signal is active low. It is used to denote data read or write operation.
RESET	nReset	O	This signal is active low. When driven active, the EPP device is reset to its initial operational mode.
ADDRSTB	nAddress Strobe	O	This signal is active low. It is used to denote address read or write operation.
PE	Paper End	I	Same as SPP mode.
SLCT	Printer Selected Status	I	Same as SPP mode.
nERR	Error	I	Same as SPP mode.
PDIR	Parallel Port Direction	O	This output shows the direction of the data transfer on the parallel port bus. A low means an output/write condition and a high means an input/read condition. This signal is normally a low (output/write) unless PCD of the control register is set or if an EPP read cycle is in progress.

Note 1: SPP and EPP can use 1 common register.
Note 2: nWrite is the only EPP output that can be over-ridden by SPP control port during an EPP cycle. For correct EPP read cycles, PCD is required to be a low.

EXTENDED CAPABILITIES PARALLEL PORT

ECP provides a number of advantages, some of which are listed below. The individual features are explained in greater detail in the remainder of this section.

- High performance half-duplex forward and reverse channel
- Interlocked handshake, for fast reliable transfer
- Optional single byte RLE compression for improved throughput (64:1)
- Channel addressing for low-cost peripherals
- Maintains link and data layer separation
- Permits the use of active output drivers
- Permits the use of adaptive signal timing
- Peer-to-peer capability

Vocabulary

The following terms are used in this document:

assert When a signal asserts it transitions to a "true" state, when a signal deasserts it transitions to a "false" state.

forward Host to Peripheral communication.
reverse Peripheral to Host communication.
PWord A port word; equal in size to the width of the ISA interface. For this implementation, PWord is always 8 bits.
1 A high level.
0 A low level.

These terms may be considered synonymous:

- PeriphClk, nAck
- HostAck, nAutoFd
- PeriphAck, Busy
- nPeriphRequest, nFault
- nReverseRequest, nInit
- nAckReverse, PError
- Xflag, Select
- ECPMode, nSelectln
- HostClk, nStrobe

Reference Document
IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev 1.09, Jan 7, 1993. This document is available from Microsoft.

The bit map of the Extended Parallel Port registers is:

	D7	D6	D5	D4	D3	D2	D1	D0	Note
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
dsr	nBusy	nAck	PError	Select	nFault	0	0	0	1
dcr	0	0	Direction	ackIntEn	SelectIn	nInit	autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpDFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	Parallel Port IRQ			Parallel Port DMA			
ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Note 1: These registers are available in all modes.
Note 2: All FIFOs use one common 16 byte FIFO.
Note 3: The ECP Parallel Port Config Reg B reflects the IRQ and DRQ selected by the Configuration Registers.

ISA IMPLEMENTATION STANDARD

This specification describes the standard ISA interface to the Extended Capabilities Port (ECP). All ISA devices supporting ECP must meet the requirements contained in this section or the port will not be supported by Microsoft. For a description of the ECP Protocol, please refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.09, Jan.7, 1993. This document is available from Microsoft.

Description

The port is software and hardware compatible with existing parallel ports so that it may be used as a standard LPT port if ECP is not required. The port is designed to be simple and requires a small number of gates to implement. It does not do any "protocol" negotiation, rather it provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward and reverse directions.

Small FIFOs are employed in both forward and reverse directions to smooth data flow and improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes deep. The port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The port also supports run length encoded (RLE) decompression (required) in hardware. compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. Hardware support for compression is optional.

Table 38 - ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
nStrobe	O	During write operations nStrobe registers data or address into the slave on the asserting edge (handshakes with Busy).
PData 7:0	I/O	Contains address or data or RLE data.
nAck	I	Indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
PeriphAck (Busy)	I	This signal deasserts to indicate that the peripheral can accept data. This signal handshakes with nStrobe in the forward direction. In the reverse direction this signal indicates whether the data lines contain ECP command information or data. The peripheral uses this signal to flow control in the forward direction. It is an "interlocked" handshake with nStrobe. PeriphAck also provides command information in the reverse direction.
PError (nAckReverse)	I	Used to acknowledge a change in the direction the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. It is an "interlocked" handshake with nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select	I	Indicates printer on line.
nAutoFd (HostAck)	O	Requests a byte of data from the peripheral when asserted, handshaking with nAck in the reverse direction. In the forward direction this signal indicates whether the data lines contain ECP address or data. The host drives this signal to flow control in the reverse direction. It is an "interlocked" handshake with nAck. HostAck also provides command information in the forward phase.
nFault (nPeriphRequest)	I	Generates an error interrupt when asserted. This signal provides a mechanism for peer-to-peer communication. This signal is valid only in the forward direction. During ECP Mode the peripheral is permitted (but not required) to drive this pin low to request a reverse transfer. The request is merely a "hint" to the host; the host has ultimate control over the transfer direction. This signal would be typically used to generate an interrupt to the host CPU.
nInit	O	Sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction. The peripheral is only allowed to drive the bi-directional data bus while in ECP Mode and HostAck is low and nSelectIn is high.
nSelectIn	O	Always deasserted in ECP mode.

Register Definitions

The register definitions are based on the standard IBM addresses for LPT. All of the standard printer ports are supported. The additional registers attach to an upper bit decode of the standard LPT port definition to avoid conflict with standard ISA devices. The port is equivalent to a generic parallel port interface and may be operated in that mode. The port registers vary depending on the mode field in the ecr. The table below lists these dependencies. Operation of the devices in modes other that those specified is undefined.

Table 39 - ECP Register Definitions

NAME	ADDRESS (Note 1)	ECP MODES	FUNCTION
data	+000h R/W	000-001	Data Register
ecpAFifo	+000h R/W	011	ECP FIFO (Address)
dsr	+001h R/W	All	Status Register
dcr	+002h R/W	All	Control Register
cFifo	+400h R/W	010	Parallel Port Data FIFO
ecpDFifo	+400h R/W	011	ECP FIFO (DATA)
tFifo	+400h R/W	110	Test FIFO
cnfgA	+400h R	111	Configuration Register A
cnfgB	+401h R/W	111	Configuration Register B
ecr	+402h R/W	All	Extended Control Register

Note 1: These addresses are added to the parallel port base address as selected by configuration register or jumpers.
Note 2: All addresses are qualified with AEN. Refer to the AEN pin definition.

Table 40 - Mode Descriptions

MODE	DESCRIPTION*
000	SPP mode
001	PS/2 Parallel Port mde
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the configuration registers)
101	(Reserved)
110	Test mode
111	Configuration mode

*Refer to ECR Register Description

DATA and ecpAFifo PORT
ADDRESS OFFSET = 00H

Modes 000 and 001 (Data Port)

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus on the rising edge of the nIOW input. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation, PD0 - PD7 ports are read and output to the host CPU.

Mode 011 (ECP FIFO - Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmitts this byte to the peripheral automatically. The operation of this register is ony defined for the forward direction (direction is 0). Refer to the ECP Parallel Port Forward Timing Diagram, located in the Timing Diagrams section of this data sheet .

DEVICE STATUS REGISTER (dsr)
ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. Bits 0 - 2 are not implemented as register bits, during a read of the Printer Status Register these bits are a low level. The bits of the Status Port are defined as follows:

BIT 3 nFault
The level on the nFault input is read by the CPU as bit 3 of the Device Status Register.

BIT 4 Select
The level on the Select input is read by the CPU as bit 4 of the Device Status Register.

BIT 5 PError
The level on the PError input is read by the CPU as bit 5 of the Device Status Register. Printer Status Register.

BIT 6 nAck
The level on the nAck input is read by the CPU as bit 6 of the Device Status Register.

BIT 7 nBusy
The complement of the level on the BUSY input is read by the CPU as bit 7 of the Device Status Register.

DEVICE CONTROL REGISTER (dcr)
ADDRESS OFFSET = 02H

The Control Register is located at an offset of '02H' from the base address. The Control Register is initialized to zero by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE
This bit is inverted and output onto the nSTROBE output.

BIT 1 AUTOFD - AUTOFEED
This bit is inverted and output onto the nAUTOFD output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 nINIT - nINITIATE OUTPUT
This bit is output onto the nINIT output without inversion.

BIT 3 SELECTIN
This bit is inverted and output onto the nSLCTIN output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

BIT 4 ackIntEn - INTERRUPT REQUEST ENABLE
The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU due

to a low to high transition on the nACK input. Refer to the description of the interrupt under Operation, Interrupts.

BIT 5 DIRECTION
If mode=000 or mode=010, this bit has no effect and the direction is always out regardless of the state of this bit. In all other modes, Direction is valid and a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

BITS 6 and 7 during a read are a low level, and cannot be written.

cFifo (Parallel Port Data FIFO)
ADDRESS OFFSET = 400h
Mode = 010

Bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte aligned. This mode is only defined for the forward direction.

ecpDFifo (ECP Data FIFO)
ADDRESS OFFSET = 400H
Mode = 011

Bytes written or DMAed from the system to this FIFO, when the direction bit is 0, are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

Data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO when the direction bit is 1. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

tFifo (Test FIFO Mode)
ADDRESS OFFSET = 400H
Mode = 110
Data bytes may be read, written or DMAed to or from the system to this FIFO in any direction.

Data in the tFIFO will not be transmitted to the to the parallel port lines using a hardware protocol handshake. However, data in the tFIFO may be displayed on the parallel port data lines.

The tFIFO will not stall when overwritten or underrun. If an attempt is made to write data to a full tFIFO, the new data is not accepted into the tFIFO. If an attempt is made to read data from an empty tFIFO, the last data byte is re-read again. The full and empty bits must always keep track of the correct FIFO state. The tFIFO will transfer data at the maximum ISA rate so that software may generate performance metrics.

The FIFO size and interrupt threshold can be determined by writing bytes to the FIFO and checking the full and serviceIntr bits.

The writeIntrThreshold can be derermined by starting with a full tFIFO, setting the direction bit to 0 and emptying it a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

The readIntrThreshold can be derermined by setting the direction bit to 1 and filling the empty tFIFO a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

Data bytes are always read from the head of tFIFO regardless of the value of the direction bit. For example if 44h, 33h, 22h is written to the FIFO, then reading the tFIFO will return 44h, 33h, 22h in the same order as was written.

cnfgA (Configuration Register A)
ADDRESS OFFSET = 400H
Mode = 111

This register is a read only register. When read, 10H is returned. This indicates to the system that this is an 8-bit implementation. (PWord = 1 byte)

cnfgB (Configuration Register B)
ADDRESS OFFSET = 401H
Mode = 111

BIT 7 compress
This bit is read only. During a read it is a low level. This means that this chip does not support hardware RLE compression. It does support hardware de-compression!

BIT 6 intrValue
Returns the value on the ISA iRq line to determine possible conflicts.

BITS [3:0] Parallel Port IRQ
Refer to Table "A" on page 169.

BITS [2:0] Parallel Port DMA
Refer to Table "B" on page 169.

ecr (Extended Control Register)
ADDRESS OFFSET = 402H
Mode = all
This register controls the extended ECP parallel port functions.

BITS 7,6,5
These bits are Read/Write and select the Mode.

BIT 4 nErrIntrEn
Read/Write (Valid only in ECP Mode)
1: Disables the interrupt generated on the asserting edge of nFault.
0: Enables an interrupt pulse on the high to low edge of nFault. Note that an interrupt will be generated if nFault is asserted (interrupting) and this bit is written from a 1 to a 0. This prevents interrupts from being lost in the time between the read of the ecr and the write of the ecr.

BIT 3 dmaEn
Read/Write
1: Enables DMA (DMA starts when serviceIntr is 0).
0: Disables DMA unconditionally.

BIT 2 serviceIntr
Read/Write
1: Disables DMA and all of the service interrupts.
0: Enables one of the following 3 cases of interrupts. Once one of the 3 service interrupts has occurred serviceIntr bit shall be set to a 1 by hardware. It must be reset to 0 to re-enable the interrupts. Writing this bit to a 1 will not cause an interrupt.

case dmaEn=1:
During DMA (this bit is set to a 1 when terminal count is reached).

case dmaEn=0 direction=0:
This bit shall be set to 1 whenever there are writeIntrThreshold or more bytes free in the FIFO.

case dmaEn=0 direction=1:
This bit shall be set to 1 whenever there are readIntrThreshold or more valid bytes to be read from the FIFO.

BIT 1 full
Read only
1: The FIFO cannot accept another byte or the FIFO is completely full.
0: The FIFO has at least 1 free byte.

BIT 0 empty
Read only
1: The FIFO is completely empty.
0: The FIFO contains at least 1 byte of data.

Table 41 - Extended Control Register

R/W	MODE
000:	Standard Parallel Port Mode . In this mode the FIFO is reset and common collector drivers are used on the control lines (nStrobe, nAutoFd, nInit and nSelectIn). Setting the direction bit will not tri-state the output drivers in this mode.
001:	PS/2 Parallel Port Mode. Same as above except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register. All drivers have active pull-ups (push-pull).
010:	Parallel Port FIFO Mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data is automatically transmitted using the standard parallel port protocol. Note that this mode is only useful when direction is 0. All drivers have active pull-ups (push-pull).
011:	ECP Parallel Port Mode. In the forward direction (direction is 0) bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and transmitted automatically to the peripheral using ECP Protocol. In the reverse direction (direction is 1) bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo. All drivers have active pull-ups (push-pull).
100:	Selects EPP Mode: In this mode, EPP is selected if the EPP supported option is selected in configuration register L3-CRF0. All drivers have active pull-ups (push-pull).
101:	Reserved
110:	Test Mode. In this mode the FIFO may be written and read, but the data will not be transmitted on the parallel port. All drivers have active pull-ups (push-pull).
111:	Configuration Mode. In this mode the confgA, confgB registers are accessible at 0x400 and 0x401. All drivers have active pull-ups (push-pull).

OPERATION

Mode Switching/Software Control

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (modes 011 or 010).

Setting the mode to 011 or 010 will cause the hardware to initiate data transfer.

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

Once in an extended forward mode the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In this case all control signals will be deasserted before the mode switch. In an ecp reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001. Since the automatic hardware ecp reverse handshake only cares about the state of the FIFO it may have acquired extra data which will be discarded. It may in fact be in the middle of a transfer when the mode is changed back to 000 or 001. In this case the port will deassert nAutoFd independent of the state of the transfer. The design shall not cause glitches on the handshake signals if the software meets the constraints above.

ECP Operation

Prior to ECP operation the Host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol. This is a somewhat complex negotiation carried out under program control in mode 000.

After negotiation, it is necessary to initialize some of the port bits. The following are required:

- Set Direction = 0, enabling the drivers.
- Set strobe = 0, causing the nStrobe signal to default to the deasserted state.
- Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.
- Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo respectively.

Note that all FIFO data transfers are byte wide and byte aligned. Address/RLE transfers are byte-wide and only allowed in the forward direction.

The host may switch directions by first switching to mode = 001, negotiating for the forward or reverse channel, setting direction to 1 or 0, then setting mode = 011. When direction is 1 the hardware shall handshake for each ECP read data byte and attempt to fill the FIFO. Bytes may then be read from the ecpDFifo as long as it is not empty.

ECP transfers may also be accomplished (albeit slowly) by handshaking individual bytes under program control in mode = 001, or 000.

Termination from ECP Mode

Termination from ECP Mode is similar to the termination from Nibble/Byte Modes. The host is permitted to terminate from ECP Mode only in specific well-defined states. The termination can only be executed while the bus is in the forward direction. To terminate while the channel is in the reverse direction, it must first be transitioned into the forward direction.

Command/Data

ECP Mode supports two advanced features to improve the effectiveness of the protocol for some applications. The features are implemented by allowing the transfer of normal 8-bit data or 8-bit commands.

When in the forward direction, normal data is transferred when HostAck is high and an 8-bit command is transferred when HostAck is low. The most significant bit of the command indicates whether it is a run-length count (for compression) or a channel address.

When in the reverse direction, normal data is transferred when PeriphAck is high and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero. Reverse channel addresses are seldom used and may not be supported in hardware.

Table 42
Forward Channel Commands (HostAck Low)
Reverse Channel Commands (PeripAck Low)

D7	D[6:0]
0	Run-Length Count (0-127) (mode 0011 0X00 only)
1	Channel Address (0-127)

Data Compression

The ECP port supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Run length encoded (RLE) compression in hardware is not supported. To transfer compressed data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. When a run-length count is received from a peripheral, the subsequent data byte is replicated the specified number of times. A run-length count of zero specifies that only one byte of data is represented by the next data byte, whereas a run-length count of 127 indicates that the next byte should be expanded to 128 bytes. To prevent data expansion, however, run-length counts of zero should be avoided.

Pin Definition

The drivers for nStrobe, nAutoFd, nInit and nSelectIn are open-collector in mode 000 and are push-pull in all other modes.

ISA Connections

The interface can never stall causing the host to hang. The width of data transfers is strictly controlled on an I/O address basis per this specification. All FIFO-DMA transfers are byte wide, byte aligned and end on a byte boundary. (The PWord value can be obtained by reading Configuration Register A, cnfgA, described in the next section.) Single byte wide transfers are always possible with standard or PS/2 mode using program control of the control signals.

Interrupts

The interrupts are enabled by serviceIntr in the ecr register.

serviceIntr = 1 Disables the DMA and all of the service interrupts.

serviceIntr = 0 Enables the selected interrupt condition. If the interrupting condition is valid, then the interrupt is generated immediately when this bit is changed from a 1 to a 0. This can occur during Programmed I/O if the number of bytes removed or added from/to the FIFO does not cross the threshold.

The interrupt generated is ISA friendly in that it must pulse the interrupt line low, allowing for interrupt sharing. After a brief pulse low following the interrupt event, the interrupt line is tri-stated so that other interrupts may assert.

An interrupt is generated when:

1. For DMA transfers: When serviceIntr is 0, dmaEn is 1 and the DMA TC is received.

2. For Programmed I/O:
   a. When serviceIntr is 0, dmaEn is 0, direction is 0 and there are writeIntrThreshold or more free bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are writeIntrThreshold or more free bytes in the FIFO.
   b. (1) When serviceIntr is 0, dmaEn is 0, direction is 1 and there are readIntrThreshold or more bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are readIntrThreshold or more bytes in the FIFO.

3. When nErrIntrEn is 0 and nFault transitions from high to low or when nErrIntrEn is set from 1 to 0 and nFault is asserted.

4. When ackIntEn is 1 and the nAck signal transitions from a low to a high.

FIFO Operation

The FIFO threshold is set in the chip configuration registers. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. (FIFO test mode will be addressed separately.) After a reset, the FIFO is disabled. Each data byte is transferred by a Programmed I/O cycle or PDRQ depending on the selection of DMA or Programmed I/O mode.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

DMA TRANSFERS

DMA transfers are always to or from the ecpDFifo, tFifo or CFifo. DMA utilizes the standard PC DMA services. To use the DMA transfers, the host first sets up the direction and state as in the programmed I/O case. Then it programs the DMA controller in the host with the desired count and memory address. Lastly it sets dmaEn to 1 and serviceIntr to 0. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, disabling DMA. In order to prevent possible blocking of refresh requests dReq shall not be asserted for more than 32 DMA cycles in a row. The FIFO is enabled directly by asserting nPDACK and addresses need not be valid. PINTR is generated when a TC is received. PDRQ must not be asserted for more than 32 DMA cycles in a row. After the 32nd cycle, PDRQ must be kept unasserted until nPDACK is deasserted for a minimum of 350nsec. (Note: The only way to properly terminate DMA transfers is with a TC.)

DMA may be disabled in the middle of a transfer by first disabling the host DMA controller. Then setting serviceIntr to 1, followed by setting dmaEn to 0, and waiting for the FIFO to become empty or full. Restarting the DMA is accomplished by enabling DMA in the host, setting dmaEn to 1, followed by setting serviceIntr to 0.

DMA Mode - Transfers from the FIFO to the Host

(Note: In the reverse mode, the peripheral may not continue to fill the FIFO if it runs out of data to transfer, even if the chip continues to request more data from the peripheral.)

The ECP activates the PDRQ pin whenever there is data in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The ECP will deactivate the PDRQ pin when the FIFO becomes empty or when the TC becomes true (qualified by nPDACK), indicating that no more data is required. PDRQ goes inactive after nPDACK goes active for the last byte of a data transfer (or on the active edge of nIOR, on the last byte, if no edge is present on nPDACK). If PDRQ goes inactive due to the FIFO going empty, then PDRQ is active again as soon as there is one byte in the FIFO. If PDRQ goes inactive due to the TC, then PDRQ is active again when there is one byte in the FIFO, and serviceIntr has been re-enabled. (Note: A data underrun may occur if PDRQ is not removed in time to prevent an unwanted cycle.)

Programmed I/O Mode or Non-DMA Mode

The ECP or parallel port FIFOs may also be operated using interrupt driven programmed I/O. Software can determine the writeIntrThreshold, readIntrThreshold, and FIFO depth by accessing the FIFO in Test Mode.

Programmed I/O transfers are to the ecpDFifo at 400H and ecpAFifo at 000H or from the ecpDFifo located at 400H, or to/from the tFifo at 400H. To use the programmed I/O transfers, the host first sets up the direction and state, sets dmaEn to 0 and serviceIntr to 0.

The ECP requests programmed I/O transfers from the host by activating the PINTR pin. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

Note: A threshold of 16 is equivalent to a threshold of 15. These two cases are treated the same.

Programmed I/O - Transfers from the FIFO to the Host

In the reverse direction an interrupt occurs when serviceIntr is 0 and readIntrThreshold bytes are available in the FIFO. If at this time the FIFO is full it can be emptied completely in a single burst, otherwise readIntrThreshold bytes may be read from the FIFO in a single burst.

readIntrThreshold =(16-<threshold>) data bytes in FIFO

An interrupt is generated when serviceIntr is 0 and the number of bytes in the FIFO is greater than or equal to (16-<threshold>). (If the threshold = 12, then the interrupt is set whenever there are 4-16 bytes in the FIFO.) The PINT pin can be used for interrupt-driven systems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. If at this time the FIFO is full, it can be completely emptied in a single burst, otherwise a minimum of (16-<threshold>) bytes may be read from the FIFO in a single burst.

Programmed I/O - Transfers from the Host to the FIFO

In the forward direction an interrupt occurs when serviceIntr is 0 and there are writeIntrThreshold or more bytes free in the FIFO. At this time if the FIFO is empty it can be filled with a single burst before the empty bit needs to be re-read. Otherwise it may be filled with writeIntrThreshold bytes.

writeIntrThreshold = (16-<threshold>) free bytes in FIFO

An interrupt is generated when serviceIntr is 0 and the number of bytes in the FIFO is less than or equal to <threshold>. (If the threshold = 12, then the interrupt is set whenever there are 12 or less bytes of data in the FIFO.) The PINT pin can be used for interrupt-driven systems. The host must respond to the request by writing data to the FIFO. If at this time the FIFO is empty, it can be completely filled in a single burst, otherwise a minimum of (16-<threshold>) bytes may be written to the FIFO in a single burst. This process is repeated until the last byte is transferred into the FIFO.

AUTO POWER MANAGEMENT

Power management capabilities are provided for the following logical devices: floppy disk, UART 1, UART 2 and the parallel port. For each logical device, two types of power management are provided; direct powerdown and auto powerdown.

FDC Power Management

Direct power management is controlled by CR22. Refer to CR22 for more information.

Auto Power Management is enabled by CR23-B0. When set, this bit allows FDC to enter powerdown when all of the following conditions have been met:

1. The motor enable pins of register 3F2H are inactive (zero).

2. The part must be idle; MSR=80H and INT = 0 (INT may be high even if MSR = 80H due to polling interrupts).

3. The head unload timer must have expired.

4. The Auto powerdown timer (10msec) must have timed out.

An internal timer is initiated as soon as the auto powerdown command is enabled. The part is then powered down when all the conditions are met.

Disabling the auto powerdown mode cancels the timer and holds the FDC block out of auto powerdown.

DSR From Powerdown

If DSR powerdown is used when the part is in auto powerdown, the DSR powerdown will override the auto powerdown. However, when the part is awakened from DSR powerdown, the auto powerdown will once again become effective.

Wake Up From Auto Powerdown

If the part enters the powerdown state through the auto powerdown mode, then the part can be awakened by reset or by appropriate access to certain registers.

If a hardware or software reset is used then the part will go through the normal reset sequence. If the access is through the selected registers, then the FDC resumes operation as though it was never in powerdown. Besides activating the RESET pin or one of the software reset bits in the DOR or DSR, the following register accesses will wake up the part:

1. Enabling any one of the motor enable bits in the DOR register (reading the DOR does not awaken the part).

2. A read from the MSR register.

3. A read or write to the Data register.

Once awake, the FDC will reinitiate the auto powerdown timer for 10 ms. The part will powerdown again when all the powerdown conditions are satisfied.

Register Behavior

Table 43 reiterates the AT and PS/2 (including Model 30) configuration registers available. It also shows the type of access permitted. In order to maintain software transparency, access to all the registers must be maintained. As Table 43 shows, two sets of registers are distinguished based on whether their access results in the part remaining in powerdown state or exiting it.

Access to all other registers is possible without awakening the part. These registers can be accessed during powerdown without changing the status of the part. A read from these registers will reflect the true status as shown in the register description in the FDC description. A write to the part will result in the part retaining the data and subsequently reflecting it when the part awakens. Accessing the part during powerdown may cause an increase in the power consumption by the part. The part will revert back to its low power mode when the access has been completed.

Pin Behavior

The FDC37C93x is specifically designed for portable PC systems in which power conservation is a primary concern. This makes the behavior of the pins during powerdown very important.

The pins of the FDC37C93x can be divided into two major categories: system interface and floppy disk drive interface. The floppy disk drive pins are disabled so that no power will be drawn through the part as a result of any voltage applied to the pin within the part's power supply range. Most of the system interface pins are left active to monitor system accesses that may wake up the part.

System Interface Pins

Table 44 gives the state of the system interface pins in the powerdown state. Pins unaffected by the powerdown are labeled "Unchanged". Input pins are "Disabled" to prevent them from causing currents internal to the FDC37C93x when they have indeterminate input values.

Table 43 - PC/AT and PS/2 Available Registers

Base + Address	Available Registers		Access Permitted
	PC-AT	PS/2 (Model 30)	
Access to these registers DOES NOT wake up the part			
00H	----	SRA	R
01H	----	SRB	R
02H	DOR (1)	DOR (1)	R/W
03H	---	---	---
04H	DSR (1)	DSR (1)	W
06H	---	---	---
07H	DIR	DIR	R
07H	CCR	CCR	W
Access to these registers wakes up the part			
04H	MSR	MSR	R
05H	Data	Data	R/W

Note 1: Writing to the DOR or DSR does not wake up the part, however, writing any of the motor enable bits or doing a software reset (via DOR or DSR reset bits) will wake up the part.

Table 44 - State of System Pins in Auto Powerdown

System Pins	State in Auto Powerdown
Input Pins	
IOR	Unchanged
IOW	Unchanged
A[0:9]	Unchanged
D[0:7]	Unchanged
RESET	Unchanged
IDENT	Unchanged
DACKx	Unchanged
TC	Unchanged
Output Pins	
IRQx	Unchanged (low)
DB[0:7]	Unchanged
DRQx	Unchanged (low)

FDD Interface Pins

All pins in the FDD interface which can be connected directly to the floppy disk drive itself are either DISABLED or TRISTATED. Pins used for local logic control or part programming are unaffected. Table 45 depicts the state of the floppy disk drive interface pins in the powerdown state.

Table 45 - State of Floppy Disk Drive Interface Pins in Powerdown

FDD Pins	State in Auto Powerdown
Input Pins	
RDATA	Input
WP	Input
TRK0	Input
INDX	Input
DRV2	Input
DSKCHG	Input
Output Pins	
MOTEN[0:3]	Tristated
DS[0:3}	Tristated
DIR	Active
STEP	Active
WRDATA	Tristated
WE	Tristated
HDSEL	Active
DENSEL	Active
DRATE[0:1]	Active

UART Power Management

Direct power management is controlled by CR22. Refer to CR22 for more information.

Auto Power Management is enabled by CR23-B4 and B5. When set, these bits allow the following auto power management operations:

1. The transmitter enters auto powerdown when the transmit buffer and shift register are empty.

2. The receiver enters powerdown when the following conditions are all met:

   a. Receive FIFO is empty
   b. The receiver is waiting for a start bit.

Note: While in powerdown the Ring Indicator interrupt is still valid and transitions when the RI input changes.

Exit Auto Powerdown

The transmitter exits powerdown on a write to the XMIT buffer. The receiver exits auto powerdown when RXDx changes state.

Parallel Port

Direct power management is controlled by CR22. Refer to CR22 for more information.

Auto Power Management is enabled by CR23-B3. When set, this bit allows the ECP or EPP logical parallel port blocks to be placed into powerdown when not being used.

The EPP logic is in powerdown under any of the following conditions:

1. EPP is not enabled in the configuration registers.

2. EPP is not selected through ecr while in ECP mode.

The ECP logic is in powerdown under any of the following conditions:

1. ECP is not enabled in the configuration registers.

2 SPP, PS/2 Parallel port or EPP mode is selected through ecr while in ECP mode.

Exit Auto Powerdown

The parallel port logic can change powerdown modes when the ECP mode is changed through the ecr register or when the parallel port mode is changed through the configuration registers.

INTEGRATED DRIVE ELECTRONICS INTERFACE

The FDC37C93x contains two IDE interfaces. This enables hard disks with embedded controllers (AT or IDE) to be interfaced to the host processor. The IDE interface performs the address decoding for the IDE interface, generates the buffer enables for external buffers and provides internal buffers for the low byte IDE data transfers. For more information, refer to the IDE pin descriptions and the ATA specification. The following example uses IDE1 base1=1F0H, base2=3F6H and IDE2 base1=170H, base2 =376H.

HOST FILE REGISTERS

The Host File Registers are accessed by the AT Host. There are two groups of registers, the AT Task File, and the Miscellaneous AT Register.

ADDRESS 1F0H-1F7H; 170H-177H
These AT registers contain the Task File Registers. These registers communicate data, command, and status information with the AT host, and are addressed when nHCS0 or nHCS2 is low.

ADDRESS 3F6H/376H;
These AT registers may be used by the BIOS for drive control. They are accessed by the AT interface when nHCS1 or nHCS3 is active low.

Figure 2 shows the AT Host Register Map.

FIGURE 2 - HOST PROCESSOR REGISTER ADDRESS MAP (AT MODE)

PRIMARY	SECONDARY	
1F0H | 1F7H	170H | 177H	TASK FILE REGISTERS
3F6H	376H	MISC. AT REGISTERS

TASK FILE REGISTERS

Task File Registers may be accessed by the host AT when pin nHDCS0 is active (low). The Data Register (1F0H) is 16 bits wide; the remaining task file registers are 8 bits wide. The task file registers are ATA and EATA compatible. Please refer to the ATA and EATA specifications. These are available from:

Global Engineering
2805 McGaw Street
Irvine, CA 92714
(800) 854-7179 or
(714) 261-1455

IDE OUTPUT ENABLES

Two IDE output Enables are available. The IDE output enables treat all IDE transfers as 16 bit transfers.

	nIDE1_OE	**nIDE2_OE**
Option 1	IDE1 (1)	IDE2 (2)
Option 2	IDE1&IDE2 (3)	(Not used)

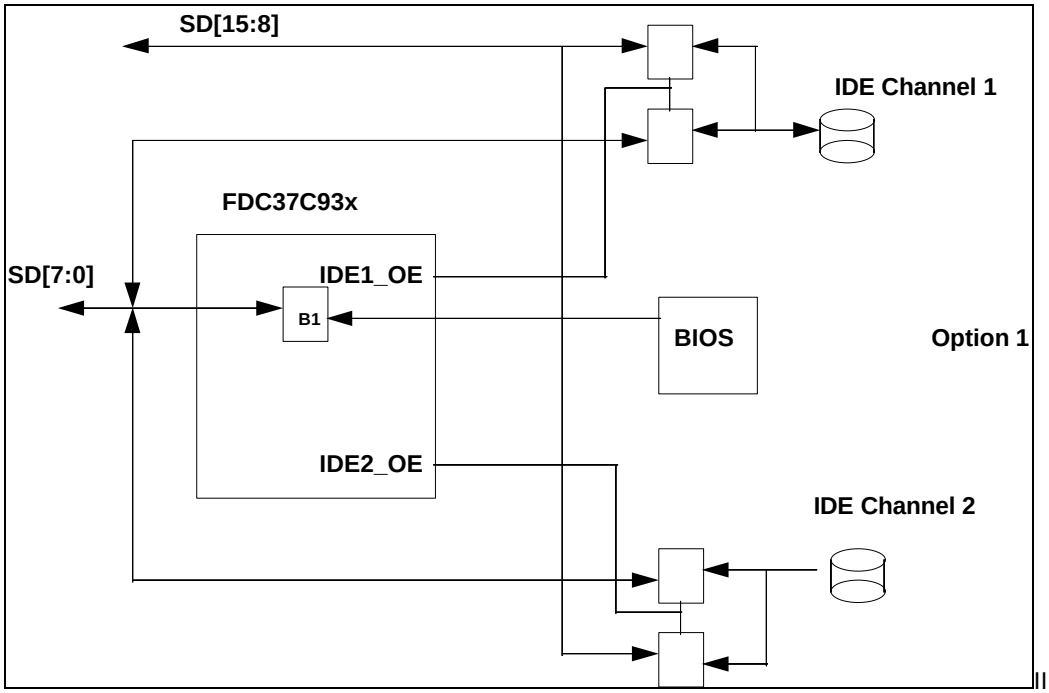
Note 1: The low and high byte transfer for IDE1 goes through external buffers controlled by IDE1_OE. (Refer to Option 1)
Note 2: The low and high byte transfer for IDE2 goes through external buffers controlled by IDE2_OE. (Refer to Option 1)
Note 3: The low and high byte transfers of IDE1 and IDE2 go through one set of external buffers controlled by IDE1. (Refer to Option 2)

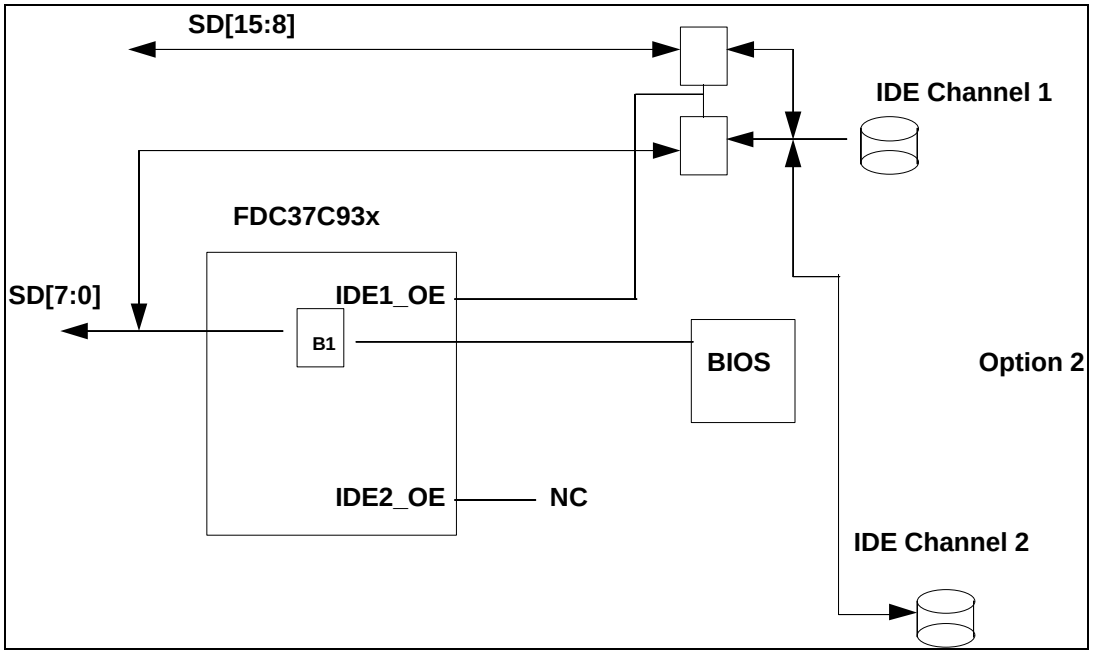
BIOS BUFFER

The FDC37C93x contains one 245 type buffer that can be used for a BIOS Buffer. If the BIOS buffer is not used, then nROMCS and nROMDIR must be tied high so as not to interfere with the boot ROM.

This function allows data transmission from the RD bus to the SD bus or from the SD bus to the RD bus. The direction of the transfer is controlled by nROMDIR. The enable input, nROMCS, can be used to disable the transfer and isolate the buses.

nROMCS	***nROMDIR***	
L	L	RD[0:7] data to SD[0:7] bus
L	H	SD[0:7] data to RD[0:7]
H	X	Isolation




SD[15:8]
IDE Channel 1
FDC37C93x
SD[7:0]
IDE1_OE
B1
BIOS
Option 2
IDE2_OE
NC
IDE Channel 2

GENERAL PURPOSE I/O FUNCTIONAL DESCRIPTION

The FDC37C93x provides a set of flexible Input/Output control functions to the system designer through a set of General Purpose I/O pins (GPI/O). These GPI/O pins may perform simple I/O or may be individually configured to provide a predefined alternate function. Power-on reset configures all GPI/O pins as simple non-inverting inputs.

General Purpose I/O Ports

The FDC37C93x has 14 independently programmable general purpose I/0 ports (GPI/O). Each GPI/O port is represented as a bit in one of two GPI/O 8-bit registers, GP1 or GP2. Only 6 bits of GP2 are implemented. Each GPI/O port and its alternate function is listed in Table 46.

Table 46 - General Purpose I/O Port Assignments

GPI/O PORT	ALTERNATE FUNCTION	REGISTER ASSIGNMENT
GP10	Interrupt Steering *	GP1, bit 0
GP11	Interrupt Steering *	GP1, bit 1
GP12	WD Timer Output or IRRX Input	GP1, bit 2
GP13	Power LED or IRTX Output	GP1, bit 3
GP14	*GP Address Decoder*	GP1, bit 4
GP15	GP Write Strobe	GP1, bit 5
GP16	Joystick RD Strobe/Joystick Chip Sel	GP1, bit 6
GP17	Joystick WR Strobe	GP1, bit 7
GP20	IDE2 Buffer Enable/8042 P20	GP2, bit 0
GP21	Serial EEPROM Data In *	GP2, bit 1
GP22	Serial EEPROM Data Out	GP2, bit 2
GP23	Serial EEPROM Clock	GP2, bit 3
GP24	Serial EEPROM Enable	GP2, bit 4
GP25	8042 P21	GP2, bit 5

Note 1: 8042 P21 is normally used for Gate A20
Note 2: 8042 P20 is normally used for the Keyboard Reset Output
* These are input-type alternate functions; all other GPI/O pins contain output-type alternate functions.

GPI/O registers GP1 and GP2 can be accessed by the host when the chip is in the normal run mode, i.e., not in Configuration Mode. The host uses an Index and Data register to access the GPI/O registers. The Power on default Index and Data registers are 0xEA and 0xEB respectively. When the chip is in configuration mode these Index and Data registers are used to access the internal configuration registers. In configuration mode the Index address may be programmed to reside on addresses 0xE0, 0xE2, 0xE4 or 0xEA. The Data address is automatically set to the Index address + 1. Upon exiting the configuration mode the new Index and Data registers are used to access registers GP1 and GP2.

To access the GP1 register the host should first make sure the chip is in the normal (run) mode. Then it should perform an IOW of 0x01 to the Index register (at 0xEX) to select GP1 and then read or write the Data register (at Index+1) to access the GP1 register. To access GP2 the host should perform an IOW of 0x02 to the Index register and then access GP2 through the Data register. *Additionally the host can access the WDT_CTRL (Watch Dog Timer Control) Configuration Register while in the normal (run) mode by writing an 0x03 to the index register.*

Table 47A - Index and Data Register

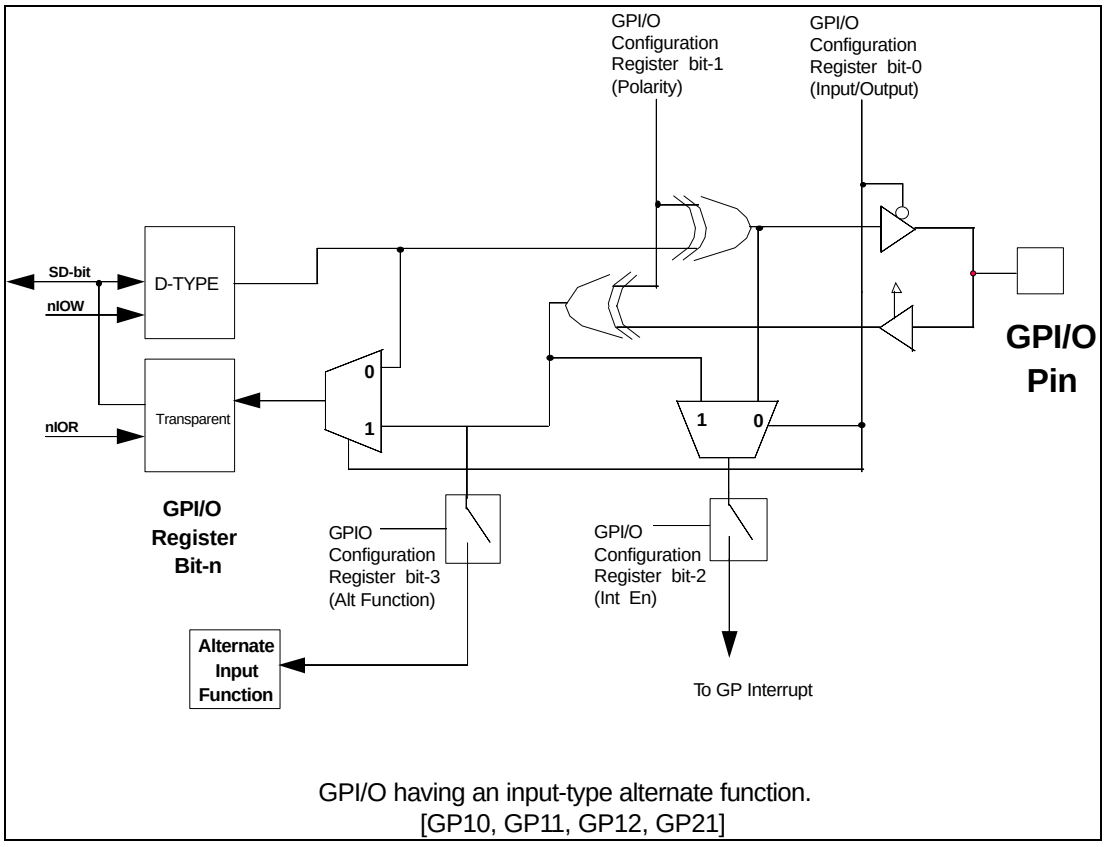
REGISTER	ADDRESS	NORMAL (RUN) MODE	CONFIG MODE
Index	OxE0, E2, E4, EA	0x01-0x03	0x00-0xFF
Data	Index address + 1	Access to GP1, GP2, Watchdog Timer Control (see Table 47B)	Access to Internal Configuration Registers

Table 47B - Index and Data Register Normal (Run) Mode

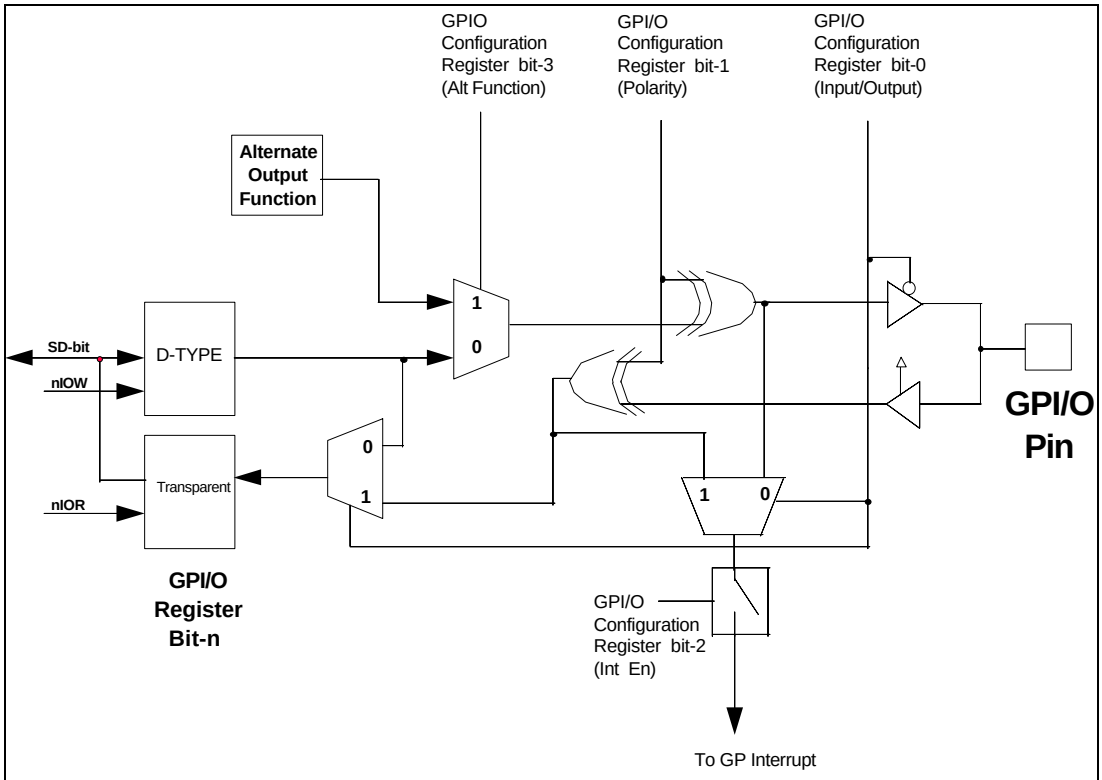
INDEX	NORMAL (RUN) MODE
0x01	Access to GP1
0x02	Access to GP2
0x03	Access to Watchdog Timer Control (L8 - CRF4)

Note 1: Watchdog timer control register L8 - F4 is also available at index 03 when not in configuration mode.

GPI/O ports contain alternate functions which are either output-type or input-type. The GPI/O port structure for each type is illustrated in the following two figures. Note: the input pin buffer is always enabled.



GPI/O having an input-type alternate function.
[GP10, GP11, GP12, GP21]



GPI/O having an output-type alternate function.
[GP12--GP17, GP20, GP22--GP25]

General Purpose I/O Configuration Registers

Assigned to each GPI/O port is an 8-bit GPI/O Configuration Register which is used to independently program each I/O port. The GPI/O Configuration Registers are only accessible when the FDC37C93x is in the Configuration Mode; more information can be found in the Configuration section of this specification.

Each GPI/O port may be programmed as either a simple inverting or non-inverting input or output port, or as an alternate function port. The least-significant four bits of each GPI/O Configuration Register define the operation of the respective GPI/O port. The basic GPI/O operations are outlined in Table 48.

In addition, the GPI/O port may be optionally programmed to steer its signal to a Combined General Purpose Interrupt request output pin on the FDC37C93x. The interrupt channel for the Combined Interrupt is selected by the GP_INT Configuration Register defined in the FDC37C93x System Configuration Section. The Combined Interrupt is the "ORed" function of the interrupt enabled GPI/O ports and will represent a standard ISA interrupt (edge high).

When programmed as an input steered onto the General Purpose Combined Interrupt (GP IRQ), the Interrupt Circuitry contains a selectable debounce/digital filter circuit in order that switches or push-buttons may be directly connected to the chip. This filter shall reject signals with pulse widths of 1ms or less. Note: there are three sets of Interrupt circuits (two dedicated and one general purpose) each of which contains an individually selectable debounce filter.

Table 48 - GPI/O Configuration Register Bits [3:0]

ALT FUNC BIT 3 0=DISABLE 1=SELECT	INT EN BIT 2 0=DISABLE 1=ENABLE	POLARITY BIT 1 0=NO INVERT 1=INVERT	I/O BIT 0 1=INPUT 0=OUTPUT	GPI/O PORT OPERATION
0	0	0	0	simple non-inverting output
0	0	0	1	simple non-inverting input
0	0	1	0	simple inverting output
0	0	1	1	simple inverting input
0	1	0	0	non-inverting output steered back to GP IRQ
0	1	0	1	non-inverting input steered to GP IRQ
0	1	1	0	inverting output steered back to GP IRQ
0	1	1	1	inverting input steered to GP IRQ
1	0	0	0	**Alternate Function Output-type :** Alternate non-inverted output. **Alternate Function Input-type :**Alternate function not valid, GPI/O pin acts as a simple non-inverting output.
1	0	0	1	**Alternate Function Output-type :** Alternate function not valid, GPI/O pin acts as a simple non-inverting input. **Alternate Function Input-type :** Alternate non-inverting input.
1	0	1	0	**Alternate Function Output-type** : Alternate output function with inverted sense **Alternate Function Input-type :** Alternate function not valid, GPI/O pin acts as a simple inverting output.

Table 48 - GPI/O Configuration Register Bits [3:0]

ALT FUNC BIT 3 0=DISABLE 1=SELECT	INT EN BIT 2 0=DISABLE 1=ENABLE	POLARITY BIT 1 0=NO INVERT 1=INVERT	I/O BIT 0 1=INPUT 0=OUTPUT	GPI/O PORT OPERATION
1	0	1	1	**Alternate Function Output-type** : Alternate output function not valid, GPI/O pin acts as a simple inverting input. **Alternate Function Input-type :**Inverting input to alternate input function.
1	1	0	0	**Alternate Function Output-type** : Alternate output function with non inverted sense steered to GP IRQ **Alternate Function Input-type :**Alternate function not valid, GPI/O pin acts as a simple non-inverting output steered to GP IRQ
1	1	0	1	**Alternate Function Output-type** : Alternate output function not valid, GPI/O pin acts as a simple non-inverting input steered to GP IRQ. **Alternate Function Input-type :**Non-inverting input to alternate input function also steered to the GP IRQ.
1	1	1	0	**Alternate Function Output-type** : Alternate output function with inverted sense steered to GP IRQ **Alternate Function Input-type :**Alternate function not valid, GPI/O pin acts as a simple inverting output steered to GP IRQ.
1	1	1	1	**Alternate Function Output-type** : Alternate output function not valid, GPI/O pin acts as a simple inverting input steered to GP IRQ. **Alternate Function Input-type :** Inverting input to alternate input function also steered to the GP IRQ.

The alternate function of GP10 and GP11 allows these GPI/O port pins to be mapped to their own independent interrupt channels. The upper nibble of the GP10 and GP11 GPI/O configuration registers is used to select the active interrupt channel for each of these ports as shown in the Configuration section of this specification.

Reading and Writing GPI/O Ports

When a GPI/O port is programmed as an input, reading it through the GPI/O register latches either the inverted or non-inverted logic value present at the GPI/O pin; writing it has no effect. When a GPI/O port is programmed as an output, the logic value written into the GPI/O register is either output to or inverted to the GPI/O pin; when read the result will reflect the contents of the GPI/O register bit. This is sumarized in Table 49.

Table 49 - GPI/O Read/Write Behavior

HOST OPERATION	GPI/O INPUT PORT	GPI/O OUTPUT PORT
Read	latched value of GPI/O pin	bit value in GP register
Write	no effect	bit placed in GP register

WATCH DOG TIMER/POWER LED CONTROL

Basic Functions

The FDC37C93x contains a Watch Dog Timer (WDT) and also has the capability to directly drive the system's Power-on LED.

The Watch Dog Time-out status bit (WDT_CTRL bit-0) is mapped to GP12 when the alternate function bit of the GP12 Configuration Register is set "and" bit-6 of the IR Options Register = 0. In addition, the Watch Dog Time-out status bit may be mapped to an interrupt through the WDT_CFG Configuration Register.

GP13 may be configured as a high current LED driver to drive the Power LED. This is accomplished by setting the alternate function bit of the GP13 Configuration Register "and" clearing bit-6 of the IR Options Register.

The Infared signals, IRRX and IRTX, are mapped to GP12 and GP13 when the alternate function bit of the GP12 and GP13 Configuration Registers is set "and" bit-6 of the IR Options Register is set.

Watch Dog Timer

The FDC37C93x's WDT has a programmable time-out ranging from 1 to 255 minutes with one minute resolution. The WDT time-out value is set through the WDT_VAL Configuration register. Setting the WDT_VAL register to 0x00 disables the WDT function (this is its power on default). Setting the WDT_VAL to any other non-zero value will cause the WDT to reload and begin counting down from the value loaded. When the WDT count value reaches zero the counter stops and sets the Watchdog time-out status bit in the WDT_CTRL Configuration Register. Note: Regardless of the current state of the WDT, the WDT time-out status bit can be directly set or cleared by the Host CPU.

There are three system events which can reset the WDT, these are a Keyboard Interrupt, a Mouse Interrupt, or I/O reads/writes to address 0x201 (the internal or an external Joystick Port). The effect on the WDT for each of these system events may be individually enabled or disabled through bits in the WDT_CFG configuration register. When a system event is enabled through the WDT_CFG register, the occurence of that event will cause the WDT to reload the value stored in WDT_VAL and reset the WDT time-out status bit if set. If all three system events are disabled the WDT will inevitably time out.

The Watch Dog Timer may be configured to generate an interrupt on the rising edge of the Time-out status bit. The WDT interrupt is mapped to an interrupt channel through the WDT_CFG Configuration Register. When mapped to an interrupt the interrupt request pin reflects the value of the WDT time-out status bit.

When the polarity bit is 0, GP12 reflect the value of the Watch Dog Time-out status bit, however when the polarity bit is 1, GP12 reflects the inverted value of the Watch Dog Time-out status bit.

The host may force a Watch Dog time-out to occur by writting a "1" to bit 2 of the WDT_CTRL (Force WD Time-out) Configuration Register. Writting a "1" to this bit forces the WDT count value to zero and sets bit 0 of the WDT_CTRL (Watch Dog Status). Bit 2 of the WDT_CTRL is self-clearing.

Power LED Toggle

Setting bit 1 of the WDT_CTRL configuration register will cause the Power LED output driver to toggle at 1 Hertz with a 50 percent duty cycle. When this bit is cleared the Power LED output will drive continuously unless it has been configured to toggle on Watch Dog time-out conditions. Setting bit 3 of the WDT_CFG configuration register will cause the Power LED output driver to toggle at 1 Hertz with a 50 percent duty cycle whenever the WDT time-out status bit is set. The truth table below clarifies the conditions for which the Power LED will toggle.

When the polarity bit is 0, the Power LED output asserts or drives low. If the polarity bit is 1 then the Power LED output asserts or drives high.

Table 50 - LED Toggle Truth Table

WDT_CTRL BIT[1] POWER LED TOGGLE	WDT_CFG BIT[3] POWER LED TOGGLE ON WDT	WDT_CTRL BIT[0] WDT T/O STATUS BIT	POWER LED STATE
1	X	X	Toggle
0	0	X	Continuous
0	1	0	Continuous
0	1	1	Toggle

Table 51 - Watchdog Timer/Power LED Configuration Registers

CONFIG REG.	BIT FIELD	DESCRIPTION
WDT_VAL	Bits[7:0]	Binary coded time-out value, 0x00 disables the WDT.
WDT_CFG	Bit[0]	Joystick enable
	Bit[1]	Keyboard enable
	Bit[2]	Mouse enable
	Bit[3]	Power LED toggle on WDT time-out
	Bits[7:4]	WDT interrupt mapping, 0000b = diables irq mapping
WDT_CTRL	Bit[0]	WDT time-out status bit
	Bit[1]	Power LED toggle
	Bit[2]	Force Timeout, self-clearing
	Bit[3]	P20 Force Timeout Enable
	Bits[7:4]	Reserved, set to zero

General Purpose Address Decoder

General Purpose I/O pin GP14 may be configured as a General Purpose Address Decode Pin. The General Purpose Address Decoder provides an output decoded from bits A11-A1 of the 12-bit address stored in a two-byte Base I/O Address Register (logical device 8 config registers 0x60,0x61) qualified with AEN. Thus, the decoder provides a two address decode where A0=X. This General Purpose output is normally active low, however the polarity may be altered through the polarity bit in its GPI/O Configuration Register.

General Purpose Write

General Purpose I/O pin GP15 may be configured as a General Purpose Write pin. The General Purpose Write provides an output decoded from the 12-bit address stored in a two-byte Base I/O Address Register (logical device 8 config registers 0x62,0x63) qualified with IOW and AEN. This General Purpose output is normally active low, however the polarity may be altered through the polarity bit in its GPI/O Configuration Register.

The GPA_GPW_EN Configuration Register contains two bits which allow the General Purpose Address Decode and Write functions to be independently enabled or disabled.

Joystick Control

The Base I/O address of the Joystick (Game) Port is fixed at address 0x201.

GP16 Joystick Function

The FDC37C93x may be configured to generate either a Joystick Chip Select or a Joystick Read Strobe on GP16. The polarity is programmable through a bit in the GP16 confiugration register. When configured as a Joystick Chip Select the output is simply a decode of the address = 0x201 qualified by AEN active. When configured as a Joystick Read Strobe the output is a decode of the address = 0x201 qualified by IOR and AEN both active. The Joystick Chip Select or Read Strobe is normally active low, however its polarity is programmable through a bit in the GP20 configuration register.

GP17 Joystick Function

The FDC37C93x may be configured to generate a Joystick Write Strobe on GP17. When configured as a Joystick Write Strobe the output is a decode of the address = 0x201 qualified by IOW and AEN both active.

The Joystick Write Strobe is normally active low, however its polarity is programmable through a bit in the GP20 configuration register.

IDE2 Buffer Enable/Reset Out

The FDC37C93x may be configured to provide an nIDE2_OE buffer enable signal on pin GP20. The IDE2 Mode Register (0xF0 of Logical Device 2) contains a bit which determines whether nIDE1_OE or nIDE2_OE is active for IDE2 transfers. If GP20 is selected as a General Purpose I/O pin, IDE2 I/O accesses must be configured to activate nIDE1_OE for IDE2 transfers if a secondary Hard Drive interface is present. The polarity of nIDE2_OE, which is normally active low, is programmable through a bit in the GP20 configuration register.

Serial EEPROM Interface

Four of the FDC37C93x's general purpose I/O pins may be configured to provide a 4 wire direct interface to a family of industry standard serial EEPROMs. For proper operation the polarity bits of these four pins must be set to 0 (non-inverting). The interface is depicted below and will allow connection to either a 93C06 (256-bit), a 93C46 (1K-bit), a 93C56 (2K-bit), or a 93C66 (4K-bit) device.

GP21 <---- Serial EEPROM Data In
GP22 ----> Serial EEPROM Data Out
GP23 ----> Serial EEPROM Clock
GP24 ----> Serial EEPROM Enable

Reset out is an internal signal from the keyboard controller (Port 20). The FDC37C93x may be configured to drive this signal onto GP20 by programming its GP I/O configuration register. Access to the serial EEPROM is only available when the FDC37C93x is in the configuration mode. A set of six configuration registers, located in Logical Device 6 (RTC) is used to fully access and configure the serial EEPROM. The registers are defined as follows:

Serial EEPROM Mode Register, 0xF1

Bits[3:0]
These are the lock bits which once set deny access to the serial EEPROM's first 128 bytes in 32 byte blocks. Bit 0 locks the first block, bit 1 the second block, bit 2 the third block and bit 3 the fourth block of 32 bytes. Once these lock bits are set they cannot be reset in any way other than by a Hard reset or a Power-on reset.

Bit[4]
This selects the type of EEPROM connected to the FDC37C93x. If cleared the device must be either a 93C06 or 93C46 and if set the device must be either an 93C56 or 93C66.This bit must be properly set before attempting to access the serial EEPROM.

Bits[7:5]
Reserved, set to zero.

Serial EEPROM Pointer Register, 0xF2

Bits[7:0]
Use this register to set the Serial EEPROM's pointer. The value in this register always reflects the current EEPROM pointer address. The Serial Device Pointer increments after each pair of reads from the Resource Data register or after each pair of writes to the Program Resource Data register.

Write EEPROM Data Register, 0xF3

Bits[7:0]
This register allows the host to write data into the serial EEPROM. The FDC37C93x supports serial EEPROMS with x16 configurations. Two bytes must be written to this register in order to generate a EEPROM write cycle. The LSB leads the MSB. The first write to this register resets bit 0 of the Write Status register. The second write resets bit 1 of the Write Status register and generates a write cycle to the serial EEPROM. The Write Status register must be polled before performing a pair of writes to this register.

Write Status Register, 0xF4

Bits[1:0]
When = (1,1)Indicates that the Write EEPROM Data register is ready to accept a pair of bytes.

When = (1,0) bit 0 is cleared on the first write of the Write EEPROM Data register. This status indicates that the serial device controller has received one byte (LSB) and is waiting for the second byte (MSB).

When = (0,0) bit 1 is cleared on the second write of the Write EEPROM Data register indicating that two bytes have been accepted and that the serial device interface is busy writing the word to the EEPROM.

Bits[6:2]
Reserved, set to zero

Bit[7]
This bit is cleared to configure the EEPROM interface for Read operations. Clearing this bit enables the serial EEPROM prefetch when the Serial EEPROM Pointer Register is updated (written or auto-incremented).

This bit is set to configure the EEPROM interface for Write operations. Setting this bit disables the serial EEPROM prefetch when the Serial EEPROM Pointer Register is updated (written or auto-incremented).

Read EEPROM Data Register, 0xF5

Bits[7:0]
This register allows the host to read data from the serial EEPROM. Data is not valid in this register until bit 0 of the Read Status Register is set. Since the EEPROM is a 16-bit device this register presents the LSB followed by the MSB for each pair of register reads. Immediately after the MSB is read bit-0 of the Read Status Register will be cleared, then the Serial EEPROM Pointer Register will be auto-incremented, then the next word of EEPROM data will be fetched, followed by the Read Status Register, bit 0 being set.

Read Status Register, 0xF6

Bit[0]
When set, indicates that data in the Read EEPROM Data register is valid. This bit is cleared when EEPROM Data is read until the next byte is valid. Reading the Read EEPROM Data register when bit 0 is clear will have no detremental effects; the data will simply be invalid.

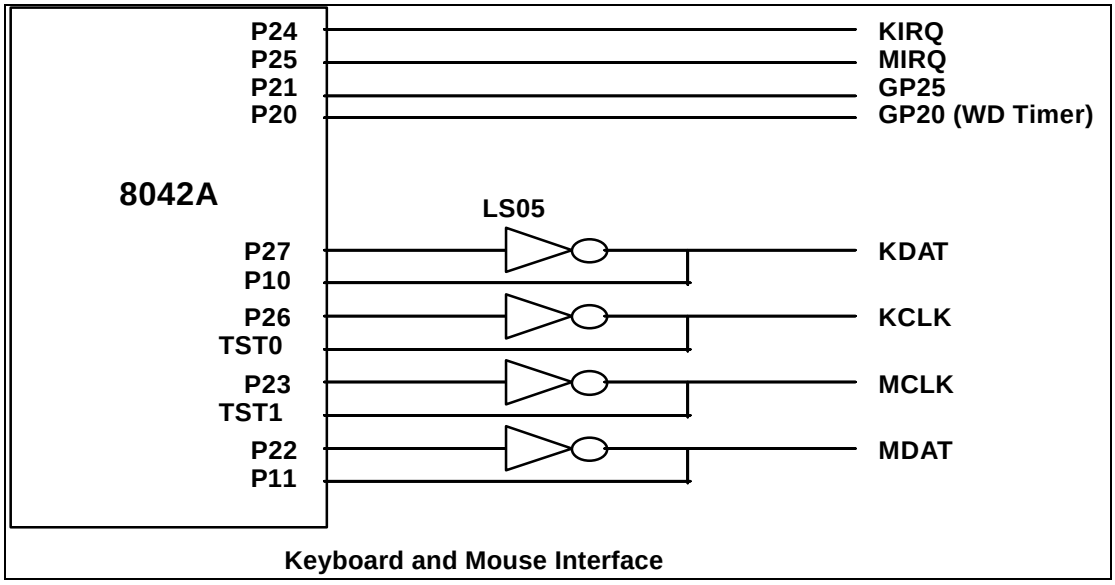
GATEA20

GATEA20 is an internal signal from the Keyboard controller (Port 21). The FDC37C93x may be configured to drive this signal onto GP25 by programming its GPI/O Configuration Register.

8042 KEYBOARD CONTROLLER AND REAL TIME CLOCK FUNCTIONAL DESCRIPTION

The FDC37C93x is a Super I/O, Real Time Clock and Universal Keyboard Controller that is designed for intelligent keyboard management in desktop computer applications. The Super I/O supports a Floppy Disk Controller, two 16550 type serial ports, one ECP/EPP Parallel Port and two IDE drive interfaces with support for four drives.

The Universal Keyboard Controller uses an 8042 microcontroller CPU core. This section concentrates on the FDC37C93x enhancements to the 8042. For general information about the 8042, refer to the "Hardware Description of the 8042" in the 8-Bit Embedded Controller Handbook.



Keyboard and Mouse Interface

KIRQ is the Keyboard IRQ
MIRQ is the Mouse IRQ
GP25 - Port 21 is GP25's alternate function output, and can be used to create a GATEA20 signal from the FDC37C93x
GP20 - This General purpose output can be configured as the 8042 Port 2.0 which is typically used to create a "keyboard reset" signal. The 8042's P20 can be used to optionally reset the Watch Dog Timer.

KEYBOARD AND RTC ISA INTERFACE

The FDC37C93x ISA interface is functionally compatible with the 8042 style host interface. It consists of the D0-7 data bus; the nIOR, nIOW and the Status register, Input Data register, and Output Data register. Table 52 shows how the interface decodes the control signals. In addition to the above signals, the host interface includes keyboard and mouse IRQ's.

Table 52 - ISA I/O Address Map

(Addresses 0x60, 0x64, 0x70 and 0x71 are qualified by AEN.)

ISA ADDRESS	BLOCK	FUNCTION
0x70 (R/W)	RTC	Address Register (70H)
0x71 (R/W)	RTC	Data Register (71H)

ISA ADDRESS	nIOW	nIOR	BLOCK	FUNCTION (NOTE 1)
0x60	0	1	KDATA	Keyboard Data Write (C/D=0)(60H)
	1	0	KDATA	Keyboard Data Read (60H)
0x64	0	1	KDCTL	Keyboard Command Write (C/D=1)(64H)
	1	0	KDCTL	Keyboard Status Read (64H)

Note 1: These registers consist of three separate 8 bit registers. Status, Data/Command Write and Data Read.

Keyboard Data Write

This is an 8 bit write only register. When written, the C/D status bit of the status register is cleared to zero and the IBF bit is set.

Keyboard Data Read

This is an 8 bit read only register. If enabled by "ENABLE FLAGS", when read, the KIRQ output is cleared and the OBF flag in the status register is cleared. If not enabled, the KIRQ and/or AUXOBF1 must be cleared in software.

Keyboard Command Write

This is an 8 bit write only register. When written, the C/D status bit of the status register is set to one and the IBF bit is set.

Keyboard Status Read

This is an 8 bit read only register. Refer to the description of the Status Register for more information.

RTC Address Register

Writing to this register sets the CMOS address that will be read or written.

RTC Data Register

A read of this register will read the contents of the selected CMOS register. A write to this register will write to the selected CMOS register.

CPU-to-Host Communication

The FDC37C93x CPU can write to the Output Data register via register DBB. A write to this register automatically sets Bit 0 (OBF) in the Status register. See Table 53.

Table 53 - Host Interface Flags

8042 INSTRUCTION	FLAG
OUT DBB	Set OBF, and, if enabled, the KIRQ output signal goes high

Host-to-CPU Communication

The host system can send both commands and data to the Input Data register. The CPU differentiates between commands and data by reading the value of Bit 3 of the Status register. When bit 3 is "1", the CPU interprets the register contents as a command. When bit 3 is "0", the CPU interprets the register contents as data. During a host write operation, bit 3 is set to "1" if SA2 = 1 or reset to "0" if SA2 = 0.

KIRQ

If "EN FLAGS" has been executed and P24 is set to a one: the OBF flag is gated onto KIRQ. The KIRQ signal can be connected to system interrupt to signify that the FDC37C93x CPU has written to the output data register via "OUT DBB,A". If P24 is set to a zero, KIRQ is forced low. On power-up, after a valid RST pulse has been delivered to the device, KIRQ is reset to 0. KIRQ will normally reflects the status of writes "DBB". (KIRQ is normally selected as IRQ1 for keyboard support.)

If "ENFLAGS has not been executed: KIRQ can be controlled by writing to P24. Writing a zero to P24 forces KIRQ low; a high forces KIRQ high.

MIRQ

If "EN FLAGS" has been executed and P25 is set to a one:; IBF is inverted and gated onto MIRQ. The MIRQ signal can be connected to system interrupt to signify that the FDC37C93x CPU has read the DBB register.

If "ENFLAGS has not been executed, MIRQ is controlled by P25, Writing a zero to P25 forces MIRQ low, a high forces MIRQ high. (MIRQ is normally selected as IRQ12 for mouse support.)

Gate A20

A general purpose P21 can be routed out to the general purpose pin GP25 for use as a software controlled Gate A20 or user defined output.

EXTERNAL KEYBOARD AND MOUSE INTERFACE

Industry-standard PC-AT-compatible keyboards employ a two-wire, bidirectional TTL interface for data transmission. Several sources also supply PS/2 mouse products that employ the same type of interface. To facilitate system expansion, the FDC37C93x provides four signal pins that may be used to implement this interface directly for an external keyboard and mouse.

The FDC37C93x has four high-drive, open-drain output, bidirectional port pins that can be used for external serial interfaces, such as ISA external keyboard and PS/2-type mouse interfaces. They are KCLK, KDAT, MCLK, and MDAT.

P26 is inverted and output as KCLK. The KCLK pin is connected to TEST0. P27 is inverted and output as KDAT. The KDAT pin is connected to P10. P23 is inverted and output as MCLK. The MCLK pin is connected to TEST1. P22 is inverted and output as MDAT. The MDAT pin is

connected to P11. NOTE: External pull-ups may be required.

KEYBOARD POWER MANAGEMENT

The keyboard provides support for two power-saving modes: soft powerdown mode and hard powerdown mode. In soft powerdown mode, the clock to the ALU is stopped but the timer/counter and interrupts are still active. In hard power down mode the clock to the 8042 is stopped. **Efforts must be made to reduce power wherever possible!**

Soft Power Down Mode

This mode is entered by executing a HALT instruction. The execution of program code is halted until either RESET is driven active or a data byte is written to the DBBIN register by a master CPU. If this mode is exited using the interrupt, and the IBF interrupt is enabled, then program execution resumes with a CALL to the interrupt routine, otherwise the next instruction is executed. If it is exited using RESET then a normal reset sequence is initiated and program execution starts from program memory location 0.

Hard Power Down Mode

This mode is entered by executing a STOP instruction. The oscillator is stopped by disabling the oscillator driver cell. When either RESET is driven active or a data byte is written to the DBBIN register by a master CPU, this mode will be exited (as above). However, as the oscillator cell will require an initialization time, either RESET must be held active for sufficient time to allow the oscillator to stabilise. Program execution will resume as above.

INTERRUPTS

The FDC37C93x provides the two 8042 interrupts. IBF and the Timer/Counter Overflow.

MEMORY CONFIGURATIONS

The FDC37C93x provides 2K of on-chip ROM and 256 bytes of on-chip RAM.

Register Definitions

Host I/F Data Register

The Input Data register and Output Data register are each 8 bits wide. A write to this 8 bit register will load the Keyboard Data Read Buffer, set the OBF flag and set the KIRQ output if enabled. A read of this register will read the data from the Keyboard Data or Command Write Buffer and clear the IBF flag. Refer to the KIRQ and Status register descriptions for more information.

Host I/F Status Register

The Status register is 8 bits wide. Table 54 shows the contents of the Status register.

Table 54 - Status Register

D7	D6	D5	D4	D3	D2	D1	D0
UD	UD	UD	UD	C/D	UD	IBF	OBF

Status Register

This register is cleared on a reset. This register is read-only for the Host and read/write by the FDC37C93x CPU.

UD Writable by FDC37C93x CPU. These bits are user-definable.

C/D (Command Data)-This bit specifies whether the input data register contains data or a command (0 = data, 1 = command). During a host data/command write operation, this bit is set to "1" if SA2 = 1 or reset to "0" if SA2 = 0.

IBF (Input Buffer Full)- This flag is set to 1 whenever the host system writes data into the input data register. Setting this flag activates the FDC37C93x CPU's nIBF (MIRQ) interrupt if enabled. When the FDC37C93x CPU reads the input data register (DBB), this bit is automatically reset and the interrupt is cleared. There is no output pin associated with this internal signal.

OBF (Output Buffer Full)- This flag is set to 1 whenever the FDC37C93x CPU write to the output data register (DBB). When the host system reads the output data register, this bit is automatically reset.

EXTERNAL CLOCK SIGNAL

The FDC37C93x X1K clock source is a 12 MHz clock generated from a 14.318 MHz clock. The reset pulse must last for at least 24 16 Mhz clock periods. The pulse-width requirement applies to both internally and externally generated reset signals. In powerdown mode, the external clock signal on X1K is not loaded by the chip.

The FDC37C93x X1C clock source must be from a crystal connected across X1C and X2C. Due to the low current internal oscillator circuit, this X1C can not be driven by an external clock signal.

DEFAULT RESET CONDITIONS

The FDC37C93x has one source of reset: an external reset via the RESET pin. Refer to Table 55 for the effect of each type of reset on the internal registers.

Table 55 - Resets

DESCRIPTION	HARDWARE RESET (RESET)
KCLK	Weak High
KDAT	Weak High
MCLK	Weak High
MDAT	Weak High
Host I/F Data Reg	N/A
Host I/F Status Reg	00H
RTCCNTRL	80H
RTCADDR	NC
RTCDATA	NC

NC: No Change N/A: Not Applicable

REAL TIME CLOCK

The Real Time Clock is a complete time of day clock with alarm and one hundred year calendar, a programmable periodic interrupt, and a programmable square wave generator.

FEATURES

- Counts seconds, minutes, and hours of the day.
- Counts days of the week, date, month and year.
- Binary or BCD representation of time, calendar and alarm.
- Three interrupts - each is separately software maskable. (No daylight savings time!)

PORT DEFINITION AND DESCRIPTION

OSC

Crystal Oscillator input. Maximum clock frequency is 32.768 KHz.

RTC Reset

The clock, calendar, or RAM functions are not affected by the system reset (RESET_DRV active). When the RESET_DRV pin is active (i.e., system reset) and the battery voltage is above 1 volt nominal, the following occurs:

1 Periodic Interrupt Enable (PIE) is cleared to 0.
2 Alarm Interrupt Enable (AIE) bit is cleared to 0.
3 Update ended Interrupt Enable (UIE) bit is cleared to 0.
4 Update ended Interrupt Flag (UF) bit is cleared to 0.
5 Interrupt Request status Flag (IRQF) bit is cleared to 0.
6 Periodic Interrupt Flag (PIF) is cleared to 0.
7 The RTC and CMOS registers are not accessable.
8 Alarm Interrupt Flag (AF) is cleared to 0.
9 nIRQ pin is in high impedance state.

When RESET_DRV is active and the battery voltage is below 1 volt nominal, the following occurs:

1 Registers 00-0D are initialized to 00h.
2 Access to all registers from the host or FDC37C93x CPU (8042) are blocked.

RTC INTERRUPT

The interrupt generated by the RTC is an active high output. The RTC interrupt output remains high as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. Activating RESET_DRV or reading register C clears the RTC interrupt.

The RTC Interrupt is brought out by programming the RTC Primary Interrupt Select to a non-zero value. If IRQ 8 is selected then the polarity of this IRQ 8 output is programmable through a bit in the OSC Global Configuration Register.

INTERNAL REGISTERS

Table 56 shows the address map of the RTC, ten bytes of time, calendar, and alarm data, four control and status bytes, 241 bytes of "CMOS" registers and one RTC control register.

Table 56 - Real Time Clock Address Map

ADDRESS	REGISTER TYPE	REGISTER FUNCTION
0	R/W	Register 0: Seconds
1	R/W	Register 1: Seconds Alarm
2	R/W	Register 2: Minutes
3	R/W	Register 3: Minutes Alarm
4	R/W	Register 4: Hours
5	R/W	Register 5: Hours Alarm
6	R/W	Register 6: Day of Week
7	R/W	Register 7: Date of Month
8	R/W	Register 8: Month
9	R/W	Register 9: Year
A	R/W	Register A:
B	R/W	Register B: (Bit 0 is Read Only)
C	R	Register C:
D	R	Register D:
E-FF	R/W	Register E-FF: General purpose

All 14 bytes are directly writable and readable by the host with the following exceptions:

a. Registers C and D are read only
b. Bit 7 of Register A is read only
c. Bits 0 of Register B is read only
d. Bits 7-1 of the Shared RTC Control register are read only.

Time Calendar and Alarm

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar and alarm by writing to these locations. The contents of the ten time, calendar and alarm bytes can be in binary or BCD as shown in Table 57.

Before initializing the internal registers, the SET bit in Register B should be set to a "1" to prevent time/calendar updates from occurring. The program initializes the ten locations in the binary or BCD format as defined by the DM bit in Register B.The SET bit may now be cleared to allow updates.

The 12/24 bit in Register B establishes whether the hour locations represent 1 to 12 or 0 to 23. The 12/24 bit cannot be changed without reinitializing the hour locations. When the 12 hour format is selected, the high order bit of the hours byte represents PM when it is a "1".

Once per second, the ten time, calendar and alarm bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the ten bytes are read at this time, the data outputs are undefined. The update cycle time is shown in Table 58. The update logic contains circuitry for automatic end-of-month recognition as well as automatic leap year compensation.

The three alarm bytes may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is any hexadecimal byte from C0 to FF inclusive. That is the two most significant bits of each byte, when set to "1" create a "don't care" situation. An alarm interrupt each hour is created with a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Table 57 - Time, Calendar and Alarm Bytes

ADD	REGISTER FUNCTION	BCD RANGE	BINARY RANGE
0	Register 0: Seconds	00-59	00-3B
1	Register 1: Seconds Alarm	00-59	00-3B
2	Register 2: Minutes	00-59	00-3B
3	Register 3: Minutes Alarm	00-59	00-3B
4	Register 4: Hours	01-12 am	01-0C
	(12 hour mode)	81-92 pm	81-8C
	(24 hour mode)	00-23	00-17
5	Register 5: Hours Alarm	01-12 am	01-0C
	(12 hour mode)	81-92 pm	81-8C
	(24 hour mode)	00-23	00-17
6	Register 6: Day of Week	01-07	01-07
7	Register 7: Day of Month	01-31	01-1F
8	Register 8: Month	01-12	01-0C
9	Register 9: Year	00-99	00-63

Update Cycle

An update cycle is executed once per second if the SET bit in Register B is clear and the DV0-DV2 divider is not clear. The SET bit in the "1" state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the seconds byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present.

The length of an update cycle is shown in Table 58. During the update cycle the time, calendar and alarm bytes are not accessible by the processor program. If the processor reads these locations before the update cycle is complete the output will be undefined. The UIP (update in progress) status bit is set during the interval. When the UIP bit goes high, the update cycle will begin 244 us later. Therefore, if a low is read on the UIP bit the user has at least 244us before time/calendar data will be changed.

Table 58 - Update Cycle Time

INPUT CLOCK FREQUENCY	UIP BIT	UPDATE CYCLE TIME	MINIMUM TIME UPDATE CYCLE
32.768 kHz	1	1948 µs	-
32.768 kHz	0	-	244 µs

Control and Status Registers

The RTC has four registers which are accessible to the processor program at all times, even during the update cycle.

REGISTER A (AH)

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP
The update in progress bit is a status flag that may be monitored by the program. When UIP is a "1" the update cycle is in progress or will soon begin. When UIP is a "0" the update cycle is not in progress and will not be for at least 244us. The time, calendar, and alarm information is fully available to the program when the UIP bit is zero. The UIP bit is a read only bit and is not affected by *RESET_DRV.* Writing the SET bit in Register B to a "1" inhibits any update cycle and then clears the UIP status bit. *The UIP bit is only valid when the RTC is enabled.* Refer to Table 58.

DV2-0
Three bits are used to permit the program to select various conditions of the 22 stage divider chain. Table 59 shows the allowable combinations. The divider selection bits are also used to reset the divider chain. When the time/calendar is first initialized, the program may start the divider chain at the precise time stored in the registers. When the divider reset is removed the first update begins one-half second later. These three read/write bits are not affected by *RESET_DRV.*

RS3-0
The four rate selection bits select one of 15 taps on the divider chain or disable the divider output. The selected tap determines rate or frequency of the periodic interrupt. The program may enable or disable the interrupt with the PIE bit in Register B. Table 60 lists the periodic interrupt rates and equivalent output frequencies that may be chosen with the RS0 - RS3 bits. These four bits are read/write bits which are not affected by *RESET_DRV.*

Table 59 - Divider Selection Bits

OSCILLATOR FREQUENCY	REGISTER A BITS			MODE
	DV2	DV1	DV0	
32.768 KHz	0	0	0	Oscillator Disabled
32.768 KHz	0	0	1	Oscillator Disabled
32.768 KHz	0	1	0	Normal Operate
32.768 KHz	0	1	1	Test
32.768 KHz	1	0	X	Test
	1	1	X	Reset Driver

Table 60 - Periodic Interrupt Rates

RATE SELECT				32.768 KHz TIME BASE	
RS3	RS2	RS1	RS0	PERIOD RATE OF INTERRUPT	FREQUENCY OF INTERRUPT
0	0	0	0	0.0	
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 us	8.192 KHz
0	1	0	0	244.141 us	4.096 KHz
0	1	0	1	488.281 us	2.048 KHz
0	1	1	0	976.562 us	1.024 KHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

REGISTER B (BH)

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0
SET	PIE	AIE	UIE	RES	DM2	24/12	DSE

SET
When the SET bit is a "0", the update functions normally by advancing the counts once per second. When the SET bit is a "1", an update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the middle of initialization. SET is a read/write bit which is not modified by RESET_DRV or any internal functions.

PIE
The periodic interrupt enable bit is a read/write bit which allows the periodic-interrupt flag (PF) bit in Register C to cause the IRQB port to be driven low. The program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3 - RS0 bits in Register A. A zero in PIE blocks IRQB from being initiated by a periodic interrupt, but the periodic flag (PF) is still set at the periodic rate. PIE is not modified by any internal function, but is cleared to "0" by a RESET_DRV.

AIE
The alarm interrupt enable bit is a read/write bit, which when set to a "1" permits the alarm flag (AF) bit in Register C to assert IRQB. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of binary 11XXXXXX). When the AIE bit is a "0", the AF bit does not initiate an IRQB signal. The RESET_DRV port clears AIE to "0". The AIE bit is not affected by any internal functions.

UIE
The update-ended interrupt enable bit is a read/write bit which enables the update-end flag (UF) bit in Register C to assert IRQB. The RESET_DRV port or the SET bit going high clears the UIE bit.

RES
Reserved - read as zero

DM
The data mode bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or by RESET_DRV. A "1" in DM signifies binary data, while a "0" in DM specifies BCD data.

24/12
The 24/12 control bit establishes the format of the hours byte as either the 24 hour mode if set to a "1", or the 12 hour mode if cleared to a "0". This is a read/write bit which is not affected by RESET_DRV or any internal function.

DSE
The daylight savings enable bit is read only and is always set to a "0" to indicate that the daylight savings time option is not available.

REGISTER C (CH) - READ ONLY REGISTER

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0
IRQF	PF	AF	UF	0	0	0	0

IRQF
The interrupt request flag is set to a "1" when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

Any time the IRQF bit is a "1", the IRQB signal is driven low. All flag bits are cleared after Register C is read or by the RESET_DRV port.

PF
The periodic interrupt flag is a read only bit which is set to a "1" when a particular edge is detected on the selected tap of the divider chain. The RS3 -RS0 bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. PF being a "1" sets the IRQF bit and initiates an IRQB signal when PIE is also a "1". The PF bit is cleared by RESET_DRV or by a read of Register C.

AF
The alarm interrupt flag when set to a "1" indicates that the current time has matched the alarm time. A "1" in AF causes a "1" to appear in IRQF and the IRQB port to go low when the AIE bit is also a "1". A RESET_DRV or a read of Register C clears the AF bit.

UF
The update-ended interrupt flag bit is set after each update cycle. When the UIE bit is also a "1", the "1" in UF causes the IRQF bit to be set and asserts IRQB. A RESET_DRV or a read of Register C causes UF to be cleared.

b3-0
The unused bits of Register C are read as zeros and cannot be written.

REGISTER D (DH) READ ONLY REGISTER

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0
VRT	0	0	0	0	0	0	0

VRT
When a "1", this bit indicates that the contents of the RTC are valid. A "0" appears in the VRT bit when the battery voltage is low. The VRT bit is read only bit which can only be set by a read of Register D. Refer to Power Management for the conditions when this bit is reset. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the time is valid.

b6:b0
The remaining bits of Register D are read as zeros and cannot be written.

Register EH-FFH: General purpose

Registers Eh-FFH are general purpose CMOS registers. These registers can be used by the host or 8051 and are fully available during the time update cycle. The contents of these registers are preserved by the battery power.

INTERRUPTS

The RTC includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from one-per-second to one-a-day. The periodic interrupt may be selected for rates from half-a-second to 122.070 us. The update ended interrupt may be used to indicate to the program that an update cycle is completed. Each of these independent interrupts are described in greater detail in other sections.

The processor program selects which interrupts, if any, it wishes to receive by writing a "1" to the appropriate enable bits in Register B. A "0" in an enable bit prohibits the IRQB port from being asserted due to that interrupt cause. When an interrupt event occurs a flag bit is set to a "1" in Register C. Each of the three interrupt sources have separate flag bits in Register C, which are set independent of the state of the corresponding enable bits in Register B. The flag bits may be used with or without enabling the corresponding enable bits. The flag bits in Register C are cleared (record of the interrupt event is erased) when Register C is read. Double latching is included in Register C to ensure the bits that are set are stable throughout the read cycle. All bits which are high when read by the program are cleared, and new interrupts are held until after the read cycle. If an interrupt flag is already set when the interrupt becomes enabled, the IRQB port is immediately activated, though the interrupt initiating the event may have occurred much earlier.

When an interrupt flag bit is set and the corresponding interrupt-enable bit is also set, the IRQB port is driven low. IRQB is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a "1" whenever the IRQB port is being driven low.

FREQUENCY DIVIDER

The RTC has 22 binary divider stages following the clock input. The output of the divider is a 1 Hz signal to the update-cycle logic. The divider is controlled by the three divider bits (DV3-DV0) in Register A. As shown in Table 59 the divider control bits can select the operating mode, or be used to hold the divider chain reset which allows precision setting of the time. When the divider chain is changed from reset to the operating mode, the first update cycle is one-half second later. The divider control bits are also used to facilitate testing of the RTC.

PERIODIC INTERRUPT SELECTION

The periodic interrupt allows the IRQB port to be triggered from once every 500 ms to once every 122.07 us. As Table 60 shows, the periodic interrupt is selected with the RS0-RS3 bits in Register A. The periodic interrupt is enabled with the PIE bit in Register B.

POWER MANAGEMENT

The RAMD signal controls all bus input to the RTC and RAM (nIOW, nIOR, RESET_DRV). When asserted, it disallows any modification of the RTC and RAM data by the host or 8051. RAMD is asserted whenever:

V_{CC} is below 4.0 volts nominal.

When the V_{CC} voltage drops below the battery voltage, the RTC switches to battery power. When V_{CC} rises above the battery voltage, the RTC switches back to system power. When the V_{CC} voltage drops below 4.0 volts nominal, all inputs are locked out so that the internal registers cannot be modified by the system. This lockout condition continues for 62 msec (min) to 125 msec (max) after the system power has been restored. The 62 msec lockout does not occur under the following conditions:

1. The Divider Chain Controls (bits 6-4) are in any mode but Normal Operation ("010").
2. The VRT bit is a "0".
3. When battery voltage is below 1 volt nominal and RESET_DRV is a "1". This will also initialize all registers 00-0D to a "00".

To minimize power consumption, the oscillator is not operational under the following conditions:

4. The Divider Chain Controls (bits 6-4) are in Oscillator Disabled mode (000, or 001).
5. If V_{CC}=0 and the battery power is removed and then re-applied (a new battery is installed) the following occurs:
   a. The oscillator is disabled immediately.
   b. Initialize all registers 00-0D to a "00" when V_{CC} is applied.

If the battery voltage is between 1 volt nominal and 2.4 volt nominal when V_{CC} is applied:

6. Clear VRT bit to "0". Maintain all other RTC bits in the state as before V_{CC} was applied

VCC	HYSTER	BATTERY	REGISTER ACCESS
<4.0	1	1	N
>4.0	0	x	Y

Hyster=1 implies that VCC <4.0 volts +/-0.25V; Hyster=0 implies that VCC >4.0 volts +/-0.25V.

CONFIGURATION

The Configuration of the FDC37C93x is very flexible and is based on the configuration architecture implemented in typical Plug-and-Play components. The FDC37C93x is designed for motherboard applications in which the resources required by their components are known. With its flexible resource allocation architecture, the FDC37C93x allows the BIOS to assign resources at POST.

SYSTEM ELEMENTS

Primary Configuration Address Decoder

After a hard reset or Power On Reset the FDC37C93x is in the Run Mode with all logical devices disabled. The logical devices may be configured through two standard Configuration I/O Ports (INDEX and DATA) by placing the FDC37C93x into Configuration Mode. The BIOS uses these configuration ports to initialize the logical devices at POST. The INDEX and DATA ports are only valid when the FDC37C93x is in Configuration Mode.

The SYSOPT pin is latched on the falling edge of the RESET_DRV or on Power On Reset to determine the configuration register's base address. The SYSOPT pin is used to select the CONFIG PORT's I/O address at power-up. The SYSOPT pin is a hardware configuration pin which is shared with the nRTS1 signal on pin 148. During reset this pin is a weak active low signal which sinks 30uA. Note: All I/O addresses are qualified with AEN.

The INDEX and DATA ports are effective only when the chip is in the Configuration State.

PORT NAME	SYSOPT= 0 (Pull-down resistor) Refer to Note 1	SYSOPT= 1 (10K Pull-up resistor)	TYPE
CONFIG PORT	0x03F0	0x0370	Write
INDEX PORT	0x03F0	0x0370	Write
DATA PORT	INDEX PORT + 1		Read/Write

Note 1: If using TTL RS232 drivers use 1K pull-down. If using CMOS RS232 drivers use 10K pull-down.

Entering the Configuration State

The device enters the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = < 0x55, 0x55>

Exiting the Configuration State

The device exits the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = < 0xAA>

Table 61 - Configuration Registers

INDEX	TYPE	HARD RESET	SOFT RESET	CONFIGURATION REGISTER
GLOBAL CONFIGURATION REGISTERS				
0x02	W	0x00	0x00	Config Control
0x03	R/W	0x03	n/a	Index Address
0x07	R/W	0x00	0x00	Logical Device Number
0x20	R	0x02	0x02	Device ID - hard wired
0x21	R	0x01	0x01	Device Rev - hard wired
0x22	R/W	0x00	0x00	Power Control
0x23	R/W	0x00	n/a	Power Mgmt
0x24	R/W	0x04	n/a	OSC
0x2D	R/W	n/a	n/a	TEST 1
0x2E	R/W	n/a	n/a	TEST 2
0x2F	R/W	0x00	n/a	TEST 3
LOGICAL DEVICE 0 CONFIGURATION REGISTERS (FDD)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61	R/W	0x03, 0xF0	0x03, 0xF0	Primary Base I/O Address
0x70	R/W	0x06	0x06	Primary Interrupt Select
0x74	R/W	0x02	0x02	DMA Channel Select
0xF0	R/W	0x0E	n/a	FDD Mode Register
0xF1	R/W	0x00	n/a	FDD Option Register
0xF2	R/W	0xFF	n/a	FDD Type Register
0xF4	R/W	0x00	n/a	FDD0
0xF5	R/W	0x00	n/a	FDD1
LOGICAL DEVICE 1 CONFIGURATION REGISTERS (IDE1)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61	R/W	0x01, 0xF0	0x01, 0xF0	Primary Base I/O Address
0x62, 0x63	R/W	0x03, 0xF6	0x03, 0xF6	Second Base I/O Address
0x70	R/W	0x0E	0x0E	Primary Interrupt Select
LOGICAL DEVICE 2 CONFIGURATION REGISTERS (IDE2)				

Table 61 - Configuration Registers

INDEX	TYPE	HARD RESET	SOFT RESET	CONFIGURATION REGISTER
0x30	R/W	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	Primary Base I/O Address
0x62, 0x63	R/W	0x00, 0x00	0x00, 0x00	Second Base I/O Address
0x70	R/W	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	n/a	IDE2 Mode Register
LOGICAL DEVICE 3 CONFIGURATION REGISTERS (Parallel Port)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	Primary Base I/O Address
0x70	R/W	0x00	0x00	Primary Interrupt Select
0x74	R/W	0x04	0x04	DMA Channel Select
0xF0	R/W	0x3C	n/a	Parallel Port Mode Register
LOGICAL DEVICE 4 CONFIGURATION REGISTERS (Serial Port 1)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	Primary Base I/O Address
0x70	R/W	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	n/a	Serial Port 1 Mode Register
LOGICAL DEVICE 5 CONFIGURATION REGISTERS (Serial Port 2)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	Primary Base I/O Address
0x70	R/W	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	n/a	Serial Port 2 Mode Register
0xF1	R/W	0x00	n/a	IR Options Register
LOGICAL DEVICE 6 CONFIGURATION REGISTERS (RTC)				
0x30	R/W	0x00	0x00	Activate
0x70	R/W	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	n/a	Real Time Clock Mode Register
0xF1	R/W	0x00	n/a	Serial EEPROM Mode Register
0xF2	R/W	0x00	0x00	Serial EEPROM Pointer

Table 61 - Configuration Registers

INDEX	TYPE	HARD RESET	SOFT RESET	CONFIGURATION REGISTER
0xF3	W	n/a	n/a	Write EEPROM Data
0xF4	bits[6:0] R bit[7] R/W	0x03	0x03	Write Status
0xF5	R	n/a	n/a	Read EEPROM Data
0xF6	R	n/a	n/a	Read Status
LOGICAL DEVICE 7 CONFIGURATION REGISTERS (Keyboard)				
0x30	R/W	0x00	0x00	Activate
0x70	R/W	0x00	0x00	Primary Interrupt Select
0x72	R/W	0x00	0x00	Second Interrupt Select
LOGICAL DEVICE 8 CONFIGURATION REGISTERS (Aux I/O)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	Primary Base I/O Address
0x62, 0x63	R/W	0x00, 0x00	0x00, 0x00	Second Base I/O Address
0xE0	R/W	0x01	n/a	GP10
0xE1	R/W	0x01	n/a	GP11
0xE2	R/W	0x01	n/a	GP12
0xE3	R/W	0x01	n/a	GP13
0xE4	R/W	0x01	n/a	GP14
0xE5	R/W	0x01	n/a	GP15
0xE6	R/W	0x01	n/a	GP16
0xE7	R/W	0x01	n/a	GP17
0xE8	R/W	0x01	n/a	GP20
0xE9	R/W	0x01	n/a	GP21
0xEA	R/W	0x01	n/a	GP22
0xEB	R/W	0x01	n/a	GP23
0xEC	R/W	0x01	n/a	GP24
0xED	R/W	0x01	n/a	GP25
0xF0	R/W	0x00	n/a	GP_INT
0xF1	R/W	0x00	n/a	GPR_GPW_EN
0xF2	R/W	0x00	n/a	WDT_VAL

Table 61 - Configuration Registers

INDEX	TYPE	HARD RESET	SOFT RESET	CONFIGURATION REGISTER
0xF3	R/W	0x00	n/a	WDT_CFG
0xF4	R/W[Note1]	0x00	n/a	WDT_CTRL

Note1 : this register contains some bits which are read or write only.

Chip Level (Global) Control/Configuration Registers[0x00-0x2F]

The chip-level (global) registers lie in the address range [0x00-0x2F]. The design MUST use all 8 bits of the ADDRESS Port for register selection. All unimplemented registers and bits ignore writes and return zero when read.

The INDEX PORT is used to select a configuration register in the chip. The DATA PORT is then used to access the selected register. These registers are accessable only in the Configuration Mode.

Table 62 - Chip Level Registers

REGISTER	ADDRESS	DESCRIPTION	STATE
Chip (Global) Control Registers			
	0x00 - 0x01	Reserved - Writes are ignored, reads return 0.	
Config Control Default = 0x00	0x02 W	The hardware automatically clears this bit after the write, there is no need for software to clear the bits. Bit 0 = 1: Soft Reset. Refer to the "Configuration Registers" table for the soft reset value for each register.	C
Index Address	0x03 R/W	Bit[7] = 1 Enable GP1, GP2, +*WDT_CTRL* when not in configuration mode = 0 Disable GP1, GP2, +*WDT_CTRL* access when not in configuration mode (Default) Bits [6:2] Reserved - Writes are ignored, reads return 0. Bits[1:0] Sets GP1/GP2 selection register used when in Run mode (not in Configuration Mode). = 11 0xEA (Default) = 10 0xE4 = 01 0xE2 = 00 0xE0	
	0x04 - 0x06	Reserved - Writes are ignored, reads return 0.	
Logical Device # Default = 0x00	0x07 R/W	A write to this register selects the current logical device. This allows access to the control and configuration registers for each logical device. Note: the Activate command operates only on the selected logical device.	C
Card Level Reserved	0x08 - 0x1F	Reserved - Writes are ignored, reads return 0.	

Table 62 - Chip Level Registers

REGISTER	ADDRESS	DESCRIPTION	STATE
Chip Level, SMSC Defined			
Device ID Hard wired = 0x02	0x20 R	A read only register which provides device identification. Bits[7:0] = 0x02 when read	C
Device Rev Hard wired = 0x01	0x21 R	A read only register which provides device revision information. Bits[7:0] = 0x01 when read	C
PowerControl Default = 0x00. on POR or Reset_Drv hardware signal.	0x22 R/W	Bit[0] FDC Power Bit[1] IDE1 Enable Bit[2] IDE2 Enable Bit[3] Parallel Port Power Bit[4] Serial Port 1 Power Bit[5] Serial Port 2 Power Bit[6:7] Reserved (read as 0) = 0 Power off or disabled = 1 Power on or enabled	C
Power Mgmt Default = 0x00. on POR or Reset_Drv hardware signal	0x23 R/W	Bit[0] FDC Bit[1] IDE1 Bit[2] IDE2 Bit[3] Parallel Port Bit[4] Serial Port 1 Bit[5] Serial Port 2 Bit[6:7] Reserved (read as 0) = 0 Intelligent Pwr Mgmt off = 1 Intelligent Pwr Mgmt on	C
OSC Default = 0x04, on POR or Reset_Drv hardware signal.	0x24 R/W	Bits[1:0] Reserved, set to zero Bits[3:2] OSC = 01 Osc is on, BRG clock is on. = 10 Same as above (01) case. = 00 Osc is on, BRG Clock Enabled. = 11 Osc is off, BRG clock is disabled. Bit [*5*:4] *Reserved*, set to zero Bit [6] 16 Bit Address Qualification = 0 12 Bit Address Qualification = 1 16 Bit Address Qualification (Refer to the 16-bit Address Qualification in the SMSC Defined Logical Device Configuration Register, Device 2 section.) Bit[7] IRQ8 Polarity	C

Table 62 - Chip Level Registers

REGISTER	ADDRESS	DESCRIPTION	STATE
		= 0 IRQ8 is active high = 1 IRQ8 is active low	
Chip Level Vendor Defined	0x25 -0x2C	Reserved - Writes are ignored, reads return 0.	
TEST 1	0x2E R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.	C
TEST 2	0x2E R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.	C
TEST 3 Default = 0x00, on POR or Reset_Drv hardware signal.	0x2F R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.	C

Logical Device Configuration/Control Registers [0x30-0xFF]

Used to access the registers that are assigned to each logical unit. This chip supports nine logical units and has nine sets of logical device registers. The nine logical devices are Floppy, IDE1, IDE2, Parallel, Serial 1 and Serial 2, Real Time Clock, Keyboard Controller, and Auxiliary_I/O. A separate set (bank) of control and configuration registers exists for each logical device and is selected with the Logical Device # Register (0x07).

The INDEX PORT is used to select a specific logical device register. These registers are then accessed through the DATA PORT.

The Logical Device registers are accessible only when the device is in the Configuration State. The logical register addresses are:

Table 63 - Logical Device Registers

LOGICAL DEVICE REGISTER	ADDRESS	DESCRIPTION	STATE
Activate[Note1] Default = 0x00	(0x30)	Bits[7:1] Reserved, set to zero. Bit[0] = 1 Activates the logical device currently selected through the Logical Device # register. = 0 Logical device currently selected is inactive	C
Logical Device Control	(0x31-0x37)	Reserved - Writes are ignored, reads return 0.	C
Logical Device Control	(0x38-0x3f)	Vendor Defined - Reserved - Writes are ignored, reads return 0.	C
Mem Base Addr	(0x40-0x5F)	Reserved - Writes are ignored, reads return 0.	C
I/O Base Addr. (see Device Base I/O Address Table) Default = 0x00	(0x60-0x6F) 0x60,2,... = addr[15:8] 0x61,3,... = addr[7:0]	All logical devices contain 0x60, 0x61. IDE1 and IDE2, (Logical Devices 0x01 and 0x02 respectively) contain 0x60 - 0x63 since the IDE registers are split and two base addresses are required. In the case of IDE [0x60,0x61] are used to set the I/O base of the TASK FILE registers and [0x62,0x63] are used to set the I/O base of the MISCELLANEOUS AT register[Note2]. Logical Device 0x08 contains 0x60 - 0x63 to support GPA on base address defined by 0x60:0x61 and GPW on a base address defined by 0x62:0x63. Unused registers will ignore writes and return zero when read.	C

Table 63 - Logical Device Registers

LOGICAL DEVICE REGISTER	ADDRESS	DESCRIPTION	STATE
Interrupt Select Defaults : 0x70 = 0x00, 0x72 = 0x00,	(0x70,072)	0x70 is implemented for each logical device. Refer to Interrupt Configuration Register description. Only the keyboard controller uses Interrupt Select register 0x72. Unused register (0x72) will ignore writes and return zero when read. Interrupts default to edge high (ISA compatible).	C
	(0x71,0x73)	Reserved - not implemented. These register locations ignore writes and return zero when read.	
DMA Channel Select Default = 0x04	(0x74,0x75)	Only 0x74 is implemented for FDC , and Parallel port. 0x75 is not implemented and ignores writes and returns zero when read. Refer to DMA Channel Configuration.	C
32-Bit Memory Space Configuration	(0x76-0xA8)	Reserved - not implemented. These register locations ignore writes and return zero when read.	
Logical Device	(0xA9-0xDF)	Reserved - not implemented. These register locations ignore writes and return zero when read.	C
Logical Device Config.	(0xE0-0xFE)	Reserved - Vendor Defined (see SMSC defined Logical Device Configuration Registers)	C
Reserved	0xFF	Reserved	C

Note 1: A logical device will be active and powered up according to the following equation:

DEVICE ON (ACTIVE) = (Activate Bit SET or Pwr/Control Bit SET).

The Logical device's Activate Bit and its Pwr/Control Bit are linked such that setting or clearing one sets or clears the other. If the I/O Base Addr of the logical device is not within the Base I/O range as shown in the Logical Device I/O map, then read or write is not valid and is ignored.

Note2: The IDE/FDC split register, normally found at either 0x3F7 or 0x377 is now an FDC support only register. The IDE logical Device will now support only a status register (typically found at 0x3F6 or 0x376). The IDE Decoder operates as follows :

nHDCS0# = IDE TASK BASE + [7:0]
nHDCS1# = IDE MISC AT BASE + 0 (typically located at 0x3F6 or 0x376)

Table 64 - I/O Base Address Configuration Register Description

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (NOTE3)	FIXED BASE OFFSETS
0x00	FDC	0x60,0x61	[0x100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : SRA +1 : SRB +2 : DOR +3 : TSR +4 : MSR/DSR +5 : FIFO +7:DIR/CCR
0x01	IDE1	0x60,0x61	[0x100:0x0FF8] ON 8 BYTE BOUNDARIES	**IDE TASK** +0 : Data Register (16 bit) +1 : ERRF/WPRE +2 : Sector Count +3 : Sector Number +4 : Cylinder Low +5 : Cylinder High +6 : Head,Drive +7 : Status/Command
		0x62,0x63	[0x100:0x0FFF] ON 1 BYTE BOUNDARIES	**IDE MISC AT** + 0 : Status/Fixed Disk
0x02	IDE2	0x60,0x61	[0x100:0x0FF8] ON 8 BYTE BOUNDARIES	**IDE TASK** +0 : Data Register (16 bit) +1 : ERRF/WPRE +2 : Sector Count +3 : Sector Number +4 : Cylinder Low +5 : Cylinder High +6 : Head,Drive +7 : Status/Command
		0x62,0x63	[0x100:0x0FFF] ON 1 BYTE BOUNDARIES	**IDE MISC AT** + 0 : Status/Fixed Disk

Table 64 - I/O Base Address Configuration Register Description

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (NOTE3)	FIXED BASE OFFSETS
0x03	Parallel Port	0x60,0x61	[0x100:0x0FFC] ON 4 BYTE BOUNDARIES (EPP Not supported) or [0x100:0x0FF8] ON 8 BYTE BOUNDARIES (all modes supported, EPP is only available when the base address is on an 8-byte boundary)	+0 : Data|ecpAfifo +1 : Status +2 : Control +3 : EPP Address +4 : EPP Data 0 +5 : EPP Data 1 +6 : EPP Data 2 +7 : EPP Data 3 +400h : cfifo|ecpDfifo|tfifo|cnfgA +401h : cnfgB +402h : ecr
0x04	Serial Port 1	0x60,0x61	[0x100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : RB/TB|LSB div +1 : IER|MSB div +2 : IIR/FCR +3 : LCR +4 : MSR +5 : LSR +6 : MSR +7 : SCR
0x05	Serial Port 2	0x60,0x61	[0x100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : RB/TB|LSB div +1 : IER|MSB div +2 : IIR/FCR +3 : LCR +4 : MSR +5 : LSR +6 : MSR +7 : SCR
0x06	RTC	**n/a**	Not Relocatable Fixed Base Address	+0 : Address Register +1 : Data Register
0x07	KYBD	**n/a**	Not Relocatable Fixed Base Address	+0 : Data Register +4 : Command/Status Reg.
0x08	Aux. I/O	0x60,0x61 0x62,0x63	[0x00:0xFFF] ON 1 BYTE BOUNDARIES [0x00:0xFFF] ON 1 BYTE BOUNDARIES	+0 : GPR +0 : GPW

Note 3: This chip uses ISA address bits [A11:A0] to decode the base address of each of its logical devices.

Table 65 - Interrupt Select Configuration Register Description

NAME	REG INDEX	DEFINITION	STATE
Interrupt request level select 0	0x70 (R/W)	Bits[3:0] selects which interrupt level is used for Interrupt 0. 0x00=no interrupt selected. 0x01=IRQ1 0x02=IRQ2 o o o 0x0E=IRQ14 0x0F=IRQ15 Note: All interrupts are edge high (except ECP/EPP)	C

Note: An Interrupt is activated by setting the Interrupt Request Level Select 0 register to a non-zero value AND :
for the FDC logical device by setting DMAEN, bit D3 of the Digital Output Register.
for the PP logical device by setting IRQE, bit D4 of the Control Port and in addition
for the PP logical device in ECP mode by clearing serviceIntr, bit D2 of the ecr.
for the Serial Port logical device by setting any combination of bits D0-D3 in the IER and by setting the OUT2 bit in the UART's Modem Control (MCR) Register.
for the RTC by (refer to the RTC section of this spec.)
for the KYBD by (refer to the KYBD controller section of this spec.)

Note: IRQ pins must tri-state if not used/selected by any Logical Device. Refer to Appendix A

Table 66 - DMA Channel Select Configuration Register Description

NAME	REG INDEX	DEFINITION	STATE
DMA Channel select 0	0x74 (R/W)	Bits[2:0] select the DMA Channel. 0x00=DMA0 0x01=DMA1 0x02=DMA2 0x03=DMA3 0x04-0x07= No DMA active	C

Note: A DMA channel is activated by setting the DMA Channel Select 0 register to [0x00-0x03] AND :
for the FDC logical device by setting DMAEN, bit D3 of the Digital Output Register.
for the PP logical device in ECP mode by setting dmaEn, bit D3 of the ecr.

Note: DMAREQ pins must tri-state if not used/selected by any Logical Device. Refer to Appendix A

SMSC Defined Logical Device Configuration Registers

The SMSC Specific Logical Device Configuration Registers reset to their default values only on hard resets generated by POR or the RESET_DRV signal. These registers are not affected by soft resets.

Table 67 - Floppy Disk Controller, Logical Device 0 [Logical Device Number = 0x00]

NAME	REG INDEX	DEFINITION	STATE
FDD Mode Register Default = 0x0E	0xF0 R/W	Bit[0] Floppy Mode = 0 Normal Floppy Mode (default) = 1 Enhanced Floppy Mode 2 (OS2) Bit[1] FDC DMA Mode = 0 Burst Mode is enabled = 1 Non-Burst Mode (default)[Note4] Bit[3:2] Interface Mode = 11 AT Mode (default) = 10 (Reserved) = 01 PS/2 = 00 Model 30 Bit[4] : Swap Drives 0,1 Mode = 0 No swap (default) = 1 Drive and Motor sel 0 and 1 are swapped. Bits[7:5] Reserved, set to zero.	C
FDD Option Register Default = 0x00	0xF1 R/W	Bits[1:0] Reserved, set to zero Bits[3:2] Density Select = 00 Normal (default) = 01 Normal (reserved for users) = 10 1 (forced to logic "1") = 11 0 (forced to logic "0") Bits[5:4] Media ID Polarity = 00 (default) = 01 = 10 = 11 Bits[7:6] Boot Floppy = 00 FDD 0 (default) = 01 FDD 1 *= 10 Reserved (neither drive A or B is a boot drive).* *= 11 Reserved (neither drive A or B is a boot drive).*	C

Table 67 - Floppy Disk Controller, Logical Device 0 [Logical Device Number = 0x00]

NAME	REG INDEX	DEFINITION	STATE
FDD Type Register Default = 0xFF	0xF2 R/W	Bits[1:0] Floppy Drive A Type Bits[3:2] Floppy Drive B Type Bits[5:4] *Reserved (could be used to store Floppy Drive C type)* Bits[7:6] *Reserved (could be used to store Floppy Drive D Type)* *Note: The FDC37C93x supports two floppy drives*	C
	0xF3 R	Reserved, Read as 0 (read only)	C
FDD0 Default = 0x00	0xF4 R/W	Bits[1:0] Drive Type select Bits[2] Read as 0 (read only) Bits[3:4] Data Rate Table Select Bits[5] Read as 0 (read only) Bits[6] Precomp Disable Bits[7] Read as 0 (read only)	C
FDD1	0xF5 R/W	Refer to definition and default for 0xF4	C

Table 68 - IDE Drive 1, Logical Device 1 [Logical Device Number = 0x01]

NAME	REG INDEX	DEFINITION	STATE
IDE1 Mode Register		IDE1 HI and LO byte pass through external buffers controlled by IDE1_OE.	

Table 69 - IDE Drive 2, Logical Device 2 [Logical Device Number = 0x02]

NAME	REG INDEX	DEFINITION	STATE
IDE2 Mode Register Default = 0x00	0xF0 R/W	Bit[0] : IDE2 Configuration Options = 0 : IDE2 HI and LO bytes pass through external buffers controlled by IDE2_OE. = 1 : IDE2_OE not used. IDE2 HI and LO byte passes through external buffer controlled by IDE1_OE. Bits[7:1] : Reserved, set to zero	C

16 Bit Address Qualification

When IDE2 is not active (IDE2 active bit = L2 - CR30 - Bit0), nHDCS2, nHDCS3 and IDE2_IRQ are in high impedance; 16_ADR = CR24.6.

	IDE2 **ACTIVE BIT = 1** **16BIT_ADR = X**	***IDE2*** **ACTIVE BIT = 0** **16BIT_ADR = 0**	***IDE2*** **ACTIVE BIT = 0** **16BIT_ADR = 1**
nHDCS2 (pin 27)	Output	Hi-Z	Input (SA13)
nHDCS3 (pin 28)	Output	Hi-Z	Input (SA14)
IDE2_IRQ (pin 29)	Input (IRQ)	Hi-Z	Input (SA15)
nCS (pin 53)	Input (SA12)	Input (SA12)	Input (SA12)

Table 70 - Parallel Port, Logical Device 3 [Logical Device Number = 0x03]

NAME	REG INDEX	DEFINITION	STATE
PP Mode Register Default = 0x3C	0xF0 R/W	Bits[2:0] Parallel Port Mode = 100 Printer Mode (default) = 000 Standard and Bi-directional (SPP) Mode = 001 EPP-1.9 and SPP Mode = 101 EPP-1.7 and SPP Mode = 010 ECP Mode = 011 ECP and EPP-1.9 Mode = 111 ECP and EPP-1.7 Mode Bit[6:3] ECP FIFO Threshold 0111b (default) Bit[7] PP Interupt Type **Not valid when the parallel port is in the Printer Mode (100) or the Standard & Bi-directional Mode (000).** = 1 Pulsed Low, released to high-Z (665/666). = 0 IRQ follows nACK when parallel port in EPP Mode or [Printer,SPP, EPP] under ECP. IRQ level type when the parallel port is in ECP, TEST, or Centronics FIFO Mode.	C

Table 71 - Serial Port 1, Logical Device 4 [Logical Device Number = 0x04]

NAME	REG INDEX	DEFINITION	STATE
Serial Port 1 Mode Register Default = 0x00	0xF0 R/W	Bit[0] MIDI Mode = 0 MIDI support disabled (default) = 1 MIDI support enabled Bit[1] High Speed = 0 High Speed Disabled(default) = 1 High Speed Enabled Bit[7:2] Reserved, set to zero	C

Table 72 - Serial Port 2, Logical Device 5 [Logical Device Number = 0x05]

NAME	REG INDEX	DEFINITION	STATE
Serial Port 2 Mode Register Default = 0x00	0xF0 R/W	Bit[0] MIDI Mode = 0 MIDI support disabled (default) = 1 MIDI support enabled Bit[1] High Speed = 0 High Speed disabled(default) = 1 High Speed enabled Bit[7:2] Reserved, set to zero	C
IR Option Register Default = 0x00 This register sets the IR Options and uses the same bit definitions as the FDC37C667	0xF1 R/W	Bit[0] Receive Polarity = 0 Active High (Default) = 1 Active Low Bit[1] Transmit Polarity = 0 Active High (Default) = 1 Active Low Bit[2] Duplex Select = 0 Full Duplex (Default) = 1 Half Duplex Bits[5:3] IR Mode = 000 Standard (Default) = 001 IrDA = 010 ASK-IR = 011 Reserved = 1xx Reserved Bit[6] IR Location Mux = 0 Use Serial port TX2 and RX2 (Default) = 1 Use alternate IRRX (pin 98) and IRTX (pin 99) Bit[7] Reserved	C

Table 73 - RTC, Logical Device 6 [Logical Device Number = 0x06]

NAME	REG INDEX	DEFINITION	STATE
RTC Mode Register Default = 0x00	0xF0 R/W	Bit[0] = 1 : Lock CMOS RAM 80-9Fh Bit[1] = 1 : Lock CMOS RAM A0-BFh Bit[2] = 1 : Lock CMOS RAM C0-DFh Bit[3] = 1 : Lock CMOS RAM E0-FFh Bits[6:4] Reserved, set to zero Bit[7] = 0 Select lower 128-byte bank of RAM (includes RTC RAM). = 1 Select Upper 128-byte bank of RAM Note: Once set, bits[3:0] can not be cleared by a write; bits[3:0] are cleared only on Power On Reset or upon a Hard Reset.	C
Serial EEPROM Mode Register Default = 0x00	0xF1 R/W	Bit[0] = 1 : Lock EEPROM 00-1Fh Bit[1] = 1 : Lock EEPROM 20-3Fh Bit[2] = 1 : Lock EEPROM 40-5Fh Bit[3] = 1 : Lock EEPROM 60-7Fh Bit[4] EEPROM Type = 0 256 bit,1K-bit (93C06,93C46) = 1 2K-bit,4K-bit (93C56,93C66) Bits[7:5] Reserved, set to zero Note: Once set, bits[3:0] can not be cleared by a write; bits[3:0] are cleared only on Power On Reset or upon a Hard Reset.	C
Serial EEPROM Pointer Default = 0x00, on POR, Reset_Drv or Software Reset.	0xF2 R/W	Use this register to set the Serial EEPROM's pointer. The value in this register always reflects the current EEPROM pointer address. The Serial Device Pointer increments after each pair of reads from the Resource Data register or after each pair of writes to the Program Resource Data register.	C
Write EEPROM Data	0xF3 W	This register is used to program the serial device from the host. This device supports serial EEPROMS in x16 configurations. Two bytes must be written to this register in order to generate a EEPROM write cycle. The LSB leads the MSB. The first write to this register resets bit 0 of the Write Status register. The second write resets bit 1 of the Write Status register and generates a write cycle to the serial EEPROM. The Write Status register must be polled before performing a pair of writes to this register.	C

Table 73 - RTC, Logical Device 6 [Logical Device Number = 0x06]

NAME	REG INDEX	DEFINITION	STATE
Write Status Default = 0x03, on POR, Reset_Drv or Software Reset.	0xF4 Bit[6:0] Read Only Bit[7] R/W	Bits [1:0] = 1,1 Indicates that the Write EEPROM Data register is ready to accept a pair of bytes. = 1,0 Bit 0 is cleared on the first write of the Write EEPROM Data register. This status indicates that the serial device controller has received one byte (LSB) and is waiting for the second byte (MSB). = 0,0 Bit 1 is cleared on the second write of the Write EEPROM Data register indicating that two bytes have been accepted and that the serial device interface is busy writing the word to the EEPROM. Bits [6:2] Reserved, set to zero Bit [7] = 0 Enables a prefetch of serial EEPROM when the Serial EEPROM Pointer Register is written. This will typically be used when the host CPU wishes random read access from the serial EEPROM. = 1 Disables a prefetch of serial EEPROM when the Serial EEPROM Pointer Register is written. This bit is typically set when the host CPU wishes to perform random word or block writes to the serial EEPROM.	C

Table 73 - RTC, Logical Device 6 [Logical Device Number = 0x06]

Read EEPROM Data	0xF5 R	This register allows the host to read data from the serial EEPROM. Data is not valid in this register until bit-0 of the Read Status Register is set. Since the EEPROM is a 16-bit device this register presents the LSB followed by th MSB for each pair of register reads. Immediately after the MSB is read bit 0 of the Read Status Register will be cleared, then the Serial EEPROM Pointer Register will be auto-incremented, then the next word of EEPROM data will be fetched, followed by the Read Status Register, bit 0 being set.	C
Read Status	0xF6 R	Bit 0 = 1 indicates that data in the Read EEPROM Data register is valid. This bit is cleared when EEPROM Data is read until the next byte is valid. Reading the Read EEPROM Data register when bit-0 is clear will have no detremental effects; the data will simply be invalid.	C

KBYD, Logical Device 7 [Logical Device Number = 0x07]. No SMSC defined registers for this device, all accesses to 0xF0 through 0xFF return zero.

Table 74 - Auxilliary I/O, Logical Device 8 [Logical Device Number = 0x08]

NAME	REG INDEX	DEFINITION	STATE
GP10 Default = 0x01	0xE0	General Purpose I/0 bit 1.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Int En =1 Enable Combined IRQ =0 Disable Combined IRQ Bit[3] Alt Func (If configured as input, the input signal is steered to the selected IRQ) =1 Select alternate function =0 Select basic I/O function Bits[7:4] Alt Fuct IRQ mapping 1111 = IRQ15 ..... 0011 = IRQ3 0010 = Invalid 0001 = IRQ1 0000 = Disable	C
GP11 Default = 0x01	0xE1	General Purpose I/0 bit 1.1 Same as for GP10	C
GP12 Default = 0x01	0xE2	General Purpose I/0 bit 1.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity :=1 Invert, =0 No Invert Bit[2] Int En =1 Enable Combined IRQ =0 Disable Combined IRQ Bit[3] Alt Func : WDT output or IRRX input. =1 Select alternate function =0 Select basic I/O function (IRRX - if bit-6 of the IR Options Register is set) Bits[7:4] : Reserved = 0000	C

Table 74 - Auxilliary I/O, Logical Device 8 [Logical Device Number = 0x08]

NAME	REG INDEX	DEFINITION	STATE
GP13 Default = 0x01	0xE3	General Purpose I/0 bit 1.3 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Int En =1 Enable Combined IRQ =0 Disable Combined IRQ Bit[3] Alt Func : Power LED or IRTX output =1 Select alternate function =0 Select basic I/O function (IRTX - if bit-6 of the IR Options Register is set) Bits[7:4] Reserved = 0000	C
GP14 Default = 0x01	0xE4	General Purpose I/0 bit 1.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Int En =1 Enable Combined IRQ =0 Disable Combined IRQ Bit[3] Alt Func: General Purpose Address Decode (Active Low) Decodes two address bytes =1 Select alternate function =0 Select basic I/O function Bits[7:4] Reserved = 0000	C
GP15 Default = 0x01	0xE5	General Purpose I/0 bit 1.5 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Int En =1 Enable Combined IRQ =0 Disable Combined IRQ Bit[3] Alt Func: Gen. Purpose Write Strobe (Active Low) =1 Select alternate function =0 Select basic I/O function Bits[7:4] Reserved = 0000	C

Table 74 - Auxilliary I/O, Logical Device 8 [Logical Device Number = 0x08]

NAME	REG INDEX	DEFINITION	STATE
GP16 Default = 0x01	0xE6	General Purpose I/0 bit 1.6 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Int En =1 Enable Combined IRQ =0 Disable Combined IRQ Bit[4:3] Alt Func: Joystick (Active Low) =01 Joystick RD Stb function =10 Joystick CS function =00 Select basic I/O function Bits[7:5] Reserved = 000	C
GP17 Default = 0x01	0xE7	General Purpose I/0 bit 1.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Int En =1 Enable Combined IRQ =0 Disable Combined IRQ Bit[3] Alt Func : Joystick Write Strobe (Active Low) =1 Select alternate function =0 Select basic I/O function Bits[7:4] Reserved = 0000	C
GP20 Default = 0x01	0xE8	General Purpose I/0 bit 2.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Int En :=1 Enable Combined IRQ =0 Disable Combined IRQ Bit[3] Alt Func: IDE2 buffer enable (Active Low) =1 Select alternate function =0 Select basic I/O function Bit[4] Alt func: *8042 P20, Typically used to generate a "Keyboard Reset" used by systems in order to switch from "protected mode" back to "real mode"* =1 Select alternate function =0 Select basic I/O function Bits[7:5] Reserved = 000 *Note: Bit[3] and Bit[4] should not both be set at the same time*	C

Table 74 - Auxilliary I/O, Logical Device 8 [Logical Device Number = 0x08]

NAME	REG INDEX	DEFINITION	STATE
GP21 Default = 0x01	0xE9	General Purpose I/0 bit 2.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Int En =1 Enable Combined IRQ =0 Disable Combined IRQ Bit[3] Alt Func: Serial EEPROM Data In =1 Select alternate function =0 Select basic I/O function Bits[7:4] Reserved = 0000	C
GP22 Default = 0x01	0xEA	General Purpose I/0 bit 2.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Int En =1 Enable Combined IRQ =0 Disable Combined IRQ Bit[3] Alt Func: Serial EEPROM Data Out =1 Select alternate function =0 Select basic I/O function Bits[7:4] Reserved = 0000	C
GP23 Default = 0x01	0xEB	General Purpose I/0 bit 2.3 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Int En =1 Enable Combined IRQ =0 Disable Combined IRQ Bit[3] Alt Func: Serial EEPROM clock =1 Select alternate function =0 Select basic I/O function Bits[7:4] Reserved = 0000	C
GP24 Default = 0x01	0xEC	General Purpose I/0 bit 2.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Int En =1 Enable Combined IRQ =0 Disable Combined IRQ Bit[3] Alt Func: Serial EEPROM enable =1 Select alternate function =0 Select basic I/O function Bits[7:4] Reserved = 0000	C

Table 74 - Auxilliary I/O, Logical Device 8 [Logical Device Number = 0x08]

NAME	REG INDEX	DEFINITION	STATE
GP25 Default = 0x01	0xED	General Purpose I/0 bit 2.5 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Int En :=1 Enable Combined IRQ =0 Disable Combined IRQ Bit[3] Alt Func: GATEA20 =1 Select alternate function =0 Select basic I/O function Bits[7:4] : Reserved, = 0000	C
	0xEE-0xEF	Reserved	C
GP_INT Default = 0x00	0xF0	General Purpose I/O Combined Interrupt Bits[2:0] Reserved, = 000 Bit[3] GP IRQ Filter Select 0 = Debounce Filter Bypassed 1 = Debounce Filter Enabled Bits[7:4] Combined IRQ mapping 1111 = IRQ15 ..... 0011 = IRQ3 0010 = Invalid 0001 = IRQ1 0000 = Disable	C
GP*A*_GPW_EN Default = 0x00	0xF1	General Purpose Read/Write enable Bit[0] *=1 enable GP Addr Decoder* *=0 disable GPA decoder.* Bit[1] =1 enable GPW, =0 disable GPW Bits[7:2] Reserved, = 000000 Note: if the logical device's activate bit is not set then bits 0 and 1 have no effect.	C
WDT_VAL Default = 0x00	0xF2	Watch-dog Timer Time-out Value Binary coded, units = minutes 0x00 Time out disabled 0x01 Time-out = 1 minute ..... 0xFF Time-out = 255 minutes	C

Table 74 - Auxilliary I/O, Logical Device 8 [Logical Device Number = 0x08]

NAME	REG INDEX	DEFINITION	STATE
WDT_CFG Default = 0x00	0xF3	Watch-dog timer Configuration Bit[0] Joy-stick Enable =1 WDT is reset upon an I/O read or write of the Game Port =0 WDT is not affected by I/O reads or writes to the Game Port. Bit[1] Keyboard Enable =1 WDT is reset upon a Keyboard interrupt. =0 WDT is not affected by Keyboard interrupts. Bit[2] Mouse Enable =1 WDT is reset upon a Mouse interrupt =0 WDT is not affected by Mouse interrupts. Bit[3] PWRLED Time-out enable =1 Enables the Power LED to toggle at a 1Hz rate with 50 percent duty cycle while the Watch-dog Status bit is set. =0 Disables the Power LED toggle during Watch-dog timeout status. Bits[7:4] WDT Interrupt Mapping 1111 = IRQ15 ..... 0011 = IRQ3 0010 = Invalid 0001 = IRQ1 0000 = Disable	C

Table 74 - Auxilliary I/O, Logical Device 8 [Logical Device Number = 0x08]

NAME	REG INDEX	DEFINITION	STATE
WDT_CTRL Default = 0x00	0xF4	Watch-dog timer Control Bit[0] Watch-dog Status Bit, R/W =1 WD timeout occured =0 WD timer counting Bit[1] Power LED Toggle Enable, R/W =1 Toggle Power LED at 1Hz rate with 50 percent duty cycle. (1/2 sec. on, 1/2 sec. off) =0 Disable Power LED Toggle Bit[2] Force Timeout, W =1 Forces WD timeout event; this bit is self-clearing Bit[3] P20 Force Timeout Enable, R/W = 1 Allows rising edge of P20, from the Keyboard Controller, to force the WD timeout event. A WD timeout event may still be forced by setting the Force Timeout Bit, bit 2. = 0 P20 activity does not generate the WD timeout event. Note: The P20 signal will remain high for a minimum of 1us and can remain high indefinitely. Therefore, when P20 forced timeouts are enabled, a self-clearing edge-detect circuit is used to generate a signal which is ORed with the signal generated by the Force Timeout Bit. Bits[7:4] Reserved - Set to 0	C

Note: This register is also available at index 03 when not in configuration mode. See Table 47B.

RESET_DRIVE

This is an active high input. The input is digitally filtered.

When this input is detected the device powers-up to its internal default state (all logical devices disabled) and remains inactive until configured otherwise.

Sequence of Operation

1. At power-up, or when the RESET_DRV signal is active all logical device configuration registers are set to their internal default state.

2. The chip enters the RUN State, and is ready to be placed into Configuration State.

3. To place the chip into the Configuration State the Config Key is sent to the chip's CONFIG PORT. Once the initiation key is received correctly the chip enters into the Configuration State (The auto Config ports are enabled).

4. The system sets the logical device information and activates desired logical devices through the chips INDEX and DATA ports.

5. The system sends other commands.

6. To exit the Configuration State the system writes 0xAA to the CONFIG PORT. The chip returns to the RUN State.

Note : Only two states are defined (Run and Configuration). In the Run State the chip will always be ready to enter the Configuration State.

APPENDIX A

FDC Core Modifications

1. FDC DMA Mode to default to Non-Burst Mode.
   a. Register xx Bit x is default to a x at powerup.

2. FDC Core command to handle Density Select function. Implement to simplify support of 3-Mode drives for users/customers.

DRIVE RATE TABLE		DATA RATE		DATA RATE		DENSEL (1)	DRATE (1)	
DRT1	**DRT0**	**SEL 1**	**SEL 0**	**MFM**	**FM**		**1**	**0**
0	0	1	1	1Meg	---	1	1	1
0	0	0	0	500	250	1	0	0
0	0	0	1	300	150	0	0	1
0	0	1	0	250	125	0	1	0
0	1	1	1	1Meg	---	1	1	1
0	1	0	0	500	250	1	0	0
0	1	0	1	500	250	0	0	1
0	1	1	0	250	125	0	1	0
1	0	1	1	1Meg	---	1	1	1
1	0	0	0	500	250	1	0	0
1	0	0	1	2Meg	---	0	0	1
1	0	1	0	250	125	0	1	0

Drive Rate Table (Recommended)
00 = Regular drives and 2.88 vertical format
01 = 3-mode drive
10 = 2 meg tape

(1) DENSEL, DRATE1 and DRATE0 map onto output pins DRVDEN0 and DRVDEN1

DT0	DT1	DRVDEN0 (1)	DRVDEN1 (1)	DRIVE TYPE
0	0	DENSEL	DRATE0	4/2/1 MB 3.5" 2/1 MB 5.25" FDDS 2/1.6/1 MB 3.5" (3-MODE)
0	1	DRATE1	DRATE0	
1	0	nDENSEL	DRATE0	
1	1	DRATE0	DRATE1	

There are two of the following registers in the configuration data space, one for each drive.
FDD0 - 0xF4
FDD1 - 0xF5

D7	D6	D5	D4	D3	D2	D1	D0
0	PTS	0	DRT1	DRT0	0	DT0	DT1

PTS = 0 Use Precompensation
= 1 No Precompensation

DTx = Drive Type select

DRTx = Data Rate Table select

(1) DENSEL, DRATE1 and DRATE0 map onto three output pins DRVDEN0 and DRVDEN1.

IDE Controller Modifications

FDC/HDC split register eliminated. Typical system design implementations put the FDC registers at I/O Base address 0x3f0 and the IDE Misc AT registers at I/O Base address 0x3f6. Looking at the registers used by the FDC and the IDE shows an overlap at I/O address 0x3f6 and 0x3f7. System I/O accesses to 0x3f6 result in no contention as 0x3f6 is undefined for the FDC. Sytem I/O writes to 0x3f7 result in no contention as the IDE interface does not perform writes to this register. The only contention would normally occur when the system issues I/O reads to 0x3f7. THE FDC37C667, HOWEVER, WILL NOT DECODE IDE ACCESS TO 0x3f7 (see section 3b, Logical Device I/O Map for IDE devices). The FDC, when configured for the AT mode, drives bit D7 only. When configured for PS/2 or Model 30 mode the FDC will drive the entire byte.

Logical Device IRQ and DMA Operation

1. IRQ and DMA Enable and Disable: Any time the IRQ or DACK for a logical block is disabled by a register bit in that logical block, the IRQ and/or DACK must be disabled. This is in addition to the IRQ and DACK disabled by the Configuration Registers (active bit or address not valid).

    a. FDC: For the following cases, the IRQ and DACK used by the FDC are disabled (high impedance). Will not respond to the DREQ
        i. Digital Output Register (Base+2) bit D3 (DMAEN) set to "0".
        ii. The FDC is in power down (disabled).

    b. IDE1 and IDE2: No additional conditions.

    c. Serial Port1 and 2:
        i. Modem Control Register (MCR) Bit D2 (OUT2) - When OUT2 is a logic "0", the serial port interrupt is forced to a high impedance state - disabled.

    d. Parallel Port:
        i. SPP and EPP modes: Control Port (Base+2) bit D4 (IRQE) set to "0", IRQ is disabled (high impedance).
        ii. ECP Mode:
            (1) (DMA) dmaEn from ecr register. See table.
            (2) IRQ - See table.

MODE (FROM ECR REGISTER)		IRQ PIN CONTROLLED BY	PDREQ PIN CONTROLLED BY
000	PRINTER	IRQE	dmaEn
001	SPP	IRQE	dmaEn
010	FIFO	(on)	dmaEn
011	ECP	(on)	dmaEn
100	EPP	IRQE	dmaEn
101	RES	IRQE	dmaEn
110	TEST	(on)	dmaEn
111	CONFIG	IRQE	dmaEn

    e. Game Port and ADDR: No IRQ or DACK used.

    f. Real Time Clock (RTC):
        i. (refer to the RTC section of this data sheet.)

    g. Keyboard Controller (KYBD):

i. (refer to the KYBD controller section of this spec.)

2. The ECP Parallel port Config Reg B reflects the IRQ and DRQ selected by the Configuration Registers.

Table "A"

IRQ SELECTED	CONFIG REG B BITS 5:3
15	110
14	101
11	100
10	011
9	010
7	001
5	111
All Others	000

Table "B"

DMA SELECTED	CONFIG REG B BITS 2:0
3	011
2	010
1	001
All Others	000

OPERATIONAL DESCRIPTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range..... 0^{o}C to $+70^{o}$C
Storage Temperature Range.....-55^{o} to $+150^{o}$C
Lead Temperature Range (soldering, 10 seconds) ..... $+325^{o}$C
Positive Voltage on any pin, with respect to Ground.....V_{cc}+0.3V
Negative Voltage on any pin, with respect to Ground..... -0.3V
Maximum V_{cc}..... +7V

*Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS

(T_A = 0°C - 70°C, V_{cc} = +5 V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}	2.2			V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		250		mV	
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.4	V	
High Input Level	V_{IHCK}	3.0			V	
ICLK2 Input Buffer						
Input Level			500		*mV*	*V P - P*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Input Leakage (All I and IS buffers)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = V_{CC}
V_{BAT}		2.4	3.0	4.0	V	
I_{BAT} Standby Current Input Leakage			1.0 100	2.0	µA nA	V_{CC}=V_{SS}=0 V_{CC}=5V, V_{BAT}=3V
O4 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 4 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -2 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 1)
O8SR Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -8 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 1)
Rise Time	T_{RT}	5			ns	
Fall Time	T_{FL}	5			ns	
O24 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 24 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -12 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O16SR Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 16 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -16 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 1)
Rise Time	T_{RT}	5			ns	
Fall Time	T_{FL}	5			ns	
OD16P Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 16 mA I_{OH} = 90 µA
Output Leakage	I_{OL}	-10		+10	µA	(Note 2) V_{IN} = 0 to V_{CC} (Note 1)
OD24 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 24 mA
Output Leakage	I_{OL}			+10	µA	V_{IN} = 0 to V_{CC} (Note 1)
OD48 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 48 mA
Output Leakage	I_{OL}			+10	µA	V_{IN} = 0 to V_{CC} (Note 1)
OP24 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 24 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -12 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
OCLK2 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 2 mA
High Output Level	V_{OH}	3.5			V	I_{OH} = -2 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 1)
ChiProtect (SLCT, PE, BUSY, nACK, nERROR)	I_{IL}			± 10	µA	V_{CC} = 0V V_{IN} = 6V Max
Backdrive (nSTROBE, nAUTOFD, nINIT, nSLCTIN)	I_{IL}			± 10	µA	V_{CC} = 0V V_{IN} = 6V Max
Backdrive (PD0-PD7)	I_{IL}			± 10	µA	V_{CC} = 0V V_{IN} = 6V Max
Suppy Current Active	I_{CCI}	*4.5*	*70*	*90*	mA	All outputs open

Note 1: All output leakages are measured with the current pins in high impedance. Output leakage is measured with the low driving output off, either for a high level output or a high impedance state.

Note 2: KBCLK, KBDATA, MCLK, MDATA contain 90µA min pull-ups.

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{CC} = 5V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

TIMING DIAGRAMS

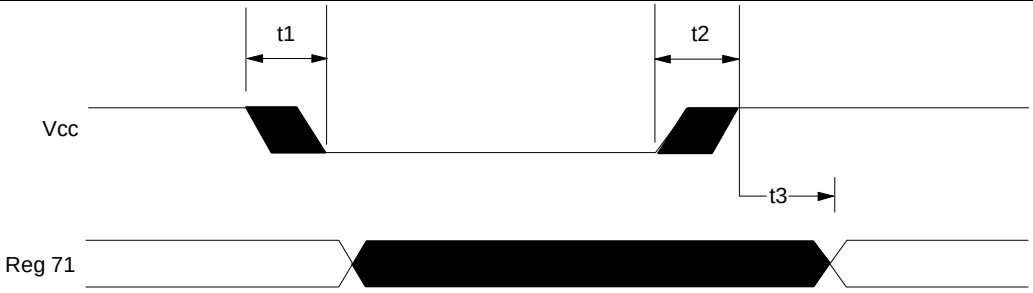


FIGURE 3 - POWER-UP TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Vcc Slew from 4.5V to 0V	300			µs
t2	Vcc Slew from 0V to 4.5V	100			µs
t3	Reg 71 after powerup (Note 1)	125		250	µs

Note 1: Internal write-protection period after Vcc passes 4.5 volts on power-up

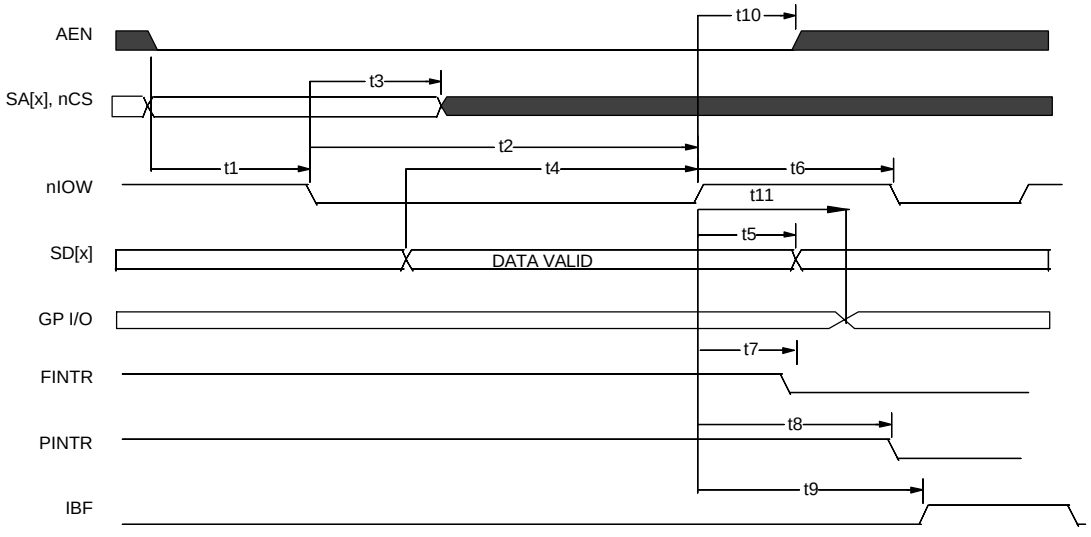


FIGURE 4 - ISA WRITE

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	SA[x], nCS and AEN valid to nIOW asserted	10			ns
t2	nIOW asserted to nIOW deasserted	80			ns
t3	nIOW asserted to SA[x], nCS invalid	10			ns
t4	SD[x] Valid to nIOW deasserted	45			ns
t5	SD[x] Hold from nIOW deasserted			0	ns
t6	nIOW deasserted to nIOW asserted	25			ns
t7	nIOW deasserted to FINTR deasserted (Note 1)			55	ns
t8	nIOW deasserted to PINTER deasserted (Note 2)			260	ns
t9	IBF (internal signal) asserted from nIOW deasserted			40	ns
t10	nIOW deasserted to AEN invalid	10			ns
t11	nIOW deasserted to GPI/O out Valid			100	ns

Note 1: FINTR refers to the IRQ used by the floppy disk.
Note 2: PINTR refers to the IRQ used by the parallel port

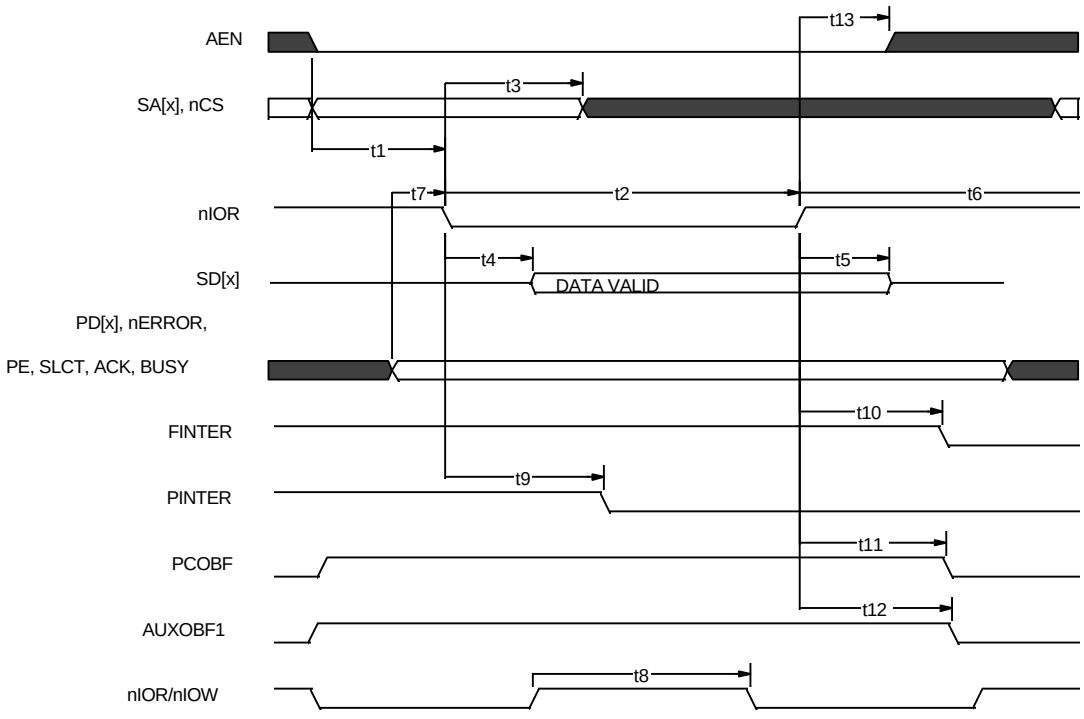


FIGURE 5A - ISA READ

SEE TIMING PARAMETERS ON PAGE 177

FIGURE 5B - ISA READ TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	SA[x], nCS and AEN valid to nIOR asserted	10			ns
t2	nIOR asserted to nIOR deasserted	50			ns
t3	nIOR asserted to SA[x], nCS invalid	10			ns
t4	nIOR asserted to Data Valid			50	ns
t5	Data Hold/float from nIOR deasserted	10		25	ns
t6	nIOR deasserted	25			ns
t8	nIOR asserted after nIOW deasserted	80			ns
t8	nIOR/nIOR, nIOW/nIOW transfers from/to ECP FIFO	150			ns
t7	Parallel Port setup to nIOR asserted			20	ns
t9	nIOR asserted to PINTER deasserted			55	ns
t10	nIOR deasserted to FINTER deasserted			260	ns
t11	nIOR deasserted to PCOBF deasserted (Notes 3,5)			80	ns
t12	nIOR deasserted to AUXOBF1 deasserted (Notes 4,5)			80	ns
t13	nIOW deasserted to AEN invalid	10			ns

Note 1: FINTR refers to the IRQ used by the floppy disk.
Note 2: PINTR refers to the IRQ used by the parallel port.
Note 3: PCOBF is used for the Keyboard IRQ.
Note 4: AUXOBF1 is used for the Mouse IRQ.
Note 5: Applies only if deassertion is performed in hardware.

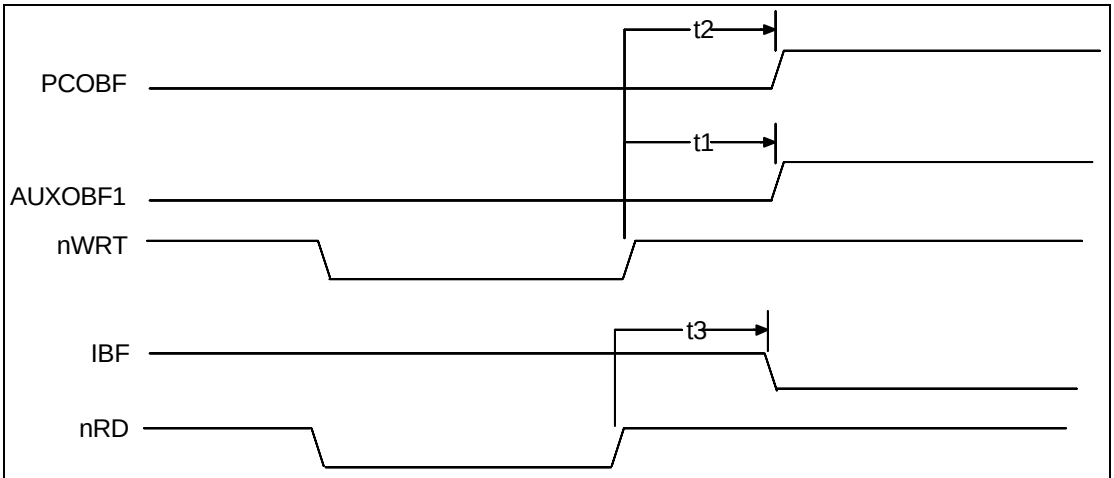


FIGURE 6 - INTERNAL 8042 CPU TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nWRT deasserted to AUXOBF1 asserted (Notes 1,2)			40	ns
t2	nWRT deasserted to PCOBF asserted (Notes 1,3)			40	ns
t3	nRD deasserted to IBF deasserted (Note 1)			40	ns

Note 1: IBF, nWRT and nRD are internal signals.
Note 2: PCOBF is used for the Keyboard IRQ.
Note 3: AUXOBF1 is used for the Mouse IRQ.

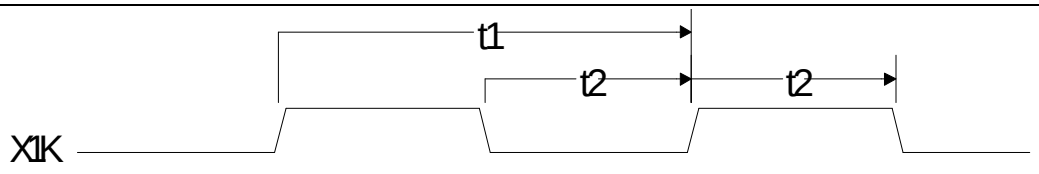


FIGURE 7A - INPUT CLOCK TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Clock Cycle Time for 14.318MHZ			65	ns
t2	Clock High Time/Low Time for 14.318MHz	25			ns
t1	Clock Cycle Time for 32KHZ				
t2	Clock High Time/Low Time for 32KHz				
	Clock Rise Time/Fall Time (not shown)			5	ns

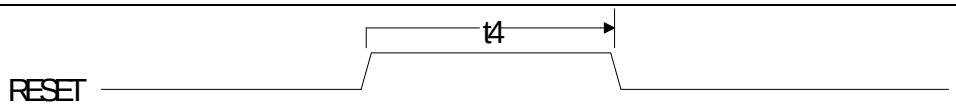


FIGURE 7B - RESET TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t4	nRESET Low Time (Note 1)	1.5			µs

Note 1: The nRESET low time is dependent upon the processor clock. The nRESET must be active for a minimum of 24 x16MHz clock cycles.

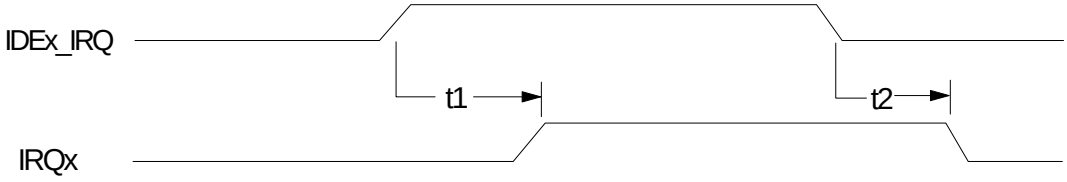


FIGURE 8 - IRQ TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	IDE_IRQ low-high edge to IRQ low-high edge propagation delay. Edge High type interrupt selected.			30	ns
t2	IDE_IRQ high-low edge to IRQ high-low edge propagation delay. Edge high type interrupt selected.			30	ns

Note: IDE IRQ input and pass-through IRQ timing

Definitions: IDE_ IRQ is the Interrupt request input from an IDE Hard Drive which is defined as a low to high edge type interrupt held high until the interrupt is serviced.

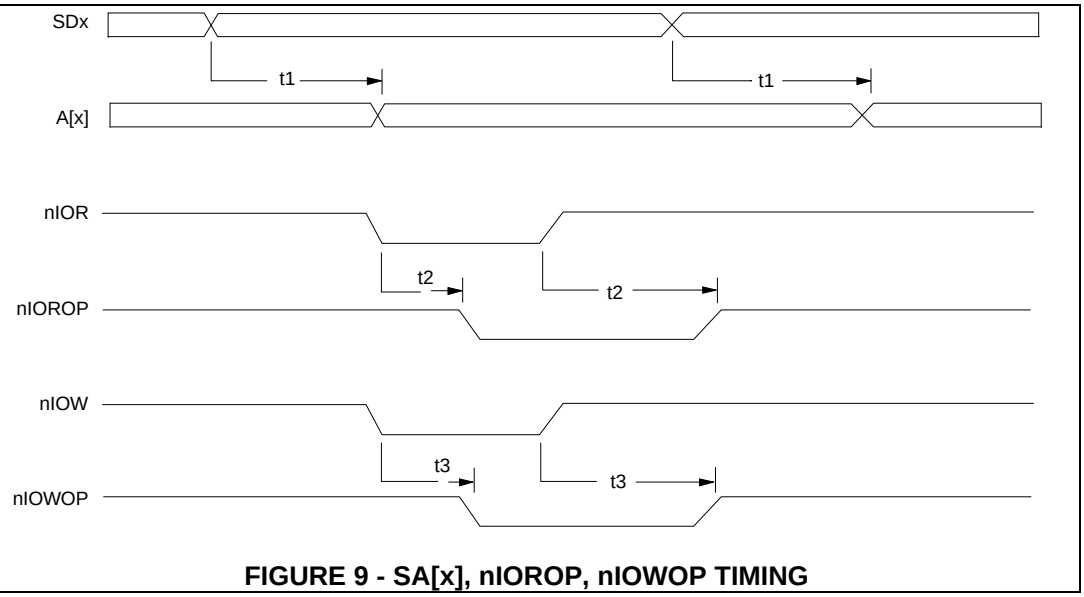


FIGURE 9 - SA[x], nIOROP, nIOWOP TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	SD[x] in to A[x] output			25	ns
t2	nIOR in to nIOROP output			25	ns
t3	nIOW in to nIOWOP output			25	ns

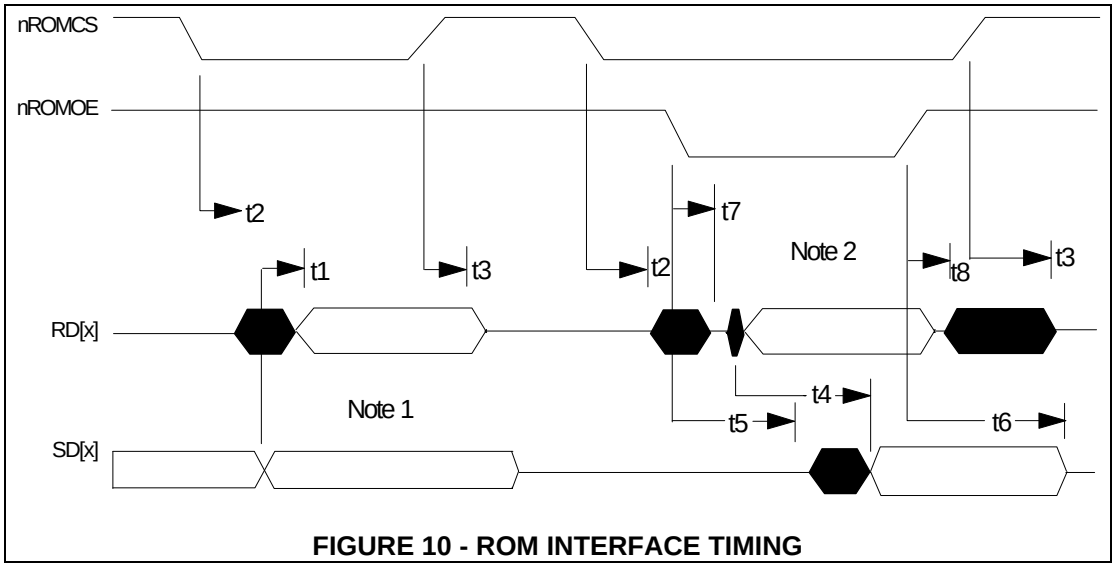


FIGURE 10 - ROM INTERFACE TIMING

Note 1: RD[x] driven by FDC37C93x, SD[x] driven by system
Note 2: RD[x] driven by ROM, SD[x] driven by FDC37C9x

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	SD[x] valid to RD[x] valid			25	ns
t2	nROMCS active to RD[X] driven			25	ns
t3	nROMCS inactive to RD[X] float			25	ns
t4	RD[x] valid to SD[x] valid			25	ns
t5	nROMCS active to SD[X] driven			25	ns
t6	nROMCS inactive to SD[X] float			25	ns
t7	nROMOE active to RD[x] float			25	ns
t8	nROMOE inactive to RD[x] driven			25	ns

Note 1: Outputs have a 50 pf load.

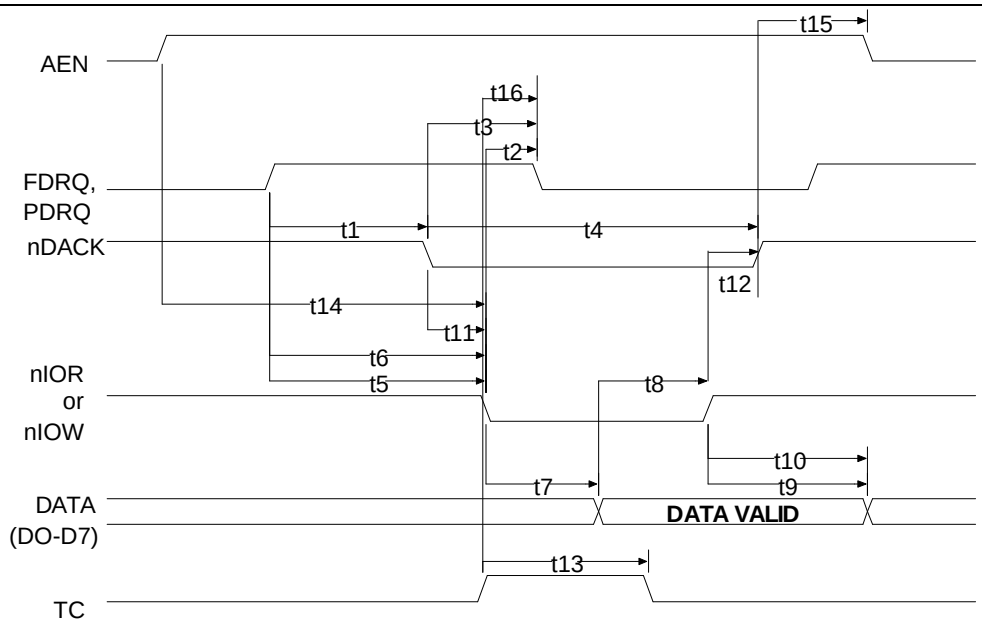


FIGURE 11 - DMA TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nDACK Delay Time from FDRQ High	0			ns
t2	DRQ Reset Delay from nIOR or nIOW			100	ns
t3	FDRQ Reset Delay from nDACK Low			100	ns
t4	nDACK Width	150			ns
t5	nIOR Delay from FDRQ High	0			ns
t6	nIOW Delay from FDRQ High	0			ns
t7	Data Access Time from nIOR Low			100	ns
t8	Data Set Up Time to nIOW High	40			ns
t9	Data to Float Delay from nIOR High	10		60	ns
t10	Data Hold Time from nIOW High	10			ns
t11	nDACK Set Up to nIOW/nIOR Low	5			ns
t12	nDACK Hold after nIOW/nIOR High	10			ns
t13	TC Pulse Width	60			ns
t14	AEN Set Up to nIOR/nIOW	40			ns
t15	AEN Hold from nDACK	10			ns
t16	TC Active to PDRQ Inactive			100	ns

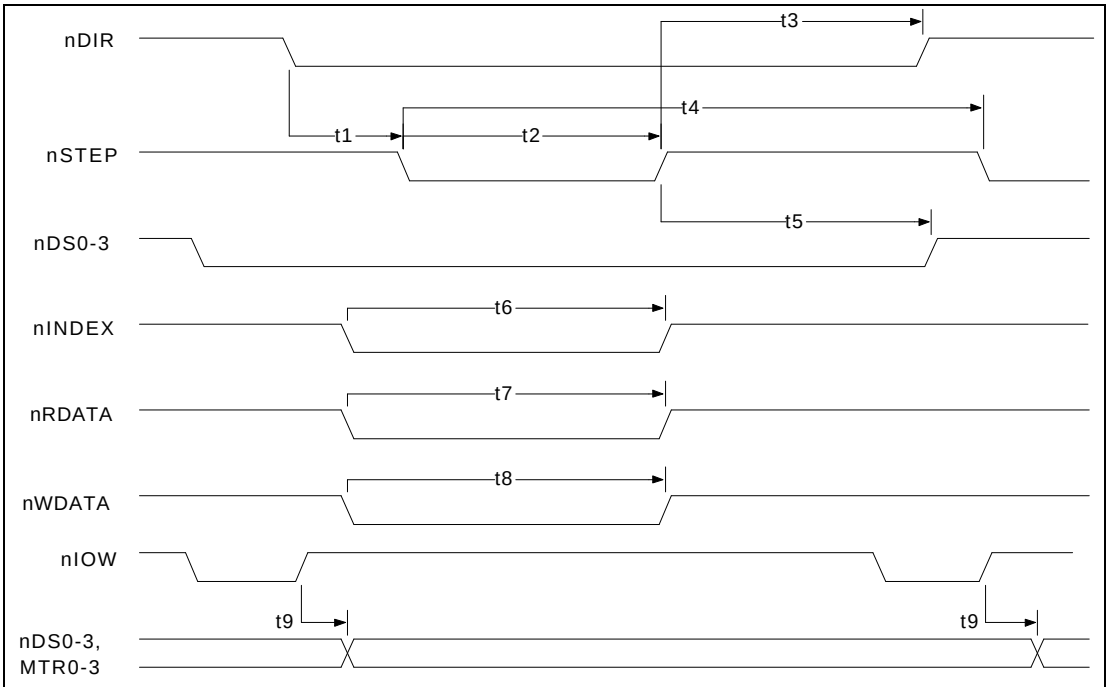


FIGURE 12 - DISK DRIVE TIMING (AT MODE ONLY)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nDIR Set Up to STEP Low		4		X*
t2	nSTEP Active Time Low		24		X*
t3	nDIR Hold Time after nSTEP		96		X*
t4	nSTEP Cycle Time		132		X*
t5	nDS0-3 Hold Time from nSTEP Low		20		X*
t6	nINDEX Pulse Width		2		X*
t7	nRDATA Active Time Low		40		ns
t8	nWDATA Write Data Width Low		.5		Y*
t9	nDS0-3, MTRO-3 from End of nIOW		25		ns

*X specifies one MCLK period and Y specifies one WCLK period.
MCLK = Controller Clock to FDC
WCLK = 2 x Data Rate

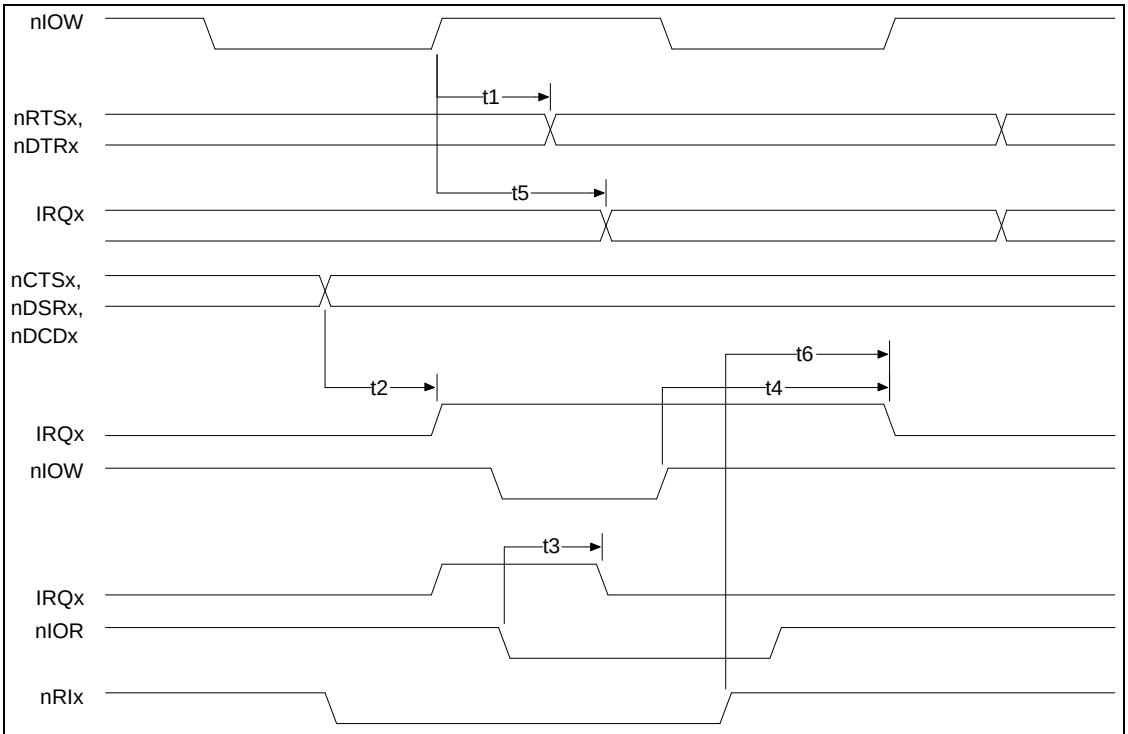


FIGURE 13 - SERIAL PORT TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nRTSx, nDTRx Delay from nIOW			200	ns
t2	IRQx Active Delay from nCTSx, nDSRx, nDCDx			100	ns
t3	IRQx Inactive Delay from nIOR (Leading Edge)			120	ns
t4	IRQx Inactive Delay from nIOW (Trailing Edge)			125	ns
t5	IRQx Inactive Delay from nIOW	10		100	ns
t6	IRQx Active Delay from nRIx			100	ns

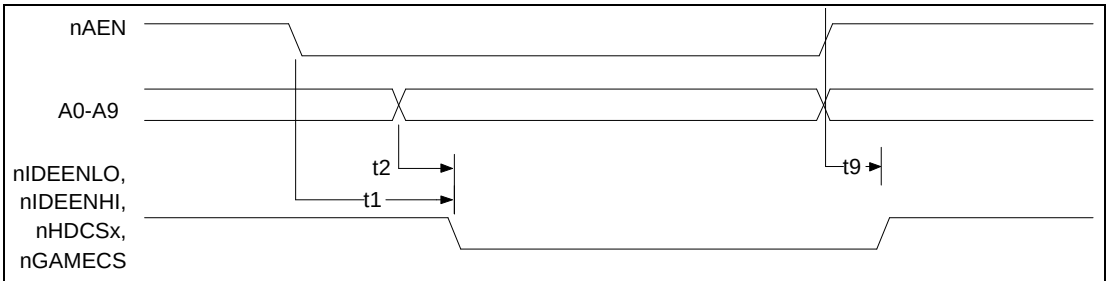


FIGURE 14 - IDE INTERFACE TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nIDEENLO, nIDEENHI, nGAMECS, nHDCSx Delay from nAEN			40	ns
t2	nIDEENLO, nIDEENHI, nGAMECS, nHDCSx Delay from A0 - A9			40	ns
t9	nIDEENLO Delay from nIDEENHI, AEN			40	ns

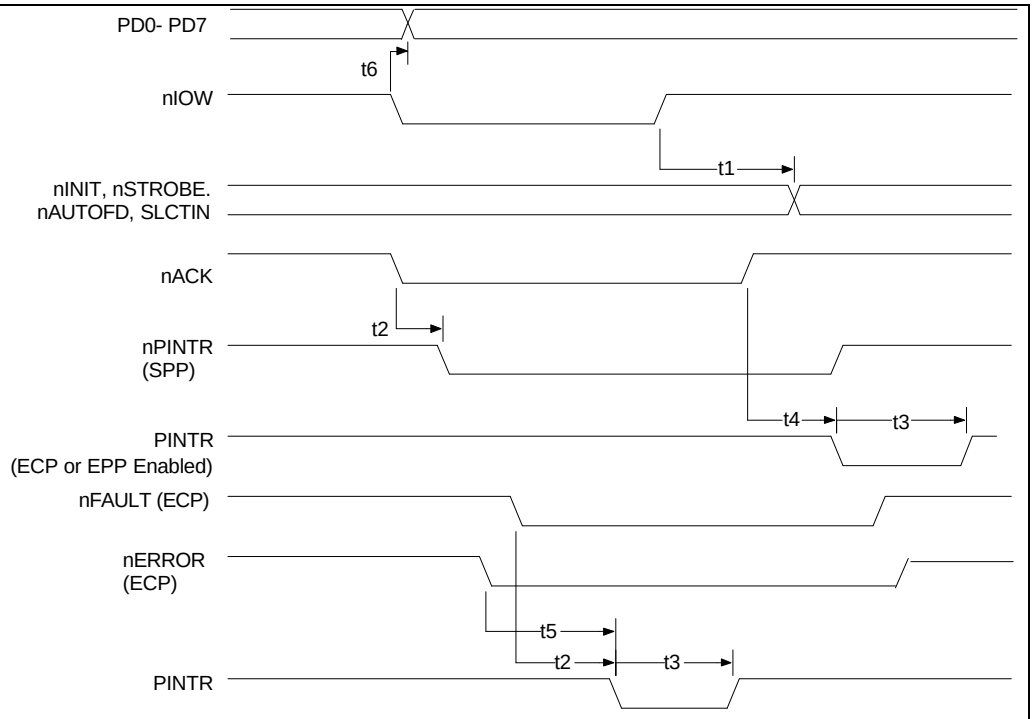


FIGURE 15 - PARALLEL PORT TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PD0-7, nINIT, nSTROBE, nAUTOFD Delay from nIOW			100	ns
t2	PINTR Delay from nACK, nFAULT			60	ns
t3	PINTR Active Low in ECP and EPP Modes	200		300	ns
t4	PINTR Delay from nACK			105	ns
t5	nERROR Active to PINTR Active			105	ns
t6	PD0 - PD7 Delay from IOW Active			100	ns

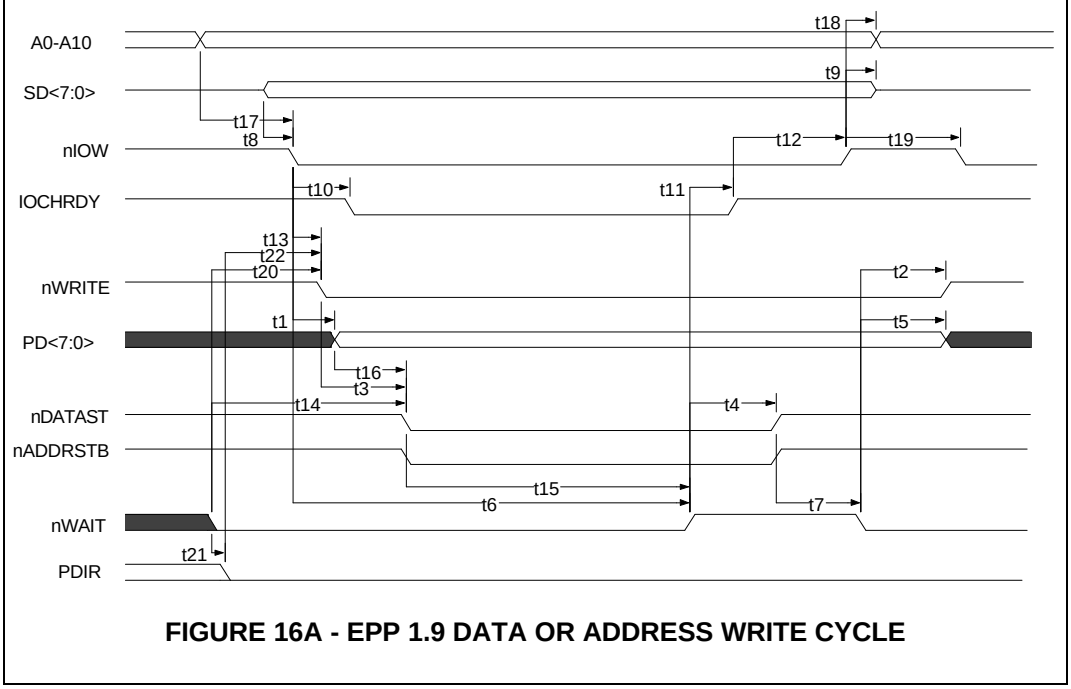


FIGURE 16A - EPP 1.9 DATA OR ADDRESS WRITE CYCLE

SEE TIMING PARAMETERS ON PAGE 189

FIGURE 16B - EPP 1.9 DATA OR ADDRESS WRITE CYCLE TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nIOW Asserted to PDATA Valid	0		50	ns
t2	nWAIT Asserted to nWRITE Change (Note 1)	60		185	ns
t3	nWRITE to Command Asserted	5		35	ns
t4	nWAIT Deasserted to Command Deasserted (Note 1)	60		190	ns
t5	nWAIT Asserted to PDATA Invalid (Note 1)	0			ns
t6	Time Out	10		12	µs
t7	Command Deasserted to nWAIT Asserted	0			ns
t8	SDATA Valid to nIOW Asserted	10			ns
t9	nIOW Deasserted to DATA Invalid	0			ns
t10	nIOW Asserted to IOCHRDY Asserted	0		24	ns
t11	nWAIT Deasserted to IOCHRDY Deasserted (Note 1)	60		160	ns
t12	IOCHRDY Deasserted to nIOW Deasserted	10			ns
t13	nIOW Asserted to nWRITE Asserted	0		70	ns
t14	nWAIT Asserted to Command Asserted (Note 1)	60		210	ns
t15	Command Asserted to nWAIT Deasserted	0		10	µs
t16	PDATA Valid to Command Asserted	10			ns
t17	Ax Valid to nIOW Asserted	40			ns
t18	nIOW Asserted to Ax Invalid	10			ns
t19	nIOW Deasserted to nIOW or nIOR Asserted	40			ns
t20	nWAIT Asserted to nWRITE Asserted (Note 1)	60		185	ns
t21	nWAIT Asserted to PDIR Low	0			ns
t22	PDIR Low to nWRITE Asserted	0			ns

Note 1: nWAIT must be filtered to compensate for ringing on the parallel bus cable. WAIT is considered to have settled after it does not transition for a minimum of 50 nsec.

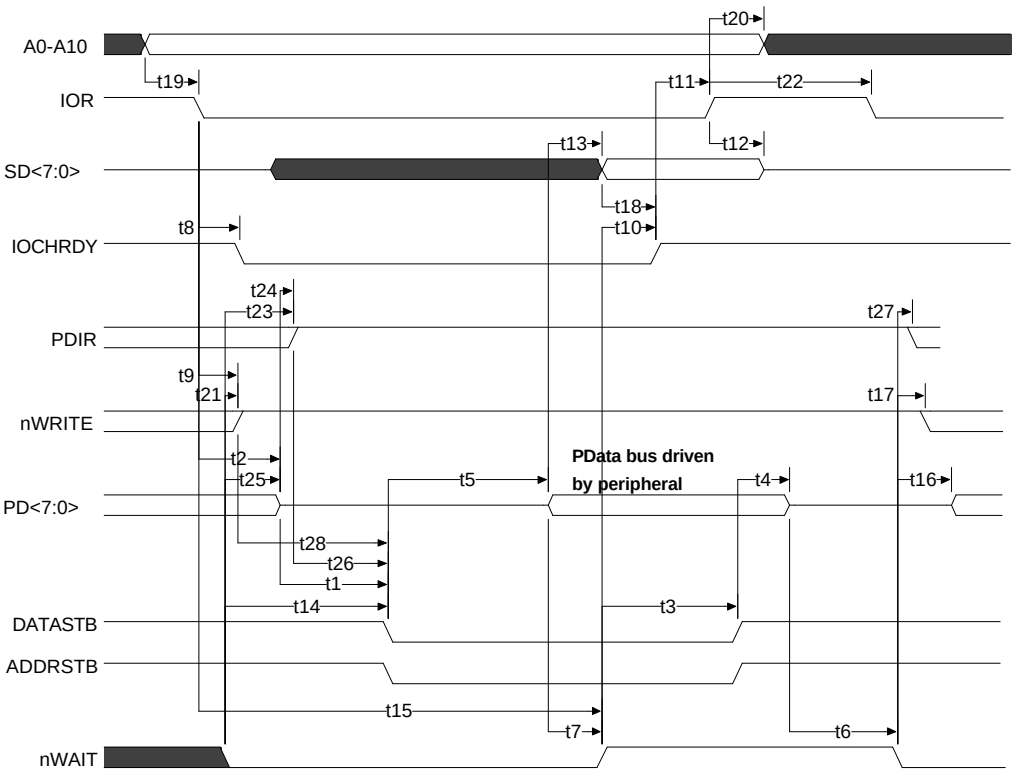


FIGURE 17A - EPP 1.9 DATA OR ADDRESS READ CYCLE

SEE TIMING PARAMETERS ON PAGE 191

FIGURE 17B - EPP 1.9 DATA OR ADDRESS READ CYCLE TIMING PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PDATA Hi-Z to Command Asserted	0		30	ns
t2	nIOR Asserted to PDATA Hi-Z	0		50	ns
t3	nWAIT Deasserted to Command Deasserted (Note 1)	60		180	ns
t4	Command Deasserted to PDATA Hi-Z	0			ns
t5	Command Asserted to PDATA Valid	0			ns
t6	PDATA Hi-Z to nWAIT Deasserted	0			µs
t7	PDATA Valid to nWAIT Deasserted	0			ns
t8	nIOR Asserted to IOCHRDY Asserted	0		24	ns
t9	nWRITE Deasserted to nIOR Asserted (Note 2)	0			ns
t10	nWAIT Deasserted to IOCHRDY Deasserted (Note 1)	60		160	ns
t11	IOCHRDY Deasserted to nIOR Deasserted	0			ns
t12	nIOR Deasserted to SDATA Hi-Z (Hold Time)	0		40	ns
t13	PDATA Valid to SDATA Valid	0		75	ns
t14	nWAIT Asserted to Command Asserted	0		195	ns
t15	Time Out	10		12	µs
t16	nWAIT Deasserted to PDATA Driven (Note 1)	60		190	ns
t17	nWAIT Deasserted to nWRITE Modified (Notes 1,2)	60		190	ns
t18	SDATA Valid to IOCHRDY Deasserted (Note 3)	0		85	ns
t19	Ax Valid to nIOR Asserted	40			ns
t20	nIOR Deasserted to Ax Invalid	10		10	ns
t21	nWAIT Asserted to nWRITE Deasserted	0		185	ns
t22	nIOR Deasserted to nIOW or nIOR Asserted	40			ns
t23	nWAIT Asserted to PDIR Set (Note 1)	60		185	ns
t24	PDATA Hi-Z to PDIR Set	0			ns
t25	nWAIT Asserted to PDATA Hi-Z (Note 1)	60		180	ns
t26	PDIR Set to Command	0		20	ns
t27	nWAIT Deasserted to PDIR Low (Note 1)	60		180	ns
t28	nWRITE Deasserted to Command	1			ns

Note 1: nWAIT is considered to have settled after it does not transition for a minimum of 50 ns.
Note 2: When not executing a write cycle, EPP nWRITE is inactive high.
Note 3: 85 is true only if t7 = 0.

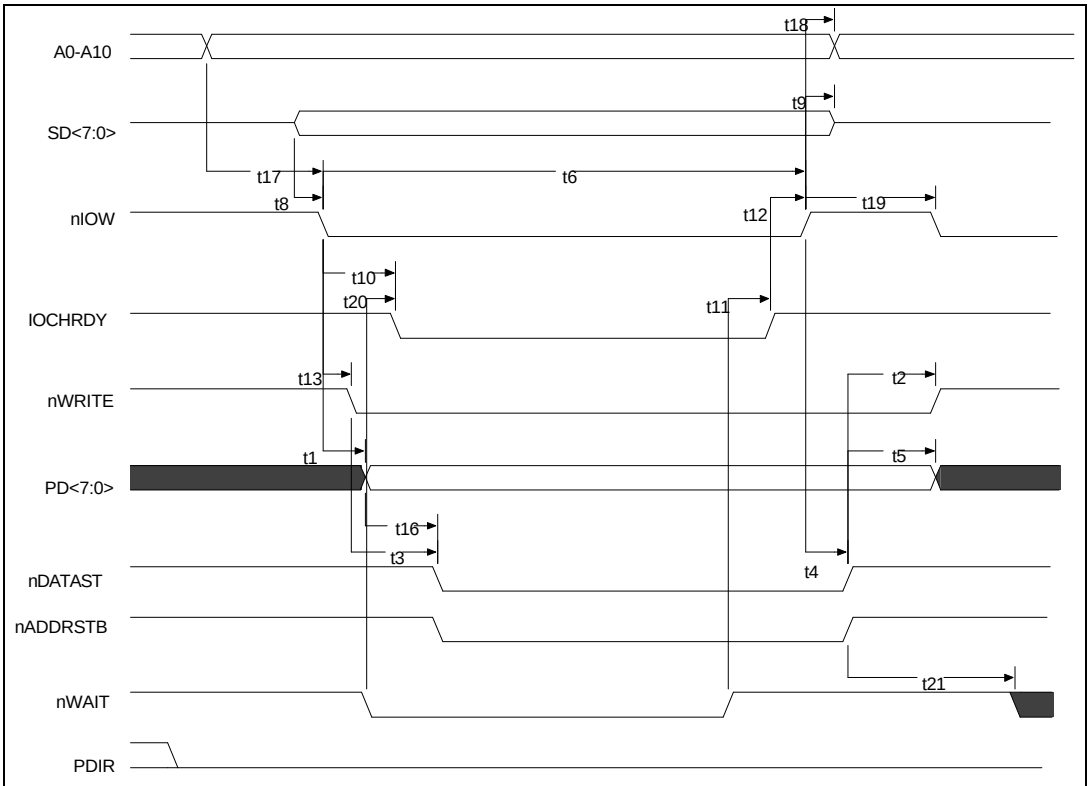


FIGURE 18A - EPP 1.7 DATA OR ADDRESS WRITE CYCLE

SEE TIMING PARAMETERS ON PAGE 193

FIGURE 18B - EPP 1.7 DATA OR ADDRESS WRITE CYCLE PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nIOW Asserted to PDATA Valid	0		50	ns
t2	Command Deasserted to nWRITE Change	0		40	ns
t3	nWRITE to Command	5		35	ns
t4	nIOW Deasserted to Command Deasserted (Note 2)			50	ns
t5	Command Deasserted to PDATA Invalid	50			ns
t6	Time Out	10		12	µs
t8	SDATA Valid to nIOW Asserted	10			ns
t9	nIOW Deasserted to DATA Invalid	0			ns
t10	nIOW Asserted to IOCHRDY Asserted	0		24	ns
t11	nWAIT Deasserted to IOCHRDY Deasserted			40	ns
t12	IOCHRDY Deasserted to nIOW Deasserted	10			ns
t13	nIOW Asserted to nWRITE Asserted	0		50	ns
t16	PDATA Valid to Command Asserted	10		35	ns
t17	Ax Valid to nIOW Asserted	40			ns
t18	nIOW Deasserted to Ax Invalid	10			µs
t19	nIOW Deasserted to nIOW or nIOR Asserted	100			ns
t20	nWAIT Asserted to IOCHRDY Deasserted			45	ns
t21	Command Deasserted to nWAIT Deasserted	0			ns

Note 1: nWRITE is controlled by clearing the PDIR bit to "0" in the control register before performing an EPP Write.
Note 2: The number is only valid if nWAIT is active when IOW goes active.

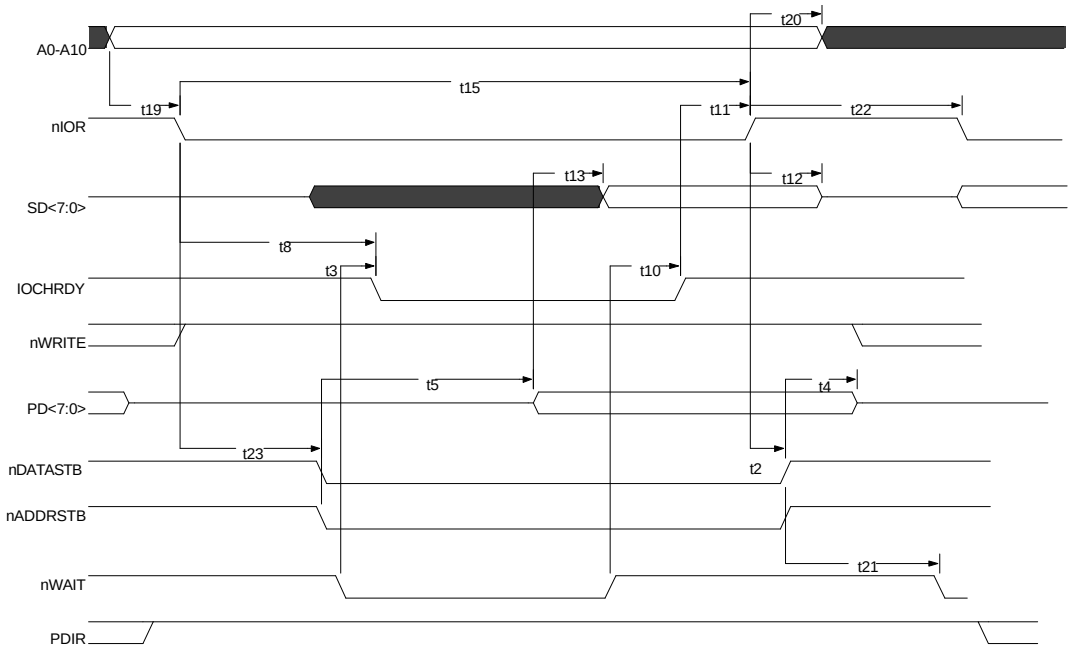


FIGURE 19A - EPP 1.7 DATA OR ADDRESS READ CYCLE

SEE TIMING PARAMETERS ON PAGE 195

FIGURE 19B - EPP 1.7 DATA OR ADDRESS READ CYCLE PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t2	nIOR Deasserted to Command Deasserted			50	ns
t3	nWAIT Asserted to IOCHRDY Deasserted	0		40	ns
t4	Command Deasserted to PDATA Hi-Z	0			ns
t5	Command Asserted to PDATA Valid	0			ns
t8	nIOR Asserted to IOCHRDY Asserted			24	ns
t10	nWAIT Deasserted to IOCHRDY Deasserted			50	ns
t11	IOCHRDY Deasserted to nIOR Deasserted	0			ns
t12	nIOR Deasserted to SDATA High-Z (Hold Time)	0		40	ns
t13	PDATA Valid to SDATA Valid			40	ns
t15	Time Out	10		12	µs
t19	Ax Valid to nIOR Asserted	40			ns
t20	nIOR Deasserted to Ax Invalid	10			ns
t21	Command Deasserted to nWAIT Deasserted	0			ns
t22	nIOR Deasserted to nIOW or nIOR Asserted	40			ns
t23	nIOR Asserted to Command Asserted			55	ns

Note: WRITE is controlled by setting the PDIR bit to "1" in the control register before performing an EPP Read.

ECP PARALLEL PORT TIMING

Parallel Port FIFO (Mode 101)

The standard parallel port is run at or near the peak 500Kbytes/sec allowed in the forward direction using DMA. The state machine does not examine and begins the next transfer based on Busy. Refer to Figure 20.

ECP Parallel Port Timing

The timing is designed to allow operation at approximately 2.0 Mbytes/sec over a 15ft cable. If a shorter cable is used then the bandwidth will increase.

Forward-Idle

When the host has no data to send it keeps HostClk () high and the peripheral will leave PeriphClk (Busy) low.

Forward Data Transfer Phase

The interface transfers data and commands from the host to the peripheral using an interlocked PeriphAck and HostClk. The peripheral may indicate its desire to send data to the host by asserting .

The Forward Data Transfer Phase may be entered from the Forward-Idle Phase. While in the Forward Phase the peripheral may asynchronously assert the () to request that the channel be reversed. When the peripheral is not busy it sets PeriphAck (Busy) low. The host then sets HostClk () low when it is prepared to send data. The data must be stable for the specified setup time prior to the falling edge of HostClk. The peripheral then sets PeriphAck (Busy) high to acknowledge the handshake. The host then sets HostClk () high. The peripheral then accepts the data and sets PeriphAck (Busy) low, completing the transfer. This sequence is shown in Figure 21.

The timing is designed to provide 3 cable round-trip times for data setup if Data is driven simultaneously with HostClk ().

Reverse-Idle Phase

The peripheral has no data to send and keeps PeriphClk high. The host is idle and keeps HostAck low.

Reverse Data Transfer Phase

The interface transfers data and commands from the peripheral to the host using an interlocked HostAck and PeriphClk.

The Reverse Data Transfer Phase may be entered from the Reverse-Idle Phase. After the previous byte has beed accepted the host sets HostAck () low. The peripheral then sets PeriphClk () low when it has data to send. The data must be stable for the specified setup time prior to the falling edge of PeriphClk. When the host is ready it to accept a byte it sets. HostAck () high to acknowledge the handshake. The peripheral then sets PeriphClk () high. After the host has accepted the data it sets HostAck () low, completing the transfer. This sequence is shown in Figure 22.

Output Drivers

To facilitate higher performance data transfer, the use of balanced CMOS active drivers for critical signals (Data, HostAck, HostClk, PeriphAck, PeriphClk) are used ECP Mode. Because the use of active drivers can present compatibility problems in Compatible Mode (the control signals, by tradition, are specified as open-collector), the drivers are dynamically changed from open-collector to totem-pole. The timing for the dynamic driver change is specified in the IEEE 1284 Extended Capabilities Port Protocol and ISA

Interface Standard, Rev. 1.09, Jan. 7, 1993, available from Microsoft. The dynamic driver change must be implemented properly to prevent glitching the outputs.

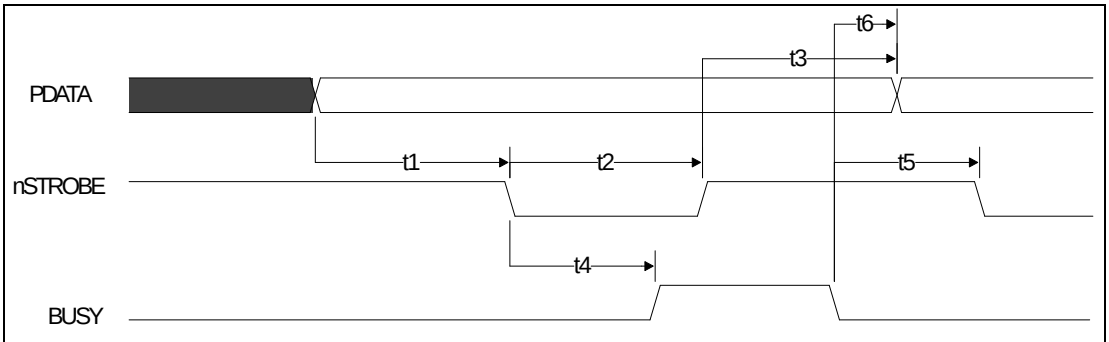


FIGURE 20 - PARALLEL PORT FIFO TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	DATA Valid to nSTROBE Active	600			ns
t2	nSTROBE Active Pulse Width	600			ns
t3	DATA Hold from nSTROBE Inactive (Note 1)	450			ns
t4	nSTROBE Active to BUSY Active			500	ns
t5	BUSY Inactive to nSTROBE Active	680			ns
t6	BUSY Inactive to PDATA Invalid (Note 1)	80			ns

Note 1: The data is held until BUSY goes inactive or for time t3, whichever is longer. This only applies if another data transfer is pending. If no other data transfer is pending, the data is held indefinitely.

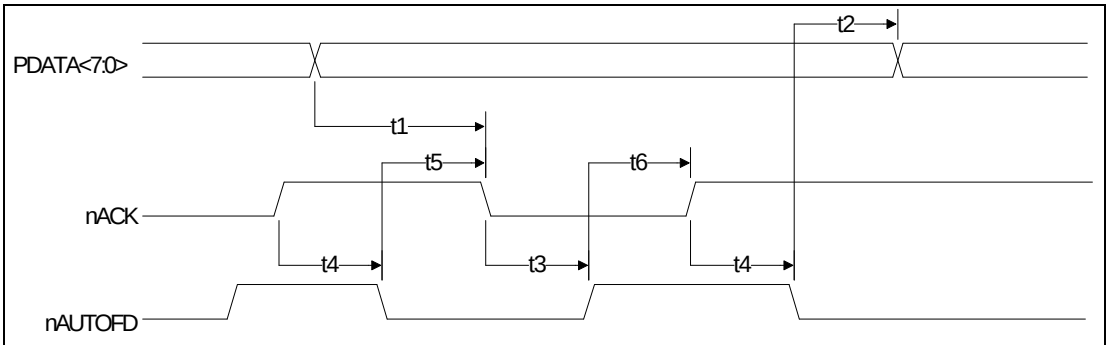


FIGURE 21 - ECP PARALLEL PORT REVERSE TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nAUTOFD Valid to nSTROBE Asserted	0		60	ns
t2	PDATA Valid to nSTROBE Asserted	0		60	ns
t3	BUSY Deasserted to nAUTOFD Changed (Notes 1,2)	80		180	ns
t4	BUSY Deasserted to PDATA Changed (Notes 1,2)	80		180	ns
t5	nSTROBE Deasserted to Busy Asserted	0			ns
t6	nSTROBE Deasserted to Busy Deasserted	0			ns
t7	BUSY Deasserted to nSTROBE Asserted (Notes 1,2)	80		200	ns
t8	BUSY Asserted to nSTROBE Deasserted (Note 2)	80		180	ns

Note 1: Maximum value only applies if there is data in the FIFO waiting to be written out.
Note 2: BUSY is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.

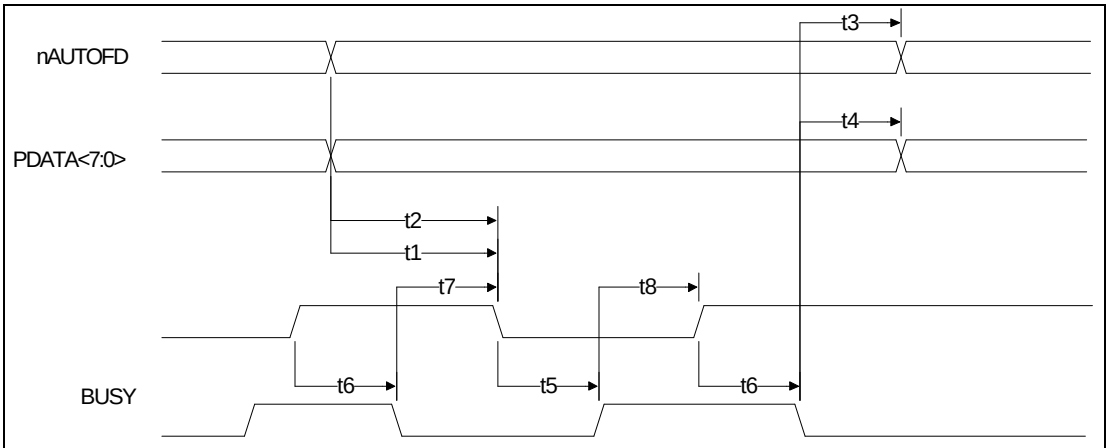
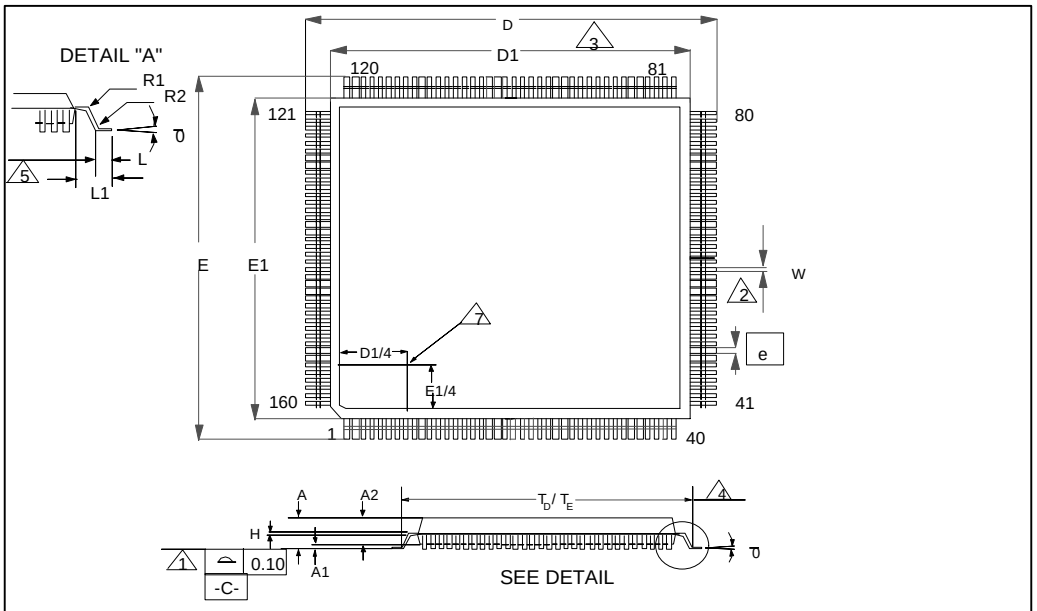


FIGURE 22 - ECP PARALLEL PORT FORWARD TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PDATA Valid to nACK Asserted	0			ns
t2	nAUTOFD Deasserted to PDATA Changed	0			ns
t3	nACK Asserted to nAUTOFD Deasserted (Notes 1,2)	80		200	ns
t4	nACK Deasserted to nAUTOFD Asserted (Note 2)	80		200	ns
t5	nAUTOFD Asserted to nACK Asserted	0			ns
t6	nAUTOFD Deasserted to nACK Deasserted	0			ns

Note 1: Maximum value only applies if there is room in the FIFO and terminal count has not been received. ECP can stall by keeping nAUTOFD low.

Note 2: nACK is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.



	MIN	NOM	MAX
A			4.07
A1	0.05		0.5
A2	3.10		3.67
D	30.95	31.20	31.45
D1	27.90	28.00	28.10
E3	30.95	31.20	31.45
E1	27.90	28.00	28.10
H	0.10		0.200
L	0.65	0.80	0.95
L1	1.60		
e	0.65BSC		
θ	0°		7°
W	0.20		0.40
R1		0.20	
R2		0.30	
T_D		30.45	
T_E		30.45	

Notes:

1) Coplanarity is 0.100 mm

2) Tolerance on the position of the leads is 0.120 mm maximum

3) Package body dimensions D1 and E1 do include the mold protrusion. Maximum mold protrusion is 0.25 mm

4) Dimensions T_D and T_E are important for testing by robotic handler

5) Dimensions for foot length L when measured the centerline of the leads are given at the table Dimension for foot length L when measured at the gauge plane 0.25 mm above the seating plane, is 0.78 - 1.03 mm

6) Controlling dimension: millimeter

7) Details of pin 1 identifier are optional but must be located within the zone indicated

FIGURE 23 - 160 PIN QFP PACKAGE OUTLINE

FDC37C93x ERRATA SHEET

PAGE	SECTION/FIGURE/ENTRY	CORRECTION	DATE REVISED
1	Real Time Clock	"typ" changed to "max"	8/14/95
1	IDE Interface	See Italicized Text	8/14/95
4	Pin Configuration	Pin #120 changed to "nROMDIR"	8/14/95
8	Bios Buffers	"nROMOE" changed to "nROMDIR"	8/14/95
10	Block Diagram	"nGPRD" changed to "nGPA", "nROMOE" changed to "nROMDIR"	8/14/95
109	Bios Buffer	"nROMOE" changed to "nROMDIR"	8/14/95
111	Table 46	"GP Read Strobe" changed to "GP Address Decoder"	8/14/95
112	Second Paragraph	See Italicized Text	8/14/95
119	General Purpose Read/Write	See Italicized Text	8/14/95
122	8042 Keyboard Controller	See Italicized Text	8/14/95
127	Port Definition and Description	See Italicized Text	8/14/95
128	RTC Interrupt	See Italicized Text	8/14/95
131	UIP/DV 2-0/RS 3-0	See Italicized Text	8/14/95
136	Power Management	First Paragraph Removed	8/14/95
142	Table 62/Bit[7]	See Italicized Text	8/14/95
144	OSC, Bits[3:2]	"when PWRGD is active. When PWRGD is inactive, OSC is off and BRG Clock is disabled (default)" was removed.	8/14/95
150	FDD Option Register, Bits[7:6]	See Italicized Text	8/14/95
151	FDD Type Register, Bits[5:4] and [7:6]	See Italicized Text	8/14/95
160	Table 74, GP20, Bit[4]	"RESET OUT (Active Low)" removed, see italicized text	8/14/95
162	Table 74	See Italicized Text	8/14/95
165	Sequence Operation	Step 2 was removed	8/14/95
167	Items 3 and 4	Removed	8/14/95

PAGE	SECTION/FIGURE/ENTRY	CORRECTION	DATE REVISED
167	"IDE Controller Modifications"	Added	8/14/95
168	"Logical Device IRQ and DMA Operation"	Added	8/14/95
173	Supply Current Active	See Italicized Text	8/14/95

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