

Features

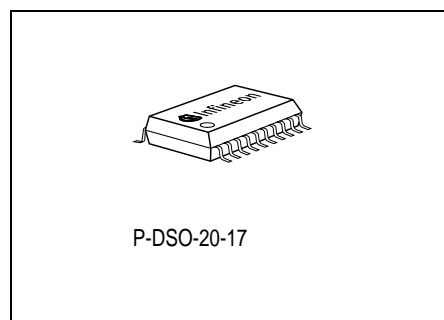
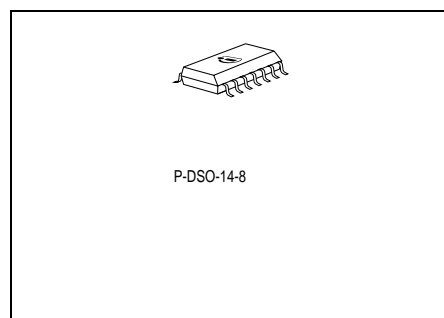
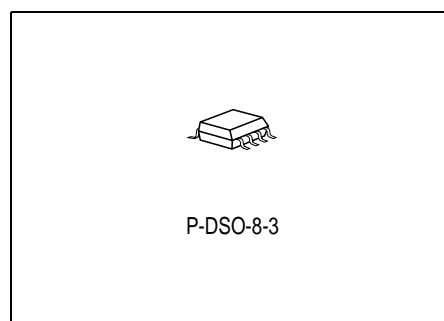
- Output voltage tolerance $\leq \pm 2\%$
- 150 mA current capability
- Very low current consumption
- Early warning
- Reset output low down to $V_Q = 1\text{ V}$
- Overtemperature protection
- Reverse polarity proof
- Adjustable reset threshold
- Very low drop voltage
- Wide temperature range
- Integrated pull up resistor at logic outputs

| Type | Ordering Code | Package |
|-------------|---------------------|-------------|
| TLE 4269 G | Q67006-A9173-A201K5 | P-DSO-8-3 |
| TLE 4269 GM | Q67006-A9288-A201K5 | P-DSO-14-8 |
| TLE 4269 GL | Q67006-A9192-C703 | P-DSO-20-17 |

■ SMD type

Functional Description

This device is an automotive suited voltage regulator with a fixed 5-V output. The maximum operating voltage is 45 V. The output is able to drive 150 mA load. It is short circuit protected and the thermal shutdown switches the output off if the junction temperature is in excess of 150 °C. A reset signal is generated for an output voltage of $V_Q < 4.65\text{ V}$. The reset threshold voltage can be decreased by external connection of a voltage divider. The reset delay time can be set by an external capacitor. Reset and sense output have integrated pull up resistors. If the integrated resistors are not desired **TLE 4279** can be used. It is also possible to supervise the input voltage by using an integrated comparator to give a low voltage warning.



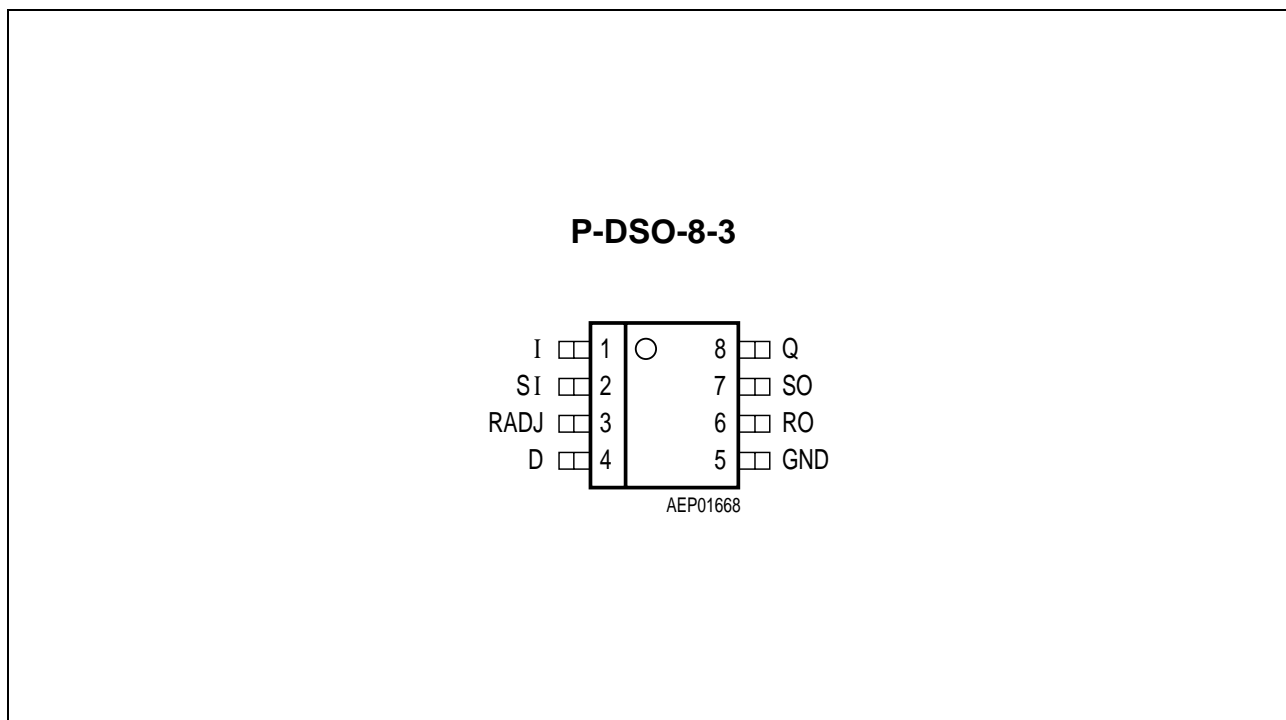


Figure 1 Pin Configuration (top view)

Pin Definitions and Functions (TLE 4269 G)

| Pin No. | Symbol | Function |
|---------|--------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | I | Input ; block to GND directly at the IC with a ceramic capacitor. |
| 2 | SI | Sense Input ; if not needed connect to Q. |
| 3 | RADJ | Reset Threshold Adjust ; if not needed connect to GND. |
| 4 | D | Reset Delay ; to select delay time, connect to GND via capacitor. |
| 5 | GND | Ground |
| 6 | RO | Reset Output ; the open-collector output is internally linked to Q via a 20 kΩ pull-up resistor. Keep open, if not needed. |
| 7 | SO | Sense Output ; the open-collector output is internally linked to the output via a 20 kΩ pull-up resistor. Keep open, if not needed. |
| 8 | Q | 5-V Output ; connect to GND with a 10 μF capacitor, ESR < 10 Ω. |

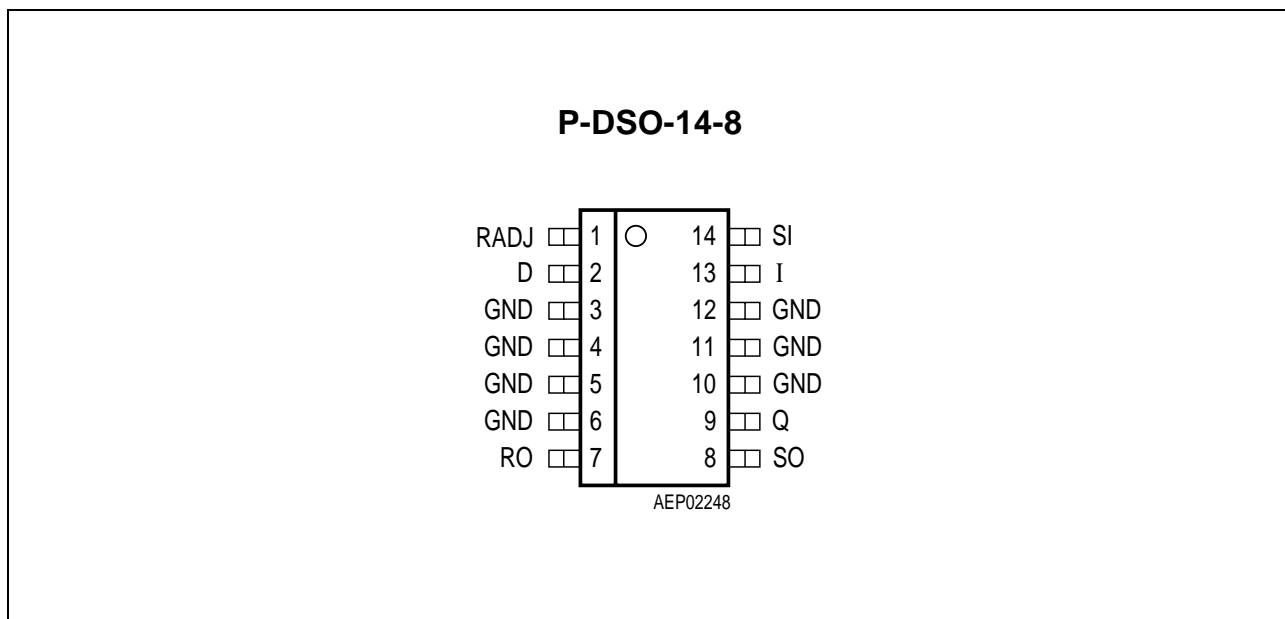


Figure 2 Pin Configuration (top view) (cont'd)

Pin Definitions and Functions (TLE 4269 GM)

| Pin No. | Symbol | Function |
|------------|--------|-----------------------------------------------------------------------------------------------------------------------------------|
| 1 | RADJ | Reset Threshold Adjust ; if not needed connect to GND. |
| 2 | D | Reset Delay ; to select delay time; connect to GND via capacitor. |
| 3, 4, 5, 6 | GND | Ground |
| 7 | RO | Reset Output ; open-collector output, internally connected to Q via a pull-up resistor of 20 kΩ. Keep open, if not needed. |
| 8 | SO | Sense Output ; open-collector output, internally connected to Q via a 20 kΩ pull-up resistor. Keep open, if not needed. |
| 9 | Q | 5-V Output ; connect to GND with a 10 μF capacitor, ESR < 10 Ω. |
| 10, 11, 12 | GND | Ground |
| 13 | I | Input ; block to GND directly at the IC with a ceramic capacitor. |
| 14 | SI | Sense Input ; if not needed connect to Q. |

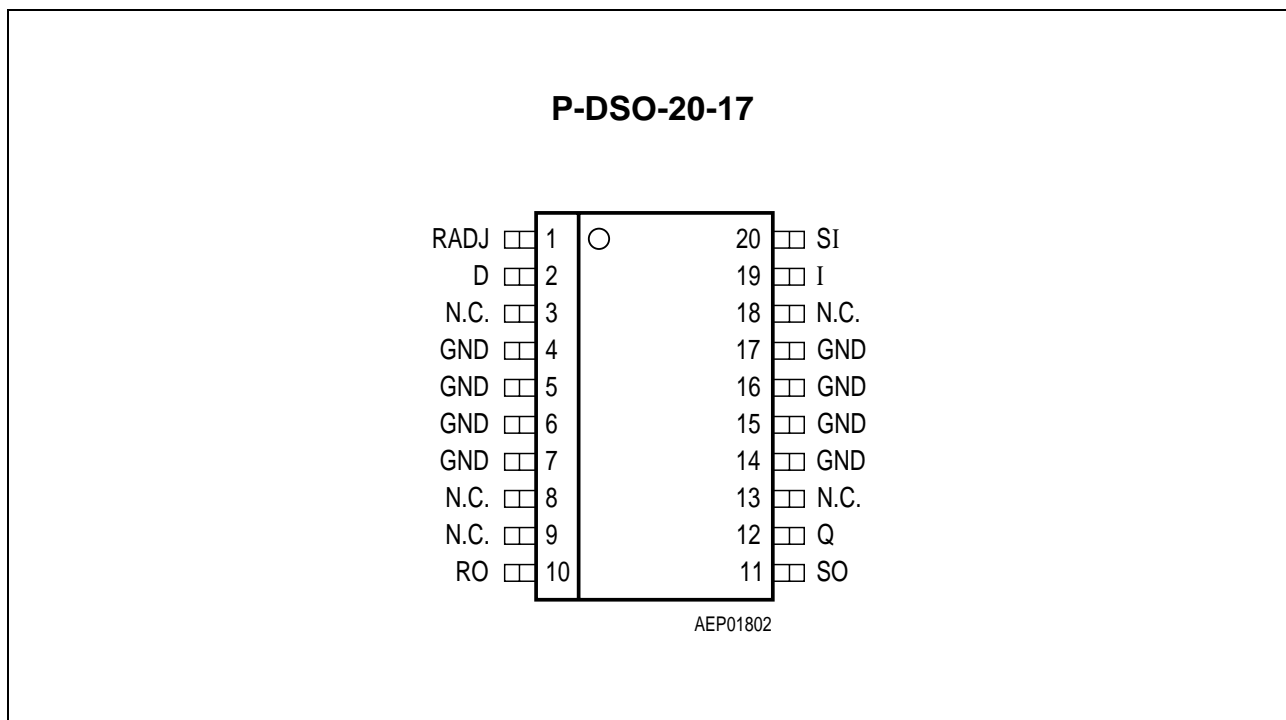


Figure 3 Pin Configuration (top view) (cont'd)

Pin Definitions and Functions (TLE 4269 GL)

| Pin No. | Symbol | Function |
|------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | RADJ | Reset Threshold Adjust ; if not needed connect to ground. |
| 2 | D | Reset Delay ; to select delay time, connect to GND via external capacitor. |
| 4-7, 14-17 | GND | Ground |
| 10 | RO | Reset Output ; the open-collector output is internally linked to Q via a 20 kΩ pull-up resistor. Keep open, if not needed. |
| 11 | SO | Sense Output ; the open-collector output is internally linked to the output via a 20 kΩ pull-up resistor. Keep open, if not needed. |
| 12 | Q | Output ; connect to GND with a 10 μF capacitor, ESR < 10 Ω. |
| 19 | I | Input ; block directly at the IC by a ceramic capacitor. |
| 20 | SI | Sense Input ; if not needed connect to Q. |

Circuit Description

The control amplifier compares a reference voltage, made highly accurate by resistance balancing, with a voltage proportional to the output voltage and drives the base of the series PNP transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element.

The reset output RO is in high-state if the voltage on the delay capacitor C_D is greater or equal V_{UD} . The delay capacitor C_D is charged with the current I_D for output voltages greater than the reset threshold V_{RT} . If the output voltage gets lower than V_{RT} ('reset condition') a fast discharge of the delay capacitor C_D sets in and as soon as V_D gets lower than V_{LD} the reset output RO is set to low-level.

The time gap for the delay capacitor discharge is the reset reaction time t_{RR} .

The reset threshold V_{RT} can be decreased via an external voltage divider connected to the pin RADJ. In this case the reset condition is reached if $V_Q < V_{RT}$ and $V_{RADJ} < V_{RAQDJ, TH}$. Dimensioning the voltage divider (see **Figure 5**) according to

$$V_{THRES} = V_{RADJ, TH} \times (R_{ADJ1} + R_{ADJ2}) / R_{ADJ2},$$

the reset threshold can be decreased down to 3.5 V. If the reset-adjust-option is not needed the RADJ-pin should be connected to GND causing the reset threshold to go to its default value (typ. 4.65 V).

A built in comparator compares the signal of the pin SI, normally fed by a voltage divider from the input voltage, with the reference and gives an early warning on the pin SO. It is also possible to superwise another voltage e.g. of a second regulator, or to build a watchdog circuit with few external components.

Application Description

The input capacitor C_1 is necessary for compensating line influences. Using a resistor of approx. 1 Ω in series with C_1 , the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor C_Q is necessary for the stability of the regulating circuit. Stability is guaranteed at values $\geq 10 \mu F$ and an ESR $\leq 10 \Omega$ within the operating temperature range. For small tolerances of the reset delay the spread of the capacitance of the delay capacitor and its temperature coefficient should be noted.

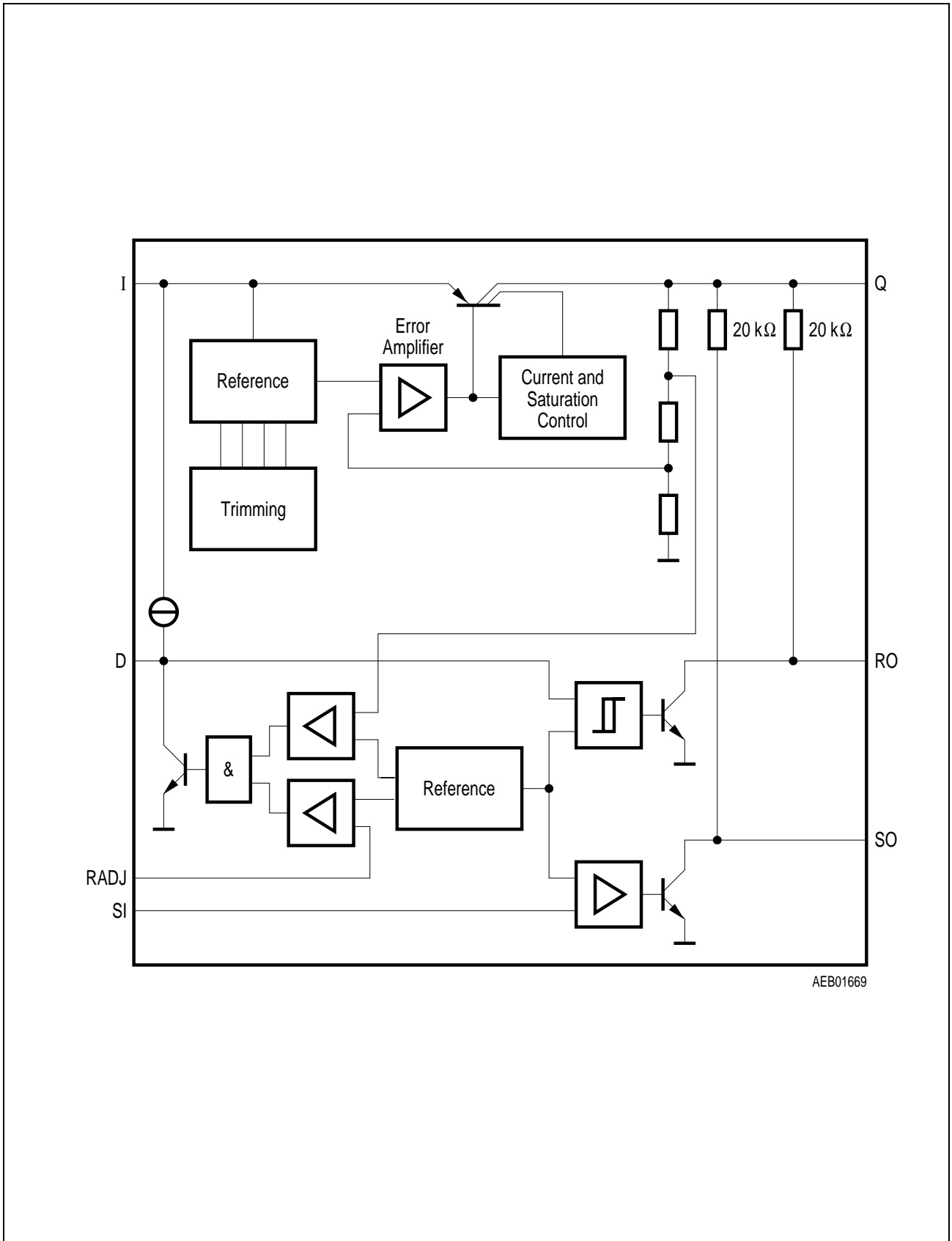


Figure 4 Block Diagram

Absolute Maximum Ratings
 $T_j = -40$ to 150 °C

| Parameter | Symbol | Limit Values | | Unit | Notes |
|-----------|--------|--------------|------|------|-------|
| | | min. | max. | | |

Input

| | | | | | |
|---------------|-------|------|----|---|------------------|
| Input voltage | V_I | - 40 | 45 | V | – |
| Input current | I_I | – | – | – | internal limited |

Sense Input

| | | | | | |
|---------------|----------|------|----|----|---|
| Input voltage | V_{SI} | - 40 | 45 | V | – |
| Input current | I_{SI} | 1 | 1 | mA | – |

Reset Threshold

| | | | | | |
|---------|------------|-------|----|----|---|
| Voltage | V_{RADJ} | - 0.3 | 7 | V | – |
| Current | I_{RADJ} | - 10 | 10 | mA | – |

Reset Delay

| | | | | | |
|---------|-------|-------|---|---|------------------|
| Voltage | V_D | - 0.3 | 7 | V | – |
| Current | I_D | – | – | – | internal limited |

Ground

| | | | | | |
|---------|-----------|----|---|----|---|
| Current | I_{GND} | 50 | – | mA | – |
|---------|-----------|----|---|----|---|

Reset Output

| | | | | | |
|---------|-------|-------|---|---|------------------|
| Voltage | V_R | - 0.3 | 7 | V | – |
| Current | I_R | – | – | – | internal limited |

Absolute Maximum Ratings (cont'd)
 $T_j = -40$ to 150 °C

| Parameter | Symbol | Limit Values | | Unit | Notes |
|-----------|--------|--------------|------|------|-------|
| | | min. | max. | | |

Sense Output

| | | | | | |
|---------|----------|-------|---|---|------------------|
| Voltage | V_{SO} | - 0.3 | 7 | V | - |
| Current | I_{SO} | - | - | - | internal limited |

5-V Output

| | | | | | |
|----------------|-------|-------|---|----|---|
| Output voltage | V_Q | - 0.5 | 7 | V | - |
| Output current | I_Q | - 10 | - | mA | - |

Temperature

| | | | | | |
|----------------------|-----------|------|-----|----|---|
| Junction temperature | T_j | - | 150 | °C | - |
| Storage temperature | T_{Stg} | - 50 | 150 | °C | - |

Operating Range

| | | | | | |
|----------------------|-------|------|-----|----|---|
| Input voltage | V_I | - | 45 | V | - |
| Junction temperature | T_j | - 40 | 150 | °C | - |

Thermal Data

| | | | | | |
|------------------|------------|---|-----------------|-------------------|-------------------------------------------------------|
| Junction-ambient | R_{thja} | - | 200 70 70 | K/W K/W K/W | P-DSO-8-3 P-DSO-14-8 P-DSO-20-17 |
| Junction-pin | R_{thjp} | - | 30 30 | K/W K/W | P-DSO-14-8 ¹⁾ P-DSO-20-17 ¹⁾ |

¹⁾ Measured to Pin 4

Characteristics
 $V_I = 13.5 \text{ V}; T_j = -40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$

| Parameter | Symbol | Limit Values | | | Unit | Measuring Condition |
|-------------------------------------------|--------------|--------------|------|------|---------------|-----------------------------------------------------------------------------------------|
| | | min. | typ. | max. | | |
| Output voltage | V_Q | 4.90 | 5.00 | 5.10 | V | $1 \text{ mA} \leq I_Q \leq 100 \text{ mA}$ $6 \text{ V} \leq V_I \leq 16 \text{ V}$ |
| Current limit | I_Q | 150 | 200 | 500 | mA | – |
| Current consumption; $I_q = I_I - I_Q$ | I_q | – | 240 | 300 | μA | $I_Q \leq 1 \text{ mA}, T_j < 85 \text{ }^\circ\text{C}$ |
| Current consumption; $I_q = I_I - I_Q$ | I_q | – | 250 | 700 | μA | $I_Q = 10 \text{ mA}$ |
| Current consumption; $I_q = I_I - I_Q$ | I_q | – | 2 | 8 | mA | $I_Q = 50 \text{ mA}$ |
| Drop voltage | V_{dr} | – | 0.25 | 0.5 | V | $I_Q = 100 \text{ mA}^1)$ |
| Load regulation | ΔV_Q | – | 10 | 30 | mV | $I_Q = 5 \text{ mA to } 100 \text{ mA}$ |
| Line regulation | ΔV_Q | – | 10 | 40 | mV | $V_I = 6 \text{ V to } 26 \text{ V}$ $I_Q = 1 \text{ mA}$ |

Reset Generator

| | | | | | | |
|------------------------------------|----------------|------|------|------|------------|-----------------------|
| Switching threshold | V_{RT} | 4.50 | 4.65 | 4.80 | V | – |
| Reset adjust switching threshold | $V_{RADJ, TH}$ | 1.26 | 1.35 | 1.44 | V | $V_Q > 3.5 \text{ V}$ |
| Reset pull up | – | 10 | 20 | 40 | k Ω | – |
| Saturation voltage | $V_{RO, SAT}$ | – | 0.1 | 0.4 | V | R_{intern} |
| Upper delay switching threshold | V_{UD} | 1.4 | 1.8 | 2.2 | V | – |
| Lower delay switching threshold | V_{LD} | 0.3 | 0.45 | 0.60 | V | – |
| Saturation voltage delay capacitor | $V_{D, SAT}$ | – | – | 0.1 | V | $V_Q < V_{RT}$ |

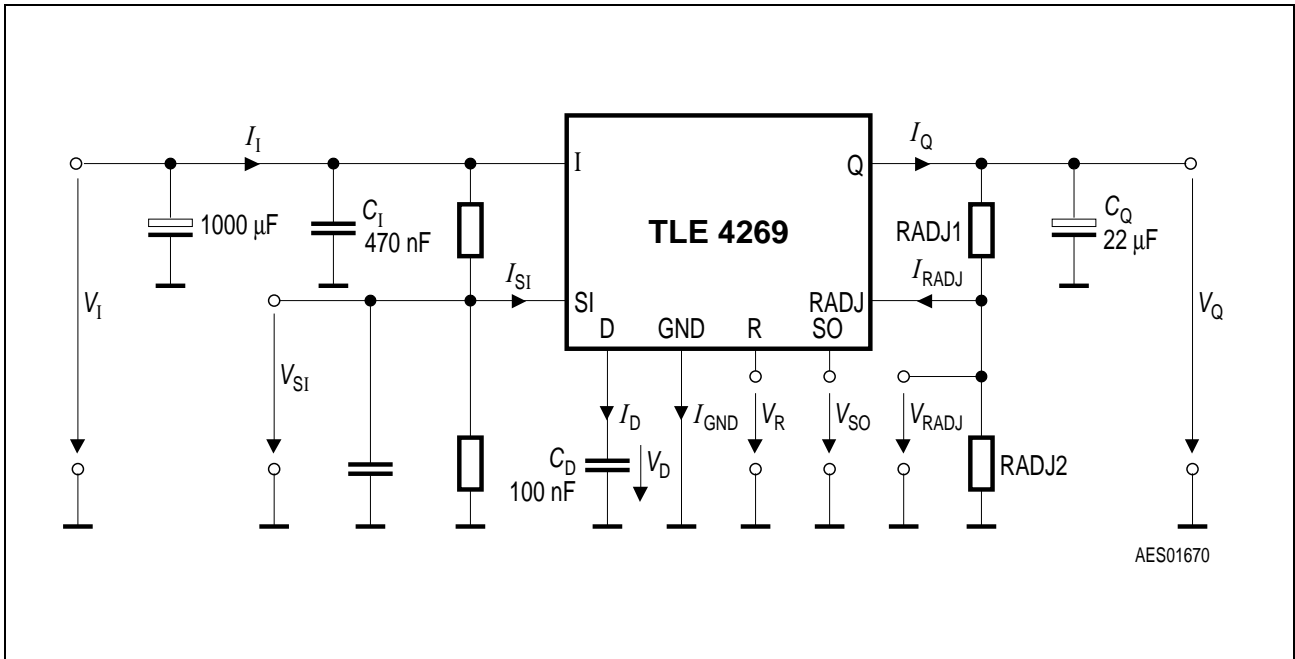
Characteristics (cont'd)
 $V_I = 13.5 \text{ V}; T_j = -40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$

| Parameter | Symbol | Limit Values | | | Unit | Measuring Condition |
|------------------------------|--------|--------------|------|------|---------------|------------------------|
| | | min. | typ. | max. | | |
| Charge current | I_D | 3.0 | 6.5 | 9.5 | μA | $V_D = 1 \text{ V}$ |
| Delay time L \rightarrow H | t_d | 17 | 28 | – | ms | $C_D = 100 \text{ nF}$ |
| Delay time H \rightarrow L | t_t | – | 1 | – | μs | $C_D = 100 \text{ nF}$ |

Input Voltage Sense

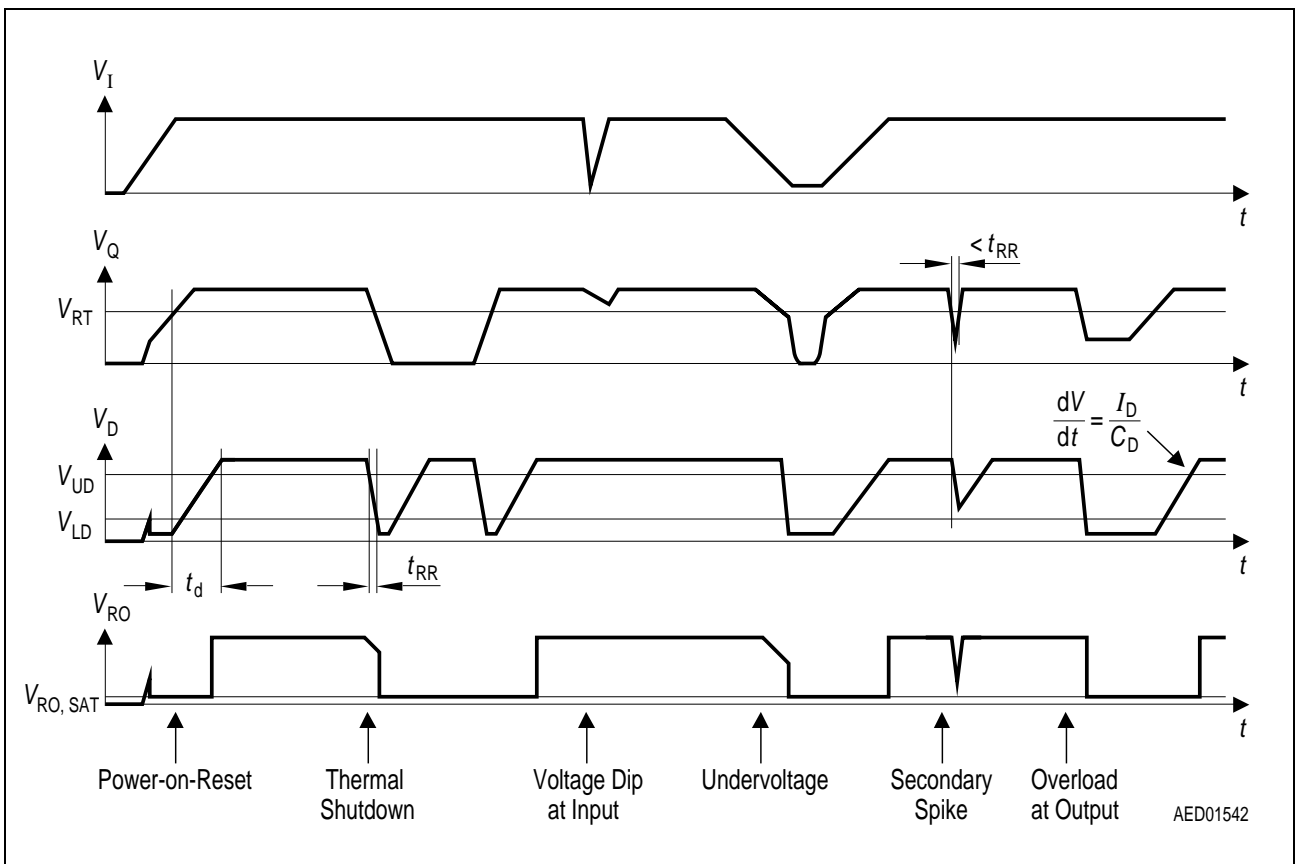
| | | | | | | |
|--------------------------|-----------------------|------|------|------|------------------|--------------------------------------------------------------------------|
| Sense threshold high | $V_{SI, \text{high}}$ | 1.24 | 1.31 | 1.38 | V | – |
| Sense threshold low | $V_{SI, \text{low}}$ | 1.16 | 1.20 | 1.28 | V | – |
| Sense output low voltage | $V_{SO, \text{low}}$ | – | 0.1 | 0.4 | V | $V_{SI} < 1.20 \text{ V};$ $V_Q > 3 \text{ V}$ R_{intern} |
| Sense pull up | – | 10 | 20 | 40 | $\text{k}\Omega$ | – |
| Sense input current | I_{SI} | – 1 | 0.1 | 1 | μA | – |

¹⁾ Drop voltage = $V_I - V_Q$ measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input.



AES01670

Figure 5 Measuring Circuit



AED01542

Figure 6 Reset Timing Diagram

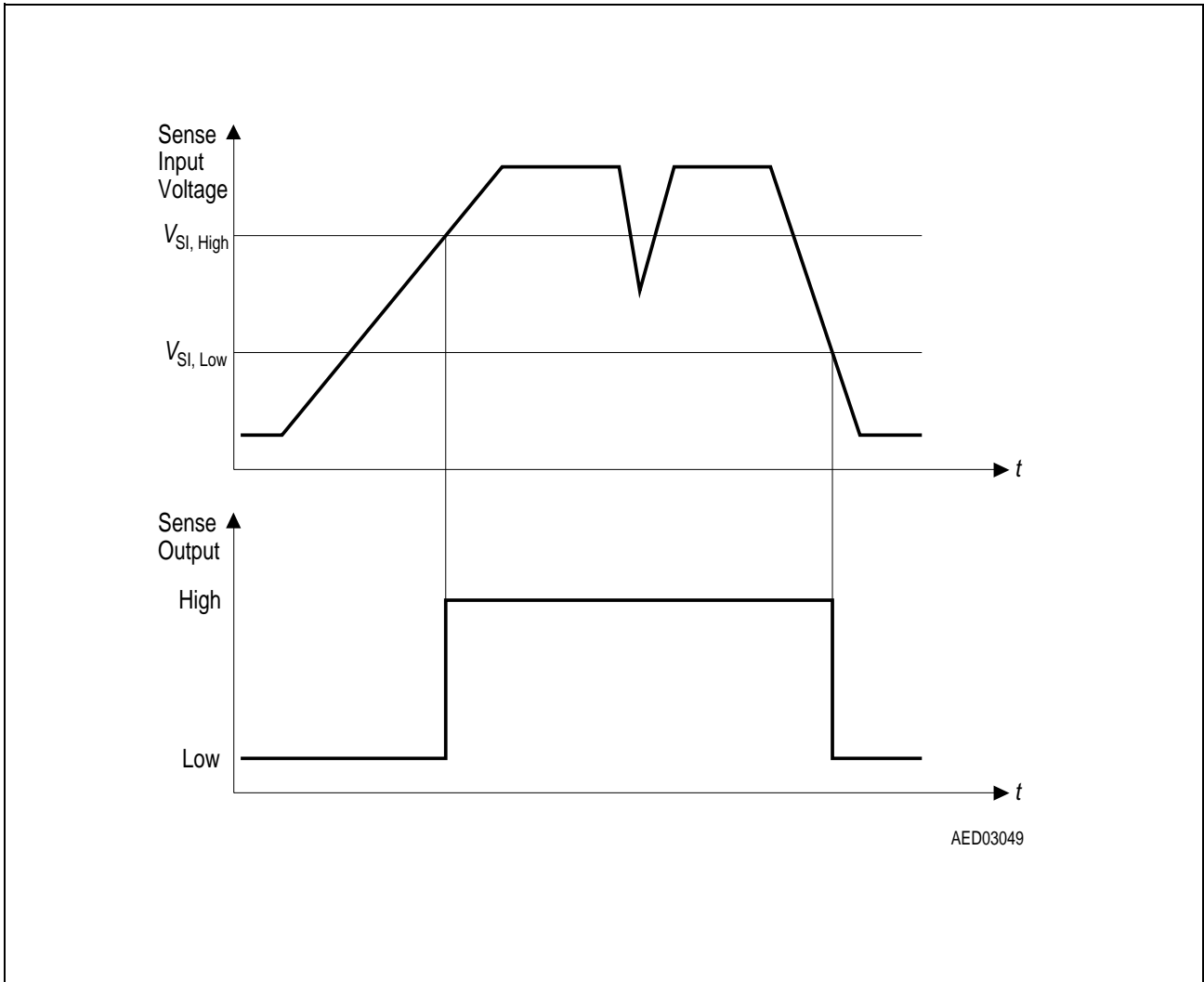
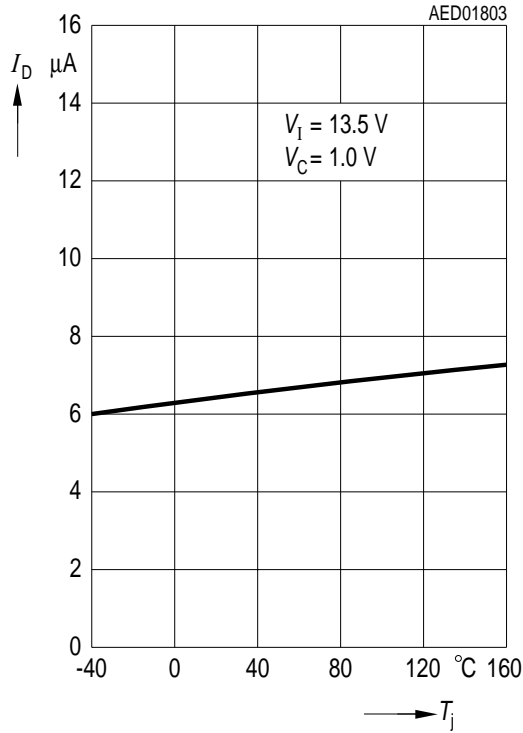
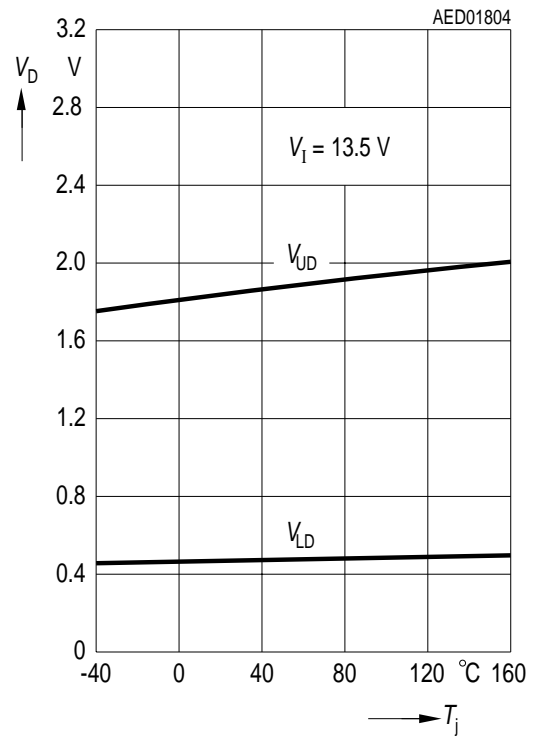


Figure 7 Sense Timing Diagram

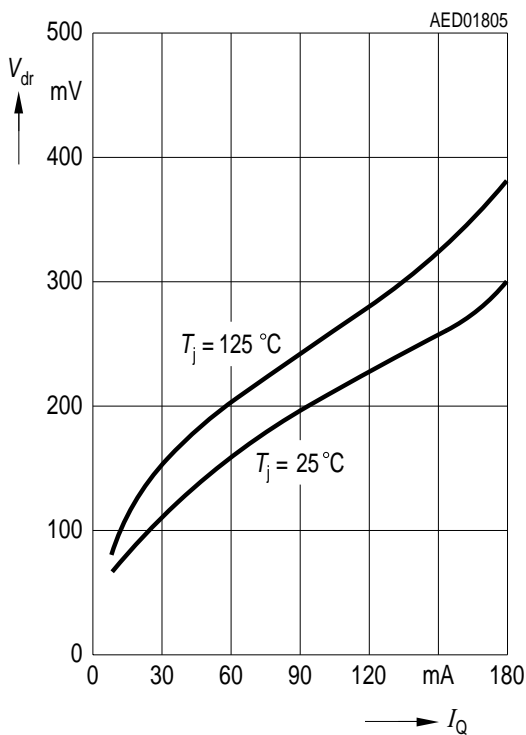
Charge Current I_D versus Temperature T_j



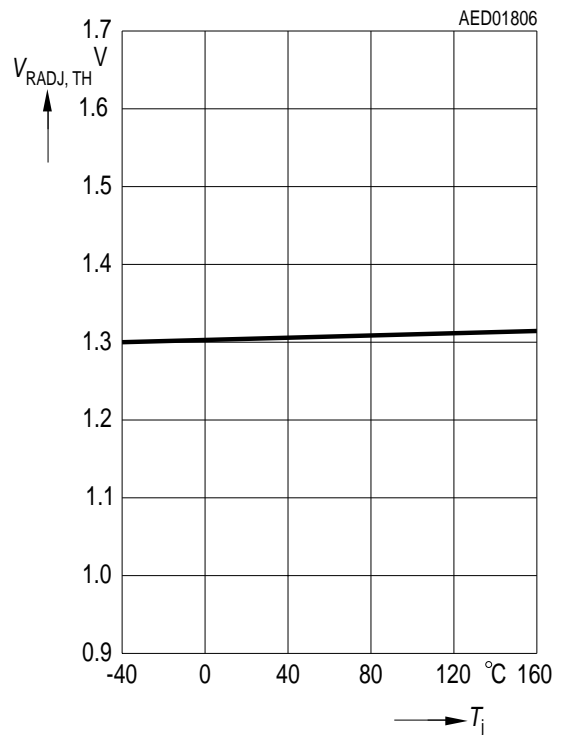
Switching Voltage V_{UD} and V_{LD} versus Temperature T_j



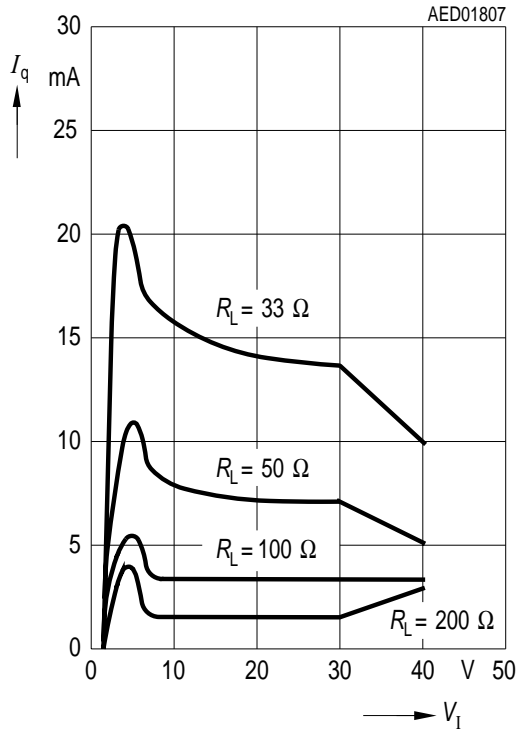
Drop Voltage V_{dr} versus Output Current I_Q



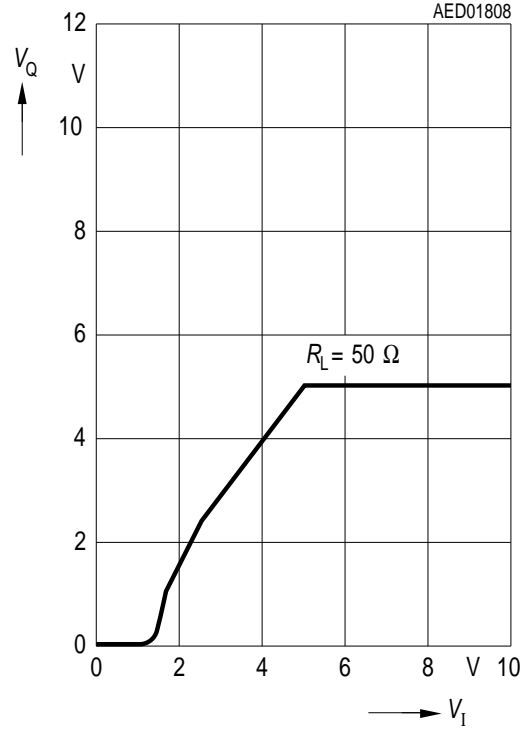
Reset Adjust Switching Threshold $V_{RADJ,TH}$ versus Temperature T_j



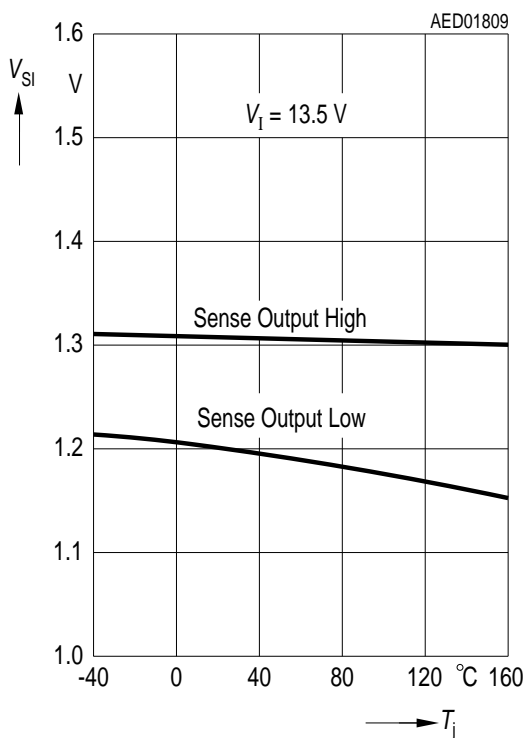
Current Consumption I_Q versus Input Voltage V_I



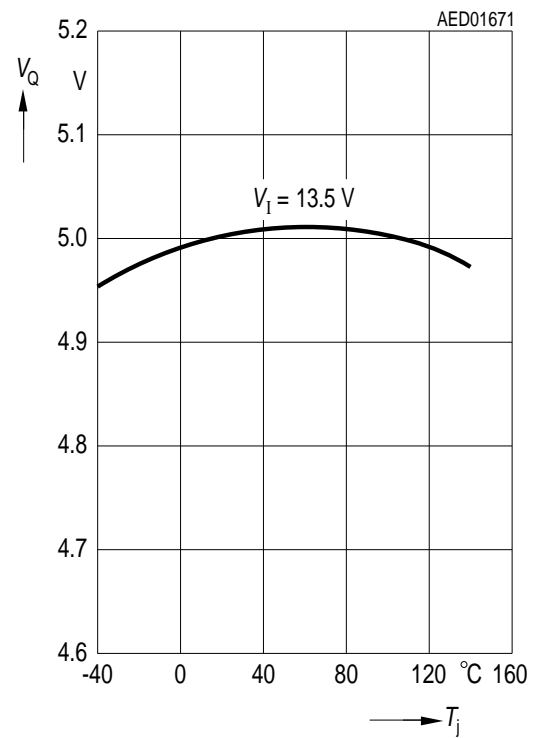
Output Voltage V_Q versus Input Voltage V_I



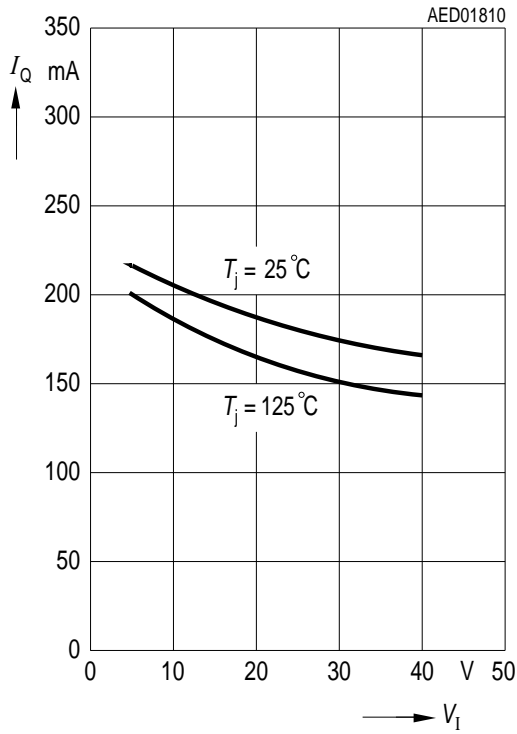
Sense Threshold V_{SI} versus Temperature T_j



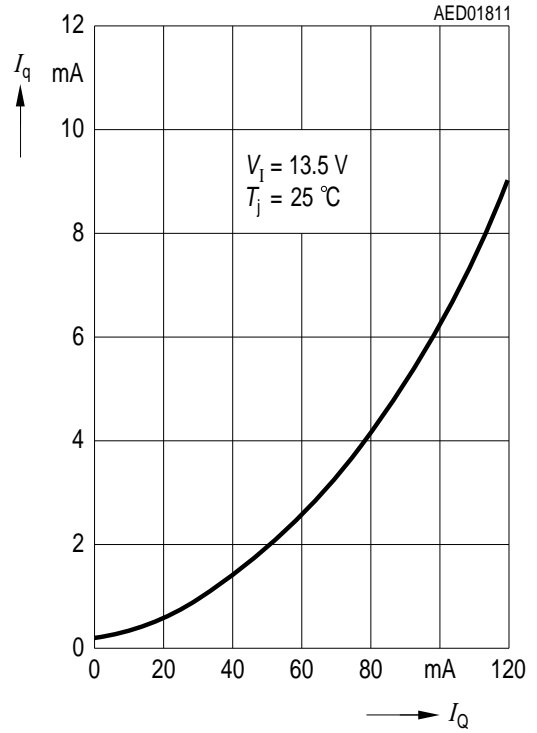
Output Voltage V_Q versus Temperature T_j



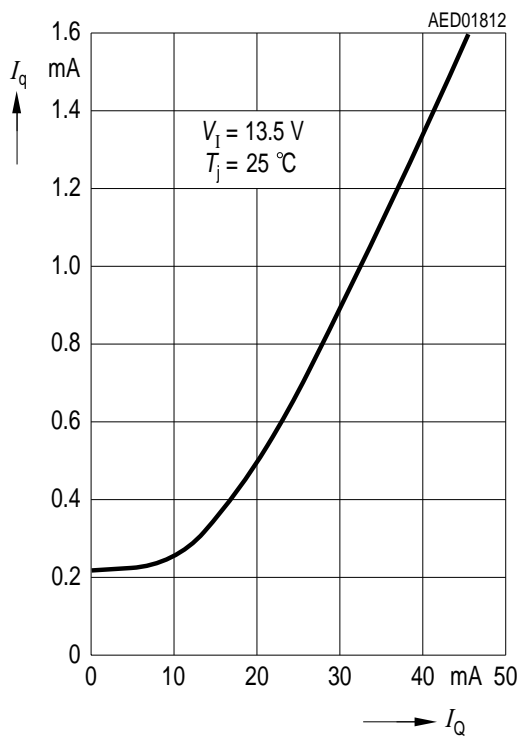
Output Current I_Q versus Input Voltage V_I



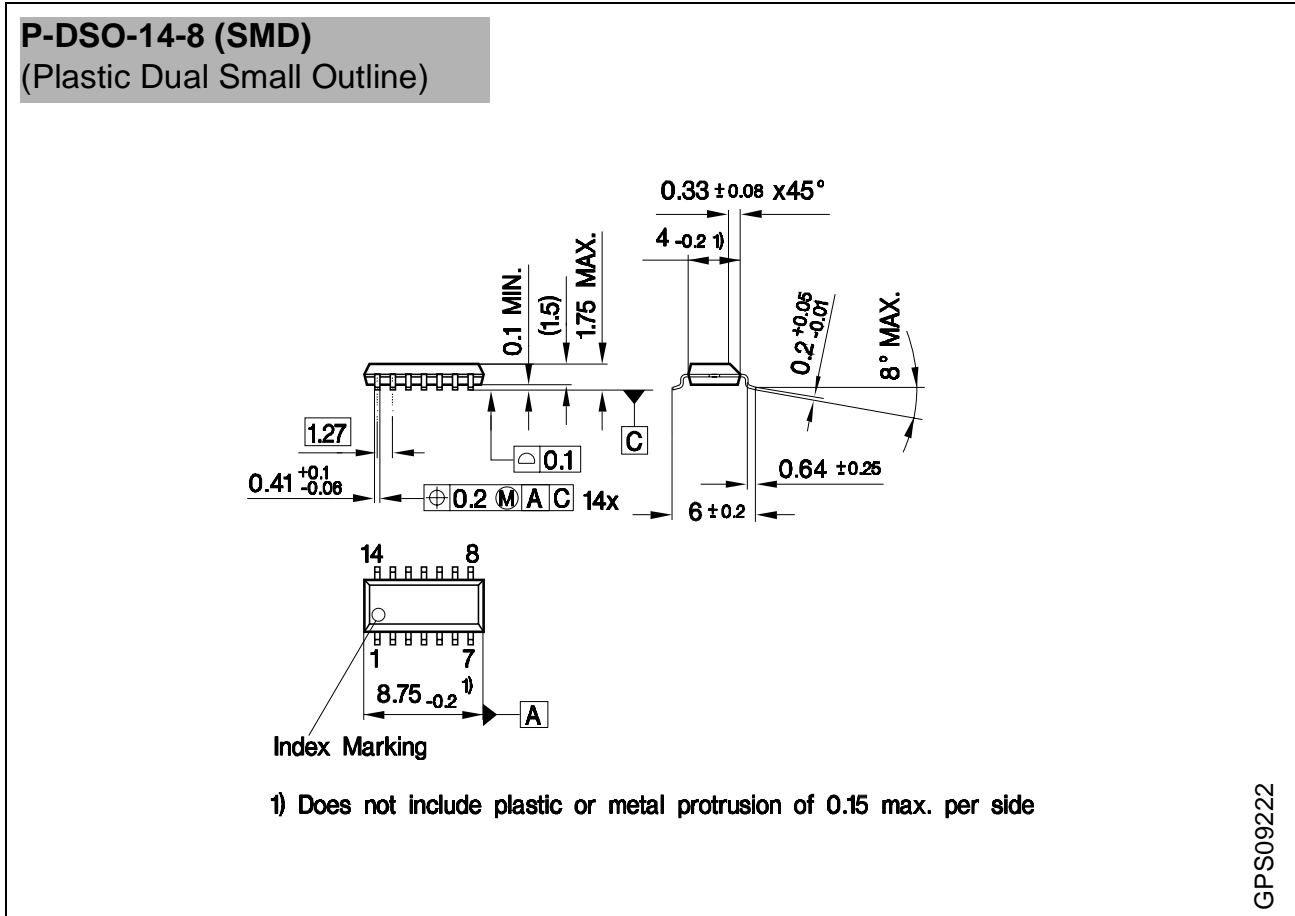
Current Consumption I_q versus Output Current I_Q



Current Consumption I_q versus Output Current I_Q



Package Outlines



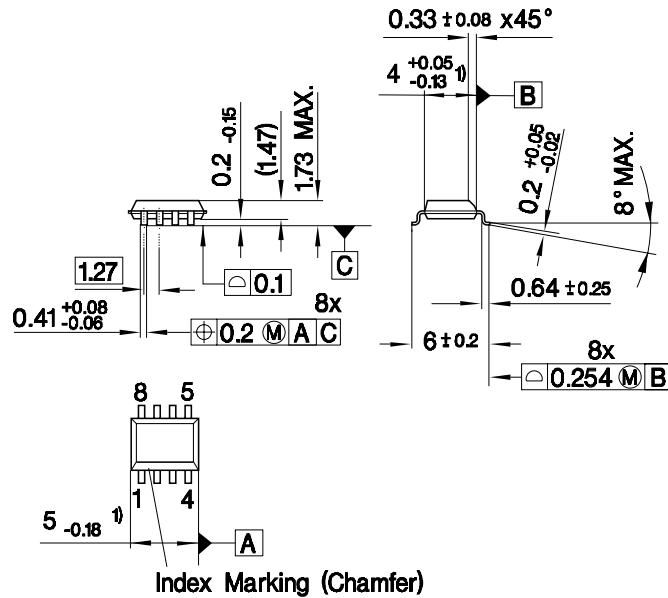
Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"

Dimensions in mm

SMD = Surface Mounted Device

P-DSO-8-3 (SMD)
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS09032

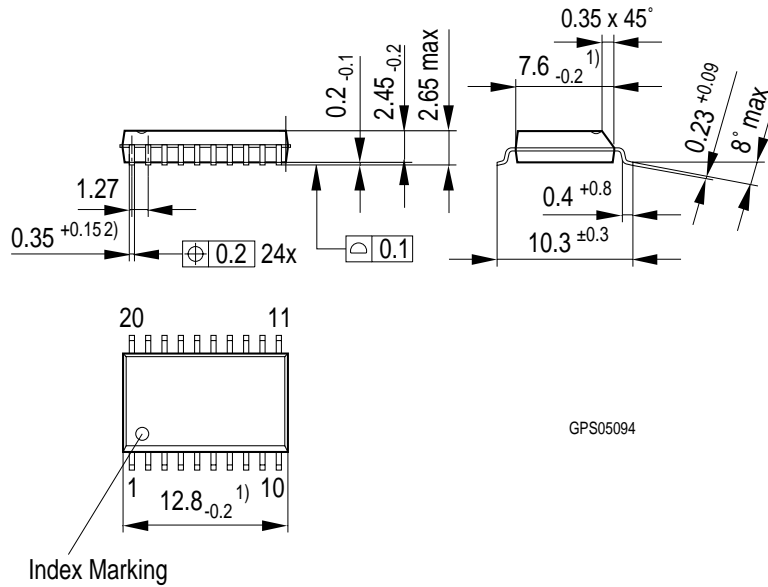
Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"

Dimensions in mm

SMD = Surface Mounted Device

P-DSO-20-17 (SMD)
 (Plastic Dual Small Outline)



- 1) Does not include plastic or metal protrusions of 0.15 max per side
 2) Does not include dambar protrusion of 0.05 max per side

Sorts of Packing

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Dimensions in mm

SMD = Surface Mounted Device

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