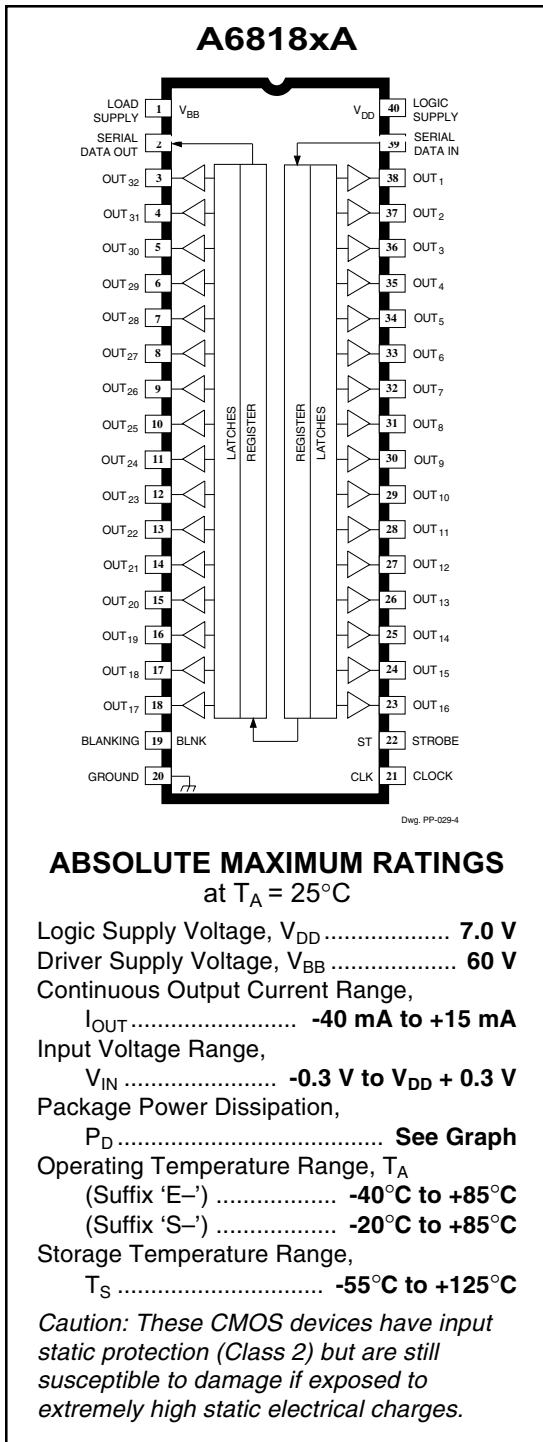


6818

DABiC-IV, 32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER



The A6818- devices combine a 32-bit CMOS shift register, accompanying data latches and control circuitry with bipolar sourcing outputs and pnp active pull downs. Designed primarily to drive vacuum-fluorescent displays, the 60 V and -40 mA output ratings also allow these devices to be used in many other peripheral power driver applications. The A6818- features an increased data input rate (compared with the older UCN/UCQ5818-F) and a controlled output slew rate.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 3.3 V or 5 V logic supply, typical serial-data input rates are up to 33 MHz.

A CMOS serial data output permits cascade connections in applications requiring additional drive lines. Similar devices are available as the A6809- and A6810- (10 bits), A6811- (12 bits), and A6812- (20 bits).

The A6818- output source drivers are npn Darlington, capable of sourcing up to 40 mA. The controlled output slew rate reduces electromagnetic noise, which is an important consideration in systems that include telecommunications and/or microprocessors and to meet government emissions regulations. For inter-digit blanking, all output drivers can be disabled and all sink drivers turned on with a BLANKING input high. The pnp active pull-downs will sink at least 2.5 mA.

Two temperature ranges are available for optimum performance in commercial (suffix S-) or industrial (suffix E-) applications. Package styles are provided for through-hole DIP (suffix -A) or minimum-area surface-mount PLCC (suffix -EP). Copper lead frames, low logic-power dissipation, and low output-saturation voltages allow these devices to drive most multiplexed vacuum-fluorescent displays over the maximum operating temperature range.

FEATURES

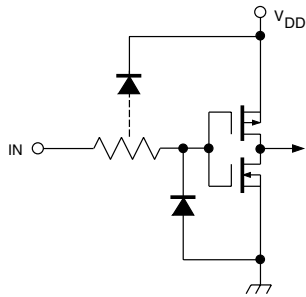
- Controlled Output Slew Rate
- High-Speed Data Storage
- 60 V Minimum Output Breakdown
- High Data Input Rate
- PNP Active Pull-Downs
- Low Output-Saturation Voltages
- Low-Power CMOS Logic and Latches
- Improved Replacements for SN75518N, SN75518NF, UCN5818-, and UCQ5818-

Complete part number includes a suffix to identify operating temperature range (E- or S-) and package type (-A or -EP). Always order by complete part number, e.g., **A6818SEP**.

6818

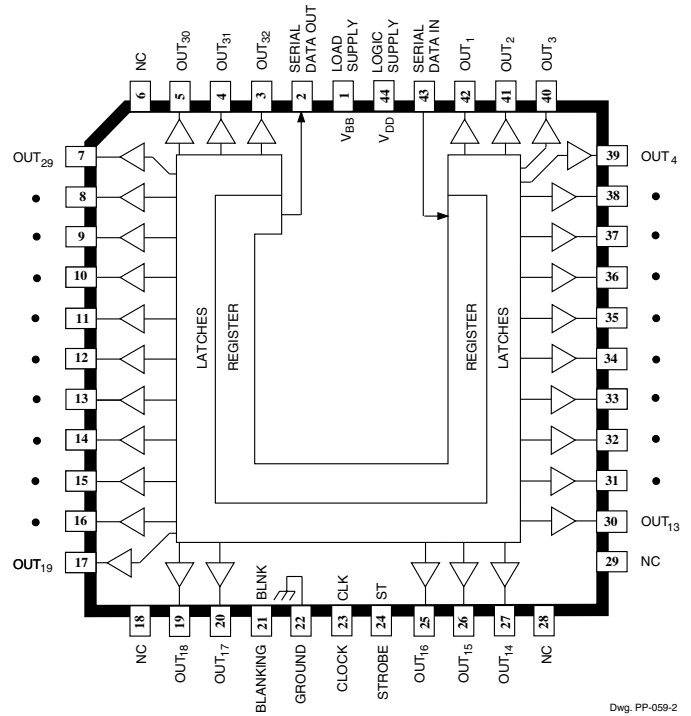
32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

TYPICAL INPUT CIRCUIT



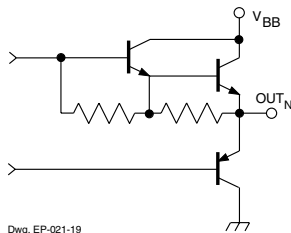
Dwg. EP-010-5

A6818xEP

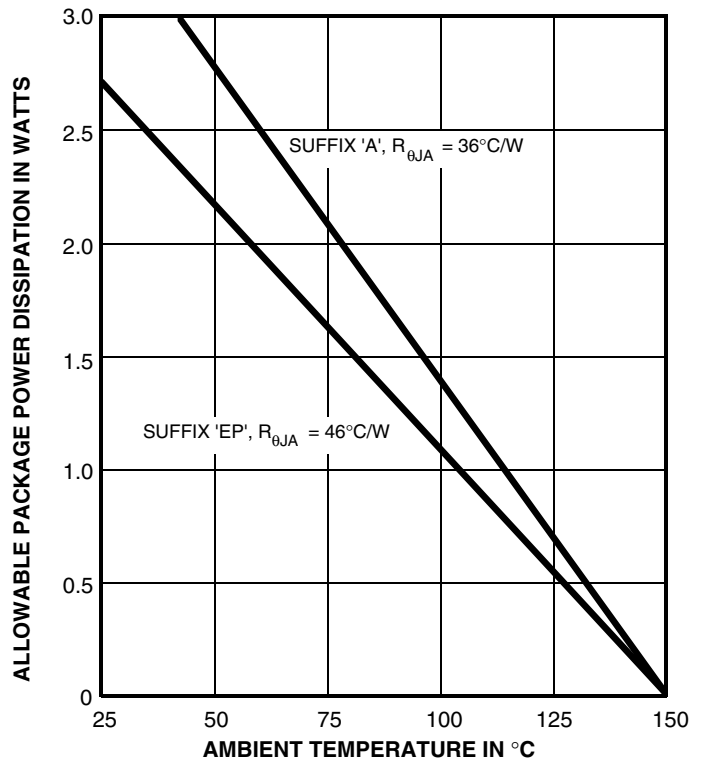


Dwg. PP-059-2

TYPICAL OUTPUT DRIVER



Dwg. EP-021-19

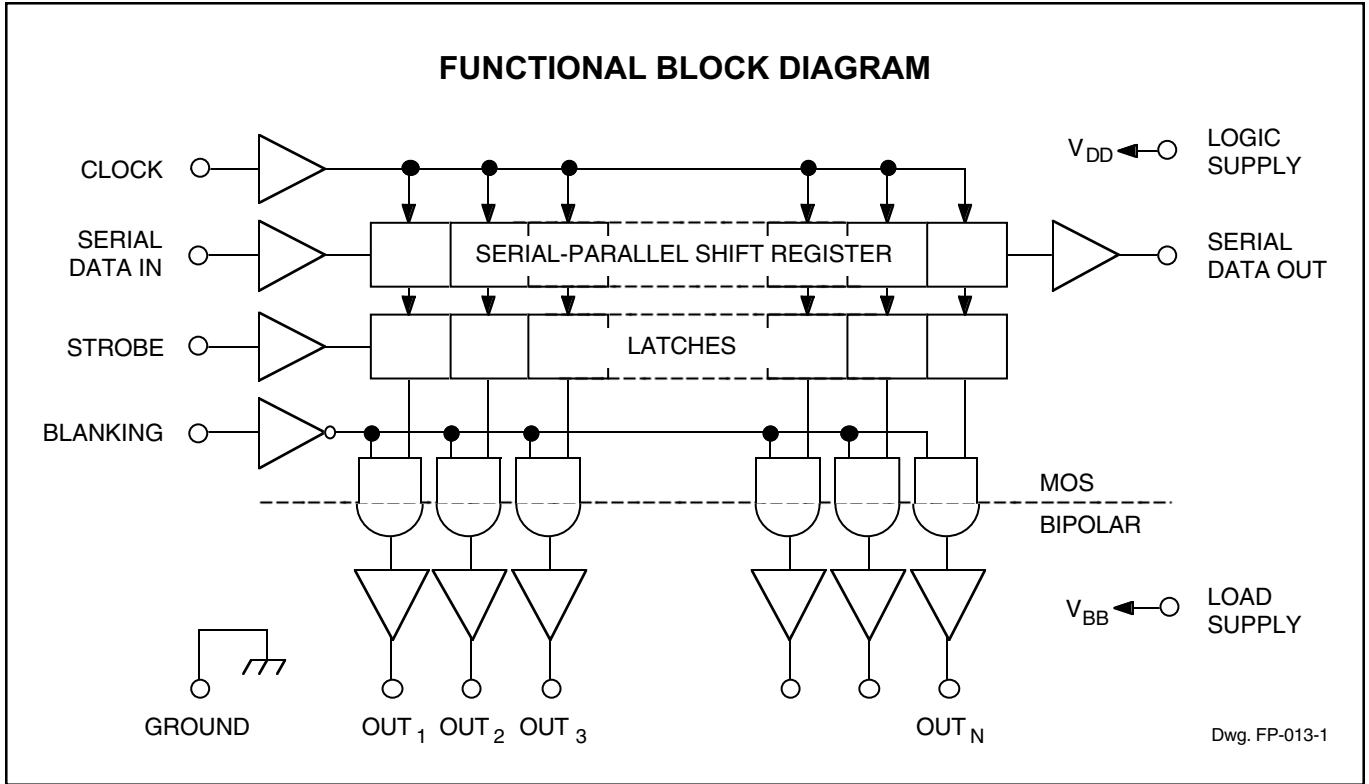


Dwg. GP-025A



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6818 32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER



TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents					Serial Data Output	Strobe Input	Latch Contents					Blanking	Output Contents						
		I ₁	I ₂	I ₃	...	I _{N-1}			I _N	I ₁	I ₂	I ₃	...		I _{N-1}	I _N	I ₁	I ₂	I ₃	...	I _{N-1}
H	⌋	H	R ₁	R ₂	...	R _{N-2}	R _{N-1}														
L	⌋	L	R ₁	R ₂	...	R _{N-2}	R _{N-1}														
X	⌋	R ₁	R ₂	R ₃	...	R _{N-1}	R _N														
		X	X	X	...	X	X	L	R ₁	R ₂	R ₃	...	R _{N-1}	R _N							
		P ₁	P ₂	P ₃	...	P _{N-1}	P _N	H	P ₁	P ₂	P ₃	...	P _{N-1}	P _N	L						
					...				X	X	X	...	X	X	H	L	L	L	...	L	L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

6818

32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

ELECTRICAL CHARACTERISTICS at $T_A = +25^\circ\text{C}$ (A6818S-) or over operating temperature range (A6818E- and A6818K-), $V_{BB} = 60\text{ V}$ unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits @ $V_{DD} = 3.3\text{ V}$			Limits @ $V_{DD} = 5\text{ V}$			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	$V_{OUT} = 0\text{ V}$	—	<-0.1	-15	—	<-0.1	-15	μA
Output Voltage	$V_{OUT(1)}$	$I_{OUT} = -25\text{ mA}$	57.5	58.3	—	57.5	58.3	—	V
	$V_{OUT(0)}$	$I_{OUT} = 1\text{ mA}$	—	1.0	1.5	—	1.0	1.5	V
Output Pull-Down Current	$I_{OUT(0)}$	$V_{OUT} = 5\text{ V to }V_{BB}$	2.5	5.0	—	2.5	5.0	—	mA
Input Voltage	$V_{IN(1)}$		2.2	—	—	3.3	—	—	V
	$V_{IN(0)}$		—	—	1.1	—	—	1.7	V
Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD}$	—	<0.01	1.0	—	<0.01	1.0	μA
	$I_{IN(0)}$	$V_{IN} = 0.8\text{ V}$	—	<-0.01	-1.0	—	<-0.01	-1.0	μA
Input Clamp Voltage	V_{IK}	$I_{IN} = -200\text{ }\mu\text{A}$	—	-0.8	-1.5	—	-0.8	-1.5	V
Serial Data Output Voltage	$V_{OUT(1)}$	$I_{OUT} = -200\text{ }\mu\text{A}$	2.8	3.05	—	4.5	4.75	—	V
	$V_{OUT(0)}$	$I_{OUT} = 200\text{ }\mu\text{A}$	—	0.15	0.3	—	0.15	0.3	V
Maximum Clock Frequency	f_c		10	33	—	10	33	—	MHz
Logic Supply Current	$I_{DD(1)}$	All Outputs High	—	0.25	0.75	—	0.3	1.0	mA
	$I_{DD(0)}$	All Outputs Low	—	0.25	0.75	—	0.3	1.0	mA
Load Supply Current	$I_{BB(1)}$	All Outputs High, No Load	—	4.5	9.0	—	4.5	9.0	mA
	$I_{BB(0)}$	All Outputs Low	—	0.2	20	—	0.2	20	μA
Blanking-to-Output Delay	$t_{dis(BQ)}$	$C_L = 30\text{ pF}$, 50% to 50%	—	0.7	2.0	—	0.7	2.0	μs
	$t_{en(BQ)}$	$C_L = 30\text{ pF}$, 50% to 50%	—	1.8	3.0	—	1.8	3.0	μs
Strobe-to-Output Delay	$t_{p(STH-QL)}$	$R_L = 2.3\text{ k}\Omega$, $C_L \leq 30\text{ pF}$	—	0.7	2.0	—	0.7	2.0	μs
	$t_{p(STH-QH)}$	$R_L = 2.3\text{ k}\Omega$, $C_L \leq 30\text{ pF}$	—	1.8	3.0	—	1.8	3.0	μs
Output Fall Time	t_f	$R_L = 2.3\text{ k}\Omega$, $C_L \leq 30\text{ pF}$	2.4	—	12	2.4	—	12	μs
Output Rise Time	t_r	$R_L = 2.3\text{ k}\Omega$, $C_L \leq 30\text{ pF}$	2.4	—	12	2.4	—	12	μs
Output Slew Rate	dV/dt	$R_L = 2.3\text{ k}\Omega$, $C_L \leq 30\text{ pF}$	4.0	—	20	4.0	—	20	V/ μs
Clock-to-Serial Data Out Delay	$t_{p(CH-SQX)}$	$I_{OUT} = \pm 200\text{ }\mu\text{A}$	—	50	—	—	50	—	ns

Negative current is defined as coming out of (sourcing) the specified device terminal.

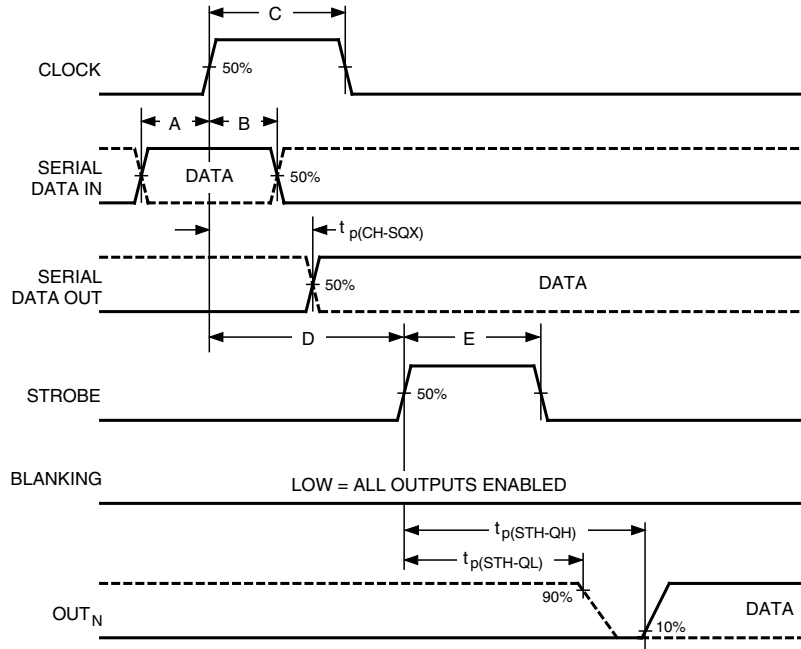
Typical data is for design information only and is at $T_A = +25^\circ\text{C}$.



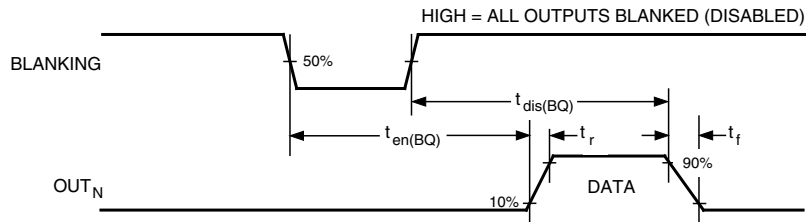
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TIMING REQUIREMENTS and SPECIFICATIONS

(Logic Levels are V_{DD} and Ground)



Dwg. WP-029



Dwg. WP-030

- A. Data Active Time Before Clock Pulse**
 (Data Set-Up Time), $t_{su(D)}$ **25 ns**
- B. Data Active Time After Clock Pulse**
 (Data Hold Time), $t_{h(D)}$ **25 ns**
- C. Clock Pulse Width, $t_w(CH)$ 50 ns**
- D. Time Between Clock Activation and Strobe, $t_{su(C)}$ 100 ns**
- E. Strobe Pulse Width, $t_w(STH)$ 50 ns**

NOTE – Timing is representative of a 10 MHz clock. Significantly higher speeds are attainable.

Serial Data present at the input is transferred to the shift register on the logic “0” to logic “1” transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

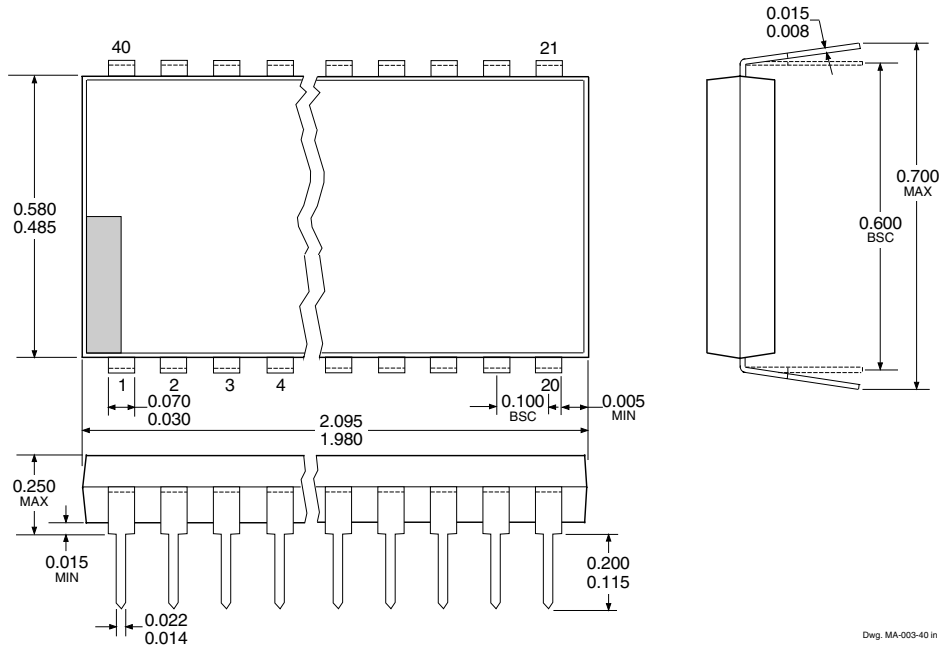
When the BLANKING input is high, the output source drivers are disabled (OFF); the pnp active pull-down sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

6818

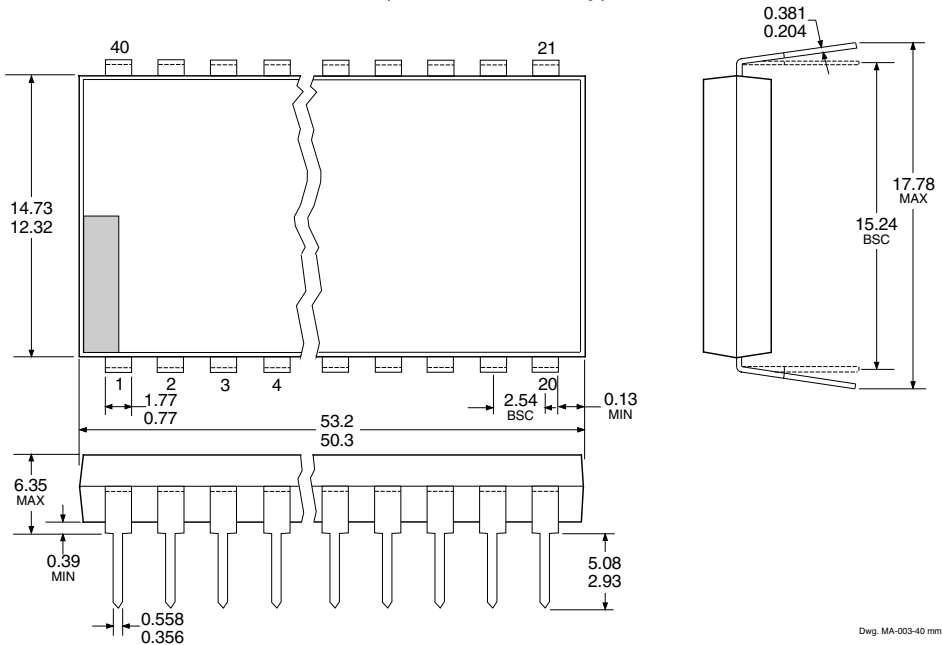
32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

A6818EA & A6811SA

Dimensions in Inches
(controlling dimensions)



Dimensions in Millimeters
(for reference only)



- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
 2. Lead spacing tolerance is non-cumulative.
 3. Lead thickness is measured at seating plane or below.



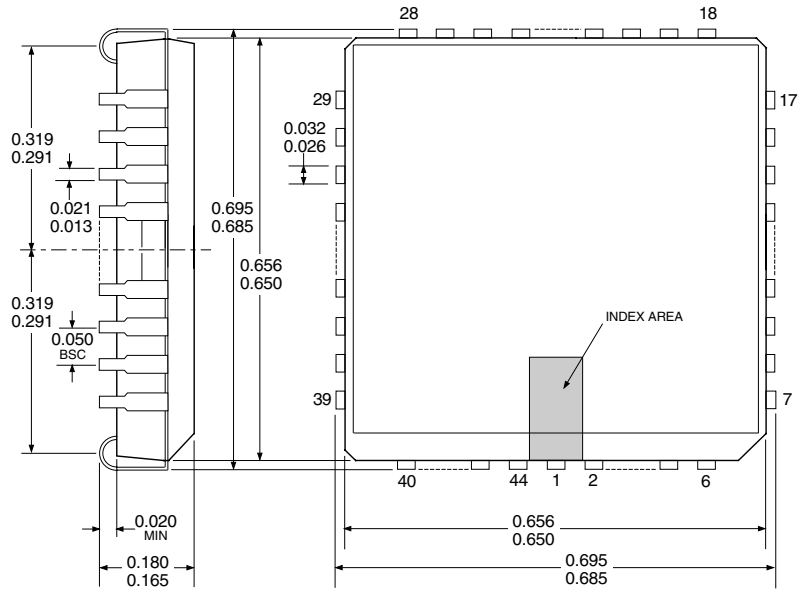
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32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

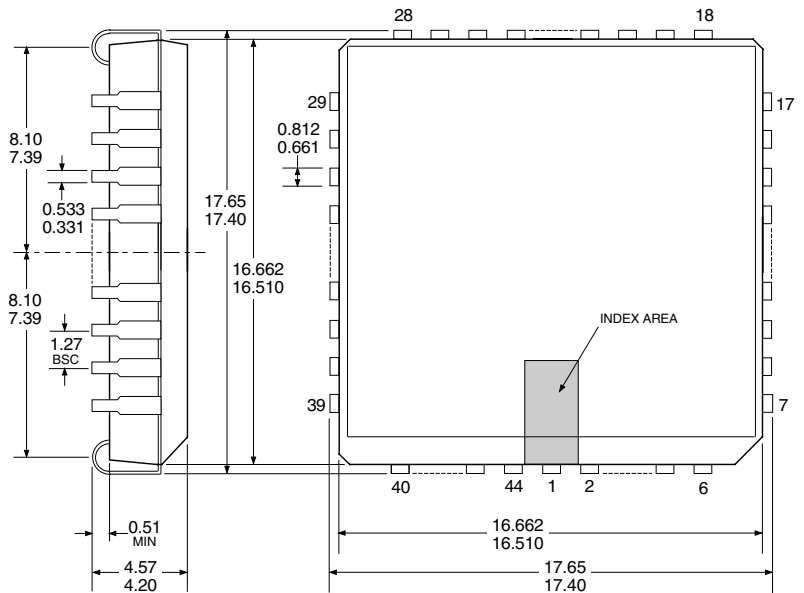
A6818EEP & A6818SEP

Dimensions in Inches
(controlling dimensions)



Dwg. MA-005-44A in

Dimensions in Millimeters
(for reference only)



Dwg. MA-005-44A mm

- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.

6818
32-BIT SERIAL-INPUT,
LATCHED SOURCE DRIVER

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