FEATURES

- Monolithic single chip device which handles ATM switch Ingress VPI/VCI address translation, cell appending, cell rate policing, counting, and OAM requirements for 65,536 VCs (virtual circuits)
- Instantaneous transfer rate of 800 Mbit/s supports a cell transfer rate of 1.42×10^6 cells/s (one STS-12c or four STS-3c).
- Concentrates the traffic from several PHY interfaces into one switch port.
- 8 or 16 bit PHY interface using direct addressing for up to 4 PHYs (compatible with Utopia Level 1 cell-level handshake) and Multi-PHY addressing for up to 32 PHYs (Utopia Level 2 compatible).
- 8 or 16 bit extended cell format SCI-PHY (52 - 64 byte extended ATM cell with prepend/postpend) interface at output to switch fabric.
- Compatible with wide range of switching fabrics and traffic management architectures including per VC or per PHY queuing.
- Provides identification/tagging of RM cells to support adjunct processing applications such as Virtual Source/Virtual Destination ABR service.
- Supports logical multicast.
- Flexible CAM-type cell identification which can use *arbitrary* VPI/VCI values and/or cell appended bytes for identification.
- Discards on command all low priority (high CLP bit) cells to relieve switch congestion.
- Can discard or tag the remainder of an AAL5 packet if a single cell in that packet is discarded or tagged due to policing.
- Includes a 16-bit FIFO buffered microprocessor bus interface for cell extraction and insertion (including OAM), VC table access, control and status monitoring, and configuration of the device.
- Supports DMA access for cell extraction and insertion.
- Uses common synchronous SRAMs for maintaining per-VC information.
- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.

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- Provides a generic 16-bit microprocessor bus interface for configuration, control and status monitoring.
- Low power, 0.6 micron, +5 Volt CMOS technology.
- 240 copper slugged plastic quad flat pack (PQFP) package.

Policing

- Policing is performed for adherence to peak cell rate (PCR), cell delay variation (CDV), sustained cell rate (SCR) and burst tolerance (BT). Violating cells can be noted, dropped or have CLP bits set to 1.
- Policing performed by an approximation to the Generic Cell Rate Algorithm (GCRA).
- Two policing instantiations available per VC. The policed cell streams can be any combination of user cells, OAM cells, Resource Management, high priority cells or low priority cells.

Cell Counting

- Counts maintained on a per VC basis include total low priority cells, total high priority cells and cells violating the traffic contract.
- Performance management counts are maintained for forward and reverse flows on a per VC basis: lost cells, misinserted cells, BIP-16 errors and the number of Severely Errored Cell Blocks (SECB).
- Counts maintained for entire device include total cells input, total cells output, OAM cells, cells discarded due to congestion, corrupted OAM cells, and cells with unassigned/invalid VPI/VCIs.

OAM Handling and Performance Monitoring

- OAM performance monitoring for all VCs as described in ITU-T Recommendation I.610, Bellcore TR-NWT-001248 and Bellcore GR-1113-CORE.
- Automatic OAM handling includes reception and generation of AIS, RDI, Forward Monitoring and Backward Reporting cells.
- Backward generated OAM cell identification/tagging provided to enable direct extraction by Egress device.
- Incoming OAM cells can be terminated or passed to the Output Cell Interface and/or microprocessor.

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- Outgoing OAM cells sourced from automatic OAM generating circuitry, Input Cell Interface or microprocessor.

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APPLICATIONS

- ATM Hubs and Workgroup Switches
- ATM Enterprise and Edge Switches

REFERENCES

- ATM Forum - ATM User-Network Interface Specification, V3.0, October, 1993
- ITU-T Recommendation I.361 - "B-ISDN ATM Layer Specification", March 1993
- ITU-T Recommendation I.371 - "Traffic Control and Congestion Control in B-ISDN", March 1993
- ITU-T Recommendation I.610 - "B-ISDN Operation and Maintenance Principles and Functions", Helsinki, March 1993.
- Bell Communications Research - Broadband Switching System (BSS) Generic Requirements, GR-1110-CORE, Issue 1, September 1994.
- Bell Communications Research -Asynchronous Transfer Mode (ATM) and ATM Adaptation Layer (AAL) Protocols, GR-1113-CORE, Issue 1, July 1994.
- Bell Communications Research - Generic Requirements for Operations of Broadband Switching Systems, TA-NWT-001248, Issue 2, October 1993.
- IEEE 1149.1 - Standard Test Access Port and Boundary Scan Architecture, May 21, 1990.
- PMC-940212, ATM_SCI_PHY, "SATURN Compliant Interface For ATM Devices", July 1994, Issue 2.
- ATM Forum/95-0013R9, Draft Version 3.0 of ATM Forum Traffic Management Specification Version 4.0, October, 1995

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APPLICATION EXAMPLES

The RCMP-800 device is combined with up to 32 PHY devices to implement the ingress direction an ATM switch port. Two ATM switch port applications are shown in Figures 1 and 2.

The RCMP-800 device accepts standard 53 byte cells through a SCI-PHY interface and outputs cells with variable length pre-pends or post-pends through a extended cell format SCI-PHY interface. The appendages added by the RCMP-800 are used by the switch for routing. The HEC can optionally be omitted. The combined pre-pend and post-pend length can vary from 0 to 10 bytes, with the cells correspondingly being 52 to 63 octets or 26 to 32 words.

Backward generated OAM cells and Resource Management cells are specially labelled by overwriting an appended byte to allow these cells to be processed and routed in the reverse direction.

The RCMP-800 utilizes external synchronous RAMs to store VPI/VCI translation tables and per VPI/VCI switch-specific routing appendages, as well as per VPI/VCI policing and performance monitoring information. All of this information is stored in a single structure called the *VC table*.

Fig. 1 OC-3 Switch Port Application

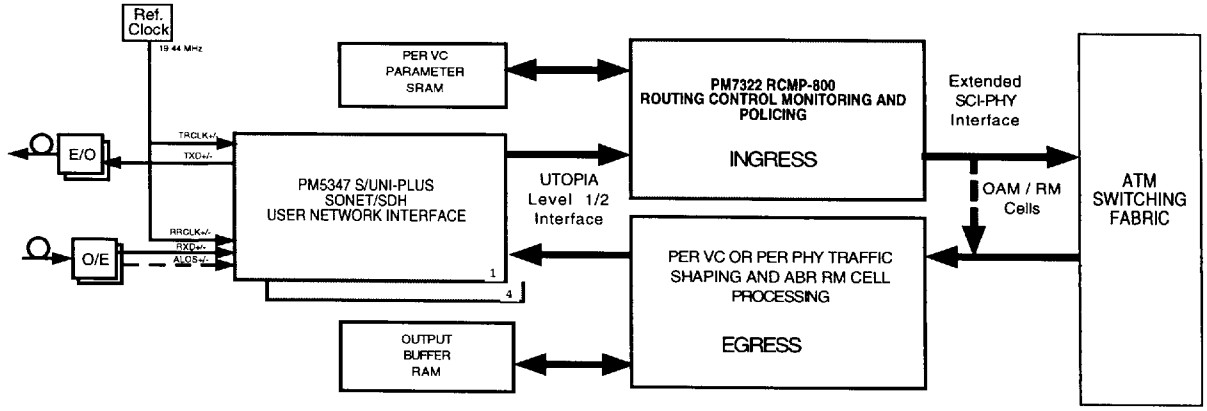

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Fig. 2 DS-1 PHY Addressing Application

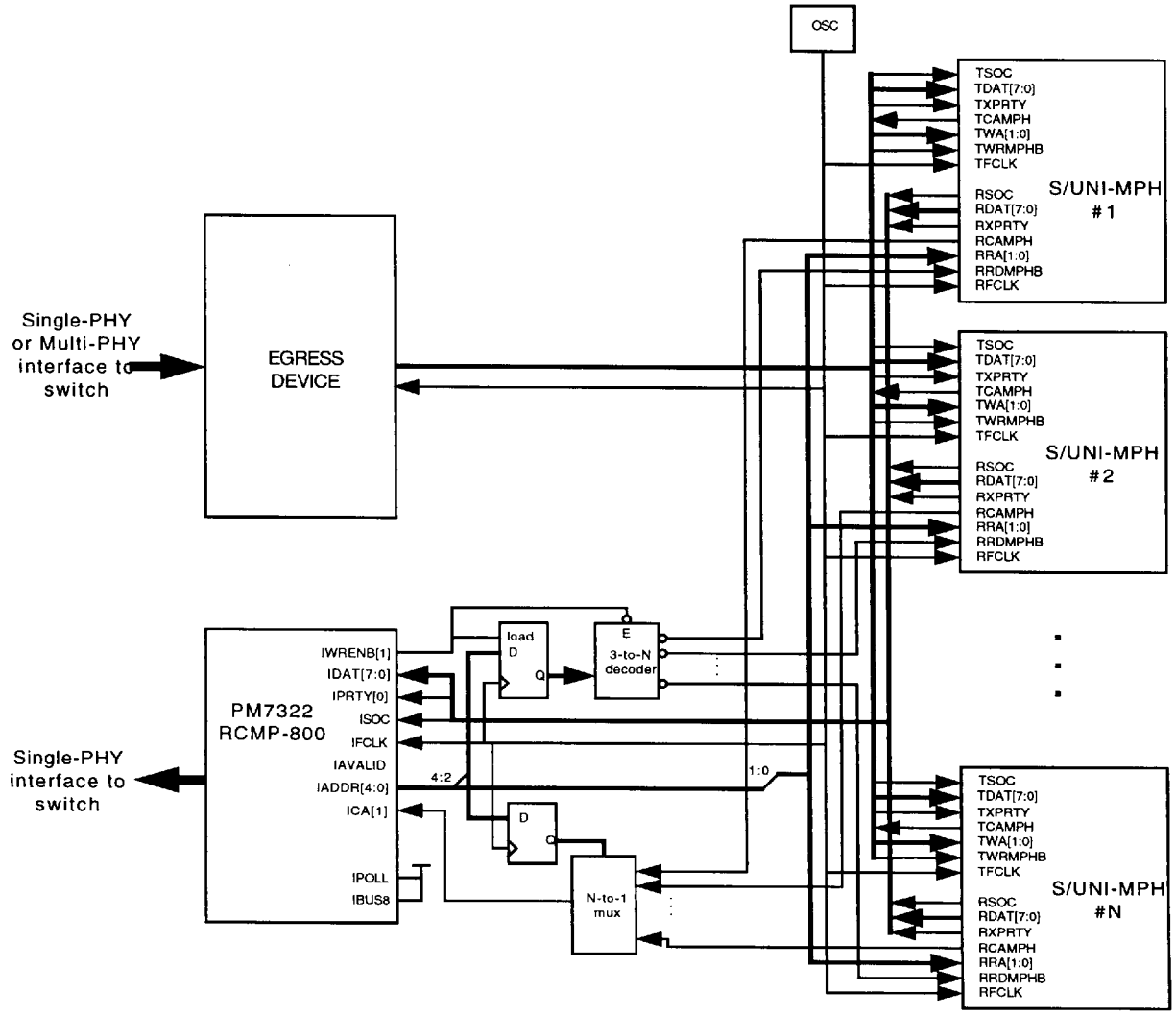

Figure 2 illustrates how up to 32 PHY Utopia Level 1 entities may be interfaced to an RCMP-800. With a minimum amount of support circuitry (eg. a single PAL), the PHY addressing mode of operation polls the PHY devices to determine the next cell for transfer. In this example, a quad DS-1 ATM device, the S/UNI-MPH (PM7344), provides the PHY transmission convergence function. Eight S/UNI-MPH devices would be required to provide 32 DS-1 ports.

The S/UNI-MPH supports PHY address polling by sampling the two least significant address bits (RRA[1:0] and TWA[1:0]) and generating the cell available status for the selected PHY entity. It also holds the last state of RRA[1:0] and TWA[1:0] before the assertion of RRDMPHB and TWRMPHB, respectively, thus latching the PHY address

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resolved by the polling process. The only support logic is that required to select between the S/UNI-MPH devices.

The IAVALID output is not required for this application.

In this application, the aggregate throughput is less than 6.144 Mbyte/s with 32 DS-1 ports; therefore, the clock oscillator frequency can be as low as 6.5 MHz.

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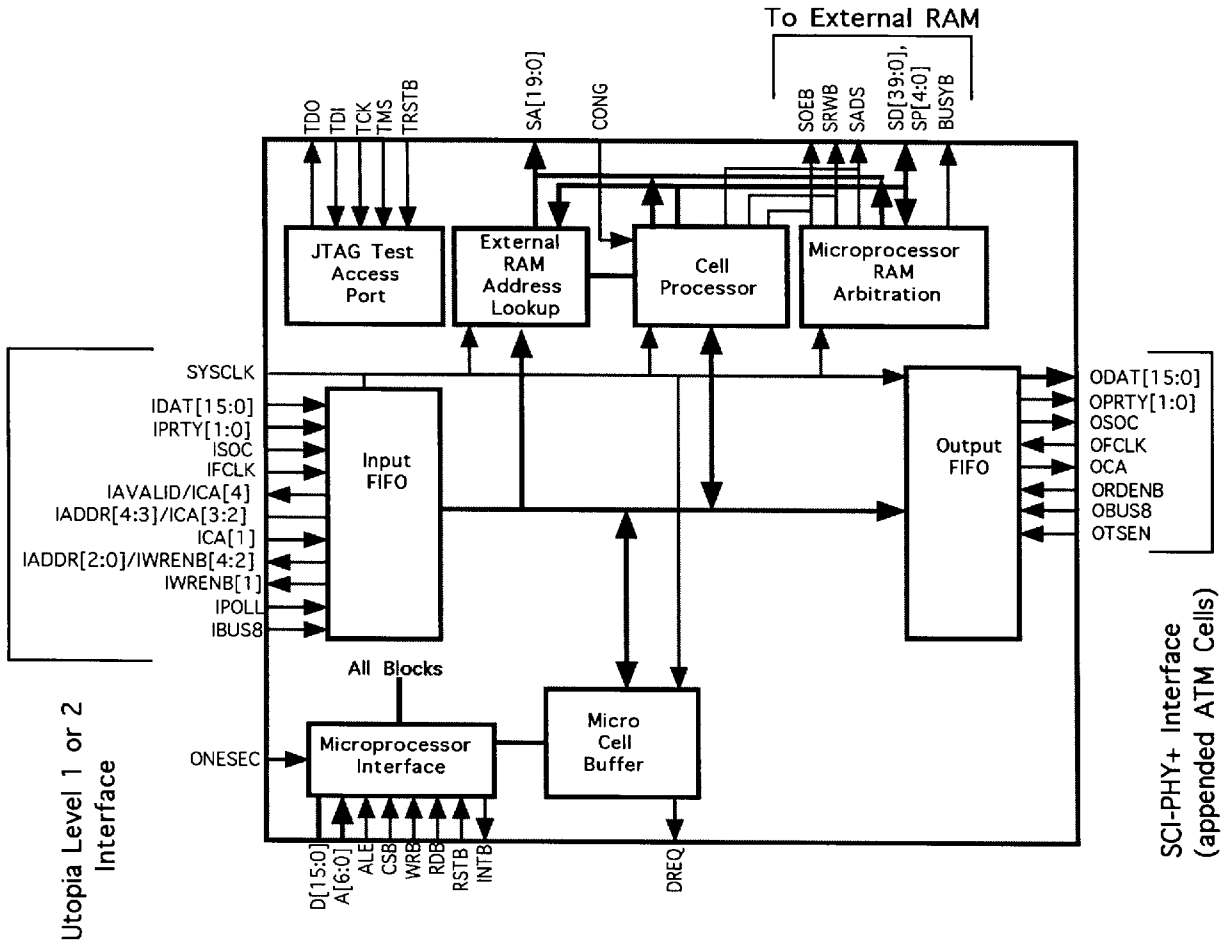
BLOCK DIAGRAM



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DESCRIPTION

The PM7322 Routing Control, Monitoring and Policing 800 Mbps (RCMP-800) device is a monolithic integrated circuit that implements ATM layer functions that include fault and performance monitoring, header translation and cell rate policing. The RCMP-800 is intended to be situated between a switch core and the physical layer devices in the ingress direction. The RCMP-800 supports a sustained aggregate throughput of 1.42×10^6 cells/s. The RCMP-800 uses external SRAM to store per-VPI/VCI data structures. The device is capable of supporting up to 65536 connections.

The Input Cell Interface can be connected to up to 32 physical layer devices through a SCI-PHY compatible bus. The 53 byte ATM cell is encapsulated in a data structure which can contain pre-pended or post-pended routing information. Received cells are buffered in a four cell deep FIFO. All Physical Layer and unassigned cells are discarded. For the remaining cells, a subset of ATM header and appended bits is used as a search key to find the VC Table Record for the virtual connection. If a connection is not provisioned and the search terminates unsuccessfully as a result, the cell is discarded and a count of invalid cells is incremented. If the search is successful, subsequent processing of the cell is dependent on contents of the cell and configuration fields in the VC Table Record.

The RCMP-800 performs header translation if so configured. The ATM header is replaced by contents of fields in the VC Table Record for the connection. The VCI contents are passed through transparently for VPCs. Appended bytes can be replaced, added or removed.

If the RCMP-800 is the end point for a F4 or F5 OAM stream, the OAM cells are dropped and processed. If the RCMP-800 is not the end point, the OAM cells are passed to the Output Cell Interface with an optional copy passed to the Microprocessor Cell Buffer. The reception of an AIS or RDI cell results in the appropriate alarm. Upon the arrival of a Forward Monitoring or Monitoring/Reporting cell, error counts are updated and a Backward Reporting cell is optionally generated. Activate/Deactivate cells are passed to the Microprocessor Cell Buffer for external processing. Continuity Check cells can be generated if no user cells have been received in the latest 1 or 2 (default) seconds.

Cell rate policing is supported through two approximations of the Generic Cell Rate Algorithm (GCRA) for each connection. Each cell that violates the traffic contract can be tagged (CLP bit set high) or discarded. To allow full flexibility, each GCRA instance can be programmed to police any combination of user cells, OAM cells, Resource Management, high priority cells or low priority cells.

The RCMP-800 supports multicasting. A single received cell can result in an arbitrary number of cells presented on the Output Cell Interface, each with its own

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unique VPI/VCI value and appended bytes. The ATM cell payload is duplicated without modification.

The Output Cell Interface can be connected to the switch core through an extended cell format SCI-PHY compatible bus. Cells are stored in a four cell deep FIFO until the downstream devices are ready to accept them. The details of how cells are handled in this FIFO depends on the particular application of the RCMP-800 and are presented in "Operational Modes" section.

The Microprocessor Interface is provided for device configuration, control and monitoring by an external microprocessor. This interface provides access to the external SRAM to allow creation of the data structure, configuration of individual connections and monitoring of the connections. The Microprocessor Cell Buffer gives access to the cell stream, either directly or through intervention by a DMA controller. Programmed cell types can be routed to a microprocessor readable sixteen cell FIFO. The microprocessor can send cells over the Output Cell Interface.

The RCMP-800 is implemented in low power, 0.6 micron, +5 Volt CMOS technology. It has TTL compatible inputs and outputs and is packaged in a 240 pin copper slugged plastic QFP package.

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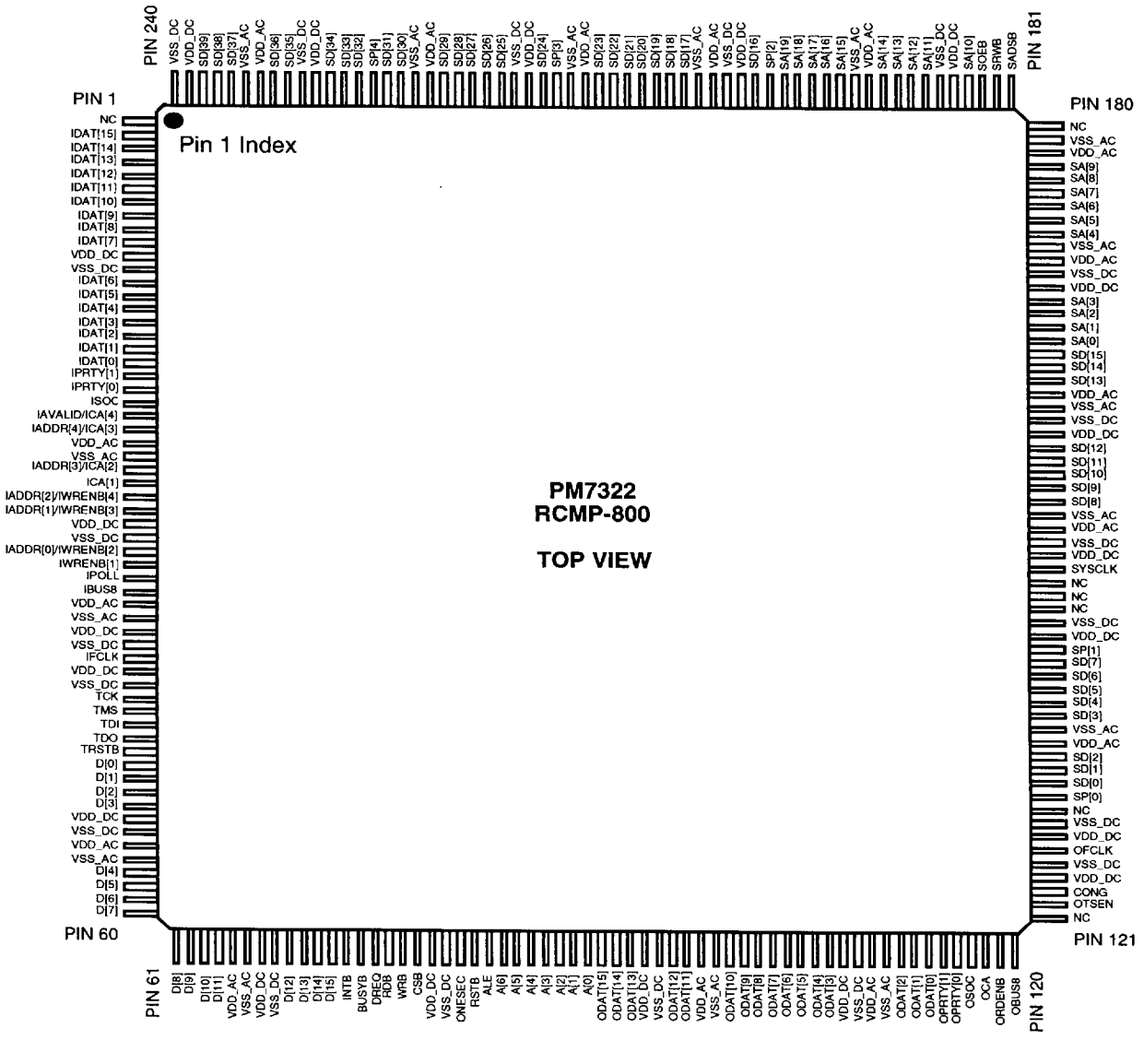
PIN DIAGRAM

The RCMP-800 is packaged in a 240 pin slugged plastic QFP package having a body size of 32 mm by 32 mm and a pin pitch of 0.5 mm.



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PIN DESCRIPTION (TOTAL 240)

Output Cell Interface Signals (24)

Pin Name	Type	Pin No.	Feature
OFCLK	Input	126	The output FIFO clock (OFCLK) is used to read words from the Output Cell Interface. OFCLK must cycle at a 52 MHz or lower instantaneous rate, but at a high enough rate to avoid FIFO overflow. OSOC, OCA, OPRTY[1:0] and ODAT[15:0] are updated on the rising edge of OFCLK. ORDENB is sampled using the rising edge of OFCLK.
OBUS8	Input	120	The 8-bit bus width select (OBUS8) input selects the Output Cell Interface bus width. When OBUS8 is tied high, a 10-bit interface consisting of a start of cell indication, parity bit and an 8-bit octet bus is selected. When OBUS8 is tied low, a 19-bit interface consisting of a start of cell indication, two parity bits and a 16-bit word bus is selected.
ORDENB	Input	119	The active low read enable (ORDENB) signal is used to indicate transfers from the Output Cell Interface. When ORDENB is sampled low using the rising edge of OFCLK, a word is read from the internal synchronous FIFO and output on bus ODAT[15:0]. When ORDENB is sampled high using the rising edge of OFCLK, no read is performed and outputs ODAT[15:0], OPRTY[1:0] and OSOC are tristated if the OTSEN input is high. ORDENB must operate in conjunction with OFCLK to access the FIFO at a high enough instantaneous rate as to avoid FIFO overflows.

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ODAT[0] ODAT[1] ODAT[2] ODAT[3] ODAT[4] ODAT[5] ODAT[6] ODAT[7] ODAT[8] ODAT[9] ODAT[10] ODAT[11] ODAT[12] ODAT[13] ODAT[14] ODAT[15]	Tristate	114 113 112 107 106 105 104 103 102 101 100 97 96 93 92 91	The output cell data (ODAT[15:0]) bus carries the ATM cell octets that are read from the output FIFO. If the IBUS8 input is high, only ODAT[7:0] carries cell octets. The ODAT[15:0] bus is updated on the rising edge of OFCLK. When the Output Cell Interface is configured for tristate operation using the OTSEN input, tristating of the ODAT[15:0] output bus is controlled by the ORDENB input. When OTSEN is low, the ODAT[15:0] bus is low when no cell is being transferred.
OPRTY[0] OPRTY[1]	Tristate	116 115	The output parity (OPRTY[1:0]) signals indicate the parity of the ODAT[15:0] bus. OPRTY[1] is the parity calculation over the ODAT[15:8] bus. OPRTY[0] is the parity calculation over the ODAT[7:0] bus. Alternately the device can be configured so that OPRTY[1] is the parity calculation over the entire ODAT[15:0] bus. Odd or even parity selection can be made using a register bit. OPRTY[1:0] is updated on the rising edge of OFCLK. When the Output Cell Interface is configured for tristate operation using the OTSEN input, tristating of the OPRTY[1:0] output bus is controlled by the ORDENB input.
OSOC	Tristate	117	The output start of cell (OSOC) signal marks the start of cell on the ODAT[15:0] bus. When OSOC is high, the first word of the cell structure is present on the ODAT[15:0] stream. OSOC is updated on the rising edge of OFCLK. When the Output Cell Interface is configured for tristate operation using the OTSEN input, tristating of the OSOC output is controlled by the ORDENB input.

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OCA	Output	118	The active polarity of this signal is programmable and defaults to active high. OCA indicates when a cell is available in the output FIFO. When asserted, the OCA signal indicates that the output FIFO has at least one cell available to be read. The OCA signal is deasserted when the output FIFO contains four or zero words available for the current cell. Selection is made using the OCALEVEL0 bit in the Output FIFO Configuration register. OCA is updated on the rising edge of OFCLK.
OTSEN	Input	122	The tristate enable (OTSEN) signal allows tristate control over the ODAT[15:0], OPRTY[1:0] and OSOC outputs. When OTSEN is high, the active low read enable input, ORDENB, controls when the ODAT[15:0], OPRTY[1:0] and OSOC outputs are driven. When OTSEN is low, the ODAT[15:0], OPRTY[1:0] and OSOC outputs are always driven.

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Input Cell Interface Signals (30)

Pin Name	Type	Pin No.	Feature
IFCLK	Input	41	The input FIFO clock (IFCLK) is used to write words to the synchronous FIFO interface. IFCLK must cycle at a 52 MHz or lower instantaneous rate. ISOC, ICA[4:1], IPRTY[1:0] and IDAT[15:0] are sampled on the rising edge of IFCLK. IWRENB[4:1], IADDR[4:0] and IAVALID are updated on the rising edge of IFCLK.
IPOLL	Input	35	The input polling select (IPOLL) pin determines the method used to poll PHY devices. If IPOLL is low, the IWRENB[4:1] and ICA[4:1] signals are connected directly to up to four single-PHY entities. If IPOLL is high, polling using address lines is used. The RCMP-800 uses the IADDR[4:0] and IAVALID outputs to perform sequential polling of the PHY devices to determine the next cell to transfer.
IBUS8	Input	36	The bus width select (IBUS8) input selects the input FIFO interface bus width. When IBUS8 is tied high, a 10-bit interface consisting of a start of cell indication, an 8-bit octet bus, and a parity bit is selected. When IBUS8 is low, a 19-bit interface consisting of a start of cell indication, a 16-bit word bus, and two parity bits is selected.
IWRENB[1] IWRENB[2] IWRENB[3] IWRENB[4]	Output	34 33 30 29	The active low write enable (IWRENB[4:1]) inputs are used to initiate writes to the input FIFO. If the IPOLL input is low, the RCMP-800 asserts one of the IWRENB[4:1] outputs to transfer a cell from one of up to four PHY devices. A valid word is expected on the IDAT[15:0] bus at the second rising edge of IFCLK after one of the enables is asserted low. When all of the enables are high, no valid data is expected. The IWRENB[4:1] outputs are updated on the rising edge of IFCLK. See Figure 7. If the IPOLL input is high, the IWRENB[4:2] pins are redefined as IADDR[2:0]. The IWRENB[1] pin is used to transfer all cells. The source PHY is selected by the IADDR[4:0] signals.

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IADDR[4] IADDR[3] IADDR[2] IADDR[1] IADDR[0]	I/O	24 27 29 30 33	If the IPOLL input is high, the IADDR[4:0] pins are used for PHY addressing. If the IPOLL input is low, the IADDR[4:0] pins are redefined as ICA[3:2] and IWRENB[4:2]. If the IPOLL input is high, the IADDR[4:0] signals are outputs and are used to address up to 32 PHY devices for the purposes of polling and selection for cell transfer. When conducting polling, in order to avoid bus contention, the RCMP-800 inserts gap cycles during which IADDR[4:0] is set to 1F hex and IAVALID to logic 0. When this occurs, no PHY device should drive ICA[1] during the following clock cycle. Polling is performed in a incrementing sequential order. The PHY device selected for transfer is based on the IADDR[4:0] value present when IWRENB[1] falls. The IADDR[4:0] bus is updated on the rising edge of IFCLK.
IAVALID	I/O	23	If the IPOLL input is high, the PHY Address Valid (IAVALID) pin is active. If the IPOLL input is low, the IAVALID pin is redefined as ICA[4]. If the IPOLL input is high, the IAVALID pin indicates that the IADDR[4:0] bus is outputting a valid PHY address for polling purposes. When this signal is deasserted, the IADDR[4:0] bus is set to 1F hex. IAVALID is not necessary when less than 32 PHY links are being polled.
IDAT[0] IDAT[1] IDAT[2] IDAT[3] IDAT[4] IDAT[5] IDAT[6] IDAT[7] IDAT[8] IDAT[9] IDAT[10] IDAT[11] IDAT[12] IDAT[13] IDAT[14] IDAT[15]	Input	19 18 17 16 15 14 13 10 9 8 7 6 5 4 3 2	The input cell data (IDAT[15:0]) bus carries the ATM cell octets that are written to the input FIFO. The IDAT[15:0] bus is sampled on the rising edge of IFCLK and is considered valid only when one of the IWRENB[4:1] signals so indicates.

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IPRTY[0] IPRTY[1]	Input	21 20	The input parity (IPRTY[1:0]) signals indicate the parity of the IDAT[15:0] bus. IPRTY[1] is expected to be the parity calculation over the IDAT[15:8] bus. IPRTY[0] is expected to be the parity calculation over the IDAT[7:0] bus. Alternately the device can be configured so that IPRTY[1] is expected to be the parity calculation over the entire IDAT[15:0] bus. Odd or even parity selection can be made using a register. A maskable interrupt status is generated upon a parity error; no other actions are taken. IPRTY[1:0] is sampled on the rising edge of IFCLK and is considered valid only when one of the IWRENB[4:1] signals so indicates.
ISOC	Input	22	The input start of cell (ISOC) signal marks the start of cell on the IDAT[15:0] bus. When ISOC is high, the first word of the cell structure is present on the IDAT[15:0] stream. It is not necessary for ISOC asserted for each cell. An interrupt may be generated if ISOC is high during any word other than the first word of the cell structure. ISOC is sampled on the rising edge of IFCLK and is considered valid only when one of the IWRENB[4:1] signals so indicates.
ICA[1] ICA[2] ICA[3] ICA[4]	I/O	28 27 24 23	The active polarity of these signals is programmable and defaults to active high. If the IPOLL input is low, the RCMP-800 asserts the appropriate IWRENB[4:1] signal in response to a round-robin polling of the ICA[4:1] signals. Once committed, the RCMP-800 will transfer an entire cell from a single physical link before servicing the next. The RCMP-800 will complete the read of an entire cell even if the associated ICA[4:1] input is deasserted during the cell. Sampling of ICA[4:1] resumes the cycle after the last octet of a cell has been transferred.

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ICA[4:1] (cont.)			If the IPOLL input is high, the ICA[3:2] pins are redefined as IADDR[4:3] and the ICA[4] pin is redefined as IAVALID.x If the IPOLL input is high, the RCMP-800 polls up to 32 PHY devices using the PHY address signals IADDR[4:0]. A PHY device being addressed by IADDR[4:0] is expected to indicate whether or not it has a complete cell available for transfer by driving ICA[1] during the clock cycle following that in which it is addressed. (When a cell transfer is in progress, the RCMP-800 will not poll the PHY device which is sending the cell and so PHY devices need not support cell availability indication during cell transfer.) The selection of a particular PHY device from which to transfer a cell is indicated by the state of IADDR[4:0] when IWRENB[1] falls.

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Synchronous SRAM Interface Signals (70)

Pin Name	Type	Pin No.	Feature
SD[39]	I/O	238	The bi-directional SRAM Data (SD[39:0]) pins interface directly with synchronous SRAM data ports. A SRAM read is performed when the RCMP-800 drives the address strobe (SADSB) low and the SRWB output high. The RCMP-800 tristates the SD[39:0] pins and samples the value driven by the SRAM on the second rising edge of the SYSCLK input after SADSB is asserted. A SRAM write is performed when RCMP-800 drives the address strobe (SADSB) low and the SRWB output low. The RCMP-800 presents valid data on the SD[39:0] pins upon the rising edge of SYSCLK which is written into the SRAM on the next SYSCLK rising edge. SD[39:0] is tri-stated on the rising edge of SYSCLK. Contention is avoided by not performing a read during the cycle after the write burst.
SD[38]		237	
SD[37]		236	
SD[36]		233	
SD[35]		232	
SD[34]		229	
SD[33]		228	
SD[32]		227	
SD[31]		225	
SD[30]		224	
SD[29]		221	
SD[28]		220	
SD[27]		219	
SD[26]		218	
SD[25]		217	
SD[24]		214	
SD[23]		210	
SD[22]		209	
SD[21]		208	
SD[20]		207	
SD[19]		206	
SD[18]		205	
SD[17]		204	
SD[16]		199	
SD[15]		163	
SD[14]		162	
SD[13]		161	
SD[12]		156	
SD[11]		155	
SD[10]		154	
SD[9]		153	
SD[8]		152	
SD[7]		140	
SD[6]		139	
SD[5]		138	
SD[4]		137	
SD[3]		136	
SD[2]		133	
SD[1]		132	
SD[0]		131	

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SP[4] SP[3] SP[2] SP[1] SP[0]	I/O	226 213 198 141 130	The SRAM Parity (SP[4:0]) pins provide parity protection over the SD[39:0] bus. SP[4] completes odd parity for SD[39:32]. SP[3] completes odd parity for SD[31:24]. SP[2] completes odd parity for SD[23:16]. SP[1] completes odd parity for SD[15:8]. SP[0] completes odd parity for SD[7:0]. SP[4:0] has the same timing as SD[39:0]. When data is being written to the external SRAM, the RCMP-800 generates correct parity. When data is being read from the external SRAM, the RCMP-800 checks the parity and generates a maskable interrupt indication upon an error. No other action is taken; therefore, the SP[4:0] may be unconnected if parity protection is not required.
SA[19] SA[18] SA[17] SA[16] SA[15] SA[14] SA[13] SA[12] SA[11] SA[10] SA[9] SA[8] SA[7] SA[6] SA[5] SA[4] SA[3] SA[2] SA[1] SA[0]	Output	197 196 195 194 193 190 189 188 187 184 177 176 175 174 173 172 167 166 165 164	The SRAM Address (SA[19:0]) outputs identify the SRAM location accessed. The sixteen least significant bits (SA[15:0] locate one of a possible 65536 VC Table entries. If 65536 connections are not required, the most significant bits of SA[15:0] may be unconnected with no physical memory associated with the unused memory space. The four most significant bits (SA[19:16]) identify the fields within a VC Table Record. In most applications, SA[19:16] is decoded to SRAM chip selects. Physical memory need not be allocated for unused fields. The SA[15:0] outputs are also used to access the Search Table. The SA[19:0] bus is updated on the rising edge of SYSCLK.
SADSB	Output	181	The SRAM Address Strobe (SADSB) qualifies the address bus. If the SADSB output is asserted low, an SRAM access is initiated. SADSB is updated on the rising edge of SYSCLK.

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SOEB	Output	183	The asynchronous SRAM Output Enable (SOEB) controls the SRAM tri-state outputs. When SOEB is low during a read cycle, the selected SRAM (as determined by SA[19:0] decoding) is expected to drive SD[39:0] and SP[4:0]. SOEB is updated on the rising edge of SYSCLK.
SRWB	Output	182	The SRAM read/write enable (SRWB) determines the SRAM access type. SRWB is qualified by the SADSB output. The RCMP-800 drives the SRWB output high if the subsequent cycle is a SRAM read. The RCMP-800 drives the SRWB output low if the current cycle is a SRAM write. SRWB is updated on the rising edge of SYSCLK.

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Microprocessor Interface Signals (30)

Pin Name	Type	Pin No.	Feature
CSB	Input	78	CSB is low during RCMP-800 Microprocessor Interface Port register accesses. If CSB is not required (i.e. register accesses controlled using the RDB and WRB signals only), CSB should be connected to an inverted version of the RSTB input.
RDB	Input	76	RDB is low during RCMP-800 Microprocessor Interface Port register read accesses. The RCMP-800 drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	77	WRB is low during a RCMP-800 Microprocessor Interface Port register write accesses. The D[15:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
DREQ	Output	75	The DMA request (DREQ) output is asserted when the Microprocessor Cell Buffer contains a cell to be read and the DMAEN bit in the Microprocessor Buffer Configuration register is a logic 1. The first read of the Microprocessor Cell Data register after DREQ is asserted will return the first word of the cell. DREQ is deasserted after the last word of the cell has been read or an abort has been signaled. The polarity of the DREQ output is programmable and defaults to active high.
BUSYB	Output	74	The BUSYB output is asserted while a µP access request to the external SRAM is pending. The BUSYB output is deasserted after the access has been completed. A µP access request is typically completed within 37 SYSCLK cycles. If the STANDBY bit in the Master Configuration is a logic 1, the access time is reduced to less than 5 SYSCLK cycles. The polarity of the BUSYB output is programmable and defaults to active low. The BUSYB should be treated as a glitch-free asynchronous output.

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D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7] D[8] D[9] D[10] D[11] D[12] D[13] D[14] D[15]	I/O	49 50 51 52 57 58 59 60 61 62 63 64 69 70 71 72	The bi-directional data bus D[15:0] is used during RCMP-800 Microprocessor Interface Port register read and write accesses. D[15:8] should contain the most significant byte of a word while D[7:0] should contain the least significant byte of a word.
A[0] A[1] A[2] A[3] A[4] A[5] A[6]/TRS	Input	90 89 88 87 86 85 84	A[6:0] selects specific Microprocessor Interface Port registers during RCMP-800 register accesses. A[6] is the Test Register Select (TRS) address pin. TRS selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses.
ALE	Input	83	ALE is active high and latches the address bus A[6:0] when low. When ALE is high, the internal address latches are transparent. It allows the RCMP-800 to interface to a multiplexed address/data bus. ALE has an integral pull up resistor.
INTB	OD Output	73	The interrupt request (INTB) output goes low when a RCMP-800 interrupt source is active and that source is unmasked. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.

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Misc. Interface Signals (66)

Pin Name	Type	Pin No.	Feature
SYSCLK	Input	147	The system clock (SYSCLK) provides timing for the RCMP-800's internal circuitry. SYSCLK should be nominally a 50% duty cycle 25 MHz to 50 MHz clock. SYSCLK should be connected to the same clock buffer as the external synchronous SRAM clock.
CONG	Input	123	The congestion indication (CONG) input signals that cell congestion is occurring in an element downstream of the RCMP-800 and that all low priority cells be dropped. If CONG is high, the RCMP-800 drops all cells with a one in the CLP bit position after policing has occurred, except AAL5 end-of-message (EOM) cells. (Dropping an EOM cell results in corrupting two packets; this does help to relieve the congestion.) CONG may be treated as an asynchronous input.
ONESEC	Input	81	The one second clock (ONESEC) provides precise timing for events such as the generation of RDI and AIS cell and the clearing of AIS, RDI and Continuity Check alarms. By default, the initiation of one second events is based on the SYSCLK period; therefore, the ONESEC input is ignored. If the SEL1SEC register bit is a logic 1, the ONESEC input becomes the source of the one second clock. ONESEC must be glitch free and may be treated as an asynchronous input.
RSTB	Scmitt Trigger Input Internal Pull-up	82	The active low reset (RSTB) signal provides an asynchronous RCMP-800 reset. RSTB is a Schmitt triggered input with an integral pull up resistor. When RSTB is forced low, all RCMP-800 registers are forced to their default states.
TCK	Input	44	The test clock (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.

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TMS	Input Internal Pull-up	45	The test mode select (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input Internal Pull-up	46	The test data input (TDI) signal carries test data into the RCMP-800 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Tristate	47	The test data output (TDO) signal carries test data out of the RCMP-800 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is tri-stated except when scanning of data is in progress.
TRSTB	Scmitt Trigger Input Internal Pull-up	48	The active low test reset (TRSTB) signal provides an asynchronous RCMP-800 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull up resistor. The JTAG TAP controller must be initialized when the RCMP-800 is powered up. If the JTAG port is not used TRSTB must be connected to the RSTB input or VSS.
VDD_DC1 VDD_DC2 VDD_DC3 VDD_DC4 VDD_DC5 VDD_DC6 VDD_DC7 VDD_DC8 VDD_DC9 VDD_DC10 VDD_DC11 VDD_DC12 VDD_DC13 VDD_DC14 VDD_DC15 VDD_DC16 VDD_DC17 VDD_DC18 VDD_DC19 VDD_DC20	Power	11 31 39 42 53 67 79 94 108 124 127 142 148 157 168 185 200 215 230 239	The DC power (VDD_DC1 - VDD_DC12) pins should be connected to a well-decoupled +5 V DC supply in common with VDD_AC.

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VSS_DC1 VSS_DC2 VSS_DC3 VSS_DC4 VSS_DC5 VSS_DC6 VSS_DC7 VSS_DC8 VSS_DC9 VSS_DC10 VSS_DC11 VSS_DC12 VSS_DC13 VSS_DC14 VSS_DC15 VSS_DC16 VSS_DC17 VSS_DC18 VSS_DC19 VSS_DC20	Ground	12 32 40 43 54 68 80 95 109 125 128 143 149 158 169 186 201 216 231 240	The DC ground (VSS_DC1 - VSS_DC12) pins should be connected to GND in common with VSS_AC.
VDD_AC1 VDD_AC2 VDD_AC3 VDD_AC4 VDD_AC5 VDD_AC6 VDD_AC7 VDD_AC8 VDD_AC9 VDD_AC10 VDD_AC11 VDD_AC12 VDD_AC13 VDD_AC14 VDD_AC15 VDD_AC16	Power	25 37 55 65 98 110 134 150 160 170 178 191 202 211 222 234	The AC power (VDD_AC1 - VDD_AC15) pins should be connected to a well-decoupled +5 V DC supply in common with VDD_DC.
VSS_AC1 VSS_AC2 VSS_AC3 VSS_AC4 VSS_AC5 VSS_AC6 VSS_AC7 VSS_AC8 VSS_AC9 VSS_AC10 VSS_AC11 VSS_AC12 VSS_AC13 VSS_AC14 VSS_AC15 VSS_AC16	Ground	26 38 56 66 99 111 135 151 159 171 179 192 203 212 223 235	The AC ground (VSS_AC1 - VSS_AC18) pins should be connected to GND in common with VSS_DC.

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Notes on Pin Description:

1. All RCMP-800 inputs and bi-directionals present minimal capacitive loading and operate at TTL logic levels.
2. All RCMP-800 digital outputs and bi-directionals have 2 mA D.C. drive capability.
3. Inputs RSTB, TRSTB, TMS, TDI and ALE have internal pull-up resistors.
4. The VSS_DC and VSS_AC ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the RCMP-800.
5. The VDD_DC and VDD_AC power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the RCMP-800.

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FUNCTIONAL DESCRIPTION

The RCMP-800 receives cells from up to 32 PHY devices, processes them, and passes them to a single switch port or queue manager. The RCMP-800 device operates as a multi-PHY master on its input side. Round-robin polling selects between the PHY devices based on the availability of cells.

The Output Cell Interface operates as a single-PHY slave. The RCMP-800 informs the bus master if it has a cell available for transfer out by asserting OCA, and waits for the bus master to assert the ORDENB signal to effect the transfer. If the output buffer becomes full, the RCMP-800 will apply back-pressure to all its input PHYs.

Logical multicasting is possible, although the system design must take into account the fact that the input PHYs may be backed-up as a result - with possible cell loss occurring.

Input Buffering

Cells received on the extended cell format SCI-PHY compatible Input Cell Interface are buffered in a 4 cell deep FIFO. The input buffer provides for the separation of internal timing from asynchronous external devices.

The SCI-PHY cell interface operates at clock rates up to 52 MHz and supports 16 bit and 8 bit wide data structures with programmable lengths. The 16 bit data structure contains 26 (HEC and User Defined Field excluded) or 27 words allocated to carrying an ATM cell and up to 5 appended words. The 8 bit data structure contains a 52 (HEC excluded) or 53 byte ATM cell and up to 10 appended bytes. The start of the data structure is indicated by the ISOC input. Refer to the "Operation" section for more detail on these data structures. The data bus is protected by the IPRTY[1:0] inputs. The parity can be configured to be odd or even. Each parity input can cover a byte or IPRTY[1] can cover all sixteen data inputs.

The input FIFO filters all unassigned cells and cells reserved for the use of the Physical Layer. Unassigned cells are identified by an all zero VPI/VCI value and CLP=0. They are filtered without notification. Physical layer cells are identified by an all zero VPI/VCI value and CLP=1. They are filtered with a resulting maskable interrupt indication and a Physical Layer cell count increment. By default, the cell coding is assumed to be for a Network-Network Interface (NNI); therefore the VPI is taken to be twelve bits. If one of the PHY links is a User-Network Interface (UNI) and the GFC field is non-zero, the cell will not be filtered by the Input Cell Interface, but will be discarded by the VC Identification circuit. As an option, all cells can be interpreted as UNI cells.

The RCMP-800 is a bus master and services the PHY devices in one of two ways: direct status arbitration or address line polling. For direct status arbitration, the RCMP-800 monitors cell available signals (ICA[4:1]) from to up four physical (PHY)

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layer devices and generates write enables (WRENB[4:1]) in response. For address line polling, ICA[1] and IWRENB[1] are shared between up to 32 PHY devices and signals IADDR[4:0] and IAVALID are used to address the latter individually. The RCMP-800 performs round-robin polling of the PHY devices to determine which have available cells. The RCMP-800 will read an entire cell from one PHY device before accessing the next PHY device. No fixed cell slots exist, but instead the RCMP-800 maximizes throughput by servicing a PHY device as soon as the bus is free and PHY device's cell available signal is asserted.

All input FIFO signals, ISOC, IWRENB[4:1], ICA[4:1], IADDR[4:0], IAVALID, IPRTY[1:0] and IDAT[15:0] are either sampled or updated on the rising edge of the IFCLK clock input.

VC Identification

The RCMP-800 makes use of a flexible approach to identify incoming cells and to determine which record in the VC Table they are associated with. The RCMP-800 is able to identify each cell's VC by searching the *VC Search Table* (see Table 1) using selected portions of the cell header, prepend, postpend along with the cell's PHY address. To do this, the RCMP-800 creates an internal *Routing Word* which is the concatenation of the cell header, cell prepend and cell postpend. The RCMP-800 is programmed to select portions of the Routing Word plus the PHY address to create a *VC Search Key*. The VC Search key, therefore, consists of portions of the cell's header, prepend, postpend and SCI-PHY address. See Figure 3.

Figure 3 is not intended to imply any restrictions on the positioning of Field A and Field B. These fields may occur any where within the appended octets or the ATM header. The Primary Key and Secondary Key may also intersect.

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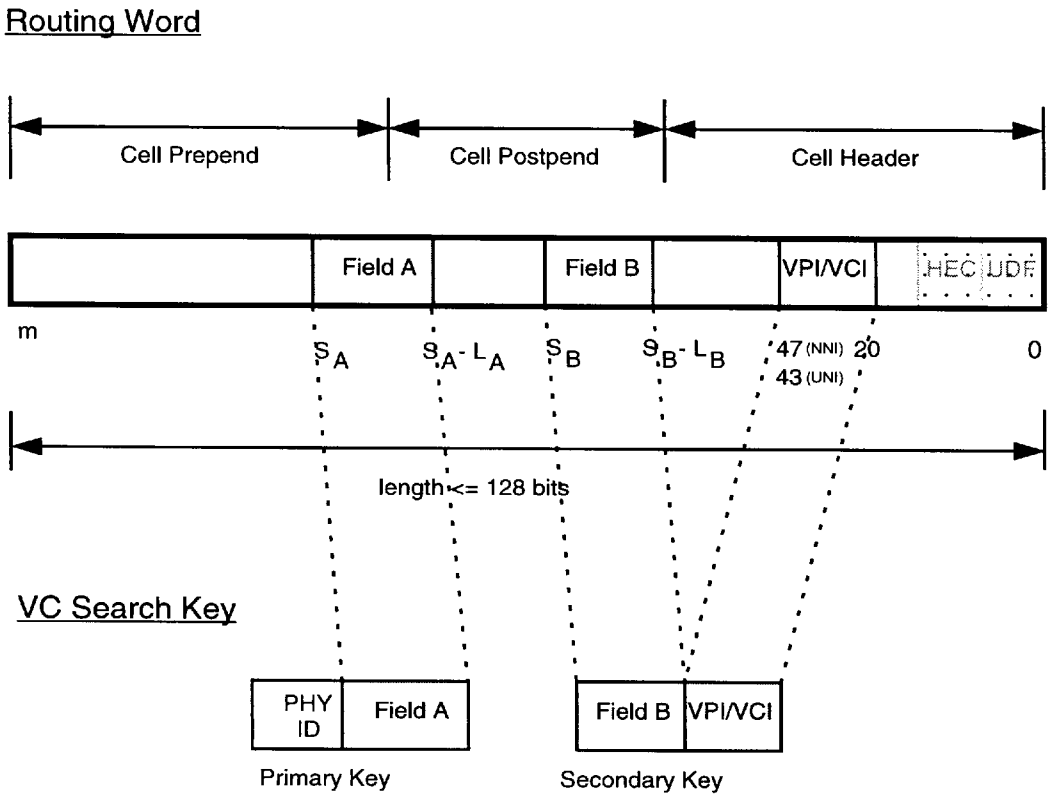
Fig. 3 VC Search Key Composition



The RCMP-800 divides the VC Search Key into two search keys - the Primary Search Key and the Secondary Search Key. The Primary Key is 0 to 16 bits long. It is constructed from two fields - the *PHY ID* and *Field A*. The PHY ID field and Field A can be programmed to be 0-5 bits and 0-16 bits long, respectively. The PHY ID is the SCI-PHY address and must, therefore, include sufficient bits to encode all the PHYs at the PHY Layer interface of the RCMP-800. Field A starts at location S_A of the Routing Word and has length L_A. The number of bits in Field A plus the number in the PHY ID field must be less than or equal to 16.

The Secondary Search Key is 39 bits long and is composed of two fields. The first field, *Field B*, is 0 to 11 bits long and may start anywhere in the routing word. Field B parameters include starting position S_B, and length L_B. The second field is the 28 bit VCI/VPI. This field is always taken from the cell's header.

Field B and the VPI/VCI field are positioned "right justified" within the routing word.

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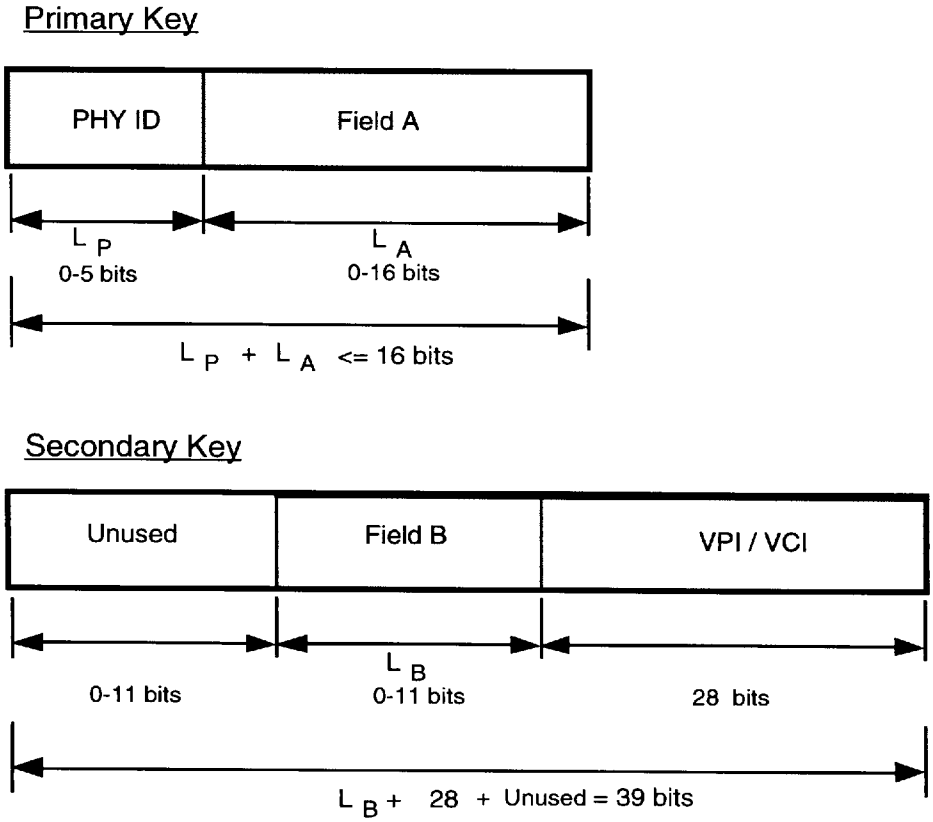
Fig. 4 Parameters of Primary Key and Secondary Key



The user can program the RCMP-800 with the length and position parameters of fields A and B. Refer to the descriptions for registers 0x28 and 0x29.

Figure 5 provides a representation of how the RCMP-800 creates the Primary and Secondary search keys. Field location and length registers are used to select Field A and Field B from the routing word. Field A and the PHYID are concatenated to form the Primary Search Key. Field B and the VPI/VCI field are concatenated to form the secondary search key.

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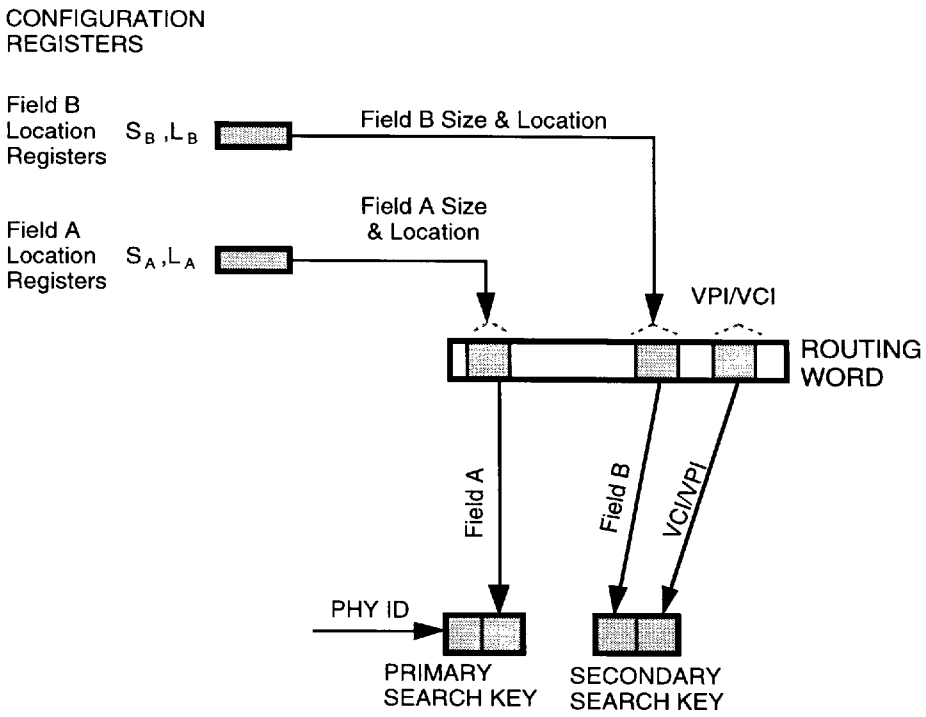
Fig. 5 Construction of Search Keys



Once the search keys are assembled, the Primary Search Key is first used to address an external direct look-up table (*Primary Table*). This table occupies 2^n memory locations where $n = L_P + L_A$, i.e. the length of the Primary Search Key. The result of this direct look up is the address of a root node of a search tree. From this root node, the Secondary Search Key is used by a patented search algorithm to find the cell's VC Table address (held in external SRAM.) The RCMP-800 requires this table address for cell processing. Table 1 provides a description of the VC Table. If the search process does not lead to the successful identification of the cell concerned (contents of the VC table address returned do not match the Secondary Search Key contents), the cell is discarded as invalid. Optionally, the cell is routed to the microprocessor cell interface for header error logging.

The length of time required to perform the VC search is variable. Since the Primary Search Key is used in a direct look up, only one cycle is required to process the Primary Key. The Secondary Search Key processing time is highly dependent on the key's contents, but the maximum number of processing cycles required is equal to the number of bits in the Secondary Search Key which must the examined to make a unique identification. Some VPI and VCI bits may always be zero; therefore, they need not be used in the search. In some instances, the Primary Search Key may overlap the Secondary Search Key; therefore, the intersecting bits are only required for the confirmation of a search and will not be used as decision points by the binary search. If the number of bits used by the binary search is no greater than

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18, a sustained rate of 1.42×10^6 cell/s is guaranteed. The general expression for guaranteed throughput is

$$\text{Throughput} = \frac{1}{(17 + \text{max.binary tree depth})(\text{SYSCLK period})} \text{cell / s}$$

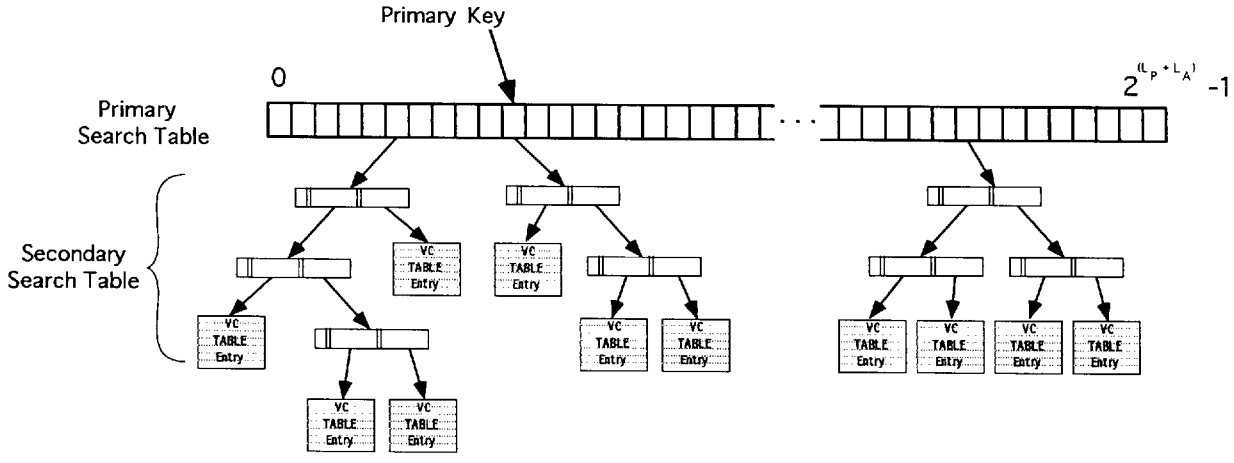
The first two words of each VC Table Record are reserved for the primary table and the search table. The third word of the VC Table Record contains the Secondary Search Key and an "NNI" bit in the most significant bit position. This word is used to confirm whether the incoming cell belongs to a provisioned virtual connection. Any unused bits within this word must be set to zero. The NNI bit identifies if the VC belongs to a Network-Network Interface. If the NNI bit is set to zero, the connection is part of a UNI which means that the four MSBs of the VPI are excluded from the secondary key verification. If the VCI field in the VC Table is all zeros, this signifies the connection is a VPC and that the VCI field is to be ignored.

Search Table Data Structure

The Primary and Secondary Search Tables reside in external SRAM. The Primary Search Table is located in the least significant 16 bits of RAM locations with SA[19:16]=0001 and requires $2^{(L_P + L_A)}$ words of memory. The Secondary Search Table resides in RAM locations with SA[19:16]=0000 and its size is bounded by the number of virtual connections supported.

Figure 6 illustrates the relationship between the Primary Search Table, Secondary Search Table and the VC Table.

Fig. 6 Data Structures



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The following gives the immutable coding rules for the search data structures. The coding supports numerous possible algorithms, but the Operations Section presents an algorithm which is optimized for most applications.

Primary Search Table

The Primary Search Table contains an array of pointers which point to the roots of binary trees. The table is directly indexed by the contents of the Primary Search Key, as defined above.

The entire Primary Search Table must be initialized to all zeros. A table value of zero represents a null pointer; therefore, the initial state means no provisioned connections are defined. If a connection is added which results in a new binary search tree (i.e. It is the only connection associated with a particular Primary Search Key.), the appropriate Primary Search Table location must point to the newly created binary search tree root. If the last connection associated with a particular Primary Search Key is taken down, the associated Primary Search Table location must be set to all zeros.

Secondary Search Table

The Secondary Search Table consists of a set of binary search trees. Each tree's root is pointed to by an entry in the Primary Search Tree. Each node in the tree is represented by a 40 bit record contained at SA[19:16]=0000, which is encoded as follows:

MSB LSB

SD[39:34]	SD[33]	SD[32:17]	SD[16]	SD[15:0]
Select	Left Leaf	Left Branch	Right Leaf	Right Branch

Select — The index of the Secondary Search Key bit upon which the branching decision is based. An index of zero represents the LSB. If the selected bit is a logic one, the "Left Leaf" and "Left Branch" fields are subsequently used. Likewise, if the selected bit is a logic zero, the "Right Leaf" and "Right Branch" are subsequently used. Typically, the Select value decreases monotonically with the depth of the tree, but other search sequences are supported by the flexibility of this bit.

If a VC belongs to a multicast, the select field is set to an all ones pattern, except the last in the linked list. For a multicast entry, the Left_Branch gives the VC table address of the multicast VC (the Left Leaf is always '1'). The Right_Branch points to the Search Table address of the next VC in the multicast. The VC search table therefore forms a linked list and may multicast an arbitrary number of cells. The linked

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	list is terminated by setting the Select field to value that is not all ones. A non all ones value in the Select field instructs the search engine that the Left_Branch field provides the final VC Search Table Address of the multicast set.
Left Leaf	This flag indicates if this node is a leaf. If "Left Leaf" is a logic one, the left branch is a leaf and the binary search terminates if the decision bit is a logic one. If "Left Leaf" is a logic zero, "Left Branch" value points to another node in the binary tree. If the VC pointed to by the Left Branch is the first VC in a multicast set, the Left_Leaf must be set to a logic 1. For the remaining VCs in the multicast set, the Left Leaf value is arbitrary, but it is recommended to be set to a logic 1 for future compatibility.
Left Branch	The pointer to the node accessed if the decision bit is a logic one. If "Left Leaf" is a logic one, "Left Branch" contains the SA[15:0] address identifying the VC Table Record for the candidate connection. If "Left Leaf" is a logic zero, "Left Branch" contains the SA[15:0] value pointing to another Secondary Search Table entry. If the Search Table entry is part of a multicast linked list, the Left Branch is the VC Table address of one VC in the multicast.
Right Leaf	This flag indicates if this node is a leaf. If "Right Leaf" is a logic one, the Right branch is a leaf and the binary search terminates if the decision bit is a logic zero. If "Right Leaf" is a logic zero, "Right Branch" value points to another node in the binary tree. If the VC pointed to by the Left Branch belongs to a multicast set, the Right_Leaf value is arbitrary, but it is recommended to be set to a logic 0 for future compatibility.
Right Branch	The pointer to the node accessed if the decision bit is a logic zero. If "Right Leaf" is a logic one, "Right Branch" contains the SA[15:0] address identifying the VC Table Record for the candidate connection. If "Right Leaf" is a logic zero, "Right Branch" contains the SA[15:0] value pointing to another Secondary Search Table entry. If the Search Table entry is part of a multicast linked list (except the last element of the list), the Right Branch is the Search Table address of the next element in the list. If the

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Search Table entry is the last element in the linked list, this field is arbitrary.

The above encoding defines the binary search tree recursively.

The following special cases must be respected:

1.) A binary tree with only one connection must have both the Left and Right Branches pointing to the solitary VC Table Record. Both Leaf flags must be a logic one.

2a.) If the Primary Search Table is not used (i.e. $L_P = L_A = 0$), the root of the single resulting binary search tree must be located at the Secondary Search Table entry at SA[15:0]=0x0000.

2b.) If the Primary Search Table is in use, no root node shall use location SA[15:0]=0x0000, although this location may be used for nodes at least one level down. A value of 0x0000 in the Primary Search Table represents a null pointer.

Cell Processing

After a VPI/VCI search has been completed for a cell, the resulting actions are dependent upon the cell contents and the VC Table Record. Particular features such as policing and OAM cell processing can be disabled on a global basis.

The VPI/VCI search results in a SA[15:0] value which points to a VC Table Record. Table 1 illustrates the fields for each VC Table Record. A description of each field is given below. If fewer than 32768 connections are supported, the most significant bits of SA[15:0] and the associated memory may not be required. The individual fields of the VC Table Record are accessed by the SA[19:16] outputs. If particular features are disabled, the associated fields are unused and no memory need be provided for them.

When a new VC is provisioned, the microprocessor must initialize the contents of the VC Table Record. Refer to the External RAM Address (MSB) and Access Control register description for details on access control. Once provisioned, the microprocessor can retrieve the contents of the VC Table Record.

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Table 1 VC Table Record

SA[19:16]	MSB(39)						LSB(0)
0000	Reserved for Search Table						
0001	MSN (8)		TUC (16)		Reserved for Search Table (16)		
0010	NNI (1)	Search FieldB (11)	VPI (12)		VCI (16)		
0011	Status (4)	Config (6)	Extended Status (9)	OAM Config (8)	UDF (8)	BWD Routing Tag (5)	
0100	L#1 (12)		TAT#1 (28)				
0101	L#2 (12)		TAT#2 (28)				
0110	I#2 (20)			I#1 (20)			
0111	Unused (1)	COCUP (1)	POLflag (2)	Action#1 (2)	Action#2 (2)	non-compliant cell count #2 (16)	non-compliant cell count #1 (16)
1000	Output Header (40)						
1001	Pre/Post pend (40)						
1010	Pre/Post pend (40)						
1011	Unused (8)		CLP=0 cell count (32)				
1100	Unused (8)		CLP=1 cell count (32)				
1101	PM Config(8)		current cell count (16)		BIP16 (16)		
1110	Backward Reporting Counts SECB(8), Lost Cells (12), Misinserted Cells (8), BIPV (12)						
1111	Forward Monitoring Counts SECB(8), Lost Cells (12), Misinserted Cells (8), BIPV (12)						

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Configuration and Status

Configuration and Status fields are available at locations SA[19:16]=0011 and 0111.

The Configuration field allows each connection to be independently provisioned:

Bit	Name	Definition
5	CONTYP	The connection type. If this bit is 1, the VC is an ABR connection. Otherwise, the VC is a VBR/CBR connection. This bit affects the choice of Cell Rate Policing Configuration Registers. When CONTYP is 1 (an ABR connection), the ABR Cell Rate Policing Configuration registers are used by the policing processor, when CONTYP is 0, the VBR/CBR Cell Rate Policing registers are used by the policing processor.
4	DROPUP	Indicates that this VC should be output to the Microprocessor Cell Interface only (not to the Output Cell Interface). Otherwise, the VC is presented on Output Cell Interface (provided it is not a cell which is filtered by the Routing Configuration Register).
3	AAL5	Identifies the VC as an AAL Type 5 Connection. This enables AAL5 packet discard/tagging.
2	Active	Identifies the VC as an active connection. If this bit is set to 1, the VC is an active connection. Otherwise the VC is an inactive connection. The bit is checked during one-second servicing to determine if the connection is still active. It is the responsibility of the microprocessor to set and clear this bit during activation and deactivation, respectively, of a connection.
1	Count User	If this bit is set, the CLP=0 and CLP=1 cell counts include user information cells.
0	Count OAM	If this bit is set, the CLP=0 and CLP=1 cell counts include OAM and RM cells.

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The Status field provides a single location for the fast determination of the connection state:

Bit	Name	Definition
3	AIS	This bit becomes a logic 1 upon the receipt of a single AIS cell. The alarm status is cleared upon the receipt of a single user cell or continuity check cell or if no AIS cell has been received within the last 3.5 +/- 0.5 sec (default) or 2.5 +/- 0.5 sec. The threshold is set by the AISRDIThresh bit of the Performance Monitoring Configuration 1 register (0x19).
2	RDI	This bit becomes a logic 1 upon the receipt of a single RDI cell. The bit is cleared if no RDI cell has been received within the 3.5 +/- 0.5 sec (default) or 2.5 +/- 0.5 sec. . The threshold is set by the AISRDIThresh bit of the Performance Monitoring Configuration 1 register (0x19).
1	CC_alarm	This bit is a logic 1 if no user, AIS or continuity check cells have been received in the latest 5.5 +/- 0.5 sec (default) or 3.5 +/- 0.5 sec seconds. The threshold is set by the CCThresh bit of the Performance Monitoring Configuration 1 register (0x19).
0	POLICE	This bit is a logic 1 if at least one cell has violated the traffic contract. This bit is not cleared upon a read; it must be cleared explicitly by writing to its location.

The Extended Status and POLflag fields contain connection state information. The POLflag field should be initialized to all zeros and the Extended Status field should be set to 0x050 during connection provisioning.

Header Translation

Any appended octets (used by non-standard PHY devices or in special applications) in incoming cells are removed after they have been used for VC identification. Once VC identification has been made, new octets contained in the VC table can be appended to each cell.

The new appended octets are contained in locations identified by SA[19:16]=0011, 1001 and 1010. Substitution of appended octets can be disabled by clearing the GPREPO bit of the Cell Processor Configuration register. If the 16 bit bus format is configured on the Output Cell Interface, the eight bit UDF field in the SA[19:16]=0011 word is placed in the user defined octet following the HEC octet location. If the 8 bit bus format is configured on the Output Cell Interface, the eight bit UDF field in the SA[19:16]=0011 word is not used. All other appended octets are sequenced in the extended cell format SCI-PHY data structure starting with the most

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significant octet of SA[19:16]=1001. Physical memory need not be provided for all octets if the SCI-PHY cell is less than 63 octets.

The header contents of each cell can be altered. The location accessed by SA[19:16]=1000 contains the new header. The forty bit field contains the entire header, although not all bits are required for all connections. The VPI portion, the VCI portion, or both can be replaced with new values recovered from the VC table once VC identification has been made. Substitution of VPI/VCI contents can be disabled by clearing the GVPIVCI bit of the Cell Processor Configuration register. The PTI field is not modified by the translation process. If the connection is a Virtual Path (i.e. the VCI value in the search key is coded as all zeros), the VCI field is passed through transparently. As a globally configurable option, the GFC field in UNI cells can be left unmodified; otherwise, it is replaced by the four most significant bits of the output header word.

Cell Routing

Each generated reverse flow cell which is presented by the Output Cell Interface may have the Backward Routing tag of the VC table inserted in its header (i.e. overwrite a byte of the header). The Backward Routing tag of the VC table is at SA[19:16] = 0011. The appended byte or header byte to be overwritten is programmable. As an option, the VPI/VCI combination may equal the incoming VPI/VCI instead of the translated value.

The destination of each OAM cell depends on the type of OAM cell and whether the RCMP-800 is the end-point for that particular OAM flow. If the RCMP-800 is not an end point, the OAM cell is routed to the same destination as the user cells. If the RCMP-800 is an end point, the default configuration terminates and processes all OAM cells except Activate/Deactivate and Loopback cells, which are routed to either the Output Cell Interface or the Microprocessor Cell Interface.

Cell Rate Policing

The RCMP-800 supports two approximations to the Generic Cell Rate Algorithm (GCRA) for each connection. The rate policing operation is performed according to the Virtual Scheduling Algorithm presented in Annex 1 of ITU-T Recommendation I.371 and the ATM Forum UNI 3.0. To allow full flexibility, the GCRA1 and GCRA2 bit vectors in the ABR Cell Rate Policing Configuration (0x1A) and VBR/CBR Rate Policing Configuration (0x1B) registers allow each instance to police many combination of cells: user cells, OAM cells, Resource Management cells (for ABR connections only), high priority cells or low priority cells. The connection type (ABR or VBR/CBR) is determined on a per-VC basis as programmed in the VC table.

The Limit (L#1 and L#2) and Increment (I#1 and I#2) fields in the VC Table must be initialized before policing is enabled. These fields are related to the traffic contract parameters as follows:

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$$I = \frac{1}{PCR(\Delta t)}$$

$$L = \frac{\tau}{\Delta t}$$ where Δt = time quantum (s)

PCR = Peak Cell Rate (cell/s)

τ = Cell Delay Variation (s)

For a Sustained Cell Rate (SCR) conformance definition, the parameters relate as follows:

$$I = \frac{1}{SCR(\Delta t)}$$ where SCR = Substained Cell Rate (cell/s)

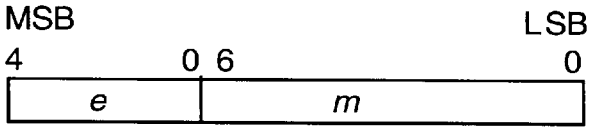
MBS = Max. Burst Size at the Peak Cell Rate (cells)

BT = Burst Tolerance (s)

$$L = \frac{BT}{\Delta t} = \frac{(MBS - 1)(\frac{1}{SCR} - \frac{1}{PCR})}{\Delta t}$$

The time quantum (Δt) can be programmed to be an 1, 2, 4 or 8 multiple of the SYSCLK period. With a 50 MHz clock, Δt is 20, 40, 80 or 160 ns.

In order to compensate for the potentially large CDV and Burst Tolerance limits anticipated in ATM networks, the Limit fields, L#1 and L#2, are encoded as floating-point values, while all other policing parameters are fixed-point values. The Limit fields are encoded as follows:



where *e* is the 5-bit exponent and *m* is the 7-bit mantissa. The value of the Limit field is computed as:

$$L = m \bullet 2^e$$

It is important to note that since the Limit field is a floating-point number, its maximum value exceeds the maximum TAT (268435455) value; therefore, L should not exceed this value. If the encoded value of L is greater than TATmax, then L shall be taken to be TATmax, i.e.

$$L \leq TAT_{max}$$

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To maximize resolution, the limit field should be encoded as a normalized floating-point number (i.e. the mantissa is MSB justified).

The value of Δt and the range of I and L determine the lowest PCR that can be policed, the PCR granularity supported at the highest expected PCR and the largest CDV expected:

$$PCR_{\min} = \frac{1}{I_{\max}\Delta t}$$

granularity (as a fraction of PCR) = $PCR\Delta t$

$$\tau_{\max} = L_{\max}\Delta t$$

With a 20 bit increment field, I_{max} is 1048575; therefore, the smallest peak rate (or sustainable rate) supported is

$$PCR_{\min} = \begin{cases} 47.7 \text{ cells/s} : \Delta t = 20\text{ns} \\ 23.8 \text{ cells/s} : \Delta t = 40\text{ns} \\ 11.9 \text{ cells/s} : \Delta t = 80\text{ns} \\ 5.96 \text{ cells/s} : \Delta t = 160\text{ns} \end{cases}$$

As described previously, the limit field, L, is a 12-bit floating-point field, with $L_{max} = 268435455$ (which is equal to TAT_{max}). Therefore

$$CDV_{\max} = \begin{cases} 5.36\text{s} : \Delta t = 20\text{ns} \\ 10.7\text{s} : \Delta t = 40\text{ns} \\ 21.4\text{s} : \Delta t = 80\text{ns} \\ 42.8\text{s} : \Delta t = 160\text{ns} \end{cases}$$

With a maximum expected cell rate of 353,207 cell/s (which is the bandwidth of an STS-3c/STM-1) and a time quantum of 20ns, the granularity of the policed rate is 0.71% of the peak rate.

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The action taken on a non-conforming cell is programmed on a per VC basis by the "Action[1:0]" field:

Action[1:0]	Definition
00	Set the POLI status bit but take no other action other than to increment the appropriate non-compliant cell count..
01	Reduce the priority of high priority cells.
10	Reduce the priority of high priority cells and discard low priority cells.
11	Discard all non-conforming cells.

Policing can be effectively disabled for a connection if the increment fields (I#1 and I#2) are set to all zeros.

The RCMP-800 performs its conformance tests sequentially. That is, GCRA1 is executed before GCRA2. In the event that a cell violates GCRA1, the actions of Action1[1:0] are performed on that cell. If the cell is not discarded as a result of this action, the modified cell (e.g. tagged cell) is passed to GCRA2. If the cell is discarded as a result of violating GCRA1, the cell is not passed on to GCRA2, and the policing parameters for GCRA1 and GCRA2 are not updated.

In general, if a GCRA fails, its TAT parameter is not updated. However, a coupling can be introduced between the update actions of GCRA1 and GCRA2. To allow for this contingency, the COCUP (COnditional Conformance UPdate) bit of the VC table can be set appropriately. If COCUP = 0, the update of GCRA1 and GCRA2 TAT parameters are completely independent. That is, the conformance or non-conformance of one GCRA has no effect on the other. If COCUP = 1, however, the GCRA1 TAT parameter update is dependent on the conformance to GCRA2. Thus, if a cell is compliant to GCRA1, the TAT parameter for GCRA1 shall be updated if and only if the cell is also compliant to GCRA2.

Two non-compliant cell counts are maintained based upon one of the following programmable definitions, as determined by the state of the NCOMP[1:0] register bits in the VBR/CBR Cell Rate Policing Configuration register:

1.) Non-compliant CLP=0 cells and non-compliant CLP=1 cells.

2.) Dropped CLP=0 cells and dropped CLP=1 cells.

3.) Cells which are non-compliant with GCRA#1, and cells compliant with GCRA#1 which are non-compliant with GCRA#2.

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4.) Cells which are non-compliant with GCRA#1, and cells which are non-compliant with GCRA#2

AAL5 Packet Tagging and Dropping

An AAL5 packet can be up to 1366 cells long. If a cell is dropped early in a packet due to policing or congestion, then the remaining cells of the packet represent wasted bandwidth. Optionally, all remaining cells of a packet can be dropped or tagged once a single cell has been dropped or tagged.

On a per-VC basis, the RCMP-800 has a configuration bit indicating the AAL as Type 5 and two status bits that indicate a cell within the packet has violated either or both of the GCRAs. For each cell received on an AAL5 connection, if either of the status flags are set, the actions dictated by the appropriate ACTION field will be taken on the remainder of the packet. The policing parameters for that GCRA will not be updated. If an EOM (SDU_type=1) cell is received, the cell is passed on and the status bits are cleared.

The CLP=0, CLP=1 and non-compliant cell counts are updated for all cells of an AAL5 packet.

Cell Counting

The RCMP-800 maintains counts on a per VC basis and over the aggregate cell stream.

The following parameters are stored on a per VC basis:

- number of low priority cells
- number of high priority cells
- non-compliant cell counts (user programmable)

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The number of cells discarded by the policing function and the number of cell reduced from high to low priority can be derived from the above counts , the state of the Action1[1:0] and Action2[1:0] fields, and the state of the NCOMP[1:0] register bits.

In order to maintain accurate non-compliant cell counts in the VC table, the RCMP-800 asserts a maskable interrupt whenever the most significant bit is set for either of the non-compliant cell counts. This allows an external microprocessor to read the counts to prevent saturation.

The low and high priority cell counts represent the state of the cells before policing. The non-compliant cell counts can be used to derived the cell counts after policing.

To provide the ability to provision scheduled measurements and special studies, each VC can be programmed to count either user information cells, OAM (including Resource Management) cells or both.

If performance monitoring is activated, the following forward monitoring and backward reporting parameters are stored on a per-VC basis:

- number of lost cells
- number of misinserted cells
- number of BIP-16 errors
- number of Severely Errored Cell Blocks (SECB)

Each of the per VC values is cleared upon a microprocessor read access to its location.

The following parameters cover the aggregate cell stream:

- number of cells received at the Input Cell Interface
- number of cells transferred through the Output Cell Interface
- number of valid OAM cells received
- number of OAM cells with an incorrect CRC-10, undefined OAM Type or undefined Function Type
- number of cells with errored headers. These include cells with unassigned/invalid VPI/VCIs or invalid PTI values
- number of CLP=1 cells dropped due to congestion
- number of physical layer cells received

Events are accumulated over consecutive intervals as defined by the period of the microprocessor initiated data latching. The RCMP-800 maintains current counts and holding registers. A latching event transfers the counter values into holding registers and resets the counters to begin accumulating events for the next interval. The counters are reset in such a manner that events occurring during the reset are not missed. The holding registers can be read via the microprocessor interface.

All counts saturate at all ones and will not roll over.

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Operations, Administration and Maintenance (OAM) Cell Servicing

The RCMP-800 is capable of terminating and monitoring F4 and F5 OAM flows. Complete processing of Fault Management, Performance Management (PM) and Continuity Check cells is provided. Activate/Deactivate and Loopback cells are passed to the Microprocessor Cell Buffer or the Output Cell Interface for external processing.

For the case of OAM processing, the following applies:

1. If the RCMP-800 is configured as a sink of PM cells, then the BIP-16, current cell count, MSN, TUC, forward statistics and backward statistics are updated independent of the outcome of cell policing.

2. If the RCMP-800 is configured as a source of PM cells, then the BIP-16, current cell count, MSN and TUC are updated dependent of the outcome of cell policing. That is, those fields are updated if and only if the cells are not discarded by the RCMP-800.

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The contents of the OAM Configuration field at SA[19:16]=0011 determine the RCMP-800's behavior with respect to a particular connection:

Bit	Name	Action if a logic 1
7	CC_RDI	Setting this bit enables the sending of RDI cells at one second intervals upon the declaration of a Continuity Check alarm at a termination point (i.e. the CC_alarm bit is set).
6	BACKRPT	Enables the generation of backward report cells. A backward report cell is output for each forward monitoring cell received at an OAM flow end-point if the SRCPM bit is a logic 0.
5	Send_AIS	Sends an AIS cell once per second. The cells genrated are encoded as End-to-End AIS cells.
4	Send_RDI	Sends an RDI cell once per second. The cells genrated are encoded as End-to-End RDI cells.
3	End_pt	Defines the RCMP-800 as an End-to-End termination point. For VPCs, all cells with VCI=4 are dropped and processed. For VCCs, all cells with PT=101 are dropped and processed.
2	Seg_end_pt	Defines the RCMP-800 as a Segment termination point. For VPCs, all cells with VCI=3 are dropped and processed. For VCCs, all cells with PT=100 are dropped and processed.
1	PM_activate	Enables performance management. PM cells are either sourced or monitored.
0	CC_activate	Enables Continuity Checking. If no user or AIS cell is received over a 1 or 2 (default) second window, a Continuity Check OAM cell is generated. The CC cell generation interval set by the CCThresh bit of the Performance Monitoring Configuration 1 register (0x19).

Upon receipt of an OAM cell, the CRC-10 is checked. If the check sum is incorrect, the OAM cell is not processed and the global errored OAM cell count is incremented. Otherwise, further processing is dependent upon the contents of the OAM Cell Type field.

If a connection is not provisioned as an end point, all incoming OAM cells are passed to the Output Cell Interface (subject to policing) regardless of whether the OAM Type or the Function Type fields have defined values. As an option, OAM cells may be discarded at non flow end-points if the CRC-10 is incorrect. At flow end-points all OAM cells are terminated, except Activate/Deactivate and Loopback cells whose handling is specified by the Routing Configuration register. If the UNDEFtoUP bit of the Routing Configuration register is a logic 1, all undefined OAM cells are routed to the Microprocessor Cell Interface for further processing or error

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logging. If the CNTUNDEF bit in the CRAM Configuration register is a logic 1, the Errored OAM Cell Count register is incremented for each cell with an undefined OAM Type or Function Type value.

The PM Configuration field (SA[19:16] = 1101) provides various PM related functions:

Bit	Name	Definition
7	$SECB_{LOST}$	This status bit indicates that a forward LOST cell count exceeded the MLOST[7:0] threshold and resulted in the declaration of a SECB. This bit is cleared upon a microprocessor read of location SA[19:16] = 1101.
6	$SECB_{MISINS}$	This status bit indicates that a forward MISINSERTED cell count exceeded the MMISINS[7:0] threshold and resulted in the declaration of a SECB. This bit is cleared upon a microprocessor read of location SA[19:16] = 1101.
5	$SECB_{BIPV}$	This status bit indicates that a forward BIPV cell count exceeded the MERROR[4:0] threshold and resulted in the declaration of a SECB. This bit is cleared upon a microprocessor read of location SA[19:16] = 1101.
4:3	BLKSIZE[1:0]	If the RCMP-800 is configured as a source of PM cells (SRCPM = 1, PM_activate = 1, and the RCMP-800 is configured as a flow-end-point), the BLKSIZE[1:0] bits select the nominal number of user cells per performance monitoring block. BLKSIZE[1:0] User cells per block 00 1024 01 128 10 256 11 512
2	PM_TYP	The PM_TYP bit determines whether end-to-end PM cells or segment PM cells are relevant to the connection. If PM_TYP is a logic 1, end-to-end PM cells will be generated (if SRCPM is a 1) or they will be analyzed (if SRCPM is a 0). If PM_TYP is a logic 0, segment PM cells will be sourced or analyzed.

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1	SRCPM	This bit provisions the RCMP-800 as a source of forward monitoring cells for the connection. Setting the SRCPM bit and PM_activate bit to logic 1 results in the presention of a forward monitoring cell on the Output Cell Interface at an interval selected by the BLKSIZE[1:0] bits. If the SRCPM bit is 0, no monitoring cells are generated, which frees up resources so that statistics can be collected for incoming monitoring cells.
0	PM0	The PM0 bit of the VC table must be set to '1' initially. This bit is cleared upon receiving the first PM cell. This clears the current cell count and BIP16. The PM0 bit is used to note the arrival of the first PM cell. The PM0 bit suppresses accumulation of error counts. If this bit is not set, errors counts will be accumulated.

Fault Management Cells

Fault Management cells are identified with an OAM Cell Type of 0001. Four types are currently supported: AIS, RDI, Continuity Check and Loopback.

An AIS alarm status bit is set upon the receipt of a single AIS cell (function type=0000). The alarm status is cleared upon the receipt of a single user cell or continuity check cell or if no AIS cell has been received within the last 3.5 +/- 0.5 sec (default) or 2.5 +/- 0.5 sec. If the AUTORDI bit in the Cell Processor Configuration register is set, an RDI cell is generated immediately upon the reception of the first AIS cell at a flow end-point and once a second thereafter until the AIS state is exited.

An RDI alarm status bit is set upon the receipt of a single RDI cell (function type=0001). The alarm status is cleared if no RDI cell has been received within the last 3.5 +/- 0.5 sec (default) or 2.5 +/- 0.5 sec.

If the "CC_activate" bit is a logic 1 and no user cells have been received within a one or two (default) second window, a Continuity Check cell is generated and passed to the Output Cell Interface. Regardless of the state of the "CC_activate" bit, if no user or Continuity Check cells are received within a 5.5 +/- 0.5 sec (default) or 3.5 +/- 0.5 sec window, the "CC_alarm" status bit is set. The "CC_alarm" is cleared upon reception of a single user or Continuity Check cell. If the AUTORDI bit in the Cell Processor Configuration register is set and the "CC_RDI" bit of the OAM Configuration field is set, an RDI cell is presented on the Output Cell Interface once a second while the Continuity Check alarm is declared.

The RCMP-800 provides support for processing of loopback cells by a microprocessor. The LB[1:0] bits of the Routing Configuration register determine which loopback cells are copied to the Microprocessor Cell Interface: all, none or just at OAM flow end-points. If the RCMP-800 is not an OAM flow end-point, all received loopback cells are routed to the Output Cell Interface.

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If the Loopback Indication is non-zero and the Loopback Location ID matches this node (coded as all '1's for flow end-points), the microprocessor should insert into the reverse direction a copy of the loopback cell with the Loopback Indication set to '0'. Otherwise, the microprocessor should discard the cell.

Performance Management Cells

Performance Management (PM) cells are identified with a OAM Cell Type of 0010.

If the RCMP-800 is not the flow end point, the PM cells are passed to the Output Cell Interface and can be monitored to generate alarms or statistics. If the RCMP-800 is provisioned as a flow end point, a received PM cell is unconditionally dropped. If the "PM_activate" bit is a logic 0 or the SRCPM register bit is logic 1, no further actions are taken.

As a flow end point, the RCMP-800 can be provisioned as source or sink of PM cells for a specific connection, but not both. If provisioned as a source (i.e. the SRCPM and the PM_activate VC table bits are both logic 1), the RCMP-800 shall generate a forward PM cell nominally every 128, 256, 512 or 1024 user cells. The contents of the cell fields are as follows:

Monitoring Sequence Number (MSN) - This field is incremented with each transmitted PM cell.

Total User Cell Number (TUC) - This field indicates the total number of transmitted user cells modulo 65536 before the monitoring cell.

Block Error Detection Code - This field is the even parity BIP-16 error detection code computed over the information field of the block of user cells transmitted after the last monitoring cell.

Time Stamp - The default of all ones is inserted.

Block Error Result - The generated cell is a forward monitoring cell; therefore, this field is coded as 6AH.

Lost/Misinserted Cell Count - The generated cell is a forward monitoring cell; therefore, each byte of this field is coded as 6AH.

A backward reporting cell is output for each forward monitoring cell received at an OAM flow end-point if the BACKRPT bit is a logic 1 and the SRCPM bit is a logic 0.

The PM0 bit of the VC table must be set to '1' initially to suppress the accumulation of error counts upon the arrival of the first forward Performance Management cell. This bit is cleared upon receiving the first PM cell.

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If the RCMP-800 is a sink of PM cells, all received user cells result in updating of the current cell count and BIP16 fields of the VC table. If the RCMP-800 is a source of PM cells, only user cells which are not discarded by the UPC function result in an updating of the current cell count and BIP16 fields of the VC table. For the purposes of Performance Management at the F4 (VPC) level , cells with VCI values of 1, 2, 5 or ≥16 are considered user cells. For the purposes of Performance Management at the F5 (VCC) level, cells with PTI values of 000 through 011 are considered user cells.

If the "PM_activate" bit is a logic 1 and the RCMP-800 is not the source of monitoring cells (i.e. the SRCPM VC table bit is logic 0), the fields of received Forward Monitoring and Monitoring/Reporting cells are compared with the accumulated data for the block of user cells since the latest PM cell. Receipt of a monitoring cell results in the updating of the statistics located at SA[19:16]=1111:

Lost Cell Count - The Lost Cell Count is incremented by the number of lost cells if the number of received cells in the block is less than the number that are expected based on the contents of the TUC field. If the number of lost cells equals or exceeds the threshold set by the MLOST[7:0] register bits, the SECB count is incremented and the lost cell accumulation is suppressed.

Misinserted Cell Count - The Misinserted Cell Count is incremented by the number of misinserted cells if the number of received cells in the block is more than the number that are expected based of the contents of the TUC field. If the number of misinserted cells equals or exceeds the threshold set by the MMISINSERT[7:0] register bits, the SECB count is incremented and the misinserted cell accumulation is suppressed.

BIP-16 Violation (BIPV) Count - The BIPV count is incremented by the number of mismatches between the locally calculated BIP-16 code and the value encoded in the BIP-16 field. If either of the MSN or the TUC values are incorrect, the BIPV accumulation is suppressed. If the number of BIPV errors equals or exceeds the threshold set by the MERRORED[4:0] register bits, the SECB count is incremented and the BIPV accumulation is suppressed.

Severely Errored Cell Block (SECB) Count - This parameter is incremented if the number of BIPVs, lost cells or misinserted cells are equal to or greater than the threshold set by the MERRORED[4:0], MLOST[7:0] and MMISINSERT[7:0] register bits, respectively.

The RCMP-800 also maintains the analogous counts for the reverse flow at SA[19:16]=1110. These counts are updated upon the reception of either a Backward Reporting cell or a Monitoring/Reporting cell. The MERRORED[4:0], MLOST[7:0] and MMISINSERT[7:0] register bits also set the SECB thresholds for the reverse flow.

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The count values contained in the SA[19:16]=1110 and 1111 locations are cleared to zero upon a microprocessor read access.

Activation/Deactivation Cells

Activation/Deactivation cells are identified with a OAM Cell Type of 1000. They are used by the management entity to implement the handshaking required to initiate or cease performance monitoring or continuity check processes.

The RCMP-800 does not process these cells. If the RCMP-800 is not an end point for an OAM cell flow, all Activation/Deactivation cells are passed to the Output Cell Interface. If the RCMP-800 is an end point for a OAM flow, the Activation/Deactivation cells are optionally passed to the Microprocessor Cell Interface or the Output Cell Interface. The flow of the Activation/Deactivation cells is controlled by the ACTDEtoUP and ACTDEtoOCIF bits of the ALCP Routing Configuration register. This enables the management entity to process the cell, and respond by modifying the "PM_activate" or "CC_activate" bit and sending back an acknowledgment.

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Resource Management Cells

Resource Management (RM) cells are identified by PTI=110 for VC-RM cells and by VCI=6 for VP-RM cells. As a programmable option, VP-RM cells can be further qualified by PTI=110.

The RCMP-800 does not process the payload of these cells, but simply passes them to the Output Cell Interface with a translated header. As an option, the RCMP-800 can copy the cells to the Microprocessor Cell Interface. RM cells are not included in Performance Management blocks.

Backward OAM and RM Cell Identification

All RCMP-800-generated backward flow OAM cells, and forward and backward Resource Management cells may be marked for easy identification by an external processing device. As a configurable option, the RCMP-800 can overwrite an arbitrary byte in the cell's appended bytes or header with a Cell Status Information byte. The contents of the Cell Status Information byte consist of the following:

Cell Status Information byte	
BWDROUTINGTAG[7:3]	CELLID[2:0]

The five-bit BWDROUTINGTAG[4:0] is stored in the VC table at SA[19:16] = 0011, and is only used for generated backward OAM cells (i.e. generated RDI and Backward Reporting). It overwrites the value normally presented for forward destined cells, so as to provide a distinction. For example, the BWDROUTINGTAG may contain the PHY identification for the egress device. The CELLID[2:0] field is encoded in all cells as follows:

CELLID[2:0]	Definition
000	All other cells: • cells received via the Input Cell Interface • cells inserted via the Microprocess Cell Inferface if • the UPHDRX register bit is a logic 1 • generated AIS cells if the TAGAIS register bit is a logic 0 • generated Continuity Check cells
001	Forward RM cell.
010	Backward RM cell.
011	Backward generated OAM cells: • generated RDI • generated Backward Reporting • generated AIS if the TAGAIS register bit is a logic 1
100-111	Reserved

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For all generated backward OAM cells (i.e. generated RDI and Backward Reporting), the RCMP-800 can be programmed to enable or disable header translation. That is, the RCMP-800 can insert either the ingress VPI/VCI or the translated VPI/VCI for a backward generated OAM cell.

Multicasting

The RCMP-800 supports multicasting. A single received cell can result in an arbitrary number of cells presented on the Output Cell Interface, each with its own unique VPI/VCI value and appended bytes. The ATM cell payload is duplicated without modification. Multicasting is implemented by having special code in the VC identification search table which indicates that the VC Table Record identified by the search process is one of a multicast set. That VC is processed and then the next VC for the same received cell is identified by a linked list pointer in the search table. This process can continue indefinitely. (Optionally, a 64 cell limit can be imposed as a watch dog.)

> Multicasting has limited utility in the ingress direction. Because the cells for all VCs are queued at the Output Cell Interface, multicasting may result in head-of-the-line blocking. Provided the multicasting cannot result in an instantaneous rate greater than the bandwidth supported by the Output Cell Interface (e.g. 800Mbit/s with a 50MHz 16-bit bus), no problems shall occur. It is the Connection Admission Control entity's responsibilty to ensure the traffic is within the rate supported.

Cell counting, cell rate policing and OAM processing is performed on the received cell, if so enabled. Therefore, the connection statistics for the multicast group are available in the VC Table Record at the head of the linked list. If the received cell is discarded due to policing, no multicasted cells are created. If the received cell is tagged, all multicasted cells are also tagged.

For multicast connections not at the head of the linked list, policing and cell counting are suppressed, in order to conserve bandwidth. The CLP=1, CLP=0 and non-compliant counts are not valid.

Each branch connection has its own VC Table Record. Therefore, header translation and OAM is supported independently for each branch.

Output Buffering

The output buffer consists of a four cell FIFO which transfers the oldest cell to the switch port whenever it signals that it will accept a cell. The FIFO output is a slave to the switch port. If the output buffer becomes full, it provides back-pressure to the Cell Processor which in turn back-pressures the Input Cell Interface.

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Congestion Control

Congestion control is handled by a single signal, CONG, entering the device. When this signal indicates that congestion is being experienced by the switch core, all low priority cells (high CLP bit) are discarded. This includes cells which are made low priority during the policing process.

JTAG Test Access Port Interface

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The RCMP-800 identification code is 073220CD hexadecimal.

Microprocessor Interface

The microprocessor interface is provided for device configuration, control and monitoring by an external microprocessor. Normal mode registers, test mode registers and the external SRAM can be accessed through this port. Test mode registers are used to enhance the testability of the RCMP-800.

The interface has a 16 bit wide data bus. Multiplexed address and data operation is supported.

SRAM Accesses

Microprocessor access to the external SRAM is provided to allow configuration and monitoring of individual connections. The VPI/VCI search state machine allocates a single cycle at the end of each search for microprocessor access. The maximum time to complete a SRAM access is 1200 ns with a SYSCLK frequency of 50 MHz. The average completion time is less than 360 ns.Upon placing the device in stand-by mode (default upon power up), all SRAM cycles become available to the microprocessor. This allows for rapid configuration of the device at start-up.

SRAM writes are initiated by writing the values to be presented on the SD[39:0] and SA[19:0] outputs to the External RAM Data and the External RAM Address registers. The BUSY status bit and the BUSYB output are asserted until the actual SRAM access is completed.

SRAM reads are initiated by writing the values to be presented on the SA[19:0] outputs to the External RAM Address registers. The values read on the SD[39:0] bus can be read from the External RAM Data registers after the BUSY status bit and the BUSYB output are deasserted.

The BUSYB output can be connected to a DMA request input of a DMA controller. The rising edge of BUSYB would initiate the next SRAM access upon the completion of the current access.

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Writing Cells

The RCMP-800 contains a one cell buffer for the assembly of a cell by the microprocessor for presentation on the Output Cell Interface. Optional header translation and CRC-10 protection provides full support of diagnostic and OAM requirements.

Writes are performed by manipulating the Microprocessor Buffer Control and Status (0x11) and Microprocessor Buffer Data (0x12) registers. Follow the steps below to write a cell:

1.) Poll the INSRDY bit in the Microprocessor Insert Buffer Control and Status register until it is a logic 1. Alternately, service the interrupts that result from setting the INSRDYE bit in the Master Interrupt Enable #1 (0x04) register. The INSRDYI bit in the Master Interrupt Status #1 (0x02) register is set whenever the INSRDY bit is asserted.

2.) Write the WRSOC bit in the Microprocessor Insert Buffer Control and Status register. At the same time, ensure that the OLEN[2:0], CRC10, UPHDRX and PHY[4:0] register bits are set to their correct values, depending on what operation is required.

If UPHDRX is a logic 1, PHY[4:0] represents the input PHY address that the cell is associated with and will be included in the search key used for VC identification.

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3.) Write the cell contents to the Microprocessor Buffer Data register. Each subsequent write enters the next word in the cell. The words shall be written in the following order:

Word #	Contents
1	1st pre-pended word (optional)
...	...
M	Last pre-pended word, M ≤ N (optional)
M+1	1st post-pended word (optional)
...	...
N	Last post-pended word, N < 6 (optional)
N+1	ATM header: GFC, VPI and VCI
N+2	ATM header: VCI, PTI and CLP
N+3	HEC and User Defined Field
N+4	1st ATM payload word
N+5	2nd ATM payload word
...	...
N+27	24th ATM payload word

If the cell's header is to be translated (UPHDRX logic 1), the number appended words shall match that programmed in the Input Cell FIFO Configuration register. If the cell's header is not be to translated (UPHDRX logic 0), the number appended words shall match that programmed in the Output Cell FIFO Configuration register. The RCMP-800 automatically handles cell length mismatches. Extra words shall be stripped with no consequences, but words that must be added to the end of the appended bytes will have arbitrary contents; therefore, the resulting cell processing may be unpredictable.

If the UPHDRX register bit is a logic 0, the written cell is presented verbatim on the Output Cell Interface.

Upon completion of a cell write, the cell will be transferred in the next available time slot.

The above sequence may be repeated to insert further cells. The assertion of the INSRDY bit indicates the transfer has been completed.

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Reading Cells

Cells received on the Input Cell Interface can be routed to the Microprocessor Cell Buffer based on the contents of the cell.

The buffer has a capacity of fifteen to eighteen cells depending on the length of the extracted cells:

Words in cell	ILEN[2:0]	Buffer Capacity
27	2	18
28	3	18
29	4	17
30	5	17
31	6	16
32	7	15

Maskable interrupt status's are generated upon the receipt of a cell and upon a buffer overflow. If a buffer overflow occurs, entire cells are lost.

Cells are written into the buffer without header translation. As an option, the HEC byte location can be overwritten with the PHY device identification. The length of the cell is determined by the CELLLEN[3:0] bits in the Input Cell FIFO Configuration register and the UPURS bit of the Cell Processor Configuration register. If the UPURS bit is a logic one, a causation word is prepended to the cell to indicate why the cell was routed to the Microprocessor Cell Buffer and provide cell status information.

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The causation word has the following format:

CAUSE[15:0]	Definition
Bit 15	PHYID[4]
Bit 14	PHYID[3]
Bit 13	PHYID[2]
Bit 12	PHYID[1]
Bit 11	PHYID[0]
Bit 10	PROV
Bit 9	End_pt
Bit 8	Seg_End_pt
Bit 7	Reserved
Bit 6	NNI
Bit 5	VPC
Bit 4	OAM_type
Bit 3	TYP[3]
Bit 2	TYP[2]
Bit 1	TYP[1]
Bit 0	TYP[0]

PHYID[4:0]: The index of the PHY device associated with the cell.

PROV: Provisioned indication. This bit is a logic 1 is the cell belongs to a provision connection. A logic 0 indicates the connection search failed to find a VC Table Record for the cell. The End_pt, Seg_Eng_pt, NNI and VPC bits are undefined if PROV is a logic 0.

End_pt: Indicates if the connection is provisioned as an OAM flow end point.

Seg_Eng_pt: Indicates if the connection is provisioned as an OAM segment flow end point.

NNI: Indicates if the connection is associated with a Network-Network Interface (NNI). A logic 0 means the connection belongs to a User-Network Interface (UNI).

VPC: Indicates if the connection is provisioned as a Virtual Path Connection (VPC). A logic 0 means the connection is provisioned as a Virtual Channel Connection (VCC).

OAM_type: A logic 1 identifies a segment OAM cell. A logic 0 identifies an end-to-end OAM cell. This bit is not defined when the TYP[3:0] field is 0000, 1011, 1100 or 1101.

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TYP[3:0] Cell type. It is encoded as follows:

TYP[3:0]	Cell Type
0000	User
0001	AIS
0010	RDI
0011	Continuity Check
0100	Loopback
0101	Forward Monitoring
0110	Backward Reporting
0111	Monitoring/Reporting
1000	Activate/Deactivate
1001	Undefined OAM
1010	Reserved
1011	Forward RM
1100	Backward RM
1101	Invalid PTI
1110	Reserved
1111	OAM cell with errored CRC-10.

The EXTCA bit of the Microprocessor Extract Buffer Control and Status (0x11) register is asserted if one or more complete cells are available in the buffer. If DMA control is enabled (DMAEN bit logic 1), the DREQ output is also asserted upon receipt of a cell. The first read of the Microprocessor Cell Buffer after either the EXTCA bit or the DREQ is asserted returns the first word of the cell. Subsequent reads return the remainder of the cell. The sequence of the words is the same as for buffer writes (see above). At any time the read pointer can be returned to the beginning of the cell by setting the RESTART bit. The current cell is discarded upon setting the ABORT bit. The DREQ output is deasserted during the read of the last word of the cell.

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Normal Mode Register Memory Map

Address	Register
0x00	Identification and Master Reset / Load Meters
0x01	Master Configuration
0x02	Interrupt Status #1
0x03	Interrupt Status #2
0x04	Interrupt Enable #1
0x05	Interrupt Enable #2
0x06	Master Clock Monitor
0x07	Latest Alarmed Connections
0x08	Input Cell FIFO Configuration
0x09	Physical Layer Cell Counter
0x0A	Input Cell Counter (LSB)
0x0B	Input Cell Counter (MSB)
0x0C	Input Polling Configuration
0x0D-0x0F	Reserved
0x10	Microprocessor Extract Buffer Control and Status
0x11	Microprocessor Insert Buffer Control and Status
0x12	Microprocessor Cell Data
0x13-0x17	Reserved
0x18	Cell Processor Configuration
0x19	Performance Monitoring Configuration 1
0x1A	Performance Monitoring Configuration 2
0x1B	ABR Cell Rate Policing Configuration
0x1C	VBR/CBR Cell Rate Policing Configuration
0x1D	Routing Configuration
0x1E-0x1F	Reserved
0x20	CRAM Configuration
0x21	External RAM Address (LSB)
0x22	External RAM Address (MSB) and Access Control
0x23	External RAM Data (LSB)
0x24	External RAM Data
0x25	External RAM Data (MSB)
0x26	Maximum VC Table Index
0x27	Search Key Construction
0x28	Field A Location and Length
0x29	Field B Location and Length
0x2A-0x2F	Reserved
0x30	Counter Status
0x31	Valid OAM Cell Count
0x32	Errored OAM Cell Count

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0x33	Invalid Cell Count
0x34	Count of Cells Dropped Due to Congestion
0x35-0x37	Reserved
0x38	Output Cell FIFO Configuration
0x39	Reserved
0x3A	Output Cell Counter (LSB)
0x3B	Output Cell Counter (MSB)
0x3C-0x3F	Reserved
0x40	Master Test
0x41-0x7F	Reserved for Test

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NORMAL MODE REGISTER DESCRIPTIONS

Normal mode registers are used to configure and monitor the operation of the RCMP-800. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[6]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the RCMP-800 to determine the programming state of the block.

3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect RCMP-800 operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the RCMP-800 operates as intended, reserved register bits must only be written with logic 0. Similarly, writing to reserved registers should be avoided.

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Master Registers

Register 0x00: Master Reset and Identity / Load Meters

Bit	Type	Function	Default
Bit 15	R/W	RESET	0
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R	TYPE[2]	0
Bit 5	R	TYPE[1]	0
Bit 4	R	TYPE[0]	1
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	0

This register allows the revision of the RCMP-800 to be read by software. This permits graceful migration to newer, feature enhanced versions of the RCMP-800.

In addition, writing to this register simultaneously loads the aggregate performance meter registers located at addresses 0x09, 0x0A, 0x0B, 0x31, 0x32, 0x33, 0x34, 0x3A and 0x3B.

ID[3:0]:

The ID bits can be read to provide a binary RCMP-800 revision number.

TYPE[2:0]:

The TYPE bits can be read to distinguish the RCMP-800 from the other members of the RCMP-800 family of devices.

RESET:

The RESET bit allows the RCMP-800 to be reset under software control. If the RESET bit is a logic 1, the entire RCMP-800 is held in reset. This bit is not self-clearing. Therefore, a logic 0 must be written to bring the RCMP-800 out of reset. Holding the RCMP-800 in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset.

Note, unlike the hardware reset input, RSTB, the software reset bit, RESET does not force the RCMP-800's digital output pins tristate.

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Register 0x01: Master Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	BUSYPOL	0
Bit 8	R/W	DREQINV	0
Bit 7	R/W	XPOLVC	0
Bit 6	R/W	RDIVC	0
Bit 5	R/W	AISVC	0
Bit 4	R/W	POLVC	0
Bit 3	R/W	CCVC	0
Bit 2	R/W	SEL1SEC	0
Bit 1	R/W	CLKRATE	0
Bit 0	R/W	STANDBY	1

STANDBY:

The STANDBY bit disables cell processing to avoid the passing of corrupted cells while initializing the RCMP-800. When STANDBY is a logic 1, the RCMP-800 is in a low power state with the cell processor and cell buffers held in reset. Microprocessor registers and the external SRAM can still be accessed. STANDBY resets to a logic 1.

If the STANDBY bit is set while cell processing is in progress, the processing of cells currently in the pipeline is completed, but no more cells are transferred into the RCMP-800.

CLKRATE:

The CLKRATE bit selects between a 25 MHz and 50 MHz SYSCLK frequency. If CLKRATE is a logic 1, a 25 MHz clock is expected; otherwise, a 50 MHz clock is expected. Other rates are allowable, but fault monitoring cells and alarms will not be generated at correct intervals. The CLKRATE bit has no effect if the SEL1SEC bit is a logic 1.

SEL1SEC:

The SEL1SEC bit determines the trigger for processing that relies on an one second clock, such as AIS and RDI cell generation. If SEL1SEC is a logic 0, the one second clock is derived from the SYSCLK, which is assumed to be 25 or 50 MHz. If SEL1SEC is a logic 1, processing is initiated on the rising edge of the ONESEC input.

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XPOLVC:

The XPOLVC (excessive policing) bit enables the updating of the Latest Alarmed Virtual Connection register (0x07) upon the receipt of a cell belonging to a connection which has a one in the most significant bit position of one of the Non-Compliant Cell Count fields. If XPOLVC is a logic 1, the Latest Alarmed Virtual Connection register will be loaded with the VC Table index of the corresponding virtual connection.

This functionality allows long integration intervals for well behaved connections, while providing the ability to transfer the Non-Compliant Cell Counts of unrestrained connections before they saturate.

CCVC:

The CCVC bit enables the updating of the Latest Alarmed Virtual Connection register (0x07) upon the change in a Continuity Check alarm status. If CCVC is a logic 1, the Latest Alarmed Virtual Connection register will be loaded with the VC Table index corresponding to the virtual connection whose "CC_alarm" bit has changed.

POLVC:

The POLVC bit enables the updating of the Latest Alarmed Virtual Connection register (0x07) upon the receipt of a cell violating a traffic contract. If POLVC is a logic 1, the Latest Alarmed Virtual Connection register will be loaded with the VC Table index corresponding to the virtual connection whose "POLI" bit has been asserted.

AISVC:

The AISVC bit enables the updating of the Latest Alarmed Virtual Connection register (0x07) upon the change in an AIS alarm status. If AISVC is a logic 1, the Latest Alarmed Virtual Connection register will be loaded with the VC Table index corresponding to the virtual connection whose "AIS" bit has changed.

RDIVC:

The CCVC bit enables the updating of the Latest Alarmed Virtual Connection register (0x07) upon the change in a RDI alarm status. If RDIVC is a logic 1, the Latest Alarmed Virtual Connection register will be loaded with the VC Table index corresponding to the virtual connection whose "RDI" bit has changed.

DREQINV:

The DREQINV bit inverts the polarity of the DREQ primary output. If DREQINV is a logic 0, the DREQ output is active high. If DREQINV is a logic 1, the DREQ output is active low.

BUSYPOL:

The BUSYPOL bit sets the polarity of the BUSYB primary output. If

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BUSYPOL is a logic 0, the BUSYB output is active low. If BUSYPOL is a logic 1, the BUSYB output is active high.

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Register 0x02: Master Interrupt Status #1

Bit	Type	Function	Default
Bit 15	R	REG3I	X
Bit 14	R	XFERI	X
Bit 13	R	INSRDYI	X
Bit 12	R	UPCAI	X
Bit 11	R	UPFOVRI	X
Bit 10	R	VCVALID	X
Bit 9	R	FULLI	X
Bit 8	R	PCELLI	X
Bit 7	R	XPOLI	X
Bit 6	R	RDII	X
Bit 5	R	AISI	X
Bit 4	R	POLI	X
Bit 3	R	CCI	X
Bit 2	R	OAMERRI	X
Bit 1	R	PTIVCII	X
Bit 0	R	INVALI	X

This register allows the source of an active interrupt to be identified. All bits in this register except REG3I are reset immediately after a read to this register.

INVALI:

The INVALI bit indicates a cell with an unprovisioned VPI/VCI combination or invalid routing bits has been received. When logic 1, the INVALI bit indicates one or more VC Table searches have not resulted in a match. A logic 1 may also indicate that a Resource Management cell with an incorrect CRC-10 has been received. This bit is cleared when this register is read.

PTIVCII:

The PTIVCII bit indicates a cell with an invalid PTI or VCI field has been received. When logic 1, the PTIVCII bit indicates one or more VCC cells have contained PTI='111', one or more VPC cells with an invalid VCI field (VCI 7 through 15) or at least one VP Resource Management cell has been received with PTI not equal to '110'. This bit is cleared when this register is read.

OAMERRI:

The OAMERRI bit indicates an OAM cell has been with an incorrect OAM Type, Function Type or Error Detection Code field. When logic 1, the OAMERRI bit indicates one or more errored OAM cells have been received. This bit is cleared when this register is read.

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CCI:

The CCI bit indicates a Continuity Check alarm has changed state. When logic 1, the CCI bit indicates the "CC_alarm" bit in the VC Table has changed for one or more virtual connections. This bit is cleared when this register is read.

If the CCVC bit of the Master Configuration register is a logic 1, the Latest Alarmed Virtual Connection register is updated with the VC Table index for the virtual connection simultaneously with the setting of the CCI bit.

POLI:

The POLI bit indicates a non-compliant cell has been received. When logic 1, the POLI bit indicates one or more cells have violated the traffic contract since the last read of this register. This bit is cleared when this register is read.

If the POLVC bit of the Master Configuration register is a logic 1, the Latest Alarmed Virtual Connection register is updated with the VC Table index for the virtual connection simultaneously with the setting of the POLI bit.

AISI:

The AISI bit indicates an AIS alarm has changed state. When logic 1, the AISI bit indicates one or more virtual connections have either entered or left the AIS state. This bit is cleared when this register is read.

If the AISVC bit of the Master Configuration register is a logic 1, the Latest Alarmed Virtual Connection register is updated with the VC Table index for the virtual connection simultaneously with the setting of the AISI bit.

RDII:

The RDII bit indicates a RDI alarm has changed state. When logic 1, the RDII bit indicates one or more virtual connections have either entered or left the RDI state. This bit is cleared when this register is read.

If the RDIVC bit of the Master Configuration register is a logic 1, the Latest Alarmed Virtual Connection register is updated with the VC Table index for the virtual connection simultaneously with the setting of the RDII bit.

XPOLI:

The excessive policing indication (XPOLI) bit becomes a logic 1 upon the receipt of a cell belonging to a connection which has a one in the most significant bit position of one of the Non-Compliant Cell Count fields. This bit is reset immediately after a read to this register.

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If the XPOLVC bit of the Master Configuration register is a logic 1, the Latest Alarmed Virtual Connection register is updated with the VC Table index for the virtual connection simultaneously with the setting of the XPOLI bit.

PCELLI:

The PCELLI bit indicates a physical layer cell has been received. When logic 1, the PCELLI bit indicates one or more cells with an all zero VCI value and a CLP=1 have been received. This bit is cleared when this register is read.

VCVALID:

The VCVALID bit becomes a logic 1 when the Latest Alarmed Virtual Connections register (0x07) contains valid information. This bit is NOT cleared when this register is read. This bit is cleared when the entire contents of the Latest Alarmed Virtual Connections register (0x07) FIFO have been read.

An image of the VCVALID bit is at address location (0x04). It is provided so that VCVALID may be sampled without clearing the interrupt status bits in this register.

FULLI:

The FULLI bit becomes a logic 1 when the output buffer has been filled to its 4 cell capacity. This may indicate failure or congestion in the entity connected to the Output Cell Interface. This bit is cleared when this register is read.

The FULLI bit may also become a logic 1 as a result of setting the FIFORST bit of the Output Cell Configuration register (0x38). With the output FIFO reset, it is unable to accept any cells, which is the same immediate symptom as a full buffer.

UPFOVRI:

The UPFOVRI bit is set high when a Microprocessor Cell Interface extract buffer overrun occurs. This bit is reset immediately after a read to this register.

UPCAI:

The UPCAI bit indicates that a cell has been written into the Microprocessor Cell extract buffer and is ready for processing. When logic 1, the UPCAI bit indicates that the EXTCA bit in the Microprocessor Extract Buffer Control and Status (0x10) register has been asserted. The UPCAI bit is cleared when this register is read.

INSRDYI:

The INSRDYI bit indicates the Microprocessor Cell Interface insert buffer is empty and is ready for another cell. This bit is cleared when this register is read.

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XFERI:

The XFERI bit indicates that the aggregate cell counters have been transferred to holding registers and the contents should be read. When logic 1, the XFERI bit indicates that either the XFER or OVR bit in the Counter Status (0x30) register has been asserted. The XFERI bit is cleared when this register is read.

REG3I:

The REG3I bit indicates that at least one bit in Register 0x03, RCMP-800 Master Interrupt Status #2, is currently asserted.

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Register 0x03: Master Interrupt Status #2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R	SRCHERRI	X
Bit 8	R	SPRTYI[4]	X
Bit 7	R	SPRTYI[3]	X
Bit 6	R	SPRTYI[2]	X
Bit 5	R	SPRTYI[1]	X
Bit 4	R	SPRTYI[0]	X
Bit 3	R	IPRTYI[1]	X
Bit 2	R	IPRTYI[0]	X
Bit 1	R	ISOCI	X
Bit 0		Unused	X

ISOCI:

The ISOCI bit is set high when the ISOC input is sampled high during any position other than the first word of the selected data structure. The write address counter is reset to the first word of the data structure when ISOC is sampled high. This bit is reset immediately after a read to this register.

IPRTYI[1:0]:

The IPRTYI[1:0] bits indicate a parity error has been detected on the IDAT[15:0] bus. When logic 1, the IPRTYI[1] bit indicates a parity error over inputs IDAT[15:0] (in word parity mode) or IDAT[15:8] (in byte parity mode). Similarly, when logic 1, the IPRTYI[0] bit indicates a parity error over inputs IDAT[7:0] in byte parity mode. (IPRTYI[0] is unused in word parity mode, i.e., when the IBYTEPRTY register bit is logic zero). Both bits are cleared when this register is read. Odd or even parity is selected using the IPTYP bit.

SPRTYI[4:0]:

The SPRTYI[4:0] bits indicate a parity error has been detected on the SD[39:0] bus. When logic 1, the SPRTYI[4] bit indicates a parity error over inputs SD[39:32]. When logic 1, the SPRTYI[3] bit indicates a parity error over inputs SD[31:24]. When logic 1, the SPRTYI[2] bit indicates a parity error over inputs SD[23:16]. When logic 1, the SPRTYI[1] bit indicates a parity error over inputs SD[15:8]. When logic 1, the SPRTYI[0] bit indicates a parity error over inputs SD[7:0]. All bits are cleared when this register is read.

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SRCHERRI:

The search error (SRCHERRI) bit indicates that a VCI/VPI search has failed due to an improperly constructed secondary search table or a bit error (correlate with SPRTYI[4:0]). This bit is set if the secondary key search takes more then 41 clock cycles or if single received cell results in 64 multicast cells when the LIMITMC register bit is logic 1. If the BADVCtoUP register bit is a logic 1, the cell associated with the failed search is routed to the Microprocessor Cell Interface. This bit is cleared when this register is read.

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Register 0x04: Master Interrupt Enable #1

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14	R/W	XFERE	0
Bit 13	R/W	INSRDYE	0
Bit 12	R/W	UPCAE	0
Bit 11	R/W	UPFOVRE	0
Bit 10	R	VCVALID	X
Bit 9	R/W	FULLE	0
Bit 8	R/W	PCELLE	0
Bit 7	R/W	XPOLE	0
Bit 6	R/W	RDIE	0
Bit 5	R/W	AISE	0
Bit 4	R/W	POLE	0
Bit 3	R/W	CCE	0
Bit 2	R/W	OAMERRE	0
Bit 1	R/W	PTIE	0
Bit 0	R/W	INVALE	0

The above enable bits control the corresponding interrupt status bits in the RCMP-800 Master Interrupt Status #1 register. When an enable bit is set to logic 1, the INTB output is asserted low when the corresponding interrupt status bit is a logic 1.

VCVALID:

The VCVALID bit becomes a logic 1 when the Latest Alarmed Virtual Connections register (0x07) contains valid information. This bit is cleared when the entire contents of the Latest Alarmed Virtual Connections register (0x07) FIFO have been read.

This bit is an image of the VCVALID bit in the Master Interrupt Status #1 register (0x02). It is provided so that VCVALID may be sampled without clearing the interrupt status bits.

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Register 0x05: Master Interrupt Enable #2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	SRCHERRE	0
Bit 8	R/W	SPRTYE[4]	0
Bit 7	R/W	SPRTYE[3]	0
Bit 6	R/W	SPRTYE[2]	0
Bit 5	R/W	SPRTYE[1]	0
Bit 4	R/W	SPRTYE[0]	0
Bit 3	R/W	IPRTYE[1]	0
Bit 2	R/W	IPRTYE[0]	0
Bit 1	R/W	ISOCE	0
Bit 0		Unused	X

The above enable bits control the corresponding interrupt status bits in the RCMP-800 Master Interrupt Status #2 register. When an enable bit is set to logic 1, the INTB output is asserted low when the corresponding interrupt status bit is a logic 1.

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Register 0x06: Master Clock Monitor

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	IFCLKA	X
Bit 1	R	OFCLKA	X
Bit 0	R	SYSCLKA	X

This register provides activity monitoring on RCMP-800 clocks. When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

IFCLKA:

The IFCLK active (IFCLKA) bit monitors for low to high transitions on the IFCLK output. IFCLKA is set high on a rising edge of IFCLK, and is set low when this register is read.

OFCLKA:

The OFCLK active (OFCLKA) bit monitors for low to high transitions on the OFCLK output. OFCLKA is set high on a rising edge of OFCLK, and is set low when this register is read.

SYSCLKA:

The SYSCLK active (SYSCLKA) bit monitors for low to high transitions on the SYSCLK input. SYSCLKA is set high on a rising edge of SYSCLK, and is set low when this register is read.

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Register 0x07: Latest Alarmed Virtual Connections

Bit	Type	Function	Default
Bit 15	R	VCINDEX[15]	X
Bit 14	R	VCINDEX[14]	X
Bit 13	R	VCINDEX[13]	X
Bit 12	R	VCINDEX[12]	X
Bit 11	R	VCINDEX[11]	X
Bit 10	R	VCINDEX[10]	X
Bit 9	R	VCINDEX[9]	X
Bit 8	R	VCINDEX[8]	X
Bit 7	R	VCINDEX[7]	X
Bit 6	R	VCINDEX[6]	X
Bit 5	R	VCINDEX[5]	X
Bit 4	R	VCINDEX[4]	X
Bit 3	R	VCINDEX[3]	X
Bit 2	R	VCINDEX[2]	X
Bit 1	R	VCINDEX[1]	X
Bit 0	R	VCINDEX[0]	X

VCINDEX[15:0]:

The VCINDEX[15:0] bits represent a pointer to the VC Table Record whose "Status" field has changed recently. This register is updated when one of the XPOLI, RDII, AISI, POLI or CCI bits in the Master Interrupt Status #2 register is asserted. The XPOLVC, RDIVC, AISVC, POLVC and CCVC bits of the Master Configuration register independently allow each of the five alarms to update this register.

This register is FIFOed. Up to seven VC indices are stored and are accessed by successive reads of this register. A logic one in the VCVALID bit position in the Master Interrupt Status #1 register (0x02) indicates one or more VC indices have been queued. (An image of the VCVALID bit is provided in register address 0x04 for convenience.) An overflow of the FIFO results in new information replacing the old. To guarantee no information is lost, this register must be read within 3.8µs of the associated interrupt assertion. (This assumes each of eight consecutive cells causes an alarm.) It is recommended the entire contents of the FIFO be transferred and cached for subsequent processing.

VCINDEX[15:0] corresponds to the value which must be written into the External RAM Address (LSB) register to access the new status information of the virtual connection.

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Register 0x08: Input Cell FIFO Configuration

Bit	Type	Function	Default
Bit 15	R/W	HECUDF	1
Bit 14	R/W	ICAINV	0
Bit 13	R/W	CELLPOST[3]	0
Bit 12	R/W	CELLPOST[2]	0
Bit 11	R/W	CELLPOST[1]	0
Bit 10	R/W	CELLPOST[0]	0
Bit 9	R/W	CELLLEN[3]	0
Bit 8	R/W	CELLLEN[2]	0
Bit 7	R/W	CELLLEN[1]	0
Bit 6	R/W	CELLLEN[0]	0
Bit 5	R/W	IBYTEPRTY	0
Bit 4	R/W	IPTYP	0
Bit 3	R/W	FIFODP[1]	0
Bit 2	R/W	FIFODP[0]	0
Bit 1	R/W	ICALEVEL0	1
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the four-cell input FIFO. When FIFORST is set to logic zero, the input FIFO operates normally. When FIFORST is set to logic one, the input FIFO is immediately emptied and ignores writes. The input FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST.

It is recommended that, whenever any other bit in this register or the Input Polling Configuration register is changed, FIFORST be set to logic one upon the change and set to logic zero after.

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ICALEVEL0:

The ICALEVEL0 bit determines how the ICA[4:1] inputs are interpreted.

If ICALEVEL0 is a logic 1, the RCMP-800 checks for close compliance to the SCI-PHY cell transfer handshake. If the ICA signal for the PHY whose cell is currently being transferred is deasserted before the end of the cell, the cell will be discarded.

If ICALEVEL0 is a logic 0, the ICA signal may be deasserted early without the loss of the cell. Once a cell transfer is initiated, the entire cell will be read contiguously regardless of the state of the ICA signal.

ICALEVEL0 is ignored if the address polling mode is selected (IPOLL input is high).

FIFODP[1:0]:

The FIFODP[1:0] bits determine the input FIFO cell depth. FIFO depth control may be important in systems where the cell latency through the RCMP-800 must be minimized. The RCMP-800 will stop reading cells when the specified depth is reached. The selectable FIFO cell depths are shown below:

FIFODP[1]	FIFODP[0]	FIFO DEPTH
0	0	4 cells
0	1	3 cells
1	0	2 cells
1	1	1 cell

IPTYP:

The IPTYP bit selects even or odd parity for inputs IPRTY[1:0]. When set to logic 1, input IPRTY[1] is the even parity bit for inputs IDAT[15:8] while input IPRTY[0] is the even parity bit for inputs IDAT[7:0]. When set to logic 0, inputs IPRTY[1:0] are the odd parity bits for inputs IDAT[15:0].

IBYTEPRTY:

The active-high input byte parity selector bit, IBYTEPRTY, selects between byte parity (2 parity bits, each over an 8-bit byte) or word parity (1 parity bit over a 16-bit word). If IBYTEPRTY is set high, IPRTY[1] is expected to be the parity over IDAT[15:8] and IPRTY[0] is expected to be the parity over IDAT[7:0]. If IBYTEPRTY is set low, IPRTY[1] is expected to be the parity over IDAT[15:0] and IPRTY[0] is ignored. The IBYTEPRTY register bit is ignored if the IBUS8 input is asserted, in which case IPRTY[0] is the parity over IDAT[7:0] and IPRTY[1] is ignored.

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CELLLEN[3:0]:

The CELLLEN[3:0] bits determine the number of words appended to the input cell.

When IBUS8 is a logic 1, the binary CELLLEN[3:0] value is the number of bytes appended to the basic 53 byte ATM cell. The maximum cell length is 63 bytes; therefore, a CELLLEN[3:0] greater than 10 decimal results in 10 appended bytes.

When IBUS8 is a logic 0, the binary CELLLEN[3:0] value is the number of words appended to the basic 27 word ATM cell. The maximum cell length is 32 words; therefore, a CELLLEN[3:0] greater than 5 decimal results in 5 appended words.

CELLPOST[3:0]:

The CELLPOST[3:0] bits determine the number of words in the input cell post-pend. The numerical difference between CELLLEN[3:0] and CELLPOST[3:0] represents the number of words in the pre-pend. It is inappropriate that CELLPOST[3:0] exceed CELLLEN[3:0].

When IBUS8 is a logic 1, the binary CELLPOST[3:0] value is the number of bytes post-pended to the basic 53 byte ATM cell.

When IBUS8 is a logic 0, the binary CELLPOST[3:0] value is the number of words post-pended to the basic 27 word ATM cell.

ICAINV:

The ICAINV bit selects the active polarity of the ICA[4:1] signals. The default configuration selects ICA[4:1] to be active high, indicating that a cell slot is available in the input FIFO when high. When ICAINV is set to logic one, the ICA[4:1] signals become active low. If the state of the ICAINV bit has been changed, the input FIFO must be reset via the FIFORST bit in order to properly initialize the ICA[4:1] outputs.

HECUDF:

The HECUDF bit determines whether or not the HEC/UDF octets are included in cells transferred over the input interface. When set to logic 1 (default), the HEC and UDF octets are included. When set to logic 0, these octets are omitted. I.e., if BUS8 is logic 0, the third word of the 27-word ATM cell is omitted and a 26-word cell (plus appended words) is transferred. If BUS8 is logic 1, the fifth octet of the 53-octet ATM cell is omitted and a 52-octet cell (plus appended octets) is transferred.

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Register 0x09: Physical Layer Cell Count

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	PICELL[7]	X
Bit 6	R	PICELL[6]	X
Bit 5	R	PICELL[5]	X
Bit 4	R	PICELL[4]	X
Bit 3	R	PICELL[3]	X
Bit 2	R	PICELL[2]	X
Bit 1	R	PICELL[1]	X
Bit 0	R	PICELL[0]	X

This register provides a count of the idle cells erroneously passed from the physical layer.

PICELL[7:0]:

The PICELL[7:0] bits indicate the number of Physical Layer cells presented to the Input Cell Interface during the last accumulation interval. A Physical Layer cell is identified by a VPI value of zero, a VCI value of zero and a CLP value of one. Physical Layer cells should not be present at the ATM Layer.

A write to either address 0x00, 0x09, 0x0A or 0x0B loads the register with the current counter value and resets the internal 8 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Physical Layer Idle Cell Counter registers. The counter should be polled every second to avoid saturating. The contents of these registers are valid within four IFCLK cycles after a transfer is triggered by a write to address 0x00, 0x09, 0x0A or 0x0B.

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Register 0x0A: Input Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	ICELL[15]	X
Bit 14	R	ICELL[14]	X
Bit 13	R	ICELL[13]	X
Bit 12	R	ICELL[12]	X
Bit 11	R	ICELL[11]	X
Bit 10	R	ICELL[10]	X
Bit 9	R	ICELL[9]	X
Bit 8	R	ICELL[8]	X
Bit 7	R	ICELL[7]	X
Bit 6	R	ICELL[6]	X
Bit 5	R	ICELL[5]	X
Bit 4	R	ICELL[4]	X
Bit 3	R	ICELL[3]	X
Bit 2	R	ICELL[2]	X
Bit 1	R	ICELL[1]	X
Bit 0	R	ICELL[0]	X

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Register 0x0B: Input Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	ICELL[23]	X
Bit 6	R	ICELL[22]	X
Bit 5	R	ICELL[21]	X
Bit 4	R	ICELL[20]	X
Bit 3	R	ICELL[19]	X
Bit 2	R	ICELL[18]	X
Bit 1	R	ICELL[17]	X
Bit 0	R	ICELL[16]	X

ICELL[23:0]:

The ICELL[23:0] bits indicate the number of cells read from the input FIFO during the last accumulation interval. The count includes all user information and OAM cells, regardless of whether the VPI/VCI value is provisioned. The count does not include physical layer idle cells (VPI=0, VCI=0, CLP=1) and unassigned cells (VPI=0, VCI=0, CLP=0).

A write to either address 0x00, 0x09, 0x0A or 0x0B loads the registers with the current counter value and resets the internal 24 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Input Cell Counter registers. The counter should be polled at least every 10 seconds to avoid saturating. The contents of these registers are valid within four SYSCLK cycles after a transfer is triggered by a write to address 0x00, 0x09, 0x0A or 0x0B.

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Register 0xC: Input Polling Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	NNI	1
Bit 4	R/W	PHYDEV[4]	0
Bit 3	R/W	PHYDEV[3]	0
Bit 2	R/W	PHYDEV[2]	0
Bit 1	R/W	PHYDEV[1]	0
Bit 0	R/W	PHYDEV[0]	0

PHYDEV[4:0]:

The PHYDEV[4:0] bits are used when the RCMP-800 polls PHY devices using IADDR[4:0] (i.e. when IPOLL is high). They indicate the number of PHY devices to be polled as follows:

PHYDEV[4:0]	Meaning
00000	Poll PHY#1 only
00001	Poll PHY#1 thru PHY#2
00010	Poll PHY#1 thru PHY#3
:	:
11110	Poll PHY#1 thru PHY#31
11111	Poll all 32 PHY devices

Setting PHYDEV[4:0] such that more PHY devices are polled than are actually connected to the RCMP-800 will not cause malfunction (provided ICA[1] is pulled low when undefined) but may result in loss of cell throughput due to unnecessarily long polling cycle times.

NNI:

The NNI bit selects whether the first four bits of the ATM cell header are used when determining whether a cell should be discarded because it is

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Unassigned or one which is reserved for the Physical Layer. When set to logic 1 (default), the NNI format is used and first four bits of the ATM cell header must be zeros for a cell to be indentified as an Unassigned or Physical Layer cell. When set to logic 0, the UNI format is used and first four bits of the ATM cell header are ignored.

If a mixture of UNI and NNI cells pass through the Input Cell Interface, this register bit should be set to a logic 1. Any Physical Layer UNI cells which contain non-zero GFC fields shall be passed through the input FIFO and subsequently rejected by the VC Identification algorithm. This results in a increment of the Invalid Cell Count instead of the Physical Layer Cell Count.

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Register 0x10: Microprocessor Extract Buffer Control and Status

Bit	Type	Function	Default
Bit 15	R	EXTCA	X
Bit 14	R	ILEN[2]	X
Bit 13	R	ILEN[1]	X
Bit 12	R	ILEN[0]	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	W	ABORT	0
Bit 3	W	RESTART	0
Bit 2	R/W	EXTPHYID	0
Bit 1	R/W	DMAEN	0
Bit 0	R/W	EXTRST	0

EXTRST:

The EXTRST bit is used to reset the extract FIFO. When EXTRST is set to logic 0, the extract FIFO operates normally. When EXTRST is set to logic 1, the extract FIFO is immediately emptied and ignores writes. The extract FIFO remains empty and continues to ignore writes until a logic 0 is written to EXTRST.

DMAEN:

The DMA enable (DMAEN) bit allows generation of a DMA request upon reception of a cell in the extract buffer. If DMAEN is a logic 1, the DREQ output is asserted when a complete cell has been written into the extract FIFO. The first read of the Microprocessor Cell Data register after DREQ is asserted returns the first word of the cell. Subsequent reads of the Microprocessor Cell Data register return the remaining words in the cell. When the cell contents are exhausted, the DREQ output is deasserted even if more cells are contained in the cell buffer. This eases the identification of cell boundaries.

If DMAEN is a logic 0, the DREQ output is held deasserted.

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EXTPHYID:

The extract physical link identification (EXTPHYID) bit allows the HEC byte of each extracted cell to be overwritten with physical link identification associated with the extracted cell, which is indicated on the IPHYID[4:0] inputs as the cell is stored in the extract buffer. The IPHYID will consist of a 5-bit number in the range 0 to 31, and will be right justified within the HEC byte of the cell. A value of 0 represents PHY 1, a value of 1 represents PHY 2, etc. up to PHY 32.

If EXTPHYID is set to a logic 1, the HEC byte will be overwritten.
If EXTPHYID is set to a logic 0, the HEC byte will be unchanged.

RESTART:

The restart cell read (RESTART) bit resets the microprocessor cell read pointer. If RESTART is set to a logic 1 during a cell read, the next word read from the Microprocessor Cell Data register will be the first word of the current cell. Subsequent reads from the Microprocessor Cell Data register return the remaining words in the cell.

RESTART is not readable and is cleared upon a read of the Microprocessor Cell Data register (0x12).

ABORT:

The read abort (ABORT) bit allows the microprocessor to discard a cell without reading the remaining contents. If ABORT is set to a logic 1, the current cell being read is purged from the buffer and the DREQ output will be deasserted.

ABORT is not readable and is cleared upon a read of the Microprocessor Cell Data register (0x12).

ILEN[2:0]:

The input cell length (ILEN[2:0]) status bits represent the length of the extracted cell currently being read. ILEN[2:0] will be valid throughout the transfer of the cell. This status information may be used to control the number of microprocessor reads for each particular cell, and would typically be read just prior to reading the cell data. Since valid cell lengths range from 32 words to 27 words, values of these bits are:

ILEN[2:0] = 111, cell length = 32 words
ILEN[2:0] = 110, cell length = 31 words
ILEN[2:0] = 101, cell length = 30 words
ILEN[2:0] = 100, cell length = 29 words
ILEN[2:0] = 011, cell length = 28 words
ILEN[2:0] = 010, cell length = 27 words
ILEN[2:0] = 001, RESERVED
ILEN[2:0] = 000, RESERVED

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EXTCA:

The microprocessor cell available (EXTCA) status bit indicates that at least one cell is present in the cell extract buffer. EXTCA is set to logic 1 when the last word of a cell is received. EXTCA is cleared to logic 0 when the last word in the buffer is read by the microprocessor. If multiple cells exist in the buffer, then EXTCA will remain at logic 1 until the last word of the last cell is read.

Assertion of the EXTCA status bit also results in a maskable interrupt.

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Register 0x11: Microprocessor Insert Buffer Control and Status

Bit	Type	Function	Default
Bit 15	R	INSRDY	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	W	WRSOC	0
Bit 10	R/W	PHY[4]	0
Bit 9	R/W	PHY[3]	0
Bit 8	R/W	PHY[2]	0
Bit 7	R/W	PHY[1]	0
Bit 6	R/W	PHY[0]	0
Bit 5	R/W	OLEN[2]	0
Bit 4	R/W	OLEN[1]	0
Bit 3	R/W	OLEN[0]	0
Bit 2	R/W	UPHDRX	0
Bit 1	R/W	CRC10	0
Bit 0	R/W	INSRST	0

INSRST:

The INSRST bit is used to reset the insert FIFO. When INSRST is set to logic 0, the insert FIFO operates normally. When INSRST is set to logic 1, the insert FIFO is immediately emptied and ignores writes. The insert FIFO remains empty and continues to ignore writes until a logic 0 is written to INSRST.

Any transfer from the insert FIFO currently in progress will be aborted.

CRC10:

The CRC-10 enable (CRC10) bit forces the generation the Error Detection Code (EDC) for cells written into the buffer. If CRC10 is set to logic 1 prior to assembling the cell in the buffer, the last 10 bits of the cell are overwritten with the standardized CRC-10 value calculated over the information field. In this case, the 6 MSBs of the last word are overwriiten with zeros prior to CRC-10 generation, and hence 6 zeros will be transmiited along with the valid CRC-10.

UPHDRX:

The header translation (UPHDRX) bit controls the header processing of the current cell written into the buffer.

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If UPHDRX was set to logic 1 prior to assembling the cell in the buffer, the current cell has its header modified before presentation on the output bus. The cell is also subject to policing, cell counting, multicasting and OAM processing just as if had been received through the Input Cell Interface. Therefore, the header information must correspond to a provisioned virtual connection, or else the cell is discarded.

If UPHDRX was a logic 0, the current cell is passed to the output without modification, with the exception that appended bytes may be added or stripped to ensure a correct cell length for the selected interface. The cell need not belong to a provisioned connection. The cell is not policed and does not affect the contents of Forward Monitoring cells and error counts. In other words, besides presenting the cell on the Output Cell Interface, the RCMP-800 ignores the existence of the cell.

OLEN[2:0]:

The OLEN[2:0] bits indicate the number of words in the inserted cell that the microprocessor is about to write. Since valid cell lengths range from 32 words to 27 words, values of these bits are:

OLEN[2:0] = 111, cell length = 32 words
OLEN[2:0] = 110, cell length = 31 words
OLEN[2:0] = 101, cell length = 30 words
OLEN[2:0] = 100, cell length = 29 words
OLEN[2:0] = 011, cell length = 28 words
OLEN[2:0] = 010, cell length = 27 words
OLEN[2:0] = 001, RESERVED
OLEN[2:0] = 000, RESERVED

PHY[4:0]:

The physical link identification bits (PHY[4:0]) determine the PHY association of the current cell being written by the microprocessor. The state of PHY[4:0] when the WRSOC is set selects the PHY device for that cell:

PHY[4:0]	Associated Source
00000	PHY #1/single PHY
00001	PHY #2
00010	PHY #3
00011	PHY #4
.....	.....
11111	PHY #32

The interpretation of the PHY[4:0] bits depends on the state of the UPHDRX bit. If UPHDRX is a logic 1, PHY[4:0] represents the input PHY the cell is associated with and will be included in the search key used for VC identification. If UPHDRX is a logic 0, PHY[4:0] is ignored.

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WRSOC:

The write start of cell (WRSOC) bit must identify the first word of the current cell that the microprocessor is writing. If WRSOC is a logic 1, the next word written to the Microprocessor Cell Data register becomes the first word of the cell. Subsequent writes to the Microprocessor Cell Data register fill the remainder of the cell sequentially and the number of writes should correspond to the programmed OLEN value. If WRSOC is set again before a complete cell is written, the existing contents will be overwritten without transmission.

WRSOC is not readable.

INSRDY:

The insert buffer ready (INSRDY) status bit indicates that the writeable cell buffer is ready to accept another complete cell. It remains set for as long as the buffer is completely empty. INSRDY is cleared upon the write of the first word of a cell. Assertion of the INSRDY bit results in a maskable interrupt.

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Register 0x12: Microprocessor Cell Data

Bit	Type	Function	Default
Bit 15	R/W	MCD[15]	X
Bit 14	R/W	MCD[14]	X
Bit 13	R/W	MCD[13]	X
Bit 12	R/W	MCD[12]	X
Bit 11	R/W	MCD[11]	X
Bit 10	R/W	MCD[10]	X
Bit 9	R/W	MCD[9]	X
Bit 8	R/W	MCD[8]	X
Bit 7	R/W	MCD[7]	X
Bit 6	R/W	MCD[6]	X
Bit 5	R/W	MCD[5]	X
Bit 4	R/W	MCD[4]	X
Bit 3	R/W	MCD[3]	X
Bit 2	R/W	MCD[2]	X
Bit 1	R/W	MCD[1]	X
Bit 0	R/W	MCD[0]	X

MCD[15:0]:

The MCD[15:0] contains the cell data destined to or read from the Microprocessor Cell Buffer.

For the cell extract buffer, the EXTCA bit and associated maskable interrupt indicate that a cell is available to be read. Alternately, the assertion of the DREQ output (if enabled by the DMAEN bit) signals the presence of the cell. Reads of this register return the words of the cell starting with the first. If necessary, the read pointer can be reset to the start of the current cell by setting the RESTART bit. Alternatively, the read pointer can be reset to the start of the next cell by setting the ABORT bit.

In a polled mode, the INSRDY register bit indicates that the microprocessor may write another cell. For interrupt driven systems, the INSRDYI interrupt status bit and associated maskable interrupt indicate that a cell may be written.

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Register 0x18: Cell Processor Configuration

Bit	Type	Function	Default
Bit 15	R/W	UPURS	0
Bit 14	R/W	LB[1]	0
Bit 13	R/W	LB[0]	0
Bit 12	R/W	CSILOC[3]	0
Bit 11	R/W	CSILOC[2]	0
Bit 10	R/W	CSILOC[1]	0
Bit 9	R/W	CSILOC[0]	0
Bit 8	R/W	VCRAstuff	0
Bit 7	R/W	AUTORDI	0
Bit 6	R/W	BWDXLAT	0
Bit 5	R/W	GFC	0
Bit 4	R/W	COUNT	0
Bit 3	R/W	GPOLICE	0
Bit 2	R/W	PM	0
Bit 1	R/W	GPREPO	0
Bit 0	R/W	GVPIVCI	0

GVPIVCI:

If the GVPIVCI bit is a logic 1, VPI/VCI translation is globally enabled so ATM VPI/VCI bytes can be replaced by the VC Table words at SRAM location SA[19:16]=1000. If the GVPIVCI bit is a logic 0, the incoming VPI/VCI combination passes through unaltered.

GPREPO:

If the GPREPO bit is a logic 1, prepend/postpend is globally enabled so appended bytes, HEC and UDF can be replaced by the VC Table words at SRAM locations SA[19:16]=0011, 1000, 1001 and 1010. If the GPREPO bit is a logic 0, the incoming bytes pass through unaltered with the exception of the CLP bit. Note, however, that if the CSILOC[3:0] field is not 0x0, then the Cell ID field will overwrite the selected pre/postpend byte or header byte.

PM:

If the PM bit is a logic 1, performance management is globally enabled. If the PM bit is a logic 0, all performance management cells are ignored at end-points and no statistics are maintained at intermediate points. When performance management is disabled, no physical memory needs to be provided at the SA[19:16]=1101, 1110 and 1111 locations.

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GPOLICE:

If the GPOLICE bit is a logic 1, cell rate policing is globally enabled on all connections. (Policing can be disabled on a per-VC basis by clearing the "Action[1:0]" field in the VC Table to zero.) If the GPOLICE bit is a logic 0, no cell rate policing is performed and no physical memory needs to be provided at the SA[19:16]=0100, 0101, 0110 and 0111 locations.

COUNT:

If the COUNT bit is a logic 1, per-VC counting is globally enabled. If the COUNT bit is a logic 0, the CLP=0 and CLP=1 cell counts are not maintained and no physical memory needs to be provided at the SA[19:16]=1011 and 1100 locations.

GFC:

The GFC bit determines if the GFC field in the ATM header is replaced or passed through unaltered. If GFC is a logic 1, the GFC field in the incoming cell is passed to the outgoing cell. If GFC is a logic 0, the GFC field is replaced by contents of the VC Table. The GFC bit has no effect if the connection belongs to a NNI.

BWDXLAT:

If the BWDXLAT is a logic 1 and GVPIVCI is a logic 1, all backward generated OAM cells have header translation performed on them. If BWDXLAT is a logic 0, the ingress VPI/VCI value is used in the header.

AUTORDI:

The AUTORDI bit enables the generation of RDI cells while in an AIS alarm or Continuity alarm state. If AUTORDI is a logic 1, an RDI cell is presented on the Output Cell Interface immediately upon the reception of the first AIS cell at a flow end-point and once a second thereafter until the AIS state is exited. Likewise, if the CC_RDI bit in the VC table is set, RDI cells are sent once per second if no user or Continuity Check cells have the received in the latest 5.5 +/- 0.5 (default) or 3.5 +/- 0.5 seconds. RDI cells can also be sent if the "Send_RDI" bit in the VC Table Record is set.

VCRAstuff:

If the VCRAstuff bit is a logic 1, all cells routed to the Microprocessor Cell Interface have the HEC and UDF bytes replaced with the VC Table index. This enables the microprocessor to immediately determine the location of a VC record in its data structure without having to perform its own binary search. This feature is provided to enable high speed processing of cells.

The EXTPHYID bit of the Microprocessor Extract Buffer Control and Status register (0x10) takes precedence over the VCRAstuff bit. If the EXTPHYID is set, the HEC byte location of extracted cells will contain the PHY identification regardless of the state of VCRAstuff.

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CSILOC[3:0]:

The CSILOC[3:0] bits determine which appended byte or header byte shall be overwritten with a Cell ID field. This is used to quickly identify Forward RM, Backward RM and generated Backward OAM cells. The CSILOC[3:0] field is encoded as follows:

CSILOC[3:0]	Definition
0000	Disable overwrite
0001	Appended byte 1
0010	Appended byte 2
0011	Appended byte 3
0100	Appended byte 4
0101	Appended byte 5
0110	Appended byte 6
0111	Appended byte 7
1000	Appended byte 8
1001	Appended byte 9
1010	Appended byte 10
1011	Header byte 1
1100	Header byte 2
1101	Header byte 3
1110	Header byte 5
1111	UDF

LB[1:0]:

The LB[1:0] bits determine which loopback cells are copied to the Microprocessor Cell Interface and which loopback cells are dropped (i.e. not presented on the Output Cell Interface):

LB[1:0]	
00	Do not copy; drop at flow end-points.
01	Do not copy; do not drop at flow end-points.
10	Copy and drop loopback cells at flow end-points.
11	Copy for all connections, drop at flow end-points.

UPURS:

The Microprocessor User Reason Symbol (UPURS) bit allows a causation word to be prepended to cell extracted to the Microprocessor Cell Interface. This allows an external microprocessor to immediately determine the reason a cell was routed to the Microprocessor Cell Interface. The extracted cell length will be one greater than the input cell length. Hence, this feature CANNOT be used if the input cell length is 32-words.

See the Microprocessor Interface description in the Functional Description section for a description of the causation word.

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Register 0x19: Performance Monitoring Configuration 1

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	TAGAIS	X
Bit 6	R/W	AISRDIThresh	0
Bit 5	R/W	CCThresh	0
Bit 4	R/W	MERROR[4]	0
Bit 3	R/W	MERROR[3]	0
Bit 2	R/W	MERROR[2]	0
Bit 1	R/W	MERROR[1]	0
Bit 0	R/W	MERROR[0]	0

MERROR[4:0]:

MERROR[4:0] is the binary representation of the threshold of BIP16 violations (BIPV) per performance monitoring block required to declare a Severely Errored Cell Block (SECB). BIPVs are not accumulated for SECBs. If MERROR[4:0] is a binary zero, SECB is not declared as a result of excessive BIPVs.

This threshold applies to both received Forward Monitoring and Backward Reporting cells.

CCThresh:

The CCThresh bit controls the Continuity Check alarm threshold period, and the period at which Continuity Check cells are generated. If CCThresh is a logic 0, the CCalarm threshold period is 5.5 +/- 0.5 sec, and CC cells are generated on two second boundaries. If CCThresh is a logic 1, the Continuity Check alarm threshold period is 3.5 +/- 0.5 sec, and CC cells are generated on one second boundaries.

AISRDIThresh:

The AISRDIThresh bit controls the AIS and RDI alarm threshold periods. If AISRDIThresh is a logic 0, the AIS and RDI alarm thresholds are 3.5 +/- 0.5 seconds. If AISRDIThresh is a logic 1, the AIS and RDI alarm thresholds are 2.5 +/- 0.5 sec.

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TAGAIS:

The TAGAIS bit determines the coding of the Cell Status Information byte that is inserted into the cell header or appended bytes for RCMP-800 generated AIS cells. If TAGAIS is a logic 0, the AIS cell's Cell Status Information byte contains a CELLID[2:0] encoded as 000 binary and the BWDROUTINGTAG[7:3] is not inserted. If TAGAIS is a logic 1, AIS cell's Cell Status Information byte contains a CELLID[2:0] encoded as 011 binary and the BWDROUTINGTAG[7:3] is inserted into the 5 MSBs of the Cell Status Information byte location.

Note that the TAGAIS does not affect the Cell Status Information byte for AIS cells received through the Input Cell Interface or the Microprocessor Cell Interface.

The TAGAIS bit allows a more flexible treatment of generated AIS cells.

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Register 0x1A: Performance Monitoring Configuration 2

Bit	Type	Function	Default
Bit 15	R/W	MMISINS[7]	0
Bit 14	R/W	MMISINS[6]	0
Bit 13	R/W	MMISINS[5]	0
Bit 12	R/W	MMISINS[4]	0
Bit 11	R/W	MMISINS[3]	0
Bit 10	R/W	MMISINS[2]	0
Bit 9	R/W	MMISINS[1]	0
Bit 8	R/W	MMISINS[0]	0
Bit 7	R/W	MLOST[7]	0
Bit 6	R/W	MLOST[6]	0
Bit 5	R/W	MLOST[5]	0
Bit 4	R/W	MLOST[4]	0
Bit 3	R/W	MLOST[3]	0
Bit 2	R/W	MLOST[2]	0
Bit 1	R/W	MLOST[1]	0
Bit 0	R/W	MLOST[0]	0

The threshold given below applies to both received Forward Monitoring and Backward Reporting cells.

MLOST[7:0]:

MLOST[7:0] is the binary representation of the threshold of lost cells per performance monitoring block required to declare a Severely Errored Cell Block (SECB). The number of lost cells is not counted for SECBs. If MLOST[7:0] is a binary zero, SECB is not declared as a result of excessive lost cells.

MMISINS[7:0]:

MMISINS[7:0] is the binary representation of the threshold of misinserted cells per performance monitoring block required to declare a Severely Errored Cell Block (SECB). The number of misinserted cells is not counted for SECBs. If MMISINS[7:0] is a binary zero, SECB is not declared as a result of excessive lost cells.

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Register 0x1B: ABR Cell Rate Policing Configuration

Bit	Type	Function	Default
Bit 15	R/W	GCRA2[7]	0
Bit 14	R/W	GCRA2[6]	0
Bit 13	R/W	GCRA2[5]	0
Bit 12	R/W	GCRA2[4]	0
Bit 11	R/W	GCRA2[3]	0
Bit 10	R/W	GCRA2[2]	0
Bit 9	R/W	GCRA2[1]	0
Bit 8	R/W	GCRA2[0]	0
Bit 7	R/W	GCRA1[7]	0
Bit 6	R/W	GCRA1[6]	0
Bit 5	R/W	GCRA1[5]	0
Bit 4	R/W	GCRA1[4]	0
Bit 3	R/W	GCRA1[3]	0
Bit 2	R/W	GCRA1[2]	0
Bit 1	R/W	GCRA1[1]	0
Bit 0	R/W	GCRA1[0]	0

It is important to note that this configuration register is only valid for ABR connections. ABR connections are designated on a per-VC basis by the CONTYP bit in the Configuration Field of the VC table.

GCRA1[7:0]

The following table indicates upon which cell streams the first cell rate policing instance (GCRA1) acts:

Cell Type	FRM		BRM		OAM		USER	
CLP Bit	0	1	0	1	0	1	0	1
Reg Bit	GCRA1[0]	GCRA1[1]	GCRA1[2]	GCRA1[3]	GCRA1[4]	GCRA1[5]	GCRA1[6]	GCRA1[7]

A logic 1 written to any of the GCRA1[7:0] bits enables GCRA1 policing for that particular cell stream. For example, to enable cell rate policing for GCRA1 on the user CLP=0+1 cell stream, the register configuration would be GCRA2[7:0]=11000000. If GCRA1[7:0] = 00000000, the first GCRA policing instance is globally disabled for ABR connections.

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GCRA2[7:0]

The following table indicates upon which cell streams the second cell rate policing instance (GCRA2) acts:

Cell Type	FRM		BRM		OAM		USER	
CLP Bit	0	1	0	1	0	1	0	1
Reg Bit	GCRA2[0]	GCRA2[1]	GCRA2[2]	GCRA2[3]	GCRA2[4]	GCRA2[5]	GCRA2[6]	GCRA2[7]

A logic 1 written to any of the GCRA2[7:0] bits enables GCRA2 policing for that particular cell stream. If GCRA2[7:0] = 00000000, the second GCRA policing instance is globally disabled for ABR connections.

Note that Resource Management (RM) cells are considered distinct and separate from OAM cells for the purposes of cell rate policing.

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Register 0x1C: VBR/CBR Cell Rate Policing Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	NCOUNT[1]	0
Bit 10	R/W	NCOUNT[0]	0
Bit 9	R/W	POLQNTM[1]	0
Bit 8	R/W	POLQNTM[0]	0
Bit 7	R/W	GCRA2[3]	0
Bit 6	R/W	GCRA2[2]	0
Bit 5	R/W	GCRA2[1]	0
Bit 4	R/W	GCRA2[0]	0
Bit 3	R/W	GCRA1[3]	0
Bit 2	R/W	GCRA1[2]	0
Bit 1	R/W	GCRA1[1]	0
Bit 0	R/W	GCRA1[0]	0

It is important to note that this configuration register is only valid for VBR/CBR connections. VBR/CBR connections are designated on a per-VC basis by the CONTYP bit in the Configuration Field of the VC table.

GCRA1[3:0]:

The GCRA1[2:0] bits determine the cell stream upon which the first cell rate policing instance acts.

Cell Type	OAM		USER	
CLP Bit	0	1	0	1
Reg Bit	GCRA1[0]	GCRA1[1]	GCRA1[2]	GCRA1[3]

A logic 1 written to any of the GCRA1[3:0] bits enables GCRA1 policing for that particular cell stream. For example, to enable cell rate policing for GCRA1 on user CLP=0+1, the register configuration would be GCRA1[3:0] = 1100. If GCRA1[3:0] = 0000, the first GCRA policing instance is globally disabled for VBR/CBR connections.

Note that Resource Management (RM) cells are considered distinct and separate from OAM cells for the purposes of cell rate policing.

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GCRA2[3:0]:

The GCRA2[2:0] bits determine the cell stream upon which the second cell rate policing instance acts.

	Cell Type		OAM	USER
CLP Bit	0	1	0	1
Reg Bit	GCRA2[0]	GCRA2[1]	GCRA2[2]	GCRA2[3]

A logic 1 written to any of the GCRA2[3:0] bits enables GCRA2 policing for that particular cell stream. If GCRA2[3:0] = 0000, the second GCRA policing instance is globally disabled for VBR/CBR connections.

Note that Resource Management (RM) cells are considered distinct and separate from OAM cells for the purposes a cell rate policing.

POLQNTM[1:0]:

The POLQNTM[1:0] bits set the time quantum for the policing functions for **both** ABR and VBR/CBR connections.

POLQNTM[1:0]	SYSCLK Period
00	1 times SYSCLK period.
01	2 times SYSCLK period
10	4 times SYSCLK period
11	8 times SYSCLK period

NCOUNT[1:0]:

The NCOUNT[1:0] bits determine how the non-compliant cell counts of the VC table are defined. NCOUNT[1:0] affects both ABR and non-ABR connections. The following definitions are user programmable:

NCOUNT[1:0]	non-compliant count #1 definition	non-compliant count #2 definition
00	non-compliant CLP=0 cells.	non-compliant CLP=1 cells.
01	dropped CLP=0 cells.	dropped CLP=1 cells.
10	Cells which are non-compliant with GCRA#1	Cells compliant with GCRA#1 which are non-compliant with GCRA#2.
11	Cells which are non-compliant with GCRA#1	Cells which are non-compliant with GCRA#2

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Register 0x1D: Routing Configuration

Bit	Type	Function	Default
Bit 15	R/W	CRC10toUP	0
Bit 14	R/W	DROPCRC10	0
Bit 13	R/W	ACTDEtoOCIF	0
Bit 12	R/W	CCtoUP	0
Bit 11	R/W	DROPINVPTIVCI	0
Bit 10	R/W	DROPBRM	0
Bit 9	R/W	DROPFRM	0
Bit 8	R/W	BADVCtoUP	0
Bit 7	R/W	BRMtoUP	0
Bit 6	R/W	FRMtoUP	0
Bit 5	R/W	ACTDEtoUP	0
Bit 4	R/W	INVPTIVCItoUP	0
Bit 3	R/W	UNDEFtoUP	0
Bit 2	R/W	RDItoUP	0
Bit 1	R/W	AIStoUP	0
Bit 0	R/W	PMtoUP	0

PMtoUP:

If PMtoUP is a logic 1, all Performance Management OAM cells are copied to the Microprocessor Cell Interface. Regardless of the state of this bit, all Performance Management OAM cells are passed to the Output Cell Interface if the RCMP-800 is not an end point for the connection.

AIStoUP:

If the AIStoUP bit is a logic 1, all AIS cells are copied to the Microprocessor Cell Interface. Regardless of the state of this bit, all AIS cells are passed to the Output Cell Interface if the RCMP-800 is not an end point for the connection.

RDItoUP:

If the RDItoUP bit is a logic 1, all RDI cells are copied to the Microprocessor Cell Interface. Regardless of the state of this bit, all RDI cells are passed to the Output Cell Interface if the RCMP-800 is not an end point for the connection.

UNDEFtoUP:

If the UNDEFtoUP bit is a logic 1, all OAM cells with an undefined OAM Type or Function Type value are copied to the Microprocessor Cell Interface. Regardless of the state of this bit, all OAM cells with an undefined OAM Type or Function Type value are passed to the Output Cell Interface if the RCMP-800 is not an end point for the connection.

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INVPTIVCItoUP:

If the INVPTIVCItoUP bit is a logic 1, all VCC cells with an invalid PTI field (PTI=111) and all VPC cells with an invalid VCI field (VCI 7 through 15) are copied to the Microprocessor Cell Interface. The DROPINVPTIVCI register bit determines whether cells with invalid PTI or VCI fields are passed to the Output Cell Interface.

ACTDEtoUP:

If the ACTDEtoUP bit is a logic 1, all activate/deactivate OAM cells are copied to the Microprocessor Cell Interface. Regardless of the state of this bit, all activate/deactivate cells are passed to the Output Cell Interface if the RCMP-800 is not an end point for the connection.

FRMtoUP:

If the FRMtoUP bit is a logic 1, all forward Resource Management (RM) cells are copied to the Microprocessor Cell Interface. Forward RM cells are identified by zero in the DIR bit position in conjunction with PTI=110 for VC-RM cells and by VCI=6 for VP-RM cells. If the VPRMSEL bit of the CRAM Configuration register is a logic 1, VP-RM cells are further qualified by PTI=110.

BRMtoUP:

If the BRMtoUP bit is a logic 1, all backward Resource Management (RM) cells are copied to the Microprocessor Cell Interface. Backward RM cells are identified by a one in the DIR bit position in conjunction with PTI=110 for VC-RM cells and VCI=6 for VP-RM cells. If the VPRMSEL bit of the CRAM Configuration register is a logic 1, VP-RM cells are further qualified by PTI=110.

BADVCtoUP:

If the BADVCtoUP bit is a logic 1, all cells with an unprovisioned VPI/VCI are routed to the Microprocessor Cell Interface for header logging.

DROPFRM:

If the DROPFRM bit is a logic 1, all forward RM cells are dropped (i.e. not passed to the Output Cell Interface). Regardless of the state of this bit, forward RM cells may be routed to the Microprocessor Cell Interface if the FRMtoUP bit is set.

DROPBRM:

If the DROPBRM bit is a logic 1, all backward RM cells are dropped (i.e. not passed to the Output Cell Interface). Regardless of the state of this bit, backward RM cells may be routed to the Microprocessor Cell Interface if the BRMtoUP bit is set.

DROPINVPTIVCI:

The DROPINVPTIVCI bit controls the dropping of VCC cells with an invalid

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PTI and all VPC cells with an invalid VCI field. If DROPINVPTIVCI is a logic 1, all VCC cells with PTI='111' and all VPC cells with a VCI between7 through 15, inclusive, are not routed to the Output Cell Interface. If DROPINVPTIVCI is a logic 0, these cells are passed transparently.

CCtoUP:

If the CCtoUP bit is a logic 1, all Continuity Check cells are copied to the Microprocessor Cell Interface.

ACTDEtoOCIF:

If the ACTDEtoOCIF bit is a logic 1, all Activate/Deactivate cells are routed to the Output Cell Interface. If ACTDEtoOCIF is 0, then at flow end-points, all Activate/Deactivate cells are dropped. Regardless of the state of this bit, all Activate/Deactivate cells are presented by the Output Cell Interface if the RCMP-800 is not a flow end-point.

DROPCRC10:

If the DROPCRC10 bit is a logic 1, all OAM cells with an errored CRC-10 are dropped (i.e. not passed to the Output Cell Interface). Regardless of the state of this bit, if the RCMP-800 is a flow end-point, all OAM cells with an errored CRC-10 are dropped.

CRC10toUP:

If the CRC10toUP bit is a logic 1, all OAM cells with an errored CRC-10 are copied to the Microprocessor Cell Interface. Regardless of the state of this bit, if the RCMP-800 is a flow end-point, all OAM cells with an errored CRC-10 are dropped (i.e. not passed to the output Output Cell Interface). If the RCMP-800 is not an OAM end flow then the state of the DROPCRC10 bit determines whether or not the cell is passed to the Output Cell Interface.

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Register 0x20: CRAM Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	DROPCRCRM	0
Bit 4	R/W	DISVERIFY	0
Bit 3	R/W	LIMITMC	0
Bit 2	R/W	CNTUNDEF	0
Bit 1	R/W	CNTINVPTIVCI	0
Bit 0	R/W	VPRMSEL	0

VPRMSEL:

The VPRMSEL bit controls the identification of the VPC Resource Management (VP-RM) cells. If VPRMSEL is a logic 0, VP-RM cells are identified by a VCI=6; the PTI field is ignored. If VPRMSEL is a logic 1, VP-RM cells are identified by a VCI=6 and a PTI=110. If the PTI field is not equal to 110, the cell is flagged is invalid and optionally can be routed to the Microprocessor Cell Interface.

CNTINVPTIVCI:

The CNTINVPTIVCI controls the counting of cells with invalid PTI or VCI values. If CNTINVPTIVCI is a logic 1, all VCC cells with PTI='111' and all VPC cells with VCI values between 7 and 15, inclusive, result in an increment of the Invalid Cell Count.

CNTUNDEF:

If the CNTUNDEF bit is a logic 1, OAM cells with undefined OAM Type and Function Type fields result in an increment of the Errored OAM Cell Count register. If CNTUNDEF is a logic 0, only CRC-10 errors result in an increment.

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LIMITMC:

If this bit is a '1' then the RCMP-800 limits the maximum size of a multicast set to 64 cells. If this bit is a '0' then a multicast set can be arbitrarily large. Setting this bit to a '1' causes to the RCMP-800 stop processing a multicast linked list after the 64th multicast cell and the set the SRCHERRI register bit. This enables the RCMP-800 to exit a multicast linked list which may have been improperly constructed and contains an endless loop. If it desired to support multicast sets greater then 64 cells the LIMITMC bit should set to a '0'.

DISVERIFY:

The Disable Verify bit controls whether or not the secondary search key is used as part of the cell confirmation step.

If this bit is a logic 1 then, after the VC search is complete, the Secondary search key IS NOT compared to the SA[19:16]=0010 word of the candidate VC Table Record. All cells with a non-null Primary Key will be considered part of a valid connection. This bit will typically be set high if the cell is identified completely using only the Primary Key or if unprovisioned cells are not possible.

If this bit is a logic 0, the binary search is completed with the "confirmation step" which compares the secondary key to the SA[19:16]=0010 word of the candidate VC Table Record.

DROPCRCRM:

If DROPCRCRM is a logic 1, the Resource Management (RM) cells which have a CRC-10 error are dropped.

If DROPCRCRM is a logic 0, the RM cells are transparently passed regardless of whether the CRC10 is in error.

Regardless of the DROPCRCRM bit, RM cells with CRC10 errors are indicated via the INVALI bit of the Master Interrupt Status #1 register (0x02).

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Register 0x21: External RAM Address (LSB)

Bit	Type	Function	Default
Bit 15	R/W	SA[15]	0
Bit 14	R/W	SA[14]	0
Bit 13	R/W	SA[13]	0
Bit 12	R/W	SA[12]	0
Bit 11	R/W	SA[11]	0
Bit 10	R/W	SA[10]	0
Bit 9	R/W	SA[9]	0
Bit 8	R/W	SA[8]	0
Bit 7	R/W	SA[7]	0
Bit 6	R/W	SA[6]	0
Bit 5	R/W	SA[5]	0
Bit 4	R/W	SA[4]	0
Bit 3	R/W	SA[3]	0
Bit 2	R/W	SA[2]	0
Bit 1	R/W	SA[1]	0
Bit 0	R/W	SA[0]	0

This register is used in conjunction with the External RAM Address (MSB) and Access Control register to access the external SRAM.

SA[15:0]:

This register holds the 16 least significant bits of the external SRAM address used for µP accesses. It identifies the desired VC Table Record.

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Register 0x22: External RAM Address (MSB) and Access Control

Bit	Type	Function	Default
Bit 15	R/W	RWB	0
Bit 14	R	BUSY	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SA[19]	0
Bit 2	R/W	SA[18]	0
Bit 1	R/W	SA[17]	0
Bit 0	R/W	SA[16]	0

This register allows the µP to access the external SRAM location addressed by the SA[19:0] bits and perform the operation specified by the RWB bit. Writing to this register with a valid address and RWB bit initiates a µP access request cycle. The contents of the External RAM Address (LSB) register should be set to the desired VC Table Record before this register is written.

SA[19:16]:

The SA[19:16] bits represent the four most significant bits of the external SRAM address used for µP accesses.

BUSY:

The BUSY bit is high while a µP access request to the external SRAM is pending. The BUSY bit goes low after the access has been completed. This register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 37 SYSCLK cycles. If the STANDBY bit in the Master Configuration is a logic 1, the access time is reduced to less than 5 SYSCLK cycles.

RWB:

The RWB bit selects the operation to be performed on the addressed SRAM location: when RWB is set to a logic 1, a read from the external SRAM is requested; when RWB is set to a logic 0, a write to the external SRAM is requested.

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After reading SSRAM address SA[19:16] = {1111, 1110, 1100 or 1011} the RCMP-800 automatically clears (writes all zeros) the location read. A read to these addresses causes the RCMP-800 to perform two SSRAM accesses. First, the read requested. Next, a write of all zeros to the SSRAM location just read.

Similarly, after reading SSRAM address SA[19:16] = 0111, the RCMP-800 clears bits 31:0 of the location just read. Bits 39:32 of the address just read are preserved.

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Register 0x23: External RAM Data (LSB)

Bit	Type	Function	Default
Bit 15	R/W	SD[15]	X
Bit 14	R/W	SD[14]	X
Bit 13	R/W	SD[13]	X
Bit 12	R/W	SD[12]	X
Bit 11	R/W	SD[11]	X
Bit 10	R/W	SD[10]	X
Bit 9	R/W	SD[9]	X
Bit 8	R/W	SD[8]	X
Bit 7	R/W	SD[7]	X
Bit 6	R/W	SD[6]	X
Bit 5	R/W	SD[5]	X
Bit 4	R/W	SD[4]	X
Bit 3	R/W	SD[3]	X
Bit 2	R/W	SD[2]	X
Bit 1	R/W	SD[1]	X
Bit 0	R/W	SD[0]	X

Register 0x24: External RAM Data

Bit	Type	Function	Default
Bit 15	R/W	SD[31]	X
Bit 14	R/W	SD[30]	X
Bit 13	R/W	SD[29]	X
Bit 12	R/W	SD[28]	X
Bit 11	R/W	SD[27]	X
Bit 10	R/W	SD[26]	X
Bit 9	R/W	SD[25]	X
Bit 8	R/W	SD[24]	X
Bit 7	R/W	SD[23]	X
Bit 6	R/W	SD[22]	X
Bit 5	R/W	SD[21]	X
Bit 4	R/W	SD[20]	X
Bit 3	R/W	SD[19]	X
Bit 2	R/W	SD[18]	X
Bit 1	R/W	SD[17]	X
Bit 0	R/W	SD[16]	X

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Register 0x25: External RAM Data (MSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	SD[39]	X
Bit 6	R/W	SD[38]	X
Bit 5	R/W	SD[37]	X
Bit 4	R/W	SD[36]	X
Bit 3	R/W	SD[35]	X
Bit 2	R/W	SD[34]	X
Bit 1	R/W	SD[33]	X
Bit 0	R/W	SD[32]	X

The External RAM Data registers contain either the data to be written into the external SRAM when a write request is initiated or the data read from the external SRAM when a read request has completed. If data is to be written to the external SRAM, these Data registers must be written before the target location's address and RWB=0 is written into the External RAM Address (MSB) and Access Control register, initiating the access. If data is to be read from the external SRAM, only the target location's address and RWB=1 is written into the External RAM Address (MSB) and Access Control register, initiating the request. Within 37 SYSCLK cycles, these registers will contain the requested data word.

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Register 0x26: Maximum VC Table Index

Bit	Type	Function	Default
Bit 15	R/W	MAX[15]	0
Bit 14	R/W	MAX[14]	0
Bit 13	R/W	MAX[13]	0
Bit 12	R/W	MAX[12]	0
Bit 11	R/W	MAX[11]	0
Bit 10	R/W	MAX[10]	0
Bit 9	R/W	MAX[9]	0
Bit 8	R/W	MAX[8]	0
Bit 7	R/W	MAX[7]	0
Bit 6	R/W	MAX[6]	0
Bit 5	R/W	MAX[5]	0
Bit 4	R/W	MAX[4]	0
Bit 3	R/W	MAX[3]	0
Bit 2	R/W	MAX[2]	0
Bit 1	R/W	MAX[1]	0
Bit 0	R/W	MAX[0]	0

MAX[15:0]

The MAX[15:0] bits represent the current maximum VC Table index (SA[15:0]). It is used by the one second servicing algorithm as the first VC Table Record serviced; the index is decremented with each subsequent connection serviced. An accurate value in this location maximizes the efficiency of the RCMP-800. Fixing this register to all ones guarantees all connections will be serviced each second. Do not set MAX[15:0] to a value greater than supported by the depth of SRAM provisioned.

Setting MAX[15:0] to all zeros effectively disables the generation of AIS, RDI and Continuity Check cells and disables the clearing of AIS, RDI and Continuity Check alarms.

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Register 0x27: Search Key Construction

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	PHY[2]	0
Bit 9	R/W	PHY[1]	0
Bit 8	R/W	PHY[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

PHY[2:0]:

The contents of PHY[2:0] determine the number of PHY ID bits in the Primary Search Key. If less than all five PHY address lines should be considered during the key search (as in the case where only a single PHY interface is used) then PHY[2:0] must be programmed with the values below:

PHY[1]	PHY[1]	PHY[0]	Number of PHY ID bits in Primary Key	Number of Supported PHYs
1	1	X	Reserved	-
1	0	1	5	32
1	0	0	4	16
0	1	1	3	8
0	1	0	2	4
0	0	1	1	2
0	0	0	0 (single PHY interface)	1

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Register 0x28: Field A Location and Length

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R/W	LA[4]	0
Bit 11	R/W	LA[3]	0
Bit 10	R/W	LA[2]	0
Bit 9	R/W	LA[1]	0
Bit 8	R/W	LA[0]	0
Bit 7		Unused	X
Bit 6	R/W	SA[6]	0
Bit 5	R/W	SA[5]	0
Bit 4	R/W	SA[4]	0
Bit 3	R/W	SA[3]	0
Bit 2	R/W	SA[2]	0
Bit 1	R/W	SA[1]	0
Bit 0	R/W	SA[0]	0

This register holds the starting location and length of Field A within the Routing Word.

SA[6:0]:

SA[6:0] form the binary address of the MSB of the Field A within the Routing Word. SA[6] is the MSB of the address.

LA[4:0]:

LA[4:0] gives the length of the Field A in bits. The length is stored in LA[4:0] as binary value with LF[4] as MSB. If no Field A is to be used then LA[4:0] should be set to '00000'. Valid values for this field range from '00000' to '10000.' As a programming example: If a 10 bit Field A should be extracted starting at the 120th bit of the Routing Word, we would set LA ='01010' (length = 10) and SA='1110111' (starting address = 119), i.e. write 0x0A77 to 0x28.

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Register 0x29: Field B Location and Length

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	LB[3]	0
Bit 10	R/W	LB[2]	0
Bit 9	R/W	LB[1]	0
Bit 8	R/W	LB[0]	0
Bit 7		Unused	X
Bit 6	R/W	SB[6]	0
Bit 5	R/W	SB[5]	0
Bit 4	R/W	SB[4]	0
Bit 3	R/W	SB[3]	0
Bit 2	R/W	SB[2]	0
Bit 1	R/W	SB[1]	0
Bit 0	R/W	SB[0]	0

This register holds the starting location and length of Field B within the Routing Word.

SB[6:0]:

SB[6:0] form the binary address of the MSB of the Field B within the Routing Word. SB[6] is the MSB of the address.

LB[3:0]:

LB[3:0] gives the length of the Field B in bits. The length is stored in LB[3:0] as binary value with LB[3] as MSB. If no Field B is to be used then LB[3:0] should be set to '0000'. Valid values for this field range from '0000' to '1011.' As a programming example: If a 10 bit Field B should be extracted starting at the 120th bit of the Routing Word, we would set LB ='1010' (length = 10) and SB0='1110111' (starting address = 119), i.e. write 0x0A77 to 0x29.

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Register 0x30: Counter Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	DROPCH	X
Bit 4	R	INVALCH	X
Bit 3	R	OAMERRCH	X
Bit 2	R	OAMCH	X
Bit 1	R	XFER	X
Bit 0	R	OVR	X

This register contains status information indicating when counter data has been transferred into the holding registers and indicating whether the holding registers have been overrun. It also indicates if the any of the counts are non-zero.

DROPCH:

The DROPCH bit is set to logic 1 if the Count of Cells Dropped Due to Congestion is a non-zero value.

INVALCH:

The INVALCH bit is set to logic 1 if the Invalid Cell Count register contains a non-zero value.

OAMERRCH:

The OAMERRCH bit is set to logic 1 if the Errored OAM Cell Count register contains a non-zero value.

OAMCH:

The OAMCH bit is set to logic 1 if the Valid OAM Cell Count register contains a non-zero value.

XFER:

The XFER bit indicates that a transfer of counter data has occurred. A logic 1 in this bit position indicates that a latch request, initiated by writing to one of the counter register locations, was received and a transfer of the counter values has occurred. A logic 0 indicates that no transfer has occurred. The

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XFER bit is cleared (acknowledged) by reading this register. The XFERI bit of the Master Interrupt Status #1 is set when the XFER bit is asserted.

OVR:

The OVR bit is the overrun status of the holding registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFER being logic 1) has not been acknowledged before the next transfer clock has been issued and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. The OVR bit is cleared by reading this register. The XFERI bit of the Master Interrupt Status #1 is set when the OVR bit is asserted.

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Register 0x31: Valid OAM Cell Count

Bit	Type	Function	Default
Bit 15	R	OAM[15]	X
Bit 14	R	OAM[14]	X
Bit 13	R	OAM[13]	X
Bit 12	R	OAM[12]	X
Bit 11	R	OAM[11]	X
Bit 10	R	OAM[10]	X
Bit 9	R	OAM[9]	X
Bit 8	R	OAM[8]	X
Bit 7	R	OAM[7]	X
Bit 6	R	OAM[6]	X
Bit 5	R	OAM[5]	X
Bit 4	R	OAM[4]	X
Bit 3	R	OAM[3]	X
Bit 2	R	OAM[2]	X
Bit 1	R	OAM[1]	X
Bit 0	R	OAM[0]	X

OAM[15:0]:

The OAM[15:0] bits represent the number of valid OAM cells that have been received since the last time the count was transferred. The count is transferred by writing to either address 0x00, 0x31, 0x32, 0x33 or 0x34. Such a write transfers the internally accumulated OAM cell count to this register within three SYSCLK cycles and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

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Register 0x32: Errored OAM Cell Count

Bit	Type	Function	Default
Bit 15	R	OAMERR[15]	X
Bit 14	R	OAMERR[14]	X
Bit 13	R	OAMERR[13]	X
Bit 12	R	OAMERR[12]	X
Bit 11	R	OAMERR[11]	X
Bit 10	R	OAMERR[10]	X
Bit 9	R	OAMERR[9]	X
Bit 8	R	OAMERR[8]	X
Bit 7	R	OAMERR[7]	X
Bit 6	R	OAMERR[6]	X
Bit 5	R	OAMERR[5]	X
Bit 4	R	OAMERR[4]	X
Bit 3	R	OAMERR[3]	X
Bit 2	R	OAMERR[2]	X
Bit 1	R	OAMERR[1]	X
Bit 0	R	OAMERR[0]	X

OAMERR[15:0]:

The OAMERR[15:0] bits represent the number of errored OAM cells that have been received since the last time the count was transferred. The count includes cells with an incorrect CRC-10, an undefined OAM Type field (optional) or an undefined Function Type field (optional). The count is transferred by writing to either address 0x00, 0x31, 0x32, 0x33 or 0x34. Such a write transfers the internally accumulated errored OAM cell count to this register within three SYSCLK cycles and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

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Register 0x33: Invalid Cell Count

Bit	Type	Function	Default
Bit 15	R	INVAL[15]	X
Bit 14	R	INVAL[14]	X
Bit 13	R	INVAL[13]	X
Bit 12	R	INVAL[12]	X
Bit 11	R	INVAL[11]	X
Bit 10	R	INVAL[10]	X
Bit 9	R	INVAL[9]	X
Bit 8	R	INVAL[8]	X
Bit 7	R	INVAL[7]	X
Bit 6	R	INVAL[6]	X
Bit 5	R	INVAL[5]	X
Bit 4	R	INVAL[4]	X
Bit 3	R	INVAL[3]	X
Bit 2	R	INVAL[2]	X
Bit 1	R	INVAL[1]	X
Bit 0	R	INVAL[0]	X

INVAL[15:0]:

The INVAL[15:0] bits represent the number of cells with invalid headers that have been received since the last time the count was transferred. The count includes cells with an unprovisioned VPI/VCI or with undefined PTI values (optional). The count is transferred by writing to either address 0x00, 0x31, 0x32, 0x33 or 0x34. Such a write transfers the internally accumulated invalid cell count to this register within three SYSCLK cycles and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

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Register 0x34: Count of Cells Dropped Due to Congestion

Bit	Type	Function	Default
Bit 15	R	DROP[15]	X
Bit 14	R	DROP[14]	X
Bit 13	R	DROP[13]	X
Bit 12	R	DROP[12]	X
Bit 11	R	DROP[11]	X
Bit 10	R	DROP[10]	X
Bit 9	R	DROP[9]	X
Bit 8	R	DROP[8]	X
Bit 7	R	DROP[7]	X
Bit 6	R	DROP[6]	X
Bit 5	R	DROP[5]	X
Bit 4	R	DROP[4]	X
Bit 3	R	DROP[3]	X
Bit 2	R	DROP[2]	X
Bit 1	R	DROP[1]	X
Bit 0	R	DROP[0]	X

DROP[15:0]:

The DROP[15:0] bits represent the number of cells that have been discarded due to an assertion of the CONG input since the last time the count was transferred. The count is transferred by writing to either address 0x00, 0x31, 0x32, 0x33 or 0x34. Such a write transfers the internally accumulated dropped cell count to this register within three SYSCLK cycles and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

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Register 0x38: Output Cell FIFO Configuration

Bit	Type	Function	Default
Bit 15	R/W	HECUDF	1
Bit 14	R/W	OCAINV	0
Bit 13	R/W	CELLPOST[3]	0
Bit 12	R/W	CELLPOST[2]	0
Bit 11	R/W	CELLPOST[1]	0
Bit 10	R/W	CELLPOST[0]	0
Bit 9	R/W	CELLLEN[3]	0
Bit 8	R/W	CELLLEN[2]	0
Bit 7	R/W	CELLLEN[1]	0
Bit 6	R/W	CELLLEN[0]	0
Bit 5	R/W	OBYTEPRTY	0
Bit 4	R/W	OPTYP	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	OCALEVEL0	1
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the four cell output FIFO. When FIFORST is set to logic 0, the FIFO operates normally. When FIFORST is set to logic 1, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic 0 is written to FIFORST.

It is recommended that, whenever any other bit in this register is changed, FIFORST be set to logic one upon the change and set to logic zero after.

The FULLI bit of the Master Interrupt Status #1 register (0x01) may become a logic 1 as a result of setting the FIFORST bit. With the output FIFO reset, it is unable to accept any cells, which is the same immediate symptom as a full buffer.

OCALEVEL0:

The OCALEVEL0 bit determines what the OCA output indicates when it transitions inactive. When OCALEVEL0 is set to logic 1, a deassertion of the OCA[1] outputs indicate that the output FIFO is empty. When OCALEVEL0 is set to logic 0, a deassertion of the OCA output indicates that the output FIFO is near empty and contains only four words.

OPTYP:

The OPTYP bit selects even or odd parity for outputs OPRTY[1:0]. When set to logic 1, output OPRTY[1] is the even parity bit for outputs ODAT[15:8] and

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output OPRTY[0] is the even parity bit for outputs ODAT[7:0]. When set to logic 0, OPRTY[1:0] are the odd parity bits for outputs ODAT[15:0].

OBYTEPRTY:

The output byte parity, OBYTEPRTY, mode bit selects between byte and word parity mode for the OPRTY[1:0] outputs. When the OBYTEPRTY bit is set to logic one, byte parity mode is selected, otherwise, word parity mode is selected. In byte parity mode, OPRTY[1] is the (odd or even) parity bit for the ODAT[15:8] outputs, and OPRTY[0] is the parity bit for the ODAT[7:0] outputs. In word parity mode, OPRTY[1] is the (odd or even) parity bit calculated for all 16 ODAT[15:0] outputs, and OPRTY[0] is held low. Word parity mode can only be selected when the OBUS8 input is low (i.e., the 16-bit FIFO interface is selected).

CELLLEN[3:0]:

The CELLLEN[3:0] bits determine the number of words in the output cell.

When OBUS8 is a logic 1, the binary CELLLEN[3:0] value is the number of bytes appended to the basic 53 byte ATM cell. The maximum cell length is 63 bytes; therefore, a CELLLEN[3:0] greater than 10 decimal results in 10 appended bytes.

When OBUS8 is a logic 0, the binary CELLLEN[3:0] value is the number of words appended to the basic 27 word ATM cell. The maximum cell length is 32 words; therefore, a CELLLEN[3:0] greater than 5 decimal results in 5 appended bytes.

CELLPOST[3:0]:

The CELLPOST[3:0] bits determine the number of words in the output cell post-pend. The numerical difference between CELLLEN[3:0] and CELLPOST[3:0] represents the number of words in the pre-pend. It is inappropriate that CELLPOST[3:0] exceed CELLLEN[3:0].

When OBUS8 is a logic 1, the binary CELLPOST[3:0] value is the number of bytes post-pended to the basic 53 byte ATM cell. When OBUS8 is a logic 0, the binary CELLPOST[3:0] value is the number of words post-pended to the basic 27 word ATM cell.

OCAINV:

The OCAINV bit selects the active polarity of the OCA signal. The default configuration selects OCA to be active high, indicating that a cell is available when high. When OCAINV is set to logic one, the OCA signal becomes active low. If the state of the OCAINV bit has been changed, the output FIFO must be reset via the FIFORST bit in order to properly initialize the OCA output.

HECUDF:

The HECUDF bit determines whether or not the HEC/UDF octets are included

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in cells transferred over the output cell interface. When set to logic 1 (default), the HEC and UDF octets are included. When set to logic 0, these octets are omitted, i.e., if BUS8 is logic 0, the third word of the 27-word ATM cell is omitted and a 26-word cell (plus appended words) is transferred. If BUS8 is logic 1, the fifth octet of the 53-octet ATM cell is omitted and a 52-octet cell (plus appended octets) is transferred.

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Register 0x3A: Output Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	OCELL[15]	X
Bit 14	R	OCELL[14]	X
Bit 13	R	OCELL[13]	X
Bit 12	R	OCELL[12]	X
Bit 11	R	OCELL[11]	X
Bit 10	R	OCELL[10]	X
Bit 9	R	OCELL[9]	X
Bit 8	R	OCELL[8]	X
Bit 7	R	OCELL[7]	X
Bit 6	R	OCELL[6]	X
Bit 5	R	OCELL[5]	X
Bit 4	R	OCELL[4]	X
Bit 3	R	OCELL[3]	X
Bit 2	R	OCELL[2]	X
Bit 1	R	OCELL[1]	X
Bit 0	R	OCELL[0]	X

Register 0x3B: Output Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	OCELL[23]	X
Bit 6	R	OCELL[22]	X
Bit 5	R	OCELL[21]	X
Bit 4	R	OCELL[20]	X
Bit 3	R	OCELL[19]	X
Bit 2	R	OCELL[18]	X
Bit 1	R	OCELL[17]	X
Bit 0	R	OCELL[16]	X

OCELL[23:0]:

The OCELL[23:0] bits indicate the number of cells read from the output FIFO during the last accumulation interval.

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A write to either address 0x00, 0x3A or 0x3B loads the registers with the current counter value and resets the internal 24 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Output Cell Counter registers. The counter should be polled at least every 10 seconds to avoid saturating. The contents of these registers are valid within four OFCLK cycles after a transfer is triggered by a write to the Output Cell Count register space.

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TEST FEATURES DESCRIPTION

Simultaneously forcing the CSB, RDB and WRB inputs low causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the RCMP-800. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[6]) is high.

The RCMP-800 supports a standard IEEE 1149.1 five signal JTAG boundary scan test port for use in board testing. All digital device inputs except SD[39:0] and SP[4:0] may be read and all digital device outputs except SD[39:0]. SP[4:0], SADSB, SRWB, SOEB and SA[19:0] may be forced via the JTAG test port.

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Register 0x40: Master Test

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	X
Bit 2	R/W	Reserved	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to enable RCMP-800 test features. All bits, except PMCTST, are reset to zero by a reset of the RCMP-800.

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tristate modes of the RCMP-800 . While the HIZIO bit is a logic 1, all output pins of the RCMP-800 except the data bus and output TDO. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1 and PMCTST is logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the RCMP-800 to drive the data bus and holding the CSB pin low tristates the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST:

The PMCTST bit is used to configure the RCMP-800 for PMC's manufacturing tests. When PMCTST is set to logic 1, the RCMP-800 microprocessor port becomes the test access port used to run the PMC "canned" manufacturing

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test vectors. The PMCTST bit can be cleared by setting CSB to logic 1 or by writing logic 0 to the bit.

Test Mode 0 Details

The RCMP-800 allows the logic levels on the device inputs to be read through the microprocessor interface.

To enable test mode 0, the following addresses must be written with 0x0000: 0x49, 0x59, 0x61 and 0x79. Reading the following address locations returns the values for the indicated inputs :

	0x41	0x48	0x4A	0x5C	0x62	0x63	0x64	0x7A	0x7B
D[15]		IDAT[15][1]			SD[15]	SD[31]			
D[14]		IDAT[14][1]			SD[14]	SD[30]			
D[13]		IDAT[13][1]	IPOLL		SD[13]	SD[29]			
D[12]		IDAT[12][1]			SD[12]	SD[28]	SP[4]		
D[11]		IDAT[11][1]	IBUS8	CONG	SD[11]	SD[27]	SP[3]	OBUS8	
D[10]		IDAT[10][1]	ISOC[1]		SD[10]	SD[26]	SP[2]		
D[9]		IDAT[9][1]	IPRTY[1][1]		SD[9]	SD[25]	SP[1]		
D[8]		IDAT[8][1]	IPRTY[0][1]		SD[8]	SD[24]	SP[0]		
D[7]		IDAT[7][1]	ICA[4][1]		SD[7]	SD[23]	SD[39]		
D[6]		IDAT[6][1]	ICA[3][1]		SD[6]	SD[22]	SD[38]		
D[5]		IDAT[5][1]	ICA[2][1]		SD[5]	SD[21]	SD[37]		
D[4]	ONESEC	IDAT[4][1]	ICA[1][1]		SD[4]	SD[20]	SD[36]		
D[3]	TCK	IDAT[3][1]			SD[3]	SD[19]	SD[35]		
D[2]	TRSTB	IDAT[2][1]			SD[2]	SD[18]	SD[34]		
D[1]	TMS	IDAT[1][1]			SD[1]	SD[17]	SD[33]		
D[0]	TDI	IDAT[0][1]			SD[0]	SD[16]	SD[32]		ORDENB

Notes:

1.) Must be clocked by IFCLK before being read.

The following inputs can not be read using the TM0 feature: SYSCLK, IFCLK, OFCLK, D[15:0], A[6:0], ALE, CSB, WRB, RDB and RSTB.

The SRAM interface pins can be controlled via the External RAM Address and External RAM Data registers (0x21 through 0x25).

JTAG Test Port

The RCMP-800 JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

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Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Identification Register

Length - 32 bits
Version number - 0H
Part Number - 7322H
Manufacturer's identification code - 0CDH
Device identification - 073220CDH

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Boundary Scan Register

The least significant bit is the first bit to be scanned in on TDI and scanned out on TDO.

Length - 92 bits

Pin/Enable	Type	Boundary Scan Register Bit	Pin/Enable	Type	Boundary Scan Register Bit
SYSCLK	I	91	CSB	I	33
IDAT[15:0]	I	90:75	WRB	I	32
IPRTY[1:0]	I	74:73	RDB	I	31
ISOC	I	72	RSTB	I	30
IFCLK	I	71	INTB	O	29
IAVALID_ICA[4]	I/O	70	DREQ	O	28
IADDR_OEB (for IAVALID_ICA[4] & IADDR_ICA[3:2])	E	69	OTSEN	I	27
IADDR_ICA[3:2]	I/O	68:67	OBUS8	I	26
ICA[1]	I	66	ORDENB	I	25
IADDR_IWRENB[4:2]	O	65:63	OCA	O	24
IWRENB[1]	O	62	OFCLK	I	23
IPOLL	I	61	OSOC	O	22
IBUS8	I	60	ODATOEB (for ODAT[15:0], OSOC and OPRTY[1:0]	E	21
ONESEC	I	59	OPRTY[1:0]	O	20:19
D[15:0]	I/O	58:43	ODAT[15:0]	O	18:3
DOEB (for D[15:0])	E	42	BUSYB	O	2
A[6:0]	I	41:35	CONG	I	1
ALE	I	34	HIZ*	E	0

* The HIZ enable tristates IADDR_IWRENB[4:2], IWRENB[1], DREQ, OCA, BUSYB, SA[19:0], SOEB, SADSB, SRWB if set to a logic 1.

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OPERATION

SCI-PHY Extended Cell Format

The SCI-PHY extended cell format is a recent enhancement of the SCI-PHY bus standard described in the "Saturn Compliant Interface for ATM Devices" document (PMC940102). The extension allows for the appending of up to 10 bytes of additional information.

Figures 6 and 7 illustrate the 8 bit wide and 16 bit wide data structures. The length of the pre-pends and post-pends are independently programmable for each interface.

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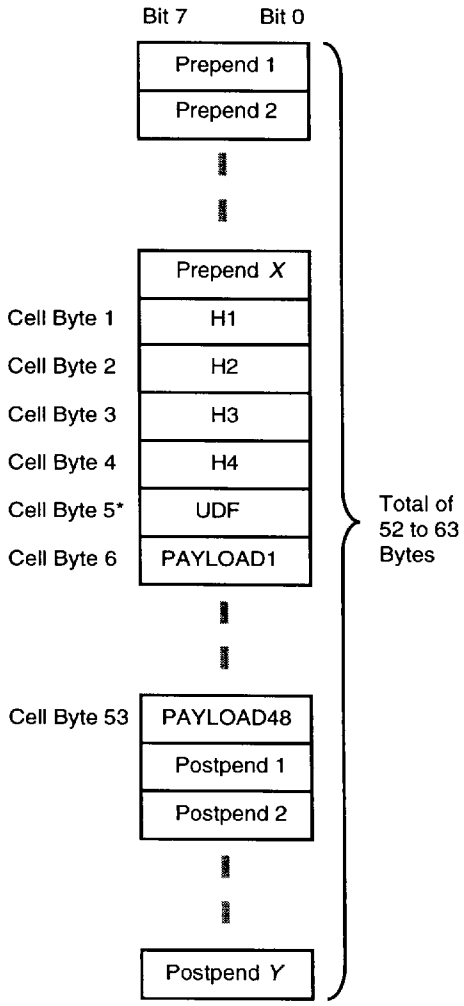
Fig. 6 Eight Bit Wide Cell Format



* Cell Byte 5 may optionally be omitted.

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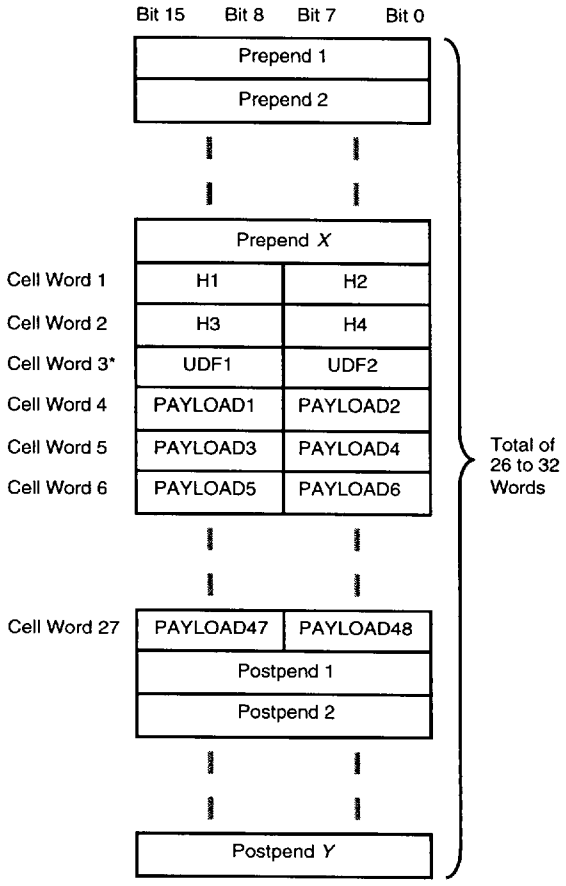
Fig. 7 Sixteen Bit Wide Cell Format



* Cell Word 3 may optionally be omitted.

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Synchronous Static RAMs

The RCMP-800 interfaces directly to synchronous static RAMs commonly used as cache for Intel Pentium and i486 processors.

Vendor	Device	Configuration	Access Time	Max. Frequency
Cypress	CY7C1031-12	64K x 18	14 ns	50 MHz
	CY7C1031-10	64K x 18	12 ns	66 MHz
Motorola	MCM67x618-11	64K x 18	11 ns	66 MHz
	MCM67x618-14	64K x 18	14 ns	66 MHz
SGS-Thomson	M67H618-14	64K x 18	14 ns	50 MHz
	M67H618-12	64K x 18	12 ns	66 MHz
Micron	MT58LC36K32B2	64K x 18		50 MHz
	MT58LC36K32M1	64K x 18		50 MHz
	MT58LC36K32C4	64K x 18		50 MHz
	MT58LC36K32A6	64K x 18		50 MHz
	MT58LC36K32B2	32K x 36	-	50 MHz
Hitachi	HM67B3632-12	32K x 36	12 ns	50 MHz
Samsung	KM718B86-9	64K x 18	9 ns	66 MHz
	KM718B86-10	64K x 18	10 ns	58 MHz
	KM718B86-12	64K x 18	12 ns	50 MHz

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OAM Cell Format

The automatic OAM cell handling supports a subset of the information fields. The processing of particular fields is not practical on the RCMP-800. Cells can be dropped to the Microprocessor Cell Interface for external processing if required. This section describes the processing of received OAM cells and the coding of fields in the generated OAM cells.

Received OAM Cells

The following illustrates the active fields in the received OAM cells. Any unsupported fields are ignored.

AIS:

OAM Type (4 bits)	Function Type (4 bits)	Function Specific Fields (45 octets)	Reserved (6 bits)	Error Detection Code (10 bits)
0001	0000	Don't care	Don't care	CRC-10

RDI:

0001	0001	Don't care	Don't care	CRC-10

Continuity Check:

0001	0100	Don't care	Don't care	CRC-10

Loopback:

0001	1000	Don't care	Don't care	CRC-10

Forward Monitoring Performance Management:

0010	0000		Don't care	CRC-10

MSN (1 oct.)	TUC (2 oct.)	BIP-16 (2 oct.)	Time Stamp Don't care (4 octets)	Unused Don't care (36 octets)

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Backward Reporting Performance Management:

0010	0001		Don't care	CRC-10

Unused Don't care (5 octets)	Time Stamp Don't care (4 oct.)	Unused Don't care (29 oct.)	Delay Result Don't care (4 oct.)	Block Error Result (1 oct.)	Lost/Misdelivered Cell Count (2 octets)

Monitoring & Reporting Performance Management:

0010	0010		000000	CRC-10

MSN (1 oct.)	TUC (2 oct.)	BIP-16 (2 oct.)	Time Stamp Don't care (4 octets)	Unused Don't care (29 octets)	Delay Result Don't care (4 oct.)	Block Error Result (1 oct.)	Lost/ Misdelivered Cell Count (2 octets)

Activation/Deactivation:

1000	Don't Care	Don't care	Don't care	CRC-10

The Error Detection Code (EDC) is verified for all received OAM cells. The polynomial represented by the 48 octet information field is divided by $x^{10}+x^9+x^5+x^4+x+1$. All OAM cells which have an all zeros remainder are processed. Cells with an incorrect EDC are discarded.

If either the AIStoUP or the RDItoUP register bit is set, the associated cell type is copied to the Microprocessor Cell Interface for OAM flows terminated by this RCMP-800. This allows for external processing of the Failure Type and Failure Location fields.

If the UNDEFtoUP register bit is set, OAM cells with undefined OAM Type fields are routed to the Microprocessor Cell Interface for OAM flows terminated by this RCMP-800.

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Generated OAM Cells

The following illustrates the coding of fields in the generated OAM cells. The coding of all supported fields is in accordance with the quoted references. Unsupported fields are coded with the specified defaults.

AIS:

OAM Type (4 bits)	Function Type (4 bits)	Function Specific Fields (45 octets)	Reserved (6 bits)	Error Detection Code (10 bits)
0001	0000	all octets 6AH	000000	CRC-10

RDI:

0001	0001	all octets 6AH	000000	CRC-10

Continuity Check:

0001	0100	all octets 6AH	000000	CRC-10

Forward Monitoring Performance Management:

0010	0000		000000	CRC-10

MSN (1 oct.)	TUC (2 oct.)	BIP-16 (2 oct.)	Time Stamp FFH (4 octets)	Unused 6AH (36 octets)

The Monitoring Cell Sequence Number (MSN) is incremented with each generated PM cell for the connection. The Total User Cell (TUC) number is incremented with each user cell received and is never reset. The BIP-16 value is calculated over all user cells since the last forward monitoring cell.

Backward Reporting Performance Management:

0010	0001		000000	CRC-10

Unused 6AH (42 oct.)	Block Error Result (1 oct.)	Lost/Misdelivered Cell Count (2 octets)

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The Block Error Result contains the BIPV for the forward monitoring cell received. If the BIPV is undefined, which occurs when the MSN is not expected or the Total User Cell Difference (TUCD) is non-zero, the Block Error Result is coded as all ones. The Lost/Misdelivered Cell Count is coded with the absolute value of the TUCD in the 15 least significant bits and a one in the most significant bit position if TUCD is negative (i.e. cells have been lost.) Misinserted cells result in a zero in the most significant bit position.

The RCMP-800 does not generate combined Monitoring/Reporting cells.

The RCMP-800 does not automatically generate Activation/Deactivation and Loopback cells. These can be inserted through the Microprocessor Cell Interface. The microprocessor is responsible for coding all fields except the CRC-10.

All generated OAM cells contain a correct Error Detection Code (EDC).

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VC Identification Search Algorithm

Within the constraints imposed by the Primary and Secondary Search Table coding rules, numerous search algorithms are supported. The building of a search data structure is a software function and is normally performed by the supervising microcontroller. A shadow data structure is required by the microcontroller to enact the modifications to the data structure. (It is possible to avoid using a shadow data structure, but efficiency is reduced by the need to perform searches through multiple SRAM accesses via the RCMP-800, each taking up to 800ns. Also, diagnostic possibilities are reduced.)

The algorithm presented below has the following features which optimize it for VC identification:

1.) Only those bits in the Secondary Search Key required to make an unique identification are examined. This minimizes the average search time.

2.) The number of nodes in the Secondary Search Table is bounded by the number of VC Table entries. Therefore, the depth of memory required for the Secondary Search Table is equal to that required for the VC Table.

3.) Nodes can be added or deleted on the fly without corrupting a binary search in progress.

A C-language example of the algorithm will be made available.

Overview

The VC search algorithm maps the cell's PHY identifier, VCI, VPI and selected portions of appended bytes to a 16-bit VC Table address. Effectively, it performs the operation of a Content Addressable Memory (CAM). The data structure created to support the VC identification is designed around maximizing the efficiency of the process.

It is the Select field in the Secondary Search Table which makes the search efficient, because it allows each branching decision to be made based on only the first bit in which two branches differ. That is, as two values are compared, starting with the MSB (most significant bit) and moving to the LSB (least significant bit), the two can be fully discriminated based on the first bit in which they differ. No other bits after that bit, regardless of how much they differ, need to be considered. Because not all bits are not examined in the binary search, the search is concluded with a

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confirmation step which compares the Secondary Search Key against the VPI/VCI of the candidate VC Table.

The following sub-sections describe the search table initialization, connection addition and connection removal processes. Refer to the VC Identification sub-section of the Functional Description section for definitions of the Primary and Secondary Search Keys, for an overview of the search process and for a definition of the data structures.

Initialization

The following are the microcontroller actions required to initialize the Search Tables and VC Tables:

1.) Set the STANDBY bit of the Master Configuration register (0x01) if not already set by an asynchronous reset.

1.) Write zeros (null pointer) to every Primary Search Table location (SA[19:16] = 0001).

2.) Write zeros to the fourth word (SA[19:16]=0011) of all VC Table entries. This clears the "Active" bit in the CONFIG field.

3.) Clear the STANDBY bit of the Master Configuration register (0x01).

The remaining SRAM locations can be initialized when required.

Adding a Connection

The following are the microcontroller actions required to provision a connection:

1.) Determine the next available VC Table address. Initialize the contents of the VC Table Record via the Microprocessor RAM Address and Data registers (0x21 through 0x25). Care should be taken to set the following fields appropriately:

All counts should be set to zero.
The "PM0" field should be set to one.
The "Extended Status" field should be set to 0x050.
The "Active" bit of the "Config" field should be set to one.

2.) Perform a binary search to determine the insertion point. The last pointer accessed in the search shall be the one modified, be it a Primary Search Table entry, left branch or right branch.

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3.) Find a free Secondary Search Table entry and initialize it. The only exception to this is when a single VC Table Record exists in a tree, in which case the solitary Secondary Search Table entry is modified.

The value of the "Select" is set to the index of the most significant bit which differs between the new VC and the "nearest" existing VC, which was found in step 2. A few insights need highlighting:

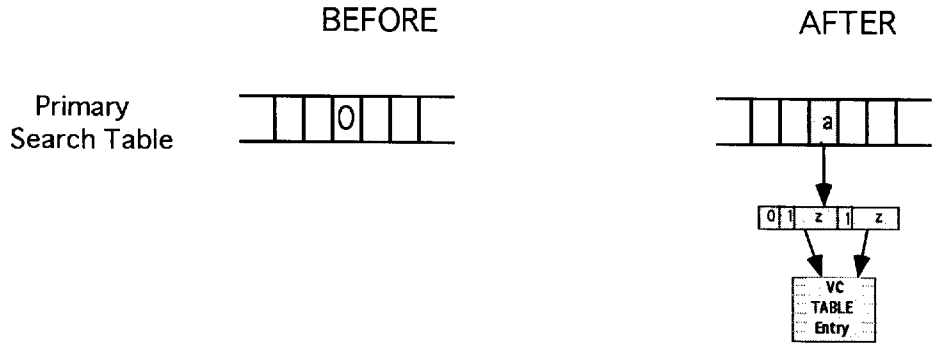
1.) If there is an overlap between Primary and Secondary Search keys (eg. the Primary key is the VPI), the intersecting bits are excluded from the binary search based on the fact they will always be the same in both keys.

2.) Due to fact that the Primary Search key includes the PHY identification, NNI and UNI connections will never reside in the same binary tree. Therefore, the "Select" determination algorithm need all start its bit comparison at the correct bit (the first bit of the ATM header for NNI and the fifth bit of the ATM header for UNI) to ensure a valid search tree.

4.) Perform a SRAM write (via the Microprocessor RAM Address and Data registers) to incorporate the new Secondary Search Table entry in the existing tree structure. This step must be performed last to ensure a binary search in progress is not corrupted.

Five distinct types of insertions are possible based on the existing tree structure:

1.) The binary tree is empty. In this case, the null primary search table pointer is modified to point to a newly created Secondary Search Table entry. Because no bits within the Secondary Search Key are required, both the left and right branches of the Secondary Search Table entry point to the same VC Table Record. The "select" field should be set to zero.



Key to data structure diagrams:
a, b, c - pointers to Secondary Search Table entries
w, x, y, z - pointers to VC Table entries

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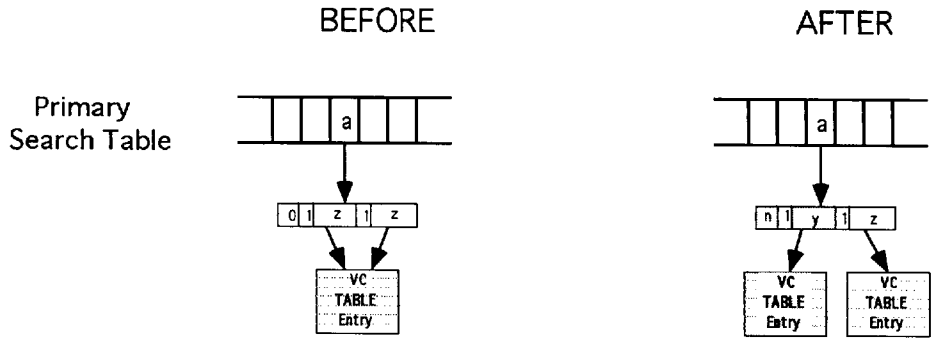
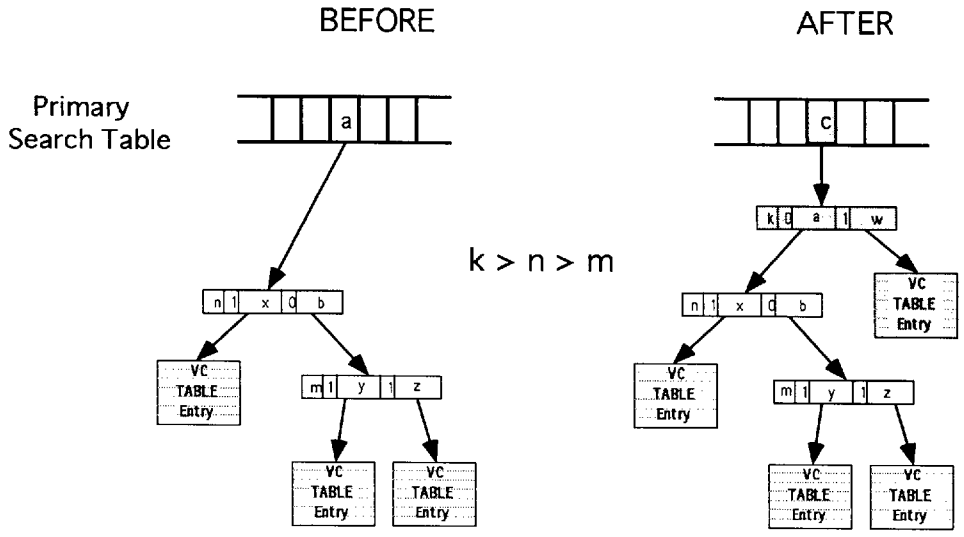
k,m,n - "select" field contents
The shaded boxes indicate those fields which have been created or modified.

2.) The binary tree contains only a single VC Table Record. Modify the "select" field to index the most significant bit of the Secondary Search Key which differs between the new and existing connection. Modify the left or right branch, as appropriate, to point to the newly created VC Table Record.



The diagram illustrates the case where the new VC has a one in the decision bit position and the existing VC has a zero in the same bit position. If the new VC had a zero in the decision bit position, the right branch would have been modified instead.

3.) The insertion point is at the root of the tree. This occurs when the new decision bit index is greater any of the indices currently in the search tree. In this case, the Primary Search Table entry is modified to point to the newly created Secondary Search Table entry. The New Secondary Search Table entry points to the new VC Table Record and the old tree root.



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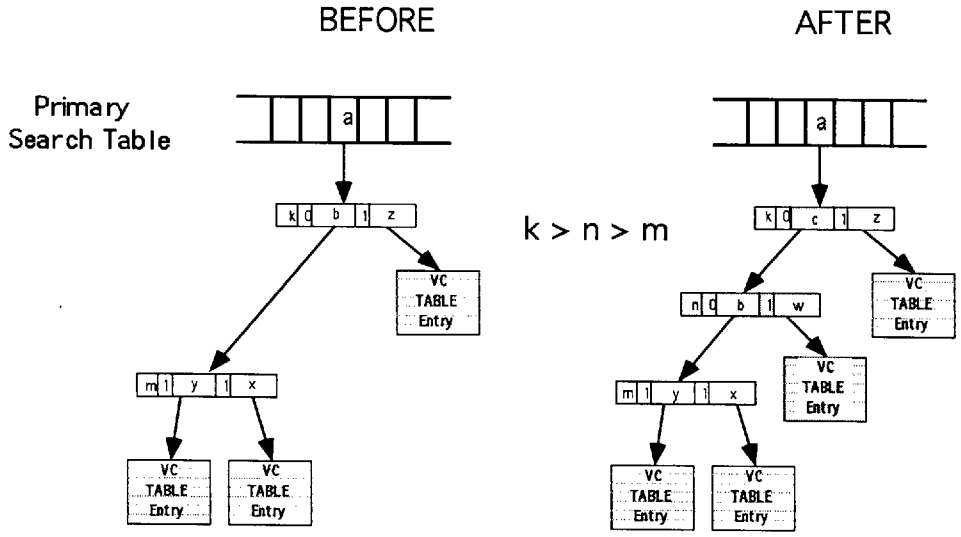
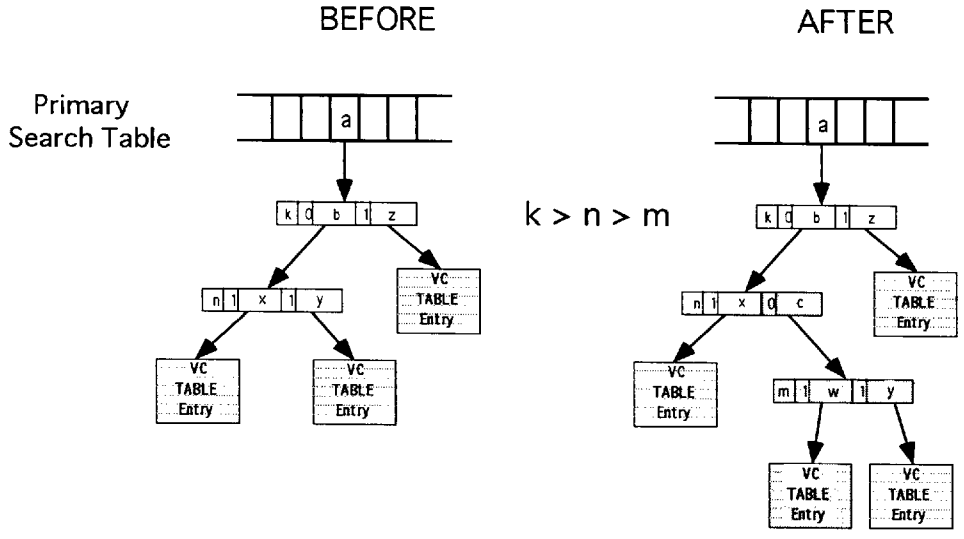
4.) The insertion point is in the middle of the binary tree. The new Secondary Search Table entry points to the new VC Table Record and an existing node in the tree. The parent of the existing node is modified to point to the new Secondary Search Table entry in the final step of the insertion.



5.) The new Secondary Search Table entry is inserted at a leaf. The search for a candidate insertion point ends on a node which already points to a VC Table Record. The new Secondary Search Table entry points to the existing VC Table Record and the new VC Table Record. The existing Secondary Search Table entry is modified to point to the new Secondary Search Table entry in the final step of the insertion.



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Removing a Connection

The following are the microcontroller actions required to remove a connection:

1.) Find the location of the Secondary Search Table entry pointing to the connection's VC Table Record.

2.) Modify the parent node (be it the Primary Table entry or another Secondary Search Table entry) of the Secondary Search Table entry being removed to point to the node remaining after the connection removal. The only exception to this is when two VC Table entries exist in a tree, in which case the solitary Secondary Search Table entry is modified. The VC is now considered unprovisioned and any cells belonging to the VC will be discarded.

3.) Tag the removed Secondary Search Table entry as free.

4.) Read the final statistics for the connection from the VC Table Record. Clear the "Active" bit of the CONFIG VC Table Record field and tag the record as free.

The connection removal process examples are not illustrated because the results are exactly the reverse of the connection provisioning. (Swap the "BEFORE" and "AFTER" labels.)

Multicast Connections

The search table may be constructed so a single received cell results in an arbitrary number of output cells. This is achieved through a linked list of Secondary Search Table entries, each with an associated VC Table Record which defines the characteristics of a outgoing VC. Adding and removing multicast VCs is done by manipulating the linked list.

All ones in the Select field of the Secondary Search Table entry identifies it as a multicast linked list element, except for the last in the linked list. The Left_Branch field contains the VC table address of the multicast VC. The Right_Branch field points to the Search Table address of the next VC in the multicast. The linked list is terminated by setting the Select field to an all zeroes value. An all zeroes value in the Select field indicates that the Left_Branch field provides the final VC Search Table Address of the multicast set.

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Adding a Multicast Connection

A multicast VC is inserted at the head of the linked list. The following are the microcontroller actions required to provision a multicast connection:

1.) Determine the next available VC Table address. Initialize the contents of the VC Table Record via the Microprocessor RAM Address and Data registers (0x21 through 0x25).

2.) Perform a binary search to determine the head of the linked list. If the binary search terminates at a VC Table Record which does not match the candidate search key (i.e. empty list), the insertion proceeds as for a non-multicast connect as described above.

3.) Find a free Secondary Search Table entry and initialize it. Set the Left_Branch to point to the VC Table address of the new VC Table Record. Set the Right_Branch to point to the Search Table address of the old head of the linked list.

An extra step is required when a unicast VC is converted to a multicast with two VCs. A second Secondary Search Table entry needs to be allocated whose Left_Branch points to the existing VC Table Record. (Although not used, it is suggested that the Right_Branch be set to all zeroes.) Set the Select field to an all zeroes value to indicate this is the end of the linked list. The new VC forms the head of the two element linked list.

4.) Perform an SRAM write (via the Microprocessor RAM Address and Data registers) to incorporate the new Secondary Search Table entry in the existing tree structure. This step must be performed last to ensure a binary search in progress is not corrupted.

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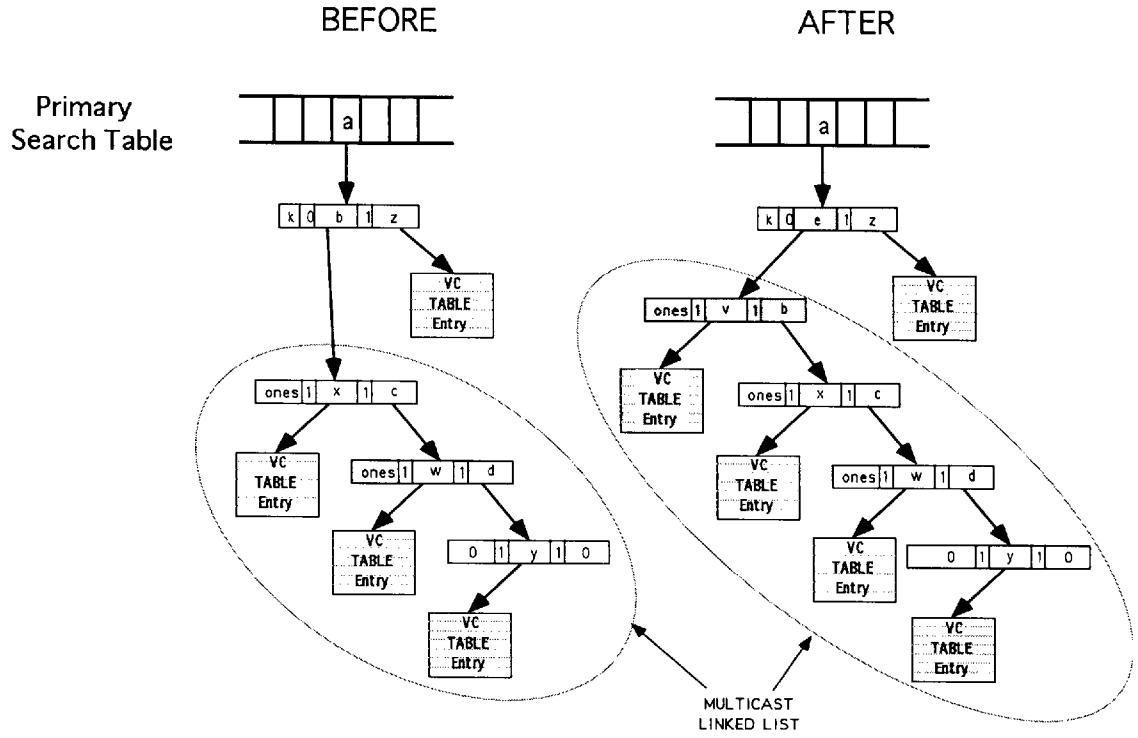
The following diagram provides an example of an insertion.



Removing a Multicast Connection

Because each multicast Virtual Connection has an incoming VPI/VCI combination identical to the other VCs in the multicast, the contents of the VC Table entries must be examined to isolate the VC to be removed. Once identified, the linked list is modified to bypass the VC.

The steps required to remove one element of a multicast are:

1.) Find the location of the Secondary Search Table entry pointing to the head of the multicast linked list.

2.) Traverse the linked list to find the VC to be removed.

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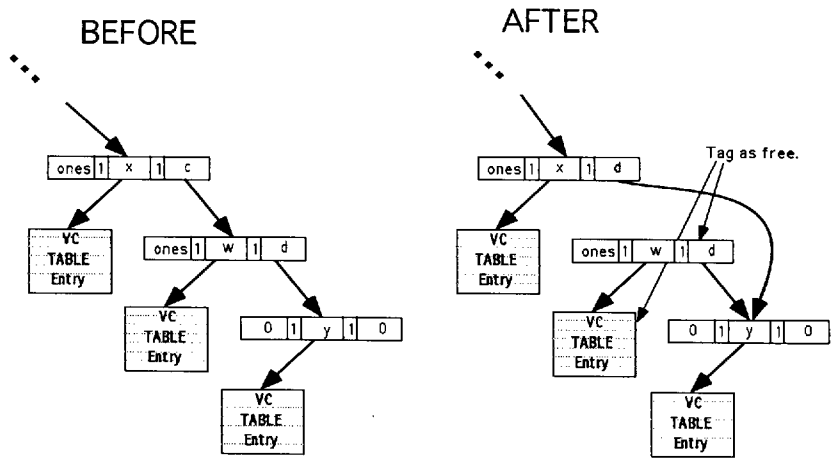
3.) Modify the Secondary Search Table entry pointing to the node being removed to point to the node following the one being removed, as illustrated below. The VC is now considered unprovisioned.



Two special cases need to be accommodated:

i.) The VC to be removed is the tail of the list. In this case, the parent node becomes the new tail and its Select field should be modified to be all zeroes.

ii.) The removal leaves only one VC in the multicast. The pointer to the head of the list, should be modified to point to the surviving VC Table Record. Two Secondary Search Table entries are freed up.

4.) Tag the removed Secondary Search Table entry (or entries) as free.

5.) Clear the "Active" bit of the CONFIG VC Table Record field and tag the record as free. If the removed VC was the head of the linked list, read the final statistics for the connection from the VC Table Record.

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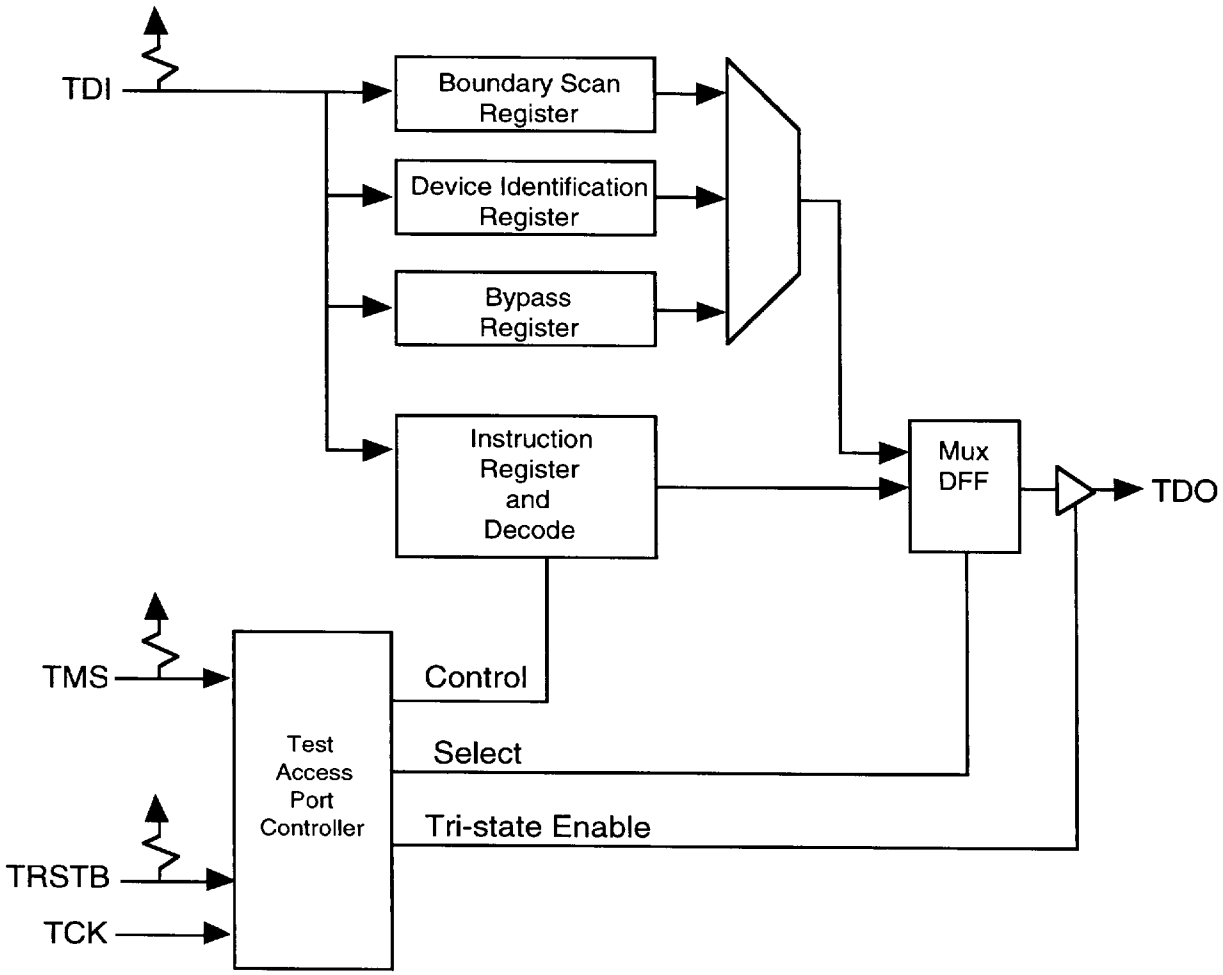
JTAG Support

The RCMP-800 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Fig. 8 Boundary Scan Architecture



The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a

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boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single bit delay from primary input, TDI to primary output , TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register placed in series with device inputs and outputs. Using the boundary scan register, all digital inputs, except SD[39:0] and SP[4:0], can be sampled and shifted out on primary output TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs, except SA[19:0], SOEB, SRWB, SADSB, SD[39:0] and SP[4:0].

TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

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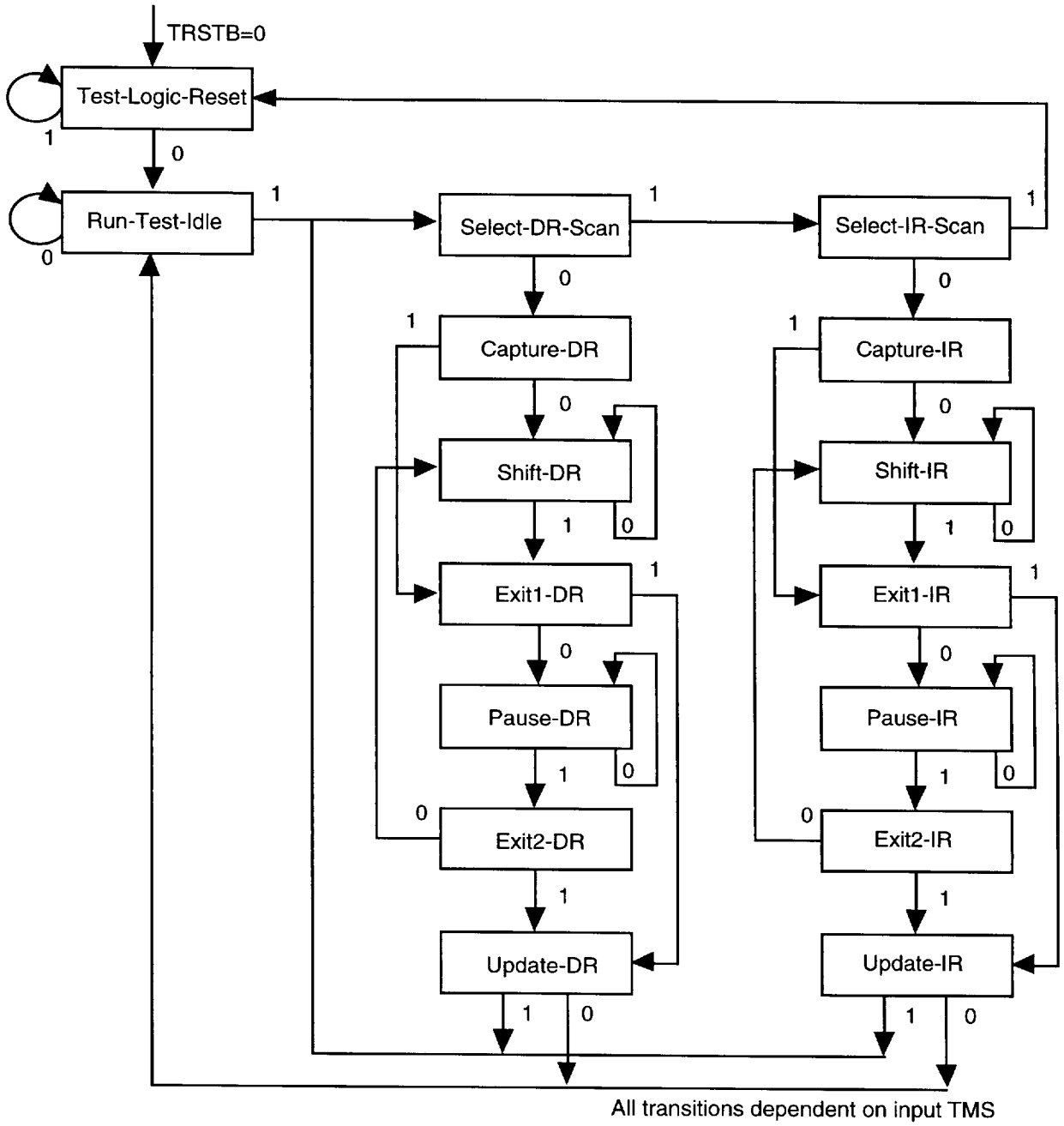
Fig. 9 TAP Controller Finite State Machine



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Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

The TDO output is enabled during states Shift-DR and Shift-IR. Otherwise, it is tri-stated.

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Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

INTEST

The internal test instruction is not fully implemented. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, primary outputs are sampled and loaded into the boundary scan register.

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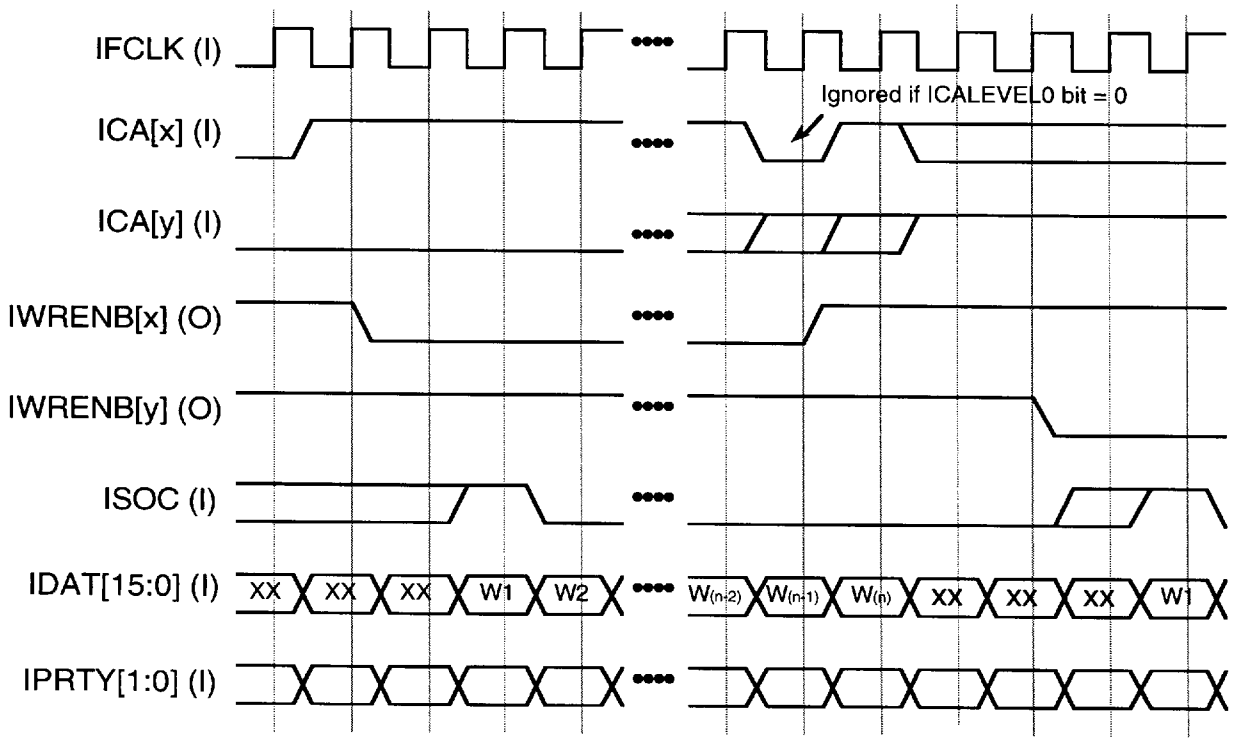
FUNCTIONAL TIMING

Input Cell Interface

Fig. 10 Input Cell Master Interface (IPOLL=0)



The Input Cell Master Interface (IPOLL=0) diagram (Fig. 10) illustrates the operation of the interface when it arbitrates accesses for a single or multiple PHYs. If operating with a single PHY interface, only the ICA[1] and IWRENB[1] control signals are active. When there is room for another cell in the RCMP-800 buffers and one of the ICA[4:1] inputs indicates that there is a cell available, the RCMP-800 will respond by asserting the associated IWRENB[4:1] output. The RCMP-800 only supports cell level handshaking; IWRENB[x] remains asserted until the entire cell is written into the FIFO. Once a transfer has been initiated, all bytes are assumed to be valid and ICA[x] is ignored until the end of the cell if the ICALEVEL0 bit of the Input Cell FIFO Configuration register (0x08) is a logic 0. If ICALEVEL0 is a logic 1, an early deassertion of ICA[x] is considered a break in the protocol and the cell is discarded.

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There is a minimum of three clock cycles between one IWRENB[x] being deasserted at the end of a cell and another IWRENB[y] being asserted at the start of the next cell.

ISOC is expected to be high during the first word of the data structure. The length of the data structure and the position of the ATM cell within the data structure is set by the CELLLEN[3:0] and CELLPOST[3:0] bits of the Input Cell FIFO Configuration register. It is not necessary for ISOC to be present each cell; the input cell write address is generated by an internal counter that flywheels in the absence of ISOC. If ISOC is sampled high during any byte other than the first byte of the data structure, an interrupt may be generated and the input cell write address counter is reset to the first byte of the data structure.

Fig. 11 Input Cell Interface Address Line Polling Master Configuration (IPOLL=1) – Example 1

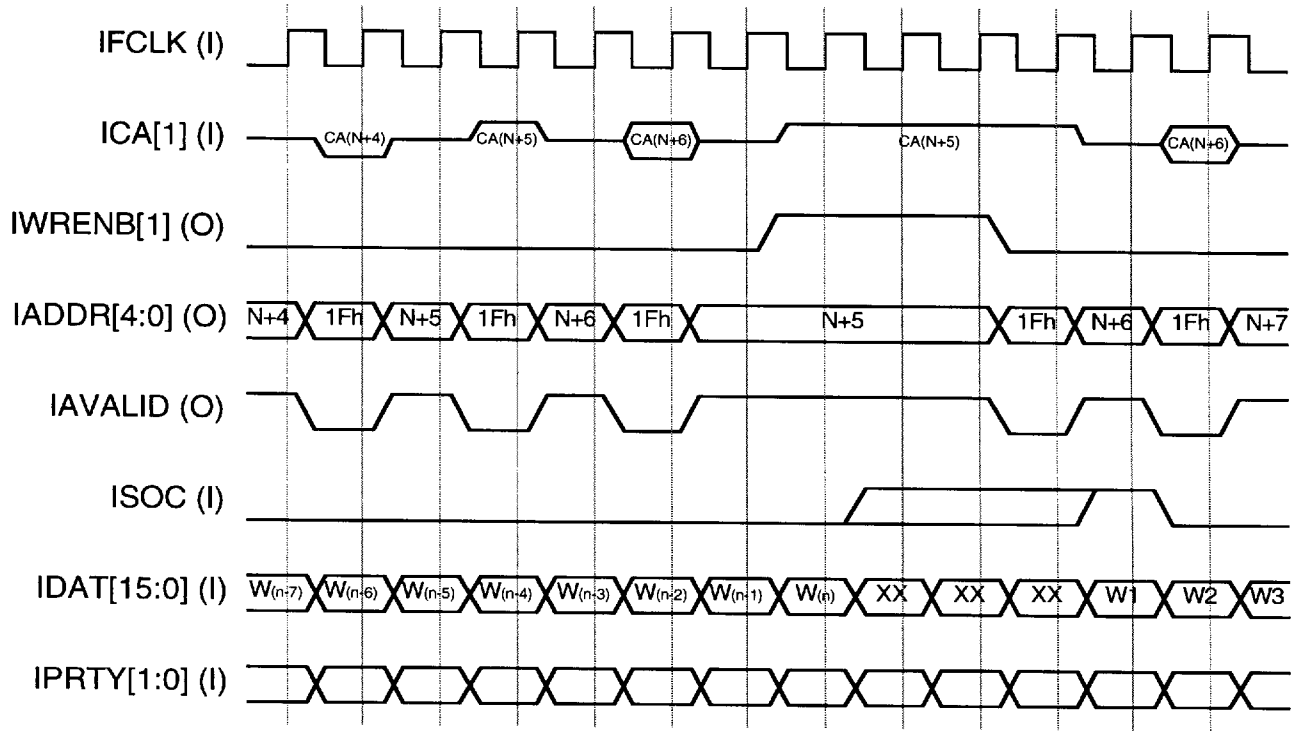

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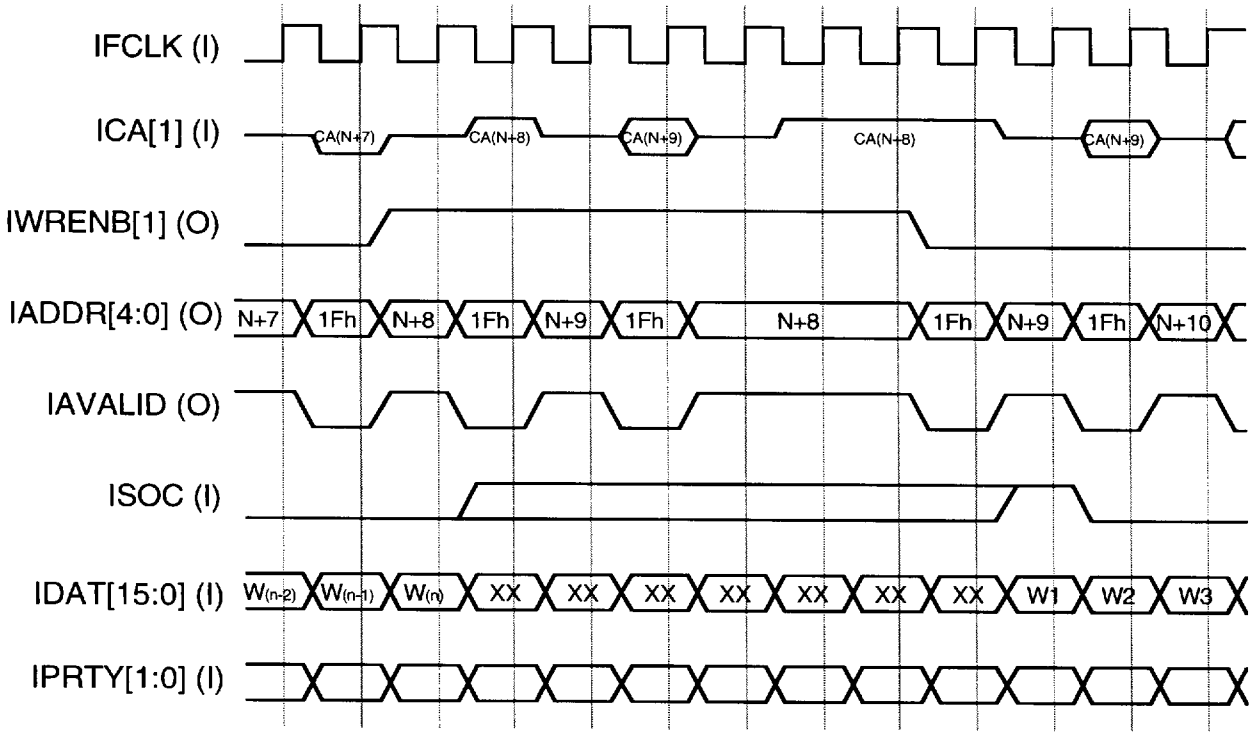
Fig. 12 Input Cell Interface Address Line Polling Master Configuration (IPOLL=1) – Example 2



Figures 11 and 12 illustrate the operation of the Input Cell Interface when it arbitrates accesses for up to 32 PHYs using address line polling. The ICA[1] and IWRENB[1] control signals are active.

The PHY devices are polled cyclically beginning with PHY#(N+1) where N is the PHY ID of the cell currently being transferred. The first PHY device to respond to polling with an available cell indication is selected for transfer of the next cell. If no PHY device responds with an available cell indication, the polling cycle repeats. If the polling cycle repeats while the current cell is being transferred, however, the PHY ID of the cell being transferred (i.e. N) is omitted from the polling sequence. This is because PHY devices compliant with the UTOPIA Level 1 interface (which can be used in polling mode with external glue logic) cannot indicate availability of a subsequent cell while they are simultaneously transferring a cell. Once transfer of the current cell is complete, PHY#N is re-inserted into the polling sequence.

When a PHY device with an available cell is found, polling ceases and the PHY device is selected for transfer of the next cell. (If the PHY is found while a cell is being transferred, its ID is output on IADDR[4:0] and held until the start of the next cell transfer.) The PHY device recognises that it has been selected to send the next cell to the RCMP-800 by the presence of its ID on IADDR[4:0] during the clock cycle

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prior to IWRENB[1] being asserted low. After IWRENB[1] is asserted low (i.e. at the start of the next cell transfer), the polling process starts again.

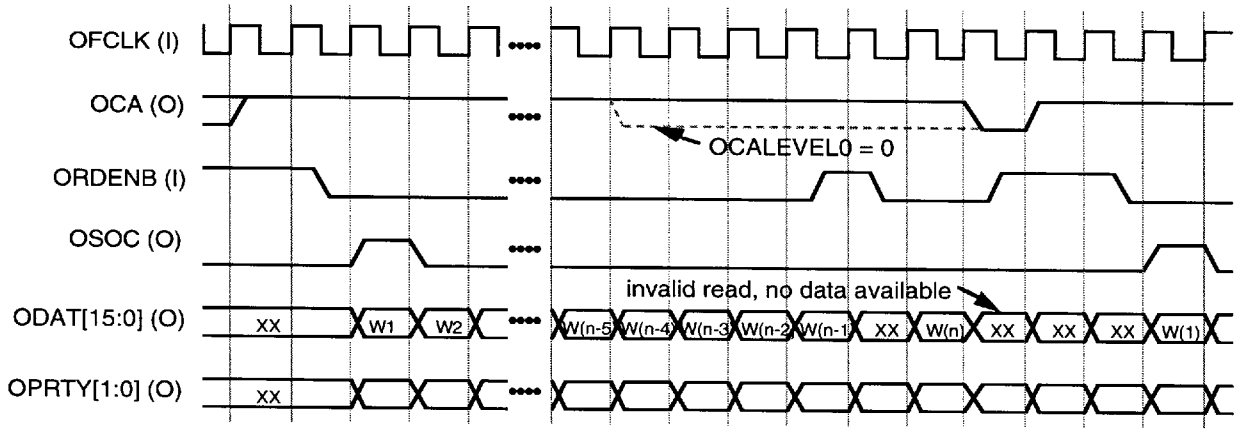
Figure 11 shows an example in which the first PHY to be found with a cell available is PHY#(N+5) and the successful poll occurs during a cell transfer. The value N+5 is therefore output on IADDR[4:0] and held until the start of the next cell transfer. Note that because of the pipelined nature of the polling process, PHY#(N+6) is unavoidably polled before PHY#(N+5) is selected. The polling reply from PHY#(N+6) is ignored. If, for any reason, PHY#(N+5) and deasserts ICA[1] before the start of the next cell transfer, the polling process starts over.

Figure 12 shows a second example in which the first PHY to be found with a cell available is PHY#(N+8) and the successful poll occurs after the previous cell transfer has completed. In this case, the value N+8 is output on IADDR[4:0] for three clock cycles after which IWRENB[1] is asserted to initiate transfer of the next cell. (Three clock cycles is the minimum required to re-sample ICA[1] and confirm that the cell is still available, i.e. that the PHY has not changed its mind.) Again, because of the pipelined nature of the polling process, PHY#(N+9) is unavoidably polled before PHY#(N+8) is selected.

ISOC is expected to be high during the first word of the data structure. The length of the data structure and the position of the ATM cell within the data structure is set by the CELLLEN[3:0] and CELLPOST[3:0] bits of the Input Cell FIFO Configuration register. It is not necessary for ISOC to be present each cell; the input cell write address is generated by an internal counter that flywheels in the absence of ISOC. If ISOC is sampled high during any byte other than the first byte of the data structure, an interrupt may be generated and the input cell write address counter is reset to the first byte of the data structure.

Output Cell Interface

Fig. 13 Output Cell Interface Single-PHY Slave (OTSEN=0)



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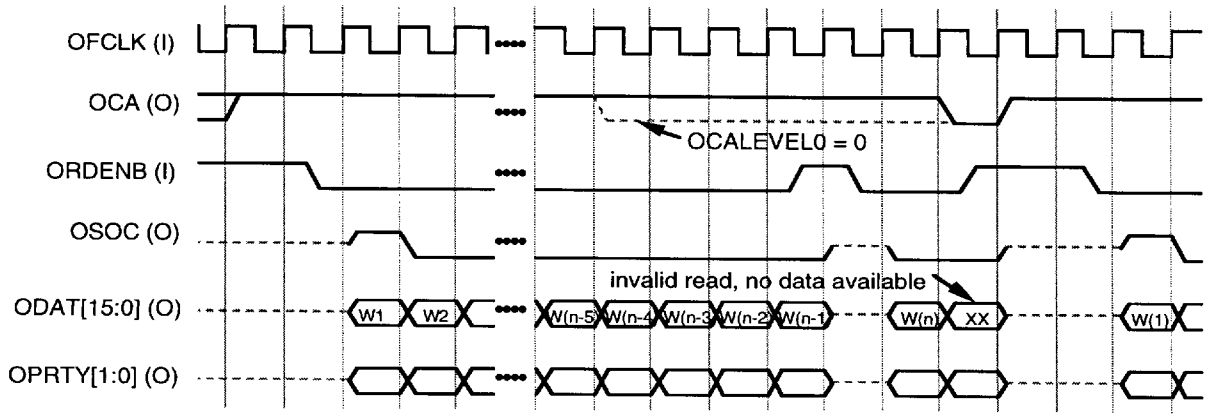
The Output Synchronous FIFO Timing Single-PHY Slave (OTSEN=0) diagram (Fig. 13) illustrates the operation of the Output Cell Interface as a bus slave with tristating disabled. The diagram illustrates the case where the OCAINV bit is a logic 0; the sense of the OCA output may be inverted by setting OCAINV to a logic 1.

The RCMP-800 indicates a cell is available by asserting the output cell available output, OCA. OCA remains high until the FIFO is near empty (four words remaining), empty or an error condition is detected. Selection of empty and near empty is made using the OCALEVEL0 bit in the Output FIFO Configuration register. For the near empty option, OCA transitions low four words before the last word of the last cell is read from the FIFO. OCA remains low for a minimum of one OFCLK clock cycle and then can transition high to indicate that there are additional cells available.

Fig. 14 Output Cell Interface Single-PHY Slave (OTSEN=1)



The Output Cell Interface Single-PHY Slave (OTSEN=1) diagram (Fig. 14) illustrates the operation of the Output Cell Interface with tristating enabled.

The functional behaviour is the same as when tristating is disabled except that OSOC, ODAT[15:0] and OPRTY[1:0] are tristated the cycle after ORDENB is deasserted.

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ABSOLUTE MAXIMUM RATINGS

Case Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to V_{DD}+0.5V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+300°C
Absolute Maximum Junction Temperature	+150°C
Power Dissipation	4 W

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D.C. CHARACTERISTICS

(T_C = -40°C to +85°C, V_{DD} = 5 V ±5%)
(Typical Conditions: T_C = 25°C, V_{DD} = 5 V)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IL}	Input Low Voltage (TTL Only)	-0.5		0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage (TTL Only)	2.0		V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage
V_{OL}	Output or Bi-directional Low Voltage (TTL Only)			0.4	Volts	V_{DD} = min, I_{OL} = -2 mA, Note 3
V_{OH}	Output or Bi-directional High Voltage (TTL Only)	VDD -0.5V			Volts	V_{DD} = min, I_{OH} = 2 mA, Note 3
V_{T+}	Reset Input High Voltage	3.5			Volts	
V_{T-}	Reset Input Low Voltage			0.6	Volts	
V_{TH}	Reset Input Hysteresis Voltage		1		Volts	
I_{ILPU}	Input Low Current (Pull ups)	+175	+350	+525	µA	V_{IL} = GND, Notes 1, 3
I_{IHPU}	Input High Current (Pull ups)	-10		+10	µA	V_{IH} = V_{DD}, Notes 1, 3
I_{IL}	Input Low Current	-10		+10	µA	V_{IL} = GND, Notes 2, 3
I_{IH}	Input High Current	-10		+10	µA	V_{IH} = V_{DD}, Notes 2, 3
C_{IN}	Input Capacitance		5		pF	
C_{OUT}	Output Capacitance		5		pF	

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C_{IO}	Bidirectional Capacitance		5		pF	
I_{DDOP}	Operating Current Processing Cells			550	mA	V_{DD} = 5.25 V, Outputs Unloaded, SYSCLK =50 MHz, IFCLK = 50 MHz, OFCLK = 50 MHz,
I_{DDSB}	Standby Current		1		mA	V_{DD} = 5.25 V, Outputs Unloaded, No Clocks

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistor.
2. Input pin or bidirectional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

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MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_C = -40°C to +85°C, V_{DD} = 5 V ±5%)

Microprocessor Interface Read Access (Fig. 15)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_L	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		50	ns
tZ_{RD}	Valid Read Negated to Output Tristate		20	ns
tP_{DREQ}	Valid Read Asserted to DREQ Deasserted		50	ns
tZ_{INTH}	Valid Read Negated to INTB Tristate		50	ns

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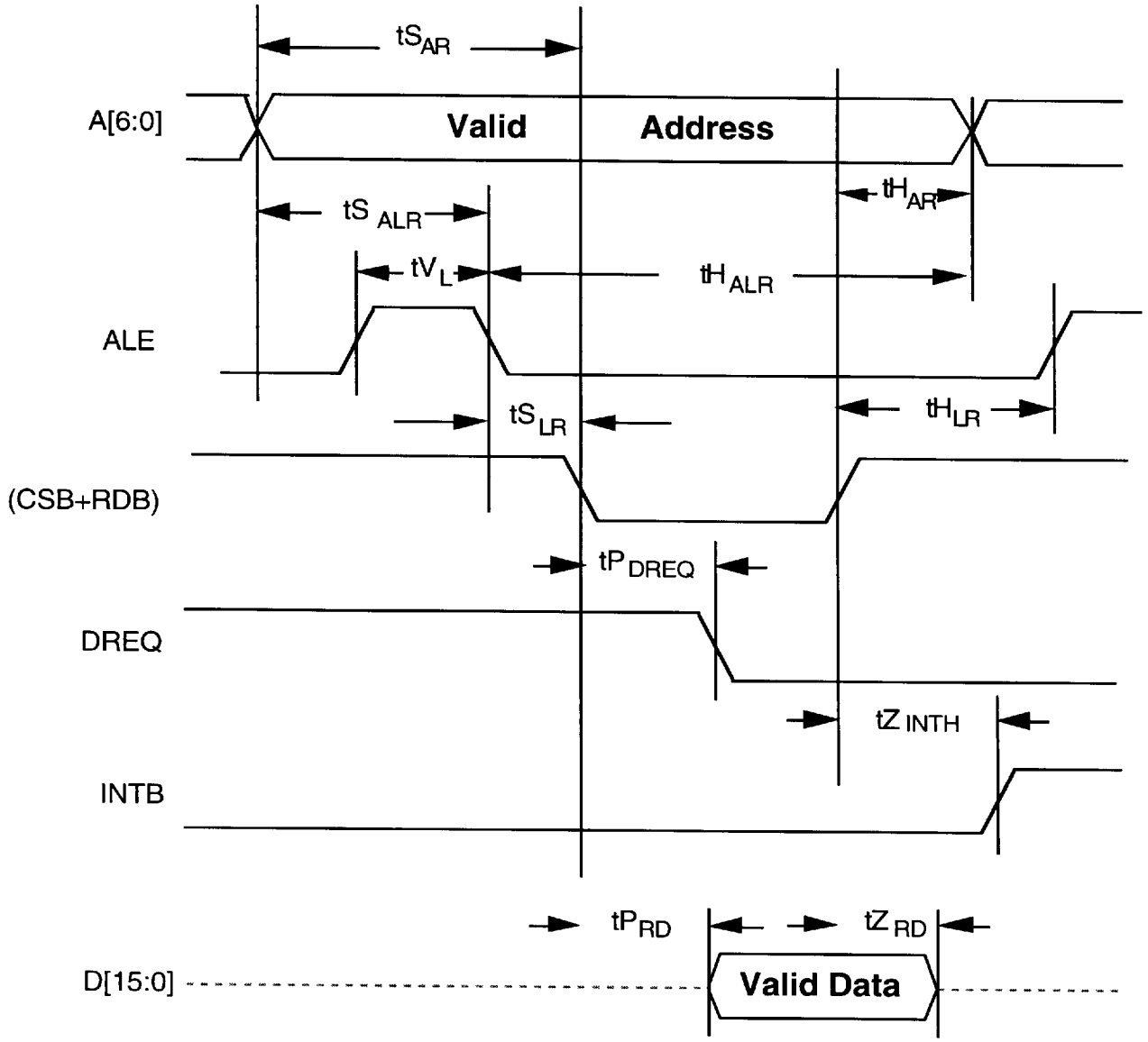
Fig. 15 Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]).

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3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. Microprocessor Interface timing applies to normal mode register accesses only.
5. In non-multiplexed address/data bus architecture's, ALE should be held high, parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR} are not applicable.
6. Parameter tH_{AR} is not applicable if address latching is used.
7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
9. Output tristate delay is the time in nanoseconds from the 1.4 Volt point of the reference signal to ±300mV of the termination voltage on the output. The test load is 50Ω to 1.4V in parallel with 10 pf to GND.

Microprocessor Interface Write Access (Fig. 16)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_L	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

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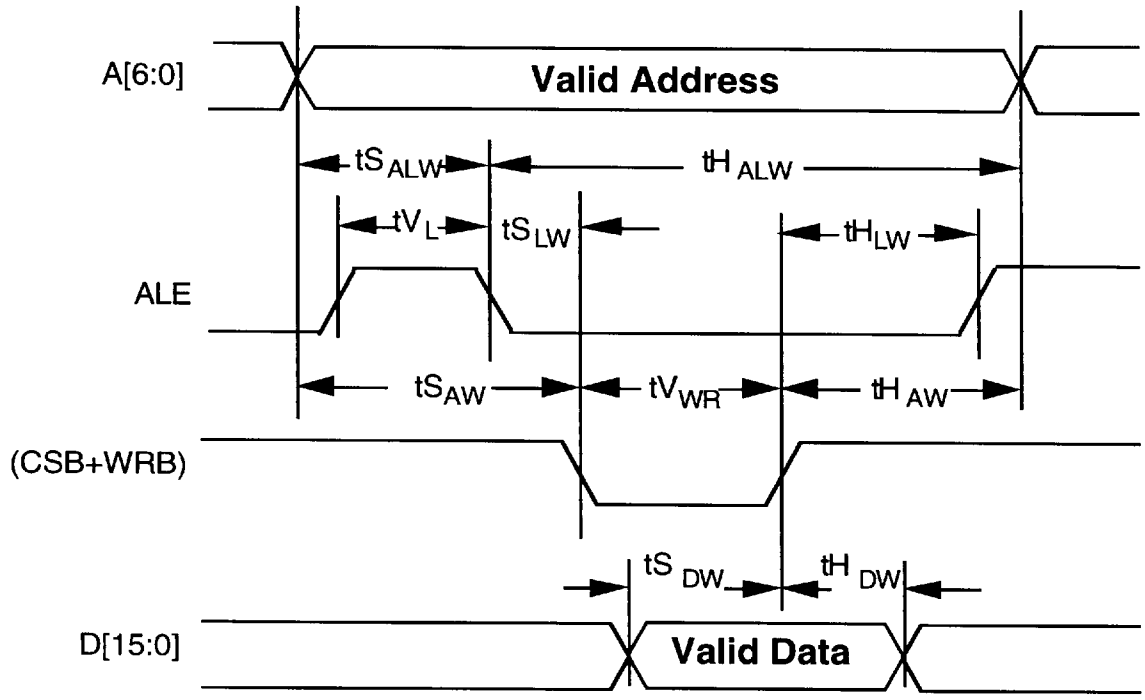
Fig. 16 Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1 A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. Microprocessor Interface timing applies to normal mode register accesses only.

3. In non-multiplexed address/data bus architecture's, ALE should be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW} are not applicable.

4. Parameter tH_{AW} is not applicable if address latching is used.

5. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

6. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

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RCMP-800 TIMING CHARACTERISTICS

(T_C = -40°C to +85°C, V_{DD} = 5 V ±5%)

Input Cell Interface (Fig. 17 and 18)

Symbol	Description	Min	Max	Units
	IFCLK Frequency		52	MHz
	IFCLK Duty Cycle	40	60	%
$^tS_{IDAT}$	IDAT[15:0] Set-up time to IFCLK	4		ns
$^tH_{IDAT}$	IDAT[15:0] Hold time to IFCLK	1		ns
$^tS_{IPRTY}$	IPRTY[1:0] Set-up time to IFCLK	4		ns
$^tH_{IPRTY}$	IPRTY[1:0] Hold time to IFCLK	1		ns
$^tS_{ISOC}$	ISOC Set-up time to IFCLK	4		ns
$^tH_{ISOC}$	ISOC Hold time to IFCLK	1		ns
$^tS_{ICA}$	ICA[4:1] Set-up time to IFCLK	4		ns
$^tH_{ICA}$	ICA[4:1] Hold time to IFCLK	1		ns
$^tP_{IWRENB}$	IFCLK High to IWRENB[4:1] Valid	1	15	ns
$^tP_{IADDR}$	IFCLK High to IADDR[4:0] Valid	1	15	ns
$^tP_{IAVALID}$	IFCLK High to IAVALID Valid	1	15	ns

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Fig. 17 Input Cell Interface Master (IPOLL=0) Timing

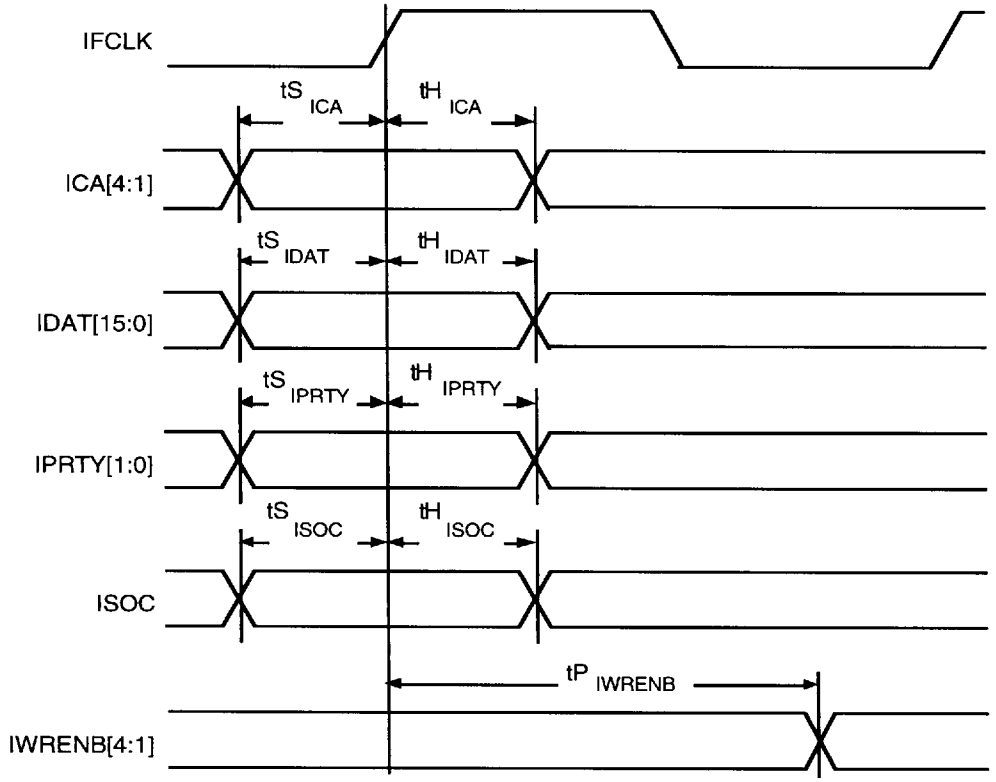

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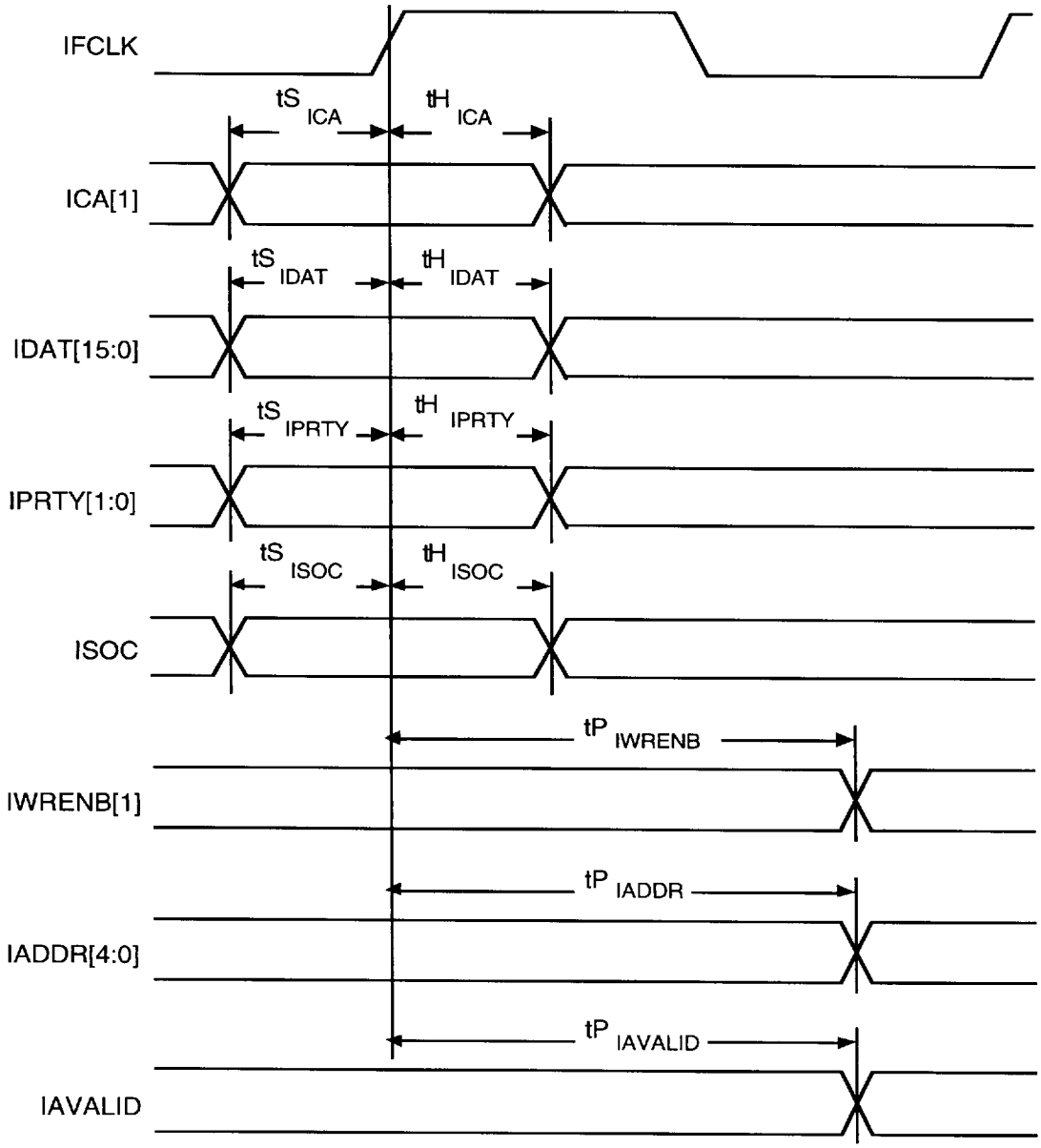
Fig. 18 Input Cell Interface Master (IPOLL=1) Timing



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Output Cell Interface (Fig. 19)

Symbol	Description	Min	Max	Units
	OFCLK Frequency		52	MHz
	OFCLK Duty Cycle	40	60	%
tS_{ORDENB}	ORDENB Set-up time to OFCLK	4		ns
tH_{ORDENB}	ORDENB Hold time to OFCLK	1		ns
tP_{OSOC}	OFCLK High to OSOC Valid	1	15	ns
tP_{ODAT}	OFCLK High to ODAT[15:0] Valid	1	15	ns
tP_{OPRTY}	OFCLK High to OPRTY[1:0] Valid	1	15	ns
tP_{OFCLK}	OFCLK High to Output Enable	1	15	ns
tZ_{OFCLK}	OFCLK High to Output Tristate	1	15	ns
tP_{OCA}	OFCLK High to OCA Valid	1	15	ns

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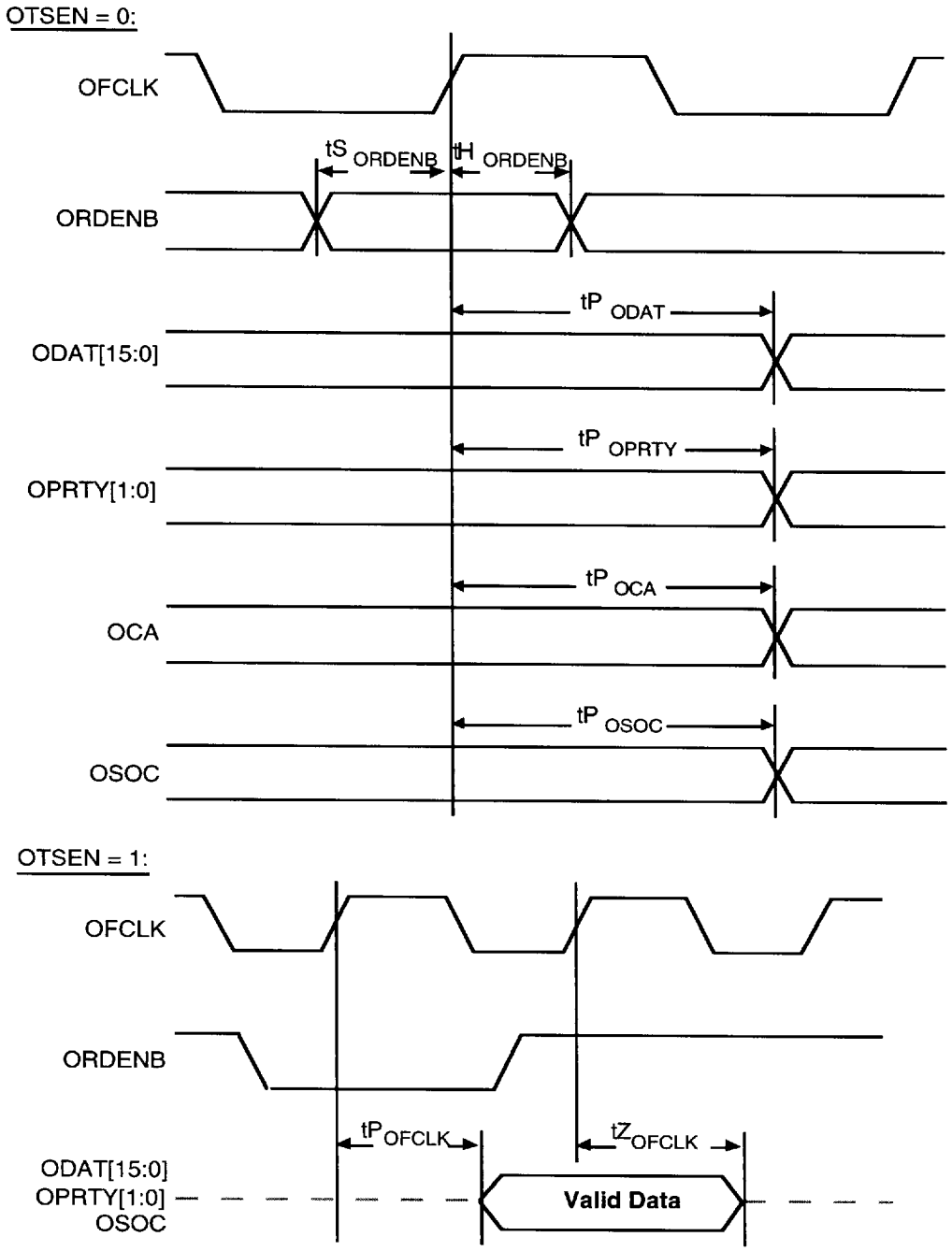
Fig. 19 Output Cell Interface Slave Timing



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Synchronous SRAM Interface (Fig. 20)

Symbol	Description	Min	Max	Units
t_{CYC}	SYSCLK Period	20	†	ns
	SYSCLK Duty Cycle	40	60	%
tS_{SD}	SD[39:0] and SP[4:0] Set-up time to SYSCLK	4		ns
tH_{SD}	SD[39:0] and SP[4:0] Hold time to SYSCLK	1		ns
tP_{SD}	SYSCLK High to SD[39:0] and SP[4:0] Valid	2	15	ns
tZ_{SD}	SYSCLK High to SD[39:0] and SP[4:0] Tri-state	1	15	ns
tP_{SA}	SYSCLK High to SA[19:0] Valid, C_L = 50pf	2	15	ns
	C_L = 20pf	1	12	
tP_{SADSB}	SYSCLK High to SADSB Valid, C_L = 50pf	2	15	ns
	C_L = 20pf	1	12	
tP_{SOEB}	SYSCLK High to SOEB Valid, C_L = 50pf	2	15	ns
	C_L = 20pf	1	12	
tP_{SRWB}	SYSCLK High to SRWB Valid, C_L = 50pf	2	15	ns
	C_L = 20pf	1	12	

† The SYSCLK period must be less than 16 times the maximum of the IFCLK and OFCLK periods for correct operation of the internal FIFOs, but it will usually be constrained by the cell throughput required. To guarantee a sustained throughput of N cell/s:

$$t_{CYC} < \frac{1}{N(\text{Max. Search Tree Depth} + 17)}$$

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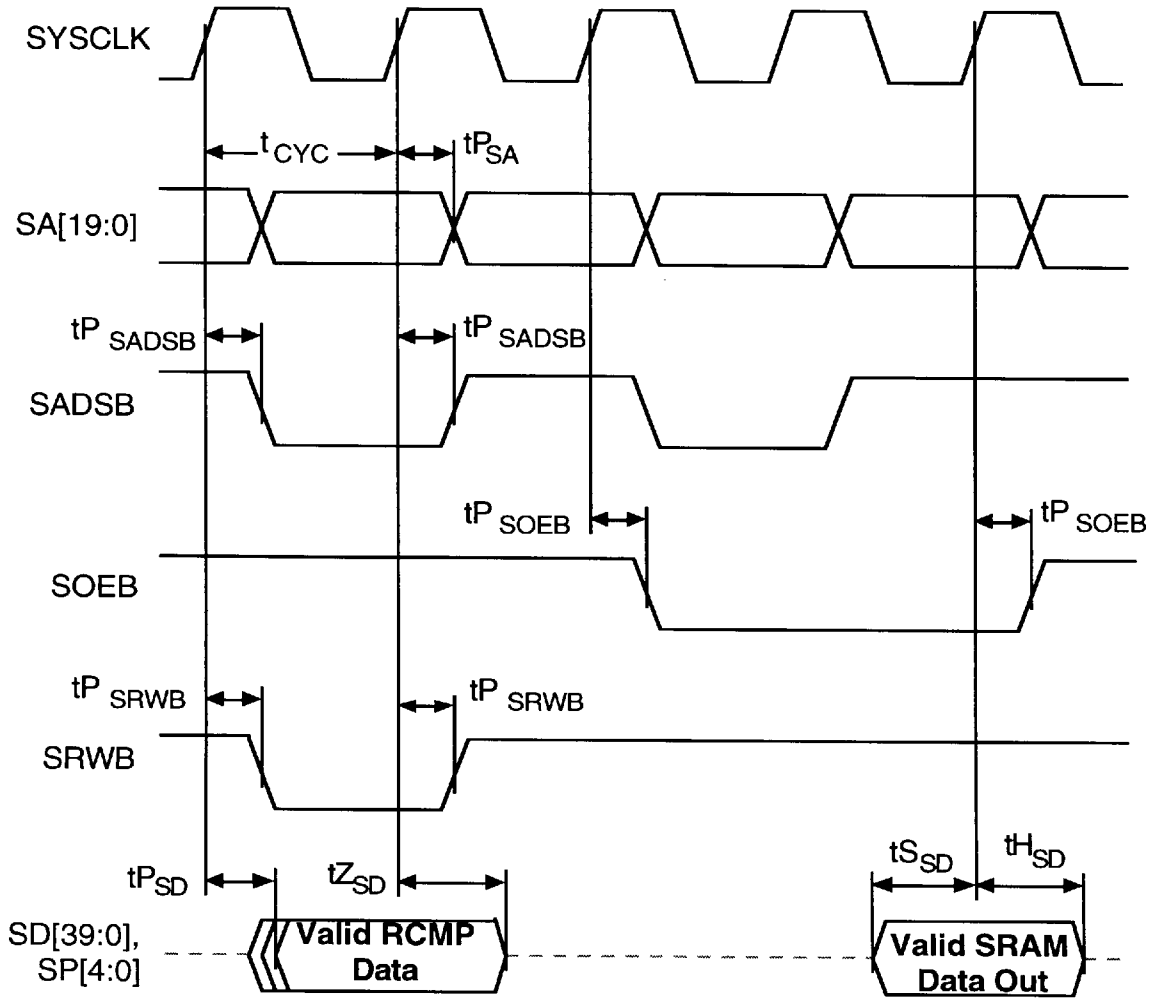
Fig. 20 Synchronous SRAM Interface Timing



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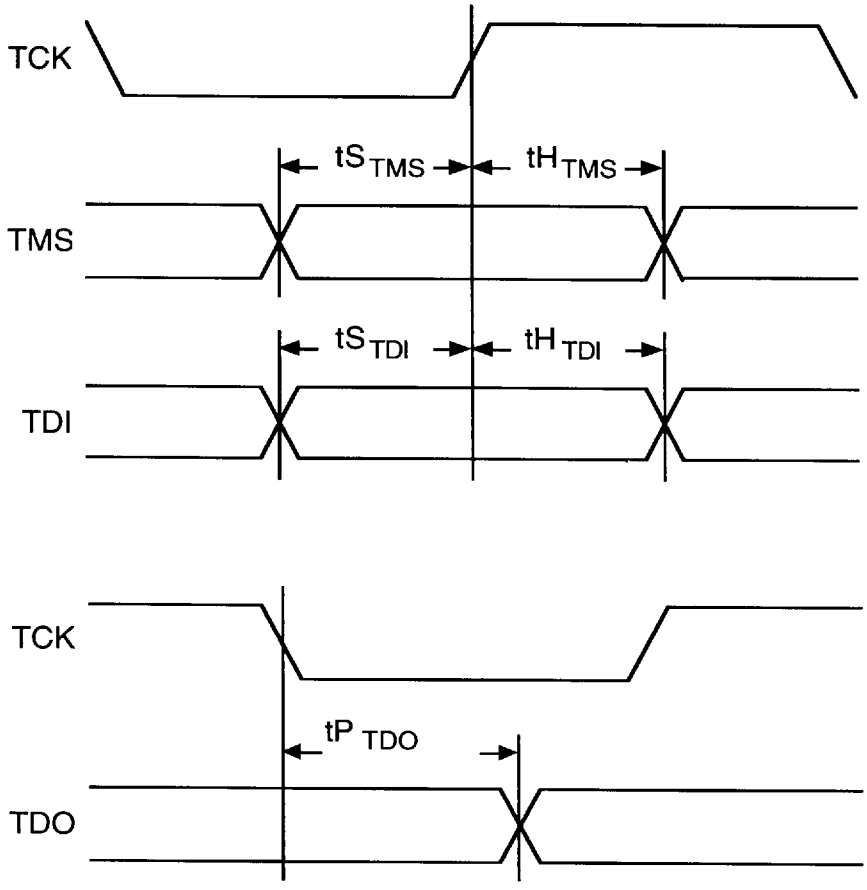
JTAG Port Interface (Fig. 21)

Symbol	Description	Min	Max	Units
	TCK Frequency	0	10	MHz
	TCK Duty Cycle	40	60	%
tS_{TMS}	TMS Set-up time to TCK	10		ns
tH_{TMS}	TMS Hold time to TCK	10		ns
tS_{TDI}	TDI Set-up time to TCK	10		ns
tH_{TDI}	TDI Hold time to TCK	10		ns
tP_{TDO}	TCK Low to TDO Valid	0	20	ns

Fig. 21 JTAG Port Interface Timing



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Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum and minimum output propagation delays are specified with a 50 pF load on the outputs, unless otherwise noted.

3. Output tristate delay is the time in nanoseconds from the 1.4 Volt point of the reference signal to ±300mV of the termination voltage on the output. The test load is 50Ω to 1.4V in parallel with 10 pf to GND.

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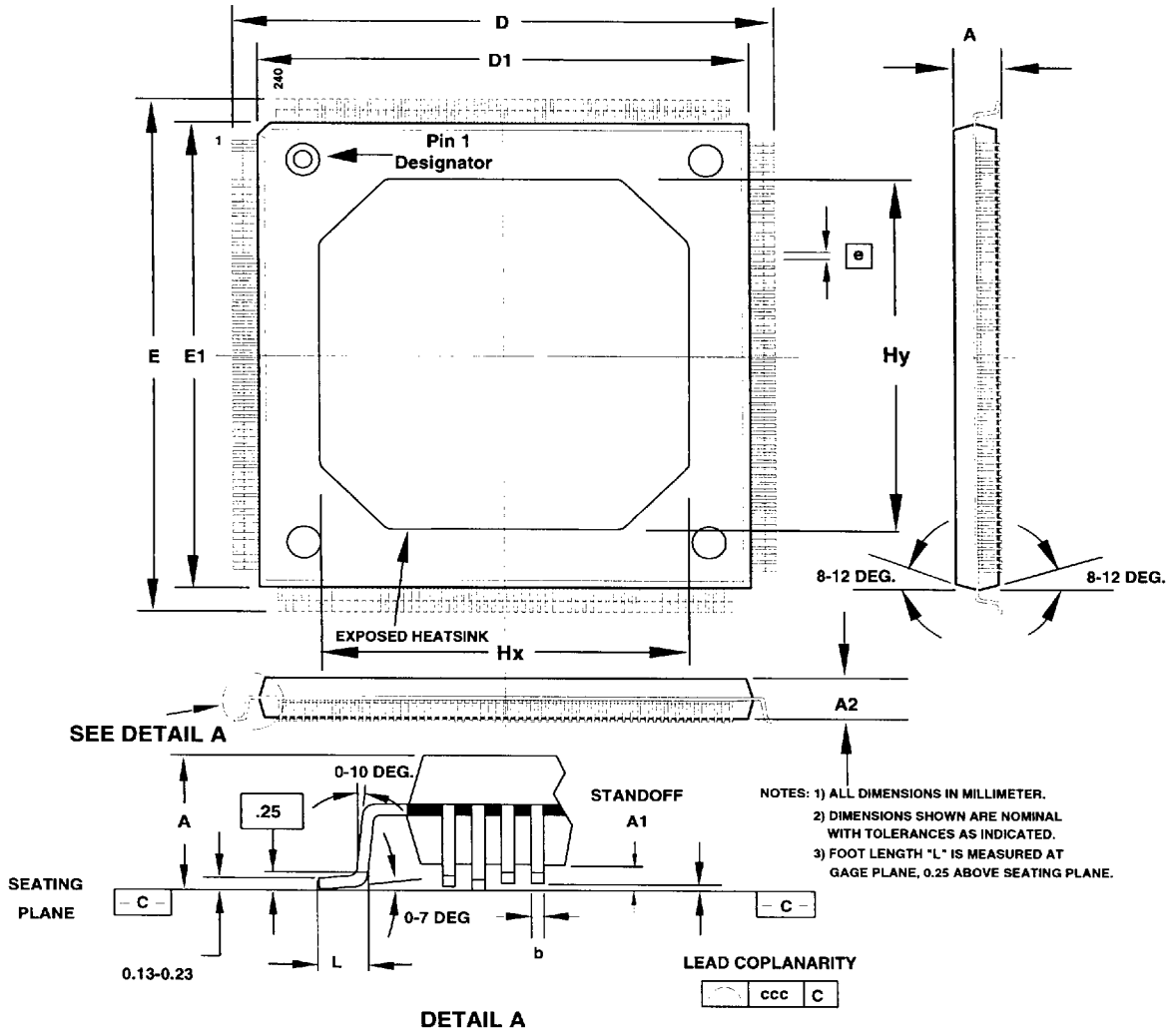
MECHANICAL INFORMATION

240 Pin Slugged Plastic Quad Flat Pack (S Suffix):



DETAIL A

PACKAGE TYPE: 240 PIN SLUGGED METRIC PLASTIC QUAD FLATPACK-SMQFP													
BODY SIZE: 32 x 32 x 3.40 MM													
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc	Hx	Hy
Min.	3.15	0.25	2.90	34.35	31.90	34.35	31.90	0.45		0.17			
Nom.				34.60	32.00	34.60	32.00	0.60	0.50	0.22		24.20	24.20
Max.	4.10	0.50	3.60	34.85	32.10	34.85	32.10	0.75		0.27	0.10		

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