MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC54/74HC4514

1-of-16 Decoder/Demultiplexer With Address Latch

High-Performance Silicon-Gate CMOS

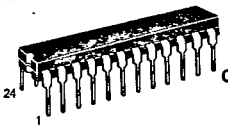
The MC54/74HC4514 is identical in pinout to the MC14514B metal-gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of a 4-bit storage latch with a Latch Enable and Chip Select input. When a low signal is applied to the Latch Enable input, the Address is stored, and decoded. When the Chip Select input is high, all sixteen outputs are forced to a low level.

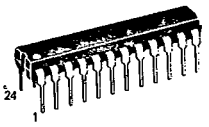
The Chip Select input is provided to facilitate the chip-select, demultiplexing, and cascading functions.

The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using the Chip Select as a data input.

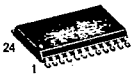
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 268 FETs or 67 Equivalent Gates



J SUFFIX
CERAMIC
CASE 758-01



N SUFFIX
PLASTIC
CASE 724-03



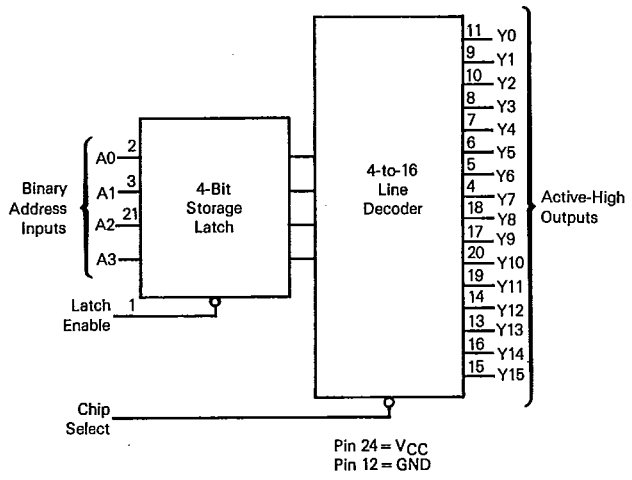
DW SUFFIX
SOIC
CASE 751E-02

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXDW	SOIC

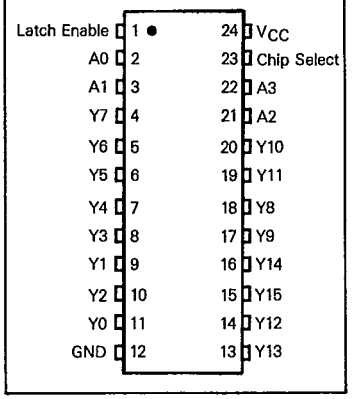
T_A = −55° to 125°C for all packages.
Dimensions in Chapter 7.

BLOCK DIAGRAM



Pin 24 = V_{CC}
Pin 12 = GND

PIN ASSIGNMENT



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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package)	260	
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC}=2.0 V	0	1000	ns
	(Figure 1)	V_{CC}=4.5 V	0	500	
		V_{CC}=6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to −55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V; $\|I_{out}\|$ ≤20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V; $\|I_{out}\|$ ≤20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL}; $\|I_{out}\|$ ≤20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V_{in}=V_{IH} or V_{IL}; $\|I_{out}\|$ ≤4.0 mA	4.5	3.98	3.84	3.70	
		$\|I_{out}\|$ ≤5.2 mA	6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL}; $\|I_{out}\|$ ≤20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V_{in}=V_{IH} or V_{IL}; $\|I_{out}\|$ ≤4.0 mA	4.5	0.26	0.33	0.40	
		$\|I_{out}\|$ ≤5.2 mA	6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in}=V_{CC} or GND; I_{out}=0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Chip Select to Output Y (Figures 1 and 5)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t_{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 5)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t_{PHL}		2.0	175	220	265	
		4.5	35	44	53	
		6.0	30	37	45	
t_{PLH}	Maximum Propagation Delay, Latch Enable to Output Y (Figures 3 and 5)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t_{PHL}		2.0	175	220	265	
		4.5	35	44	53	
		6.0	30	37	45	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V_{CC} = 5.0 V 70	pF

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Input A to Latch Enable (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t_h	Minimum Hold Time, Latch Enable to Input A (Figure 4)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t_w	Minimum Pulse Width, Latch Enable (Figure 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

SWITCHING WAVEFORMS

FIGURE 1

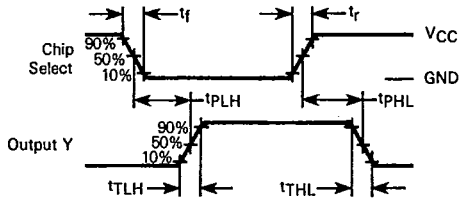


FIGURE 2

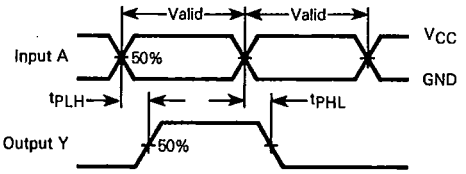


FIGURE 3

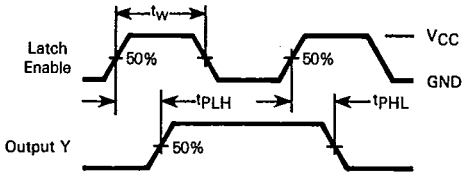


FIGURE 4

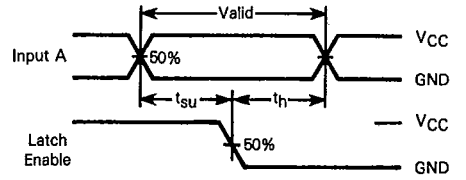
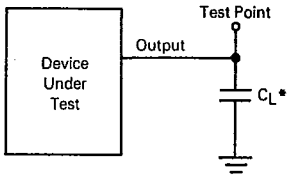


FIGURE 5 — TEST CIRCUIT



* Includes all probe and jig capacitance.

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FUNCTION TABLE

Latch Enable	Chip Select	Address Inputs A3	A2	A1	A0	Selected Output (High)
H	L	L	L	L	L	Y0
H	L	L	L	L	H	Y1
H	L	L	L	H	L	Y2
H	L	L	L	H	H	Y3
H	L	L	H	L	L	Y4
H	L	L	H	L	H	Y5
H	L	L	H	H	L	Y6
H	L	L	H	H	H	Y7
H	L	H	L	L	L	Y8
H	L	H	L	L	H	Y9
H	L	H	L	H	L	Y10
H	L	H	L	H	H	Y11
H	L	H	H	L	L	Y12
H	L	H	H	L	H	Y13
H	L	H	H	H	L	Y14
H	L	H	H	H	H	Y15
X	H	X	X	X	X	All Outputs = L
L	L	X	X	X	X	Latched Data

PIN DESCRIPTIONS

ADDRESS INPUTS

A0, A1, A2, A3 (PINS 2, 3, 21, 22) — Address Inputs. These inputs are decoded to produce a high level on one of 16 outputs. The inputs are arranged such that A3 is the most-significant bit and A0 is the least-significant bit. The decimal equivalent of the binary input address indicates which of the 16 data outputs, Y0-Y15, is selected.

OUTPUTS

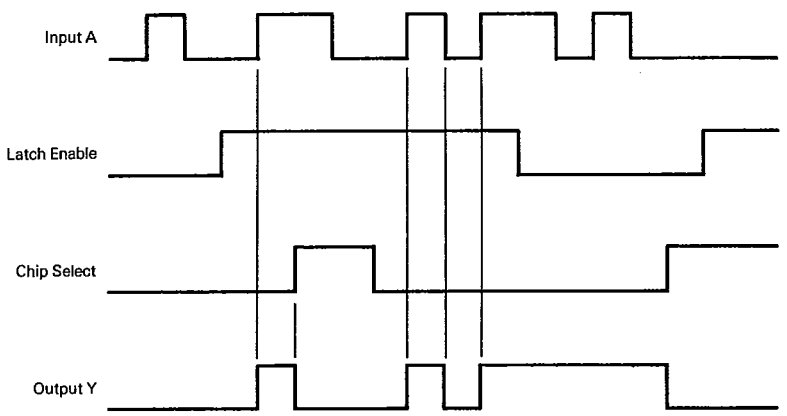
Y0-Y15 (PINS 11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15) — Active-High Outputs. These outputs produce a high level when selected (Latch Enable = H, Chip Select = L) and are at a low level when not selected.

CONTROL INPUTS

LATCH ENABLE (PIN 1) — Latch Enable Input. A low level on this input stores the data on the Address data inputs in the 4-bit latch. A high level on the Latch Enable input makes the latch transparent and allows the outputs to follow the inputs. Note that the data is latched only while the Latch Enable input is at a low level.

CHIP SELECT (PIN 23) — Chip Select Input. A high on this input produces a low level on all outputs, regardless of what appears at the address or Latch Enable inputs. A low level on the Chip Select input allows the selected output to produce a high level.

TIMING DIAGRAM



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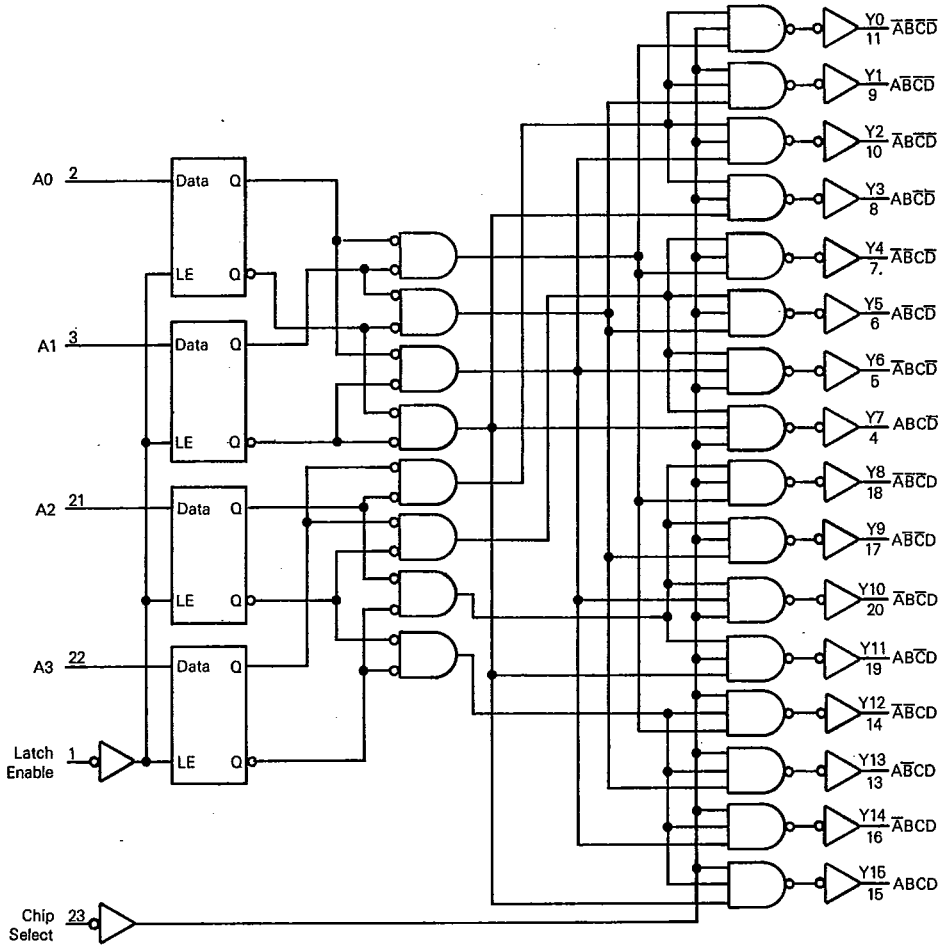
EXPANDED LOGIC DIAGRAM



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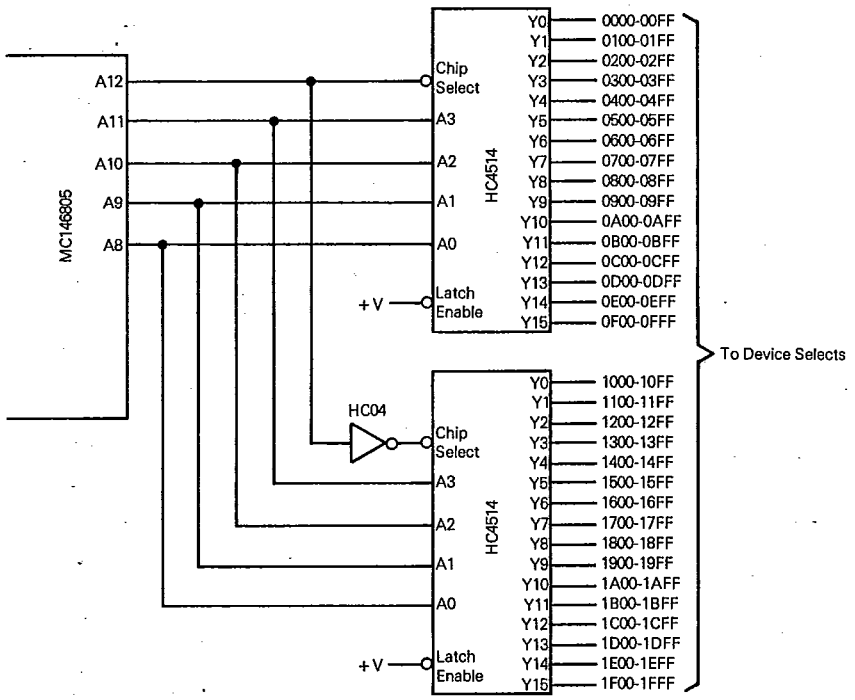
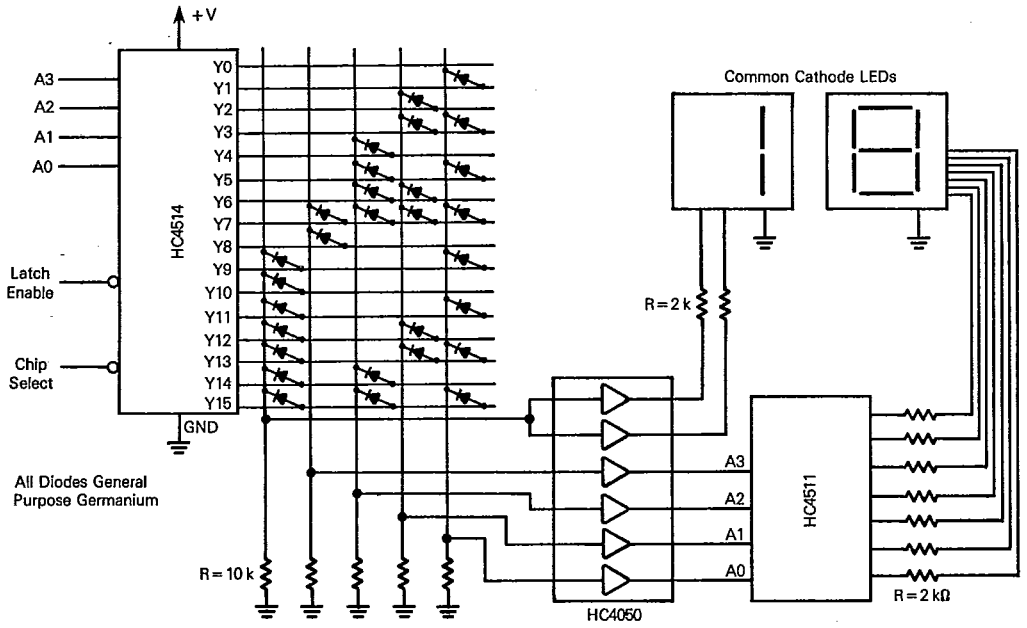
MICROPROCESSOR MEMORY DECODING



CODE TO CODE CONVERSION — HEXADECIMAL TO BCD



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