National Semiconductor

August 2000

# LM359
# Dual, High Speed, Programmable, Current Mode (Norton) Amplifiers

## General Description

The LM359 consists of two current differencing (Norton) input amplifiers. Design emphasis has been placed on obtaining high frequency performance and providing user programmable amplifier operating characteristics. Each amplifier is broadbanded to provide a high gain bandwidth product, fast slew rate and stable operation for an inverting closed loop gain of 10 or greater. Pins for additional external frequency compensation are provided. The amplifiers are designed to operate from a single supply and can accommodate input common-mode voltages greater than the supply.

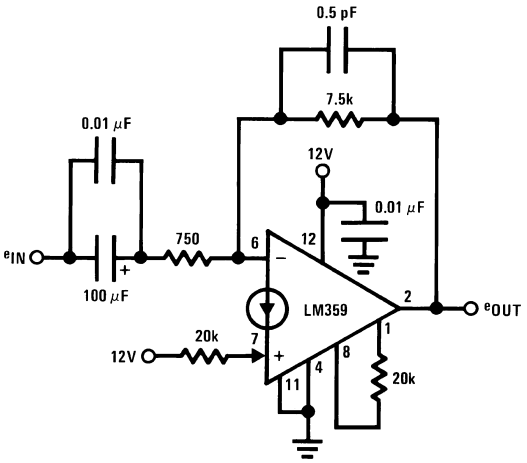
## Applications

- General purpose video amplifiers
- High frequency, high Q active filters
- Photo-diode amplifiers
- Wide frequency range waveform generation circuits
- All LM3900 AC applications work to much higher frequencies

## Features

- User programmable gain bandwidth product, slew rate, input bias current, output stage biasing current and total device power dissipation
- High gain bandwidth product ($I_{SET}$ = 0.5 mA)
  400 MHz for $A_V$ = 10 to 100
  30 MHz for $A_V$ = 1
- High slew rate ($I_{SET}$ = 0.5 mA)
  60 V/µs for $A_V$ = 10 to 100
  30 V/µs for $A_V$ = 1
- Current differencing inputs allow high common-mode input voltages
- Operates from a single 5V to 22V supply
- Large inverting amplifier output swing, 2 mV to $V_{CC}$ − 2V
- Low spot noise, $6\ nV/\sqrt{Hz}$, for f > 1 kHz

## Typical Application

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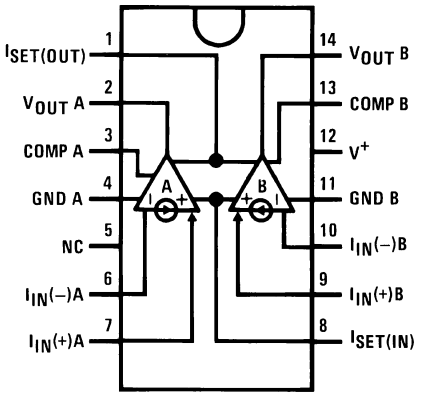
- $A_V$ = 20 dB
- −3 dB bandwidth = 2.5 Hz to 25 MHz
- Differential phase error < 1° at 3.58 MHz
- Differential gain error < 0.5% at 3.58 MHz

## Connection Diagram

**Dual-In-Line Package**

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**Top View**
**Order Number LM359M or LM359N**
**See NS Package Number M14A or N14A**

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

Supply Voltage 22 $V_{DC}$
or ±11 $V_{DC}$

Power Dissipation (Note 2)
- J Package 1W
- N Package 750 mW

Maximum $T_J$
- J Package +150˚C
- N Package +125˚C

Thermal Resistance

J Package

$\theta_{jA}$ 147˚C/W still air
110˚C/W with 400 linear feet/min air flow

N Package

$\theta_{jA}$ 100˚C/W still air
75˚C/W with 400 linear feet/min air flow

Input Currents, $I_{IN}(+)$ or $I_{IN}(-)$ 10 $mA_{DC}$

Set Currents, $I_{SET(IN)}$ or $I_{SET(OUT)}$ 2 $mA_{DC}$

Operating Temperature Range
- LM359 0˚C to +70˚C

Storage Temperature Range −65˚C to +150˚C

Lead Temperature
- (Soldering, 10 sec.) 260˚C

Soldering Information
- Dual-In-Line Package
  - Soldering (10 sec.) 260˚C
- Small Outline Package
  - Vapor Phase (60 sec.) 215˚C
  - Infrared (15 sec.) 220˚C

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

ESD rating to be determined.

## Electrical Characteristics

$I_{SET(IN)} = I_{SET(OUT)}$ = 0.5 mA, $V_{supply}$ = 12V, $T_A$ = 25˚C unless otherwise noted

| Parameter | Conditions | LM359 | | | Units |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Open Loop Voltage | $V_{supply}$ = 12V, $R_L$ = 1k, f = 100 Hz | 62 | 72 | | dB |
| Gain | $T_A$ = 125˚C | | 68 | | dB |
| Bandwidth | $R_{IN}$ = 1 kΩ, $C_{comp}$ = 10 pF | 15 | 30 | | MHz |
| Unity Gain | | | | | |
| Gain Bandwidth Product | $R_{IN}$ = 50Ω to 200Ω | 200 | 400 | | MHz |
| Gain of 10 to 100 | | | | | |
| Slew Rate | | | | | |
| Unity Gain | $R_{IN}$ = 1 kΩ, $C_{comp}$ = 10 pF | | 30 | | V/µs |
| Gain of 10 to 100 | $R_{IN}$ < 200Ω | | 60 | | V/µs |
| Amplifier to Amplifier Coupling | f = 100 Hz to 100 kHz, $R_L$ = 1k | | −80 | | dB |
| Mirror Gain | at 2 mA $I_{IN}(+)$, $I_{SET}$ = 5 µA, $T_A$ = 25˚C | 0.9 | 1.0 | 1.1 | µA/µA |
| (Note 3) | at 0.2 mA $I_{IN}(+)$, $I_{SET}$ = 5 µA | 0.9 | 1.0 | 1.1 | µA/µA |
| | Over Temp. | | | | |
| | at 20 µA $I_{IN}(+)$, $I_{SET}$ = 5 µA | 0.9 | 1.0 | 1.1 | µA/µA |
| | Over Temp. | | | | |
| ΔMirror Gain | at 20 µA to 0.2 mA $I_{IN}(+)$ | | 3 | 5 | % |
| (Note 3) | Over Temp, $I_{SET}$ = 5 µA | | | | |
| Input Bias Current | Inverting Input, $T_A$ = 25˚C | | 8 | 15 | µA |
| | Over Temp. | | | 30 | µA |
| Input Resistance (βre) | Inverting Input | | 2.5 | | kΩ |
| Output Resistance | $I_{OUT}$ = 15 mA rms, f = 1 MHz | | 3.5 | | Ω |
| Output Voltage Swing | $R_L$ = 600Ω | | | | |
| $V_{OUT}$ High | $I_{IN}(-)$ and $I_{IN}(+)$ Grounded | 9.5 | 10.3 | | V |
| $V_{OUT}$ Low | $I_{IN}(-)$ = 100 µA, $I_{IN}(+)$ = 0 | | 2 | 50 | mV |

## Electrical Characteristics (Continued)

$I_{SET(IN)} = I_{SET(OUT)} = 0.5$ mA, $V_{supply} = 12V$, $T_A = 25^\circ C$ unless otherwise noted

| Parameter | Conditions | LM359 | | | Units |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Output Currents | | | | | |
| Source | $I_{IN}(-)$ and $I_{IN}(+)$ Grounded, $R_L = 100\Omega$ | 16 | 40 | | mA |
| Sink (Linear Region) | $V_{comp} - 0.5V = V_{OUT} = 1V$, $I_{IN}(+) = 0$ | | 4.7 | | mA |
| Sink (Overdriven) | $I_{IN}(-) = 100\ \mu A$, $I_{IN}(+) = 0$, $V_{OUT}$ Force = 1V | 1.5 | 3 | | mA |
| Supply Current | Non-Inverting Input Grounded, $R_L = \infty$ | | 18.5 | 22 | mA |
| Power Supply Rejection (Note 4) | f = 120 Hz, $I_{IN}(+)$ Grounded | 40 | 50 | | dB |

**Note 1:** "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

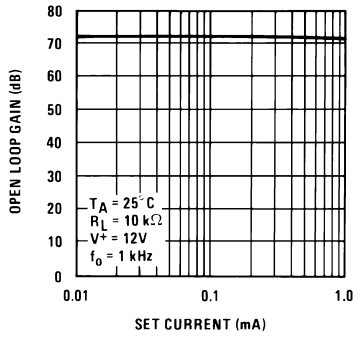
**Note 2:** See Maximum Power Dissipation graph.

**Note 3:** Mirror gain is the current gain of the current mirror which is used as the non-inverting input. $\left(A_I = \frac{I_{IN}(-)}{I_{IN}(+)}\right)$ ΔMirror Gain is the % change in $A_I$ for two different mirror currents at any given temperature.

**Note 4:** See Supply Rejection graphs.

## Typical Performance Characteristics

**Open Loop Gain**

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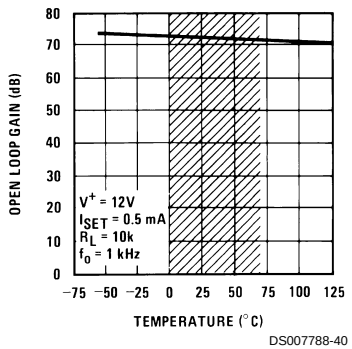
**Open Loop Gain**

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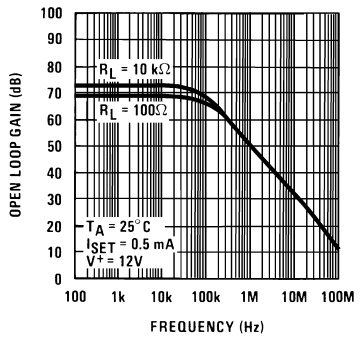
**Note:** Shaded area refers to LM359

**Open Loop Gain**

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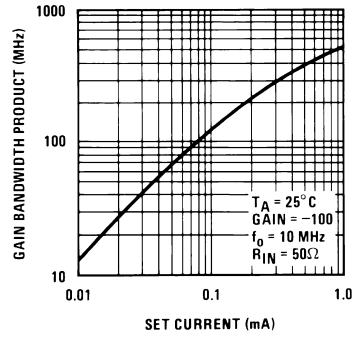
**Gain Bandwidth Product**

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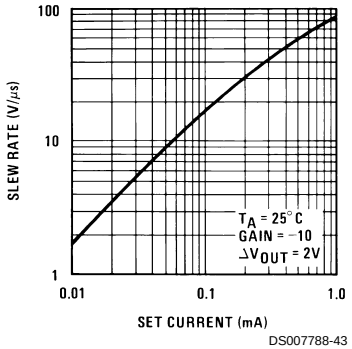
**Slew Rate**

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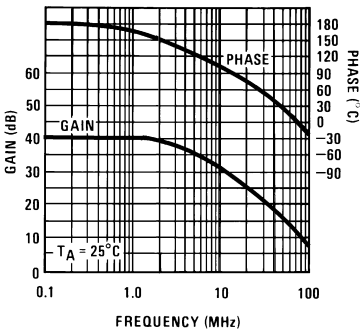
**Gain and Phase**
**Feedback Gain = − 100**

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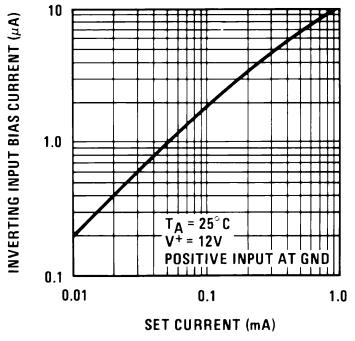
## Typical Performance Characteristics (Continued)

### Inverting Input Bias Current

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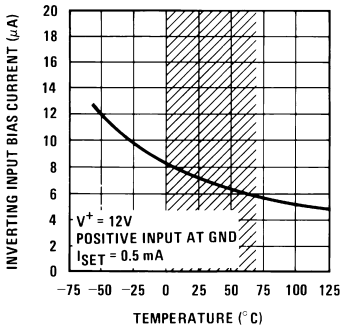
### Inverting Input Bias Current

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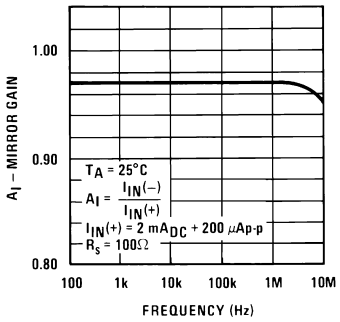
**Note:** Shaded area refers to LM359

### Mirror Gain

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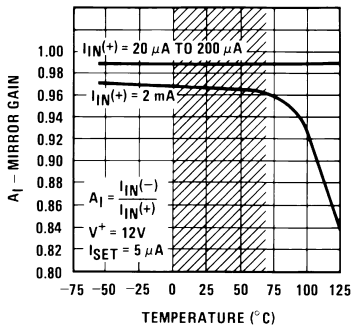
### Mirror Gain

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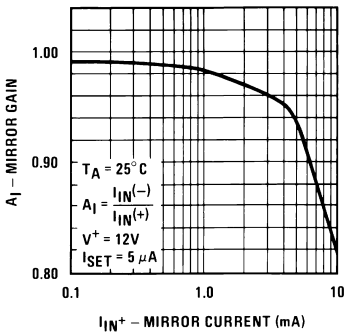
**Note:** Shaded area refers to LM359

### Mirror Gain

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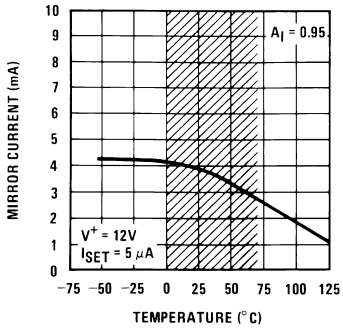
### Mirror Current

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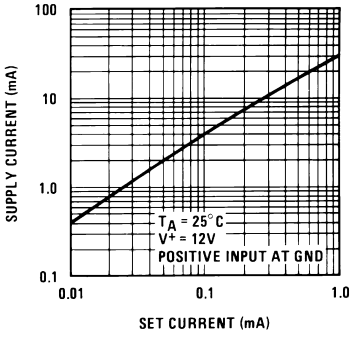
**Note:** Shaded area refers to LM359

### Supply Current

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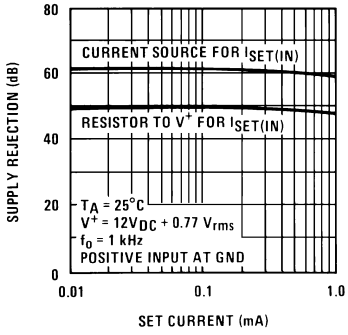
### Supply Rejection

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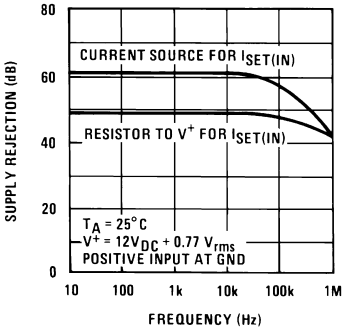
### Supply Rejection

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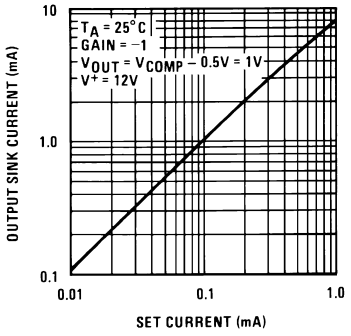
## Typical Performance Characteristics (Continued)

**Output Sink Current**

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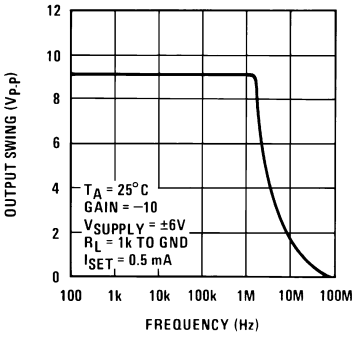
**Output Swing**

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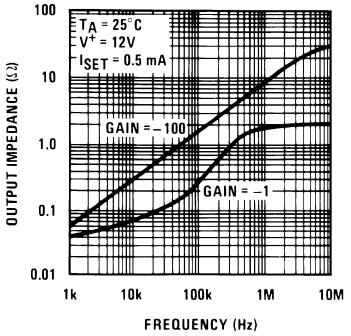
**Output Impedance**

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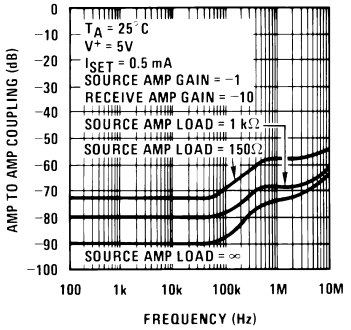
**Amplifier to Amplifier Coupling (Input Referred)**

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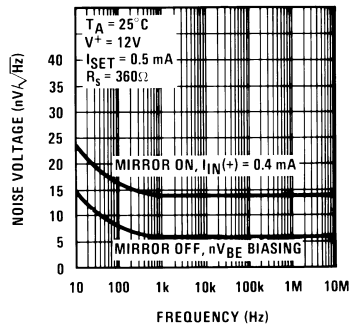
**Noise Voltage**

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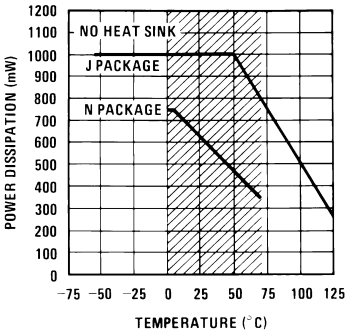
**Maximum Power Dissipation**

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**Note:** Shaded area refers to LM359J/LM359N

## Application Hints

The LM359 consists of two wide bandwidth, decompensated current differencing (Norton) amplifiers. Although similar in operation to the original LM3900, design emphasis for these amplifiers has been placed on obtaining much higher frequency performance as illustrated in *Figure 1*.

This significant improvement in frequency response is the result of using a common-emitter/common-base (cascode) gain stage which is typical in many discrete and integrated video and RF circuit designs. Another versatile aspect of these amplifiers is the ability to externally program many internal amplifier parameters to suit the requirements of a wide variety of applications in which this type of amplifier can be used.

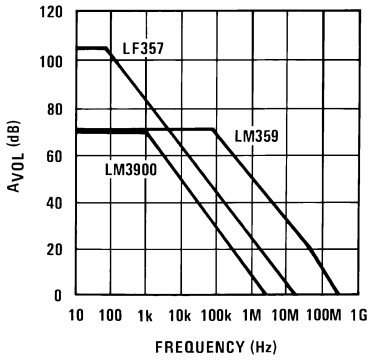


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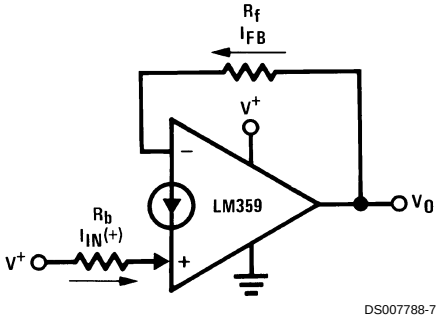
**FIGURE 1.**

### DC BIASING

The LM359 is intended for single supply voltage operation which requires DC biasing of the output. The current mirror circuitry which provides the non-inverting input for the amplifier also facilitates DC biasing the output. The basic operation of this current mirror is that *the current (both DC and AC) flowing into the non-inverting input will force an equal amount of current to flow into the inverting input* . The mirror gain ($A_I$) specification is the measure of how closely these two currents match. For more details see National Application Note AN-72.

## Application Hints (Continued)

DC biasing of the output is accomplished by establishing a reference DC current into the (+) input, $I_{IN}(+)$, and requiring the output to provide the (−) input current. This forces the output DC level to be whatever value necessary (within the output voltage swing of the amplifier) to provide this DC reference current, *Figure 2*.




$$V_{o(DC)} = V_{BE}(-) + I_{FB}\,R_f$$

$$I_{FB} = I_{IN}(+)\,A_I + I_b(-)$$

$$I_{IN}(+) = \frac{V^+ - V_{BE}(+)}{R_b}$$

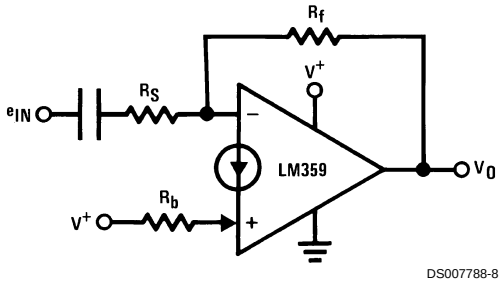
$I_b(-)$ is the inverting input bias current

**FIGURE 2.**

The DC input voltage at each input is a transistor $V_{BE}$ ($\simeq$ 0.6 $V_{DC}$) and must be considered for DC biasing. For most applications, the supply voltage, $V^+$, is suitable and convenient for establishing $I_{IN}(+)$. The inverting input bias current, $I_b(-)$, is a direct function of the programmable input stage current (see current programmability section) and to obtain predictable output DC biasing set $I_{IN}(+) \geq 10 I_b(-)$.

## Application Hints (Continued)

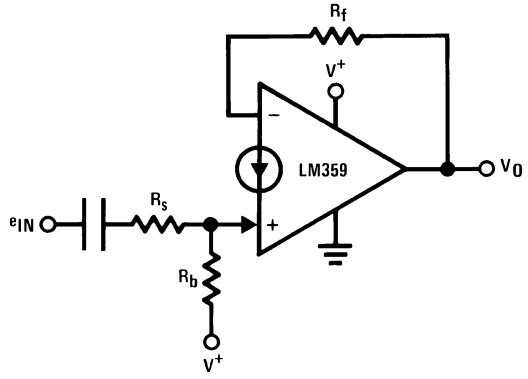
The following figures illustrate typical biasing schemes for AC amplifiers using the LM359:




$$A_{V(AC)} = -\frac{R_f}{R_s}$$

$$V_{o(DC)} = V_{BE}(-) + R_f\left[\frac{V^+ - V_{BE}(+)}{R_b} + I_b(-)\right]$$

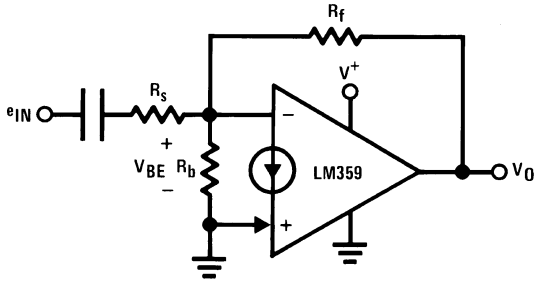
**FIGURE 3. Biasing an Inverting AC Amplifier**




$$A_{V(AC)} = +\frac{R_f}{R_s + r_e}$$

$$V_{o(DC)} = V_{BE}(-) + R_f\left[\frac{V^+ - V_{BE}(+)}{R_b} + I_b(-)\right]$$

**FIGURE 4. Biasing a Non-Inverting AC Amplifier**




$$A_{V(AC)} = -\frac{R_f}{R_s}$$

$$V_{o(DC)} = V_{BE}(-)\left(1 + \frac{R_f}{R_B}\right) + I_b(-)R_f$$

**FIGURE 5. $nV_{BE}$ Biasing**

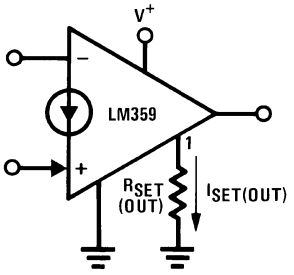
The $nV_{BE}$ biasing configuration is most useful for low noise applications where a reduced input impedance can be accommodated (see typical applications section).

### OPERATING CURRENT PROGRAMMABILITY ($I_{SET}$)

The input bias current, slew rate, gain bandwidth product, output drive capability and total device power consumption of both amplifiers can be simultaneously controlled and optimized via the two programming pins $I_{SET(OUT)}$ and $I_{SET(IN)}$.

#### $I_{SET(OUT)}$

The output set current ($I_{SET(OUT)}$) is equal to the amount of current sourced from pin 1 and establishes the class A biasing current for the Darlington emitter follower output stage. Using a single resistor from pin 1 to ground, as shown in *Figure 6*, this current is equal to:



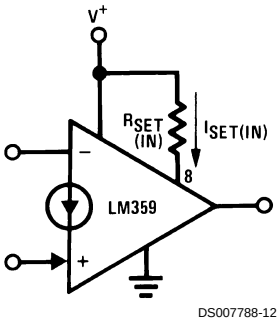

$$I_{SET(OUT)} = \frac{V^+ - V_{BE}}{R_{SET(OUT)} + 500\Omega}$$

**FIGURE 6. Establishing the Output Set Current**

The output set current can be adjusted to optimize the amount of current the output of the amplifier can sink to drive load capacitance and for loads connected to $V^+$. *The maximum output sinking current is approximately 10 times $I_{SET(OUT)}$* . This set current is best used to reduce the total device supply current if the amplifiers are not required to drive small load impedances.

#### $I_{SET(IN)}$

The input set current $I_{SET(IN)}$ is equal to the current flowing into pin 8. A resistor from pin 8 to $V^+$ sets this current to be:




$$I_{SET(IN)} = \frac{V^+ - V_{BE}}{R_{SET(IN)} + 500\Omega}$$

**FIGURE 7. Establishing the Input Set Current**

$I_{SET(IN)}$ is most significant in controlling the AC characteristics of the LM359 as it directly sets the total input stage current of the amplifiers which determines the maximum slew rate, the frequency of the open loop dominant pole, the input resistance of the (−) input and the biasing current $I_b(-)$. All of

## Application Hints (Continued)

these parameters are significant in wide band amplifier design. The input stage current is approximately 3 times $I_{SET(IN)}$ and by using this relationship the following first order approximations for these AC parameters are:

$$S_{r(MAX)} = \text{max slew rate} \cong \frac{3\, I_{SET(IN)}\, (10^{-6})}{C_{comp}} (V/\mu s)$$

$$\text{frequency of dominant pole} \cong \frac{3\, I_{SET(IN)}}{2\pi\, C_{comp}\, A_{VOL}\, (0.026V)} (Hz)$$

$$\text{input resistance} = \beta re \cong \frac{150\, (0.026V)}{3 I_{SET(IN)}} (\Omega)$$

where $C_{comp}$ is the total capacitance from the compensation pin (pin 3 or pin 13) to ground, $A_{VOL}$ is the low frequency open loop voltage gain in V/V and an ambient temperature of 25˚C is assumed (KT/q = 26 mV and $\beta_{typ}$ = 150). $I_{SET(IN)}$ also controls the DC input bias current by the expression:

$$I_b(-) = \frac{3 I_{SET}}{\beta} \cong \frac{I_{SET}}{50} \text{ for NPN } \beta = 150$$

which is important for DC biasing considerations.

The total device supply current (for both amplifiers) is also a direct function of the set currents and can be approximated by:

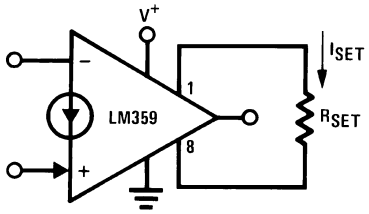
$$I_{supply} \simeq 27 \times I_{SET(OUT)} + 11 \times I_{SET(IN)}$$

with each set current programmed by individual resistors.

### PROGRAMMING WITH A SINGLE RESISTOR

Operating current programming may also be accomplished using only one resistor by letting $I_{SET(IN)}$ equal $I_{SET(OUT)}$. The programming current is now referred to as $I_{SET}$ and it is created by connecting a resistor from pin 1 to pin 8 (*Figure 8*).

$$I_{SET} = \frac{V^+ - 2\, V_{BE}}{R_{SET} + 1\, k\Omega} \text{ where } V_{BE} \cong 0.6V$$




$I_{SET(IN)} = I_{SET(OUT)} = I_{SET}$

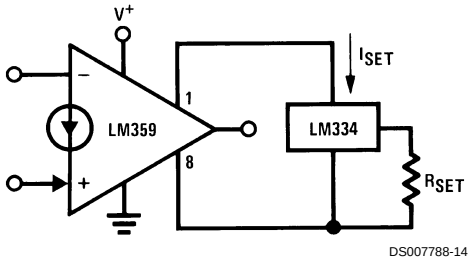
**FIGURE 8. Single Resistor Programming of $I_{SET}$**

This configuration does not affect any of the internal set current dependent parameters differently than previously discussed except the total supply current which is now equal to:

$$I_{supply} \simeq 37 \times I_{SET}$$

Care must be taken when using resistors to program the set current to prevent significantly increasing the supply voltage above the value used to determine the set current. This would cause an increase in total supply current due to the resulting increase in set current and the maximum device power dissipation could be exceeded. The set resistor value(s) should be adjusted for the new supply voltage.

One method to avoid this is to use an adjustable current source which has voltage compliance to generate the set current as shown in *Figure 9*.




$$I_{SET} = \frac{67.7\ mV}{R_{SET}} @ 25°C$$

**FIGURE 9. Current Source Programming of $I_{SET}$**

This circuit allows $I_{SET}$ to remain constant over the entire supply voltage range of the LM359 which also improves power supply ripple rejection as illustrated in the Typical Performance Characteristics. It should be noted, however, that the current through the LM334 as shown will change linearly with temperature but this can be compensated for (see LM334 data sheet).

Pin 1 must never be shorted to ground or pin 8 never shorted to $V^+$ without limiting the current to 2 mA or less to prevent catastrophic device failure.

### CONSIDERATIONS FOR HIGH FREQUENCY OPERATION

The LM359 is intended for use in relatively high frequency applications and many factors external to the amplifier itself must be considered. Minimization of stray capacitances and their effect on circuit operation are the primary requirements. The following list contains some general guidelines to help accomplish this end:

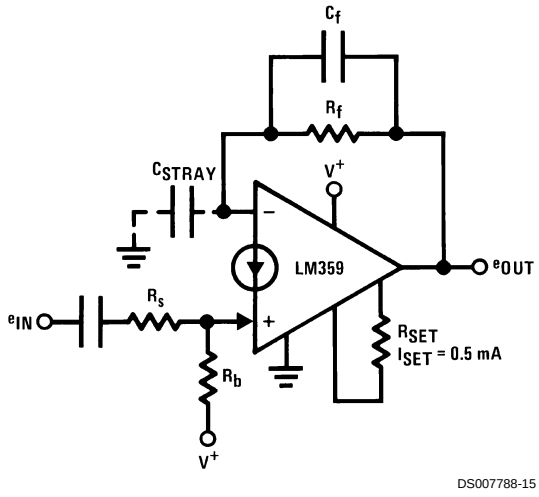
1. Keep the leads of all external components as short as possible.
2. Place components conducting signal current from the output of an amplifier away from that amplifier's non-inverting input.
3. Use reasonably low value resistances for gain setting and biasing.
4. Use of a ground plane is helpful in providing a shielding effect between the inputs and from input to output. Avoid using vector boards.
5. Use a single-point ground and single-point supply distribution to minimize crosstalk. Always connect the two grounds (one from each amplifier) together.
6. Avoid use of long wires (> 2") but if necessary, use shielded wire.
7. Bypass the supply close to the device with a low inductance, low value capacitor (typically a 0.01 µF ceramic) to create a good high frequency ground. If long supply leads are unavoidable, a small resistor (~10Ω) in series with the bypass capacitor may be needed and using shielded wire for the supply leads is also recommended.

### COMPENSATION

The LM359 is internally compensated for stability with closed loop inverting gains of 10 or more. For an inverting gain of less than 10 and all non-inverting amplifiers (the amplifier always has 100% negative current feedback regardless of the

## Application Hints (Continued)

gain in the non-inverting configuration) some external frequency compensation is required because the stray capacitance to ground from the (−) input and the feedback resistor add additional lagging phase within the feedback loop. The value of the input capacitance will typically be in the range of 6 pF to 10 pF for a reasonably constructed circuit board. When using a feedback resistance of 30 kΩ or less, the best method of compensation, without sacrificing slew rate, is to add a lead capacitor in parallel with the feedback resistor with a value on the order of 1 pF to 5 pF as shown in *Figure 10* .




$C_f$ = 1 pF to 5 pF for stability

**FIGURE 10. Best Method of Compensation**

Another method of compensation is to increase the effective value of the internal compensation capacitor by adding capacitance from the COMP pin of an amplifier to ground. An external 20 pF capacitor will generally compensate for all gain settings but will also reduce the gain bandwidth product and the slew rate. These same results can also be obtained by reducing $I_{SET(IN)}$ if the full capabilities of the amplifier are not required. This method is termed over-compensation.

Another area of concern from a stability standpoint is that of capacitive loading. The amplifier will generally drive capacitive loads up to 100 pF without oscillation problems. Any larger C loads can be isolated from the output as shown in *Figure 11*. Over-compensation of the amplifier can also be used if the corresponding reduction of the GBW product can be afforded.

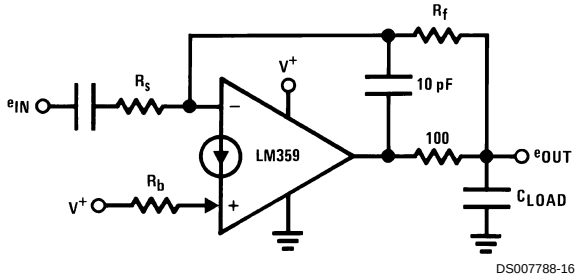



**FIGURE 11. Isolating Large Capacitive Loads**

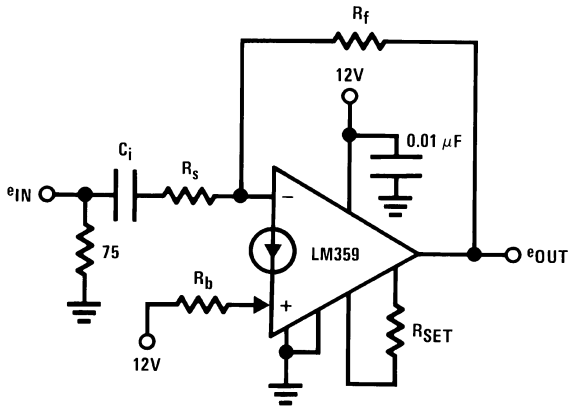
In most applications using the LM359, the input signal will be AC coupled so as not to affect the DC biasing of the amplifier. This gives rise to another subtlety of high frequency circuits which is the effective series inductance (ESL) of the coupling capacitor which creates an increase in the impedance of the capacitor at high frequencies and can cause an unexpected gain reduction. Low ESL capacitors like solid tantalum for large values of C and ceramic for smaller values are recommended. A parallel combination of the two types is even better for gain accuracy over a wide frequency range.

### AMPLIFIER DESIGN EXAMPLES

The ability of the LM359 to provide gain at frequencies higher than most monolithic amplifiers can provide makes it most useful as a basic broadband amplification stage. The design of standard inverting and non-inverting amplifiers, though different than standard op amp design due to the current differencing inputs, also entail subtle design differences between the two types of amplifiers. These differences will be best illustrated by design examples. For these examples a practical video amplifier with a passband of 8 Hz to 10 MHz and a gain of 20 dB will be used. It will be assumed that the input will come from a 75Ω source and proper signal termination will be considered. The supply voltage is 12 $V_{DC}$ and single resistor programming of the operating current, $I_{SET}$, will be used for simplicity.

### AN INVERTING VIDEO AMPLIFIER

1. Basic circuit configuration:




2. Determine the required $I_{SET}$ from the characteristic curves for gain bandwidth product.

$$GBW_{MIN} = 10 \times 10\ MHz = 100\ MHz$$

For a flat response to 10 MHz a closed loop response to two octaves above 10 MHz (40 MHz) will be sufficient.
Actual GBW = 10 x 40 MHz = 400 MHz
$I_{SET}$ required = 0.5 mA

$$R_{SET} = \frac{V^+ - 2\,V_{BE}}{I_{SET}} - 1\,k\Omega = \frac{10.8V}{0.5\,mA} - 1\,k\Omega = 20.6\,k\Omega$$

## Application Hints (Continued)

3. Determine maximum value for $R_f$ to provide stable DC biasing

$$I_{f(MIN)} \geq 10 \times \frac{3\, I_{SET}}{\beta} = \begin{array}{l}100\ \mu A \text{ minimum DC} \\ \text{feedback current}\end{array}$$

Optimum output DC level for maximum symmetrical swing without clipping is:

$$V_{oDC(opt)} = \frac{V_{o(MAX)} - V_{o(MIN)}}{2} + V_{o(MIN)}$$

$$\approx \frac{(V^+ - 3\, V_{BE}) - 2\ mV}{2}$$

$$V_{oDC(opt)} \cong \frac{12 - 1.8V}{2} = \frac{10.2V}{2} = 5.1\ V_{DC}$$

$R_{f(MAX)}$ can now be found:

$$R_{f(MAX)} = \frac{V_{oDC(opt)} - V_{BE}(-)}{I_{f(MIN)}} = \frac{5.1V - 0.6V}{100\ \mu A} = 45\ k\Omega$$

This value should not be exceeded for predictable DC biasing.

4. Select $R_s$ to be large enough so as not to appreciably load the input termination resistance:

$$R_s \geq 750\Omega;\ \text{Let } R_s = 750\Omega$$

5. Select $R_f$ for appropriate gain:

$$A_V = -\frac{R_f}{R_s} \text{ so; } R_f = 10\, R_s = 7.5\ k\Omega$$

7.5 kΩ is less than the calculated $R_{f(MAX)}$ so DC predictability is insured.

6. Since $R_f$ = 7.5k, for the output to be biased to 5.1 $V_{DC}$, the reference current $I_{IN}(+)$ must be:

$$I_{IN}(+) = \frac{5.1V - V_{BE}(-)}{R_f} = \frac{5.1V - 0.6V}{7.5\ k\Omega} = 600\ \mu A$$

Now $R_b$ can be found by:

$$R_b = \frac{V^+ - V_{BE}(+)}{I_{IN}(+)} = \frac{12 - 0.6}{600\ \mu A} = 19\ k\Omega$$

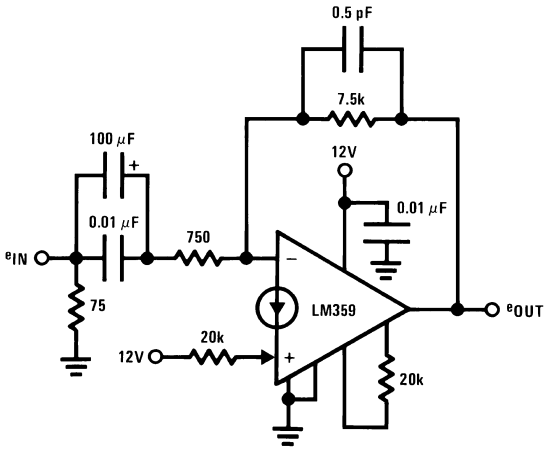
7. Select $C_i$ to provide the proper gain for the 8 Hz minimum input frequency:

$$C_i \geq \frac{1}{2\pi\, R_s\, (f_{low})} = \frac{1}{2\pi\, (750\Omega)\, (8\ Hz)} = 26\ \mu F$$

A larger value of $C_i$ will allow a flat frequency response down to 8 Hz and a 0.01 µF ceramic capacitor in parallel with $C_i$ will maintain high frequency gain accuracy.

8. Test for peaking of the frequency response and add a feedback "lead" capacitor to compensate if necessary.

**Final Circuit Using Standard 5% Tolerance Resistor Values:**

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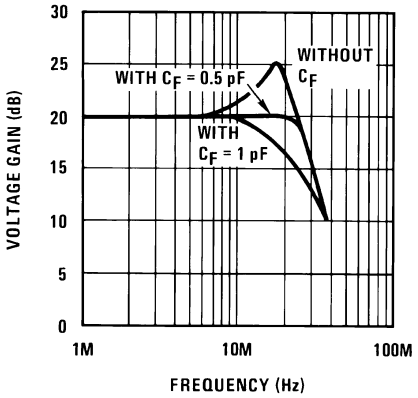
**Circuit Performance:**




DS007788-19

$V_{o(DC)}$ = 5.1V
Differential phase error < 1° for 3.58 MHz $f_{IN}$
Differential gain error < 0.5% for 3.58 MHz $f_{IN}$
$f_{-3\ dB}$ low = 2.5 Hz

### A NON-INVERTING VIDEO AMPLIFIER

For this case several design considerations must be dealt with.

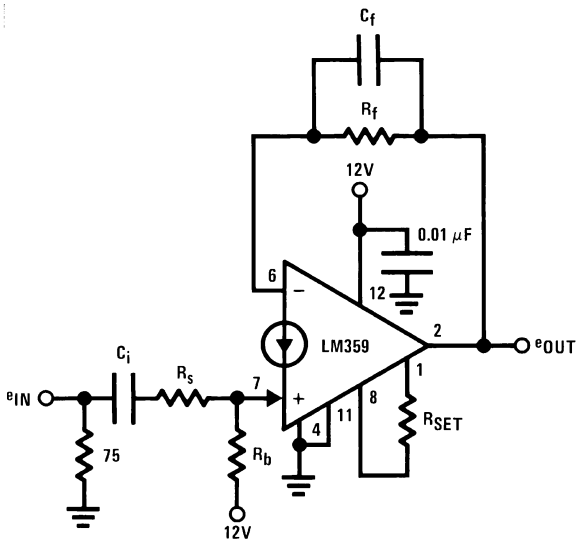
- The output voltage (AC and DC) is strictly a function of the size of the feedback resistor and the sum of AC and DC "mirror current" flowing into the (+) input.
- The amplifier always has 100% current feedback so external compensation is required. Add a small (1 pF–5 pF) feedback capacitance to leave the amplifier's open loop response and slew rate unaffected.
- To prevent saturating the mirror stage the total AC and DC current flowing into the amplifier's (+) input should be less than 2 mA.
- The output's maximum negative swing is one diode above ground due to the $V_{BE}$ diode clamp at the (−) input.

## Application Hints (Continued)

**DESIGN EXAMPLE:**

$e_{IN}$ = 50 mV (MAX), $f_{IN}$ = 10 MHz (MAX), desired circuit BW = 20 MHz, $A_V$ = 20 dB, driving source impedance = 75Ω, $V^+$ = 12V.

1. Basic circuit configuration:




DS007788-20

2. Select $I_{SET}$ to provide adequate amplifier bandwidth so that the closed loop bandwidth will be determined by $R_f$ and $C_f$. To do this, the set current should program an amplifier open loop gain of at least 20 dB at the desired closed loop bandwidth of the circuit. For this example, an $I_{SET}$ of 0.5 mA will provide 26 dB of open loop gain at 20 MHz which will be sufficient. Using single resistor programming for $I_{SET}$:

$$R_{SET} = \frac{V^+ - 2\,V_{BE}}{I_{SET}} - 1\,k\Omega = 20.6\,k\Omega$$

3. Since the closed loop bandwidth will be determined by

$$R_f \text{ and } C_f \left( f_{-3\,dB} = \frac{1}{2\pi\, R_f\, C_f} \right)$$

to obtain a 20 MHz bandwidth, both $R_f$ and $C_f$ should be kept small. It can be assumed that $C_f$ can be in the range of 1 pF to 5 pF for carefully constructed circuit boards to insure stability and allow a flat frequency response. This will limit the value of $R_f$ to be within the range of:

$$\frac{1}{2\pi\ 5\ pF\ 20\ MHz} \le R_f \le \frac{1}{2\pi\ 1\ pF\ 20\ MHz}$$

$$\text{or } 1.6\,k\Omega \le R_f \le 7.96\,k\Omega$$

Also, for a closed loop gain of +10, $R_f$ must be 10 times $R_s$ + $r_e$ where $r_e$ is the mirror diode resistance.

4. So as not to appreciably load the 75Ω input termination resistance the value of ($R_s$ + $r_e$) is set to 750Ω.
5. For $A_v$ = 10; $R_f$ is set to 7.5 kΩ.
6. The optimum output DC level for symmetrical AC swing is:

$$V_{oDC(opt)} = \frac{V_{o(MAX)} - V_{o(MIN)}}{2} + V_{o(MIN)}$$

$$= \frac{(12 - 1.8)V - 0.6V}{2} + 0.6V = 5.4\,V_{DC}$$

7. The DC feedback current must be:

$$I_{FB} = \frac{V_{oDC(opt)} - V_{BE(-)}}{R_f} = \frac{5.4V - 0.6V}{7.5k}$$

$$= 640\ \mu A = I_{IN(+)}$$

DC biasing predictability will be insured because 640 µA is greater than the minimum of $I_{SET}$/5 or 100 µA.
For gain accuracy the total AC and DC mirror current should be less than 2 mA. For this example the maximum AC mirror current will be:

$$\frac{\pm e_{in\ peak}}{R_s + r_e} = \frac{\pm 50\ mV}{750\Omega} = \pm 66\ \mu A$$

therefore the total mirror current range will be 574 µA to 706 µA which will insure gain accuracy.

8. $R_b$ can now be found:

$$R_b = \frac{V^+ - V_{BE(+)}}{I_{IN(+)}} = \frac{12 - 0.6}{640\ \mu A} = 17.8\,k\Omega$$

9. Since $R_s$ + $r_e$ will be 750Ω and $r_e$ is fixed by the DC mirror current to be:

$$r_e = \frac{KT}{q\, I_{IN(+)}} = \frac{26\ mV}{640\ \mu A} \cong 40\Omega \text{ at } 25°C$$

$R_s$ must be 750Ω–40Ω or 710Ω which can be a 680Ω resistor in series with a 30Ω resistor which are standard 5% tolerance resistor values.

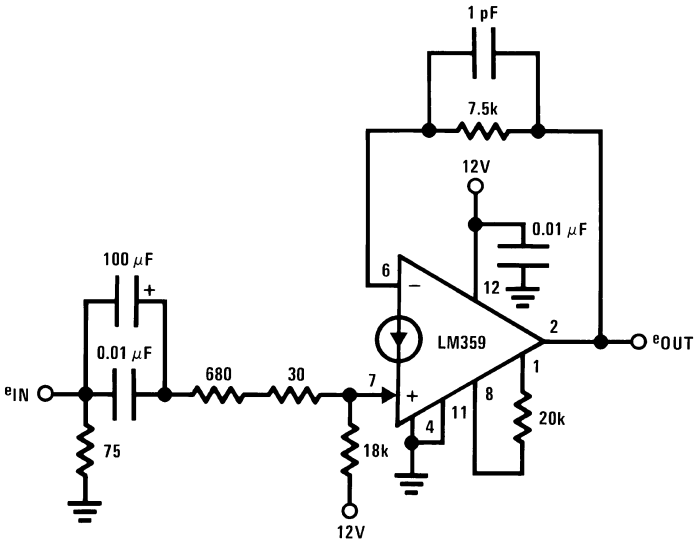
10. As a final design step, $C_i$ must be selected to pass the lower passband frequency corner of 8 Hz for this example.

$$C_i = \frac{1}{2\pi\,(R_s + r_e)\, f_{low}} = \frac{1}{2\pi\,(750\Omega)\,(8\ Hz)} = 26.5\ \mu F$$

A larger value may be used and a 0.01 µF ceramic capacitor in parallel with $C_i$ will maintain high frequency gain accuracy.

## Application Hints (Continued)

**Final Circuit Using Standard 5% Tolerance Resistor Values**

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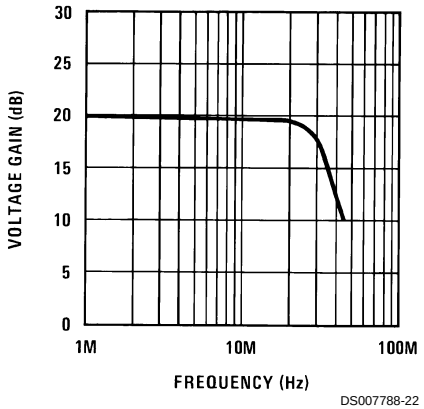
**Circuit Performance**




DS007788-22

$V_{O(DC)}$ = 5.4V
Differential phase error < 0.5°
Differential gain error < 2%
$f_{-3\ dB}$ low = 2.5 Hz

## Application Hints (Continued)

### GENERAL PRECAUTIONS

The LM359 is designed primarily for single supply operation but split supplies may be used if the negative supply voltage is well regulated as the amplifiers have no negative supply rejection.

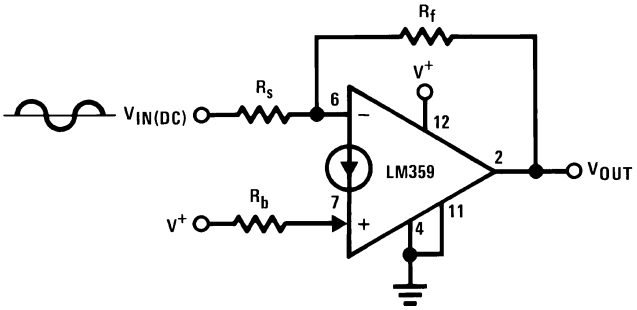
The total device power dissipation must always be kept in mind when selecting an operating supply voltage, the programming current, $I_{SET}$, and the load resistance, particularly when DC coupling the output to a succeeding stage. To prevent damaging the current mirror input diode, the mirror current should always be limited to 10 mA, or less, which is important if the input is susceptible to high voltage transients. The voltage at any of the inputs must not be forced more negative than −0.7V without limiting the current to 10 mA.

The supply voltage must never be reversed to the device; however, plugging the device into a socket backwards would then connect the positive supply voltage to the pin that has no internal connection (pin 5) which may prevent inadvertent device failure.

## Typical Applications

**DC Coupled Inputs**

**Inverting**

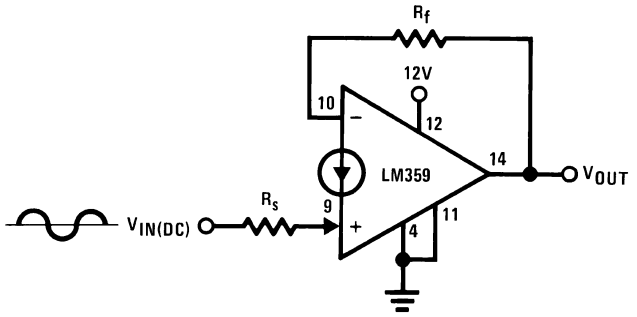



DS007788-23

$$V_{o(DC)} = \left[\frac{V^+ - V_{BE(+)}}{R_b} - \frac{V_{IN(DC)} - V_{BE(-)}}{R_s}\right] R_f + V_{BE(-)}$$

$$A_{V(AC)} = \frac{R_f}{R_s}$$

**Non-Inverting**




DS007788-24

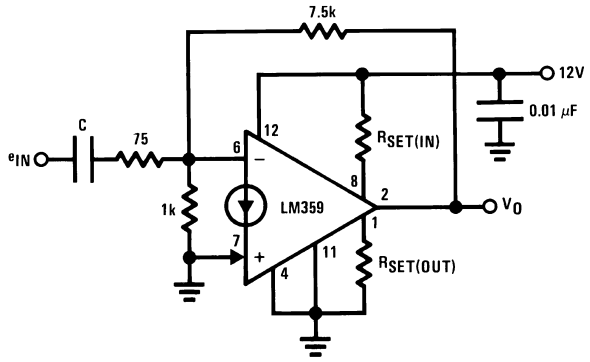
$$V_{o(DC)} = V_{BE(-)} + \frac{(V_{IN(DC)} - V_{BE(+)})\, R_f}{R_s}$$

$$A_{V(AC)} = +\frac{R_f}{R_s + r_{e(+)}}$$

- Eliminates the need for an input coupling capacitor
- Input DC level must be stable and can exceed the supply voltage of the LM359 provided that maximum input currents are not exceeded.

## Typical Applications (Continued)

**Noise Reduction using $nV_{BE}$ Biasing**

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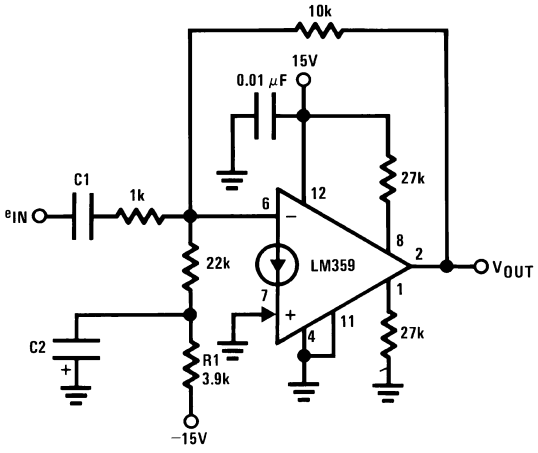
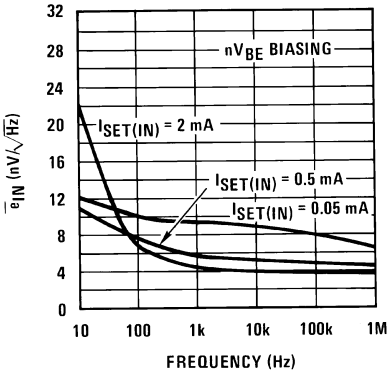
**$nV_{BE}$ Biasing with a Negative Supply**




DS007788-26

- R1 and C2 provide additional filtering of the negative biasing supply

**Typical Input Referred Noise Performance**

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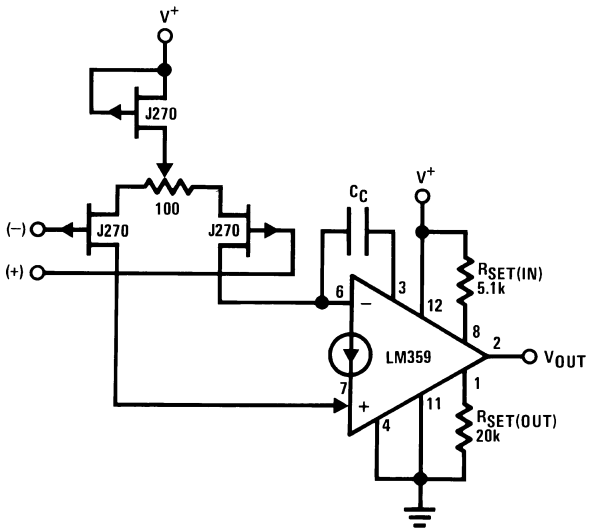
**Adding a JFET Input Stage**

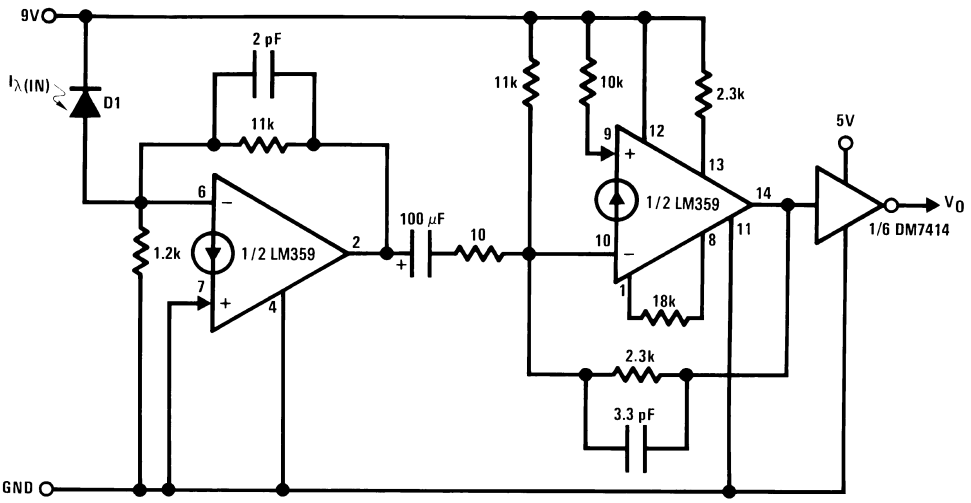



DS007788-28

- FET input voltage mode op amp
- For $A_V$ = +1; BW = 40 MHz, $S_r$ = 60 V/µs; $C_C$ = 51 pF
- For $A_V$ = +11; BW = 24 MHz, $S_r$ = 130 V/µs; $C_C$ = 5 pF
- For $A_V$ = +100; BW = 4.5 MHz, $S_r$ = 150 V/µs; $C_C$ = 2 pF
- $V_{OS}$ is typically <25 mV; 100Ω potentiometer allows a $V_{OS}$ adjust range of ≈ ±200 mV
- Inputs must be DC biased for single supply operation

## Typical Applications (Continued)

**Photo Diode Amplifier**



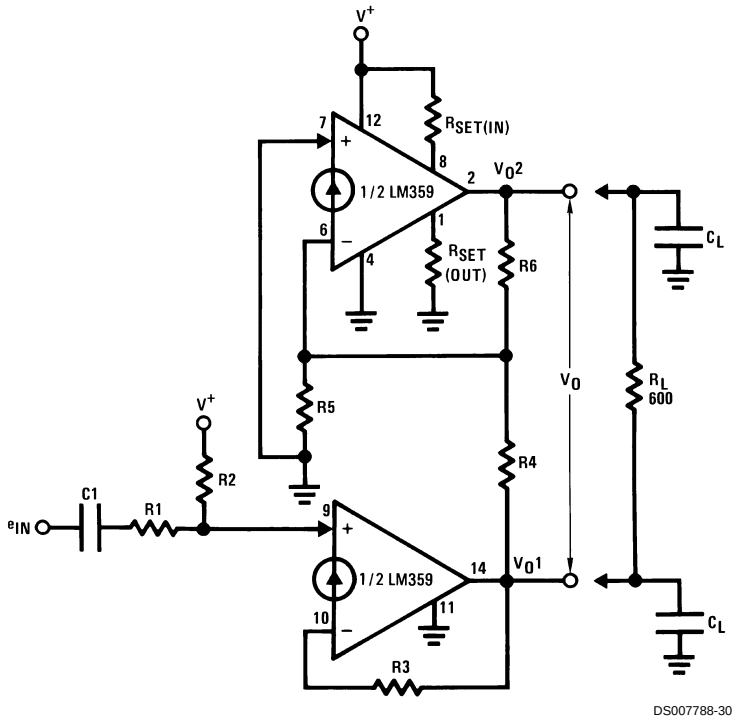

DS007788-29

D1 ~ RCA N-Type Silicon P-I-N Photodiode

- Frequency response of greater than 10 MHz
- If slow rise and fall times can be tolerated the gate on the output can be removed. In this case the rise and the fall time of the LM359 is 40 ns.
- $T_{PDL}$ = 45 ns, $T_{PDH}$ = 50 ns − $T^2L$ output

## Typical Applications (Continued)

**Balanced Line Driver**




DS007788-30

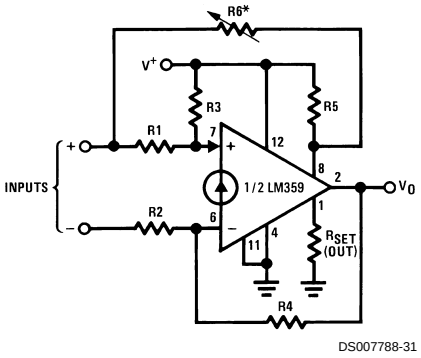
For $V_o1 = V_o2 = \frac{V^+}{2}$, $\frac{R3}{R2} = \frac{V^+ - 2\phi}{2(V^+ - \phi)}$, $\frac{R6}{R5} = \frac{V^+ - 2\phi}{\phi}$ where $\phi \approx 0.6V$

$$A_V = \frac{R3}{R1}\left(\frac{R6}{R4} + 1\right)$$

- 1 MHz−3 dB bandwidth with gain of 10 and 0 dbm into 600Ω
- 0.3% distortion at full bandwidth; reduced to 0.05% with bandwidth of 10 kHz
- Will drive $C_L$ = 1500 pF with no additional compensation, ±0.01 µF with $C_{comp}$ = 180 pF
- 70 dB signal to noise ratio at 0 dbm into 600Ω, 10 kHz bandwidth

## Typical Applications (Continued)

### Difference Amplifier




$$V_{o(DC)} = \frac{R4}{R3}(V^+ - \phi) \text{ where } \phi = 0.6V$$

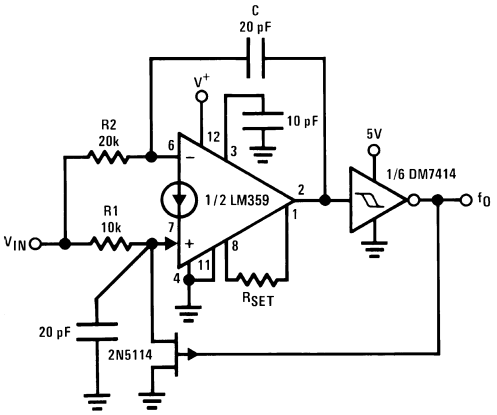
$$A_V = \frac{R4}{R1} \text{ for } R1 = R2$$

- CMRR is adjusted for max at expected CM input signal

$$R6 \approx \frac{R5}{5}, \text{ for } R5 = 100\ k\Omega$$

- Wide bandwidth
- 70 dB CMRR typ
- Wide CM input voltage range

### Voltage Controlled Oscillator




$$f_o = \frac{V_{IN} - \phi}{4\ C\Delta V\ R1}$$

where: R2 = 2R1

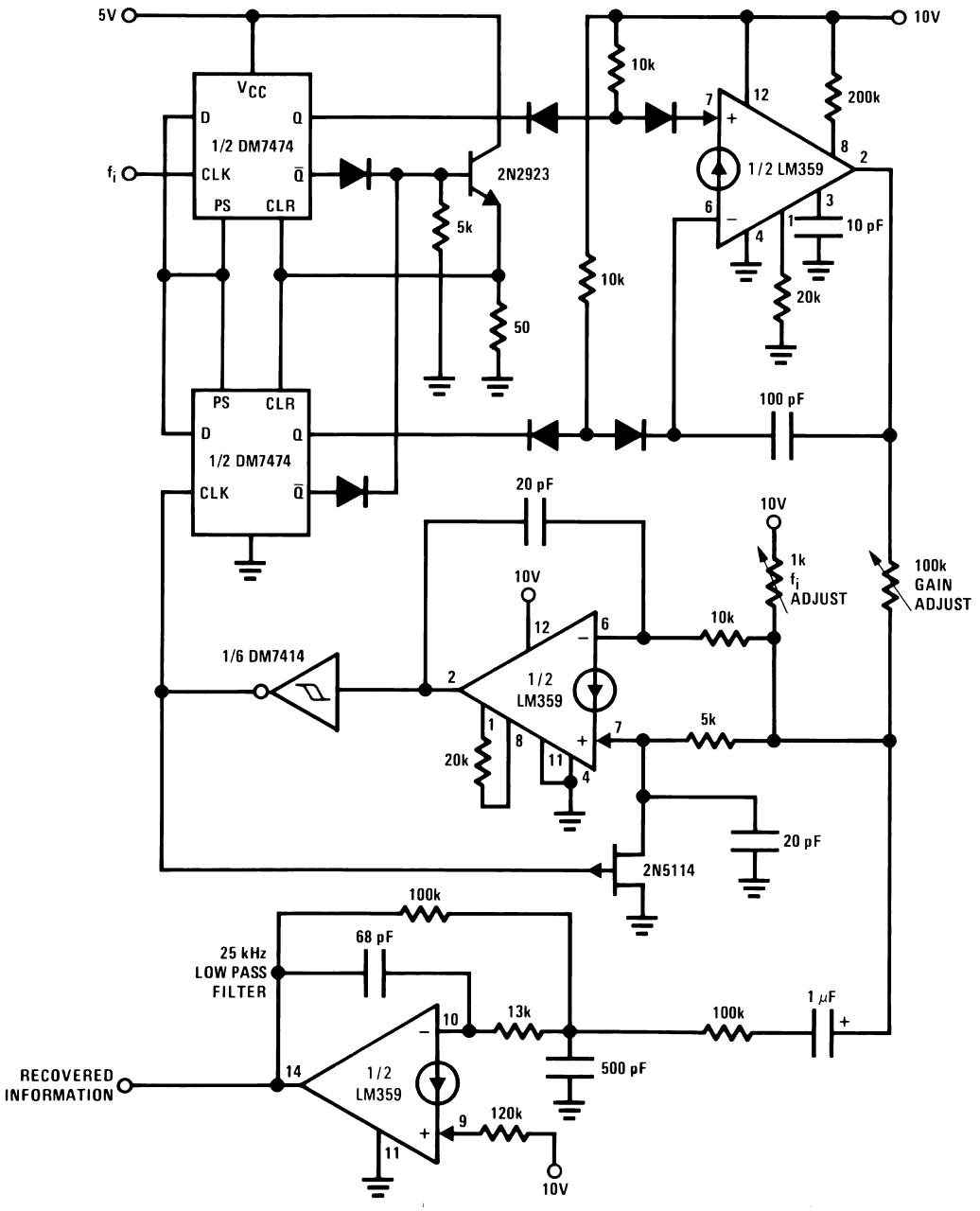
$\phi$ = amplifier input voltage = 0.6V

$\Delta V$ = DM7414 hysteresis, typ 1V

- 5 MHz operation
- $T^2L$ output

## Typical Applications (Continued)

**Phase Locked Loop**



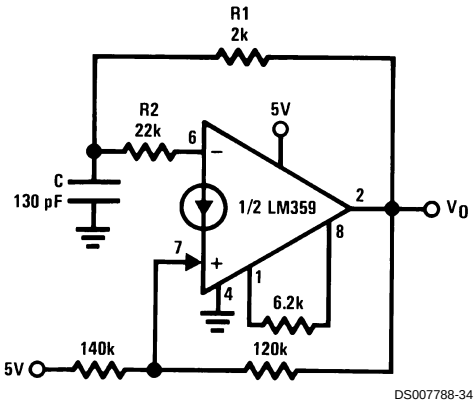

DS007788-33

- Up to 5 MHz operation
- $T^2L$ compatible input

All diodes = 1N914

## Typical Applications (Continued)

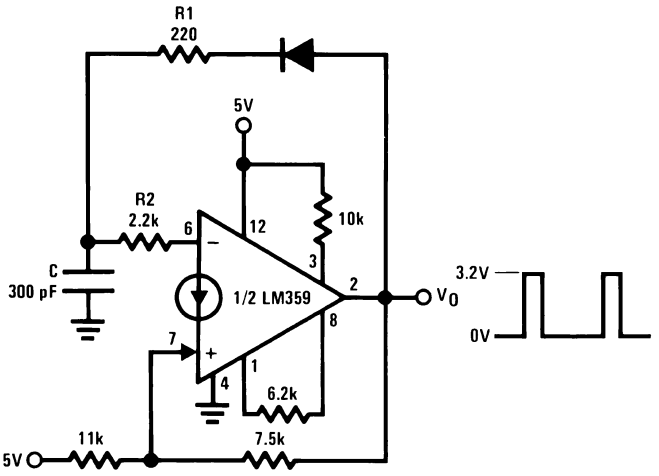
### Squarewave Generator




DS007788-34

f = 1 MHz
Output is TTL compatible
Frequency is adjusted by R1 & C (R1 ≪ R2)

### Pulse Generator

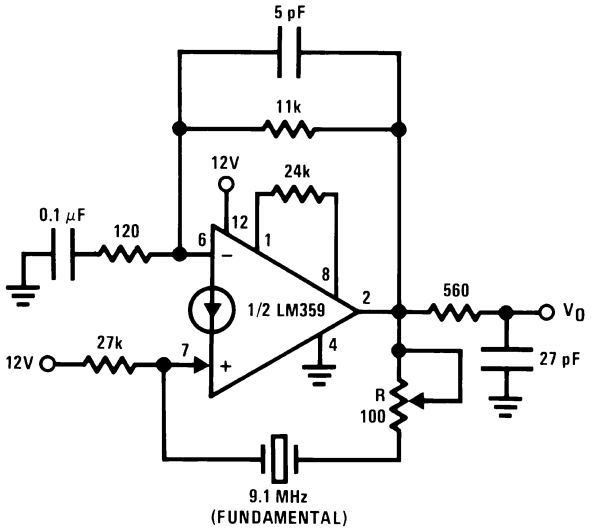



DS007788-36

Output is TTL compatible
Duty cycle is adjusted by R1
Frequency is adjusted by C
f = 1 MHz
Duty cycle = 20%

## Typical Applications (Continued)

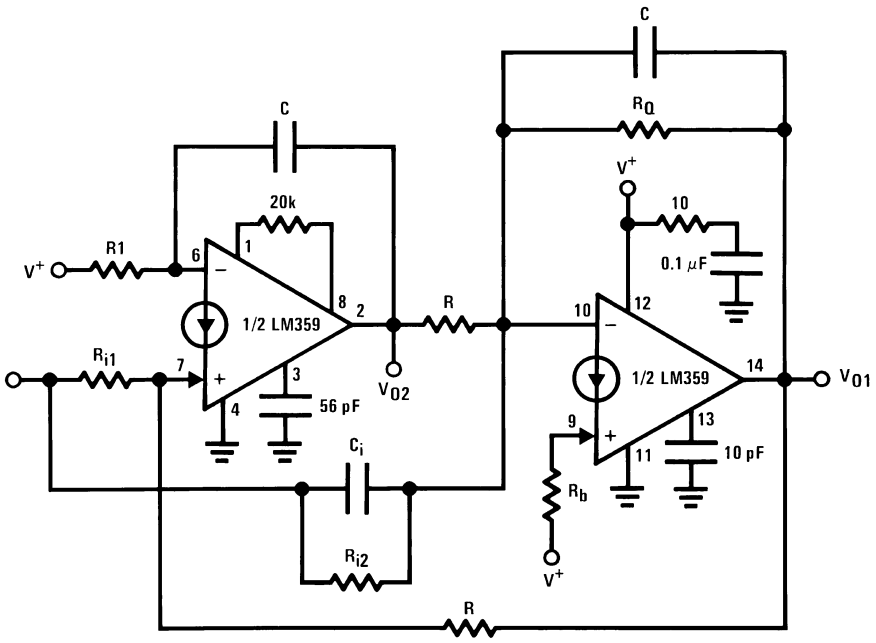
**Crystal Controlled Sinewave Oscillator**




DS007788-37

$V_o$ = 500 mVp-p
f = 9.1 MHz
THD < 2.5%

**High Performance 2 Amplifier Biquad Filter(s)**




DS007788-35

- The high speed of the LM359 allows the center frequency $Q_o$ product of the filter to be: $f_o$x $Q_o \leq 5$ MHz
- The above filter(s) maintain performance over wide temperature range
- One half of LM359 acts as a true non-inverting integrator so only 2 amplifiers (instead of 3 or 4) are needed for the biquad filter structure

## Typical Applications (Continued)

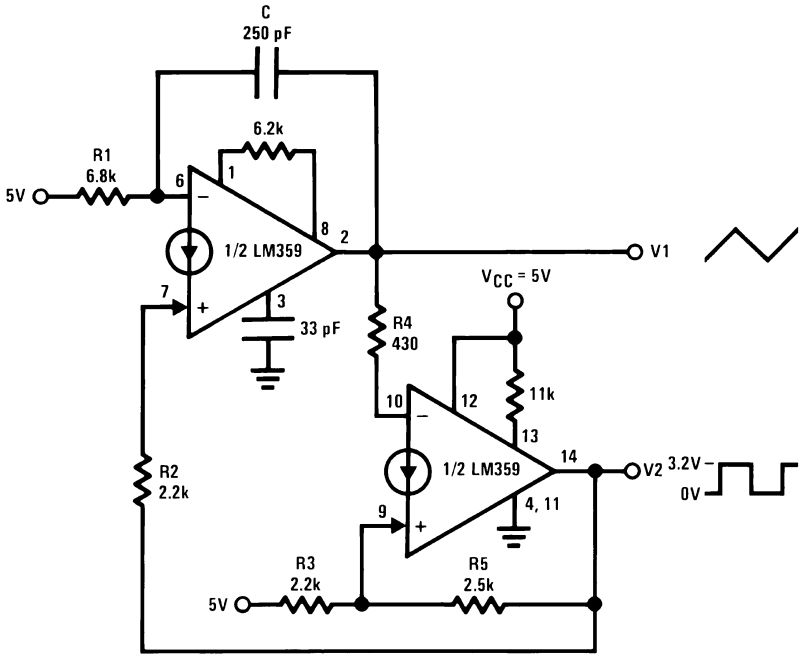
**DC Biasing Equations for $V_{01(DC)} \simeq V_{02(DC)} \simeq V^+/2$**

| | |
|---|---|
| Type I | $\frac{2\,V_{IN(DC)}}{V^+ (R_{i2})} + \frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; R1 = 2R |
| Type II | $\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; R1 = 2R |
| Type III | $\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}; \frac{1}{R1} = \frac{V_{IN(DC)}}{V^+ (R_{i1})} + \frac{1}{2R}$ |

**Analysis and Design Equations**

| Type | $V_{O1}$ | $V_{O2}$ | $C_i$ | $R_{i2}$ | $R_{i1}$ | $f_o$ | $Q_o$ | $f_Z$(notch) | $H_{o(LP)}$ | $H_{o(BP)}$ | $H_{o(HP)}$ | $H_{o(BR)}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| I | BP | LP | O | $R_{i2}$ | ∞ | $\frac{1}{2}\pi RC$ | $R_Q/R$ | — | $R/R_{i2}$ | $R_Q/R_{i2}$ | — | — |
| II | HP | BP | $C_i$ | ∞ | ∞ | $\frac{1}{2}\pi RC$ | $R_Q/R$ | — | — | $R_QC_i/RC$ | $C_i/C$ | — |
| III | Notch/ BR | — | $C_i$ | ∞ | $R_{i1}$ | $\frac{1}{2}\pi RC$ | $R_Q/R$ | $\frac{1}{2\pi}\sqrt{RR_iCC_i}$ | — | — | — | $H_o\Big\vert_{f \to \infty} = C_i/C$<br>$H_o\Big\vert_{f \to O} = C/R_i$ |

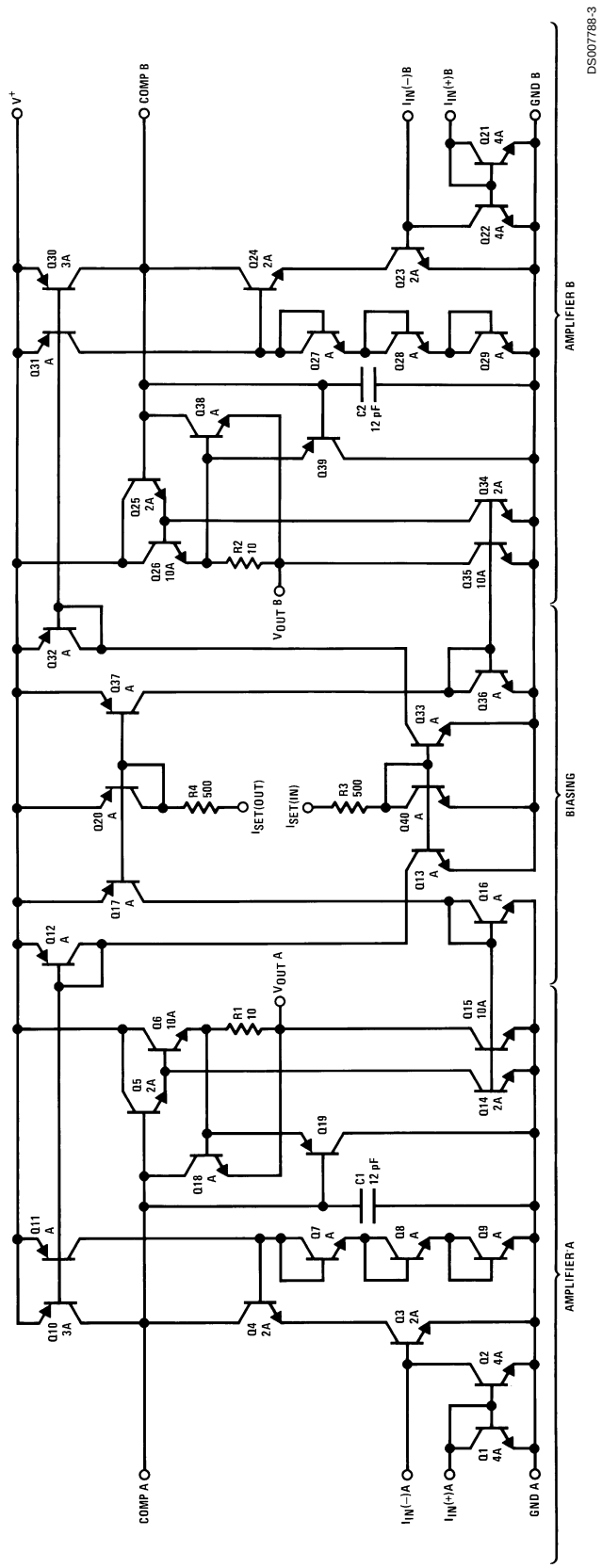
**Triangle Waveform Generator**



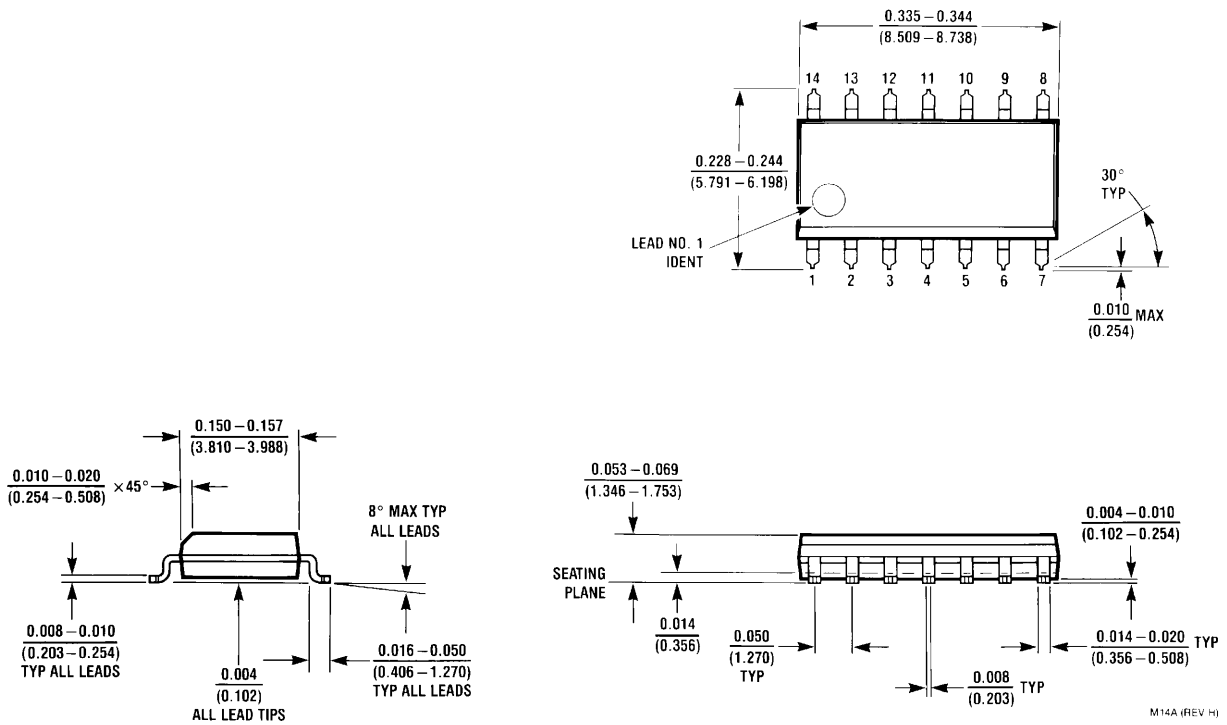

DS007788-38

V2 output is TTL compatible
R2 adjusts for symmetry of the triangle waveform
Frequency is adjusted with R5 and C

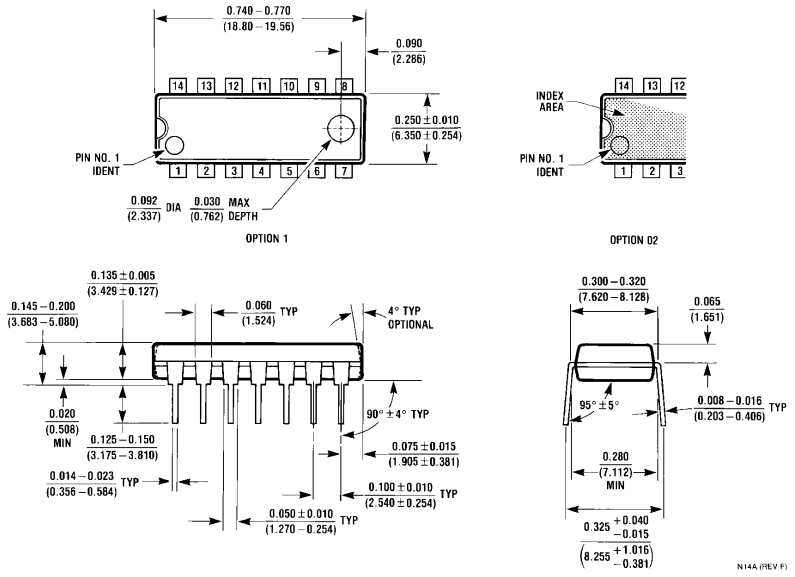
## Schematic Diagram



## Physical Dimensions inches (millimeters) unless otherwise noted




**S.O. Package (M)**
**Order Number LM359M or LM359MX**
**NS Package Number M14A**




**Molded Dual-In-Line Package (N)**
**Order Number LM359N**
**NS Package Number N14A**

## Notes

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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