W40S11-23

Clock Buffer/Driver

Features

- **Thirteen skew-controlled CMOS clock outputs (SDRAM0:12)**
- **Supports three SDRAM DIMMs**
- **Ideal for high-performance systems designed around Intel's latest chip set**
- **SMBus serial configuration interface**
- **Clock Skew between any two outputs is less than 250 ps**
- **1- to 5-ns propagation delay**
- **DC to 133-MHz operation**
- **Single 3.3V supply voltage**
- **Low power CMOS design packaged in a 28-pin, 300-mil SOIC (Small Outline Integrated Circuit), 28-pin, 173-mil (Thin Shrink Small Outline Package), and 28-pin, 209-mil SSOP (Small Shrink Outline Package)**

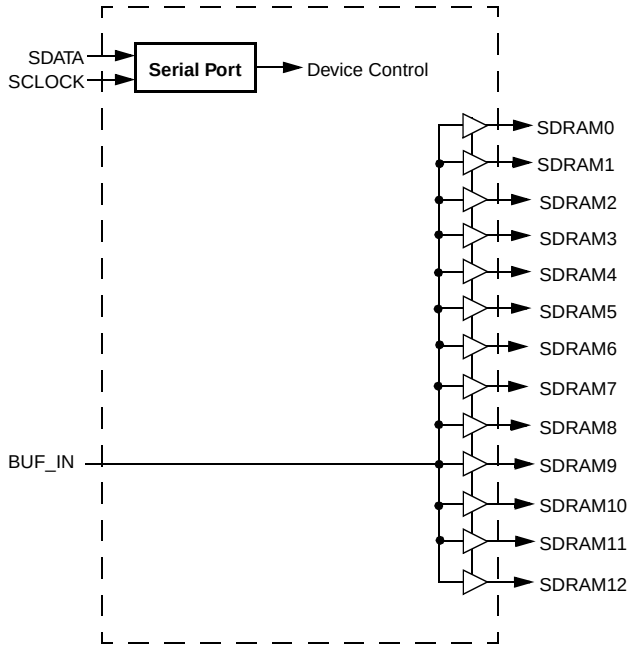
Key Specifications

Supply Voltages: ..... V_{DD} = 3.3V±5%
Operating Temperature: ..... 0°C to +70°C
Input Threshold: ..... 1.5V typical
Maximum Input Voltage: ..... V_{DD} + 0.5V
Input Frequency: ..... 0 to 133 MHz
BUF_IN to SDRAM0:12 Propagation Delay: ..... 1.0 to 5.0 ns
Output Edge Rate: ..... ≥1.5 V/ns
Output Clock Skew: ..... ±250 ps
Output Duty Cycle: ..... 45/55% worst case
Output Impedance: ..... 15Ω typical
Output Type: ..... CMOS rail-to-rail

Overview

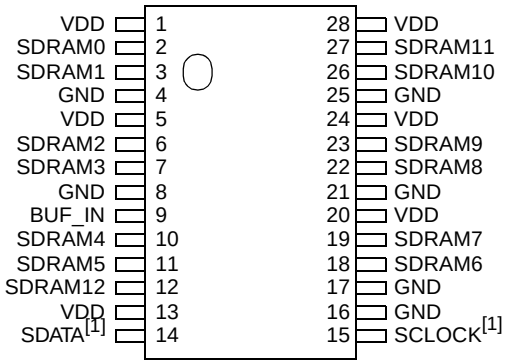
The Cypress W40S11-23 is a low-voltage, thirteen-output clock buffer. Output buffer impedance is approximately 15Ω, which is ideal for driving SDRAM DIMMs.

Block Diagram



Pin Configuration

SOIC



Note:
1. Internal pull-up resistor of 250K on SDATA and SCLOCK inputs (not CMOS level).

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
SDRAM0:12	2, 3, 6, 7, 10, 11, 18, 19, 22, 23, 26, 27, 12	O	***SDRAM Outputs:*** Provides buffered copy of BUF_IN. The propagation delay from a rising input edge to a rising output edge is 1 to 5 ns. All outputs are skew controlled to within ± 250 ps of each other.
BUF_IN	9	I	***Clock Input:*** This clock input has an input threshold voltage of 1.5V (typ).
SDATA	14	I/O	***SMBus Data Input:*** Data should be presented to this input as described in the SMBus section of this data sheet. Internal 250-kΩ pull-up resistor.
SCLOCK	15	I	***SMBus Clock Input:*** The SMBus data clock should be presented to this input as described in the SMBus section of this data sheet. Internal 250-kΩ pull-up resistor.
VDD	1, 5, 13, 20, 24, 28	P	***Power Connection:*** Power supply for core logic and output buffers. Connected to 3.3V supply.
GND	4, 8, 16, 17, 21, 25	G	***Ground Connection:*** Connect all ground pins to the common system ground plane.

Functional Description

Output Drivers

The W40S11-23 output buffers are CMOS type which deliver a rail-to-rail (GND to V_{DD}) output voltage swing into a nominal capacitive load. Thus output signaling is both TTL and CMOS level compatible. Nominal output buffer impedance is 15Ω.

Operation

Data is written to the W40S11-23 in ten bytes of eight bits each. Bytes are written in the order shown in *Table 1*.

Table 1. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the W40S11-23 to accept the bits in Data Bytes 0–6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W40S11-23 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the W40S11-23, bit values are ignored (Don't Care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the W40S11-23, bit values are ignored (Don't Care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to *Table 2*	The data bits in these bytes set internal W40S11-23 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions refer to *Table 2*.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3	Don't Care	Refer to Cypress Frequency Timing Generators.
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Writing Data Bytes

Each bit in the data bytes control a particular device function. Bits are written MSB (most significant bit) first, which is bit 7.

Table 2 gives the bit formats for registers located in Data Bytes 0–6.

Table 2. Data Bytes 0–2 Serial Configuration Map[2]

Bit(s)	Affected Pin		Control Function	Bit Control	
	Pin No.	Pin Name		0	1
Data Byte 0 SDRAM Active/Inactive Register (1 = Enable, 0 = Disable)					
7	11	SDRAM5	Clock Output Disable	Low	Active
6	10	SDRAM4	Clock Output Disable	Low	Active
5	N/A	Reserved	(Reserved)	-	-
4	N/A	Reserved	(Reserved)	-	-
3	7	SDRAM3	Clock Output Disable	Low	Active
2	6	SDRAM2	Clock Output Disable	Low	Active
1	3	SDRAM1	Clock Output Disable	Low	Active
0	2	SDRAM0	Clock Output Disable	Low	Active
Data Byte 1 SDRAM Active/Inactive Register (1 = Enable, 0 = Disable)					
7	27	SDRAM11	Clock Output Disable	Low	Active
6	26	SDRAM10	Clock Output Disable	Low	Active
5	23	SDRAM9	Clock Output Disable	Low	Active
4	22	SDRAM8	Clock Output Disable	Low	Active
3	N/A	Reserved	(Reserved)	-	-
2	N/A	Reserved	(Reserved)	-	-
1	19	SDRAM7	Clock Output Disable	Low	Active
0	18	SDRAM6	Clock Output Disable	Low	Active
Data Byte 2 SDRAM Active/Inactive Register (1 = Enable, 0 = Disable)					
7	N/A	Reserved	(Reserved)	-	-
6	12	SDRAM12	Clock Output Disable	Low	Active
5	N/A	Reserved	(Reserved)	--	--
4	N/A	Reserved	(Reserved)	--	--
3	N/A	Reserved	(Reserved)	--	--
2	N/A	Reserved	(Reserved)	--	--
1	N/A	Reserved	(Reserved)	--	--
0	N/A	Reserved	(Reserved)	--	--

Note:
2. At power-up all SDRAM outputs are enabled and active. Program Reserved bits to a “0.”

How To Use the Serial Data Interface

Electrical Requirements

Figure 1 illustrates electrical characteristics for the serial interface bus used with the W40S11-23. Devices send data over the bus with an open drain logic output that can (a) pull the bus line LOW, or (b) let the bus default to logic 1. The pull-up resistor on the bus (both clock and data lines) establish a default logic 1. All bus devices generally have logic inputs to receive data.

Although the W40S11-23 is a receive-only device (no data write-back capability), it does transmit an “acknowledge” data pulse after each byte is received. Thus, the SDATA line can both transmit and receive data.

The pull-up resistor should be sized to meet the rise and fall times specified in AC parameters, taking into consideration total bus line capacitance.

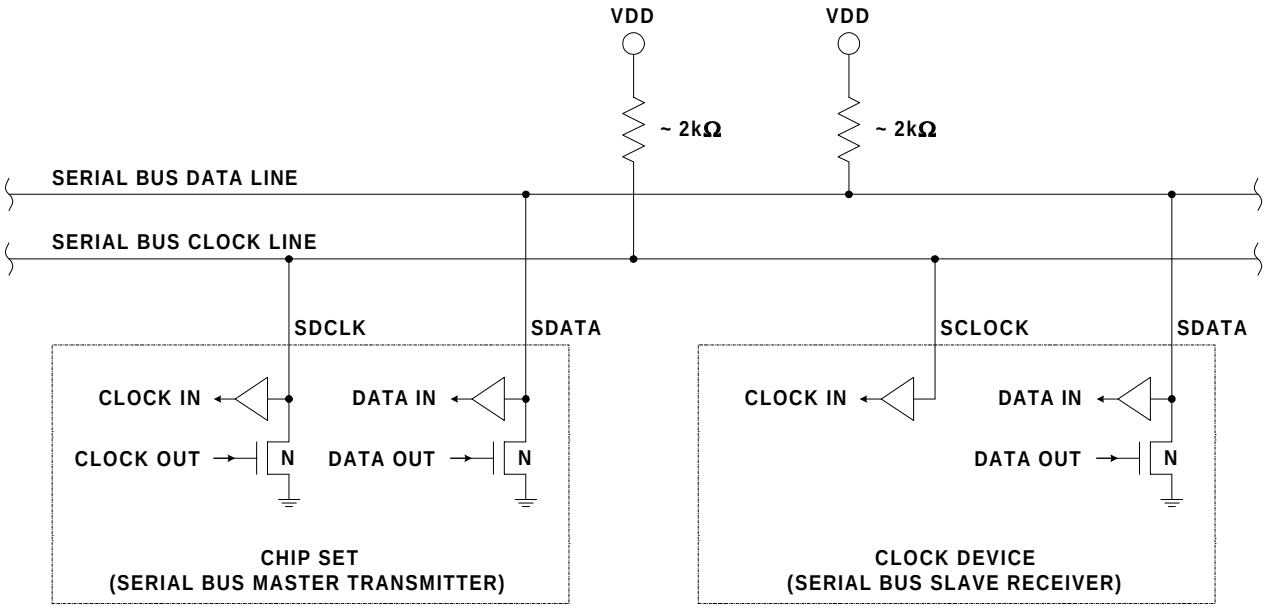


Figure 1. Serial Interface Bus Electrical Characteristics

Signaling Requirements

As shown in *Figure 2*, valid data bits are defined as stable logic 0 or 1 condition on the data line during a clock HIGH (logic 1) pulse. A transitioning data line during a clock HIGH pulse may be interpreted as a start or stop pulse (it will be interpreted as a start or stop pulse if the start/stop timing parameters are met).

A write sequence is initiated by a “start bit” as shown in *Figure 3*. A “stop bit” signifies that a transmission has ended.

As stated previously, the W40S11-23 sends an “acknowledge” pulse after receiving eight data bits in each byte as shown in *Figure 4*.

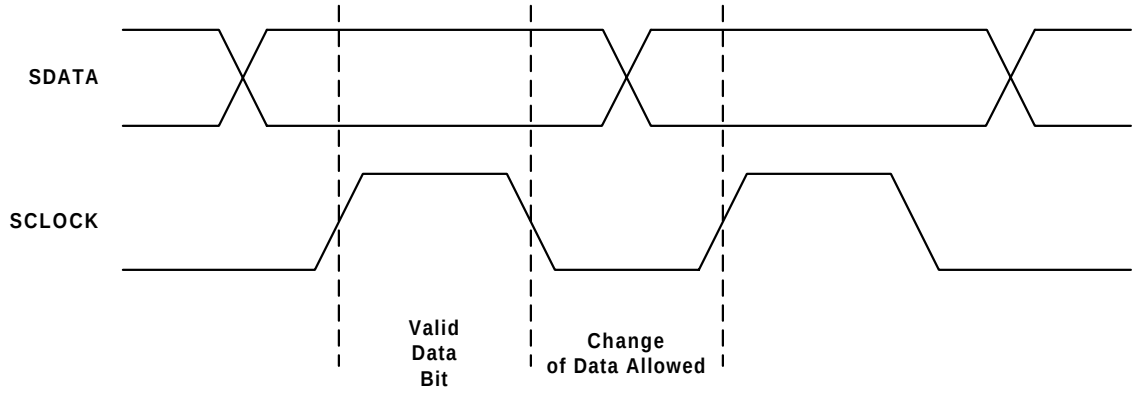


Figure 2. Serial Data Bus Valid Data Bit

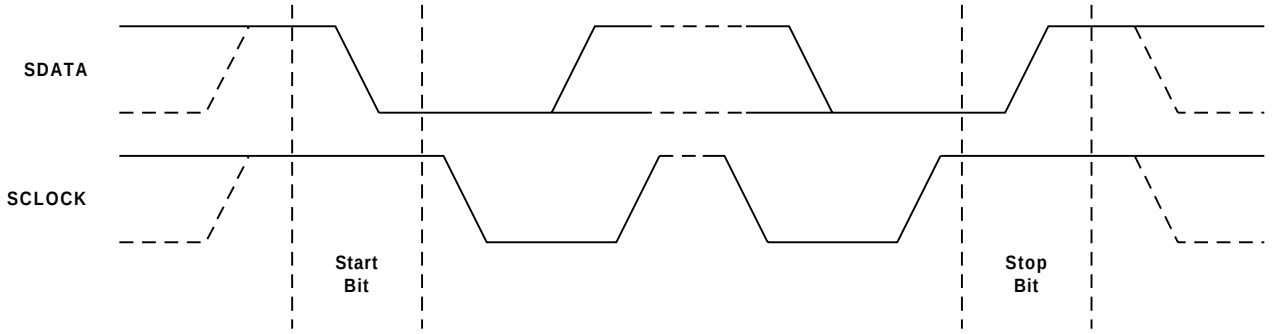


Figure 3. Serial Data Bus Start and Stop Bit

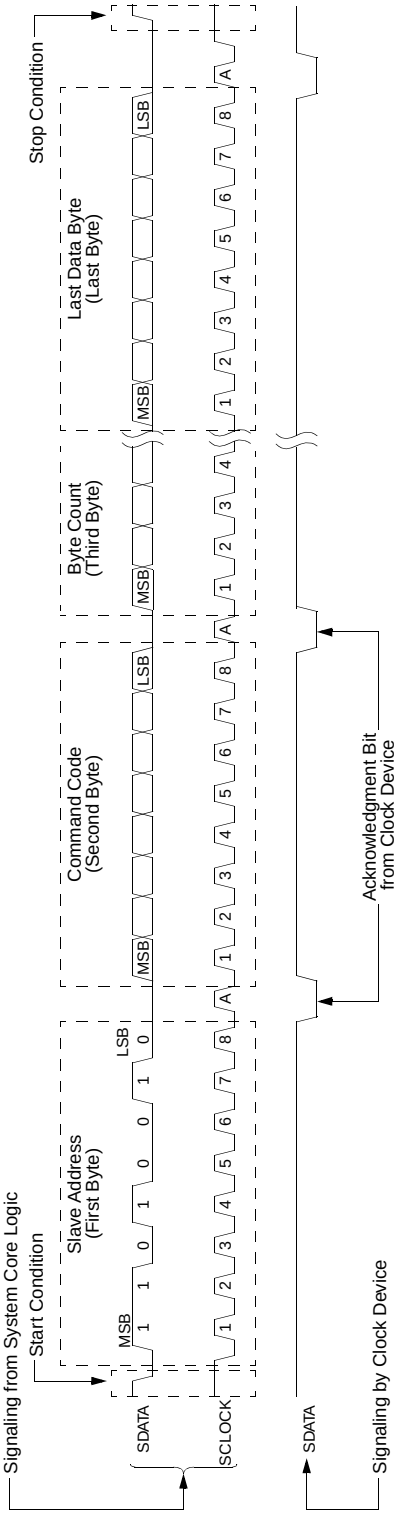


Figure 4. Serial Data Bus Write Sequence

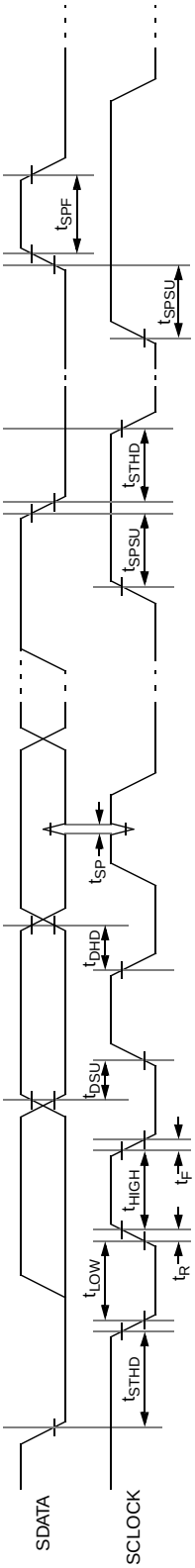


Figure 5. Serial Data Bus Timing Diagram

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 3.3V±5%

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
I_{DD}	3.3V Supply Current	BUF_IN = 100 MHz			250	mA
Logic Inputs						
V_{IL}	Input Low Voltage		GND–0.3		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD}+0.5	V
I_{ILEAK}	Input Leakage Current, BUF_IN		–5		+5	µA
I_{ILEAK}	Input Leakage Current[3]		–20		+5	µA
Logic Outputs (SDRAM0:12)						
V_{OL}	Output Low Voltage	I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage	I_{OH} = –1 mA	3.1			V
I_{OL}	Output Low Current	V_{OL} = 1.5V	65	100	160	mA
I_{OH}	Output High Current	V_{OH} = 1.5V	70	110	185	mA
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance				5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

Note:
3. SDATA and SCLOCK logic pins have 250-kΩ internal pull-up resistors.

AC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 3.3V ±5% (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition	Min	Typ	Max	Unit
f_{IN}	Input Frequency		0		133	MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1.5		4.0	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1.5		4.0	V/ns
t_{SR}	Output Skew, Rising Edges				250	ps
t_{SF}	Output Skew, Falling Edges				250	ps
t_{EN}	Output Enable Time		1.0		8.0	ns
t_{DIS}	Output Disable Time		1.0		8.0	ns
t_{PR}	Rising Edge Propagation Delay		1.0		5.0	ns
t_{PF}	Falling Edge Propagation Delay		1.0		5.0	ns
t_D	Duty Cycle	Measured at 1.5V	45		55	%
Z_o	AC Output Impedance			15		Ω
t_{PR}	Rising Edge Propagation Delay		1.0		5.0	ns

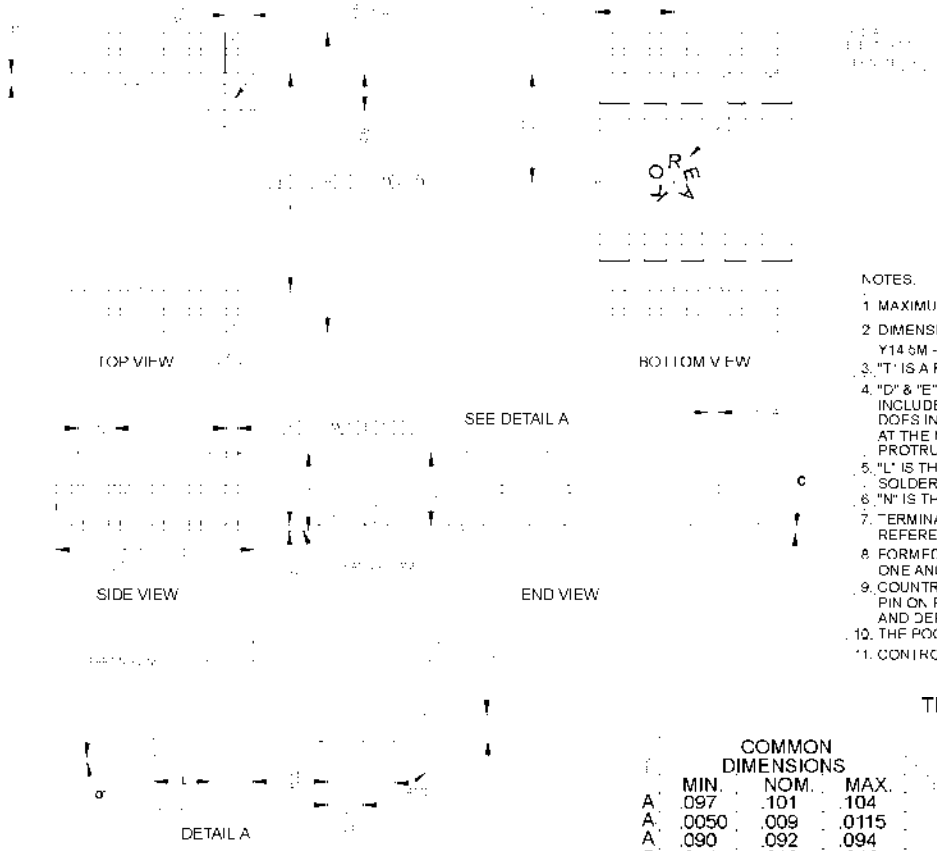
Ordering Information

Ordering Code	Freq. Mask Code	Package Name	Package Type
W40S11	-23	G X H	28-pin SOIC (300 mils) 28-pin TSSOP (173 mil) 28-pin SSOP (209 mil)

Document #: 38-00793-*B

Package Diagrams

28-Pin Small Outline Integrated Circuit (SOIC, 0.300 inch)



NOTES.

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025
2. DIMENSIONING & TOLERANCES PER ANSI Y14.5M - 1982
3. "T" IS A REFERENCE DATUM
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE
6. "N" IS THE NUMBER OF TERMINAL POSITIONS
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. COUNTRY OF ORIGIN, LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION
10. THE POCKETS ON THE BOTTOM ARE OPTIONAL
11. CONTROLLING DIMENSION: INCHES

THIS TABLE IN INCHES

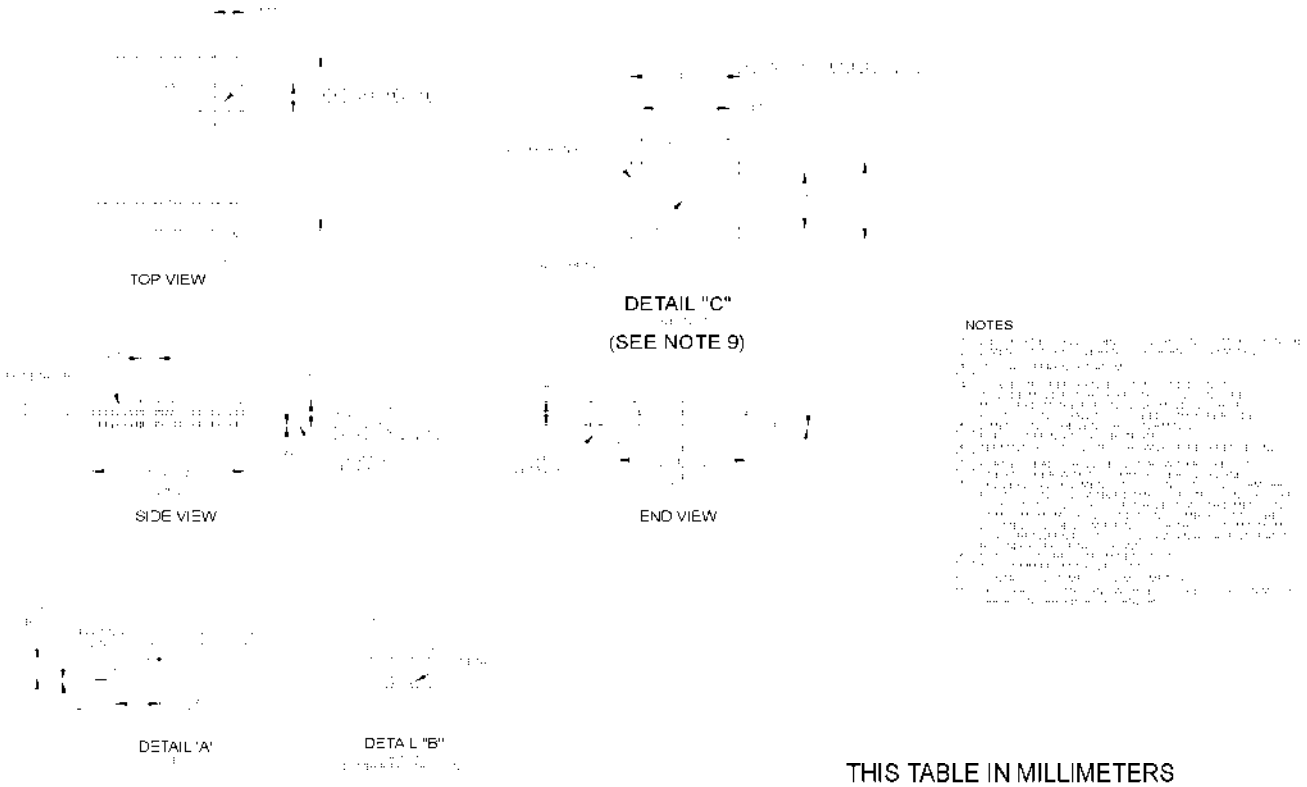
	COMMON DIMENSIONS				NOTE 3 VARIATIONS	D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.097	.101	.104		AA	.402	.407	.412	16
A1	.0050	.009	.0115		AB	.451	.456	.461	18
A2	.090	.092	.094		AC	.500	.505	.510	20
B	.014	.016	.019		AD	.602	.607	.612	24
C	.0091	.010	.0125		AE	.701	.706	.711	28
D	SEE VARIATIONS			3					
E	.292	.296	.299						
e		.050 BSC							
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

	COMMON DIMENSIONS				NOTE 3 VARIATIONS	D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	2.46	2.56	2.64		AA	10.21	10.34	10.46	16
A1	0.127	0.22	0.29		AB	11.46	11.58	11.71	18
A2	2.29	2.34	2.39		AC	12.70	12.83	12.95	20
B	0.35	0.41	0.48		AD	15.29	15.42	15.54	24
C	0.23	0.25	0.32		AE	17.81	17.93	18.06	28
D	SEE VARIATIONS			3					
E	7.42	7.52	7.59						
e		1.27 BSC							
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	2.16	2.36	2.54						

Package Diagrams (continued)

28-Pin Thin Shrink Small Outline Package (TSSOP, 173-mil)



THIS TABLE IN MILLIMETERS

	COMMON DIMENSIONS				NOTE VARI-ATIONS	4 D			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A			1.10		AA	2.90	3.00	3.10	8
A1	0.05	0.10	0.15		AB	4.90	5.00	5.10	14
A2	0.85	0.90	0.95		AC	4.90	5.00	5.10	16
b	0.19	-	0.30	8	AD	6.40	6.50	6.60	20
b1	0.19	0.22	0.25		AE	7.70	7.80	7.90	24
c	0.090	-	0.20		AF	9.60	9.70	9.80	28
c1	0.090	0.127	0.135						
D	SEE VARIATIONS			4					
E	4.30	4.40	4.50	4					
e	0.65 BSC								
H	6.25	6.40	6.50						
L	0.50	0.60	0.70	5					
N	SEE VARIATIONS			6					
	0°	4°	8°						

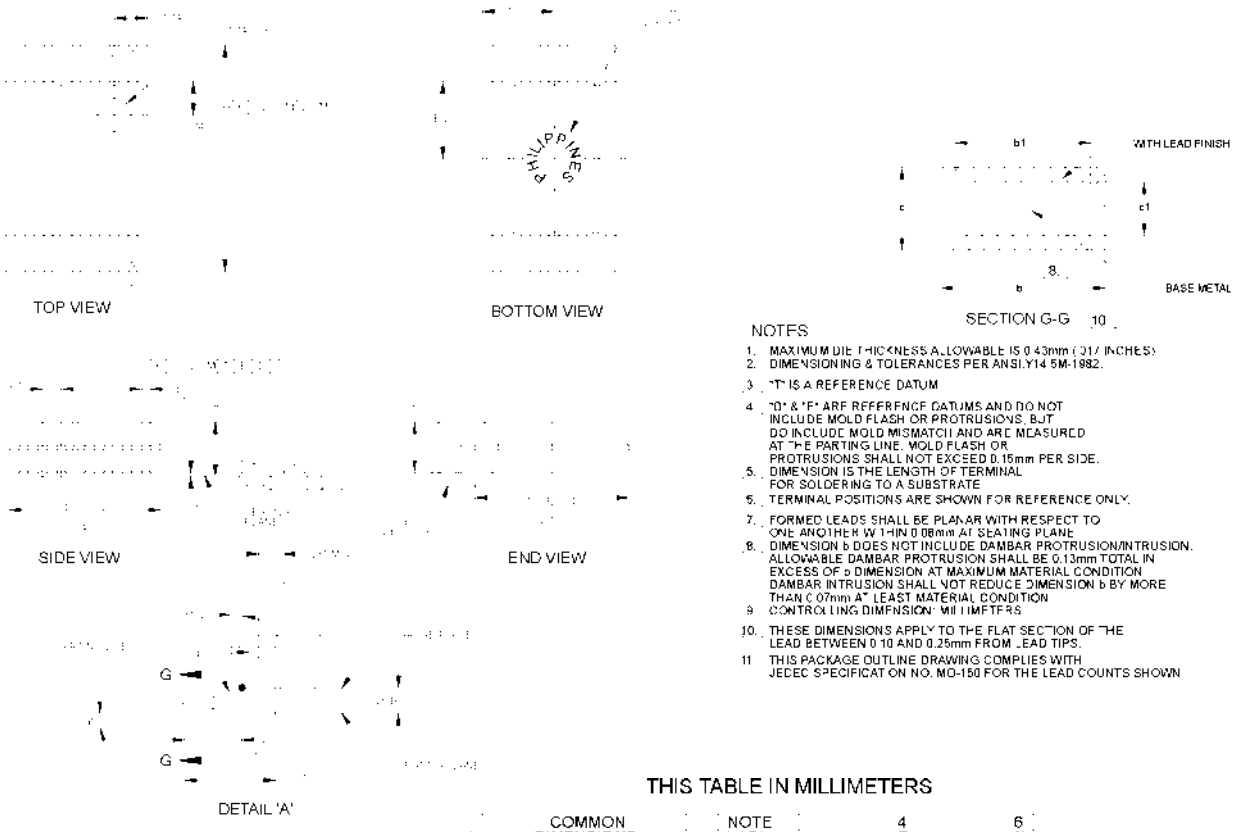
THIS TABLE IN INCHES

	COMMON DIMENSIONS				NOTE VARI-ATIONS	4 D			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A			.0433		AA	114	.118	.122	8
A1	002	.004	.006		AB	193	197	201	14
A2	.0335	.0354	.0374		AC	193	.197	.201	16
b	.0075	-	.0118	8	AD	252	.256	.260	20
b1	0075	0087	0098		AE	303	307	311	24
c	.0035	-	.0079		AF	.378	.382	.386	28
c1	.0035	0050	.0053						
D	SEE VARIATIONS			4					
E	169	.173	.177	4					
e	.0256 BSC								
H	.246	.252	.256						
L	020	.024	.028	5					
N	SEE VARIATIONS			6					
	0°	4°	8°						

VARIATION AF IS DESIGNED BUT NOT TOOLED

Package Diagrams (continued)

28-Pin Small Shrink Outline Package (SSOP, 209 mils)



NOTES

1. MAXIMUM DIE THICKNESS ALLOWABLE IS 0.43mm (.017 INCHES)
2. DIMENSIONING & TOLERANCES PER ANSI Y14.5M-1982.
3. "D" IS A REFERENCE DATUM
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.08mm AT SEATING PLANE
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13mm TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.07mm AT LEAST MATERIAL CONDITION
9. CONTROLLING DIMENSION: MILLIMETERS
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25mm FROM LEAD TIPS.
11. THIS PACKAGE OUTLINE DRAWING COMPLIES WITH JEDEC SPECIFICATION NO. MO-150 FOR THE LEAD COUNTS SHOWN

THIS TABLE IN MILLIMETERS

	COMMON DIMENSIONS			NOTE	VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	1.73	1.86	1.99		AA	9.07	9.20	9.33	14
A1	0.05	0.13	0.21		AB	9.07	9.20	9.33	16
A2	1.68	1.73	1.78		AC	7.07	7.20	7.33	20
b	0.25	-	0.38	8,10	AD	8.07	8.20	8.33	24
b1	0.25	0.30	0.33	10	AE	10.07	10.20	10.33	28
c	0.09	-	0.20	10	AF	10.07	10.20	10.33	30
c1	0.09	0.15	0.16	10					
D	SEE VARIATIONS			4					
E	5.23	5.30	5.38	4					
e	0.65 BSC								
H	7.60	7.80	7.90						
L	0.63	0.75	0.95	5					
L1	1.25 REF								
N	SEE VARIATIONS			6					
	0°	4°	8°						
R	0.09	0.15							

VARIATION AF
IS DESIGNED BUT NOT TOOLED

THIS TABLE IN INCHES

	COMMON DIMENSIONS			NOTE	VARIATIONS	4 D			6 N
	MIN	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.068	.073	.078		AA	.239	.244	.249	14
A1	.002	.005	.008		AB	.239	.244	.249	16
A2	.066	.068	.070		AC	.278	.284	.288	20
b	.010	-	.015	8,10	AD	.318	.323	.328	24
b1	.010	.012	.013	10	AE	.397	.402	.407	28
c	.004	-	.008	10	AF	.397	.402	.407	30
c1	.004	.006	.006	10					
D	SEE VARIATIONS			4					
E	.205	.209	.212	4					
e	.0256 BSC								
H	.301	.307	.311						
L	.025	.030	.037	5					
L1	.049 REF								
N	SEE VARIATIONS			6					
	0°	4°	8°						
R	.004	.006							