



MICROCHIP

24AA512/24LC512/24FC512

512K I²C™ CMOS Serial EEPROM

Device Selection Table

Part Number	Vcc Range	Max. Clock Frequency	Temp. Ranges
24AA512	1.8-5.5V	400 kHz ⁽¹⁾	I
24LC512	2.5-5.5V	400 kHz	I, E
24FC512	2.5-5.5V	1 MHz	I

Note 1: 100 kHz for Vcc < 2.5V

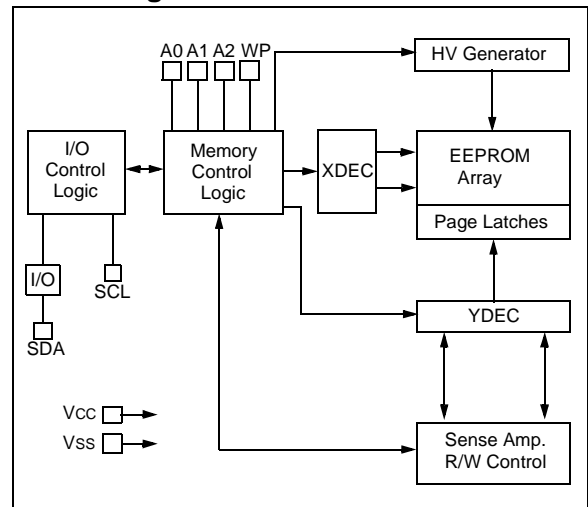
Features:

- Low-power CMOS technology:
 - Maximum write current 5 mA at 5.5V
 - Maximum read current 400 µA at 5.5V
 - Standby current 100 nA, typical at 5.5V
- 2-wire serial interface bus, I²C™ compatible
- Cascadable for up to eight devices
- Self-timed erase/write cycle
- 128-byte Page Write mode available
- 5 ms max. write cycle time
- Hardware write-protect for entire array
- Schmitt Trigger inputs for noise suppression
- 1,000,000 erase/write cycles
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP, SOIC (208 mil), and DFN packages
- 14-lead TSSOP package
- Pb-free finishes available
- Temperature ranges:
 - Industrial (I): -40°C to +85°C
 - Automotive (E): -40°C to +125°C

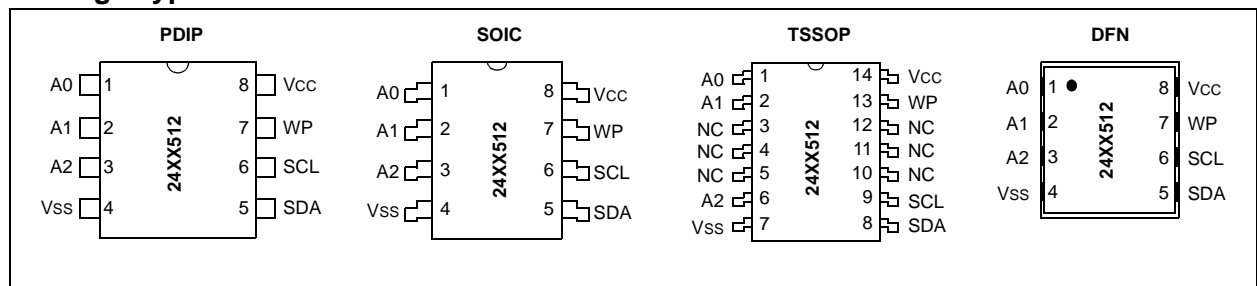
Description:

The Microchip Technology Inc. 24AA512/24LC512/24FC512 (24XX512*) is a 64K x 8 (512 Kbit) Serial Electrically Erasable PROM, capable of operation across a broad voltage range (1.8V to 5.5V). It has been developed for advanced, low-power applications such as personal communications and data acquisition. This device also has a page write capability of up to 128 bytes of data. This device is capable of both random and sequential reads up to the 512K boundary. Functional address lines allow up to eight devices on the same bus, for up to 4 Mbit address space. This device is available in the standard 8-pin plastic DIP, SOIC, DFN and 14-lead TSSOP packages.

Block Diagram



Package Type



* 24XX512 is used in this document as a generic part number for the 24AA512/24LC512/24FC512 devices.

24AA512/24LC512/24FC512

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....	6.5V
All inputs and outputs w.r.t. VSS	-0.6V to VCC +1.0V
Storage temperature	-65°C to +150°C
Ambient temperature with power applied.....	-40°C to +125°C
ESD protection on all pins	≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Electrical Characteristics:			
			Industrial (I): VCC = +1.8V to 5.5V		TA = -40°C to +85°C	
			Automotive (E): VCC = +2.5V to 5.5V		TA = -40°C to +125°C	
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Conditions
D1	—	A0, A1, A2, SCL, SDA and WP pins:	—	—	—	—
D2	VIH	High-level input voltage	0.7 VCC	—	V	—
D3	VIL	Low-level input voltage	—	0.3 VCC 0.2 VCC	V V	VCC ≥ 2.5V VCC < 2.5V
D4	VHYS	Hysteresis of Schmitt Trigger inputs (SDA, SCL pins)	0.05 VCC	—	V	VCC ≥ 2.5V (Note)
D5	VOL	Low-level output voltage	—	0.40	V	IoL = 3.0 ma @ VCC = 4.5V IoL = 2.1 ma @ VCC = 2.5V
D6	ILI	Input leakage current	—	±1	µA	VIN = VSS or VCC, WP = VSS VIN = VSS or VCC, WP = VCC
D7	ILO	Output leakage current	—	±1	µA	VOUT = VSS or VCC
D8	CIN, COUT	Pin capacitance (all inputs/outputs)	—	10	pF	VCC = 5.0V (Note) TA = 25°C, FCLK = 1 MHz
D9	Icc Read	Operating current	—	400	µA	VCC = 5.5V, SCL = 400 kHz
	Icc Write		—	5	mA	VCC = 5.5V
D10	Iccs	Standby current	—	1	µA	TA = -40°C to +85°C SCL = SDA = VCC = 5.5V A0, A1, A2, WP = VSS
			—	5	µA	TA = -40°C to +125°C SCL = SDA = VCC = 5.5V A0, A1, A2, WP = VSS

Note: This parameter is periodically sampled and not 100% tested.

24AA512/24LC512/24FC512

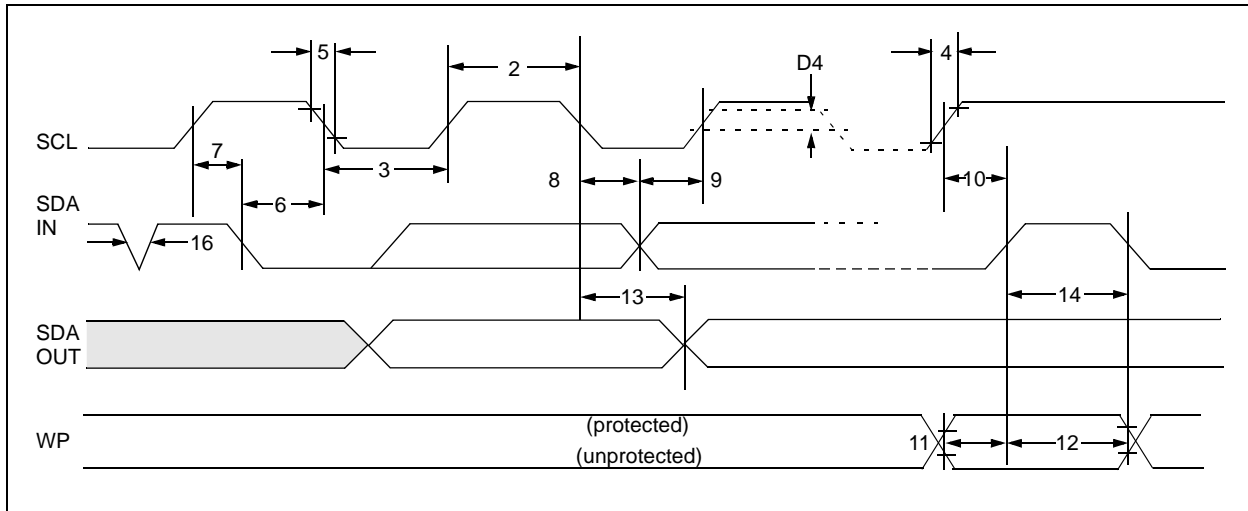
TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics:			
			Industrial (I):		V _{CC} = +1.8V to 5.5V	T _A = -40°C to +85°C
			Automotive (E):		V _{CC} = +2.5V to 5.5V	T _A = -40°C to +125°C
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Conditions
1	FCLK	Clock frequency	—	100	kHz	1.8V ≤ V _{CC} < 2.5V
			—	400		2.5V ≤ V _{CC} ≤ 5.5V
			—	1000		2.5V ≤ V _{CC} ≤ 5.5V 24FC512
2	THIGH	Clock high time	4000	—	ns	1.8V ≤ V _{CC} < 2.5V
			600	—		2.5V ≤ V _{CC} ≤ 5.5V
			500	—		2.5V ≤ V _{CC} ≤ 5.5V 24FC512
3	TLOW	Clock low time	4700	—	ns	1.8V ≤ V _{CC} < 2.5V
			1300	—		2.5V ≤ V _{CC} ≤ 5.5V
			500	—		2.5V ≤ V _{CC} ≤ 5.5V 24FC512
4	TR	SDA and SCL rise time (Note 1)	—	1000	ns	1.8V ≤ V _{CC} < 2.5V
			—	300		2.5V ≤ V _{CC} ≤ 5.5V
			—	300		2.5V ≤ V _{CC} ≤ 5.5V 24FC512
5	TF	SDA and SCL fall time (Note 1)	—	300	ns	All except, 24FC512
			—	100		2.5V ≤ V _{CC} ≤ 5.5V 24FC512
6	THD:STA	Start condition hold time	4000	—	ns	1.8V ≤ V _{CC} < 2.5V
			600	—		2.5V ≤ V _{CC} ≤ 5.5V
			250	—		2.5V ≤ V _{CC} ≤ 5.5V 24FC512
7	TSU:STA	Start condition setup time	4700	—	ns	1.8V ≤ V _{CC} < 2.5V
			600	—		2.5V ≤ V _{CC} ≤ 5.5V
			250	—		2.5V ≤ V _{CC} ≤ 5.5V 24FC512
8	THD:DAT	Data input hold time	0	—	ns	(Note 2)
9	TSU:DAT	Data input setup time	250	—	ns	1.8V ≤ V _{CC} < 2.5V
			100	—		2.5V ≤ V _{CC} ≤ 5.5V
			100	—		2.5V ≤ V _{CC} ≤ 5.5V 24FC512
10	TSU:STO	Stop condition setup time	4000	—	ns	1.8V ≤ V _{CC} < 2.5V
			600	—		2.5V ≤ V _{CC} ≤ 5.5V
			250	—		2.5V ≤ V _{CC} ≤ 5.5V 24FC512
11	TSU:WP	WP setup time	4000	—	ns	1.8V ≤ V _{CC} < 2.5V
			600	—		2.5V ≤ V _{CC} ≤ 5.5V
			600	—		2.5V ≤ V _{CC} ≤ 5.5V 24FC512
12	THD:WP	WP hold time	4700	—	ns	1.8V ≤ V _{CC} < 2.5V
			1300	—		2.5V ≤ V _{CC} ≤ 5.5V
			1300	—		2.5V ≤ V _{CC} ≤ 5.5V 24FC512
13	TAA	Output valid from clock (Note 2)	—	3500	ns	1.8V ≤ V _{CC} < 2.5V
			—	900		2.5V ≤ V _{CC} ≤ 5.5V
			—	400		2.5V ≤ V _{CC} ≤ 5.5V 24FC512
14	TBUF	Bus free time: Time the bus must be free before a new transmission can start	4700	—	ns	1.8V ≤ V _{CC} < 2.5V
			1300	—		2.5V ≤ V _{CC} ≤ 5.5V
			500	—		2.5V ≤ V _{CC} ≤ 5.5V 24FC512
16	TSP	Input filter spike suppression (SDA and SCL pins)	—	50	ns	All except, 24FC512 (Notes 1 and 3)
17	TWC	Write cycle time (byte or page)	—	5	ms	—
18	—	Endurance	1,000,000	—	cycles	25°C (Note 4)

- Note 1:** Not 100% tested. C_B = total capacitance of one bus line in pF.
- Note 2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
- Note 3:** The combined TSP and V_{HYS} specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a T_I specification for standard operation.
- Note 4:** This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at www.microchip.com.

24AA512/24LC512/24FC512

FIGURE 1-1: BUS TIMING DATA



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	PDIP	SOIC	14-lead TSSOP	DFN	Function
A0	1	1	1	1	User Configured Chip Select
A1	2	2	2	2	User Configured Chip Select
(NC)	—	—	3, 4, 5	—	Not Connected
A2	3	3	6	3	User Configured Chip Select
Vss	4	4	7	4	Ground
SDA	5	5	8	5	Serial Data
SCL	6	6	9	6	Serial Clock
(NC)	—	—	10, 11, 12	—	Not Connected
WP	7	7	13	7	Write-Protect Input
Vcc	8	8	14	8	+1.8V to 5.5V (24AA512) +2.5V to 5.5V (24LC512) +2.5V to 5.5V (24FC512)

2.1 A0, A1 and A2 Chip Address Inputs

The A0, A1 and A2 inputs are used by the 24XX512 for multiple device operations. The logic levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight devices may be connected to the same bus by using different Chip Select bit combinations. These inputs must be connected to either Vcc or Vss.

In most applications, the chip address inputs A0, A1 and A2 are hard-wired to logic '0' or logic '1'. For applications in which these pins are controlled by a microcontroller or other programmable logic device, the chip address pins must be driven to logic '0' or logic '1' before normal device operation can proceed.

2.2 Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open-drain terminal, therefore, the SDA bus requires a pull-up resistor to Vcc (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz and 1 MHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

2.3 Serial Clock (SCL)

This input is used to synchronize the data transfer from and to the device.

2.4 Write-Protect (WP)

This pin must be connected to either Vss or Vcc. If tied to Vss, write operations are enabled. If tied to Vcc, write operations are inhibited but read operations are not affected.

3.0 FUNCTIONAL DESCRIPTION

The 24XX512 supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The bus must be controlled by a master device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24XX512 works as a slave. Both master and slave can operate as a transmitter or receiver, but the master device determines which mode is activated.

24AA512/24LC512/24FC512

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line, while the clock line is high, will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus Not Busy (A)

Both data and clock lines remain high.

4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must end with a Stop condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device.

4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit. See Figure 4-2 for acknowledge timing.

Note: The 24XX512 does not generate any Acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24XX512) will leave the data line high to enable the master to generate the Stop condition.

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

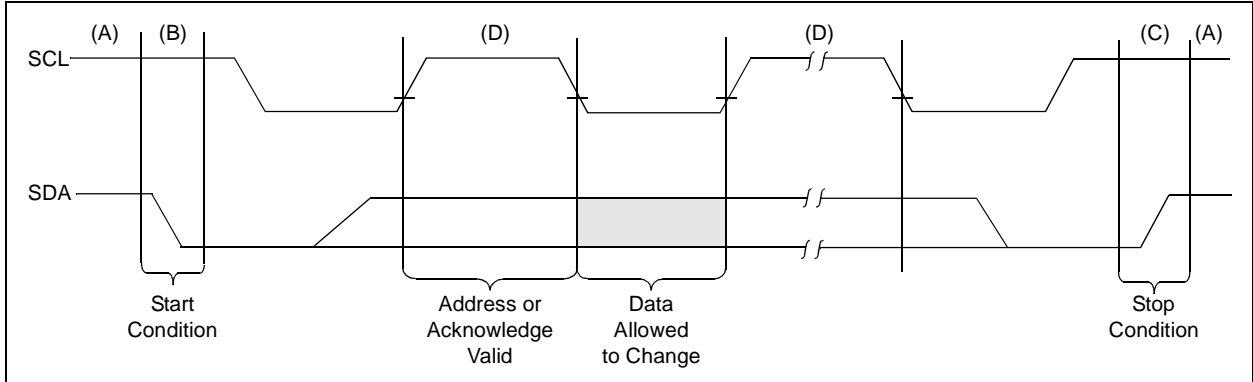
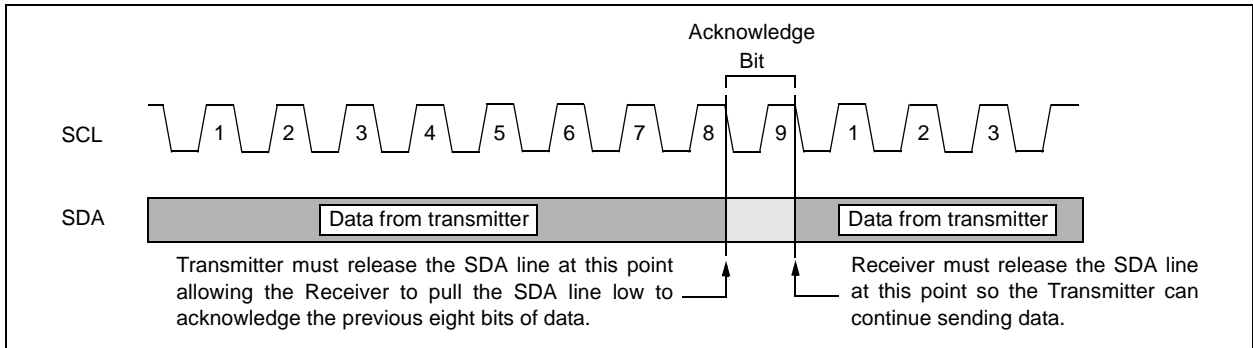


FIGURE 4-2: ACKNOWLEDGE TIMING



24AA512/24LC512/24FC512

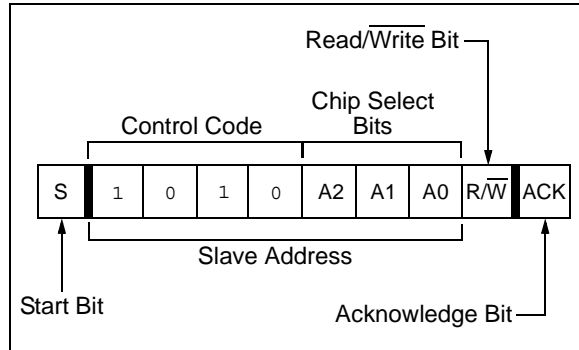
5.0 DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the master device (Figure 5-1). The control byte consists of a 4-bit control code; for the 24XX512 this is set as '1010' binary for read and write operations. The next three bits of the control byte are the Chip Select bits (A2, A1 and A0). The Chip Select bits allow the use of up to eight 24XX512 devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits are in effect the three Most Significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 5-2). Because all A15...A0 are used, there are no upper address bits that are "don't care". The upper address bits are transferred first, followed by the Less Significant bits.

Following the Start condition, the 24XX512 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a '1010' code and appropriate device select bits, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/W bit, the 24XX512 will select a read or write operation.

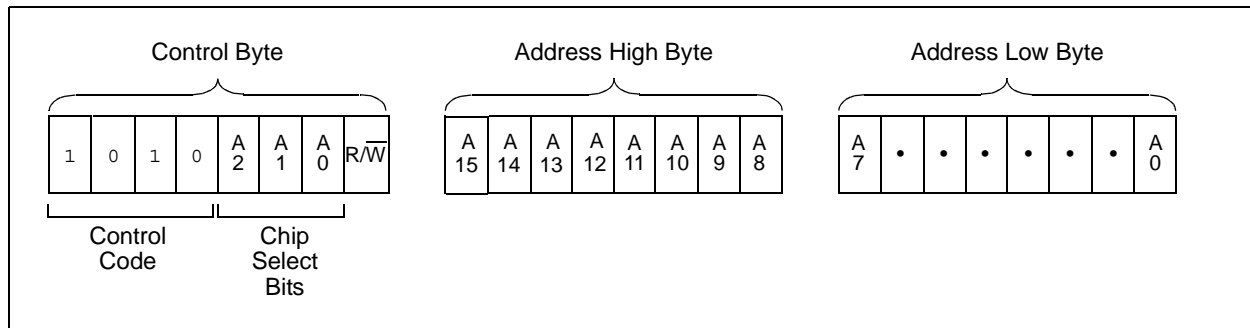
FIGURE 5-1: CONTROL BYTE FORMAT



5.1 Contiguous Addressing Across Multiple Devices

The Chip Select bits A2, A1 and A0 can be used to expand the contiguous address space for up to 4 Mbit by adding up to eight 24XX512 devices on the same bus. In this case, software can use A0 of the **control byte** as address bit A16; A1 as address bit A17; and A2 as address bit A18. It is not possible to sequentially read across device boundaries.

FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



6.0 WRITE OPERATIONS

6.1 Byte Write

Following the Start condition from the master, the control code (four bits), the Chip Select (three bits) and the R/\overline{W} bit (which is a logic low) are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that the address high byte will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the high-order byte of the word address and will be written into the Address Pointer of the 24XX512. The next byte is the Least Significant Address Byte. After receiving another Acknowledge signal from the 24XX512, the master device will transmit the data word to be written into the addressed memory location. The 24XX512 acknowledges again and the master generates a Stop condition. This initiates the internal write cycle and during this time, the 24XX512 will not generate Acknowledge signals (Figure 6-1). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written and the device will immediately accept a new command. After a byte Write command, the internal address counter will point to the address location following the one that was just written.

6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24XX512 in the same way as in a byte write. But instead of generating a Stop condition, the master transmits up to 127 additional bytes, which are temporarily stored in the on-chip page buffer and will be written into memory after the master has transmitted a Stop condition. After receipt of each word, the seven lower Address Pointer bits are internally incremented by one. If the master should transmit more than 128 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written and the device will immediately accept a new command.

6.3 Write Protection

The WP pin allows the user to write-protect the entire array (0000-FFFF) when the pin is tied to Vcc. If tied to Vss the write protection is disabled. The WP pin is sampled at the Stop bit for every Write command (Figure 1-1). Toggling the WP pin after the Stop bit will have no effect on the execution of the write cycle.

Note: Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size - 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

24AA512/24LC512/24FC512

FIGURE 6-1: BYTE WRITE

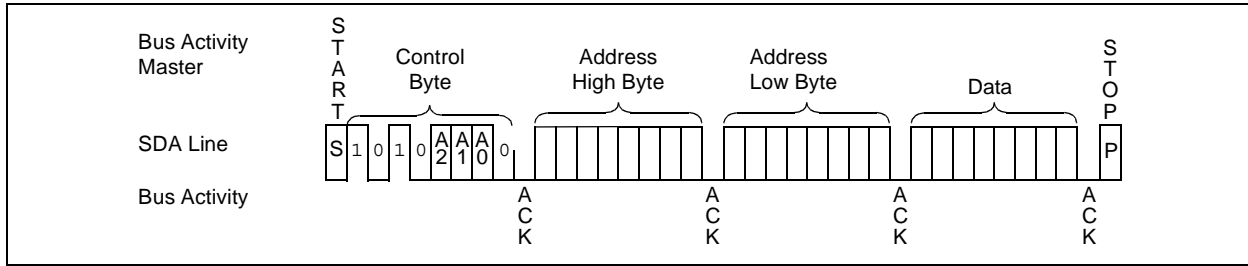
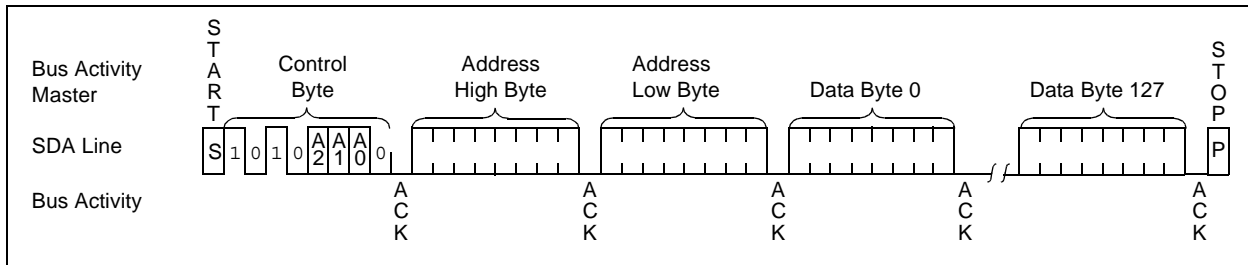


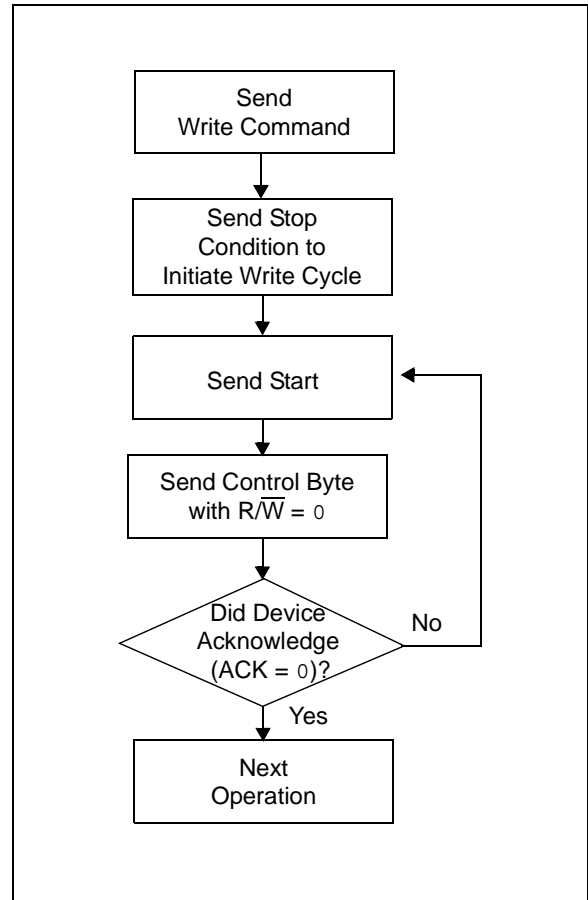
FIGURE 6-2: PAGE WRITE



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition, followed by the control byte for a Write command ($R/\bar{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the Start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



24AA512/24LC512/24FC512

8.0 READ OPERATION

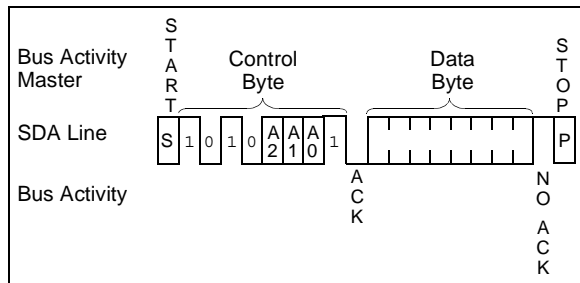
Read operations are initiated in the same way as write operations with the exception that the R/\overline{W} bit of the control byte is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 24XX512 contains an address counter that maintains the address of the last word accessed, internally incremented by '1'. Therefore, if the previous read access was to address 'n' (n is any legal address), the next current address read operation would access data from address $n + 1$.

Upon receipt of the control byte with R/\overline{W} bit set to '1', the 24XX512 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the 24XX512 discontinues transmission (Figure 8-1).

FIGURE 8-1: CURRENT ADDRESS READ



8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24XX512 as part of a write operation (R/\overline{W} bit set to '0'). After the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. Then, the master issues the control byte again but with the R/\overline{W} bit set to a one. The 24XX512 will then issue an acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer but does generate a Stop condition which causes the 24XX512 to discontinue transmission (Figure 8-2). After a random Read command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24XX512 transmits the first data byte, the master issues an acknowledge as opposed to the Stop condition used in a random read. This acknowledge directs the 24XX512 to transmit the next sequentially addressed 8-bit word (Figure 8-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge, but will generate a Stop condition. To provide sequential reads, the 24XX512 contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation. The internal Address Pointer will automatically roll over from address FFFF to address 0000 if the master acknowledges the byte received from the array address FFFF.

24AA512/24LC512/24FC512

FIGURE 8-2: RANDOM READ

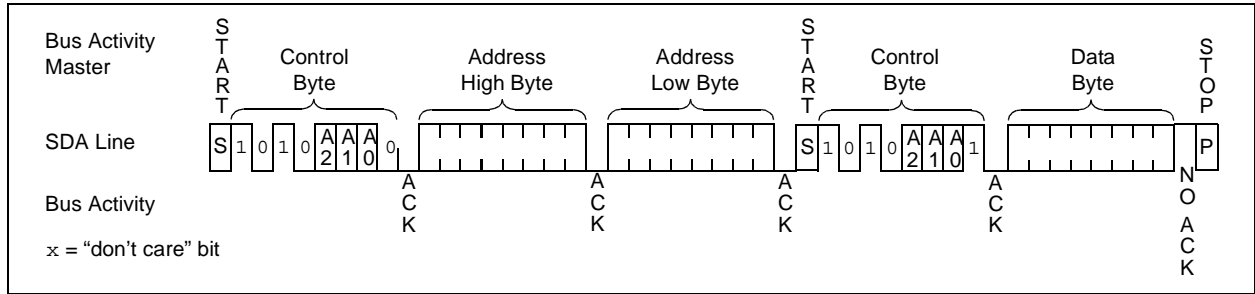
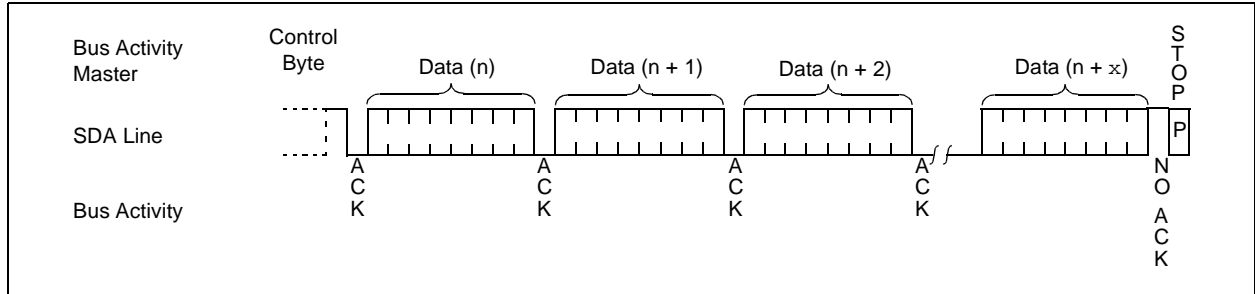


FIGURE 8-3: SEQUENTIAL READ

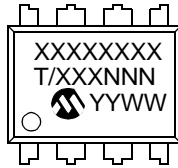


24AA512/24LC512/24FC512

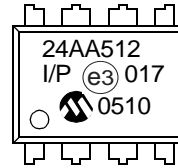
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

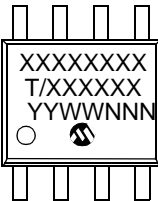
8-Lead PDIP (300 mil)



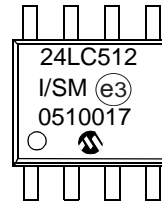
Example:



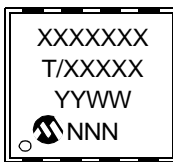
8-Lead SOIC (208 mil)



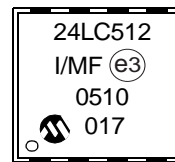
Example:



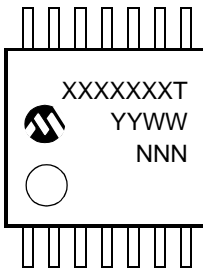
8-Lead DFN-S



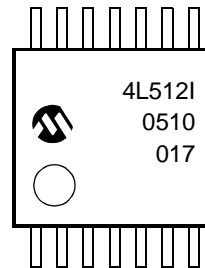
Example:



14-Lead TSSOP



Example:

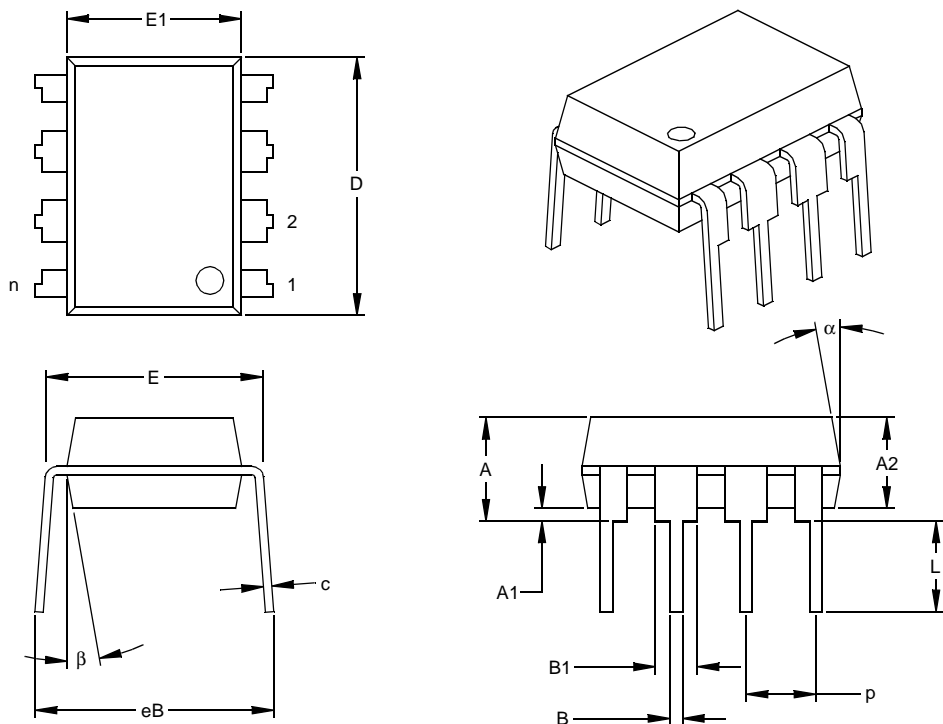


Legend:	XX...X	Customer-specific information*
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	T	Temperature
	Blank	Commercial
	I	Industrial
	E	Extended
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

*Standard device marking consists of Microchip part number, year code, week code, and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

24AA512/24LC512/24FC512

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

Notes:

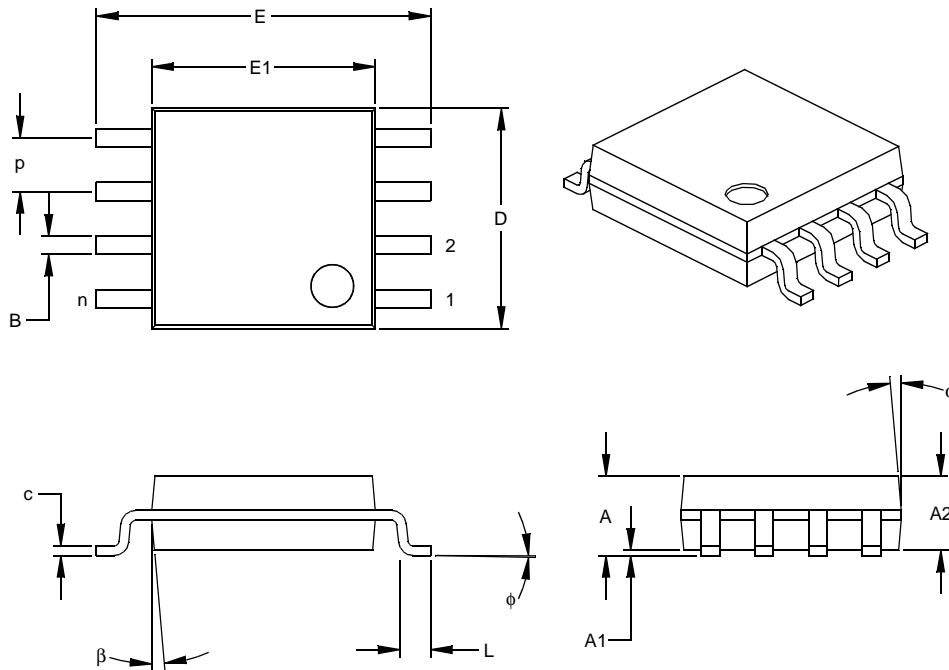
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-018

24AA512/24LC512/24FC512

8-Lead Plastic Small Outline (SM) – Medium, 208 mil (SOIC)



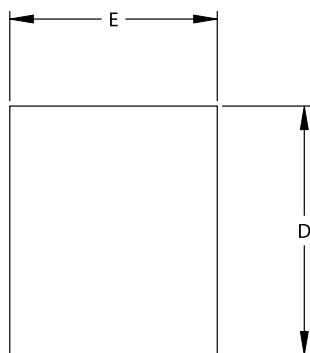
Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.070	.075	.080	1.78	1.97	2.03
Molded Package Thickness	A2	.069	.074	.078	1.75	1.88	1.98
Standoff §	A1	.002	.005	.010	0.05	0.13	0.25
Overall Width	E	.300	.313	.325	7.62	7.95	8.26
Molded Package Width	E1	.201	.208	.212	5.11	5.28	5.38
Overall Length	D	.202	.205	.210	5.13	5.21	5.33
Foot Length	L	.020	.025	.030	0.51	0.64	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.43	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
 § Significant Characteristic

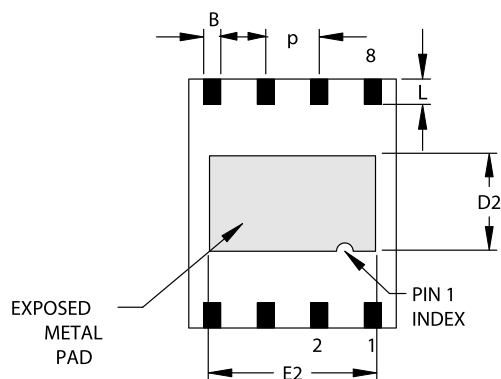
Notes:
 Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
 Drawing No. C04-056

24AA512/24LC512/24FC512

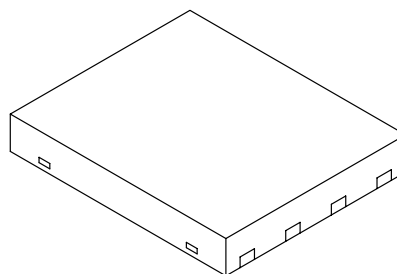
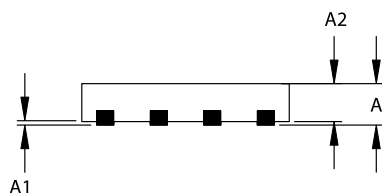
8-Lead Plastic Dual Flat No Lead Package (MF) 6x5 mm Body (DFN-S) – Saw Singulated



TOP VIEW



BOTTOM VIEW



Dimension Limits	Units	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p	.050 BSC			1.27 BSC		
Overall Height	A	.033	.035	.037	0.85	0.90	0.95
Package Thickness	A2	.031	.035	.037	0.80	0.89	0.95
Standoff	A1	.000	.0004	.002	0.00	0.01	0.05
Base Thickness	A3	.007	.008	.009	0.17	0.20	0.23
Overall Length	E	.195	.197	.199	4.95	5.00	5.05
Exposed Pad Length	E2	.152	.157	.163	3.85	4.00	4.15
Overall Width	D	.234	.236	.238	5.95	6.00	6.05
Exposed Pad Width	D2	.089	.091	.093	2.25	2.30	2.35
Lead Width	B	.014	.016	.019	0.35	0.40	0.47
Lead Length	L	.024		.026	0.60		0.65

Notes:

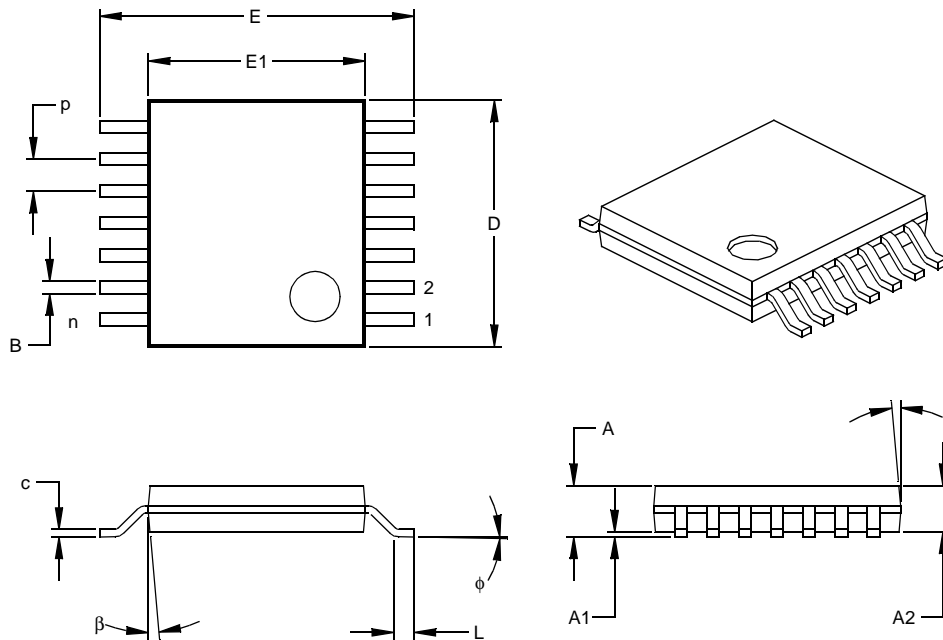
JEDEC equivalent: MO-220

Drawing No. C04-122

Revised 11/3/03

24AA512/24LC512/24FC512

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Dimension Limits	Units	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
 § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEDEC Equivalent: MO-153

Drawing No. C04-087

APPENDIX A: REVISION HISTORY

Revision D

Correction to Section 1.0, Electrical Characteristics.

Revision E

Correction to Section 1.0., Ambient Temperature

Correction to Section 6.2, Page Write

Revision F

Add E3 (Pb-free) to marking examples.

Updated Marking Legend and On-line Support.

Revision G

Revised Sections 2.1, 2.4 and 6.3.

24AA512/24LC512/24FC512

NOTES:

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com, click on Customer Change Notification and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: <http://support.microchip.com>

24AA512/24LC512/24FC512

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To: Technical Publications Manager
RE: Reader Response
From: Name _____
Company _____
Address _____
City / State / ZIP / Country _____
Telephone: (_____) _____ - _____ FAX: (_____) _____ - _____

Application (optional):

Would you like a reply? ___Y ___N

Device: 24AA512/24LC512/24FC512 Literature Number: DS21754G

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

24AA512/24LC512/24FC512

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	<u>X</u>	Examples:
Device	Temperature Range	Package	Lead Finish	
Device:	24AA512:	512 Kbit 1.8V I ² C Serial EEPROM		a) 24AA512-I/P: Industrial Temp., 1.8V, PDIP package.
	24AA512T:	512 Kbit 1.8V I ² C Serial EEPROM (Tape and Reel)		b) 24AA512T-I/SM: Tape and Reel, Industrial Temp., 1.8V, SOIC package.
	24LC512:	512 Kbit 2.5V I ² C Serial EEPROM		c) 24AA512-I/ST14: Industrial Temp., 1.8V, 14-lead, TSSOP package.
	24LC512T:	512 Kbit 2.5V I ² C Serial EEPROM (Tape and Reel)		d) 24AA512-I/MF: Industrial Temp., 1.8V, DFN package.
	24FC512:	512 Kbit 1 MHz I ² C Serial EEPROM		e) 24LC512-E/P: Extended Temp., 2.5V, PDIP package.
	24FC512T:	512 Kbit 1 MHz I ² C Serial EEPROM (Tape and Reel)		f) 24LC512-I/SM: Industrial Temp., 2.5V, SOIC package.
Temperature Range:	I	= -40°C to +85°C		g) 24LC512T-I/SM: Tape and Reel, Industrial Temp., 2.5V, SOIC package.
	E	= -40°C to +125°C		h) 24LC512-I/MF: Industrial Temp., 2.5V, DFN package.
Package:	P	= Plastic DIP (300 mil body), 8-lead		i) 24FC512-I/P: Industrial Temp., 2.5V, High Speed, PDIP package.
	SM	= Plastic SOIC (208 mil body), 8-lead		j) 24FC512-I/SM: Industrial Temp., 2.5V, High Speed, SOIC package.
	ST14	= Plastic TSSOP (4.4 mm), 14-lead		k) 24FC512T-I/SM: Tape and Reel, Industrial Temp., 2.5V, High Speed, SOIC package.
	MF	= Micro Lead Frame (6x5 mm body), 8-lead		l) 24LC512T-I/SM: Industrial Temp., 2.5V, SOIC package, Tape & Reel, Pb-free
Lead Finish:	Blank	= Pb-free – Matte Tin (see Note 1)		m) 24LC512-I/PG: Industrial Temp., 2.5V, PDIP package, Pb-free
	G	= Pb-free – Matte Tin only		

Note 1: Most products manufactured after January 2005 will have a Matte Tin (Pb-free) finish. Most products manufactured before January 2005 will have a finish of approximately 63% Sn and 37% Pb (Sn/Pb). Please visit www.microchip.com for the latest information on Pb-free conversion, including conversion date codes.

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

24AA512/24LC512/24FC512

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, microID, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, PowerSmart, rPIC, and SmartShunt are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.


AmpLab, FilterLab, Migratable Memory, MXDEV, MXLAB, PICMASTER, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, dsPICDEM, dsPICDEM.net, dsPICworks, ECAN, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, Linear Active Thermistor, MPASM, MPLIB, MPLINK, MPSIM, PCKIT, PICDEM, PICDEM.net, PICLAB, PICtail, PowerCal, PowerInfo, PowerMate, PowerTool, rLAB, rPICDEM, Select Mode, Smart Serial, SmartTel, Total Endurance and WiperLock are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2005, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

**QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949:2002 ==**

Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://support.microchip.com>
Web Address:
www.microchip.com

Atlanta
Alpharetta, GA
Tel: 770-640-0034
Fax: 770-640-0307

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

San Jose
Mountain View, CA
Tel: 650-215-1444
Fax: 650-961-0286

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8676-6200
Fax: 86-28-8676-6599

China - Fuzhou
Tel: 86-591-8750-3506
Fax: 86-591-8750-3521

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Shunde
Tel: 86-757-2839-5507
Fax: 86-757-2839-5571

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7250
Fax: 86-29-8833-7256

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-2229-0061
Fax: 91-80-2229-0062

India - New Delhi
Tel: 91-11-5160-8631
Fax: 91-11-5160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471-6166
Fax: 81-45-471-6122

Korea - Gumi
Tel: 82-54-473-4301
Fax: 82-54-473-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Penang
Tel: 604-646-8870
Fax: 604-646-5086

Philippines - Manila
Tel: 632-634-9065
Fax: 632-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-572-9526
Fax: 886-3-572-6459

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Weis
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-352-30-52
Fax: 34-91-352-11-47

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820