ANALOG DEVICES

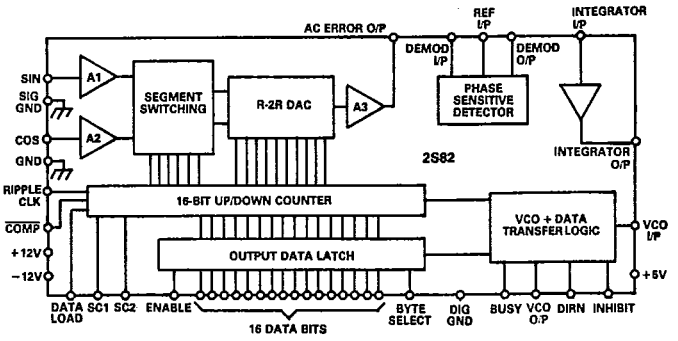
Variable Resolution, Monolithic Resolver-to-Digital Converter

T-71-35-03 **2S82**

FEATURES
Monolithic (BiMOS II) Tracking R/D Converter
44-Pin J Leaded Chip Carrier (LCC)
10-, 12-, 14- and 16-Bit Resolution Set by User
Ratiometric Conversion
Low Power Consumption – 300mW typ
Dynamic Performance Set by User
High max Tracking Rate 1040 rps (10 Bits)
Velocity Output
VCO Output (Inter LSB Output)
Data Complement Facility
Military Temperature Range Version

APPLICATIONS
Brushless Motor Control
Process Control
Numerical Control of Machine Tools
Robotics
Axis Control

2S82 FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The 2S82 is a monolithic 10-, 12-, 14- or 16-bit tracking resolver-to-digital converter contained in a 44-pin J leaded chip carrier package. Two extra functions are provided in the new surface mount package – COMPLEMENT and VCO OUTPUT. All other functions are identical to the 2S80.

The converter allows users to select their own resolution and dynamic performance with external components. This allows the users great flexibility in defining the converter that best suits their system requirements. The converter allows users to select the resolution to be 10, 12, 14 or 16 bits and to track resolver signals rotating at up to 1040 revs per second (62,400 rpm) when set to 10-bit resolution.

The 2S82 converts resolver format input signals into a parallel natural binary digital word using a ratiometric tracking conversion method. This ensures high noise immunity and tolerance of lead length when the converter is remote from the resolver.

The 10-, 12-, 14- or 16-bit output word is tristate available in two bytes on the 16 output data lines. BYTE SELECT, ENABLE and INHIBIT pins ensure easy data transfer to 8- and 16-bit data buses, and outputs are provided to allow for cycle or pitch counting in external counters.

An analog signal proportional to velocity is also available.

Reference frequency operating range for the 2S82 is 50Hz to 20,000Hz.

PRODUCT HIGHLIGHTS

Monolithic. A one-chip surface mount package solution reduces the package size required and increases reliability.

Resolution Set by User. Two control pins are used to select the resolution of the 2S82 to be 10, 12, 14 or 16 bits allowing the user to use the 2S82 with optimum resolution for each application.

Ratiometric Tracking Conversion. Conversion technique provides continuous output position data without conversion delay and is insensitive to absolute signal levels. It also provides good noise immunity and a tolerance to harmonic distortion on the reference and input signals.

Dynamic Performance Set by the User. By selecting external resistor and capacitor values, the user can determine bandwidth, maximum tracking rate and velocity scaling of the converter to match the system requirements. The external components required are all low cost, preferred value resistors and capacitors, and the component values are easy to select using the simple instructions given.

Velocity Output. An analog signal proportional to velocity is available and is linear to typically one percent. This can be used in place of a velocity transducer in many applications to provide loop stabilization and velocity feedback data.

Low Power Consumption. Typically only 300mW.

ORDERING INFORMATION

Model	Accuracy (Arc mins)	Operating Temperature Range	Package Options
2S82HP	22 + 1LSB	0 to +70°C	Plastic LCC
2S82JP	8 + 1LSB	0 to +70°C	Plastic LCC
2S82KP	4 + 1LSB	0 to +70°C	Plastic LCC
2S82LP	2 + 1LSB	0 to +70°C	Plastic LCC

SPECIFICATIONS (typical at 25°C unless otherwise specified)

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Model	2S82	Units	Notes
TYPICAL CONVERTER PERFORMANCE (Connected as shown in Figure 1)			
Resolution	10, 12, 14 or 16	bits	
Accuracy HP Option	±22 + 1LSB	arc mins	Accuracy will be affected by the offset at the INTEGRATOR I/P.
JP Option	±8 + 1LSB	arc mins	
KP Option	±4 + 1LSB	arc mins	
LP Option	±2 + 1LSB	arc mins	
Tracking Rate Range			
10-Bit Resolution	0 to 1040	rps	User Selected, max rate limited to 1/16 of the reference frequency.
12-Bit Resolution	0 to 260	rps	
14-Bit Resolution	0 to 65	rps	
16-Bit Resolution	0 to 16.25	rps	
Operating Frequency Range	50 to 20,000	Hz	
Repeatability of Position Output	1	LSB	
Bandwidth	User Selectable		
Velocity Signal			See "Using the Velocity Signal."
Linearity			
Over Full Range	±1	% of output	See VCO spec.
Reversion Error	±1	%	With power supplies adjusted for best performance.
Zero Offset	+6	mV	For max tracking rate range. Depends on VCO I/P resistor (R6).
Zero Offset Tempco	−22	µV/°C	For max tracking rate range. Depends on VCO I/P resistor (R6).
Gain Scaling Accuracy	±10	% FSD	
Output Voltage	±8	V dc	
Noise and Ripple			
at LSB Rate	2	mV	See section "Using the Velocity Output."
Dynamic Ripple (Peak)	1.5	% of mean output	
ANALOG INPUTS			
Protection	All analog inputs are diode protected against overvoltage at ±8V.		
REFERENCE INPUT			
Frequency	50–20,000	Hz	
Voltage Level Nominal	2	V rms	
Max	11	V peak	
Input Bias Current	60 (typ), 150 (max)	nA	
Input Impedance	>1	MΩ	
SIGNAL INPUTS (SIN, COS)			
Frequency	50–20,000	Hz	
Allowable Phase Shift (Signal to Reference)	10	Degrees	
Voltage Level	2, ±10%	V rms	
Input Bias Current	60 (typ), 150 (max)	nA	
Input Impedance	>1	MΩ	
Maximum Voltage Nominal	±8	V	
DIGITAL INPUTS	TTL Compatible		Except DATA LOAD and SHORT CYCLE INPUTS.
INHIBIT			
Sense	Logic LO to inhibit		See section "INHIBIT Input."
Time to Data Stable (After Negative Going Edge of INHIBIT)	600	ns	
DATA LOAD			
Sense	Internally pulled up to +12V. Unconnected for normal operation. Logic LO allows data to be loaded into the counters from the data lines.		Connect when multiplexing the 2S82 or when using as a control transformer. Ensure data lines are in high impedance state when loading data.
SHORT CYCLE INPUTS (SC1, SC2)			Internally pulled up to $+V_S$. Used to select the resolution of the converter. 0 = Digital Ground. Drive low with open collector TTL. 1 = Open Circuit (internally pulled up through 100kΩ).
	SC1	SC2	
For 10-Bit Resolution	0	0	
For 12-Bit Resolution	0	1	
For 14-Bit Resolution	1	0	
For 16-Bit Resolution	1	1	
BYTE SELECT			
Sense Logic HI	8 MSBs selected on data lines 1 to 8. LS Byte selected on data lines 9 to 16.		The size of the LS Byte will be between 2 and 8 bits depending on the resolution selected.
Logic LO	LS Byte selected on data lines 1 to 8 and 9 to 16.		
Time to Data Available (After Change in State)	150 (typ), 450 (max)		ns

Model	2S82	Units	Notes
COMPLEMENT	Internally pulled up to +12V. Unconnected for normal operation. Logic LO to activate.		
ENABLE			
Sense	Logic LO to enable position outputs. Logic HI position outputs in high impedance state.		
Enable and Disable Times	200 (typ), 550 (max)	ns	
ANALOG OUTPUTS			
Protection	Short-circuit output current limited to ±8mA, ±30%.		
Output Voltage Range, typ	+9 to −9	V	With 1mA load.
max	+10.5 to −10.5	V	
min	+8 to −8	V	
DIGITAL OUTPUTS			
Format	V_L = +5V	TTL Compatible	Voltage on V_L sets the voltage level of the digital outputs.
	V_L = +12V	CMOS Compatible	
POSITION OUTPUTS			
Format	Three-state natural binary		
Resolution	10, 12, 14 or 16	bits	
Number of Data Lines	16		
Max Load	3	LSTTL	
Monotonicity			
HP, JP, KP Options	Guaranteed to 14 bits		
LP Option	Guaranteed to 16 bits		
DIRECTION			
Sense	Logic HI when counting up. Logic LO when counting down.		
Timing	Only changes, if required, at start of output position data cycle.		
Max Load	3	LSTTL	
RIPPLE CLOCK			
Sense	Positive going edge when counting up from all "1s" and when counting down from all "0s" as data changes.		
Timing	Edge occurs at least 300ns before change in DIR can occur.		
Width	300 (min)	ns	
Reset	By start of next data update.		
Max Load	3	LSTTL	
BUSY			
Sense	Logic HI when converter position output changing.		
Timing	Positive going edge 50ns before change in position output.		
Width typ	300	ns	
min	200	ns	
max	600	ns	
Max Load	3	LSTTL	See Section "BUSY Output."
POWER SUPPLIES			The 2S82 may latch up if $+V_S$ is applied without $-V_S$.
Voltage Levels			
$+V_S$	+12 ±10%	V	
$-V_S$	−12 ±10%	V	
$+V_L$	+5 to +14	V	
Current			Over operating temperature range.
$+V_S$, $-V_S$ at 12V	12 (typ), 23 (max)	mA	
$+V_S$, $-V_S$ at 13.2V	19 (typ), 30 (max)	mA	
$+V_L$	0.5 (typ), 1.5 (max)	mA	
GENERAL			
Operating Temperature Range HP, JP, KP, LP Options	0 to +70	°C	
Storage Temperature Range (All Options)	−25 to +85	°C	
Weight	0.2 (5)	oz (grams)	
VCO OUTPUT	±3 (±10%)	V/LSB	The VCO output swings between ±3V depending on the resolver direction.

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CONVERTER CHARACTERISTICS

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Model	2S82	Units	Notes
RATIO MULTIPLIER			
Function	AC ERROR output represents the difference between the angle at the SIN and COS inputs compared to the position output angle.		
AC ERROR Output Scaling			
10-Bit Resolution	177.6	mV/bit	
12-Bit Resolution	44.4	mV/bit	
14-Bit Resolution	11.1	mV/bit	
16-Bit Resolution	2.775	mV/bit	
Accuracy			Maximum over temp. range.
HP Option	±22	arc mins	
JP Option	±8	arc mins	
KP Option	±4	arc mins	
LP Option	±2	arc mins	
Differential Nonlinearity			
HP, JP, KP Options	<1	Bits in 14	Guaranteed monotonic to 14 bits when connected in tracking mode.
LP Option	<1	Bits in 16	Guaranteed monotonic to 16 bits when connected in tracking mode.
PHASE SENSITIVE DETECTOR			Specified over operating frequency range. Tested at 1kHz.
Output Offset Voltage	12 (max)	mV	
Gain of Signal (dc Out, rms In)			
In Phase w.r.t. Reference	−0.9 ±2%		
In Quadrature w.r.t. Reference	±0.02 (max)		
Input Bias Current	60 (typ), 150 (max)	nA	
Input Impedance	>1	MΩ	
Input Voltage Range	+8 to −8	V	
INTEGRATOR			
Open Loop Gain at 10kHz	60 ±3	dB	
Dead Zone Current	100	nA/LSB	See section "Integrator."
Input Offset Voltage	1 (typ), 5 (max)	mV	
Input Bias Current	60 (typ), 150 (max)	nA	
Output Voltage Range (min)	+8 to −8	V	
Input Impedance	>1	MΩ	
Input Voltage Range	+8 to −8	V	
VCO			
Maximum Rate	1.1	MHz	
VCO Rate	7.4 ± 10%	kHz/μA	With ±12V supplies.
VCO Rate Tempco	−0.05	%/°C	
Input Offset Voltage	1 (typ), 5 (max)	mV	
Input Bias Current	120 (typ), 300 (max)	nA	
Input Bias Current Tempco	−0.55	nA/°C	
Input Voltage Range	−8 to +8	V	
Linearity of Absolute Rate			
Over Full Range	±1 (typ), ±3 (max)	%	
Over 0 to 50% of Max Range	+1 (max)	%	
Reversion Error	<3 (max)	%	Symmetrical power supplies.
Sensitivity of Reversion Error to Symmetry of Power Supplies	8	%/V of Asymmetry	See section "Using the Velocity Output."

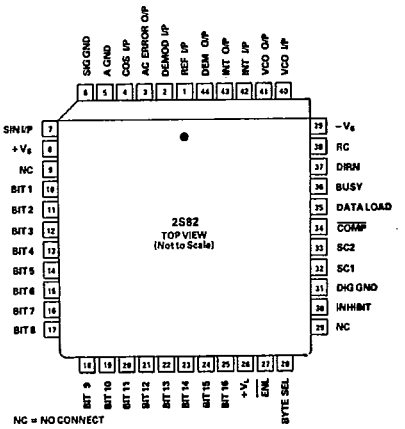
Specifications subject to change without notice.

ABSOLUTE MAXIMUM INPUTS (with respect to GND)

$+V_S$[1]	0V to +14V dc
$-V_S$	0V to −14V dc
$+V_L$	0V to $+V_S$
Reference	+14V to $-V_S$
Sin	+14V to $-V_S$
Cos	+14V to $-V_S$
Any Logical Input	−0.4V to $+V_L$ dc
Demodulator Input	+14V to $-V_S$
Integrator Input	+14V to $-V_S$
VCO Input	+14V to $-V_S$

NOTE
[1]**CAUTION** – Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.

PIN CONFIGURATION



OPERATION OF THE CONVERTER

When connected in a circuit such as is shown in Figure 1, the 2S82 operates as a tracking resolver-to-digital converter and forms a type 2 closed loop system. This means that the output will automatically follow the input for speeds up to the selected maximum tracking rate. No convert command is necessary as the conversion is initiated by each LSB increment of the input. Each LSB increment of the converter initiates a BUSY pulse.

Because the conversion depends on the ratio of the input signals, the 2S82 is remarkably tolerant of input amplitude and frequency (there is no need of an accurate, stable oscillator to produce the reference signal). The inclusion of a phase sensitive detector in the conversion loop ensures a high immunity to signals that are not coherent or are in quadrature with the reference signal.

Two major areas of the 2S82 specification can be selected by the user to optimize the total system performance. The resolution of the digital output is set by the state of the inputs SC1 and SC2 to be 10, 12, 14 or 16 bits, and the dynamic characteristics of bandwidth and tracking rate are selected by the choice of external components.

Position Output

The resolver shaft position is represented at the converter output by a natural binary parallel digital word.

As the digital output of the converter passes through the major carries, i.e., all "1s" to all "0s" or the converse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

The direction of input rotation is indicated by the DIRECTION (DIR) logic output. This direction data is always valid in advance of a RIPPLE CLOCK pulse and, as it is internally latched, only changes with a change in direction.

Both the RIPPLE CLOCK pulse and the DIRECTION data are unaffected by the application of the INHIBIT.

The static accuracy quoted is the worst case error that can occur over the full operating temperature excluding the effect of offset signals at the INTEGRATOR INPUT (which can be trimmed out) and with the following conditions: input signal amplitudes are within 5% of the nominal values; signal and reference frequency is within the specified operating range; phase shift between signal and reference is less than 10 degrees; signal and reference waveform harmonic distortion is less than 10%.

These test conditions are selected primarily to establish a repeatable acceptance test procedure which can be traced to national standards. In practice, the 2S82 can be used well outside these operating conditions providing the following points are observed.

Signal Amplitude (Sine and Cosine Inputs)

The amplitude of the signal inputs should be maintained within 5% of the nominal values if full performance is required from the velocity signal.

The digital position output is relatively insensitive to amplitude variation. Increasing the input signal levels by more than 10% will result in a dramatic loss in accuracy due to internal overload. Reducing level will result in a steady decline in accuracy. With the signal levels at 50% of the correct value, the angular error will increase to an amount equivalent to 1.3LSB. At this level the repeatability will also degrade to 2LSB and the dynamic response will also change, since the dynamic characteristics are proportional to the signal level.

The 2S82 will not be damaged if the signal inputs are applied to the converter without the power supplies and/or the reference.

Reference Voltage Level

The amplitude of the reference signal applied to the converter's input is not critical, but care should be taken to ensure it is kept below the absolute maximum voltage.

The 2S82 will not be damaged if the reference is supplied to the converter without the power supplies and/or the signal inputs.

Harmonic Distortion

The amount of harmonic distortion allowable on the signal and reference lines mainly depends on the type of transducer being used.

Square waveforms can be used but the input levels should be adjusted so that the average value is 1.9V rms. (For example, a square wave should be 1.9V peak.)

Note: The figure specified of 10% harmonic distortion is for calibration convenience only.

Velocity Signal

The tracking converter technique generates an internal signal at the output of the integrator (the INTEGRATOR OUTPUT pin) that is proportional to the rate of change of the input angle. This is a dc analog output referred to as the VELOCITY signal.

DC Error Signal

The signal at the output of the phase sensitive detector (DEMODULATOR OUTPUT) is the signal to be nulled by the tracking loop and is therefore proportional to the error between the input angle and the output digital angle. This is the DC ERROR of the converter; and as the converter is a type 2 servo loop, it will increase if the output fails to track the input for any reason. It is an indication that the input has exceeded the maximum tracking rate of the converter or, due to some internal malfunction, the converter is unable to reach a null. By connecting two external comparators, this voltage can be used as a "built-in test."

CONNECTING THE CONVERTER

The power supply voltages connected to $+V_S$ and $-V_S$ pins should be $\pm 12V$ and must not be reversed. If one rail is connected without the other, the converter will not operate and may "latch up." In this case, the removal of both rails is necessary in order for the converter to function correctly again. The voltage applied to V_L can be $+5V$ to $+V_S$.

It is suggested that decoupling capacitors are connected in parallel between the power lines $+V_S$, $-V_S$ and ANALOG GROUND adjacent to the converter. Suggested values of 100nF (ceramic) and 10μF (tantalum). Decoupling capacitors of 100nF and 10μF should also be connected between $+V_L$ and DIGITAL GROUND adjacent to the converter.

When more than one converter is used on a card, then separate decoupling capacitors should be used for each converter.

The resolver connections should be made to the SIN and COS inputs, REFERENCE INPUT and SIGNAL GROUND as shown in Figure 7 and described in section "CONNECTING THE RESOLVER". The two signal ground wires from the

resolver should be joined at the SIGNAL GROUND pin of the converter to minimize the coupling between the sine and cosine signals. For this reason it is also recommended that the resolver is connected using twisted pair cables with the sine, cosine and reference signals twisted separately.

SIGNAL GROUND and ANALOG GROUND are connected internally. ANALOG GROUND and DIGITAL GROUND must be connected externally.

The external components required should be connected as shown in Figure 1.

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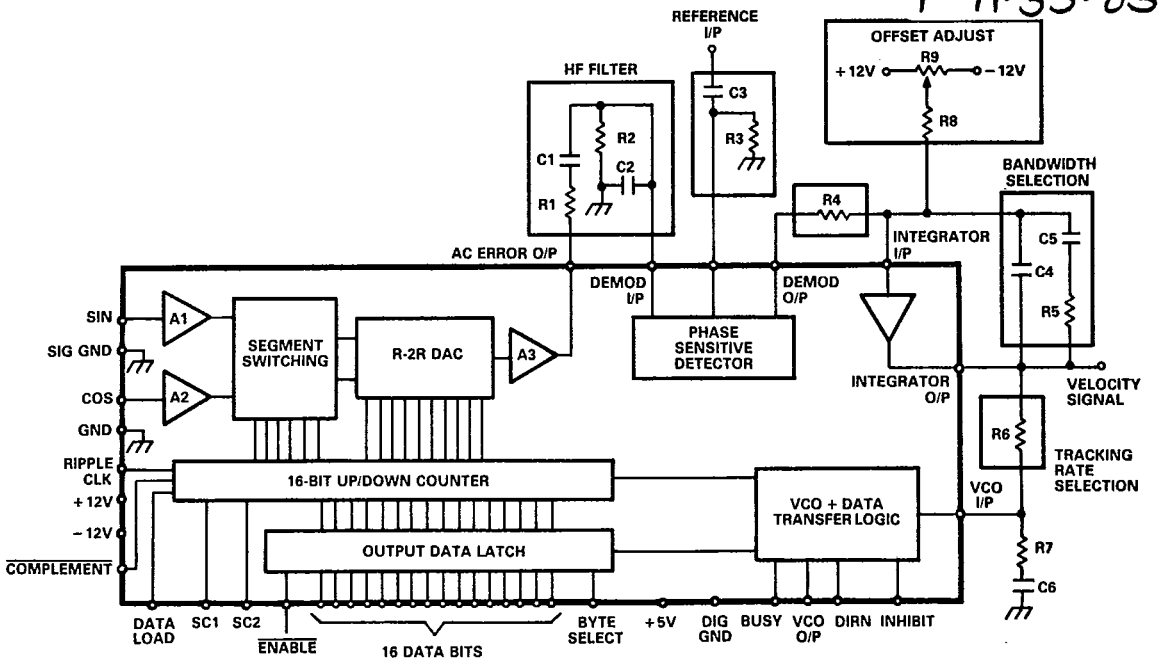

Figure 1. 2S82 Connection Diagram

SELECTING THE RESOLUTION

The resolution of the 2S82 can be selected to be 10, 12, 14 or 16 bits by use of the short cycling inputs SC1 and SC2. The required resolution can be selected as shown in the specification section.

The choice of resolution will affect the values of R4 and R6 which scale the inputs to the integrator and the VCO respectively (see section "COMPONENT SELECTION"). If the resolution is changed, then new values of R4 and R6 must be switched into the circuit.

Note: When changing resolution under dynamic conditions, a period of uncertainty will exist before position and velocity data is valid.

COMPONENT SELECTION

The following instructions describe how to select the external components to the converter in order to achieve the required bandwidth and tracking rate. In all cases the nearest "preferred value" component should be used and a 5% tolerance will not degrade the overall performance of the converter. Care should be taken that the resistors and capacitors will function over the required operating temperature range. The components should be connected as shown in Figure 1.

For more detailed information and explanation, see section "CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE."

1. HF Filter (R1, R2, C1, C2)
   The function of the HF filter is to reduce the amount of noise present on the signal inputs to the 2S82, reaching the Phase Sensitive Detector and affecting the outputs. R1 and C2 may be omitted – in which case R2 = R3 and C1 = C3, calculated below – but their use is particularly recommended if noise from a switch mode motor drive is present.

   Values should be chosen so that

   $$R1 = R2 \leq 56k\Omega$$

   $$C1 = C2 = \frac{1}{2\pi\, R1\, f_{REF}}$$

   and f_{REF} = reference frequency. (Hz)

   This filter gives an attenuation of 3 times at the input to the phase sensitive detector.

2. Gain Scaling Resistor (R4)
   If R1, C2 are fitted then:

   $$R4 = \frac{E_{DC}}{100 \times 10^{-9}} \times \frac{1}{3}\,\Omega$$

   If R1, C2 are not fitted then:

   $$R4 = \frac{E_{DC}}{100 \times 10^{-9}}\,\Omega$$

   where E_{DC} = 160×10^{-3} for 10 bits resolution
   = 40×10^{-3} for 12 bits
   = 10×10^{-3} for 14 bits
   = 2.5×10^{-3} for 16 bits
   = Scaling at the DC ERROR in volts

3. AC Coupling of Reference Input (R3, C3)
Select R3 and C3 so that there is no significant phase shift at the reference frequency. That is,

$$R3 = 100k\Omega$$

$$C3 > \frac{1}{10^5 \times f_{REF}}$$

4. Maximum Tracking Rate (R6)
The VCO input resistor R6 sets the maximum tracking rate of the converter and hence the velocity scaling as at the max tracking rate the velocity output will be 8V.

Decide on your required maximum tracking rate, "T," in revolutions per second. Note that "T" must not exceed the specified maximum tracking rate or 1/16 of the reference frequency.

$$R6 = \frac{5.92 \times 10^7}{T \times p}\ k\Omega$$

where p = bit per rev
= 1,024 for 10 bits resolution
= 4,096 for 12 bits
= 16,384 for 14 bits
= 65,536 for 16 bits

5. Closed Loop Bandwidth Selection (C4, C5, R5)
a. Choose the Closed Loop 3dB Bandwidth (f_{BW}) required ensuring that

$$f_{REF} > 2.5 \times f_{BW}$$

Typical values may be 100Hz for 400Hz reference frequency and 500 to 1000Hz for 5kHz reference frequency.

b. Select C4 so that

$$C4 = \frac{20.2 \times 10^{-3}}{R6 \times f_{BW}^2}$$

with R6 in kΩ and f_{BW} in Hz selected above.

c. C5 is given by

$$C5 = 5 \times C4$$

d. R5 is given by

$$R5 = \frac{4}{2 \times \pi \times f_{BW} \times C5}\ \Omega$$

6. VCO Phase Compensation
The following values of C6 and R7 should be fitted.

C6 = 470pF R7 = 68Ω

7. Offset Adjust
Offset and bias current at the integrator input can cause an additional positional offset at the output of the converter of 1 arc min typical, 5.3 arc mins maximum. If this can be tolerated, then R8 and R9 can be omitted from the circuit.

If fitted, the following values of R8 and R9 should be used: R8 = 4.7MΩ, R9 = 1MΩ potentiometer.

To adjust for zero offset, ensure the resolver is disconnected and all the other external components are fitted. Connect the COS pin to the REFERENCE INPUT and the SIN pin to the SIGNAL GROUND and with the power and reference applied, adjust the potentiometer to give all "0s" on the digital output bits.

The potentiometer may be replaced by select on test resistors if preferred.

PIN FUNCTIONS

REFERENCE I/P	Input pin for the reference signal.
DEMOD I/P	Demodulator input pin.
AC ERROR O/P	Output of ratio multiplier.
COS	Input pin for cosine signal from resolver.
ANALOG GROUND	Power ground.
SIGNAL GROUND	Ground pin for signals from resolver.
SIN	Input pin for sine signal from resolver.
$+V_S$	Main positive power supply.
BIT 1 – BIT 16	Parallel output data bits.
V_L	Logic power supply.
$\overline{\text{ENABLE}}$	Logic "HI" sets the output data bits to a high impedance state, a logic "LO" presents the data in the latches to the output pins.
BYTE SELECT	Selects the data output bits presented on data bits 1 to 8. Logic "HI" will present the 8 most significant bits; a logic "LO" will present the least significant byte.
INHIBIT	Logic "LO" inhibits the data transfer from the counter to the output latches.
DIGITAL GROUND	Ground pin for digital circuitry.
SC1, SC2	Logic inputs used for selecting the resolution of the converter.
DATA LOAD	Logic "LO" allows data to be loaded into the counters.
BUSY	Converter BUSY. A logic "HI" indicates that the output latches are being updated and data should not be transferred.
DIRECTION	Logic output indicating the direction of rotation of the input signals.
RIPPLE CLOCK	A negative going pulse whenever the output of the converter changes from all "1s" top all "0s" or the converse.
$-V_S$	Main negative power supply.
VCO I/P	Input pin to VCO.
INTEGRATOR I/P	Input pin of integrator.
INTEGRATOR O/P	Output pin of integrator.
DEMOD O/P	Output pin of demodulator.
$\overline{\text{COMPLEMENT}}$	Logic "LO" to activate
VCO O/P	Output pin of VCO.

DATA TRANSFER
Data transfer can be accomplished using either the INHIBIT input or the trailing edge of the BUSY pulse output.

INHIBIT Input:
The INHIBIT logic input only inhibits the data transfer from the internal up-down counter to the output latches and, therefore, does not interrupt the operation of the tracking loop. Releasing the INHIBIT automatically generates a BUSY pulse to refresh the output data.

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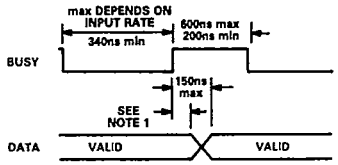
The output data is valid 350ns after the application of a logic "Lo" to the INHIBIT but the INHIBIT input must remain "Lo" for at least 600ns; otherwise the BUSY pulse generated by the logic "Lo" to "Hi" transition of the INHIBIT input may overlap the BUSY pulse that may have occurred at the time the INHIBIT is applied. The time required to assert the INHIBIT is 100ns.

BUSY Output:
The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses at TTL levels. A BUSY pulse is initiated each time the input moves by an analog equivalent of an LSB and the internal counter is incremented or decremented or the INHIBIT input is released.

Typically the width of the BUSY pulse is 350ns during the position data output updates. The trailing edge of the BUSY pulse indicates that the position data output has been updated and is ready for transfer. The maximum load on the BUSY output using the trailing edge of the BUSY pulse is 3 LSTTL loads.



NOTE 1
THE USE OF THE LEADING EDGE OF THE BUSY TO PREDICT DATA UPDATES IS ADVERSELY AFFECTED BY THE CAPACITIVE LOADING ON THE BUSY PULSE. TO ENSURE THAT THE LEADING EDGE OF THE BUSY PULSE OVERLAPS DATA TRANSITIONS, THE MAXIMUM LOAD ON BUSY OUTPUT SHOULD BE 15pF AND IT SHOULD BE PULLED UP TO −5 VOLT SUPPLY VIA A 5kΩ. THIS WILL RESTRICT THE MAXIMUM LOAD ON THE BUSY OUTPUT TO 1 LSTTL LOAD.

Figure 2. Timing Diagram

$\overline{\text{ENABLE}}$ Input:
The ENABLE input determines the state of the output data. A logic "Hi" maintains the output data pins in the high impedance condition, and application of a logic "Lo" presents the data in the latches to the output pins. The operation of the ENABLE has no effect on the conversion process.

BYTE SELECT Input:
The BYTE SELECT input selects the byte of position data to be presented at the data output Bits 1 to 8. The least significant byte will be presented on data output Bits 9 to 16 (with the ENABLE input taken to a logic "Lo") regardless of the state of the BYTE SELECT pin. Note that when the 2S82 is used with a resolution less than 16 bits the unused data lines are pulled to a logic "Lo." A logic "Hi" on the BYTE SELECT input will present the eight most significant data bits on data output Bits 1 and 8. A logic "Lo" will present the least significant byte on data outputs 1 to 8, i.e., data outputs 1 to 8 will duplicate data outputs 9 to 16.

The operation of the BYTE SELECT has no effect on the conversion process of the converter.

RIPPLE CLOCK Output:
As the output of the converter passes through the major carry, i.e., all "1s" to all "0s" or the converse, a positive going edge on the RIPPLE CLOCK (RC) output is initiated indicating that a revolution, or a pitch, of the input has been completed. The pulse has a minimum width of 300ns and is reset by the start of the next data update cycle.

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DIRECTION Output:
The DIRECTION (DIR) logic output indicates the direction of the input rotation, and this data is valid in advance of the RIPPLE CLOCK pulse and stays valid until the direction changes. This is the start of the next data update cycle – if the direction of rotation of the inputs has changed – and will be at least 300ns after the rising edge of the RIPPLE clock.

The DIR and RC outputs are unaffected by the state of the INHIBIT input.

$\overline{\text{COMPLEMENT}}$
The $\overline{\text{COMPLEMENT}}$ pin is internally pulled up to +12V in the INACTIVATE STATE. It is pulled down to DIGITAL GROUND (~100μA) to ACTIVATE.

When used in conjunction with the DATA LOAD pin, Strobing Data Load and $\overline{\text{COMPLEMENT}}$ pins "LOW" will set the logic "HIGH" bits of the 2S82 counter to a "LOW" state. Those bits of the applied data which are logic "LOW" will not change the corresponding bits in the 2S82 counter.

For example:

Initial Counter State	– – – 1 0 1 0 1 – – –
Applied Data Word	– – – 1 1 0 0 0 – – –
Counter State after Data Load Only	– – – 1 1 0 0 0 – – –
Initial Counter State	– – – 1 0 1 0 1 – – –
Applied Data Word	– – – 1 1 0 0 0 – – –
Counter State after Data Load and Complement	– – – 0 0 1 0 1 – – –

In order to read the output the following procedure should be followed:
1. Place outputs in high impedance state (ENABLE – "HIGH").
2. Present data to pins.
3. Pull DATA LOAD and COMPLEMENT pins to ground.
4. Wait 100ns.
5. Remove data from pins.
6. Remove outputs from high impedance state (ENABLE – "LOW").
7. Read Outputs.

CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE
The 2S82 allows the user great flexibility in choosing the dynamic characteristics of the resolver-to-digital conversion to ensure the optimum system performance. The characteristics are set by the external components shown in Figure 1, and the section "COMPONENT SELECTION" explains how to select desired maximum tracking rate and bandwidth values. The following paragraphs explain in greater detail the circuit of the 2S82 and the variations in the dynamic performance available to the user.

Loop Compensation
The 2S82 (connected as shown in Figure 1) behaves as a type 2 tracking servo loop where the VCO/counter combination and the integrator perform the two integration functions inherent in a type 2 loop.

Additional compensation in the form of a pole/zero pair is required to stabilize any type 2 loop to avoid the loop gain characteristic crossing the 0dB axis with 180° of additional phase lag, as shown in Figure 4. This compensation is implemented by the integrator components (R4, C4, R5, C5).

The overall response of such a system is that of a unity gain second order low pass filter, with the angle of the resolver as the input and the digital position data as the output.

The 2S82 does not have to be connected as tracking converter; parts of the circuit can be used independently. This is particularly true of the ratio multiplier which can be used as a control transformer.

A block diagram of the 2S82 is given in Figure 3.

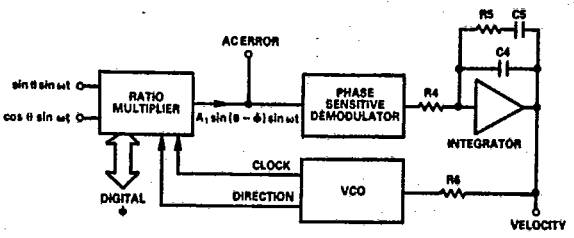

Figure 3. 2S82 Functional Diagram

Ratio Multiplier

The ratio multiplier is the input section of the 2S82 and compares the signal from the resolver inputs, θ, to the digital angle, φ, held in the counter. Any difference between these two angles results in an analog voltage at the AC ERROR OUTPUT. This circuit function has historically been called a "Control Transformer" as it was originally performed by a mechanical device known by that name.

The AC ERROR signal is given by

$$A1 \sin(\theta - \phi) \sin\omega t.$$

where $\omega = 2\pi f_{REF}$

f_{REF} = reference frequency

A1, the gain of the ratio multiplier stage is 14.5 times.

So for 2V rms inputs signals
AC ERROR output in volts/(bit of error)

$$= 2 \times \sin\left(\frac{360}{p}\right) \times A1$$

where p = bits per rev
- = 1,024 for 10 bits resolution
- = 4,096 for 12 bits
- = 16,384 for 14 bits
- = 65,536 for 16 bits

Giving AC ERROR output
- = 178mV rms/bit @ 10 bits resolution
- = 44.5mV rms/bit @ 12 bits
- = 11.125mV rms/bit @ 14 bits
- = 2.78mV rms/bit @ 16 bits.

The ratio multiplier will operate in exactly the same way whether the 2S82 is connected as a tracking converter or as a control transformer, where data is preset into the counters using the DATA LOAD pin.

HF Filter

The AC ERROR OUTPUT may be fed to the PSD via a simple ac coupling network (R2, C1) to remove any dc offset at this point. Note, however, that the PSD of the 2S82 is a wideband demodulator and is capable of aliasing HF noise down to within the loop bandwidth. This is most likely to happen where the resolver is situated in particularly noisy environments, and the user is advised to fit a simple HF filter R1, C2 prior to the phase sensitive demodulator.

The attenuation and frequency response of a filter will affect the loop gain and must be taken into account in deriving the loop transfer function. The suggested filter (R1, C1, R2, C2) is shown in Figure 1 and gives an attenuation at the reference frequency (f_{REF}) of 3 times at the input to the phase sensitive demodulator.

Values of the components used in the filter must be chosen to ensure that the phase shift at f_{REF} is within the allowable signal to reference phase shift of the converter.

Phase Sensitive Demodulator

The phase sensitive demodulator is effectively ideal and develops a mean dc output at the DEMODULATOR OUTPUT pin of

$$\frac{\pm 2\sqrt{2}}{\pi} \times \text{(DEMODULATOR INPUT rms voltage)}$$

for sinusoidal signals in phase or antiphase with the reference (for a square wave the DEMODULATOR OUTPUT voltage will equal the DEMODULATOR INPUT). This provides a signal at the DEMODULATOR OUTPUT which is a dc level proportional to the positional error of the converter.

DC Error Scaling = 160mV/bit (10 bits resolution)
- = 40mV/bit (12 bits resolution)
- = 10mV/bit (14 bits resolution)
- = 2.5mV/bit (16 bits resolution)

When the tracking loop is closed, this error is nulled to zero unless the converter input angle is accelerating.

Integrator

The integrator components (R4, C4, R5, C5) are external to the 2S82 to allow the user to determine the optimum dynamic characteristics for any given application. The section "COMPONENT SELECTION" explains how to select components for a chosen bandwidth.

Since the output from the integrator is fed to the VCO INPUT, it is proportional to velocity (rate of change of output angle) and can be scaled by selection of R6, the VCO input resistor. This is explained in the section "VOLTAGE CONTROLLED OSCILLATOR (VCO)" below.

To prevent the converter from "flickering" (i.e., continually toggling by ±1 bit when the quantized digital angle, φ, is not an exact representation of the input angle, θ) feedback is internally applied from the VCO to the integrator input to ensure that the VCO will only update the counter when the error is greater than or equal to 1 bit. In order to ensure that this feedback "hysteresis" is set to 1LSB the input current to the integrator must be scaled to be 100nA/bit. So,

$$R4 = \frac{\text{DC Error Scaling (mV/bit)}}{100\ (\text{nA/bit})}\ M\Omega$$

Any offset at the input of the integrator will affect the accuracy of the conversion as it will be treated as an error signal and offset the digital output. One LSB of extra error will be added for each 100nA of input bias current. The method of adjusting out this offset is given in the section "COMPONENT SELECTION."

5

Voltage Controlled Oscillator (VCO)

The VCO is essentially a simple integrator feeding a pair of dc level comparators. Whenever the integrator output reaches one of the comparator threshold voltages, a fixed charge is injected into the integrator input to balance the input current. At the same time the counter is clocked either up or down, dependent on the polarity of the input current. In this way the counter is clocked at a rate proportional to the magnitude of the input current of the VCO.

During the reset period the input continues to be integrated although the reset period is constant at 400ns.

The VCO rate is fixed for a given input current by the VCO scaling factor,

$= 7.4\text{kHz}/\mu\text{A}$

The tracking rate in rps per μA of VCO input current can be found by dividing the VCO scaling factor by the number of LSB changes per rev (i.e., 4096 for 12-bit resolution).

The input resistor R6 determines the scaling between the converter velocity signal voltage at the INTEGRATOR OUTPUT pin and the VCO input current. Thus to achieve a 5V output at 100 rps (6000 rpm) and 12-bit resolution the VCO input current must be:

$(100 \times 4096)/(7400) = 55.3\mu\text{A}$

Thus, R6 would be set to: $5/(55.3 \times 10^{-6}) = 90\text{k}\Omega$

The velocity offset voltage depends on the VCO input resistor, R6, and the VCO bias current and is given by

Velocity Offset Voltage = R6 × (VCO bias current)

The temperature coefficient of this offset is given by

Velocity Offset Tempco = R6 × (VCO bias current tempco)

where the VCO bias current tempco is typically $-0.55\text{nA}/^{\circ}\text{C}$.

The maximum recommended rate for the VCO is 1.1MHz which sets the maximum possible tracking rate.

Since the maximum voltage swing available at the integrator output is ±8V, this implies that the minimum value for R6 is 54kΩ. As

$$\text{Max Current} = \frac{1.1 \times 10^6}{7.4 \times 10^3} = 149\mu\text{A}$$

$$\text{Min Value } R_6 = \frac{8}{149 \times 10^{-6}} = 54\text{k}\Omega$$

VCO OUTPUT

VCO OUTPUT: In order to overcome the "free play" inherent in a servo system using digitized position feedback, an analog output voltage is available representing the resolver shaft position within the least significant bit of the digital angle output.

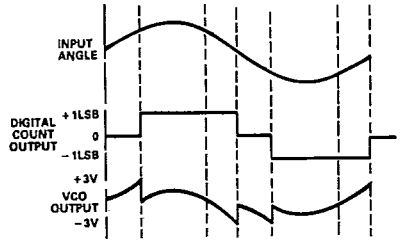

Figure 4.

The converter updates the output if the error is an LSB or greater and the VCO output gives the positional error smaller than 1LSB.

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Figure 4 illustrates how the VCO output compensates for the instances where, due to hysteresis, there is no change in the digital count output for 1LSB change in input angle. The sum of the digital count output and VCO output equals the actual input angle.

Transfer Function

By selecting components using the method outlined in the section "Component Selection" the converter will have a critically damped time response and maximum phase margin. The closed-loop transfer function is given by:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{14\,(1 + s_N)}{(s_N + 2.4)\,(s_N^2 + 3.4\,s_N + 5.8)}$$

where, s_N, the normalized frequency variable is

$$s_N = \frac{2}{\pi}\,\frac{s}{f_{BW}}$$

and f_{BW} is the closed-loop 3dB bandwidth (selected by the choice of external components).

The acceleration constant, K_A, is given approximately by

$$K_A = 6 \times (f_{BW})^2 \quad \text{sec}^{-2}$$

The normalized gain and phase diagrams are given in Figures 5 and 6.

The small signal step response is shown in Figure 6. The time from the step to the first peak is t_1, and the t_2 is the time from

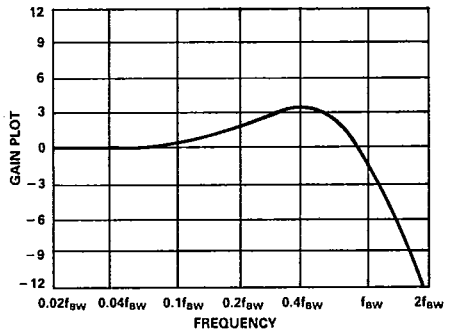

Figure 5. 2S82 Gain Plot

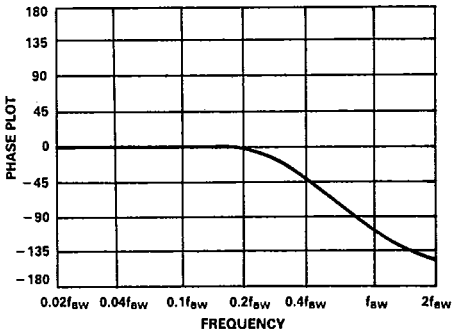

Figure 6. 2S82 Phase Plot

the step until the converter as settled to 1LSB. The times t_1 and t_2 are given approximately by

$$t_1 = \frac{1}{f_{BW}}$$

$$t_2 = \frac{5}{f_{BW}} \times \frac{R}{12}$$

where R = resolution, i.e., 10, 12, 14 or 16.

The large signal step response (for steps greater than 10 degrees) applies when the error voltage will exceed the linear range of the converter. Typically the converter will take 3 times longer to reach the first peak for a 179 degrees step.

The response to a velocity step, the velocity output will exhibit the same time response characteristics as outlined above for the position output.

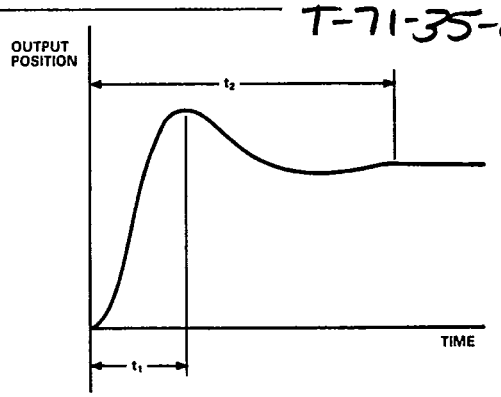

Figure 7. 2S82 Small Step Response

5

APPLICATIONS

USING THE 2S82 AS A CONTROL TRANSFORMER

The ratio multiplier section of the 2S82 can be used independently to the rest of the converter to perform the function of control transformer. In this mode the signal from the resolver inputs, θ, is compared to a digital angle, ϕ, loaded into the counters. Any difference between these two angles results in an analog voltage at the AC ERROR OUTPUT. To use the device in this way the DATA LOAD pin is used.

Applying a logic "Lo" to the DATA LOAD pin will allow data to be loaded into the counters of the converter from the data lines. It is important that the data lines are placed in the high impedance state before loading data.

To operate the 2S82 as a tracking resolver-to-digital converter the DATA LOAD pin should be left unconnected as it is pulled high internally to +12V.

CAUSES OF ADDITIONAL ERROR

Integrator Offset

Additional inaccuracies in the conversion of the resolver signals will result from an offset at the input to the integrator as it will be treated as an error signal. This error will be typically 1 arc minute over the operating temperature range.

A description of how to adjust for zero offset is given in the section "COMPONENT SELECTION" and the circuit required is shown in Figure 1.

Differential Phase Shift

Phase shift between the sine and the cosine signals from the resolver is known as differential phase shift and can cause static error. Some differential phase shift will be present on all resolvers as a result of coupling. A small resolver residual voltage (quadrature voltage) indicates a small differential phase shift. Additional phase shift can be introduced if the sine channel wires and the cosine channel wires are treated differently. For instance, different cable lengths or different loads could cause differential phase shift.

The additional error caused by differential phase shift on the input signals approximates to

Error = 0.53 a·b arc minutes

where a = differential phase shift in degrees
and b = signal to reference phase shift in degrees.

This error can be minimized by choosing a resolver with a small residual voltage, ensuring that the sine and cosine signals are handled identically and removing the reference phase shift (see section "CONNECTING THE RESOLVER"). By taking these precautions, the extra error can be made insignificant.

Resolver Phase Shift

Under static operating conditions phase shift between the reference and the signal lines alone will not theoretically affect the converter's static accuracy.

However, most resolvers exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

$$\frac{\text{Shaft Speed (rps)} \times \text{Phase Shift (Degs)}}{\text{Reference Frequency}}$$

For example, for a phase shift of 20 degrees, a shaft rotation of 22 rps and a reference frequency of 5kHz, the converter will exhibit an additional error of:

$$\frac{22 \times 20}{5000} = 0.088 \text{ degrees}$$

This effect can be eliminated by putting a phase shift in the reference to the converter equivalent to the phase shift in the resolver (see section "CONNECTING THE RESOLVER").

NOTE: Capacitive and inductive crosstalk in the signal and reference leads and wiring can cause similar problems.

USING THE VELOCITY SIGNAL

The signal at the INTEGRATOR OUTPUT pin relative to the ANALOG GROUND pin is an analog voltage proportional to the rate of change of the input angle. This signal can be used to stabilize servo loops or in place of a velocity transducer. Although the conversion loop of the 2S82 includes a digital section there is an additional totally analog feedback loop around the velocity signal. This ensures that there is no digital effects on the output signal and that the loop is closed even when the input signals are such that the digital output does not change.

A better quality velocity signal will be achieved if the following points are considered.

1. Protection.
   The velocity signal should be buffered before use.
2. Reversion Error.
   If necessary, the reversion error can be reduced by a simple trimming circuit. Reversion error, or side-to-side nonlinearity, is a result of differences in the up and down rates of the VCO. The reversion error can be nulled by varying one supply rail relative to the other.
3. Ripple and Noise.
   Noise on the input signals to the converter is the major cause of noise on the velocity signal. This can be reduced to a minimum if the following precautions are taken:

   The resolver is connected to the converter using separate screened twisted pair cable for the sine, cosine and reference signals.

   Care is taken to reduce the external noise wherever possible.

   An HF filter is fitted before the Phase Sensitive Demodulator (as described in the section HF FILTER).

   A resolver is chosen that has a low residual voltage, i.e., a small signal in quadrature with the reference.

   Components are selected to operate the 2S82 with the lowest acceptable bandwidth.

   Feedthrough of the reference frequency should be removed by a filter on the velocity signal.

   The signal voltages are 2V rms to prevent a ripple at the LSB switching rate. This is because the 1LSB of analog feedback that prevents the output from flickering will be incorrectly scaled (see section "INTEGRATOR").

If the above precautions are taken, a very good noise and ripple performance is obtainable making the 2S82 velocity signal usable in very noisy environments, for instance in motor drive applications with PWM switching noise.

The positional error curve of the converter and the resolver will result in an apparent acceleration when the resolver is rotating at a constant velocity. The main result of this will be a ripple on the velocity signal twice per revolution.

CONNECTING THE RESOLVER

The recommended connection circuit is shown in Figure 8.

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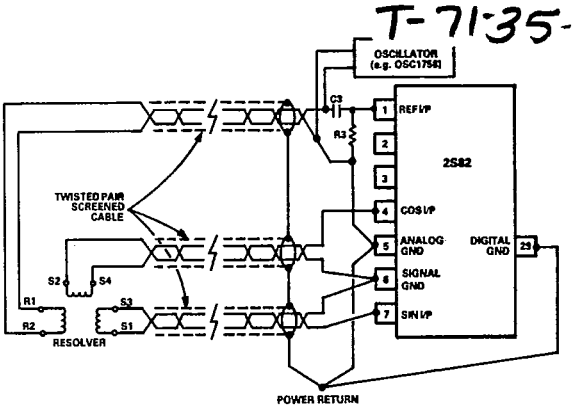

Figure 8. Connecting the 2S82 to a Resolver

In cases where the reference phase relative to the input signals from the resolver requires adjustment, this can be easily achieved by varying the value of the resistor R2 of the HF filter (see Figure 1).

Assuming that R1 = R2 = R and C1 = C2 = C

and Reference Frequency $= \frac{1}{2\pi R C}$

By altering the value of R2 the phase of the reference relative to the input signals will change in an approximately linear manner for phase shifts of up to 10 degrees.

Increasing R2 by 10% introduces a phase lag of 2 degrees. Decreasing R2 by 10% introduces a phase lead of 2 degrees.

For signal and reference voltages greater than 2V rms a simple voltage divider circuit of resistors can be used to generate the correct signal level at the converter. Care should be taken to ensure that the ratios of the resistors between the sine signal line and ground and the cosine signal line and ground are the same. Any difference will result in an additional position error.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Plastic Leaded Chip Carrier