

DUAL 2-INPUT OR GATE

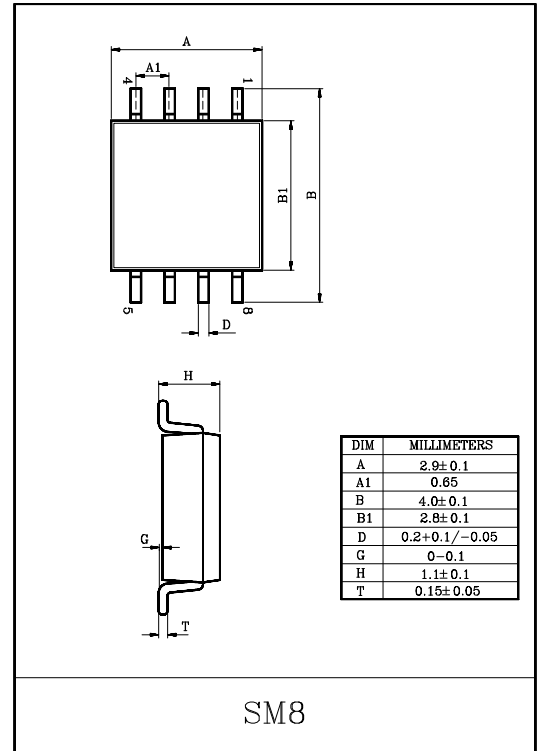
The KIC7W32FU is a high speed C²MOS 2-INPUT OR GATE fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the C²MOS low power dissipation. The internal circuit is composed of 3 stage including buffer output, which enables high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

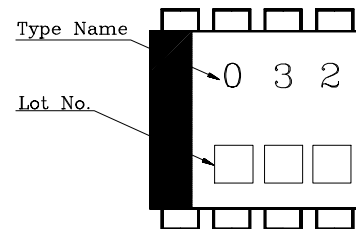
- High Speed : $t_{pd}=6ns$ (Typ.) at $V_{CC}=5V$.
- Low Power Dissipation : $I_{CC}=1\mu A$ (Max.) at $T_a=25^\circ C$.
- High Noise Immunity : $V_{NIH}=V_{NIL}=28\% V_{CC}$ (Min.).
- Output Drive Capability : 10 LSTTL Loads.
- Symmetrical Output Impedance : $|I_{OH}|=I_{OL}=4mA$ (Min.)
- Balanced Propagation Delays : $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range : $V_{CC(opr)}=2\sim 6V$.

MAXIMUM RATINGS (T_a=25°C)

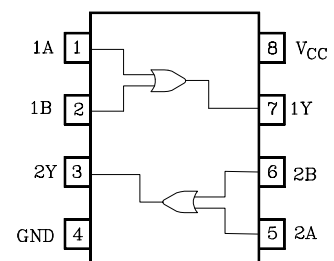
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V _{CC}	-0.5~7	V
DC Input Voltage	V _{IN}	-0.5~V _{CC} +0.5	V
DC Output Voltage	V _{OUT}	-0.5~V _{CC} +0.5	V
Input Diode Current	I _{IK}	±20	mA
Output Diode Current	I _{OK}	±20	mA
DC Output Current	I _{OUT}	±25	mA
DC V _{CC} /Ground Current	I _{CC}	±25	mA
Power Dissipation	P _D	300	mW
Storage Temperature	T _{stg}	-65~150	°C
Lead Temperature (10s)	T _L	260	°C



MARKING

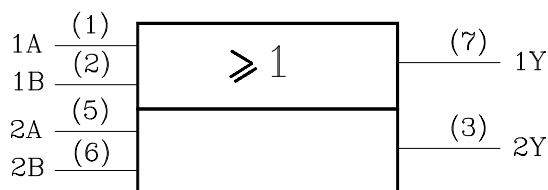


PIN CONNECTION(TOP VIEW)



KIC7W32FU

LOGIC DIAGRAM



TRUTH TABLE

A	B	Y
H	H	H
L	H	H
H	L	H
L	L	L

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 ($V_{CC}=2.0V$) 0~ 500 ($V_{CC}=4.5V$) 0~ 400 ($V_{CC}=6.0V$)	ns

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITION	$T_a=25^\circ\text{C}$			$T_a=-40\sim 85^\circ\text{C}$		UNIT					
			V_{CC}	MIN.	TYP.	MAX.	MIN.		MAX.				
High-Level Input Voltage	V_{IH}	-	2.0	1.5	-	-	1.5	-	V				
			4.5	3.15	-	-	3.15	-					
			6.0	4.2	-	-	4.2	-					
Low-Level Input Voltage	V_{IL}	-	2.0	-	-	0.5	-	0.5	V				
			4.5	-	-	1.35	-	1.35					
			6.0	-	-	1.8	-	1.8					
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu\text{A}$	2.0	1.9	2.0	-	1.9	-	V			
				4.5	4.4	4.5	-	4.4	-				
				6.0	5.9	6.0	-	5.9	-				
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IL}$	$I_{OL}=20\mu\text{A}$	2.0	-	0.0	0.1	-	0.1	V			
				4.5	-	0.0	0.1	-	0.1				
				6.0	-	0.0	0.1	-	0.1				
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	± 0.1	-	± 1.0	μA			
				Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND	6.0	-	-		1.0	-	10.0

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AC ELECTRICAL CHARACTERISTICS (C_L=15pF, V_{CC}=5V, Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	Ta=25°C			UNIT
			MIN.	TYP.	MAX.	
Output Transition Time	t _{TLH} t _{THL}	-	-	4	8	ns
Propagation Delay Time	t _{pLH} t _{pHL}	-	-	6	12	ns

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t _{TLH} t _{THL}	-	2.0	-	25	75	-	95	ns
			4.5	-	7	15	-	19	
			6.0	-	6	13	-	16	
Propagation Delay Time	t _{pLH} t _{pHL}	-	2.0	-	27	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Input Capacitance	C _{IN}	-	-	5	10	-	10	pF	
Power Dissipation Capacitance	C _{PD}	(Note 1)	-	21	-	-	-		

Note 1 : C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit.)

Average operating current can be obtained by the equation hereunder.

$$I_{CC(oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per gate)}$$