P89LV51RD2

8-bit 80C51 3 V low power 64 kB Flash microcontroller with 1 kB RAM

Rev. 01 — 30 June 2003 **Product data**

1. General description

The P89LV51RD2 is an 80C51 microcontroller with 64 kB Flash and 1024 bytes of data RAM.

A key feature of the P89LV51RD2 is its X2 mode option. The design engineer can choose to run the application with the conventional 80C51 clock rate (12 clocks per machine cycle) or select the X2 mode (6 clocks per machine cycle) to achieve twice the throughput at the same clock frequency. Another way to benefit from this feature is to keep the same performance by reducing the clock frequency by half, thus dramatically reducing the EMI.

The Flash program memory supports both parallel programming and in serial In-System Programming (ISP). Parallel programming mode offers gang-programming at high speed, reducing programming costs and time to market. ISP allows a device to be reprogrammed in the end product under software control. The capability to field/update the application firmware makes a wide range of applications possible.

The P89LV51RD2 is also In-Application Programmable (IAP), allowing the Flash program memory to be reconfigured even while the application is running.

2. Features

- 80C51 Central Processing Unit
- 3 V Operating voltage from 0 to 33 MHz
- 64 kB of on-chip Flash program memory with ISP (In-System Programming) and IAP (In-Application Programming)
- Supports 12-clock (default) or 6-clock mode selection via software or ISP
- SPI (Serial Peripheral Interface) and enhanced UART
- PCA (Programmable Counter Array) with PWM and Capture/Compare functions
- Four 8-bit I/O ports with three high-current Port 1 pins (16 mA each)
- Three 16-bit timers/counters
- Programmable Watchdog timer (WDT)
- Eight interrupt sources with four priority levels
- Second DPTR register
- Low EMI mode (ALE inhibit)
- TTL- and CMOS-compatible logic levels

- Brown-out detection
- Low power modes
  - Power-down mode with external interrupt wake-up
  - Idle mode
- PDIP40, PLCC44 and TQFP44 packages

3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
P89LV51RD2BA	PLCC44	plastic leaded chip carrier; 44 leads	
P89LV51RD2FA			
P89LV51RD2BBC	TQFP44	plastic thin quad flat package; 44 leads	
P89LV51RD2BN	PDIP40	plastic dual in-line package; 40 leads	

3.1 Ordering options

Table 2: Ordering options

Type number	Temperature range	Frequency
P89LV51RD2BA	0 °C to +70 °C	0 to 33 MHz
P89LV51RD2FA	–40 °C to +85 °C	
P89LV51RD2BBC	0 °C to +70 °C	
P89LV51RD2BN	0 °C to +70 °C	

4. Block diagram

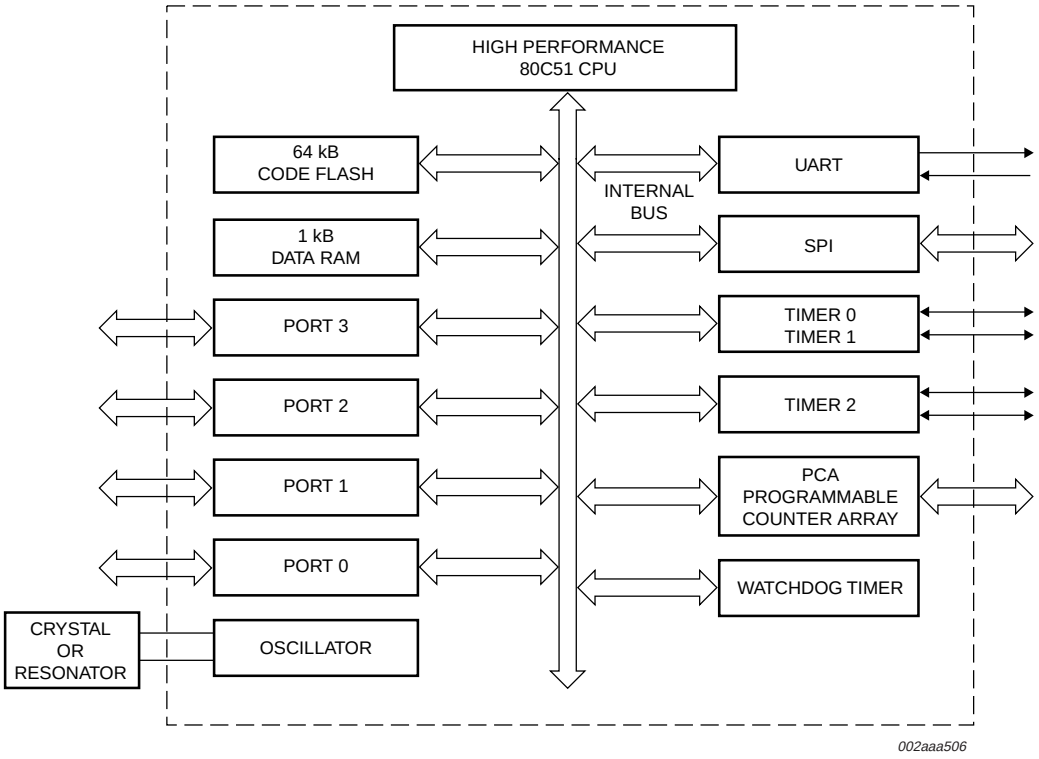

Fig 1. P89LV51RD2 block diagram.

5. Pinning information

5.1 Pinning

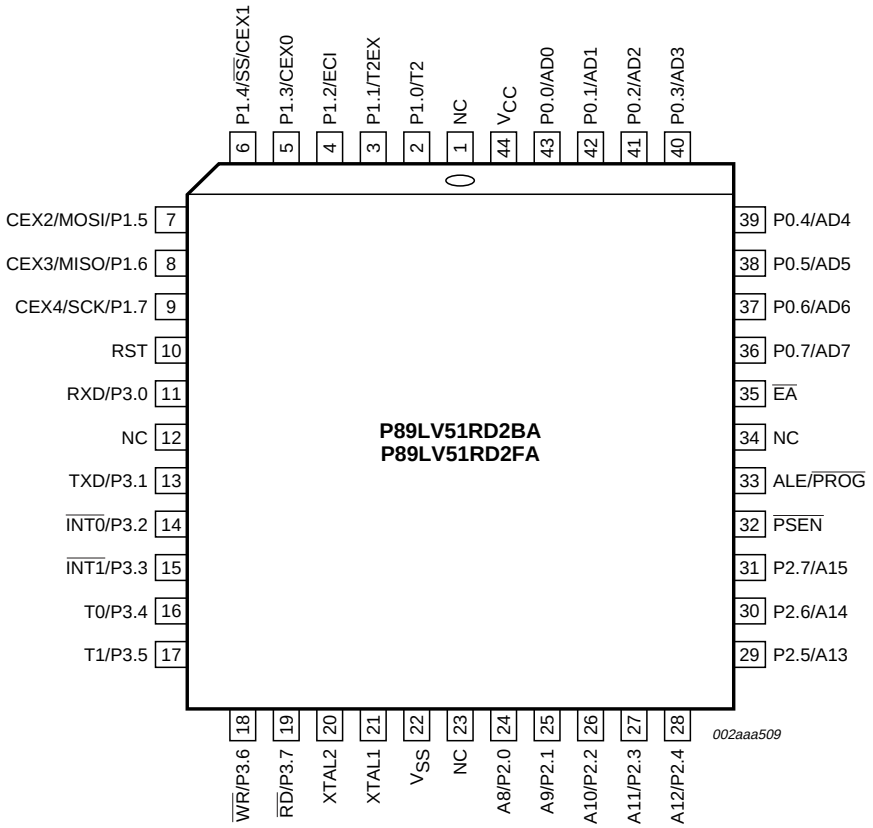

Fig 2. PLCC44 pin configuration.

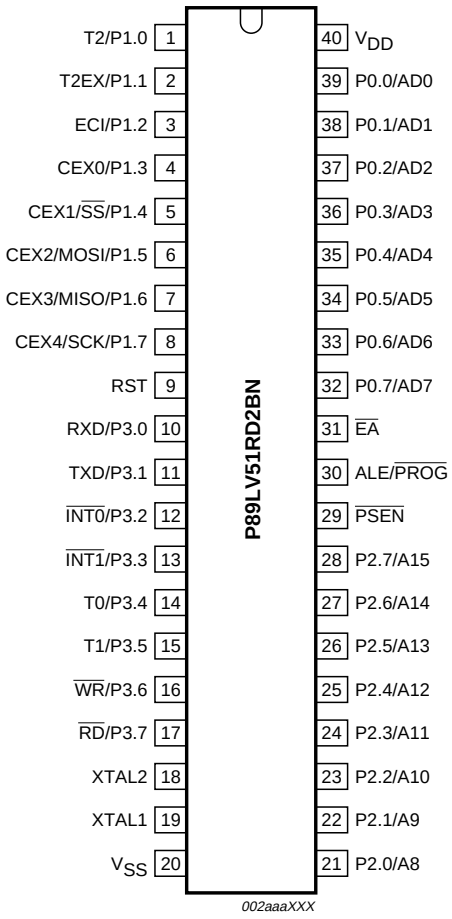

Fig 3. PDIP40 pin configuration.

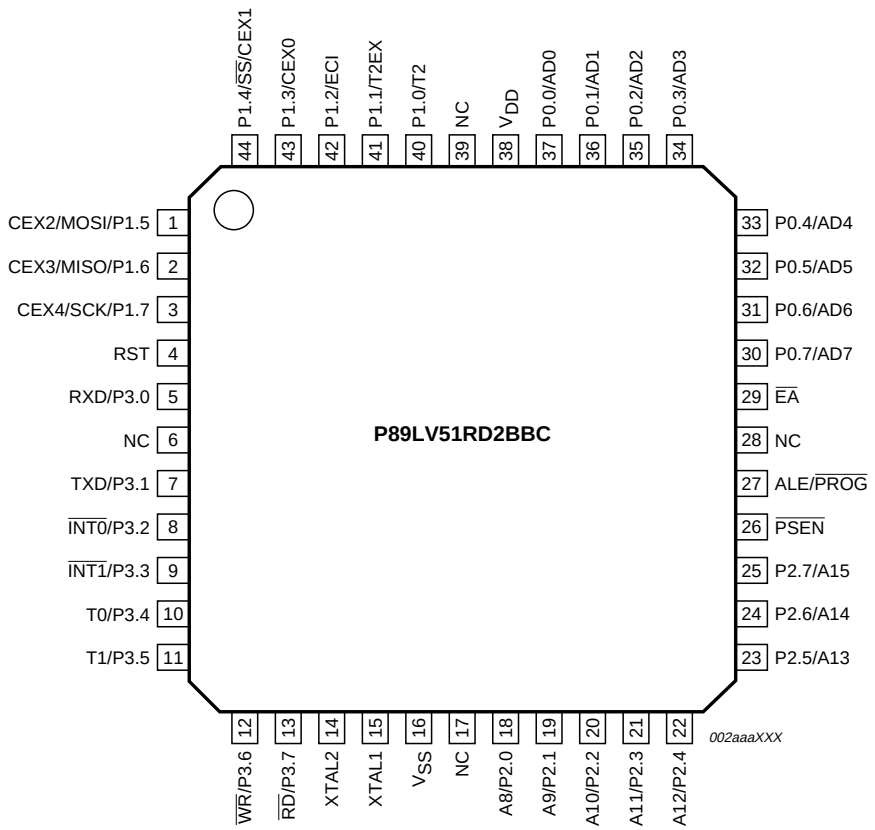

Fig 4. TQFP44 pin configuration.

5.2 Pin description

Table 3: P89LV51RD2 pin description

Symbol	Pin			Type	Description
	DIP40	TQFP44	PLCC44		
P0.0 to P0.7	39-32	37-30	43-36	I/O	**Port 0:** Port 0 is an 8-bit open drain bi-directional I/O port. Port 0 pins that have '1's written to them float, and in this state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external code and data memory. In this application, it uses strong internal pull-ups when transitioning to '1's. Port 0 also receives the code bytes during the external host mode programming, and outputs the code bytes during the external host mode verification. External pull-ups are required during program verification or as a general purpose I/O port.
P1.0 to P1.7	1-8	40-44, 1-3	2-9	I/O with internal pull-up	**Port 1:** Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 1 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups. P1.5, P1.6, P1.7 have high current drive of 16 mA. Port 1 also receives the low-order address bytes during the external host mode programming and verification.
P1.0	1	40	2	I/O	**T2:** External count input to Timer/counter 2 or Clock-out from Timer/counter 2
P1.1	2	41	3	I	**T2EX**: Timer/counter 2 capture/reload trigger and direction control
P1.2	3	42	4	I	**ECI**: External clock input. This signal is the external clock input for the PCA.
P1.3	4	43	5	I/O	**CEX0**: Capture/compare external I/O for PCA Module 0 Each capture/compare module connects to a Port 1 pin for external I/O. When not used by the PCA, this pin can handle standard I/O.
P1.4	5	44	6	I/O	**$\overline{SS}$**: Slave port select input for SPI **CEX1**: Capture/compare external I/O for PCA Module 1
P1.5	6	1	7	I/O	**MOSI**: Master Output Slave Input for SPI **CEX2**: Capture/compare external I/O for PCA Module 2
P1.6	7	2	8	I/O	**MISO**: Master Input Slave Output for SPI **CEX3**: Capture/compare external I/O for PCA Module 3
P1.7	8	3	9	I/O	**SCK**: Master Output Slave Input for SPI **CEX4**: Capture/compare external I/O for PCA Module 4

Table 3: P89LV51RD2 pin description...*continued*

Symbol	Pin			Type	Description
	DIP40	TQFP44	PLCC44		
P2.0 to P2.7	21-28	18-25	24-31	I/O with internal pull-up	**Port 2**: Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. Port 2 pins are pulled HIGH by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 2 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups. Port 2 sends the high-order address byte during fetches from external program memory and during accesses to external Data Memory that use 16-bit address (MOVX@DPTR). In this application, it uses strong internal pull-ups when transitioning to '1's. Port 2 also receives some control signals and a partial of high-order address bits during the external host mode programming and verification.
P3.0 to P3.7	10-17	5, 7-13	11, 13-19	I/O with internal pull-up	**Port 3**: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins are pulled HIGH by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 3 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups. Port 3 also receives some control signals and a partial of high-order address bits during the external host mode programming and verification.
P3.0	10	5	11	I	**RXD**: serial input port
P3.1	11	7	13	O	**TXD**: serial output port
P3.2	12	8	14	I	**$\overline{\text{INT0}}$**: external interrupt 0 input
P3.3	13	9	15	I	**$\overline{\text{INT1}}$**: external interrupt 1 input
P3.4	14	10	16	I	**T0**: external count input to Timer/counter 0
P3.5	15	11	17	I	**T1**: external count input to Timer/counter 1
P3.6	16	12	18	O	**$\overline{\text{WR}}$**: external data memory write strobe
P3.7	17	13	19	O	**$\overline{\text{RD}}$**: external data memory read strobe
$\overline{\text{PSEN}}$	29	26	32	I/O	**Program Store Enable**: $\overline{\text{PSEN}}$ is the read strobe for external program memory. When the device is executing from internal program memory, $\overline{\text{PSEN}}$ is inactive (HIGH). When the device is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. A forced HIGH-to-LOW input transition on the $\overline{\text{PSEN}}$ pin while the RST input is continually held HIGH for more than 10 machine cycles will cause the device to enter external host mode programming.
RST	9	4	10	I	**Reset**: While the oscillator is running, a HIGH logic state on this pin for two machine cycles will reset the device. If the $\overline{\text{PSEN}}$ pin is driven by a HIGH-to-LOW input transition while the RST input pin is held HIGH, the device will enter the external host mode, otherwise the device will enter the normal operation mode.

Table 3: P89LV51RD2 pin description...*continued*

Symbol	Pin			Type	Description
	DIP40	TQFP44	PLCC44		
$\overline{EA}$	31	29	35	I	**External Access Enable**: $\overline{EA}$ must be connected to V_{SS} in order to enable the device to fetch code from the external program memory. $\overline{EA}$ must be strapped to V_{DD} for internal program execution. However, Security lock level 4 will disable $\overline{EA}$, and program execution is only possible from internal program memory. The $\overline{EA}$ pin can tolerate a high voltage of 12 V.
ALE/ $\overline{PROG}$	30	27	33	I/O	**Address Latch Enable:** ALE is the output signal for latching the low byte of the address during an access to external memory. This pin is also the programming pulse input ($\overline{PROG}$) for flash programming. Normally the ALE[1] is emitted at a constant rate of $\frac{1}{6}$ the crystal frequency[2] and can be used for external timing and clocking. One ALE pulse is skipped during each access to external data memory. However, if AO is set to 1, ALE is disabled.
NC	-	6, 17, 28, 39	1, 12, 23, 34	I/O	**No Connect**
XTAL1	19	15	21	I	**Crystal 1**: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	14	20	O	**Crystal 2:** Output from the inverting oscillator amplifier.
V_{DD}	40	38	44	I	**Power supply**
V_{SS}	20	16	22	I	**Ground**

[1] ALE loading issue: When ALE pin experiences higher loading (>30 pF) during the reset, the microcontroller may accidentally enter into modes other than normal working mode. The solution is to add a pull-up resistor of 3 kΩ to 50 kΩ to V_{DD}, e.g., for ALE pin.

[2] For 6-clock mode, ALE is emitted at $\frac{1}{3}$ of crystal frequency.

6. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	operating bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature range		–65	+150	°C
$V_{\overline{EA}}$	voltage on $\overline{EA}$ pin to V_{SS}		–0.5	14	V
V_n	DC voltage on any pin to ground potential		–0.5	V_{DD} + 0.5	V
V_{it}	transient voltage (<20 ns) on any other pin to V_{SS}		–1.0	V_{DD} + 1.0	V
$I_{OL(I/O)}$	maximum I_{OL} per I/O pins P1.5, P1.6, P1.7		-	20	mA
$I_{OL(I/O)}$	maximum I_{OL} per I/O for all other pins		-	15	mA
$P_{tot(pack)}$	total power dissipation per package	T_{amb} = 25 °C	-	1.5	W
	through hole lead soldering temperature	10 seconds	-	300	°C
	surface mount lead soldering temperature	3 seconds	-	240	°C
	output short circuit current	[1]	-	50	mA

[1] Outputs shorted for no more than one second. No more than one output shorted at a time. (Based on package heat transfer limitations, not device power consumption.)

7. Recommended operating conditions

Table 5: Operating range

Symbol	Description	Min	Max	Unit
T_{amb}	ambient temperature under bias			
	commercial	0	+70	°C
	industrial	–40	+85	°C
V_{DD}	supply voltage	2.7	3.6	V
f_{osc}	oscillator frequency	0	33	MHz
	oscillator frequency for in-application programming	0.25	33	MHz

Table 6: Reliability characteristics

Symbol	Parameter	Minimum specification	Units	Test method
N_{END}[1]	endurance	10,000	cycles	JEDEC Standard A117
T_{DR}[1]	data retention	100	years	JEDEC Standard A103
I_{LTH}[1]	latch up	100 + I_{DD}	mA	JEDEC Standard 78

[1] This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 7: Recommended system power-up timings

Symbol	Parameter	Minimum	Unit
$T_{PU-READ}$[1]	Power-up to read operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to write operation	100	µs

[1] This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 8: Pin impedance

(V_{DD} = 3.3 V, T_{amb} = 25 °C, f = 1 MHz, other pins open)

Parameter	Description	Test condition	Maximum	Unit
$C_{I/O}$[1]	I/O pin capacitance	$V_{I/O}$ = 0 V	15	pF
C_{IN}[1]	input capacitance	V_{IN} = 0 V	12	pF
L_{PIN}	pin inductance		20	nH

[1] This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

8. Static characteristics

Table 9: DC electrical characteristics

T_{amb} = 0 °C to +70 °C or –40 °C to +85 °C; V_{DD} = 2.7 V to 3.6 V; V_{SS} = 0 V

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IL}	LOW-level input voltage	2.7 V < V_{DD} < 3.6 V	–0.5	0.7	V
V_{IH}	HIGH-level input voltage	2.7 V < V_{DD} < 3.6 V	0.2V_{DD} + 0.9	V_{DD} + 0.5	V
V_{IH1}	HIGH-level input voltage (XTAL1, RST)	2.7 V < V_{DD} < 3.6 V	0.7V_{DD}	V_{DD} + 0.5	V
V_{OL}	LOW-level output voltage (ports 1.5, 1.6, 1.7)	V_{DD} = 2.7 V; I_{OL} = 16 mA	-	1.0	V
V_{OL}	LOW-level output voltage (ports 1, 2, 3)[1]	V_{DD} = 2.7 V			
		I_{OL} = 100 µA	-	0.3	V
		I_{OL} = 1.6 mA	-	0.45	V
		I_{OL} = 3.5 mA	-	1.0	V
V_{OL1}	LOW-level output voltage (port 0, ALE, $\overline{PSEN}$)[1][3]	V_{DD} = 2.7 V			
		I_{OL} = 200 µA	-	0.3	V
		I_{OL} = 3.2 mA	-	0.45	V
V_{OH}	HIGH-level output voltage (ports 1, 2, 3, ALE, $\overline{PSEN}$)[4]	V_{DD} = 2.7 V			
		I_{OH} = -10 µA	V_{DD} – 0.3	-	V
		I_{OH} = -30 µA	V_{DD} – 0.7	-	V
		I_{OH} = -60 µA	V_{DD} – 1.5	-	V
V_{OH1}	HIGH-level output voltage (port 0 in External Bus Mode)[4]	V_{DD} = 2.7 V			
		I_{OH} = -200 µA	V_{DD} – 0.3	-	V
		I_{OH} = -3.2 mA	V_{DD} – 0.7	-	V
V_{BOD}	brown-out detection voltage		2.35	2.55	V
I_{IL}	logic 0 input current (ports 1, 2, 3)	V_{IN} = 0.4 V	-	–75	µA
I_{TL}	logic 1-to-0 transition current (ports 1, 2, 3)[5]	V_{IN} = 2 V	-	–650	µA
I_{LI}	input leakage current (port 0)	0.45 V < V_{IN} < V_{DD} – 0.3 V	-	±10	µA
R_{RST}	RST pull-down resistor		-	225	kΩ
C_{IO}	pin capacitance[6]	@ 1 MHz, T_{amb} = 25 °C	-	15	pF
I_{DD}	power supply current				
	active mode	@ 12 MHz	-	11.5	mA
		@ 33 MHz	-	30	mA
	idle mode	@ 12 MHz	-	8.5	mA
		@ 33 MHz	-	21	mA
	power-down mode (min. V_{DD} = 2 V)	T_{amb} = 0 °C to +70 °C	-	45	µA
		T_{amb} = –40 °C to +85 °C	-	55	µA

[1] Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

a) Maximum I_{OL} per 8-bit port: 26 mA

b) Maximum I_{OL} total for all outputs: 71 mA

c) If I_{OL} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

[2] Capacitive loading on Ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise due to external bus capacitance discharging into the Port 0 and 2 pins when the pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

[3] Load capacitance for Port 0, ALE and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.

[4] Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the V_{DD} – 0.7 specification when the address bits are stabilizing.

[5] Pins of Ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V.

[6] Pin capacitance is characterized but not tested. $\overline{EA}$ = 25 pF (max).

9. Dynamic characteristics

Table 10: AC characteristics

Over operating conditions: load capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF

T_{amb} = 0 °C to +70 °C or −40 °C to +85 °C; V_{DD} = 2.7 V to 3.6 V @ 33 MHz; V_{SS} = 0 V

Symbol	Parameter	33 MHz (X1 mode) 16 MHz (X2 mode)[1]		Variable		Unit
		Min	Max	Min	Max	
$1/T_{CLCL}$	X1 Mode oscillator frequency	0	33	0	33	MHz
$1/2T_{CLCL}$	X2 Mode oscillator frequency	0	16	0	16	MHz
t_{LHLL}	ALE pulse width	46	-	$2T_{CLCL} - 15$	-	ns
t_{AVLL}	address valid to ALE LOW	5	-	$T_{CLCL} - 25$	-	ns
t_{LLAX}	address hold after ALE LOW	5	-	$T_{CLCL} - 25$	-	ns
t_{LLIV}	ALE LOW to valid instruction in	-	56	-	$4T_{CLCL} - 65$	ns
t_{LLPL}	ALE LOW to $\overline{PSEN}$ LOW	5	-	$T_{CLCL} - 25$	-	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	66	-	$T_{CLCL} - 25$	-	ns
t_{PLIV}	$\overline{PSEN}$ LOW to valid instruction in	-	35	-	$3T_{CLCL} - 55$	ns
t_{PXIX}	input instruction hold after $\overline{PSEN}$	-	-	0	-	ns
t_{PXIZ}	input instruction float after $\overline{PSEN}$	-	25	-	$T_{CLCL} - 5$	ns
t_{PXAV}	$\overline{PSEN}$ to address valid	22	-	$T_{CLCL} - 8$	-	ns
t_{AVIV}	address to valid instruction in	-	72	-	$5T_{CLCL} - 80$	ns
t_{PLAZ}	$\overline{PSEN}$ LOW to address float	-	10	-	10	ns
t_{RLRH}	$\overline{RD}$ pulse width	142	-	$6T_{CLCL} - 40$	-	ns
t_{WLWH}	write pulse width ($\overline{WR}$)	142	-	$6T_{CLCL} - 40$	-	ns
t_{RLDV}	$\overline{RD}$ LOW to valid data in	-	62	-	$5T_{CLCL} - 90$	ns
t_{RHDX}	data hold after $\overline{RD}$	0	-	0	-	ns
t_{RHDZ}	data float after $\overline{RD}$	-	36	-	$2T_{CLCL} - 25$	ns
t_{LLDV}	ALE LOW to valid data in	-	152	-	$8T_{CLCL} - 90$	ns
t_{AVDV}	address to valid data in	-	183	-	$9T_{CLCL} - 90$	ns
t_{LLWL}	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW	66	116	$3T_{CLCL} - 25$	$3T_{CLCL} + 25$	ns
t_{AVWL}	address to $\overline{RD}$ or $\overline{WR}$ LOW	46	-	$4T_{CLCL} - 75$	-	ns
t_{WHQX}	data hold after $\overline{WR}$	3	-	$T_{CLCL} - 27$	-	ns
t_{QVWH}	data valid to $\overline{WR}$ HIGH	142	-	$7T_{CLCL} - 70$	-	ns
t_{RLAZ}	$\overline{RD}$ LOW to address float	-	0	-	0	ns
t_{WHLH}	$\overline{RD}$ to $\overline{WR}$ HIGH to ALE HIGH	5	55	$T_{CLCL} - 25$	$T_{CLCL} + 25$	ns

[1] Calculated values are for X1 mode only.

10. Revision history

Table 11: Revision history

Rev	Date	CPCN	Description
01	20030630	-	Product data (9397 750 11669); ECN 853-2432 30075 dated 27 June 2003

11. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

12. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contents

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