

2SA1597, 2SC4146



2018A

PNP/NPN Epitaxial Planar
Silicon Transistors

T-37-13
T-35-11

Switching Applications (with Bias Resistances R1=4.7kΩ, R2=47kΩ)

©2480

Applications

- Switching circuit, inverter circuit, interface circuit, driver circuit

Features

- On-chip bias resistance (R1=4.7kohms, R2=47kohms)
- Small-sized package (CP)

(): 2SA1597

Absolute Maximum Ratings at Ta=25°C

			unit
Collector to Base Voltage	V _{CB0}	(-)50	V
Collector to Emitter Voltage	V _{CEO}	(-)50	V
Emitter to Base Voltage	V _{EBO}	(-)6	V
Collector Current	I _C	(-)100	mA
Peak Collector Current	i _{cp}	(-)200	mA
Collector Dissipation	P _C	200	mW
Junction Temperature	T _J	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C

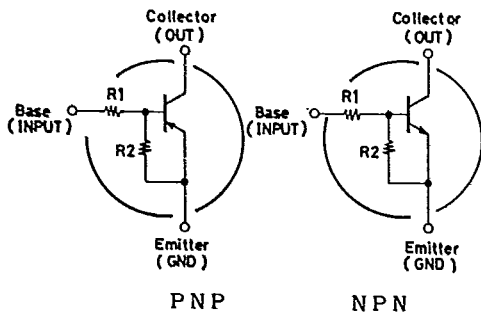
Electrical Characteristics at Ta=25°C

			min	typ	max	unit
Collector Cutoff Current	I _{CB0}	V _{CB} =(-)40V, I _E =0			(-)0.1	uA
Collector Cutoff Current	I _{CEO}	V _{CE} =(-)40V, I _B =0			(-)0.5	uA
Emitter Cutoff Current	I _{EBO}	V _{EB} =(-)5V, I _C =0	(-)74	(-)97	(-)138	uA
DC Current Gain	h _{FE}	V _{CE} =(-)5V, I _C =(-)5mA	70			
Gain-Bandwidth Product	f _T	V _{CE} =(-)10V, I _C =(-)5mA		250		MHz
				(200)		
Output Capacitance	c _{ob}	V _{CB} =(-)10V, f=1MHz		3.5		pF
				(5.3)		
C-E Saturation Voltage	V _{CE(sat)}	I _C =(-)10mA, I _B =(-)0.5mA		(-)0.1	(-)0.3	V
C-B Breakdown Voltage	V _{(BR)CBO}	I _C =(-)10uA, I _E =0	(-)50			V
C-E Breakdown Voltage	V _{(BR)CEO}	I _C =(-)100uA, R _{BE} =∞	(-)50			V

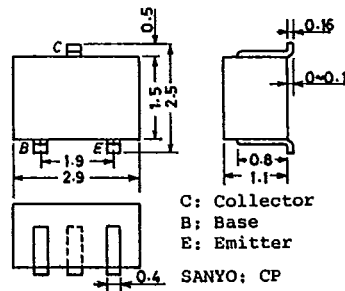
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Marking 2SA1597:XL, 2SC4146:FT

Electrical Connection



Case Outline 2018A (unit:mm)



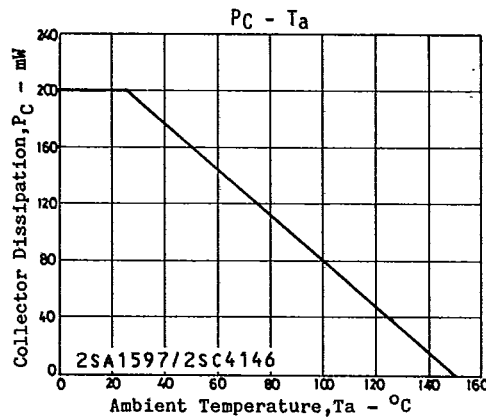
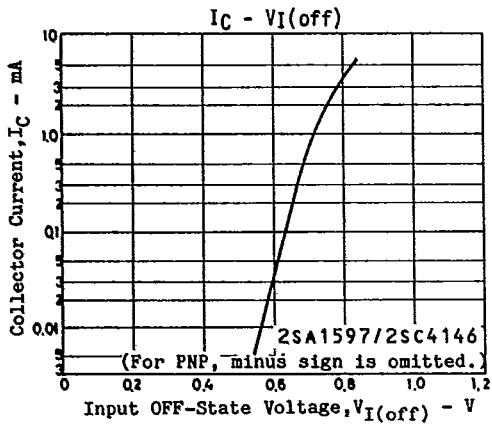
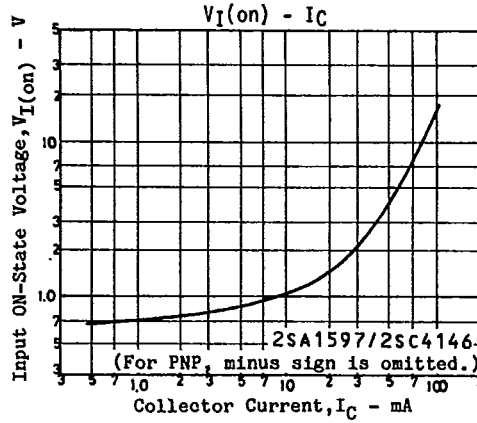
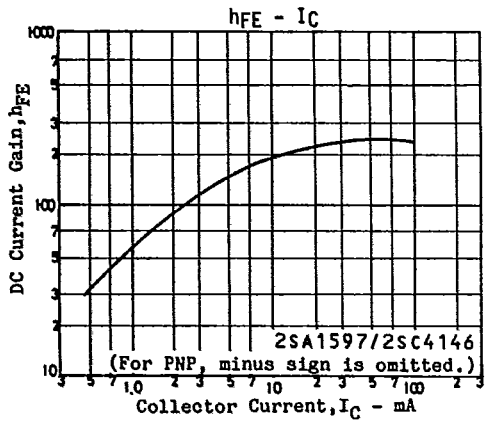
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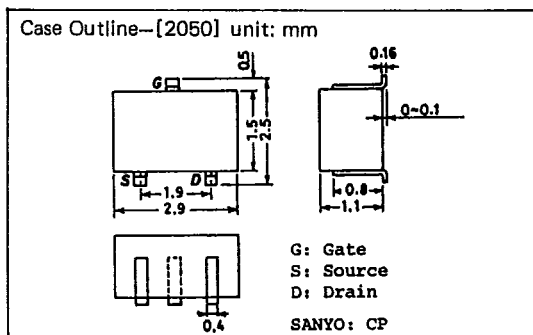
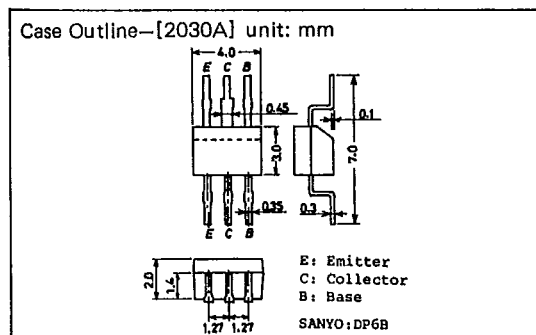
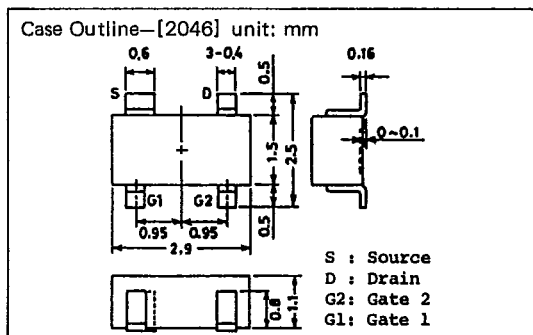
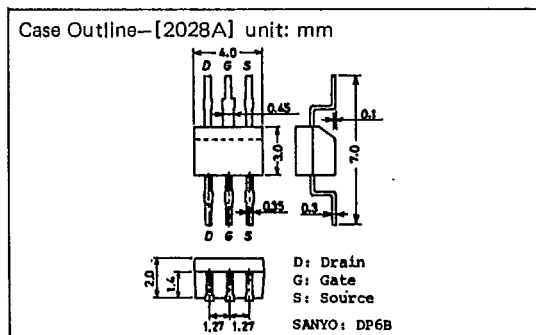
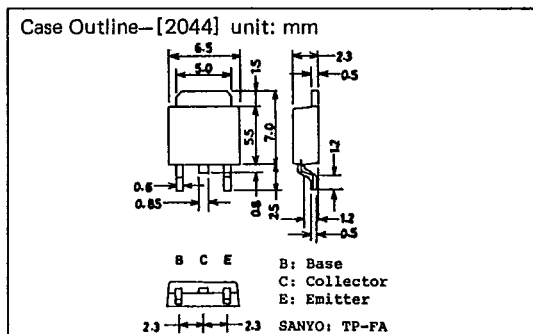
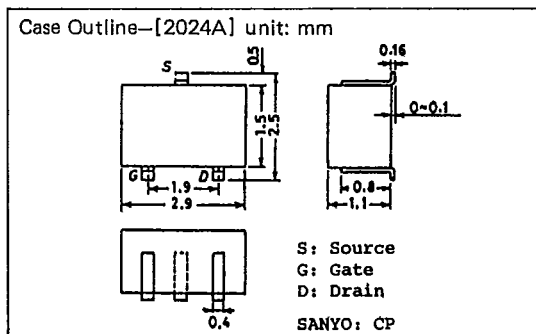
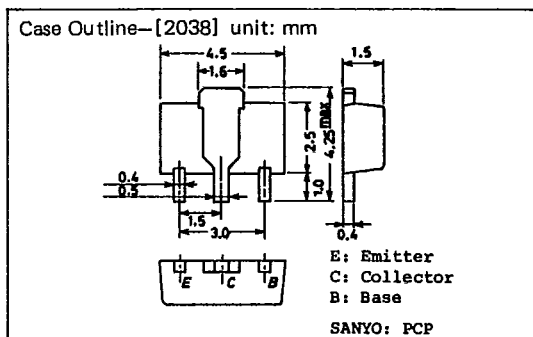
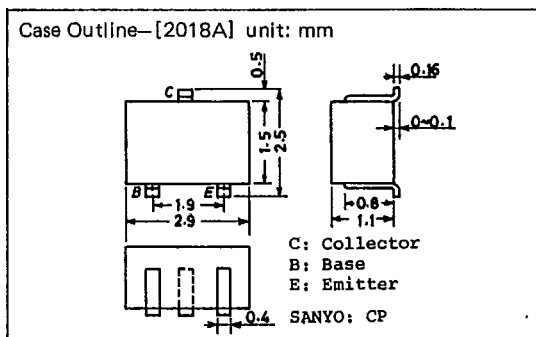
		min	typ	max	unit
Input OFF-State Voltage	$V_{I(off)}$ $V_{CE}=(-)5V, I_C=(-)100\mu A$	(-)0.5	(-)0.6	(-)0.8	V
Input ON-State Voltage	$V_{I(on)}$ $V_{CE}=(-)0.2V, I_C(-)5mA$	(-)0.7	(-)0.85	(-)1.3	V
Input Resistance	R_I	3.3	4.7	6.1	kohm
Resistance Ratio	$R1/R2$	0.09	0.1	0.11	



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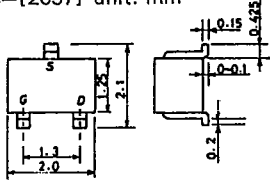
CASE OUTLINES OF SURFACE MOUNT TRANSISTORS

- All of Sanyo surface mount transistor case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.



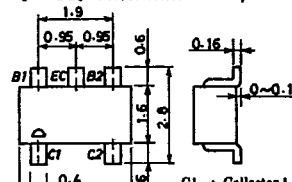
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Case Outline—[2057] unit: mm



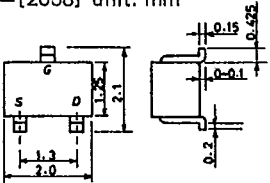
S: Source
G: Gate
D: Drain
SANYO: MCP

Case Outline—[2066] unit: mm



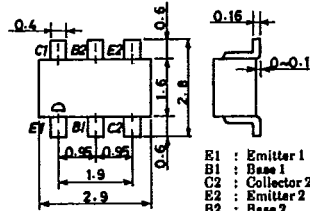
C1 : Collector 1
C2 : Collector 2
B2 : Base 2
EC : Emitter Common
B1 : Base 1
SANYO : CP6

Case Outline—[2058] unit: mm



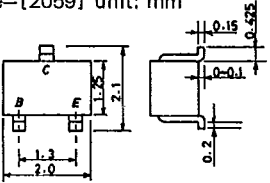
G: Gate
S: Source
D: Drain
SANYO: MCP

Case Outline—[2067] unit: mm



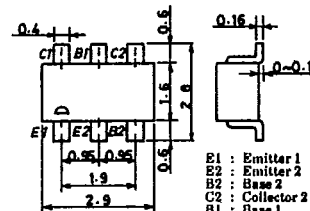
E1 : Emitter 1
B1 : Base 1
C2 : Collector 2
E2 : Emitter 2
B2 : Base 2
C1 : Collector 1
SANYO : CP6

Case Outline—[2059] unit: mm



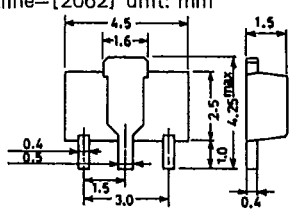
B: Base
C: Collector
E: Emitter
SANYO: MCP

Case Outline—[2068] unit: mm



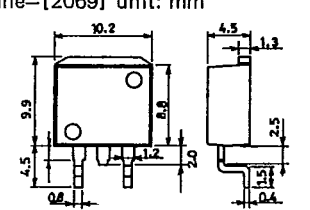
B1 : Emitter 1
E2 : Emitter 2
B2 : Base 2
C2 : Collector 2
B1 : Base 1
C1 : Collector 1
SANYO : CP6

Case Outline—[2062] unit: mm



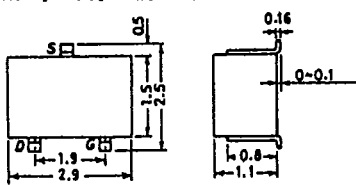
S: Source
D: Drain
G: Gate
SANYO: PCP

Case Outline—[2069] unit: mm



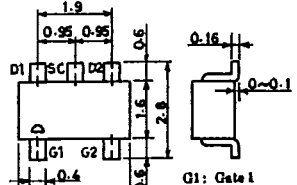
B: Base
C: Collector
E: Emitter
SANYO: SMP

Case Outline—[2065] unit: mm



S: Source
D: Drain
G: Gate
SANYO: CP

Case Outline—[2070] unit: mm



G1 : Gate 1
G2 : Gate 2
D2 : Drain 2
SC : Source Common
D1 : Drain 1
SANYO : CP6

T-9120

