ALPHA
SEMICONDUCTOR
Excellence in Analog Power Products

AS7660

DC-to-DC Voltage Converter

FEATURES
- Converts +5V Logic Supply To .... ±5V System
- Wide Input Voltage Range .... 1.2V to 12V
- Low Power Supply 500µA
- Efficient Voltage Conversion 99.9%
- RS232 Negative Power Supply
- Low Cost, Simple to Use
- Available in Standard 8 Pin Low Cost SOIC & µSOIC™
- ESD Protection up to 3KV
- Similar to Industry Standard ICL7660

APPLICATIONS
- -5 Volts for LCD
- A-to-D Converters
- D-to-A Converters
- Multiplexers
- Operational Amplifiers

PRODUCT DESCRIPTION
The ALPHA Semiconductor AS7660 DC-to-DC converter will generate a negative voltage from a positive source. The AS7660 generates -5V in +5V digital systems and with two external capacitors, the device will convert a 1.2V to 12V input signal to a -1.2V to -12V level. AS7660 input can also be as low as 1.0V by connecting LV to Ground.

AS7660 chip contains a DC Power Supply Regulator, RC Oscillator, Voltage-Level Transistor, four Output Power MOS Switches, and a unique logic element which ensures latch-up free operation.

The Oscillator, when unloaded, oscillates at a nominal frequency of 10KHZ for input voltage for 5 volts. The frequency can be lowered by the addition of an external capacitor to the OSC terminal, or the Oscillator may be overdriven by an external clock.

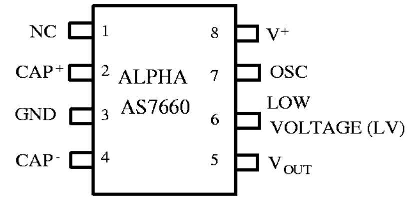
Applications include analog-to-digital converters, digital-to-analog converters, operational amplifiers and multiplexers. Many of these systems require negative supply voltages. The AS7660 allows +5V digital logic systems to incorporate these analog components without an additional main power source. Lower part count, less real estate, ease of use are just a few of the benefits of the AS7660. ALPHA Semiconductor, is the only manufacturer to use AS7660 in the very small µSOIC™.

ORDERING INFORMATION

Part Number	Temperature Range	Package Type
AS7660P	-40°C to +85°C	8 PIN DIP
AS7660S	-40°C to +85°C	8 PIN SOIC
AS7660Z	-40°C to +85°C	µSOIC™ 8-PIN

PIN CONNECTIONS

8-Pin P-DIP (P)
8-Pin Surface Mount (S)
µSOIC™ (Z)



Top View

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ....+13V...
LV and OSC Inputs
Voltage (Note 1)...............................0.3V to (V^+ +0.3V) for V^+ <5.5V
(V^+ -5.5V) to (V^+ to 0.3V) for V^+ <5.5V
Current into LV (Note 1) ....20µA for V^+ > 3.5V...
Output Short Duration ($V_{SUPPLY} \leq$ 5.5V) .... Continuous
Power Dissipation (Note 2)
Plastic DIP 375mW
Plastic SOIC...800mW

Operating Temperature Range
I Suffix... -40°C to +85°C
Storage Temperature Range............... -65°C to +150°C
Lead Temperature (Soldering, 10 sec).............. +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

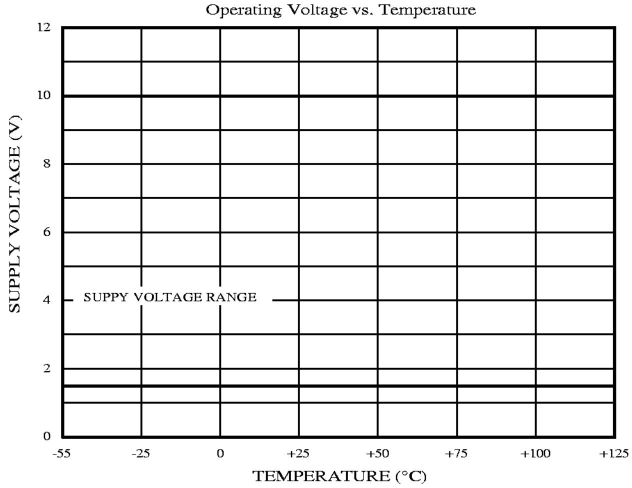
ELECTRICAL CHARACTERISTICS V^+ = 5V, T_A = +25°C, C_{OSC} = 0, Test Circuit (Figure 1), unless otherwise specified.

Parameter	Conditions	AS7660 Min	Typ.	Max	Units
Supply Current	$R_L = \infty$		170	500	µA
Supply Voltage Range, High	O° ≤ T_A + 70°C, R_L = 10kΩ, LV Open -55°C ≤ T_A ≤ +125°, 10kΩ, LV Open	3 3		6.5 5	V
Supply Voltage Range, Low D_X in Circuit	Min ≤ T_A ≤ Max, R_L = 10kΩ, LV to GND	1.5		3.5	V
Supply Voltage Range, High D_X in Circuit	Min ≤ T_A ≤ Max, R_L = 10kΩ, LV Open	3		10	V
Supply Voltage Range, Low D_X in Circuit	Min ≤ T_A ≤ Max, R_L = 10kΩ, LV to GND	1.5		3.5	V
Output Source Resistance	I_{OUT} = 20mA, T_A = 25°C I_{OUT} = 20mA, 0°C ≤ T_A ≤ +70°C (C Device) V^+ = 2V, I_{OUT} = 3mA, LV to GND 0°C ≤ T_A ≤ +70°C		55	100 120 300	Ω
Oscillator Frequency			10		kHz
Power Efficiency	R_L = 5kΩ	95	98		%
Voltage Conversion Efficiency	$R_L = \infty$	97	99.9		%
Oscillator Impedance	V^+ = 2V V^+ = 5V		1 100		MΩ kΩ

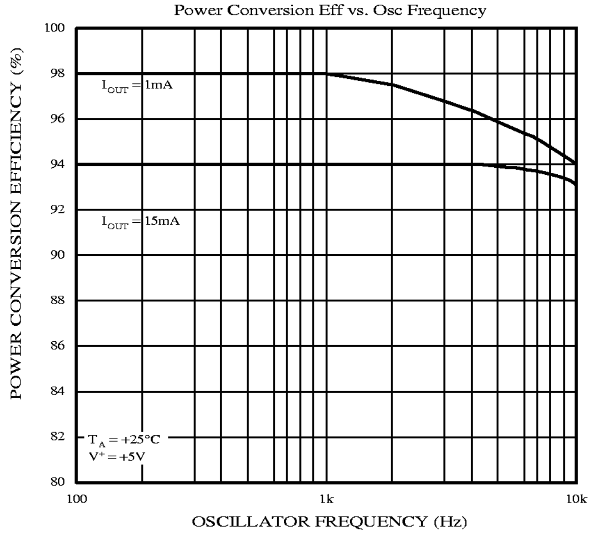
NOTES:
1. Connecting any input terminal to voltages greater than C+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the AS7660.
2. Derate linearly above 50°C by 5.5mW/°C.

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 1)

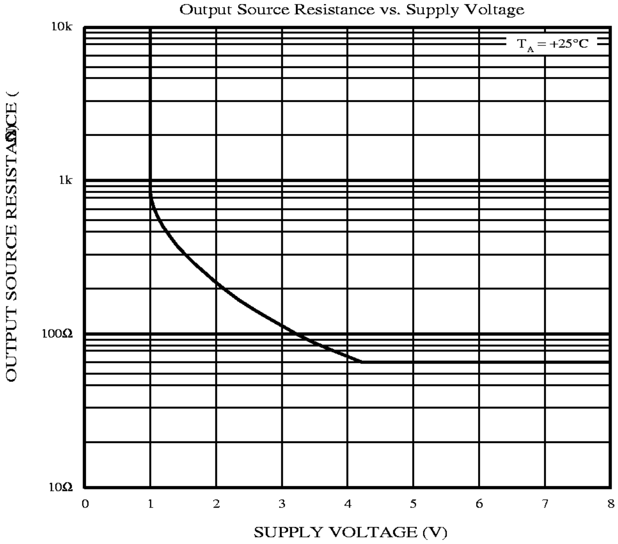
Operating Voltage vs. Temperature



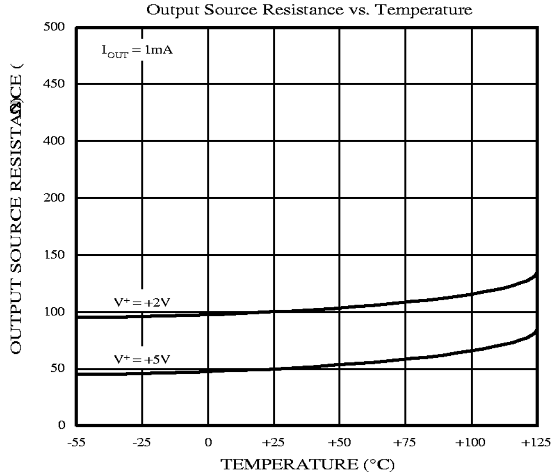
Power Conversion Eff vs. Osc Frequency



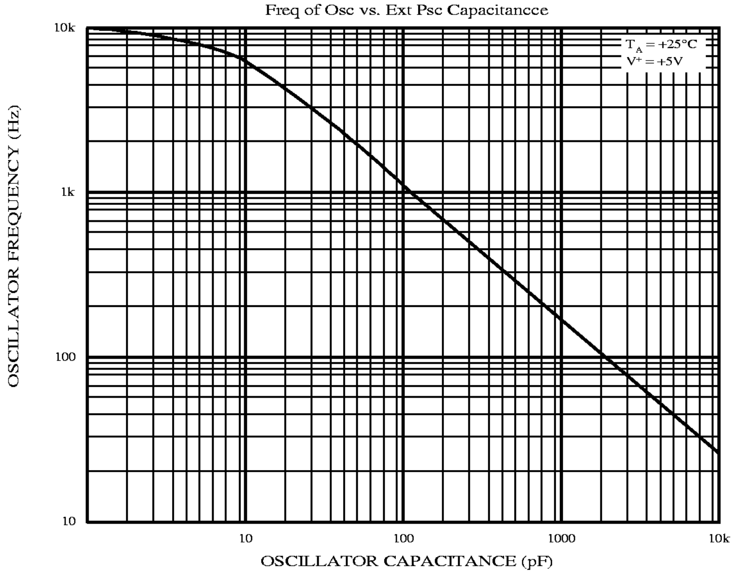
Output Source Resistance vs. Supply Voltage



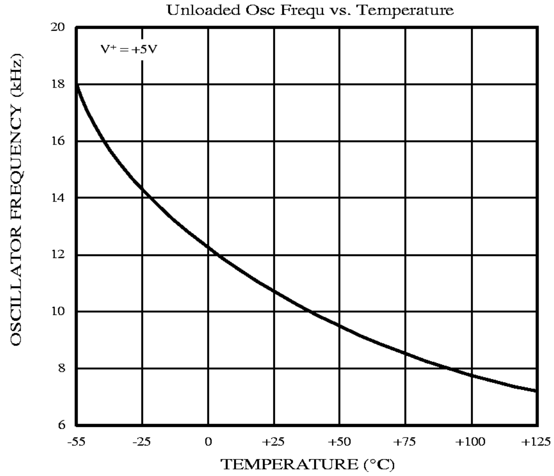
Output Source Resistance vs. Temperature



Freq of Osc vs. Ext Psc Capacitancce

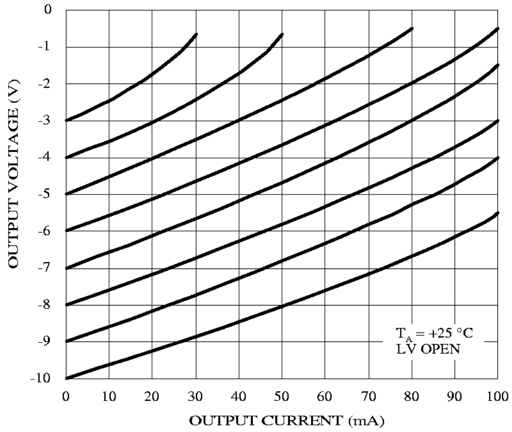


Unloaded Osc Frequ vs. Temperature

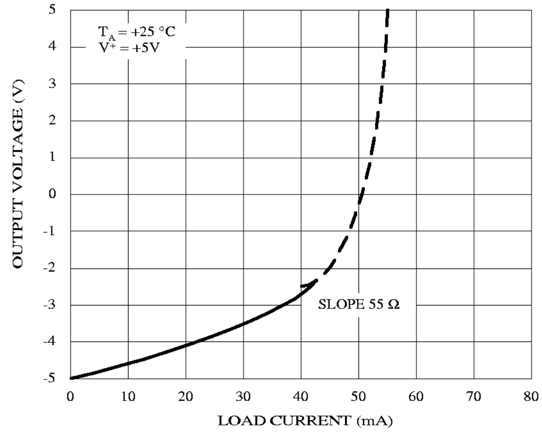


TYPICAL PERFORMANCE CHARACTERISTICS (Cont.)

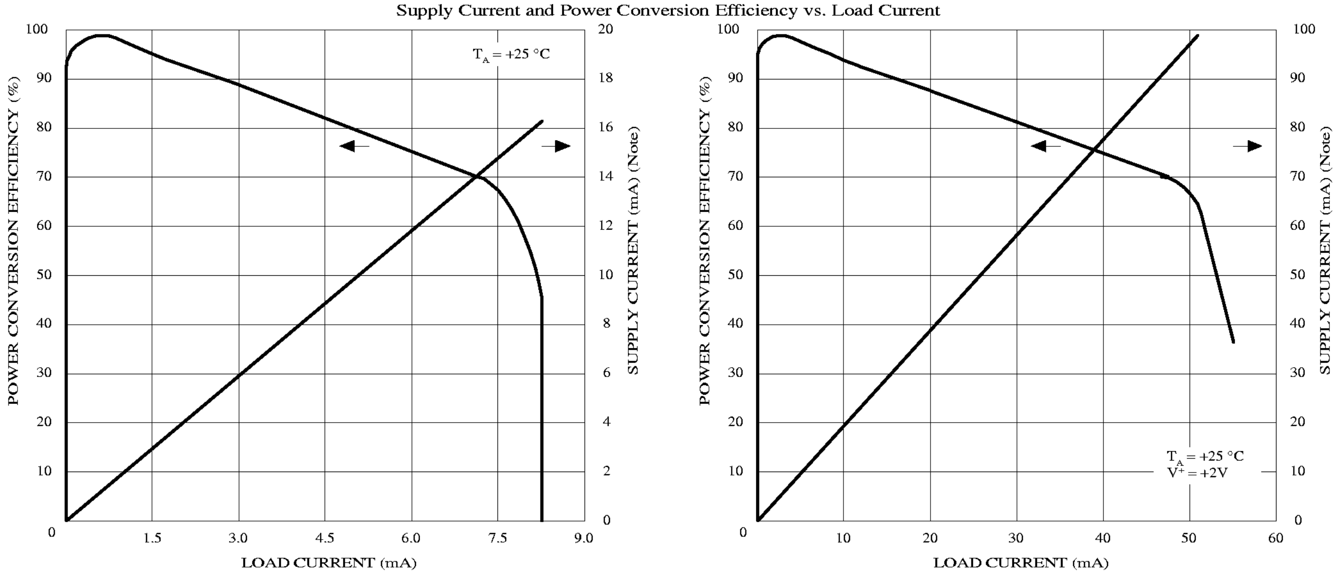
Output Voltage vs. Output Current



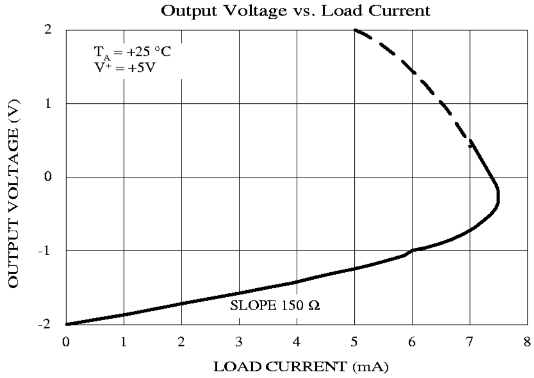
Output Voltage vs. Load Current

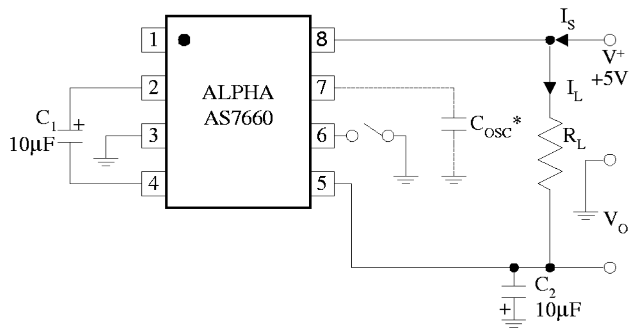


Supply Current and Power Conversion Efficiency vs. Load Current



Output Voltage vs. Load Current





NOTES: *For large values of C_{OSC}* (>1000 pF), the values of C_1 and C_2 should be increased to 100µF.

Figure 1. AS7660 Test Circuit

CIRCUIT DESCRIPTION

The AS7660 contains all the necessary circuitry to complete a voltage doubler, with the exception of two external capacitors, which may be inexpensive 10 µF polarized electrolytic capacitors. Operation is best understood by considering Figure 2, which shows an idealized voltage doubler. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2, such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2.

The four switches in Figure 2 are MOS power switches, S_1 is a P-channel device, and S_2, S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse-biased with respect to their sources, but not so much as to degrade their ON resistances. In addition, at circuit start-up, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this will result in high power losses and probable device latch-up.

This problem is eliminated in the AS7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.

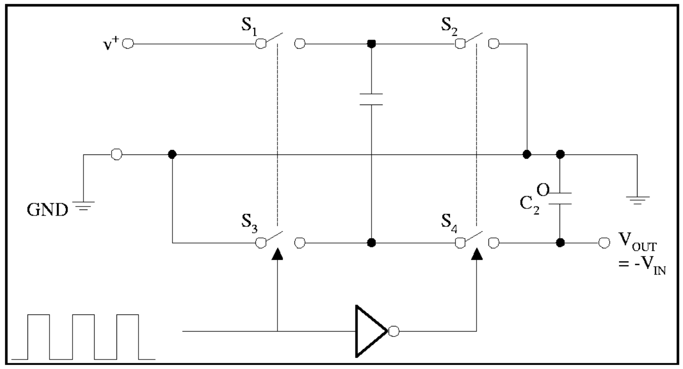


Figure 2. Idealized Switched Capacitor

The voltage regulator portion of the AS7660 is an integral part of the anti-latch-up circuitry. Its inherent voltage drop can, however, degrade operation at low voltages. To improve low-voltage operation, the LV pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5V, the LV terminal must be left open to ensure latch-up-proof operation and prevent device damage.

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory, a voltage multiplier can approach 100% efficiency if certain conditions are met:

1. The drive circuitry consumes minimal power.
2. The output switches have extremely low ON resistance and virtually no offset.
3. The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The AS7660 approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs. The energy lost is defined by:

$$E = 1/2\, C_1 (V_1^2 - V_2^2)$$

V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 2), compared to the value of R_L, there will be a substantial difference in voltages V_1 and V_2. Therefore, it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

DOS AND DON'TS

- Do not exceed maximum supply voltages.
- Do not connect LV terminal to GND for supply voltages greater than 3.5V
- Do not short circuit the output to V^+ supply for voltages above 5.5V for extended periods; however, transient conditions including start up are okay.
- When using polarized capacitors in the inverting mode, the + terminal of C_1 must be connected to pin 2 of the AS7660 and the - terminal of C_2 must be connected to GND Pin 4.

SIMPLE NEGATIVE VOLTAGE CONVERTER

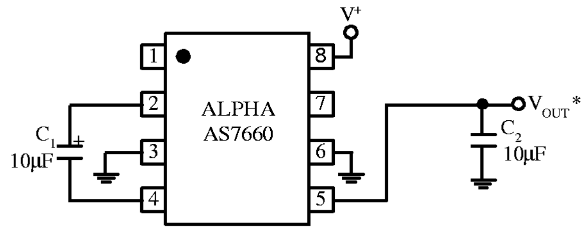
Figure 3 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operation range of + 1.2V to +12V, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5V.

The output characteristics of the circuit in Figure 3 are those of a nearly ideal voltage source in series with 70Ω. Thus, for a load current of -10mA and a supply voltage of +5V, the output voltage would be -4.3V.

The dynamic output impedance of the AS7660 is due, primarily, to capacitive reactance of the charge transfer capacitor (C_1). Since this capacitor is connected to the output for only 1/2 of the cycle, the equation is

$$X_C = \frac{2}{2\pi f\, C_1} = 3.18\Omega,$$

where f = 10 kHz and C_1 = 10 µF.



*NOTES: $V_{OUT} = -n\,V^+$ for $1.2V \le V^+ \le 12V$

PARALLELING DEVICES

Any number of AS7660 voltage converters may be paralleled to reduce output resistance (Figure 4). The reservoir capacitor, C_2, serves all devices, while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\text{ (of AS7660)}}{n\text{ (number of devices)}}$$

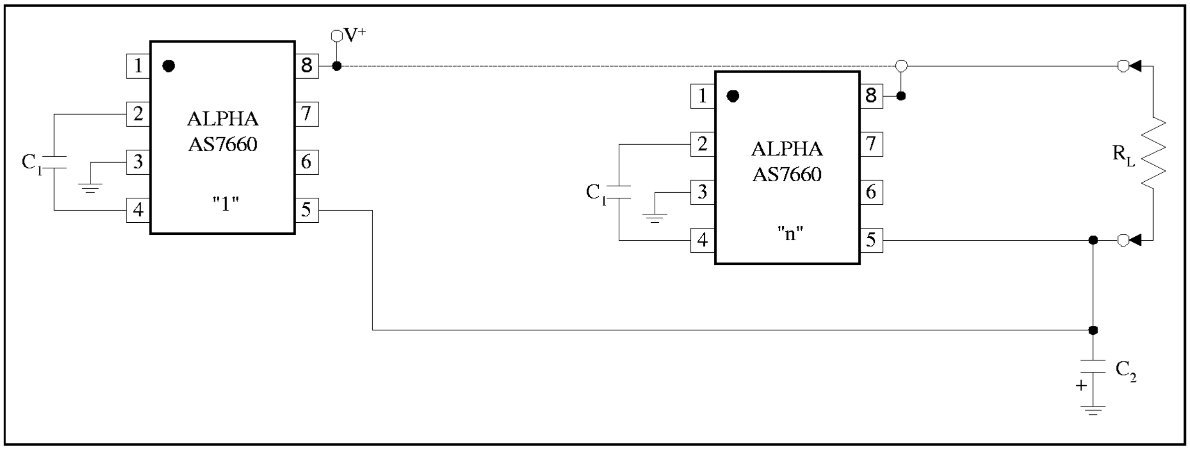


Figure 4. Paralleling Devices Lowers Output Impedance

CASCADING DEVICES

The AS7660 may be cascaded as shown (Figure 6) to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\ (V_{IN})$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual AS7660 R_{OUT} values.

CHANGING THE AS7660 OSCILLATOR FREQUENCY

It may be desirable in some applications (due to noise or other considerations) to increase the oscillator frequency. This is achieved by overdriving the oscillator form an external clock, as shown in Figure 6. In order to prevent possible device latch-up, a 1 kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10 kΩ pull-up resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

It is also possible to increase the conversion efficiency of the AS7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC}, as shown in figure 7. Lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and the reservoir (C_2) capacitors. To overcome this, increase the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100 pF capacitor between pin 7 (OSC) and pin 8 (V^+) will lower the oscillator frequency to 1 kHz from its nominal frequency of 10 kHz (a multiple of 10), and necessitate a corresponding increase in the values of C_1 and C_2 (from 10 µF to 100 µF).