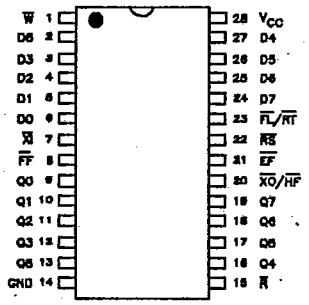
T-46-35

Dallas Semiconductor
4096 x 9 FIFO

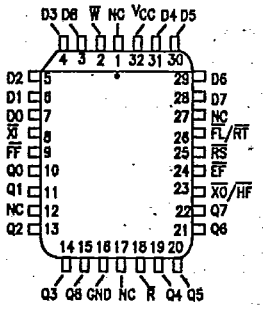
PRELIMINARY
DS2012 28-Pin DIP
DS2012R 32-Pin PLCC

FEATURES
- First-In, first-out memory based architecture
- Flexible 4096 x 9 organization
- Low power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- Available in 50 ns, 65 ns, and 80 ns access times
- Industrial temperature range -40°C to +85°C available designated N

PIN CONNECTIONS



28-PIN DIP



32-PIN PLCC

PIN NAMES

$\overline{W}$	- WRITE
$\overline{R}$	- READ
$\overline{RS}$	- RESET
FL/RT	- First Load/Retransmit
D_{0-8}	- Data In
Q_{0-8}	- Data Out
$\overline{XI}$	- Expansion In
$\overline{XO}/\overline{HF}$	- Expansion Out/Half Full
$\overline{FF}$	- Full Flag
$\overline{EF}$	- Empty Flag
V_{CC}	- 5 Volts
GND	- Ground
NC	- No Connect

DESCRIPTION
The DS2012 implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full, and empty flags, and unlimited expansion capability in both word size and depth. The main application of the DS2012 is as a rate buffer, sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. A half-full flag is available in the single-device and width-expansion configurations. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the WRITEs and READs are internally sequential, thereby requiring no address information, the pinout definition will serve this and future higher-densinty devices. The ninth bit is provided to support control or parity functions. Refer to DS2011 data sheet for detailed device description.

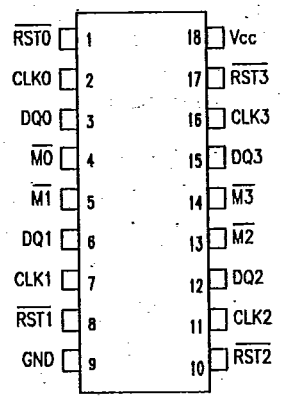
Dallas Semiconductor
Quad Port Serial RAM

PRELIMINARY
DS2015

FEATURES

- Four partitioned easy access ports
- No arbitration required
- Message flag for each port
- Low pin count serial access
- Simultaneous multiport reads
- Message length of up to eight bytes
- Low power CMOS
- Space saving 18 pin DIP
- Directly interfaces to the DS1206 Phantom interface
- Provides a low cost interconnect for up to four microprocessor based systems

PIN CONNECTIONS



PIN NAMES

$\overline{RST0}$-$\overline{RST3}$	Port 0 - Port 3 Reset
D/Q0-D/Q3	Port 0 - Port 3 Data I/O
CLK0-CLK3	Port 0 - Port 3 Clock
$\overline{M0}$-$\overline{M3}$	Port 0 - Port 3 Message Ready
GND	Ground
Vcc	+5 Volts

DESCRIPTION

The DS2015 Quad Port Serial RAM is a low cost device which can be used to loosely couple up to four microprocessors or microcontrollers. Arbitration is handled by protocol and a message center which forces discipline and prevents collisions. Each port has access to all other ports for reading information and can write information only in its own memory area. The memory space for each port is 64 bits. Access to and from each port takes place over a three wire serial bus. The serial bus keeps pin count low while affording sufficient bandwidth to accommodate loosely coupled system communication. Each port also has a message flag which can be used to warn of message ready conditions.

OPERATION

The DS2015 has four separate three wire serial ports. Each port has direct read and write access to eight message bytes of RAM which are designated as belonging to that particular port. In addition, each port has read only access to three groups of eight message bytes each which are designated as belonging to the three other ports. Messages are sent between any port by reading and writing the eight message bytes of the four ports. An optional check byte is provided for each group of eight message bytes to verify data integrity (see Figure 1). All of the cells within the RAM matrix are quad-ported and can be read simultaneously from four different directions. This reduces arbitration to concerns of write operations only.

Each of the four three wire serial ports contains a three byte protocol register which defines access to the RAM, and sets the discipline which controls arbitration between the four ports.

Protocol Register

The first byte of the protocol register is called the port select (see Figure 2). This byte contains an eight bit pattern which must match the first 8 bits sent on an active port or any further activity will be ignored (Figure 3). A port is active when the reset line is inactive (high) and the CLK input is transitioning. The first eight bits are sent into a port on the D/Q line. The second byte of the protocol register contains eight bits of status information about activity on all four ports. This byte, called the message center, is read only and divided into two nibbles; messages sent and mailbox. The first four bits tell which messages the port has sent to other ports that have not been received. By reading these four bits, the inquiring port knows not to send new messages because all the receiving ports have not read to a previously sent message. Each message sent bit is cleared when the receiving port reads the last bit of its message or the $\overline{RST}$ input of the receiving port is driven low. The next four bits of the message center provide each port with the knowledge of pending messages which are ready for reading and the number of the port or ports which are sending the message(s). These bits are set by the destination bits of each port when a sending port finishes writing the last bit of a message. The mailboxes are read only bits. All message center bits are driven out on the DQ line while $\overline{RST}$ is inactive and the clock is transitioning. The third byte of the protocol register contains the execution code. The execution code byte is also divided into two four bit nibbles; the action code and the destination. This byte is write only and data is input on the D/Q line with $\overline{RST}$ inactive and the CLK input transitioning. The action code bits have only three patterns which will allow subsequent action to take place (Figure 3). An action code of four zeros (0000) calls for a read message action to occur in one of the four sections of the Quad Port RAM as specified by the destination bits. A read message can occur to only one port and, therefore, only one destination bit can be set for an action code of 0000. Once a destination bit is set, a complete message of eight bytes must be read in order to reset the message sent bit in the sending port's protocol register. An action code of a one and three zeros (1000) calls for a write message action to be performed. A write message can only be written in the section of the Quad Port RAM that is identified with the sending port. However, a message which is written by a sending port can be directed to one or more ports by the destination bits. The destination bits will cause the mailbox bits in the protocol register of each port which is to receive the message to be set to logic one as soon as the last bit of the message is written by the sending port. An action code of two ones and two zeros (1100) calls for a write message action to be performed with more

FIGURE 1: QUAD PORT BLOCK DIAGRAM

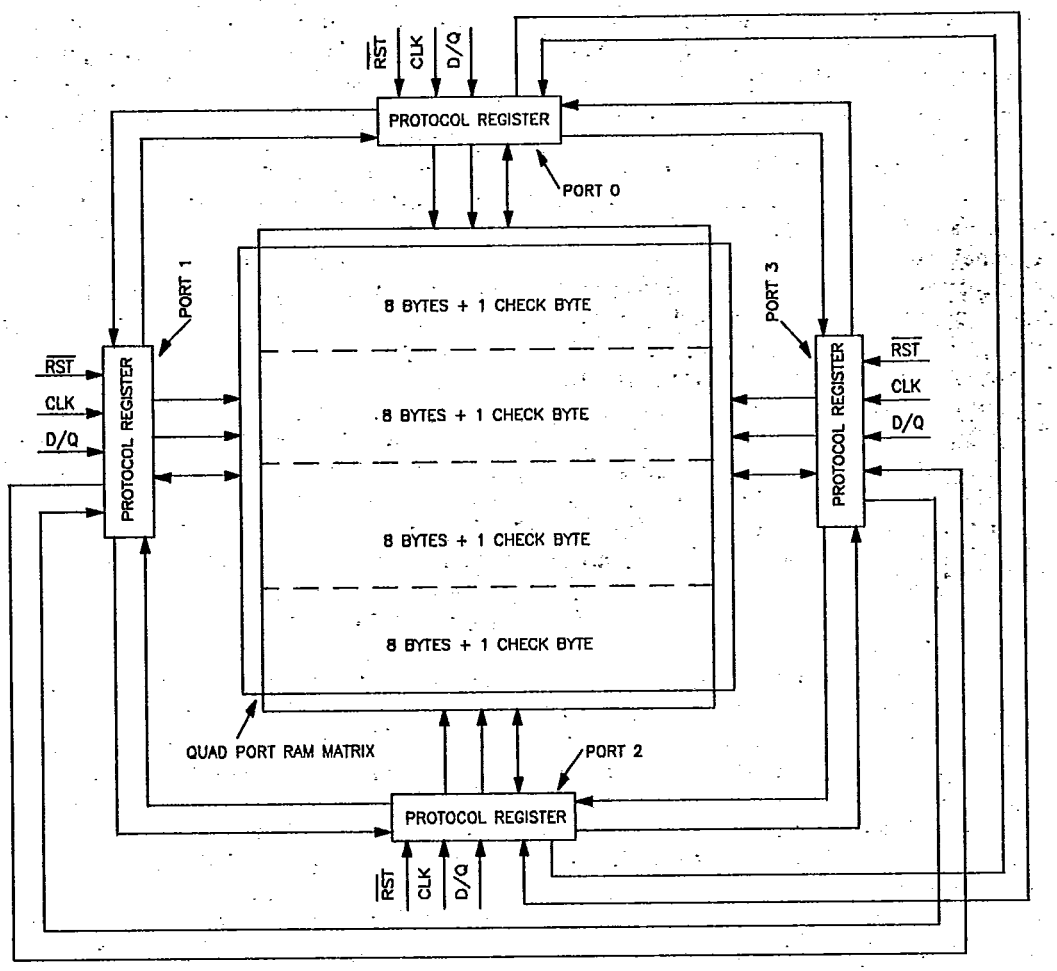
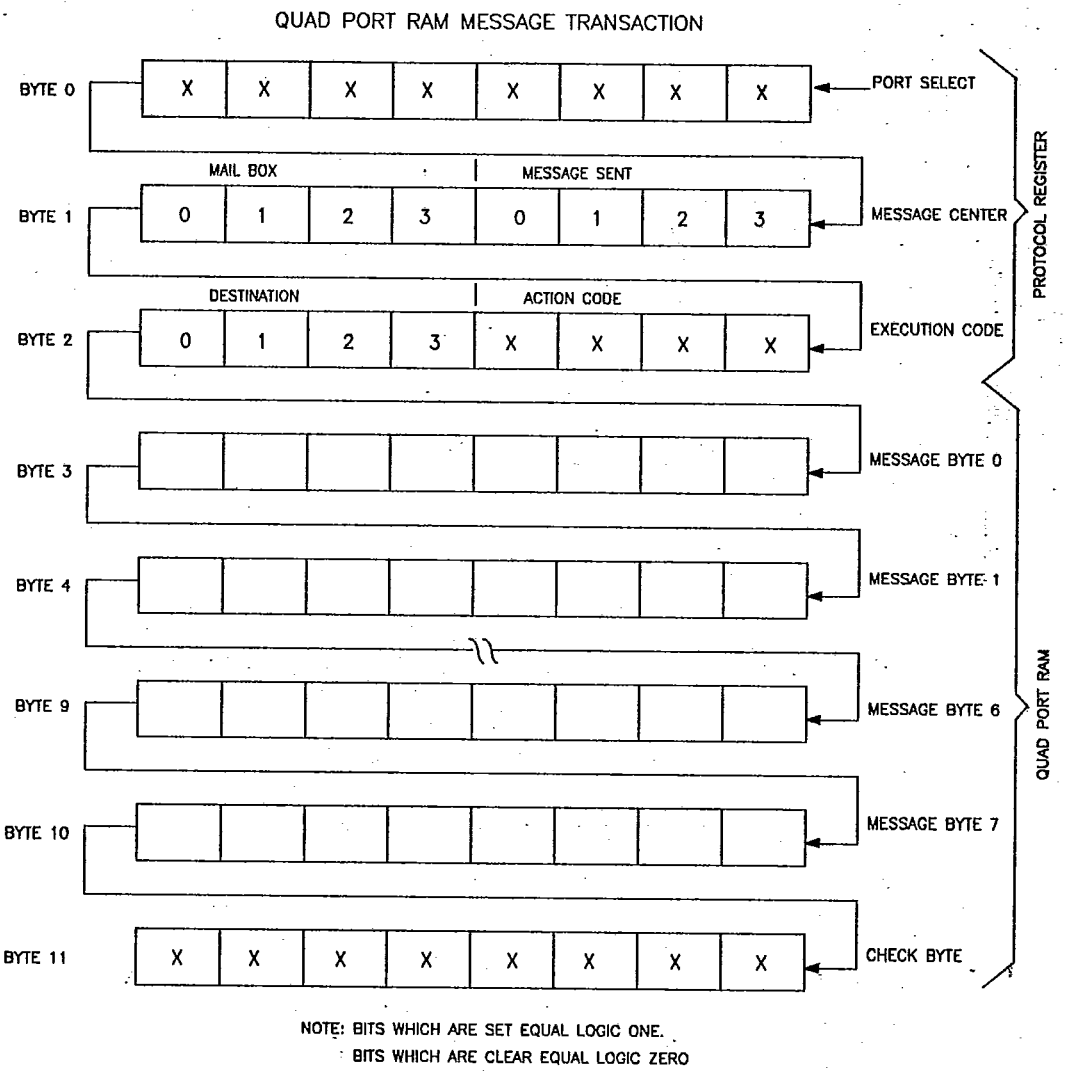
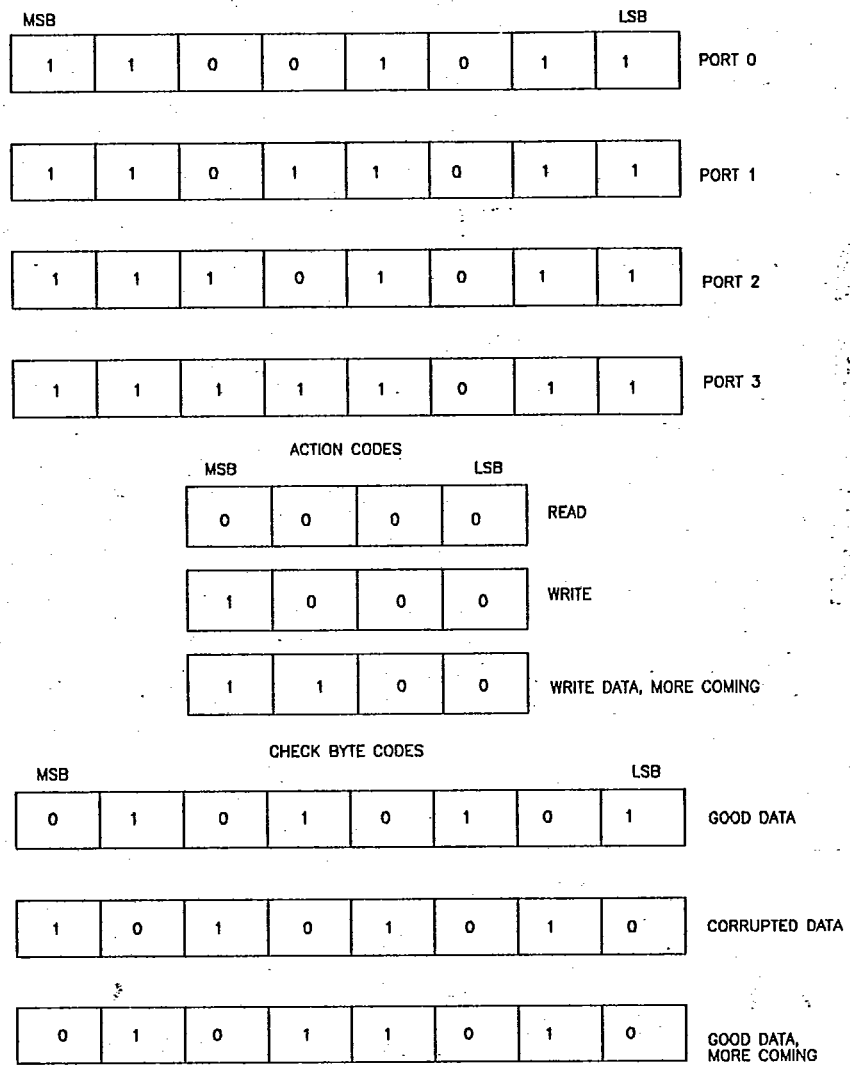


FIGURE 2: QUAD PORT RAM MESSAGE TRANSACTION



NOTE: BITS WHICH ARE SET EQUAL LOGIC ONE.
BITS WHICH ARE CLEAR EQUAL LOGIC ZERO

FIGURE 3: PORT SELECT CODE



data coming. This action code works exactly the same as a standard write message action with one exception. The check byte which follows an eight byte message is driven to a special code which, when read by a receiving port, indicates that more messages will be coming. This information can be used by a receiving port to reduce the overhead of constantly polling for new messages.

Quad Port RAM

As mentioned, each port has direct read and write access to eight message bytes and read access to three groups of eight message bytes. Once the protocol register has been correctly accessed, one of the four sections of the Quad Port will be read or that section of the Quad Port RAM which is dedicated to the transmitting port will be written. When sending a message, all eight message bytes must be written. When receiving a message, all eight of the message bytes should be read. If fewer than all eight bytes are accessed, the message centers may be incorrect and errant communications between ports can result.

Check Byte

A check byte (byte 11) is provided at the end of each of the eight message byte groups. The check byte is read only and provides information to a receiving port. Reading the check byte code is optional and may not be necessary in applications where software discipline is stringent enough to avoid accidental collisions between messages sent and messages received. Three different codes give status to a receiving port about the message which has just been read (Figure 3): good data, corrupted data, and good data with more data coming. When the check byte is read with a good data code, the data which is read by a receiving port is correct and valid. This check byte code assures the receiving port that a sending port is not writing a new message while the receiving port is attempting to read the previous message. When the check byte is read with a corrupted data code, the data which is read by a receiving port is suspect. This check byte warns the receiving port that the sending port is writing a new message while the receiving port is reading an older message. When the check byte is read with a good data and more coming code, the data which is read by a receiving port is correct and valid and additional messages will follow. This check byte code can be used by a receiving port to reduce the overhead of constant polling. If the check byte indicates that a new message will follow, the receiving port is warned to expect a new message.

Polling vs. Message Flags

The DS2015 Quad Port RAM has two methods of warning the sending and receiving ports of impending message status. The software method of polling avoids the complication of additional hardware which is required to connect the message ready pins to a host sending/receiving unit. Polling is accomplished with a receiving unit by satisfying the port select byte of the protocol register and reading the message center. When a port is being polled, care should be taken to avoid entering the execution code portion of the protocol register. When polling a port, communications can be terminated by taking the $\overline{RST}$ input signal low. An alternate method of alerting a host sending/receiving unit of impending message status is to use the message ready signals to interrupt when a message is ready to be read. The message ready pins ($\overline{M0}$-$\overline{M3}$) are driven to an active state (low) when a sending port has written the last bit of the eight message bytes and $\overline{RST}$ of the sending port is set to the inactive state (low),

provided the appropriate destination bit is set. When the message ready pin is set to an active state, a receiving unit can execute a software routine to service the interrupt and read the pending message.

$\overline{RST}$ Control

All message transactions are initiated by driving the $\overline{RST}$ port input high. The $\overline{RST}$ input serves two functions. First, it turns on control logic which allows access to the protocol register. Second, the $\overline{RST}$ signal provides a method of terminating message transfer. Care must be taken when terminating a message transfer to avoid errant information in the message center. The following rules will avoid all problems.

1. While polling the message center for new messages, always terminate the transaction by driving $\overline{RST}$ low after completing a read of the message center byte and before entering the execution code byte.

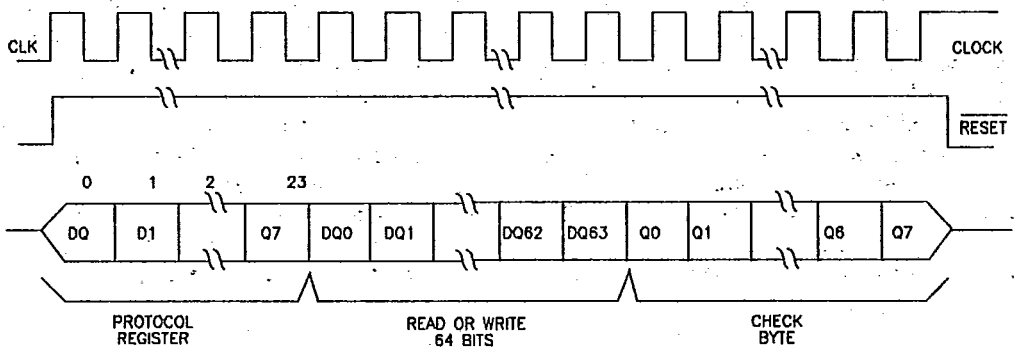
2. When sending a message, all eight messsage bytes must be written. If fewer than eight bytes are written, the mailbox bit of the destination port(s) may not be set and the check byte may indicate corrupted data.

3. When receiving a message, all eight bytes should be read. However, if $\overline{RESET}$ is used to terminate a message which is being read, the message sent bit and the mailbox bit are cleared as $\overline{RST}$ is driven low. When reading a message, the check byte is optional and can be either read or ignored.

Clock Control

A clock cycle is a sequence of a falling edge followed by a rising edge. For message inputs, the data must be valid during the rising edge of the clock cycle. Protocol bits and message bits are input on the rising edge of the clock. Protocol bits and message bits are output on the falling edge of the clock. All message transfer terminates if $\overline{RST}$ is low and the D/Q pins will then go to a high impedance state. When message transfer is terminated using $\overline{RST}$, the transition of $\overline{RST}$ must occur while the clock is at high level to avoid disturbing the last bit of data. Figure 4 illustrates message transfer.

FIGURE 4: QUAD PORT MESSAGE TRANSFER



ABSOLUTE MAXIMUM RATINGS*

Voltage on a pin to ground: -1.0 to + 7.0V
Operating temperature: 0°C to 70°C
Storage temperature: -55°C to + 125°C

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Logic 1	V_{IH}	2.0		Vcc+0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	Vcc	4.5	5.0	5.5	V	1

D.C ELECTRICAL CHARACTERISTICS

(0°C to 70°C, Vcc = 5V+/- 10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Leakage	I_{IL}	-1		1	uA	
Output Leakage	I_{LO}			1	uA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ .4V	I_{OL}	+4			mA	
Supply Current	I_{CC}			6	mA	2

CAPACITANCE

(T_A=25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_N	5	pF	
Output Capacitance	C_{OUT}	7	pF	

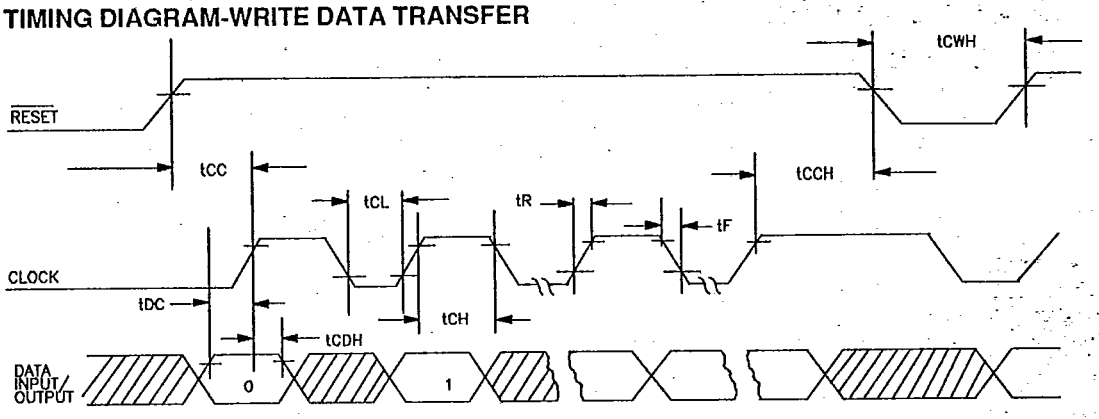
A.C ELECTRICAL CHARACTERISTICS

(0°C to 70°C, Vcc = 5V+/- 10%)

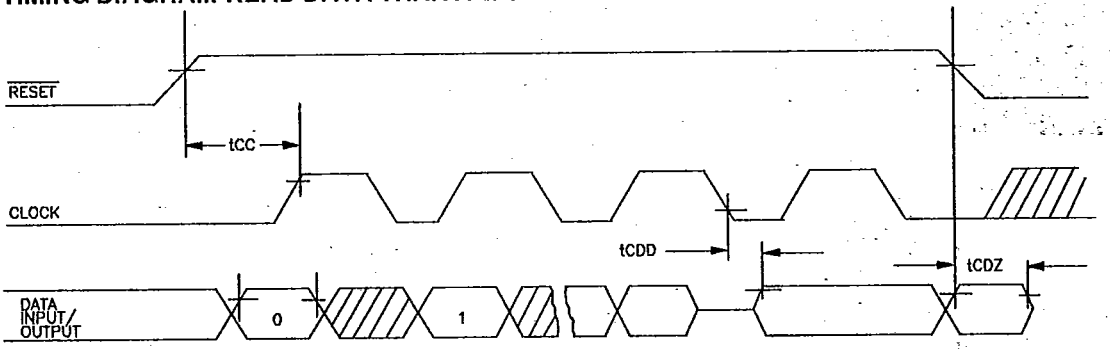
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	
CLK to Data Hold	t_{CDH}	40			ns	
CLK to Data Delay	t_{CDD}			125	ns	
CLK Low Time	t_{CL}	125			ns	
CLK High Time	t_{CH}	125			ns	
CLK Frequency	f_{CLK}	D.C		4.0	MHZ	
CLK Rise and Fall	t_R,t_F			500	ns	
$\overline{RST}$ to CLK Set Up	t_{CC}	1			us	
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	
$\overline{RST}$ to I/O High Z	t_{CDZ}			50	ns	
$\overline{RST}$ to Message Ready	t_{RF}			100	ns	

QUAD SERIAL PORT RAM TIMING DIAGRAM

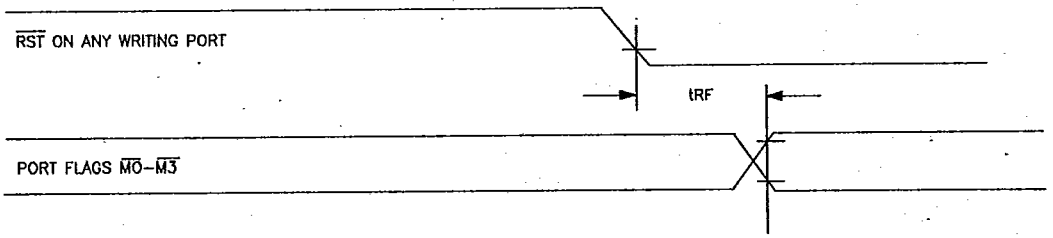
TIMING DIAGRAM-WRITE DATA TRANSFER



TIMING DIAGRAM-READ DATA TRANSFER



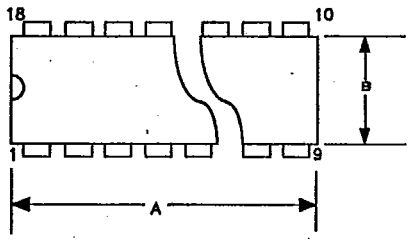
TIMING DIAGRAM-MESSAGE READY



Notes

1. All voltages are referenced to ground.
2. All outputs are open.

DS2015
Quad Port Serial RAM
18 Pin DIP



DIM.	INCHES	
	MIN.	MAX.
A	0.860	0.940
B	0.240	0.260
C	0.120	0.140
D	0.290	0.310
E	0.020	0.040
F	0.110	0.130
G	0.090	0.110
H	.320	.370
J	0.008	0.012
K	0.015	0.021