ProASIC^{PLUS} Flash Family FPGAs

FlashLock™

Features and Benefits

High Capacity
- 75,000 to 1 million System Gates
- 27k to 198kbits of Two-Port SRAM
- 66 to 712 User I/Os

Reprogrammable Flash Technology
- 0.22µ 4LM Flash-based CMOS Process
- Live at Power-Up, Single-Chip Solution
- No Configuration Device Required
- Retains Programmed Design during Power-Down/Power-Up Cycles

Performance
- 3.3V, 32-bit PCI (up to 50 MHz)
- Two Integrated PLLs
- External System Performance up to 150 MHz

Secure Programming
- The Industry's Most Effective Security Key (FlashLock™) Prevents Read Back of Programming Bitstream

Low Power
- Low Impedance Flash Switches
- Segmented Hierarchical Routing Structure
- Small, Efficient, Configurable (Combinatorial or Sequential) Logic Cells

High Performance Routing Hierarchy
- Ultra-Fast Local and Long-Line Network
- High Speed Very Long-Line Network
- High Performance, Low Skew, Splittable Global Network
- 100% Routability and Utilization

I/O
- Schmitt-Trigger Option on Every Input
- 2.5V/3.3V Support with Individually-Selectable Voltage and Slew Rate
- Bidirectional Global I/Os
- Compliance with PCI Specification Revision 2.2
- Boundary-Scan Test IEEE Std. 1149.1 (JTAG) Compliant
- Pin Compatible Packages across ProASIC^{PLUS} Family

Unique Clock Conditioning Circuitry
- PLL with Flexible Phase, Multiply/Divide and Delay Capabilities
- Internal and/or External Dynamic PLL Configuration
- Two LVPECL Differential Pairs for Clock or Data Inputs

Standard FPGA and ASIC Design Flow
- Flexibility with Choice of Industry-Standard Frontend Tools
- Efficient Design through Frontend Timing and Gate Optimization

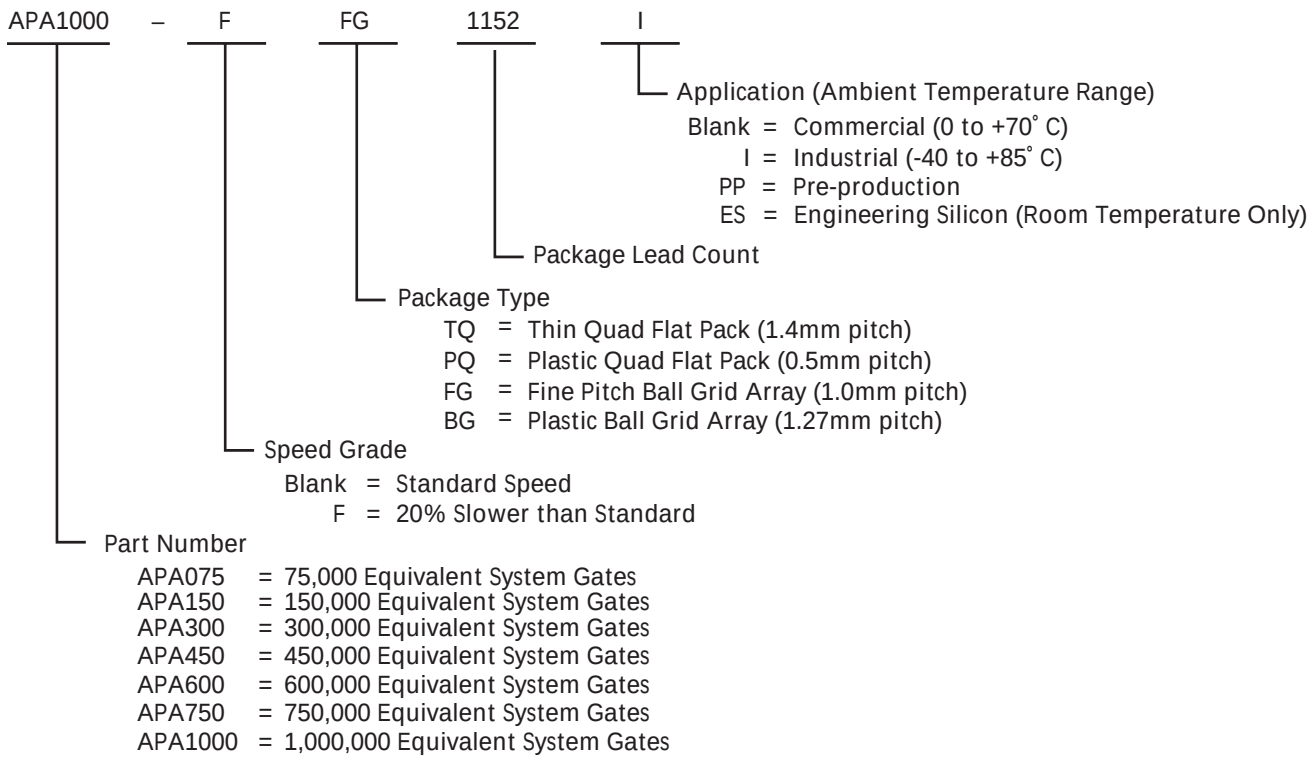
ISP Support
- In-System Programming (ISP) via JTAG Port

SRAMs and FIFOs
- ACTgen Netlist Generation Ensures Optimal Usage of Embedded Memory Blocks
- 24 SRAM and FIFO Configurations with Synchronous and Asynchronous Operation up to 150 MHz (typical)

Table 1 • **ProASIC^{PLUS} Product Profile**

Device	**APA075**	**APA150**	**APA300**	**APA450**	**APA600**	**APA750**	**APA1000**
Maximum System Gates	75,000	150,000	300,000	450,000	600,000	750,000	1,000,000
Maximum Tiles (Registers)	3,072	6,144	8,192	12,288	21,504	32,768	56,320
Embedded RAM Bits (k=1,024 bits)	27k	36k	72k	108k	126k	144k	198k
Embedded RAM Blocks (256x9)	12	16	32	48	56	64	88
LVPECL	2	2	2	2	2	2	2
PLL	2	2	2	2	2	2	2
Global Networks	4	4	4	4	4	4	4
Maximum Clocks	24	32	32	48	56	64	88
Maximum User I/Os	158	242	290	344	454	562	712
JTAG ISP	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Package (by pin count)							
TQFP	100, 144	100	–	–	–	–	–
PQFP	208	208	208	208	208	208	208
PBGA	–	456	456	456	456	456	456
FBGA	144	144, 256	144, 256	144, 256, 484	256, 484, 676	676, 896	896, 1152

Ordering Information



Plastic Device Resources

	User I/Os*									
Device	**TQFP 100-Pin**	**TQFP 144-Pin**	**PQFP 208-Pin**	**PBGA 456-Pin**	**FBGA 144-Pin**	**FBGA 256-Pin**	**FBGA 484-Pin**	**FBGA 676-Pin**	**FBGA 896-Pin**	**FBGA 1152-Pin**
APA075	66	107	158		100					
APA150	66		158	242	100	186				
APA300			158	290	100	186				
APA450			158	344	100	186	344			
APA600			158	356		186	370	454		
APA750			158	356				454	562	
APA1000			158	356					642	712

Package Definitions

TQFP = Thin Quad Flat Pack, PQFP = Plastic Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array

*Each pair of PECL I/Os were counted as one user I/O.

General Guideline

Maximum performance numbers in this datasheet are based on characterized data. Actel does not guarantee performance beyond the limits specified within the datasheet.

Product Availability

	Speed Grade		Application	
	Std.	–F*	C	I
APA075 Device				
100-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔
144-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔
144-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔
APA150 Device				
100-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔
456-Pin Plastic Ball Grid Array (PBGA)	✔	✔	✔	✔
144-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔
256-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔
APA300 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔
456-Pin Plastic Ball Grid Array (PBGA)	✔	✔	✔	✔
144-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔
256-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔
APA450 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔
456-Pin Plastic Ball Grid Array (PBGA)	✔	✔	✔	✔
144-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔
256-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔
484-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔
APA600 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔
456-Pin Plastic Ball Grid Array (PBGA)	✔	✔	✔	✔
256-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔
484-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔
676-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔
APA750 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔
456-Pin Plastic Ball Grid Array (PBGA)	✔	✔	✔	✔
676-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔
896-Pin Plastic Ball Grid Array (FBGA)	✔	✔	✔	✔
APA1000 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔
456-Pin Plastic Ball Grid Array (PBGA)	✔	✔	✔	✔
896-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔
1152-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔

Notes:

**–F parts are only available as commercial temperature devices.*

Applications: C = Commercial *Availability: ✔= Available*

I = Industrial *PP = Product Planned*

Table of Contents

General Description

The ProASIC^PLUS family of devices, Actel's second generation Flash FPGAs, offers enhanced performance over Actel's ProASIC family. It combines the advantages of ASICs with the benefits of programmable devices through nonvolatile Flash technology. This enables engineers to create high-density systems using existing ASIC or FPGA design flows and tools. In addition, the ProASIC^PLUS family offers a unique clock conditioning circuit based on two on-board phase-locked loops (PLLs). The family offers up to 1 million system gates, supp/ +;,//orted with up to 198kbits of two-port SRAM and up to 712 user I/Os, all providing 50 MHz PCI performance.

Advantages to the designer extend beyond performance. Unlike SRAM-based FPGAs, four levels of routing hierarchy simplify routing, while the use of Flash technology allows all functionality to be live at power-up. No external Boot PROM is required to support device programming. While on-board security mechanisms prevent all access to the program information, reprogramming can be performed in-system to support future design iterations and field upgrades. The device's architecture mitigates the complexity of ASIC migration at higher user volume. This makes ProASIC^PLUS a cost-effective solution for applications in the networking, communications, computing, and avionics markets.

The ProASIC^PLUS family achieves its nonvolatility and reprogrammability through an advanced Flash-based 0.22µm LVCMOS process with four-layers of metal. Standard CMOS design techniques are used to implement logic and control functions, including the PLLs and LVPECL inputs. This results in predictable performance fully compatible with gate arrays.

The ProASIC^PLUS architecture provides granularity comparable to gate arrays. The device core consists of a Sea-of-Tiles™. Each tile can be configured as a flip-flop, latch, or three-input/one-output logic function by programming the appropriate Flash switches. The combination of fine granularity, flexible routing resources, and abundant Flash switches allow 100% utilization and over 95% routability for highly congested designs. Tiles and larger functions are interconnected through a four-level routing hierarchy.

Embedded two-port SRAM blocks with built-in FIFO/RAM control logic can have user-defined depth and width. Users can also select programming for synchronous or asynchronous operation, as well as parity generations or checking.

The unique clock conditioning circuitry in each device includes two clock conditioning blocks. Each block provides a PLL core, delay lines, phase shifts (0°, 90°, 180°, 270°), and clock multipliers/dividers, as well as the circuitry needed to provide bidirectional access to the PLL. The PLL block contains four programmable frequency dividers, which allow the incoming clock signal to be divided by a wide range of factors from 1 to 64. The clock conditioning circuit also delays or advances the incoming reference clock up to 8 ns (in increments of 0.25 ns). The PLL can be configured internally or externally during operation without redesigning or reprogramming the part. In addition to the PLL, there are two LVPECL differential input pairs to accommodate high speed clock and data inputs.

To support customer needs for more comprehensive, lower cost board-level testing, Actel's ProASIC^PLUS devices are fully compatible with IEEE Standard 1149.1 for test access port and boundary-scan test architecture. For more information concerning the Flash FPGA implementation, please refer to the "Boundary Scan (JTAG)" on page 1-10.

ProASIC^PLUS devices are available in a variety of high-performance plastic packages. Those packages and the performance features discussed above are described in more detail in the following sections.

ProASIC^PLUS Architecture

The proprietary ProASIC^PLUS architecture provides granularity comparable to gate arrays.

The ProASIC^PLUS device core consists of a Sea-of-Tiles™ (Figure 1-1). Each tile can be configured as a three-input logic function (e.g., NAND gate, D-Flip-Flop, etc.) by programming the appropriate Flash switch interconnections (Figure 1-2 on page 1-3 and Figure 1-3 on page 1-3). Tiles and larger functions are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Flash switches are programmed to connect signal lines to the appropriate logic cell inputs and outputs. Dedicated high-performance lines are connected as needed for fast, low-skew global signal distribution throughout the core. Maximum core utilization is possible for virtually any design.

ProASIC^PLUS devices also contain embedded two-port SRAM blocks with built-in FIFO/RAM control logic. Programming options include synchronous or asynchronous operation, two-port RAM configurations, user defined depth and width, and parity generation or checking. Please see the "Embedded Memory Configurations" on page 1-20 for more information.

Flash Switch

Unlike SRAM FPGAs, ProASIC^PLUS uses a live on power-up ISP Flash switch as its programming element.

In the ProASIC^PLUS Flash switch, two transistors share the floating gate, which stores the programming information. One is the sensing transistor, which is only used for writing and verification of the floating gate voltage. The other is the switching transistor. It can be used in the architecture to connect/separate routing nets or to configure logic. It is also used to erase the floating gate (Figure 1-2 on page 1-3).

Logic Tile

The logic tile cell (Figure 1-3 on page 1-3) has three inputs (any or all of which can be inverted) and one output (which can connect to both ultra-fast local and efficient long-line routing resources). Any three-input, one-output logic function (except a three-input XOR) can be configured as one tile. The tile can be configured as a latch with clear or set or as a flip-flop with clear or set. Thus, the tiles can flexibly map logic and sequential gates of a design.

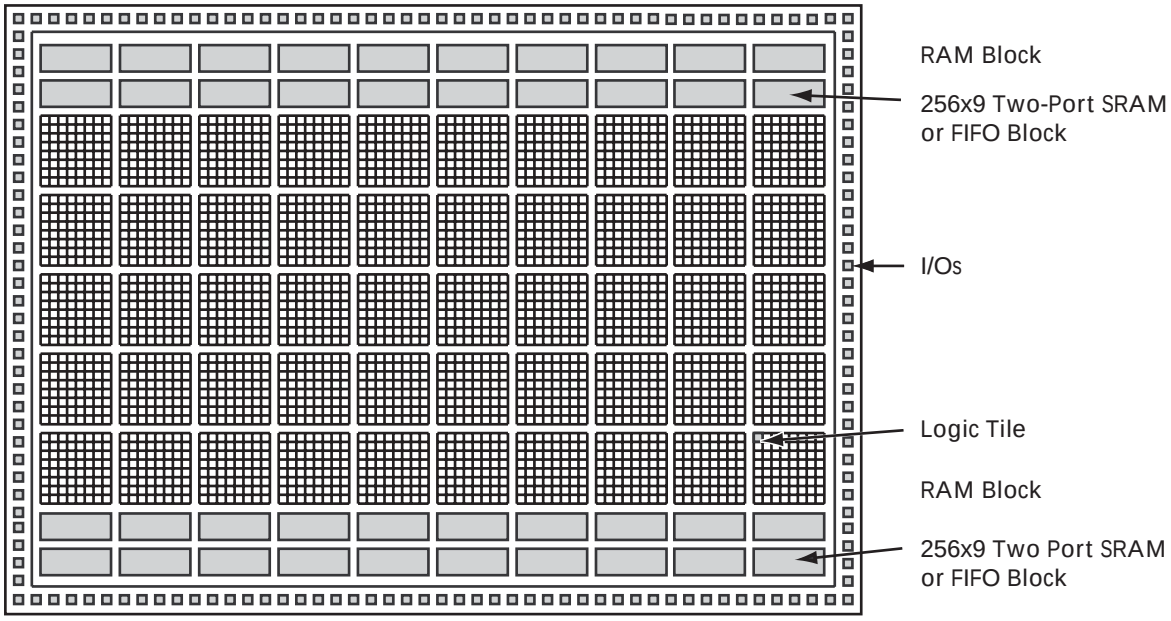


Figure 1-1 • **The ProASIC^PLUS Device Architecture**

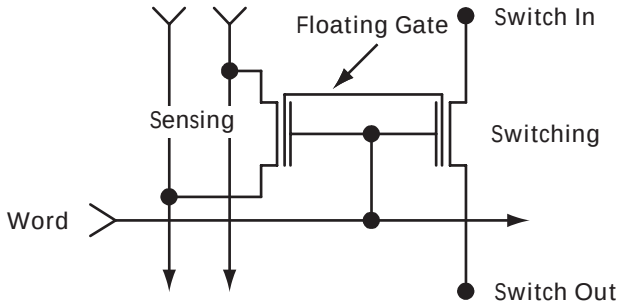


Figure 1-2 • **Flash Switch**

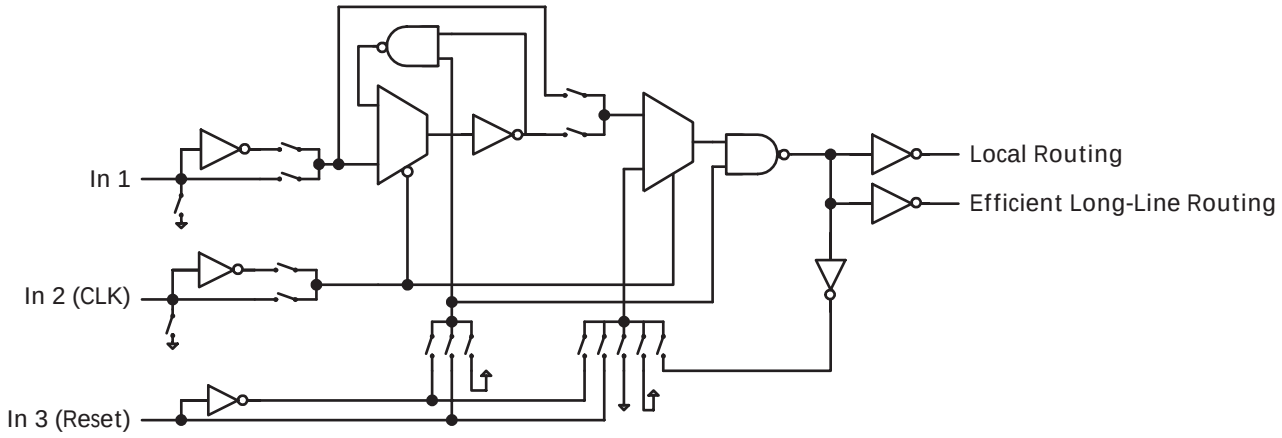


Figure 1-3 • **Core Logic Tile**

Routing Resources

The routing structure of ProASIC^PLUS devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources, efficient long-line resources, high speed very long-line resources, and high performance global networks.

The ultra-fast local resources are dedicated lines that allow the output of each tile to connect directly to every input of the eight surrounding tiles (Figure 1-4 on page 1-4).

The efficient long-line resources provide routing for longer distances and higher fanout connections. These resources vary in length (spanning 1, 2, or 4 tiles), run both vertically and horizontally, and cover the entire ProASIC^PLUS device (Figure 1-5 on page 1-4). Each tile can drive signals onto the efficient long-line resources, which can in turn, access every input of every tile. Active buffers are inserted automatically by routing software to limit the loading effects due to distance and fanout.

The high-speed very long-line resources, which span the entire device with minimal delay, are used to route very long or very high fanout nets. (Figure 1-6 on page 1-5).

The high-performance global networks are low skew, high fanout nets that are accessible from external pins or from internal logic (Figure 1-7 on page 1-6). These nets are typically used to distribute clocks, resets, and other high fanout nets requiring a minimum skew. The global networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically with signals accessing every input on all tiles.

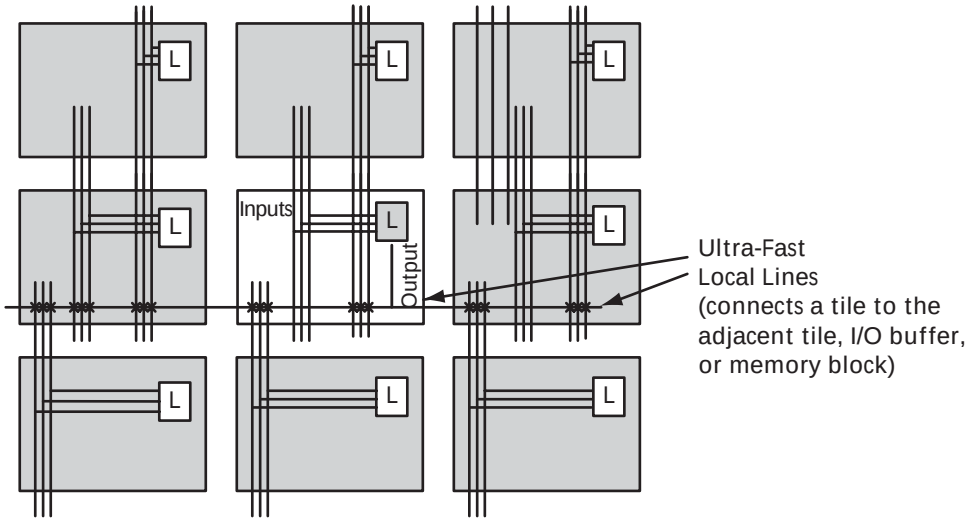


Figure 1-4 • **Ultra-Fast Local Resources**

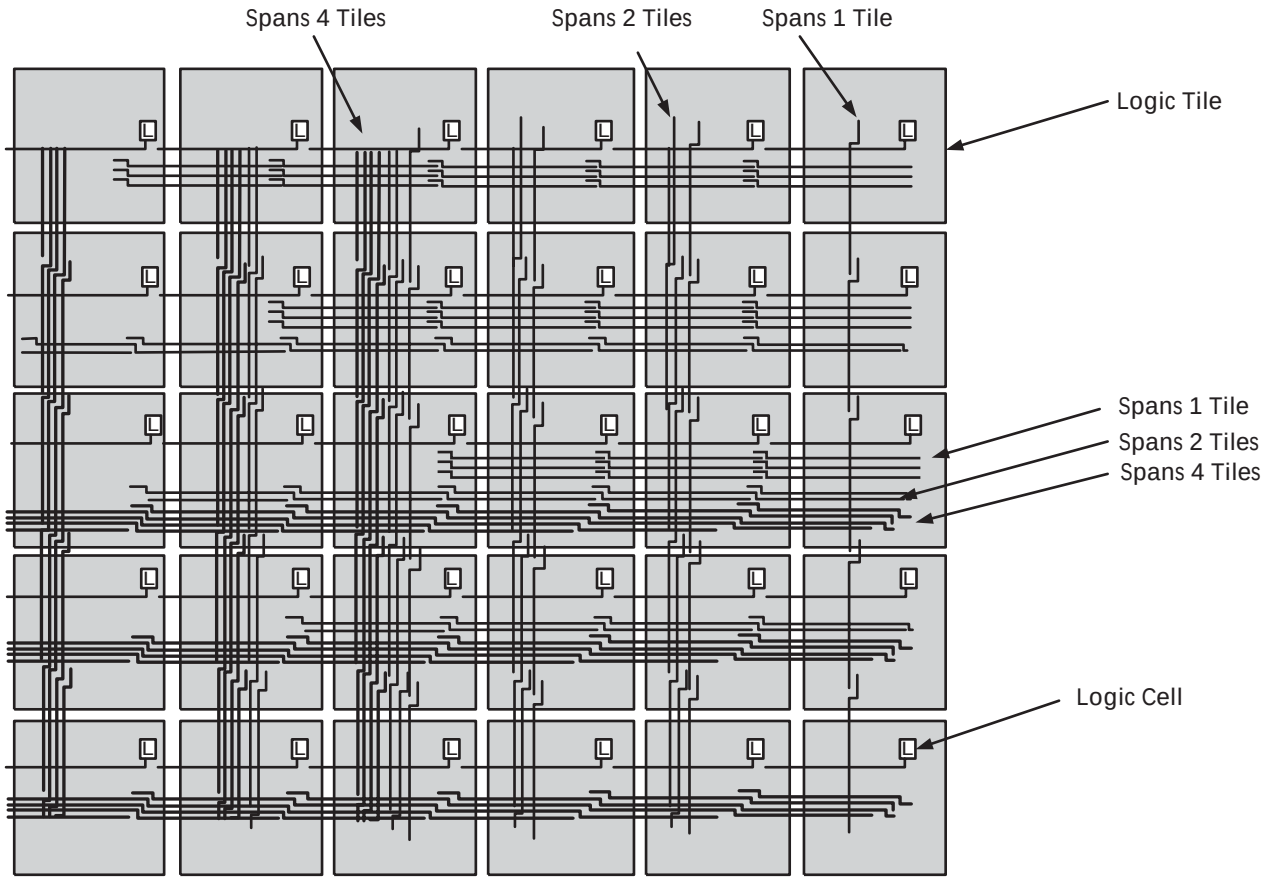


Figure 1-5 • **Efficient Long-Line Resources**

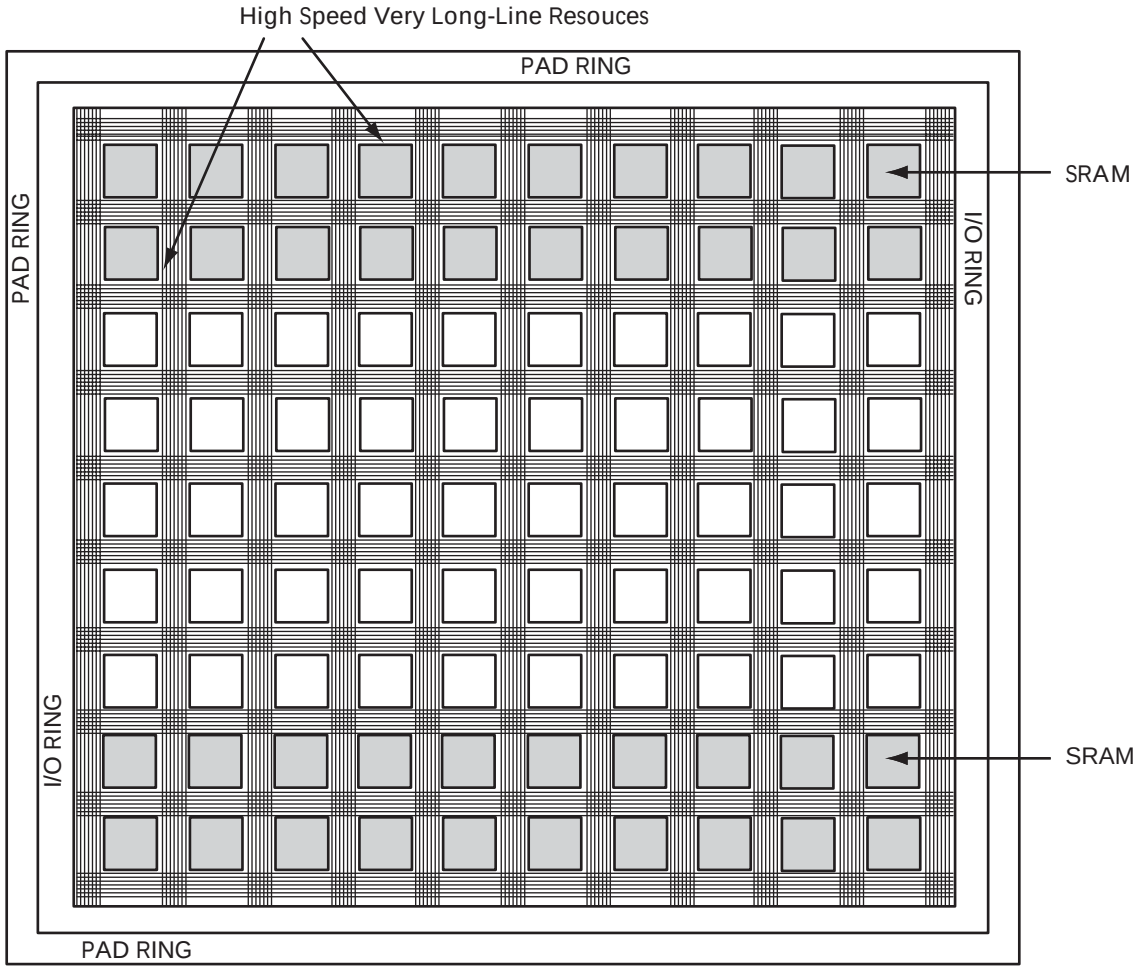


Figure 1-6 • **High Speed Very Long-Line Resources**

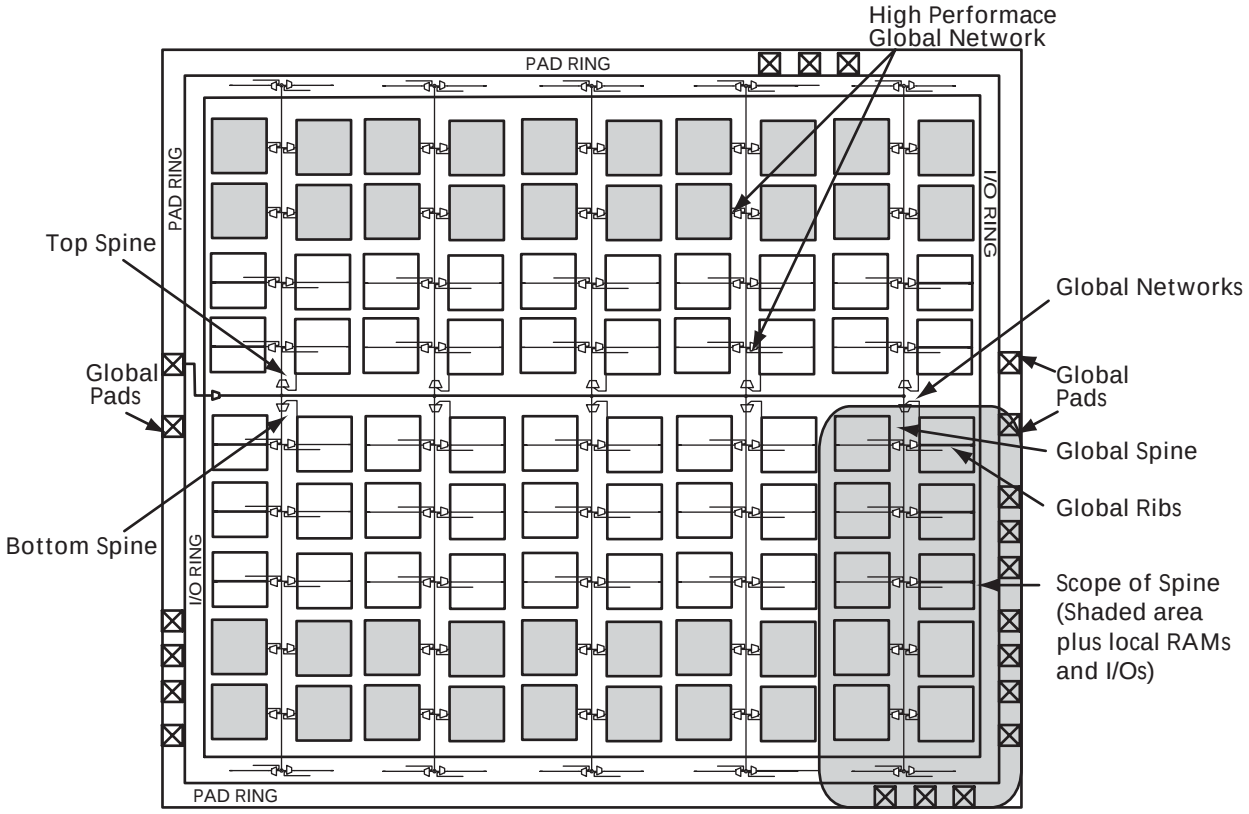
Clock Resources

The ProASIC^PLUS family offers powerful and flexible control of circuit timing through the use of analog circuitry. Each chip has two clock conditioning blocks containing a phase-locked loop (PLL) core, delay lines, phase shifter (0°, 90°, 180°, 270°), clock multiplier/ dividers and all the circuitry needed for the selection and interconnection of inputs to the global network (thus providing bidirectional access to the PLL). This permits the PLL block to drive inputs and/or outputs via the two global lines on each side of the chip (four total lines). This circuitry is discussed in more detail in the "ProASICPLUS Clock Management System" on page 1-11.

Clock Trees

One of the main architectural benefits of ProASIC^PLUS is the set of power and delay friendly global networks. ProASIC^PLUS offers four global trees. Each of these trees is based on a network of spines and ribs that reach all the tiles in their regions (Figure 1-7 on page 1-6). This flexible clock tree architecture allows users to map up to 88 different internal/external clocks in an APA1000 device. Details on the clock spines and various numbers of the family are given in Table 1-1 on page 1-6.

The flexible use of the ProASIC^PLUS clock spine allows the designer to cope with several design requirements. Users implementing clock-resource intensive applications can easily route external or gated internal clocks using global routing spines. Users can also drastically reduce delay penalties and save buffering resources by mapping critical high-fanout nets to spines. For design hints on using these features, refer to Actel's *Efficient Use of ProASIC Clock Trees* application note.



Note: *This figure shows routing for only one global path.*

Figure 1-7 • **High Performance Global Network**

Table 1-1 • **Clock Spines**

	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
Global Clock Networks (Trees)	4	4	4	4	4	4	4
Clock Spines/Tree	6	8	8	12	14	16	22
Total Spines	24	32	32	48	56	64	88
Top or Bottom Spine Height (Tiles)	16	24	32	32	48	64	80
Tiles in Each Top or Bottom Spine	512	768	1,024	1,024	1,536	2,048	2,560
Total Tiles	3,072	6,144	8,192	12,288	21,504	32,768	56,320

Array Coordinates

During many place-and-route operations in Actel's Designer software tool, it is possible to set constraints that require array coordinates.

Table 1-2 on page 1-7 is provided as a reference. The array coordinates are measured from the lower left (0,0). They can be used in region constraints for specific groups, designated by a wildcard, and containing core cells, I/Os, and memories.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and core cells. In addition, the I/O coordinate system changes depending on the die/package combination.

Core cell coordinates start at the lower left corner (1,1) or (1,5) if memories are present at the bottom. Memory coordinates use the same system and are indicated in Table 1-2 on page 1-7. The memory coordinates for an APA1000 are illustrated in Figure 1-8 on page 1-7. For more information on how to use constraints, see the *Designer User's Guide* or online help for ProASIC^PLUS software tools.

Table 1-2 • **Array Coordinates**

	Logic Tile				Memory Rows		All	
	Min.		Max.		Bottom	Top		
Device	**x**	**y**	**x**	**y**	**y**	**y**	**Min.**	**Max.**
APA075	1	1	96	32	–	(33,33) or (33, 35)	0,0	97, 37
APA150	1	1	128	48	–	(49,49) or (49, 51)	0,0	129, 53
APA300	1	5	128	68	(1,1) or (1,3)	(69,69) or (69, 71)	0,0	129, 73
APA450	1	5	192	68	(1,1) or (1,3)	(69,69) or (69, 71)	0,0	193, 73
APA600	1	5	224	100	(1,1) or (1,3)	(101,101) or (101, 103)	0,0	225, 105
APA750	1	5	256	132	(1,1) or (1,3)	(133,133) or (133, 135)	0,0	257, 137
APA1000	1	5	352	164	(1,1) or (1,3)	(165,165) or (165, 167)	0,0	353, 169

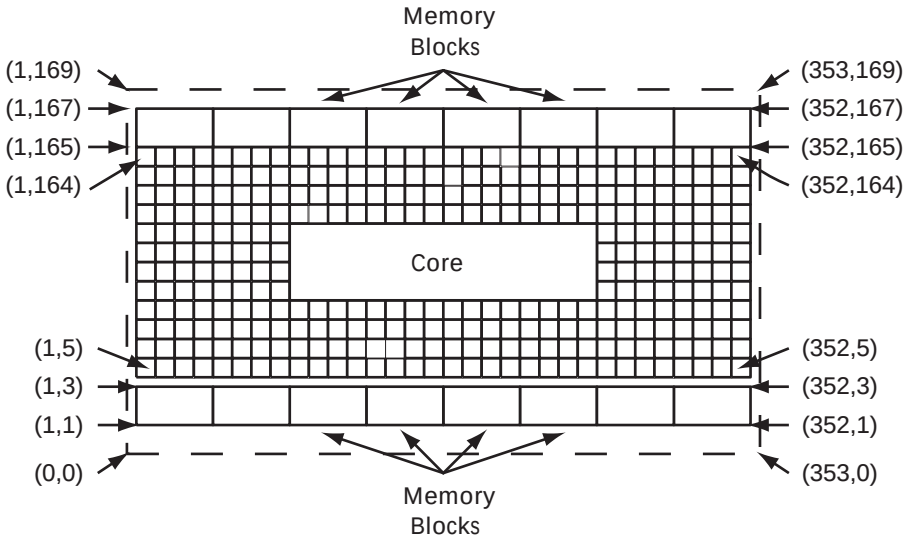


Figure 1-8 • **Core Cell Coordinates for the APA1000**

Input/Output Blocks

To meet complex system demands, the ProASIC^PLUS family offers devices with a large number of user I/O pins, up to 712 on the APA1000. If the I/O pad power supply (V_{DDP}) is 3.3V, each I/O can be selectively configured at the 2.5V and 3.3V threshold levels[1]. Table 1-3 shows the available supply voltage configurations (the PLL block uses an independent 2.5V supply on the AVDD and AGND pins). All I/Os include ESD protection circuits. Each I/O has been tested to 2000V to the human body model (per JESD22 (HBM)).

Table 1-3 • **ProASIC^PLUS I/O Power Supply Voltages**

	V_{DDP}	
	2.5V	**3.3V**
Input Compatibility	2.5V	3.3V, 2.5V
Output Drive	2.5V	3.3V, 2.5V[1]

Note: *V_{DD} is always 2.5V.*

1. Please refer to the mixed-mode interfacing section in the I/O Features in ProASIC^PLUS Flash FPGAs application note for details.

Six or seven standard I/O pads are grouped with a GND pad and either a V_{DD} (core power) or V_{DDP} (I/O power) pad. Two reference bias signals circle the chip. One protects the cascaded output drivers, while the other creates a virtual V_{DD} supply for the I/O ring.

I/O pads are fully configurable to provide the maximum flexibility and speed. Each pad can be configured as an input, an output, a tristate driver, or a bidirectional buffer (Figure 1-9 and Table 1-4).

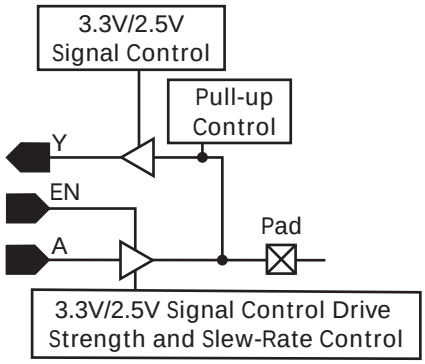


Figure 1-9 • **I/O Block Schematic Representation**

Table 1-4 • **I/O Features**

Function	Description
I/O pads configured as inputs	• Individually selectable 2.5V or 3.3V threshold levels • Optional pull-up resistor • Optionally configurable as Schmitt trigger input. The Schmitt trigger input option can be configured as an input only, not a bidirectional buffer. This input type may be slower than a standard input under certain conditions and has a typical hysteresis of 0.35V. I/O macros with an "S" in the standard I/O library have added Schmitt capabilities. • 3.3V PCI Compliant
I/O pads configured as outputs	• Individually selectable 2.5V or 3.3V compliant output signals • 2.5V – JEDEC JESD 8-5 • 3.3V – JEDEC JESD 8-A (LVTTL and LVCMOS) • 3.3V PCI compliant • Ability to drive LVTTL and LVCMOS levels • Selectable drive strengths • Selectable slew rates • Tristate
I/O pads configured as bidirectional buffers	• Individually selectable 2.5V or 3.3V compliant output signals • 2.5V – JEDEC JESD 8-5 • 3.3V – JEDEC JESD 8-A (LVTTL and LVCMOS) • 3.3V PCI compliant • Optional pull-up resistor • Selectable drive strengths • Selectable slew rates • Tristate

Power-Up Sequencing

While ProASIC^PLUS devices are live at power-up, the order of V_{DD} and V_{DDP} power-up is important during system start-up. V_{DD} should be powered up before (or coincident with) V_{DDP} on ProASIC^PLUS devices. Failure to follow these guidelines may result in undesirable pin behavior during system start-up. For more information, refer to Actel's *ProASIC^PLUS Family Devices Power-Up Behavior* application note.

LVPECL Input Pads

In addition to standard I/O pads and power pads, ProASIC^PLUS devices have a single LVPECL input pad on both the east and west sides of the device, along with AVDD and AGND pins to power the PLL block. The LVPECL pad cell consists of an input buffer (containing a low voltage differential amplifier) and a signal and its complement, PPECL (I/P) (PECLN) and NPECL (PECLREF). The LVPECL input pad cell differs from the standard I/O cell in that it is operated from V_{DD} only.

Since it is exclusively an input, it requires no output signal, output enable signal, or output configuration bits. As a special high-speed differential input, it also does not require pull ups. Recommended termination for LVPECL inputs is shown in Figure 1-10. The LVPECL pad cell compares voltages, as illustrated in Figure 1-11, on the PPECL (I/P) pad and the NPECL pad and sends the results to the global MUX (Figure 1-14 on page 1-13). This high speed, low skew output essentially controls the clock conditioning circuit.

LVPECLs are designed to meet LVPECL JEDEC receiver standard levels (Table 1-5).

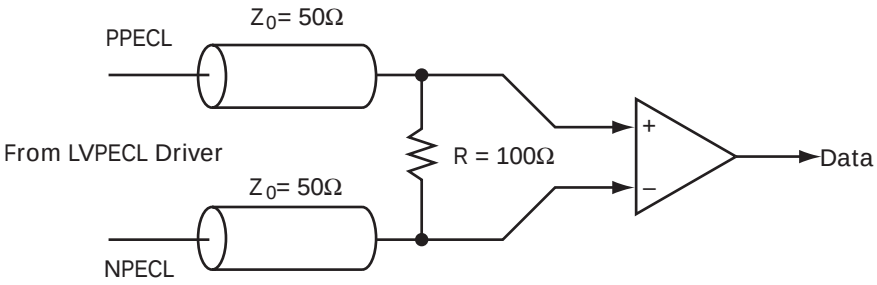


Figure 1-10 • **Recommended Termination for LVPECL Inputs**

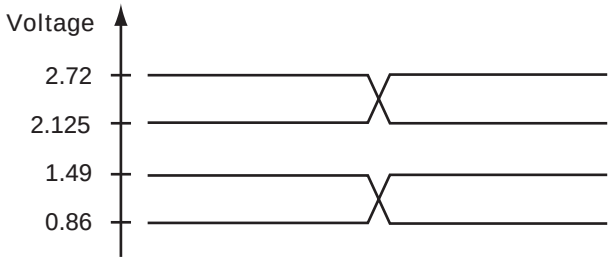


Figure 1-11 • **LVPECL High and Low Threshold Values**

Table 1-5 • **LVPECL Receiver Specifications**

Symbol	Parameter	Min.	Max	Units
V_{IH}	Input High Voltage	1.49	2.72	V
V_{IL}	Input Low Voltage	0.86	2.125	V
V_{ID}	Differential Input Voltage	0.3	V_{DD}	V

Boundary Scan (JTAG)

ProASIC^PLUS devices are compatible with IEEE Standard 1149.1, which defines a set of hardware architecture and mechanisms for cost-effective board-level testing. The basic ProASIC^PLUS boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers, and instruction register (Figure 1-12). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS) and the optional IDCODE instruction (Table 1-6).

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI and TDO (test data input and output), TMS (test mode selector) and TRST (test reset input). TMS, TDI and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary-scan test usage. Actel recommends that a nominal 20kΩ pull-up resistor is added to TDO and TCK pins.

The TAP controller is a four-bit state machine (16 states) that operates as shown in Figure 1-13 on page 1-11. The ’1’s and ‘0’s represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

ProASIC^PLUS devices have to be programmed at least once for complete boundary-scan functionality to be available. If boundary-scan functionality is required prior to partial programming, refer to online technical support on the Actel website and search for ProASIC^PLUS BSDL.

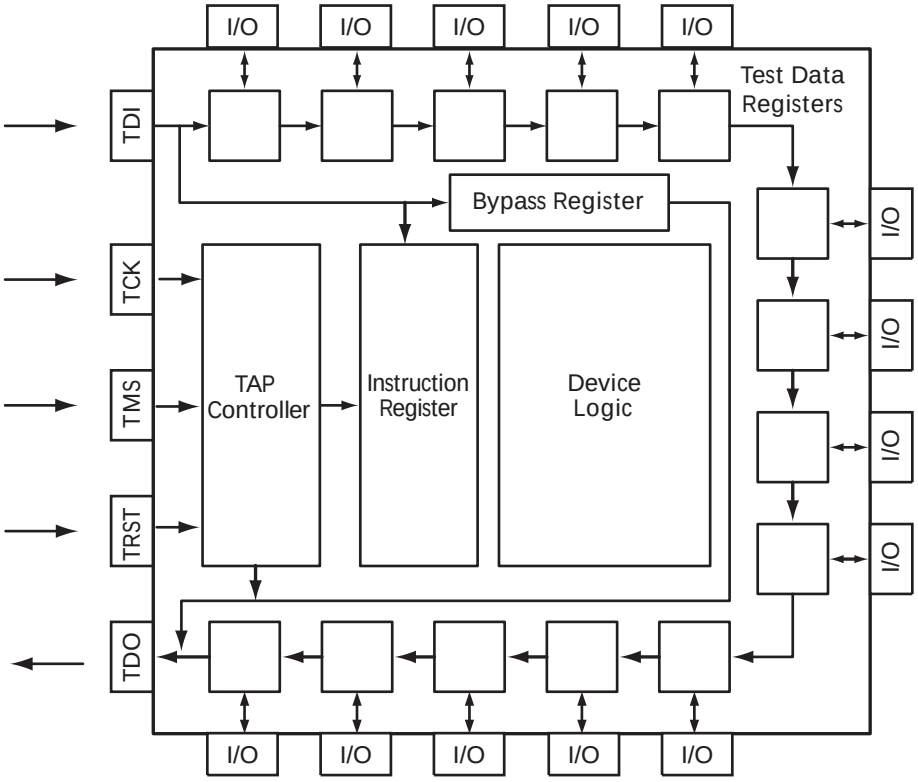


Figure 1-12 • **ProASIC^PLUS JTAG Boundary Scan Test Logic Circuit**

Table 1-6 • **Boundary-Scan Opcodes**

	Hex Opcode
EXTEST	00
SAMPLE/PRELOAD	01
IDCODE	0F
CLAMP	05
BYPASS	FF

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles. The TRST pin may also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

ProASIC^PLUS devices support three types of test data registers: bypass, device identification, and boundary

scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (lowest significant byte (LSB), ID number, part number and version). The boundary-scan register observes and controls the state of each I/O pin.

Each I/O cell has three boundary-scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin. The serial pins are used to serially connect all the boundary-scan register cells in a device into a boundary-scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

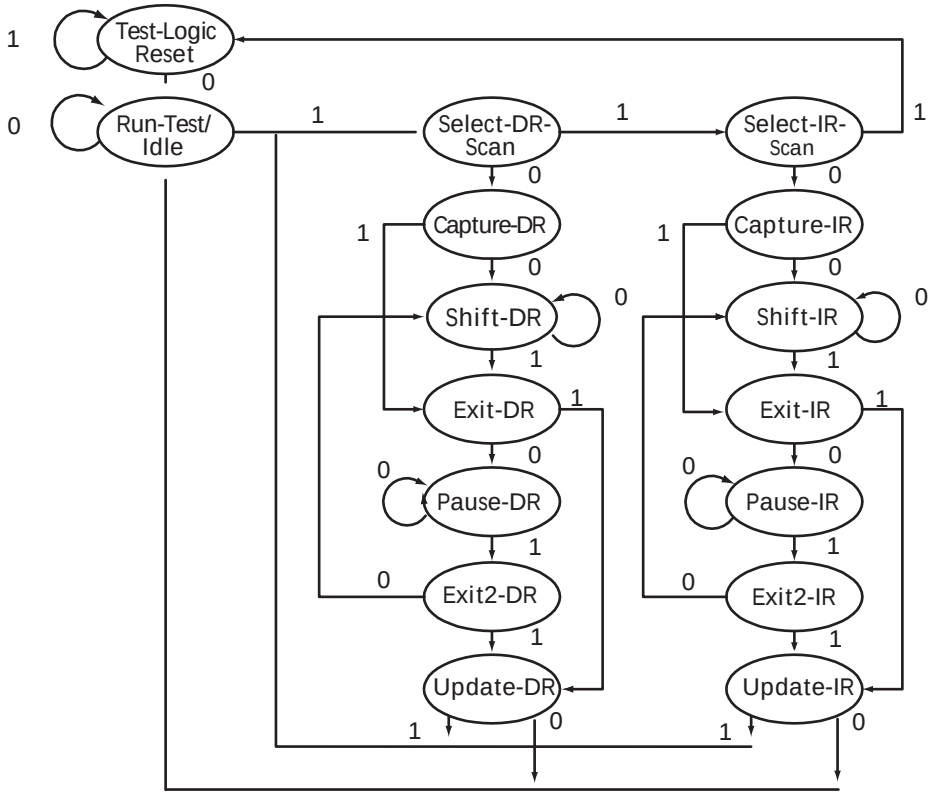


Figure 1-13 • **TAP Controller State Diagram**

Timing Control and Characteristics

ProASIC^PLUS Clock Management System

Introduction

ProASIC^PLUS devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC^PLUS family contains two phase-locked loop (PLL) blocks which perform the following functions:

- Clock Phase Adjustment via Programmable Delay (250 ps steps from –8 ns to +8 ns)
- Clock Skew Minimization
- Clock Frequency Synthesis

Each PLL has the following key features:

- Input Frequency Range (f_{IN}) = 1.5 to 180 MHz
- Feedback Frequency Range (f_{VCO}) = 1.5 to 180 MHz
- Output Frequency Range (f_{OUT}) = 6 to 180 MHz
- Output Phase Shift = 0 °, 90 °, 180 °, and 270 °
- Output Duty Cycle = 50%
- Low Output Jitter (max at 25°C)
  - f_{VCO} <10 MHz. Jitter ±1% or better

- 10 MHz < f_{VCO} < 60 MHz. Jitter ±2% or better
- f_{VCO} > 60 MHz. Jitter ±1% or better

Note: Jitter(ps) = Jitter(%)*(10/Frequency (MHz))

For Example:
Jitter in picoseconds at 1 MHz = 1(%)*(10/1 (MHz)) = 10ps

- Maximum Acquisition Time = 80µs
- Low Power Consumption – 6.9 mW (max – analog supply) + 7.0µW/MHz (max – digital supply)

Physical Implementation

Each side of the chip contains a clock conditioning circuit based upon a 180 MHz PLL block (Figure 1-14 on page 1-13). Two global multiplexed lines extend along each side of the chip to provide bidirectional access to the PLL on that side (neither MUX can be connected to the opposite side's PLL). Each global line has optional LVPECL input pads (described below). The global lines may be driven by either the LVPECL global input pad or the outputs from the PLL block or both. Each global line can be driven by a different output from the PLL. Unused global pins can be configured as regular I/Os or left unconnected. They default to an input with pull-up. The two signals available to drive the global networks are as follows (Figure 1-15 on page 1-14, Table 1-7 on page 1-14, and Table 1-8 on page 1-15):

Global A (secondary clock)

- Output from Global MUX A
- Conditioned version of PLL output (f_{OUT}) – delayed or advanced
- Divided version of either of the above
- Further delayed version of either of the above (0.25 ns, 0.50 ns, or 4.00 ns delay)[1]

Global B

- Output from Global MUX B
- Delayed or advanced version of f_{OUT}
- Divided version of either of the above
- Further delayed version of either of the above (0.25 ns, 0.50 ns, or 4.00 ns delay)[1]

Functional Description

Each PLL block contains four programmable dividers as shown in Figure 1-14 on page 1-13. These allow frequency scaling of the input clock signal as follows:

- The n divider divides the input clock by integer factors from 1 to 32.
- The m divider in the feedback path allows multiplication of the input clock by integer factors ranging from 1 to 64.
- The two dividers together can implement any combination of multiplication and division resulting in a clock frequency between 24 and 180 MHz exiting the PLL core. This clock has a fixed 50% duty cycle.
- The output frequency of the PLL core is given by the following formula (f_{REF} is the reference clock frequency):

$$f_{OUT} = f_{REF} * m/n$$

- The third and fourth dividers (u and v) permit the signals applied to the global network to each be further divided by integer factors ranging from 1 to 4.

The implementations:

$$f_{GLB} = m/(n*u)$$

$$f_{GLA} = m/(n*v)$$

enable the user to define a wide range of frequency multipliers and divisors. The clock conditioning circuit can advance or delay the clock up to 8 ns (in increments of 0.25 ns) relative to the positive edge of the incoming reference clock. The system also allows for the selection of output frequency clock phases of 0°, 90°, 180°, and 270°.

Prior to the application of signals to the rib drivers, they pass through programmable delay units, one per global network. These units permit the delaying of global signals relative to other signals to assist in the control of input set-up times. Not all possible combinations of input and output modes can be used. The degrees of freedom available in the bidirectional global pad system and in the clock conditioning circuit have been restricted. This avoids unnecessary and unwieldy design kit and software work.

Lock Signal

An active-high Lock signal (added via the ACTgen PLL development tool) indicates that the PLL has locked to the incoming clock signal. Users can employ the Lock signal as a soft reset of the logic driven by GLB and/or GLA.

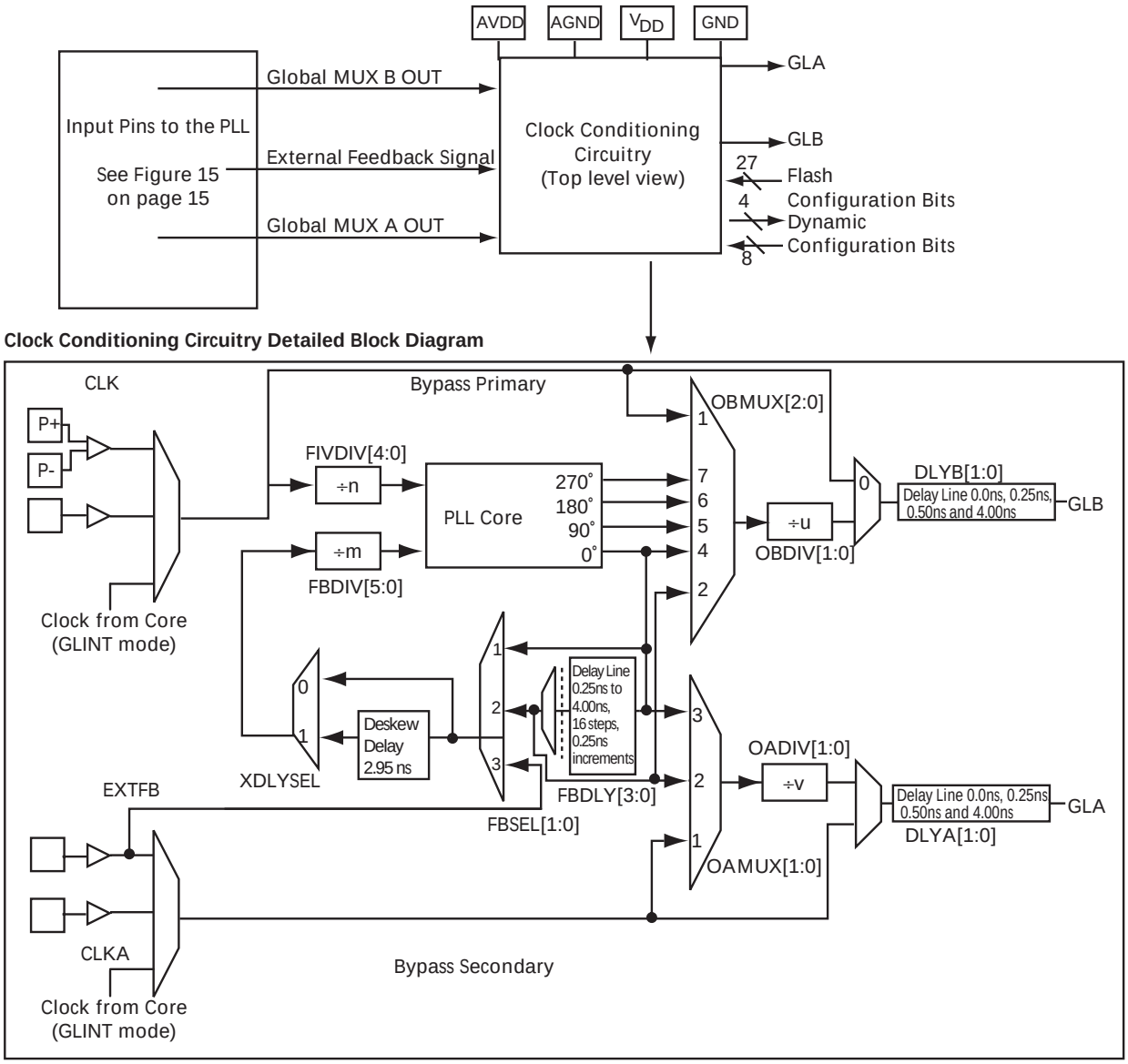
PLL Configuration Options

The PLL can be configured during design (via Flash-configuration bits set in the programming bitstream) or dynamically during device operation, thus eliminating the need for complete reprogramming. The dynamic configuration bits are loaded into a serial-in/parallel-out shift register provided in the clock conditioning circuit of

1. *This mode is available through the delay feature of the Global MUX driver.*

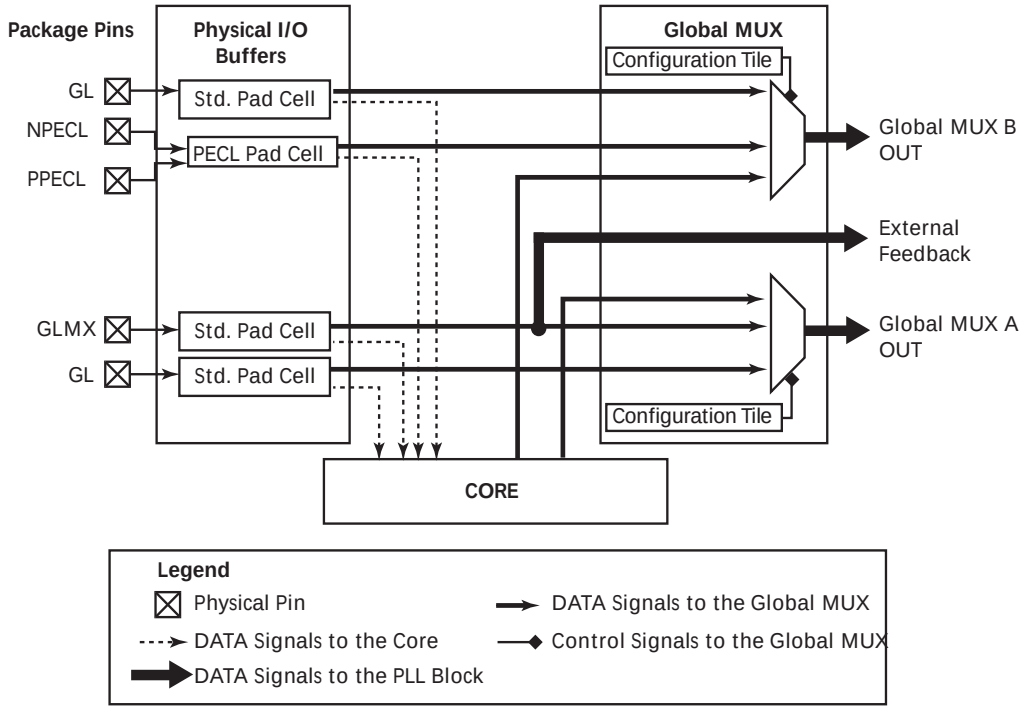
each PLL and then latched into the PLL block. The JTAG ports can be used along with a built-in user JTAG interface hardware to load the configuration shift register externally. Another option is internal dynamic configuration via user-designed hardware. Refer to Actel's *ProASIC^PLUS PLL Dynamic Reconfiguration Using JTAG* application note for more information.

For information on the clock conditioning circuit, refer to Actel's *Using ProASIC^PLUS Clock Conditioning Circuits* application note..



1. FBDLY is a programmable delay line from 0 to 4 ns in 250 ps increments.
2. DLYA, DLYB, DLYAFB are programmable delay lines, each with selectable values 0, 250 ps, 500 ps, and 4 ns.
3. OBDIV will also divide the phase-shift since it takes place after the PLL Core.

Figure 1-14 • **PLL Block – Top-Level View and Detailed PLL Block Diagram**



Note: *When a signal from an I/O tile is connected to the core, it cannot be connected to the Global MUX at the same time.*

Figure 1-15 • **Input Connectors to ProASIC^PLUS Clock Conditioning Circuitry**

Table 1-7 • **Clock-Conditioning Circuitry MUX Settings**

MUX	Datapath	Comments
FBSEL		
1	Internal Feedback	
2	Internal Feedback and Advance Clock Using FBDLY	–0.25 to –4 ns in 0.25ns increments
3	External Feedback (EXTFB)	
XDLYSEL		
0	Feedback Unchanged	
1	Deskew feedback by advancing clock by system delay	Fixed delay of -2.95 ns
OBMUX	**GLB**	
0	Primary bypass, no divider	
1	Primary bypass, use divider	
2	Delay Clock Using FBDLY	+0.25 to +4 ns in 0.25ns increments
4	Phase Shift Clock by 0°	
5	Phase Shift Clock by +90°	
6	Phase Shift Clock by +180°	
7	Phase Shift Clock by +270°	
OAMUX	**GLA**	
0	Secondary bypass, no divider	
1	Secondary bypass, use divider	
2	Delay Clock Using FBDLY	+0.25 to +4 ns in 0.25ns increments
3	Phase Shift Clock by 0°	

Table 1-8 • **Clock-Conditioning Circuitry Delay-Line Settings**

Delay Line	Delay Value (ns)
DLYB	
0	0
1	+0.25
2	+0.50
3	+4.0
DLYA	
0	0
1	+0.25
2	+0.50
3	+4.0

Sample Implementations

Frequency Synthesis

Figure 1-16 on page 1-16 illustrates an example where the PLL is used to multiply a 33 MHz external clock up to 133 MHz. Figure 1-17 on page 1-16 uses two dividers to synthesize a 50 MHz output clock from a 40 MHz input reference clock. The input frequency of 40 MHz is multiplied by 5 and divided by 4, giving an output clock (GLB) frequency of 50 MHz. When dividers are used, a given ratio can be generated in multiple ways, allowing the user to stay within the operating frequency ranges of the PLL. For example, in this case the input divider could have been 2 and the output divider also 2, giving us a division of the input frequency by 4 to go with the feedback loop division (effective multiplication) by 5.

Adjustable Clock Delay

Figure 1-18 on page 1-17 illustrates the delay of the input clock by employing one of the adjustable delay lines. This is easily done in ProASIC^PLUS by bypassing the PLL core entirely and using the output delay line. Notice also that the output clock can be effectively advanced relative to the input clock by using the delay line in the feedback path. This is shown in Figure 1-19 on page 1-17.

Clock Skew Minimization

Figure 1-20 on page 1-18 indicates how feedback from the clock network can be used to create minimal skew between the distributed clock network and the "input" clock. The input clock is fed to the reference clock input of the PLL. The output clock (GLA) feeds a clock network. The feedback input to the PLL uses a clock input delayed by a routing network. The PLL then adjusts the phase of the input clock to match the delayed clock, thus providing nearly zero effective skew between the two clocks. Refer to Actel's *Using ProASIC^PLUS Clock Conditioning Circuits* application note for more information.

Logic Tile Timing Characteristics

Timing characteristics for ProASIC^PLUS devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all ProASIC^PLUS family members. Internal routing delays are device dependent. Design dependency means that actual delays are not determined until after placement and routing of the user's design are complete. Delay values may then be determined by using the Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment prior to placement and routing. Refer to the Actel *Designer User's Guide* or online help for details on using constraints.

Timing Derating

Since ProASIC^PLUS devices are manufactured with a CMOS process, device performance will vary with temperature, voltage, and process. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and optimal process variations. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case process variations (within process specifications).

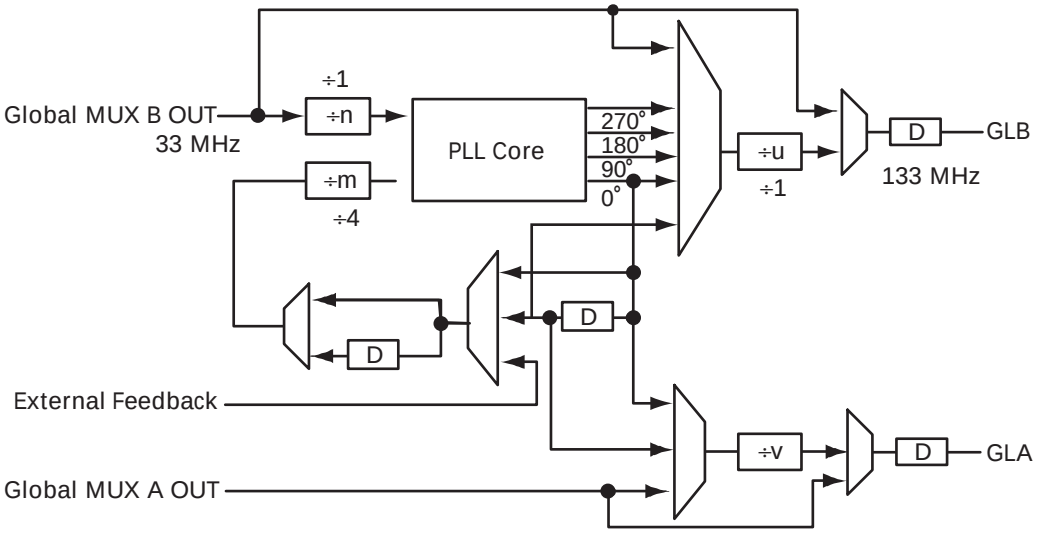


Figure 1-16 • **Using the PLL 33 MHz In, 133 MHz Out**

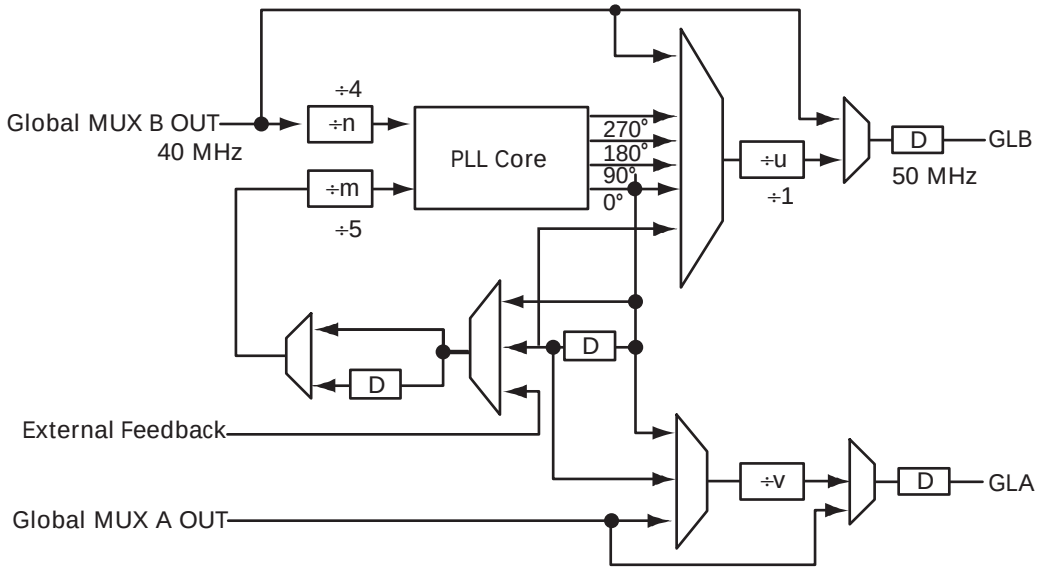


Figure 1-17 • **Using the PLL 40 MHz In, 50 MHz Out**

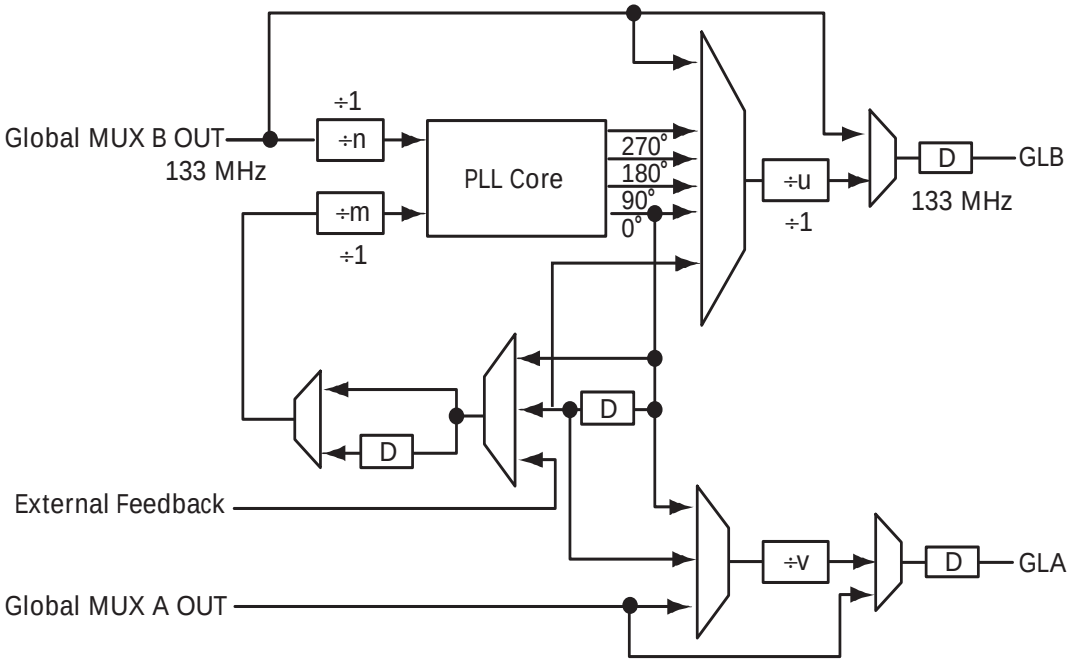


Figure 1-18 • **Using the PLL to Delay the Input Clock**

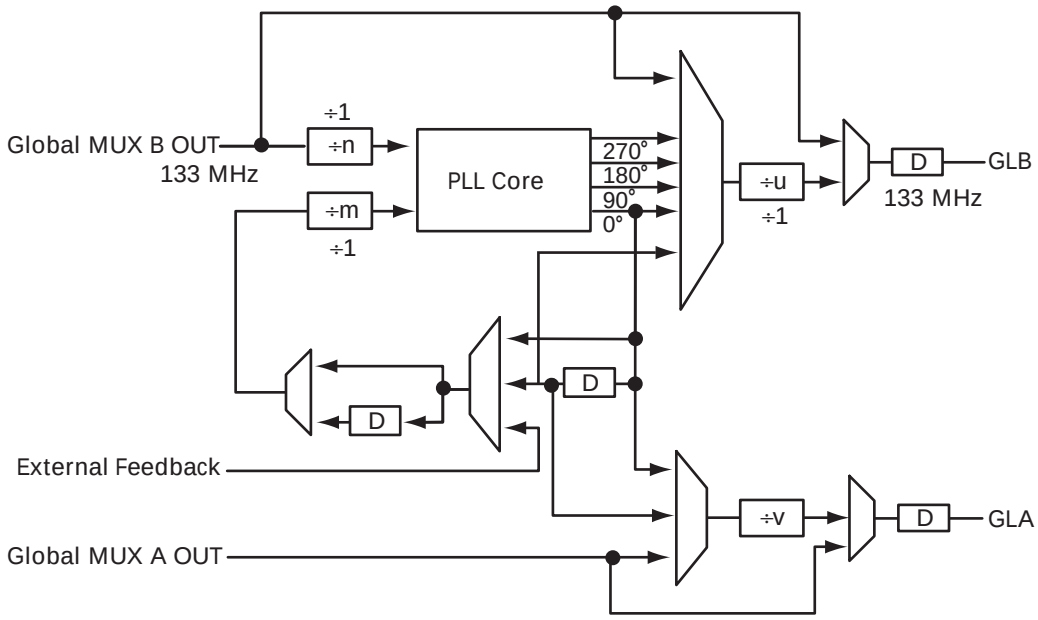


Figure 1-19 • **Using the PLL to "Advance" the Input Clock**

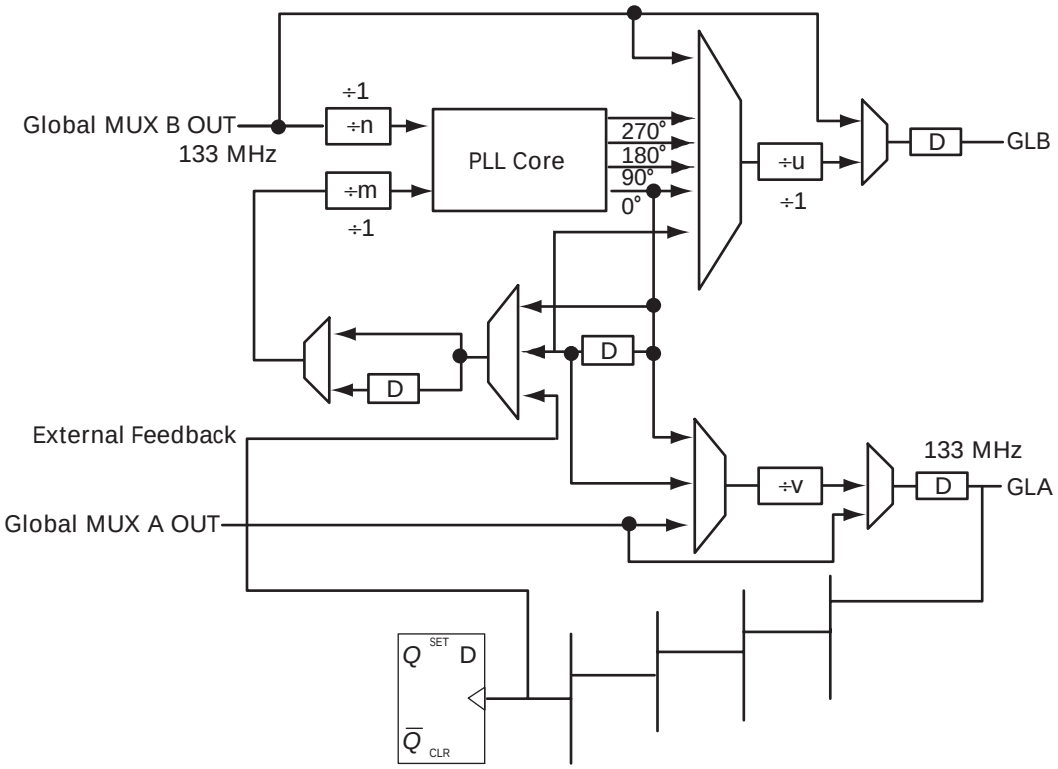


Figure 1-20 • **Using the PLL for Clock De-Skewing**

PLL Electrical Specifications

Parameter	Value	Notes
Frequency Ranges		
Reference Frequency f_{IN} (min.)	1.5 MHz	Clock conditioning circuitry (min.) lowest input frequency
Reference Frequency f_{IN} (max.)	180 MHz	Clock conditioning circuitry (max.) highest input frequency
OSC Frequency f_{VCO} (min.)	24 MHz	Lowest output frequency voltage controlled oscillator
OSC Frequency f_{VCO} (max.)	180 MHz	Highest output frequency voltage controlled oscillator
Clock Conditioning Circuitry f_{OUT} (min.)	6 MHz	Lowest output frequency clock conditioning circuitry
Clock Conditioning Circuitry f_{OUT} (max.)	180 MHz	Highest output frequency clock conditioning circuitry
Long Term Jitter Peak-to-Peak Max.*		
Temperature	**Frequency MHz**	
	f_{VCO}<10 / **10<f_{VCO}<60** / **f_{VCO}>60**	
25°C (or higher)	±1% / ±2% / ±1%	Jitter(ps) = Jitter(%)*(10/Frequency (MHz)) For Example: Jitter in picoseconds at 1 MHz = 1(%)*(10/1 (MHz)) = 10ps
0°C	±1.5% / ±2.5% / ±1%	
–40°C	±2.5% / ±3.5% / ±1%	
Acquisition Time from Cold Start		
Acquisition Time (max.)	30 µs	$f_{VCO} \leq 40$ MHz
Acquisition Time (max.)	80 µs	$f_{VCO} > 40$ MHz
Power Consumption		
Analog Supply Power (max*)	6.9 mW	
Digital Supply Current (max)	7 µW/MHz	
Duty Cycle	50% ±0.5%	

Note: **High clock frequencies (>60 MHz)*

User Security

FlashLock™

ProASIC^PLUS devices have FlashLock protection bits that, once programmed, block the entire programmed contents from being read externally. If locked, the user can only reprogram the device employing the user-defined security key. This protects the device from being read back and duplicated. Since programmed data is stored in nonvolatile memory cells (which are actually very small capacitors), rather than in the wiring, physical deconstruction cannot be used to compromise data. This approach is further hampered by the placement of the memory cells beneath the four metal layers (whose removal cannot be accomplished without disturbing the charge in the capacitor). This is the highest security provided in the industry. For more information, refer to Actel's *Design Security in Nonvolatile Flash and Antifuse FPGAs* white paper.

Embedded Memory Floorplan

The embedded memory is located across the top and bottom of the device in 256x9 blocks (Figure 1-1 on page 1-2). Depending upon the device, up to 88 blocks are available to support a variety of memory configurations. Each block can be programmed as an independent memory or combined (using dedicated memory routing resources) to form larger, more complex memories. A single memory configuration could include blocks from both the top and bottom memory locations.

Embedded Memory Configurations

The embedded memory in the ProASIC^PLUS family provides great configuration flexibility (Table 1-9 on page 1-20). Unlike many other programmable vendors each ProASIC^PLUS block is designed and optimized as a two-port memory (1 read, 1 write). This provides 198kbits of total memory for two-port and single port usage in the APA1000 device.

Each memory can be configured as FIFO or SRAM, with independent selection of synchronous or asynchronous read and write ports (Table 1-10). Additional characteristics include programmable flags as well as parity checking and generation. Figure 1-21 on page 1-21 and Figure 1-22 on page 1-22 show the block diagrams of the basic SRAM and FIFO blocks. Table 1-11 on page 1-22 and Table 1-12 on page 1-23 describe memory block SRAM and FIFO interface signals, respectively. A single memory is designed to operate at up to 150 MHz (standard speed grade typical conditions).

Each block contains a 256 word, 9-bit wide (1 read port, 1 write port) memory. The memory blocks may be combined in parallel to form wider memories or stacked to form deeper memories (Figure 1-23 on page 1-23). This provides optimal bit widths of 9 (1 block), 18, 36, and 72, and optimal depths of 256, 512, 768, and 1,024. Refer to Actel's *A Guide to ACTgen Macros* for more information.

Figure 1-24 on page 1-24 gives an example of optimal memory usage. Ten blocks with 23,040 bits have been used to generate three memories of various widths and depths. Figure 1-25 on page 1-24 shows how memory can be used in parallel to create extra read ports. In this example, using only 10 of the 88 available blocks of the APA1000 yields an effective 6,912 bits of multiple port memories. The Actel ACTgen software facilitates building wider and deeper memories for optimal memory usage.

Table 1-9 • **ProASIC^PLUS Memory Configurations by Device**

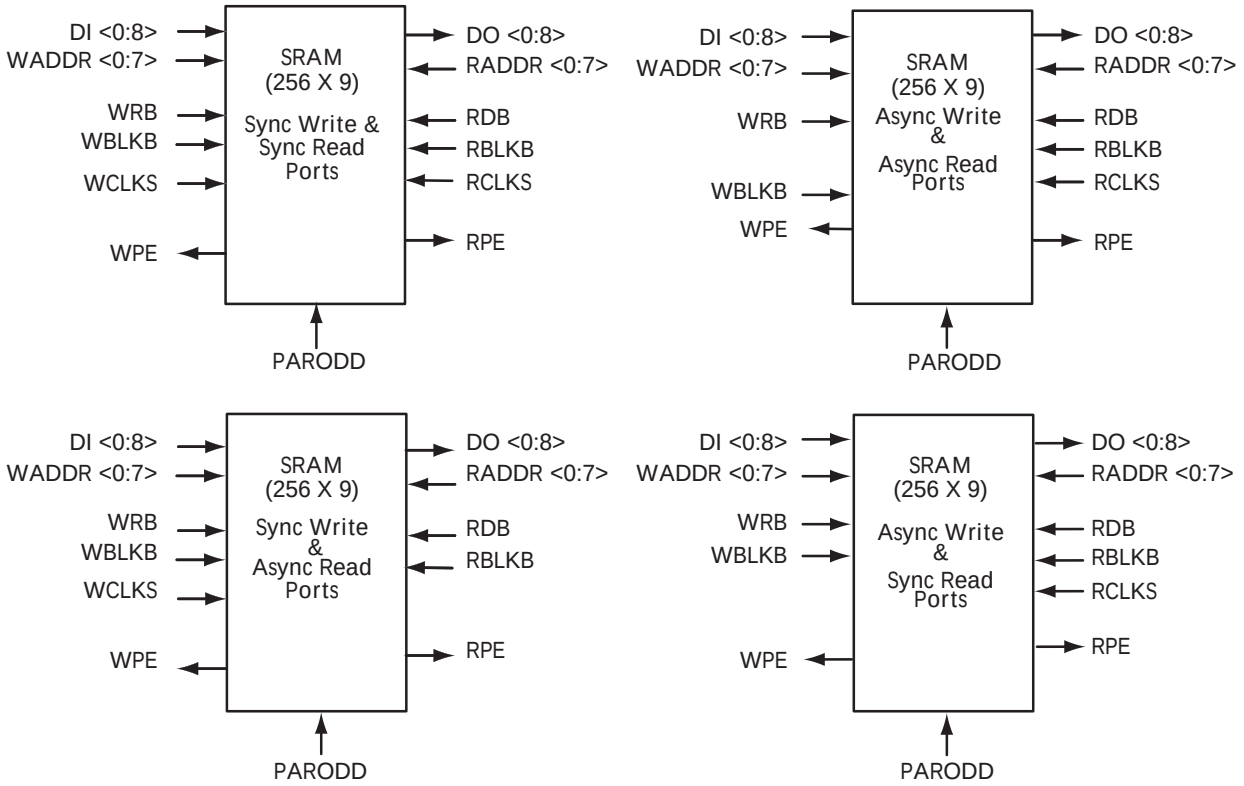
Device	Bottom	Top	Maximum Width		Maximum Depth	
			D	W	D	W
APA075	0	12	256	108	1,536	9
APA150	0	16	256	144	2,048	9
APA300	16	16	256	144	2,048	9
APA450	24	24	256	216	3,072	9
APA600	28	28	256	252	3,584	9
APA750	32	32	256	288	4,096	9
APA1000	44	44	256	396	5,632	9

Table 1-10 • **Basic Memory Configurations**

Type	Write Access	Read Access	Parity	Library Cell Name
RAM	Asynchronous	Asynchronous	Checked	RAM256x9AA
RAM	Asynchronous	Asynchronous	Generated	RAM256x9AAP
RAM	Asynchronous	Synchronous Transparent	Checked	RAM256x9AST
RAM	Asynchronous	Synchronous Transparent	Generated	RAM256x9ASTP
RAM	Asynchronous	Synchronous Pipelined	Checked	RAM256x9ASR
RAM	Asynchronous	Synchronous Pipelined	Generated	RAM256x9ASRP
RAM	Synchronous	Asynchronous	Checked	RAM256x9SA
RAM	Synchronous	Asynchronous	Generated	RAM256xSAP
RAM	Synchronous	Synchronous Transparent	Checked	RAM256x9SST
RAM	Synchronous	Synchronous Transparent	Generated	RAM256x9SSTP
RAM	Synchronous	Synchronous Pipelined	Checked	RAM256x9SSR
RAM	Synchronous	Synchronous Pipelined	Generated	RAM256x9SSRP
FIFO	Asynchronous	Asynchronous	Checked	FIFO256x9AA

Table 1-10 • **Basic Memory Configurations (Continued)**

Type	Write Access	Read Access	Parity	Library Cell Name
FIFO	Asynchronous	Asynchronous	Generated	FIFO256x9AAP
FIFO	Asynchronous	Synchronous Transparent	Checked	FIFO256x9AST
FIFO	Asynchronous	Synchronous Transparent	Generated	FIFO256x9ASTP
FIFO	Asynchronous	Synchronous Pipelined	Checked	FIFO256x9ASR
FIFO	Asynchronous	Synchronous Pipelined	Generated	FIFO256x9ASRP
FIFO	Synchronous	Asynchronous	Checked	FIFO256x9SA
FIFO	Synchronous	Asynchronous	Generated	FIFO256x9SAP
FIFO	Synchronous	Synchronous Transparent	Checked	FIFO256x9SST
FIFO	Synchronous	Synchronous Transparent	Generated	FIFO256x9SSTP
FIFO	Synchronous	Synchronous Pipelined	Checked	FIFO256x9SSR
FIFO	Synchronous	Synchronous Pipelined	Generated	FIFO256x9SSRP



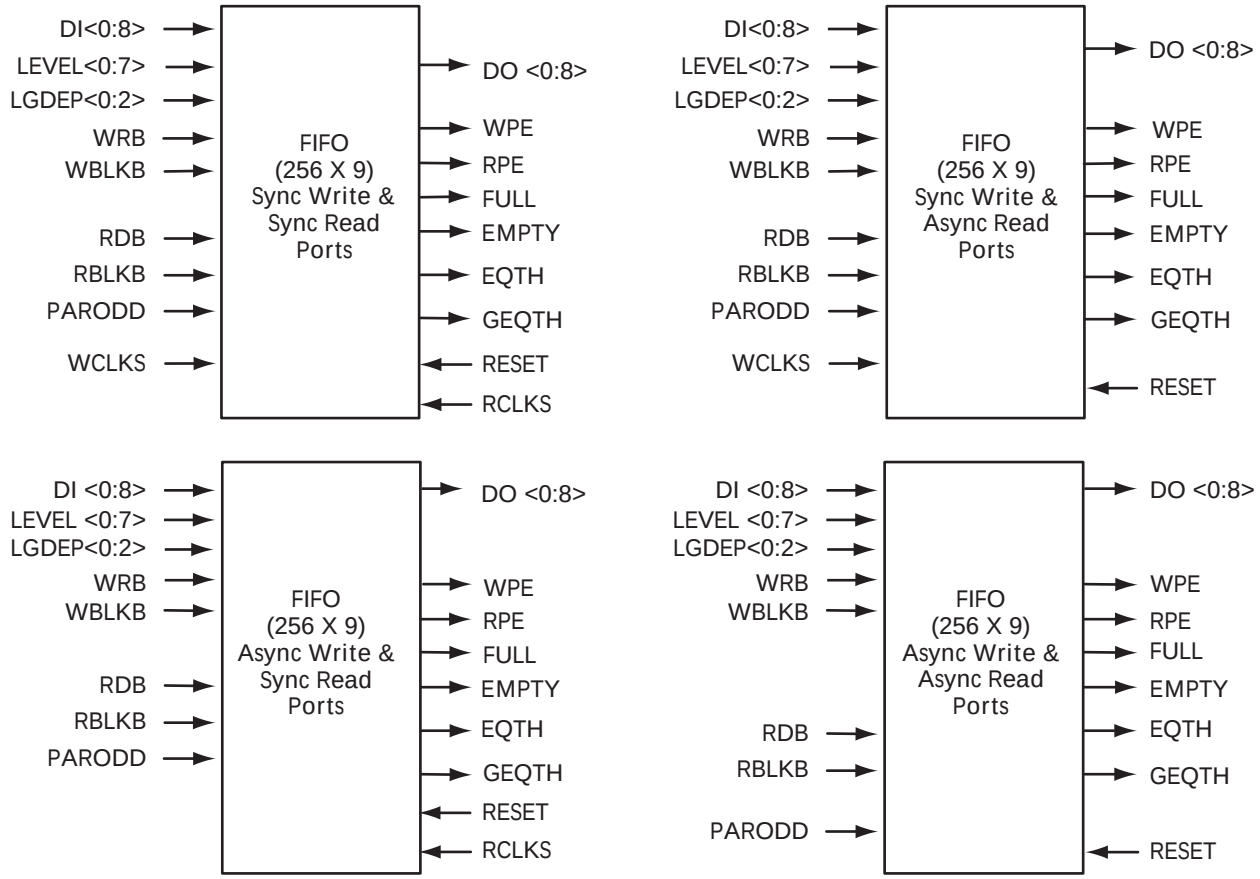
Note: *To save area while using embedded memories, the memory blocks contain multiplexers (called DMUX) for each output signal. These DMUX cells do not consume any core logic tiles and connect directly to high speed routing resources between the memory blocks. They are used when memories are cascaded and are automatically inserted by the software tools.*

Figure 1-21 • **Example SRAM Block Diagrams**

Table 1-11 • **Memory Block SRAM Interface Signals**

SRAM Signal	Bits	In/Out	Description
WCLKS	1	IN	Write clock used on synchronization on write side
RCLKS	1	IN	Read clock used on synchronization on read side
RADDR<0:7>	8	IN	Read address
RBLKB	1	IN	Read block select (active LOW)
RDB	1	IN	Read pulse (active LOW)
WADDR<0:7>	8	IN	Write address
WBLKB	1	IN	Write block select (active LOW)
DI<0:8>	9	IN	Input data bits <0:8>, <8> can be used for parity in
WRB	1	IN	Write pulse (active LOW)
DO<0:8>	9	OUT	Output data bits <0:8>, <8> can be used for parity out
RPE	1	OUT	Read parity error (active HIGH)
WPE	1	OUT	Write parity error (active HIGH)
PARODD	1	IN	Selects odd parity generation/detect when high, even when low

Note: *Not all signals shown are used in all modes.*



Note: *To save area while using embedded memories, the memory blocks contain multiplexers (called DMUX) for each output signal. These DMUX cells do not consume any core logic tiles and connect directly to high speed routing resources between the memory blocks. They are used when memories are cascaded and are automatically inserted by the software tools.*

Figure 1-22 • **Basic FIFO Block Diagrams**

Table 1-12 • **Memory Block FIFO Interface Signals**

FIFO Signal	Bits	In/Out	Description
WCLKS	1	IN	Write clock used for synchronization on write side
RCLKS	1	IN	Read clock used for synchronization on read side
LEVEL <0:7>	8	IN	Direct configuration implements static flag logic
RBLKB	1	IN	Read block select (active LOW)
RDB	1	IN	Read pulse (active LOW)
RESET	1	IN	Reset for FIFO pointers (active LOW)
WBLKB	1	IN	Write block select (active LOW)
DI<0:8>	9	IN	Input data bits <0:8>, <8> will be generated if PARGEN is true
WRB	1	IN	Write pulse (active LOW)
FULL, EMPTY	2	OUT	FIFO flags. FULL prevents write and EMPTY prevents read
EQTH, GEQTH	2	OUT	EQTH is true when the FIFO holds the number of words specified by the LEVEL signal. GEQTH is true when the FIFO holds (LEVEL) words or more
DO<0:8>	9	OUT	Output data bits <0:8>
RPE	1	OUT	Read parity error (active HIGH)
WPE	1	OUT	Write parity error (active HIGH)
LGDEP <0:2>	3	IN	Configures DEPTH of the FIFO to 2 (LGDEP+1)
PARODD	1	IN	Parity generation/detect – Even when low, odd when high

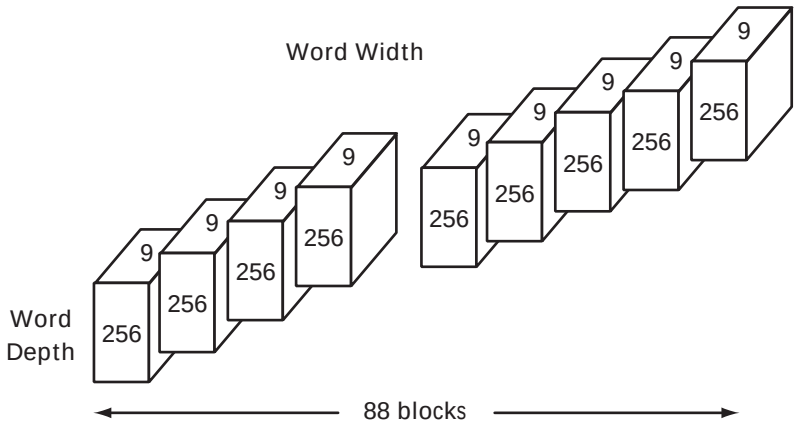


Figure 1-23 • **APA1000 Memory Block Architecture**

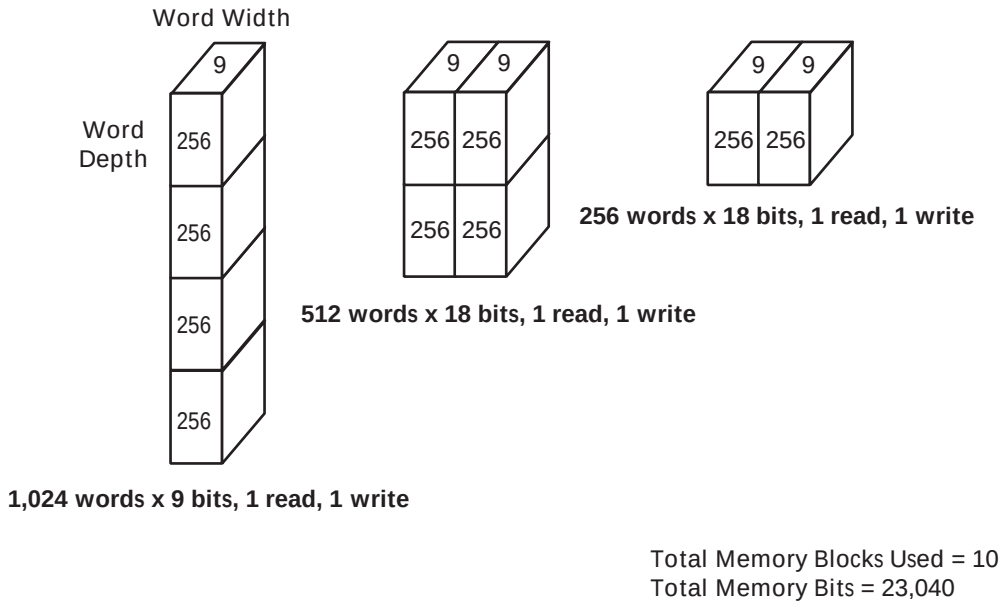


Figure 1-24 • **Example Showing Memories with Different Widths and Depths**

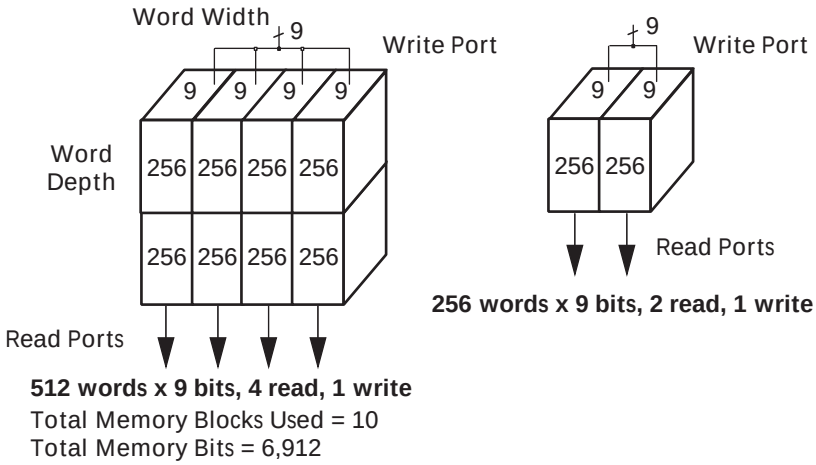


Figure 1-25 • **Multiport Memory Usage**

Design Environment

The ProASICPLUS family of FPGAs is fully supported by both Actel's Libero™ Integrated Design Environment (IDE) and Actel's Designer FPGA Development Software. Actel's Designer software provides a comprehensive suite of backend development tools for FPGA development. The Designer software includes timing-driven place-and-route, a world-class integrated static timing analyzer and constraints editor, a design netlist schematic viewer, and SmartPower, a tool that allows the user to quickly estimate the power consumption in a design.

Libero IDE provides an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools (Figure 1-26 on page 1-25). Libero IDE includes Synplicity® Synplify AE for Actel, Mentor Graphics™ ViewDraw AE for Actel, Actel's own Designer software, Model Technology™ ModelSim AE HDL Simulator, and SynaptiCAD™ WaveFormer Lite AE.

ISP

The user can generate *.bit or *.stp programming files from the Designer software and can use these files to program a device.

ProASIC^PLUS devices can be programmed in system. For more information on ISP of ProASIC^PLUS devices, refer to the *In-System Programming ProASIC^PLUS Devices* and *Performing Internal In-System Programming Using Actel's ProASIC^PLUS Devices* application notes. Prior to being programmed for the first time, the ProASIC^PLUS device I/Os are inputs with pull-ups.

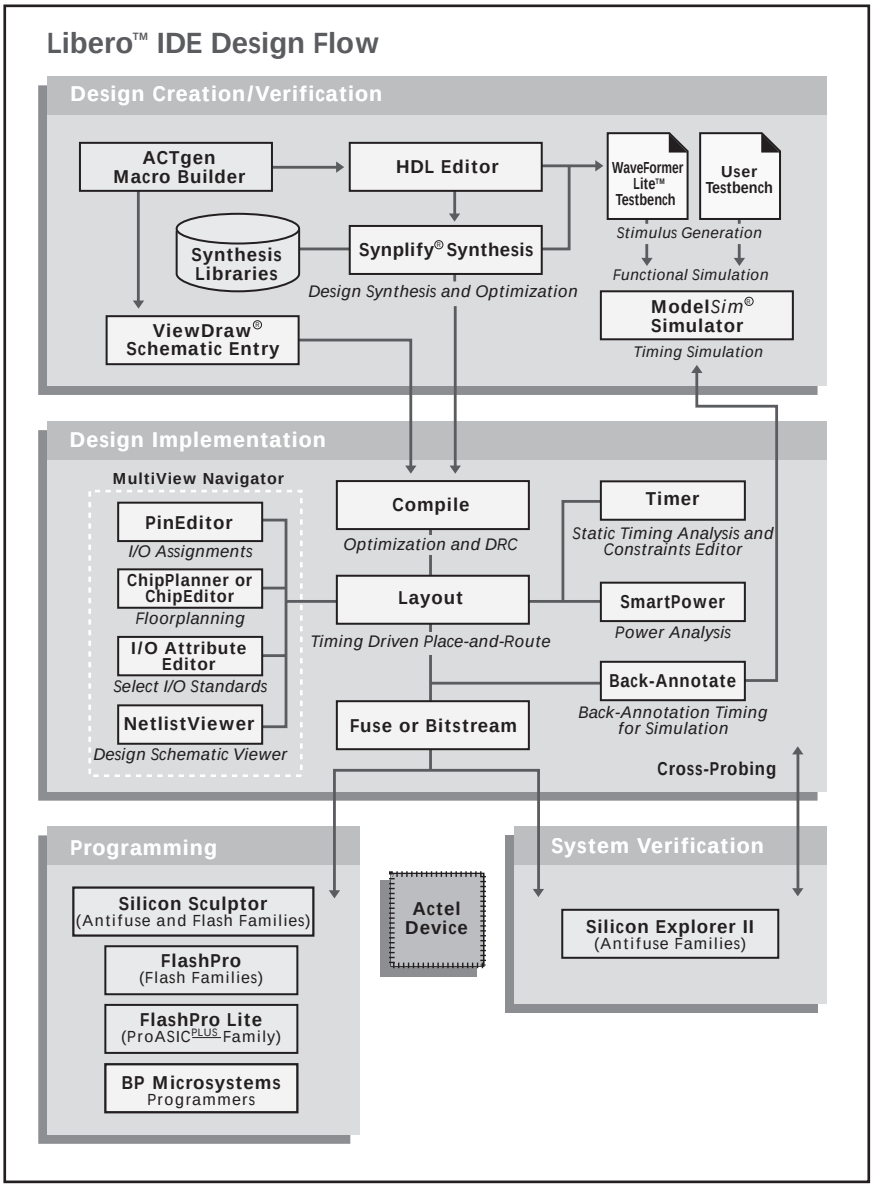


Figure 1-26 • **Design Flow**

Related Documents

Application Notes

Efficient Use of ProASIC Clock Trees
http://www.actel.com/documents/clocktree.pdf
I/O Features in ProASIC^PLUS Flash FPGAs
http://www.actel.com/documents/PAPLUSLVPECL.pdf
ProASIC^PLUS Family Devices Power-Up Behavior
http://www.actel.com/documents/PAPLUS_PowerUp.pdf
ProASIC^PLUS PLL Dynamic Reconfiguration Using JTAG
http://www.actel.com/documents/PAPLUSPLLdynamicAN.pdf
Using ProASIC^PLUS Clock Conditioning Circuits
http://www.actel.com/documents/PAPLUSPLLan.pdf
In-System Programming ProASIC^PLUS Devices
http://www.actel.com/documents/External_ISP_AN.pdf
Performing Internal In-System Programming Using Actel's ProASIC^PLUS Devices
http://www.actel.com/documents/PAplusISPAN.pdf

White Paper

Design Security in Nonvolatile Flash and Antifuse FPGAs
http://www.actel.com/documents/DesignSecurity.pdf

User's Guide

Designer User's Guide
http://www.actel.com/documents/designerUG.pdf
Flash Macro Library Guide
http://www.actel.com/documents/PA_libguide.pdf

Package Thermal Characteristics

The ProASIC^PLUS family is available in several package types with a range of pin counts. Actel has selected packages based on high pin count, reliability factors, and superior thermal characteristics.

Thermal resistance defines the ability of a package to conduct heat away from the silicon, through the package to the surrounding air. Junction-to-ambient thermal resistance is measured in degrees Celsius/Watt and is represented as Theta ja (Θ_{ja}). The lower the thermal resistance, the more efficiently a package will dissipate heat.

A package's maximum allowed power (P) is a function of maximum junction temperature (T_J), maximum ambient operating temperature (T_A), and junction-to-ambient thermal resistance Θ_{ja}. Maximum junction temperature is the maximum allowable temperature on the active surface of the IC and is 110° C. P is defined as:

$$P = \frac{T_J - T_A}{\Theta_{ja}}$$

Θ_{ja} is a function of the rate (in linear feet per minute – lfpm) of airflow in contact with the package. When the estimated power consumption exceeds the maximum allowed power, other means of cooling, such as increasing the airflow rate, must be used.

Table 1-13 • **Package Thermal Characteristics**

Package Type	Pin Count	Θ_{jc}	Θ_{ja} Still Air	Θ_{ja} 300 ft./ min.	Units
Thin Quad Flat Pack (TQFP)	100	12	37.5	30	°C/W
Thin Quad Flat Pack (TQFP)	144	11	32	24	°C/W
Plastic Quad Flat Pack (PQFP)	208	8	30	23	°C/W
PQFP with Heatspreader	208	3.8	20	17	°C/W
Plastic Ball Grid Array (PBGA)	456	3	15.6	12	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	38.8	26.7	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	25	22	°C/W
Fine Pitch Ball Grid Array (FBGA)[1]	484	3.2	20	15	°C/W
Fine Pitch Ball Grid Array (FBGA)[2]	484	3.2	20.5	16.6	°C/W
Fine Pitch Ball Grid Array (FBGA)	676	3.2	16.4	11.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	896	2.4	13.6	10.3	°C/W
Fine Pitch Ball Grid Array (FBGA)	1152	1.8	12	8.9	°C/W

Notes:

1. Depopulated Array
2. Full Array

Calculating Typical Power Dissipation

ProASIC^PLUS device power is calculated with both a static and an active component. The active component is a function of both the number of tiles utilized and the system speed. Power dissipation can be calculated using the following formula:

$$P_{total} = P_{dc} + P_{ac}$$

where:

- P_{dc} = 12.5 mW (Typically 2.5V x 5mA)

P_{dc} includes the static components of:
$P_{VDDP} + P_{VDD} + P_{AVDD}$

- P_{ac} = $P_{clock} + P_{storage} + P_{logic} + P_{inputs} + P_{outputs} + P_{memory} + P_{pll}$

P_{clock}, the clock component of power dissipation, is given by

$$P_{clock} = (P1 + P2 * R - P7*R^2) * Fs$$

where:

- P1 = 100 µW/MHz is the basic power consumption of the clock tree per MHz of the clock
- P2 = 1.3 µW/MHz is the incremental power consumption of the clock tree per storage tile – also per MHz of the clock
- P7 = 0.00003 µW/MHz is a correction factor for highly loaded clock-trees
- R = the number of storage tiles clocked by this clock
- Fs = the clock frequency

$P_{storage}$, the storage-tile (Register) component of AC power dissipation, is given by

$$P_{storage} = P5 * ms * Fs$$

where:

- P5 = 1.1 µW/MHz is the average power consumption of a storage-tile per MHz of its output toggling rate. The maximum output toggling rate is Fs/2
- ms = the number of storage tiles (Register) switching during each Fs cycle
- Fs = the clock frequency

P_{logic}, the logic-tile component of AC power dissipation, is given by

$$P_{logic} = P3 * mc * Fs$$

where:

- P3 = 1.4 µW/MHz, is the average power consumption of a logic tile per MHz of its output toggling rate. The maximum output toggling rate is Fs/2
- mc = the number of logic tiles switching during each Fs cycle
- Fs = the clock frequency

$P_{outputs}$, the I/O component of AC power dissipation, is given by

$$P_{outputs} = (P4 + (C_{load} * V_{DDP}^2)) * p * Fp$$

where:

- P4 = 326 µW/MHz is the intrinsic power consumption of an output pad normalized per MHz of the output frequency. This is the total I/O current $V_{DD} + V_{DDP}$
- C_{load} = the output load
- p = the number of outputs
- Fp = the average output frequency

The input's component of AC power dissipation is given by

$$P_{inputs} = P8 * q * Fq$$

where:

- P8 = 29 µW/MHz is the intrinsic power consumption of an input pad normalized per MHz of the input frequency
- q = the number of inputs
- Fq = the average input frequency

$$P_{pll} = P9 * N_{pll}$$

where:

- P9 = 7.5 mW. This value has been estimated at maximum PLL clock frequency
- N_{pll} = number of PLLs used

Finally, P_{memory}, the memory component of AC power consumption, is given by

$$P_{memory} = P6 * N_{memory} * F_{memory} * E_{memory}$$

where:

- P6 = 175 µW/MHz is the average power consumption of a memory block per MHz of the clock
- N_{memory} = the number of RAM/FIFO blocks (1 block = 256 words * 9 bits)

- F_{memory} = the clock frequency of the memory
- E_{memory} = the average number of active blocks divided by the total number of blocks (N) of the memory.
  - Typical values for E_{memory} would be 1/4 for a 1k x 8,9,16, 32 memory and 1/16 for a 4kx8, 9, 16, and 32 memory
  - In addition, an application-dependent component to E_{memory} can be considered. For example, for a 1kx8 memory using only 1 cycle out of 3, E_{memory} = 1/4*1/3 = 1/12

The following is an APA750 example using a shift register design with 13,440 storage tiles (Register) and 0 logic tiles. This design has one clock at 10 MHz, and 24 outputs toggling at 5 MHz. We then calculate the various components as follows:

P_{clock}

- sF = 10 MHz
- R = 13,440

=> $P_{clock} = (P1 + P2 * R - P7*R^2) * Fs = 124.2$ mW

$P_{storage}$

- ms= 13,440 (in a shift register 100% of storage-tiles are toggling at each clock cycle and Fs = 10 MHz)

=> $P_{storage} = P5 * ms * Fs = 147.8$ mW

P_{logic}

- m = 0 (no logic tile in this shift-register)

=> $P_{logic} = 0$ mW

$P_{outputs}$

- C_{load} = 40 pF
- V_{DDP} = 3.3 V
- p = 24
- Fp = 5 MHz

=> $P_{outputs} = (P4 + C_{load} * V_{DDP}^2) * p * Fp = 87.3$ mW

P_{inputs}

- q = 1
- Fq = 10 MHz

=> $P_{inputs} = P8 * q * Fq = 0.3$ mW

P_{memory}

N_{memory} = 0 (no RAM/FIFO in this shift-register)

=> $P_{memory} = 0$ mW

P_{ac}

=> 360 mW

P_{total}

$P_{dc} + P_{ac} = 372$ mW (Typical)

Operating Conditions

Standard and –F parts are the same unless otherwise noted. –F parts are only available as commercial.

Table 1-14 • **Absolute Maximum Ratings***

Parameter	Condition	Minimum	Maximum	Units
Supply Voltage Core (V_{DD})		–0.3	3.0	V
Supply Voltage I/O Ring (V_{DDP})		–0.3	4.0	V
DC Input Voltage		–0.3	V_{DDP} + 0.3	V
PCI DC Input Voltage		–1.0	V_{DDP} + 1.0	V
PCI DC Input Clamp Current (absolute)	V_{IN} < –1 or V_{IN} = $V_{DDP + 1V}$	10		mA
LVPECL Input Voltage		–0.3	$V_{DDP + 0.5}$	V
GND		0	0	V

Note: **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Table 1-15 • **Programming, Storage and Operating Limits**

Product Grade	Programming Cycles	Program Retention	Storage Temperature		Operating
			Min.	Max.	T_J Max Junction Temperature
Commercial	500	20 years	–55°C	110°C	110°C
Industrial	500	20 years	–55°C	110°C	110°C

Note: *This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.*

Table 1-16 • **Supply Voltages**

Mode	V_{DD}	V_{DDP}
Single Voltage	2.5V	2.5V
Mixed Voltage*	2.5V	3.3V

Note: **Please refer to the mixed-mode interfacing section in the I/O Features in ProASIC PLUS Flash FPGAs application note for more information.*

Table 1-17 • **Recommended Maximum Operating Conditions Programming and PLL Supplies**

Parameter	Condition	Commercial/Industrial		Units
		Minimum	Maximum	
V_{PP}	During Programming	15.8	16.5	V
	Normal Operation[1]	0	16.5	V
V_{PN}	During Programming	–13.8	–13.2	V
	Normal Operation[2]	–13.8	0	V
I_{PP}	During Programming		25	mA
I_{PN}	During Programming		10	mA
AVDD		V_{DD}	V_{DD}	V
AGND		GND	GND	V

Notes:

1. Please refer to the "VPP Programming Supply Pin" on page 1-64 for more information.
2. Please refer to the "VPN Programming Supply Pin" on page 1-64 for more information.

Table 1-18 • **Recommended Operating Conditions**

Parameter	Symbol	Limits	
		Commercial	Industrial
DC Supply Voltage (2.5V I/Os)	V_{DD} & V_{DDP}	2.5V ± 0.2V	2.5V ± 0.2V
DC Supply Voltage (2.5V, 3.3V I/Os*)	V_{DDP} V_{DD}	3.3V ± 0.3V 2.5V ± 0.2V	3.3V ± 0.3V 2.5V ± 0.2V
Operating Ambient Temperature Range	T_A	0°C to 70°C	–40°C to 85°C
Maximum Operating Junction Temperature	T_J	110°C	110°C

Note: **Please refer to the mixed-mode interfacing section in the I/O Features in ProASIC^PLUS Flash FPGAs application note for more information.*

Table 1-19 • **DC Electrical Specifications (V_{DDP} = 2.5V ±0.2V)[1]**

Symbol	Parameter	Conditions		Commercial / Industrial[1,2]			
				Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage High Drive (OB25LPH) Low Drive (OB25LPL)	I_{OH} = –6 mA I_{OH} = –12 mA I_{OH} = –24 mA I_{OH} = –3 mA I_{OH} = –6 mA I_{OH} = –8 mA		2.1 2.0 1.7 2.1 1.9 1.7			V
V_{OL}	Output Low Voltage High Drive (OB25LPH) Low Drive (OB25LPL)	I_{OL} = 8 mA I_{OL} = 15 mA I_{OL} = 24 mA I_{OL} = 4 mA I_{OL} = 8 mA I_{OL} = 15 mA				0.2 0.4 0.7 0.2 0.4 0.7	V
V_{IH}	Input High Voltage			1.7		V_{DDP} + 0.3	V
V_{IL}	Input Low Voltage			–0.3		0.7	V
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (OTB25LPU)	$V_{IN} \geq$ 1.25V		6		56	kΩ
HYST	Input Hysteresis Schmitt	See Table 1-4 on page 1-8		0.3	0.35	0.45	V
I_{IN}	Input Current	with pull up (V_{IN} = GND)		–240		– 20	µA
		without pull up (V_{IN} = GND or V_{DD})		–10		10	µA
I_{DDQ}	Quiescent Supply Current (standby) Commercial	VIN = GND[3] or VDD	Std.		5.0	15	mA
			–F		5.0	25	mA
I_{DDQ}	Quiescent Supply Current (standby) Industrial	V_{IN} = GND[3] or V_{DD}	Std.		5.0	20	mA

Notes:

1. All process conditions. Junction Temperature: –40 to +110°C.
2. –F parts are only available as commercial.
3. No pull-up resistor.
4. This will not exceed 2mA total per device.

Table 1-19 • **DC Electrical Specifications (V_{DDP} = 2.5V ±0.2V)[1] (Continued)**

Symbol	Parameter	Conditions		Commercial / Industrial[1,2] Min.	Typ.	Max.	Units
I_{OZ}	3-State Output Leakage Current	V_{OH} = GND or V_{DD}	Std.	–10		10	µA
			–F[4]	–10		100	µA
I_{OSH}	Output Short Circuit Current High High Drive (OB25LPH) Low Drive (OB25LPL)	 V_{IN} = V_{SS} V_{IN} = V_{SS}		 –120 –100			mA
I_{OSL}	Output Short Circuit Current Low High Drive (OB25LPH) Low Drive (OB25LPL)	 V_{IN} = V_{DDP} V_{IN} = V_{DDP}				 100 30	mA
$C_{I/O}$	I/O Pad Capacitance					10	pF
C_{CLK}	Clock Input Pad Capacitance					10	pF

Notes:

1. All process conditions. Junction Temperature: –40 to +110°C.
2. –F parts are only available as commercial.
3. No pull-up resistor.
4. This will not exceed 2mA total per device.

Table 1-20 • **DC Electrical Specifications (V_{DDP} = 3.3V ±0.3V and V_{DD} 2.5V ±0.2V)[1]**

Symbol	Parameter	Conditions	Commercial / Industrial[1,2] Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage 3.3V I/O, High Drive (OB33P) 3.3V I/O, Low Drive (OB33L)	I_{OH} = –14 mA I_{OH} = –24 mA I_{OH} = –6 mA I_{OH} = –12 mA	0.9*V_{DDP} 2.4 0.9*V_{DDP} 2.4			V
	Output High Voltage 2.5V I/O, High Drive (OB25H)[3] 2.5V I/O, Low Drive (OB25L)[3]	I_{OH} = –0.1 mA I_{OH} = –0.5 mA I_{OH} = –3.0 mA I_{OH} = –0.1 mA I_{OH} = –0.5 mA I_{OH} = –1.0 mA	2.1 2.0 1.7 2.1 2.0 1.7			V
V_{OL}	Output Low Voltage 3.3V I/O, High Drive (OB33P) 3.3V I/O, Low Drive (OB33L)	I_{OL} = 15 mA I_{OL} = 20 mA I_{OL} = 28 mA I_{OL} = 7 mA I_{OL} = 10 mA I_{OL} = 15 mA			0.1V_{DDP} 0.4 0.7 0.1V_{DDP} 0.4 0.7	V
	Output Low Voltage 2.5V I/O, High Drive (OB25H)[3] 2.5V I/O, Low Drive (OB25L)[3]	I_{OL} = 7 mA I_{OL} = 14 mA I_{OL} = 28 mA I_{OL} = 5 mA I_{OL} = 10 mA I_{OL} = 15 mA			0.2 0.4 0.7 0.2 0.4 0.7	V
V_{IH}	Input High Voltage 3.3V LVTTL/LVCMOS 2.5V Mode		2 1.7		V_{DDP} + 0.3 V_{DDP} + 0.3	V
V_{IL}	Input Low Voltage 3.3V LVTTL/LVCMOS 2.5V Mode		 –0.3 –0.3		 0.8 0.7	V
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (IOB33U)	$V_{IN} \geq$ 1.5V	7		43	kΩ
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (IOB25U)	$V_{IN} \geq$ 1.5V	7		43	kΩ
I_{IN}	Input Current	with pull up (V_{IN} = GND)	–300		–40	µA
		without pull up (V_{IN} = GND or V_{DD})	–10		10	µA

Notes:

1. All process conditions. Junction Temperature: –40 to +110°C.
2. –F parts are only available as commercial.
3. Please refer to the mixed-mode interfacing section in the I/O Features in ProASIC^PLUS Flash FPGAs application note for guidelines and usage.
4. No pull-up resistor.
5. This will not exceed 2mA total per device.

Table 1-20 • **DC Electrical Specifications (V_{DDP} = 3.3V ±0.3V and V_{DD} 2.5V ±0.2V)[1] (Continued)**

Symbol	Parameter	Conditions		Commercial / Industrial[1,2] Min.	Typ.	Max.	Units
I_{DDQ}	Quiescent Supply Current (standby) Commercial	V_{IN} = GND[4] or V_{DD}	Std.		5.0	15	mA
			–F		5.0	25	mA
I_{DDQ}	Quiescent Supply Current (standby) Industrial	V_{IN} = GND[4] or V_{DD}	Std.		5.0	20	mA
I_{OZ}	3-State Output Leakage Current	V_{OH} = GND or V_{DD}	Std.	–10		10	µA
			–F[4]	–10		100	µA
I_{OSH}	Output Short Circuit Current High 3.3V High Drive (OB33P) 3.3V Low Drive (OB33L) 2.5V High Drive (OB25H)[3] 2.5V Low Drive (OB25L)[3]	V_{IN} = GND V_{IN} = GND V_{IN} = GND V_{IN} = GND		 –200 –100 –20 –10			mA
I_{OSL}	Output Short Circuit Current Low 3.3V High Drive 3.3V Low Drive 2.5V High Drive[3] 2.5V Low Drive[3]	V_{IN} = V_{DD} V_{IN} = V_{DD} V_{IN} = V_{DD} V_{IN} = V_{DD}				 200 100 200 100	mA
$C_{I/O}$	I/O Pad Capacitance					10	pF
C_{CLK}	Clock Input Pad Capacitance					10	pF

Notes:

1. All process conditions. Junction Temperature: –40 to +110°C.
2. –F parts are only available as commercial.
3. Please refer to the mixed-mode interfacing section in the I/O Features in ProASIC^PLUS Flash FPGAs application note for guidelines and usage.
4. No pull-up resistor.
5. This will not exceed 2mA total per device.

Table 1-21 • **DC Specifications (3.3V PCI Operation)[1]**

Symbol	Parameter	Condition		Commercial / Industrial[2,3] Min.	Commercial / Industrial[2,3] Max.	Units
V_{DD}	Supply Voltage for Core			2.3	2.7	V
V_{DDP}	Supply Voltage for I/O Ring			3.0	3.6	V
V_{IH}	Input High Voltage			$0.5V_{DDP}$	V_{DDP} + 0.5	V
V_{IL}	Input Low Voltage			–0.5	$0.3V_{DDP}$	V
I_{IPU}	Input Pull-up Voltage[4]			$0.7V_{DDP}$		V
I_{IL}	Input Leakage Current[5]	$0 < V_{IN} < V_{CCI}$	Std.	–10	10	µA
			–F[6]	–10	100	µA
V_{OH}	Output High Voltage	I_{OUT} = –500 µA		$0.9V_{DDP}$		V
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA			$0.1V_{DDP}$	V
C_{IN}	Input Pin Capacitance (except CLK)				10	pF
C_{CLK}	CLK Pin Capacitance			5	12	pF

Notes:

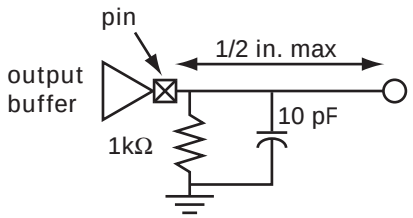
1. For PCI operation, use OTB33PH, OB33PH, IOB33PH, IB33, or IB33S macro library cell only.
2. All process conditions. Junction Temperature: –40 to +110°C.
3. –F parts are available as commercial only.
4. This specification is guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers with applications sensitive to static power utilization should ensure that the input buffer is conducting minimum current at this input voltage.
5. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
6. The sum of the leakage currents for all inputs shall not exceed 2mA per device.

Table 1-22 • **AC Specifications (3.3V PCI Revision 2.2 Operation)**

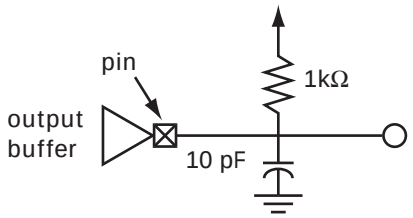
Symbol	Parameter	Condition	Commercial / Industrial		Units
			Min.	Max.	
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 0.3V_{CCI}$*	$-12V_{CCI}$		mA
		$0.3V_{CCI} \le V_{OUT} < 0.9V_{CCI}$*	$(-17.1 + (V_{DDP} - V_{OUT}))$		mA
		$0.7V_{CCI} < V_{OUT} < V_{CCI}$*		See equation C – page 124 of the PCI Specification document rev. 2.2	
	(Test Point)	$V_{OUT} = 0.7V_{CC}$*		$-32V_{CCI}$	mA
$I_{OL(AC)}$	Switching Current Low	$V_{CCI} > V_{OUT} \ge 0.6V_{CCI}$*	$16V_{DDP}$		mA
		$0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}$ [1]	$(26.7V_{OUT})$		mA
		$0.18V_{CCI} > V_{OUT} > 0$*		See equation D – page 124 of the PCI Specification document rev. 2.2	
	(Test Point)	$V_{OUT} = 0.18V_{CC}$		$38V_{CCI}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$V_{CCI} + 4 > V_{IN} \ge$ ς$_{CCI}$ + 1	$25 + (V_{IN} - V_{DDP} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	$0.2V_{CCI}$ to $0.6V_{CCI}$ load*	1	4	V/ns
$slew_F$	Output Fall Slew Rate	$0.6V_{CCI}$ to $0.2V_{CCI}$ load*	1	4	V/ns

Note: ** Refer to the PCI Specification document rev. 2.2.*

Pad Loading Applicable to the Rising Edge PCI



Pad Loading Applicable to the Falling Edge PCI



Tristate Buffer Delays

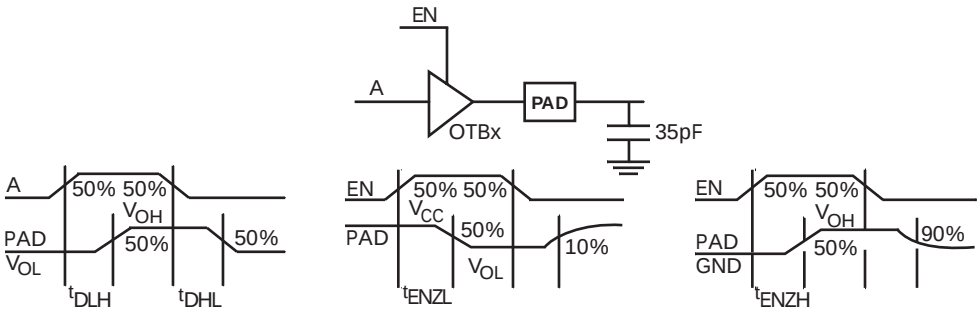


Figure 1-27 • **Tristate Buffer Delays**

Table 1-23 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, 35 pF load, T_J = 70°C

Macro Type	Description	Max t_{DLH}[1]		Max t_{DHL}[2]		Max t_{ENZH}[3]		Max t_{ENZL}[4]		Units
		STD	–F	STD	–F	STD	–F	STD	–F	
OTB33PH	3.3V, PCI Output Current, High Slew Rate	2.0	2.4	2.2	2.6	2.2	2.6	2.0	2.4	ns
OTB33PN	3.3V, High Output Current, Nominal Slew Rate	2.2	2.6	2.9	3.5	2.4	2.9	2.1	2.5	ns
OTB33PL	3.3V, High Output Current, Low Slew Rate	2.5	3.0	3.2	3.9	2.7	3.3	2.8	3.4	ns
OTB33LH	3.3V, Low Output Current, High Slew Rate	2.6	3.1	4.0	4.8	2.8	3.4	3.0	3.6	ns
OTB33LN	3.3V, Low Output Current, Nominal Slew Rate	2.9	3.5	4.3	5.2	3.2	3.8	4.1	4.9	ns
OTB33LL	3.3V, Low Output Current, Low Slew Rate	3.0	3.6	5.6	6.7	3.3	3.9	5.5	6.6	ns
OTB25HH	2.5V, High Output Current, High Slew Rate[5]	3.1	3.8	1.8	2.2	2.8	3.4	1.7	2.0	ns
OTB25HN	2.5V, High Output Current, Nominal Slew Rate[5]	3.1	3.7	2.7	3.3	2.9	3.5	2.7	3.2	ns
OTB25HL	2.5V, High Output Current, Low Slew Rate[5]	3.1	3.7	3.9	4.7	2.9	3.5	3.8	4.6	ns
OTB25LH	2.5V, Low Output Current, High Slew Rate[5]	4.6	5.6	2.9	3.5	4.6	5.5	2.9	3.4	ns
OTB25LN	2.5V, Low Output Current, Nominal Slew Rate[5]	4.6	5.6	3.7	4.5	4.6	5.5	3.6	4.3	ns
OTB25LL	2.5V, Low Output Current, Low Slew Rate[5]	4.6	5.6	5.1	6.1	4.5	5.4	4.8	5.8	ns
OTB25LPHH	2.5V, Low Power, High Output Current, High Slew Rate[6]	2.0	2.4	2.1	2.5	2.3	2.7	2.0	2.4	ns
OTB25LPHN	2.5V, Low Power, High Output Current, Nominal Slew Rate[6]	2.4	2.9	3.0	3.6	2.7	3.2	2.1	2.5	ns
OTB25LPHL	2.5V, Low Power, High Output Current, Low Slew Rate[6]	2.9	3.5	3.2	3.8	3.1	3.8	2.7	3.2	ns
OTB25LPLH	2.5V, Low Power, Low Output Current, High Slew Rate[6]	2.7	3.3	4.6	5.5	3.0	3.6	2.6	3.1	ns
OTB25LPLN	2.5V, Low Power, Low Output Current, Nominal Slew Rate[6]	3.5	4.2	4.2	5.1	3.8	4.5	3.8	4.6	ns
OTB25LPLL	2.5V, Low Power, Low Output Current, Low Slew Rate[6]	4.0	4.8	5.3	6.4	4.2	5.1	5.1	6.1	ns

Notes:

1. t_{DLH}=Data-to-Pad HIGH
2. t_{DHL}=Data-to-Pad LOW
3. t_{ENZH}=Enable-to-Pad, Z to HIGH
4. t_{ENZL} = Enable-to-Pad, Z to LOW
5. Please refer to the mixed-mode interfacing section in the I/O Features in ProASIC^PLUS Flash FPGAs application note for guidelines and usage.
6. Low power I/O work with V_{DDP}=2.5V ±10% only. V_{DDP}=2.3V for delays.

Output Buffer Delays

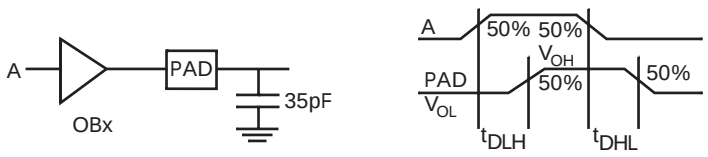


Figure 1-28 • **Output Buffer Delays**

Table 1-24 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, 35 pF load, T_J = 70°C

Macro Type	Description	Max t_{DLH}[1]		Max t_{DHL}[2]		Units
		STD	–F	STD	–F	
OB33PH	3.3V, PCI Output Current, High Slew Rate	2.0	2.4	2.2	2.6	ns
OB33PN	3.3V, High Output Current, Nominal Slew Rate	2.2	2.6	2.9	3.5	ns
OB33PL	3.3V, High Output Current, Low Slew Rate	2.5	3.0	3.2	3.9	ns
OB33LH	3.3V, Low Output Current, High Slew Rate	2.6	3.1	4.0	4.8	ns
OB33LN	3.3V, Low Output Current, Nominal Slew Rate	2.9	3.5	4.3	5.2	ns
OB33LL	3.3V, Low Output Current, Low Slew Rate	3.0	3.6	5.6	6.7	ns
OB25HH	2.5V, High Output Current, High Slew Rate[3]	3.1	3.8	1.8	2.2	ns
OB25HN	2.5V, High Output Current, Nominal Slew Rate[3]	3.1	3.7	2.7	3.3	ns
OB25HL	2.5V, High Output Current, Low Slew Rate[3]	3.1	3.7	3.9	4.7	ns
OB25LH	2.5V, Low Output Current, High Slew Rate[3]	4.6	5.6	2.9	3.5	ns
OB25LN	2.5V, Low Output Current, Nominal Slew Rate[3]	4.6	5.6	3.7	4.5	ns
OB25LL	2.5V, Low Output Current, Low Slew Rate[3]	4.6	5.6	5.1	6.1	ns
OB25LPHH	2.5V, Low Power, High Output Current, High Slew Rate[4]	2.0	2.4	2.1	2.6	ns
OB25LPHN	2.5V, Low Power, High Output Current, Nominal Slew Rate[4]	2.4	2.9	3.0	3.6	ns
OB25LPHL	2.5V, Low Power, High Output Current, Low Slew Rate[4]	2.9	3.5	3.2	3.8	ns
OB25LPLH	2.5V, Low Power, Low Output Current, High Slew Rate[4]	2.7	3.3	4.6	5.5	ns
OB25LPLN	2.5V, Low Power, Low Output Current, Nominal Slew Rate[4]	3.5	4.2	4.2	5.1	ns
OB25LPLL	2.5V, Low Power, Low Output Current, Low Slew Rate[4]	4.0	4.8	5.3	6.4	ns

Notes:

1. t_{DLH} = Data-to-Pad HIGH
2. t_{DHL} = Data-to-Pad LOW
3. Please refer to the mixed-mode interfacing section in the I/O Features in ProASIC^PLUS Flash FPGAs application note for guidelines and usage.
4. Low power I/O work with V_{DDP}=2.5V ±10% only. V_{DDP}=2.3V for delays.

Input Buffer Delays

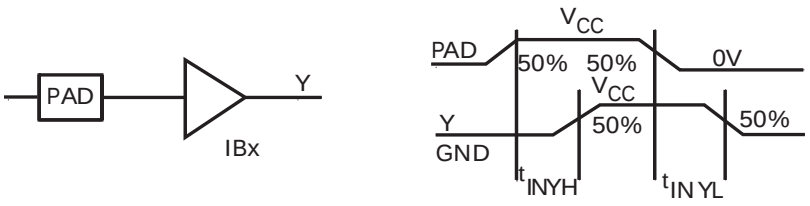


Figure 1-29 • **Input Buffer Delays**

Table 1-25 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 70°C

Macro Type	Description	Max. t_{INYH}[1]		Max. t_{INYL}[2]		Units
		Std.	–F	Std.	–F	
IB25	2.5V, CMOS Input Levels[3], No Pull-up Resistor	0.7	0.9	0.8	1.0	ns
IB25S	2.5V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	0.7	0.9	0.8	1.0	ns
IB25LP	2.5V, CMOS Input Levels[3], Low Power	0.9	1.1	0.6	0.8	ns
IB25LPS	2.5V, CMOS Input Levels[3], Low Power, Schmitt Trigger	0.7	0.9	0.9	1.1	ns
IB33	3.3V, CMOS Input Levels[3], No Pull-up Resistor	0.4	0.5	0.6	0.7	ns
IB33S	3.3V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	0.6	0.7	0.8	0.9	ns

Notes:

1. t_{INYH} = Input Pad-to-Y HIGH
2. t_{INYL} = Input Pad-to-Y LOW
3. LVTTL delays are the same as CMOS delays.
4. For LP Macros, V_{DDP}=2.3V for delays.

Global Input Buffer Delays

Table 1-26 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 70°

Macro Type	Description	Max. t_{INYH}[1]		Max. t_{INYL}[2]		Units
		Std.	–F	Std.	–F	
GL25	2.5V, CMOS Input Levels[3], No Pull-up Resistor	1.3	1.6	1.0	1.2	ns
GL25S	2.5V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	1.3	1.6	1.0	1.2	ns
GL25LP	2.5V, CMOS Input Levels[3], Low Power	1.1	1.2	1.0	1.3	ns
GL25LPS	2.5V, CMOS Input Levels[3], Low Power, Schmitt Trigger	1.3	1.6	1.0	1.1	ns
GL33	3.3V, CMOS Input Levels[3], No Pull-up Resistor	1.0	1.2	1.1	1.3	ns
GL33S	3.3V, CMOS Input Levels[3], No Pull-up Resistor, Schmitt Trigger	1.0	1.2	1.1	1.3	ns
PECL	PPECL Input Levels	1.0	1.2	1.1	1.3	ns

Notes:

1. t_{INYH} = Input Pad-to-Y HIGH
2. t_{INYL} = Input Pad-to-Y LOW
3. LVTTL delays are the same as CMOS delays.
4. For LP Macros, V_{DDP}=2.3V for delays.

Predicted Global Routing Delay

Table 1-27 • **Worst-Case Commercial Conditions[1]**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 70°C

Parameter	Description	Max.		Units
		Std.	–F	
t_{RCKH}	Input Low to High[2]	1.1	1.3	ns
t_{RCKL}	Input High to Low[2]	1.0	1.2	ns
t_{RCKH}	Input Low to High[3]	0.8	1.0	ns
t_{RCKL}	Input High to Low[3]	0.8	1.0	ns

Notes:

1. The timing delay difference between tile locations is less than 15ps.
2. Highly loaded row 50%.
3. Minimally loaded row.

Global Routing Skew

Table 1-28 • **Worst-Case Commercial Conditions**
V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 70°C

Parameter	Description	Max.		Units
		Std.	–F	
t_{RCKSWH}	Maximum Skew Low to High	270	320	ps
t_{RCKSHH}	Maximum Skew High to Low	270	320	ps

Module Delays

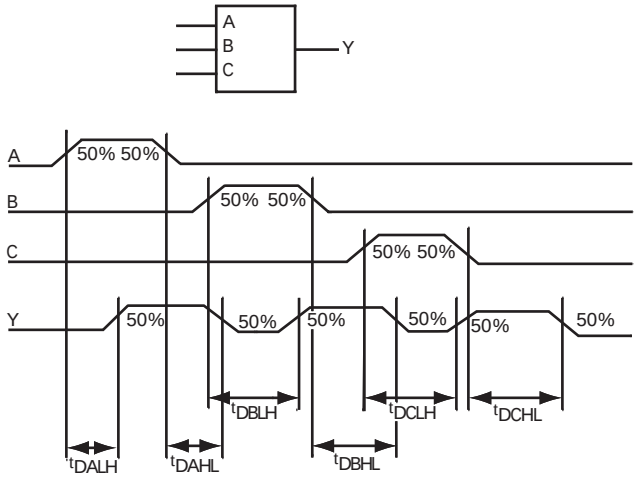


Figure 1-30 • **Module Delays**

Sample Macrocell Library Listing

Table 1-29 • **Worst-Case Commercial Conditions[1]**
V_{DD} = 2.3V, TJ = 70° C

Cell Name	Description		Standard Max	Standard Min	–F Max	–F Min	Units
NAND2	2-Input NAND		0.5		0.6		ns
AND2	2-Input AND		0.7		0.8		ns
NOR3	3-Input NOR		0.8		1.0		ns
MUX2L	2-1 MUX with Active Low Select		0.5		0.6		ns
OA21	2-Input OR into a 2-Input AND		0.8		1.0		ns
XOR2	2-Input Exclusive OR		0.6		0.8		ns
LDL	Active Low Latch (LH/HL)						ns
	CLK-Q	LH[2]	0.9		1.1		
		HL[2]	0.8		0.9		
	t_{setup}			0.7		0.8	
	t_{hold}			0.1		0.2	
DFFL	Negative Edge-Triggered D-type Flip-Flop (LH/HL)						ns
	CLK-Q	LH[2]	0.9		1.1		
		HL[2]	0.8		1.0		
	t_{setup}			0.6		0.7	
	t_{hold}			0.0		0.0	

Notes:

1. Intrinsic delays have a variable component, coupled to the input slope of the signal. These numbers assume an input slope typical of local interconnect.
2. LH and HL refer to the Q transitions from Low to High and High to Low, respectively.

Table 1-30 • **Recommended Operating Conditions**

Parameter	Symbol	Limits
		Commercial/Industrial
Maximum Clock Frequency*	f_{CLOCK}	180 MHz
Maximum RAM Frequency*	f_{RAM}	150 MHz
Maximum Rise/Fall Time on Inputs*		
• Schmitt Mode (10% to 90%)	t_R/t_F	100 ns
• Non-schmitt Mode (10% to 90%)	t_R/t_F	10 ns
Maximum LVPECL Frequency*		180 MHz
Maximum t_{CK} Frequency (JTAG)	t_{CK}	10 MHz

Note: **–F parts will be 20% slower than standard commercial devices.*

Table 1-31 • **Slew Rates Measured at C = 30pF, Nominal Power Supplies and 25°C**

Type	Trig. Level	Rising Edge (nS)	Slew Rate (V/nS)	Falling Edge (nS)	Slew Rate (V/nS)	PCI Mode
OB33PH	10%-90%	1.60	1.65	1.65	1.60	Yes
OB33PN	10%-90%	1.57	1.68	3.32	0.80	No
OB33PL	10%-90%	1.57	1.68	1.99	1.32	No
OB33LH	10%-90%	3.80	0.70	4.84	0.55	No
OB33LN	10%-90%	4.19	0.63	3.37	0.78	No
OB33LL	10%-90%	5.49	0.48	2.98	0.89	No
OB25HH[2]	20%-60%	3.31	0.30	0.75	1.33	No
OB25HN[2]	20%-60%	3.20	0.32	0.77	1.30	No
OB25HL[2]	20%-60%	3.27	0.31	0.77	1.30	No
OB25LH[2]	20%-60%	8.41	0.12	1.38	0.72	No
OB25LN[2]	20%-60%	8.54	0.12	1.15	0.87	No
OB25LL[2]	20%-60%	8.50	0.12	1.19	0.84	No
OB25LPHH	10%-90%	1.55	1.29	1.56	1.28	No
OB25LPHN	10%-90%	1.70	1.18	2.08	0.96	No
OB25LPHL	10%-90%	1.97	1.02	2.09	0.96	No
OB25LPLH	10%-90%	3.57	0.56	3.93	0.51	No
OB25LPLN	10%-90%	4.65	0.43	3.28	0.61	No
OB25LPLL	10%-90%	5.52	0.36	3.44	0.58	No

Notes:

1. Standard and –F parts.
2. Please refer to the mixed-mode interfacing section in the I/O Features in ProASIC^PLUS Flash FPGAs application note for guidelines and usage.

Embedded Memory Specifications

This section discusses ProASIC^PLUS SRAM/FIFO embedded memory and its interface signals, including timing diagrams that show the relationships of signals as they pertain to single embedded memory blocks (Table 1-32). Table 1-10 on page 1-20 shows basic SRAM and FIFO configurations. Simultaneous Read and Write to the same location must be done with care. On such accesses the DI bus is output to the DO bus.

Enclosed Timing Diagrams—SRAM Mode:

- "Synchronous SRAM Read, Access Timed Output Strobe (Synchronous Transparent)"
- "Synchronous SRAM Read, Pipeline Mode Outputs (Synchronous Pipelined)"
- "Asynchronous SRAM Write"
- "Asynchronous SRAM Read, Address Controlled, RDB=0"
- "Asynchronous SRAM Read, RDB Controlled"
- "Synchronous SRAM Write"

- Embedded Memory Specifications

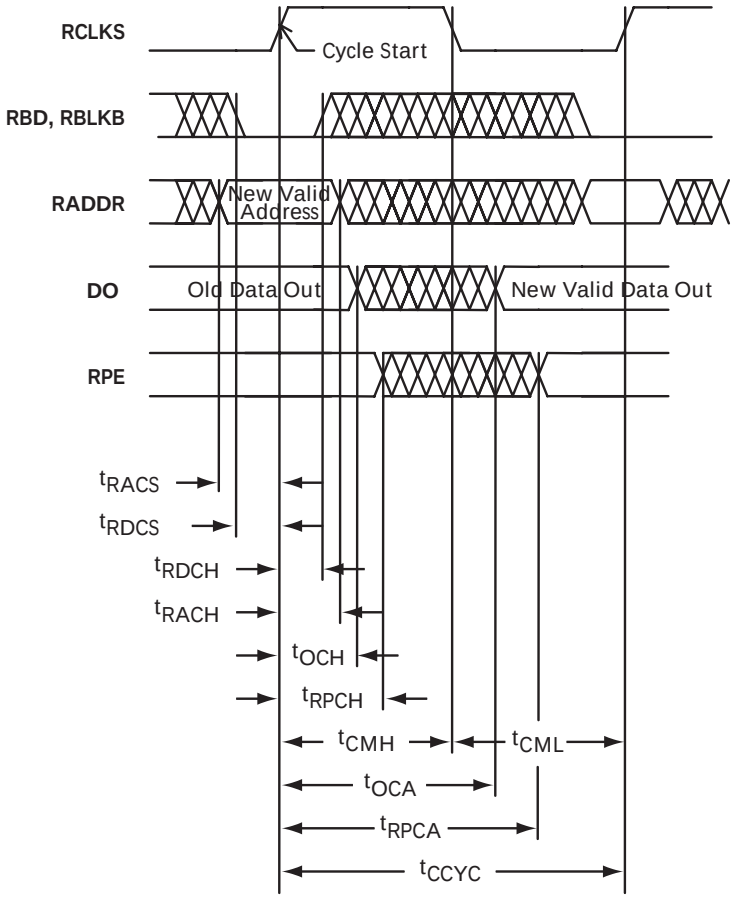
The difference between synchronous transparent and pipeline modes is the timing of all the output signals from the memory. In transparent mode, the outputs will change within the same clock cycle to reflect the data requested by the currently valid access to the memory. If clock cycles are short (high clock speed), the data requires most of the clock cycle to change to valid values (stable signals). Processing of this data in the same clock cycle is nearly impossible. Most designers add registers at all outputs of the memory to push the data processing into the next clock cycle. An entire clock cycle can then be used to process the data. To simplify use of this memory setup, suitable registers have been implemented as part of the memory primitive and are available to the user in the synchronous pipeline mode. In this mode, the output signals will change shortly after the second rising edge, following the initiation of the read access.

Table 1-32 • **Memory Block SRAM Interface Signals**

SRAM Signal	Bits	In/Out	Description
WCLKS	1	IN	Write clock used on synchronization on write side
RCLKS	1	IN	Read clock used on synchronization on read side
RADDR<0:7>	8	IN	Read address
RBLKB	1	IN	True read block select (active LOW)
RDB	1	IN	True read pulse (active LOW)
WADDR<0:7>	8	IN	Write address
WBLKB	1	IN	Write block select (active LOW)
DI<0:8>	9	IN	Input data bits <0:8>, <8> can be used for parity in
WRB	1	IN	Negative true write pulse
DO<0:8>	9	OUT	Output data bits <0:8>, <8> can be used for parity out
RPE	1	OUT	Read parity error (active HIGH)
WPE	1	OUT	Write parity error (active HIGH)
PARODD	1	IN	Selects odd parity generation/detect when high, even when low

Note: *Not all signals shown are used in all modes.*

Synchronous SRAM Read, Access Timed Output Strobe (Synchronous Transparent)



Note: *The plot shows the normal operation status.*

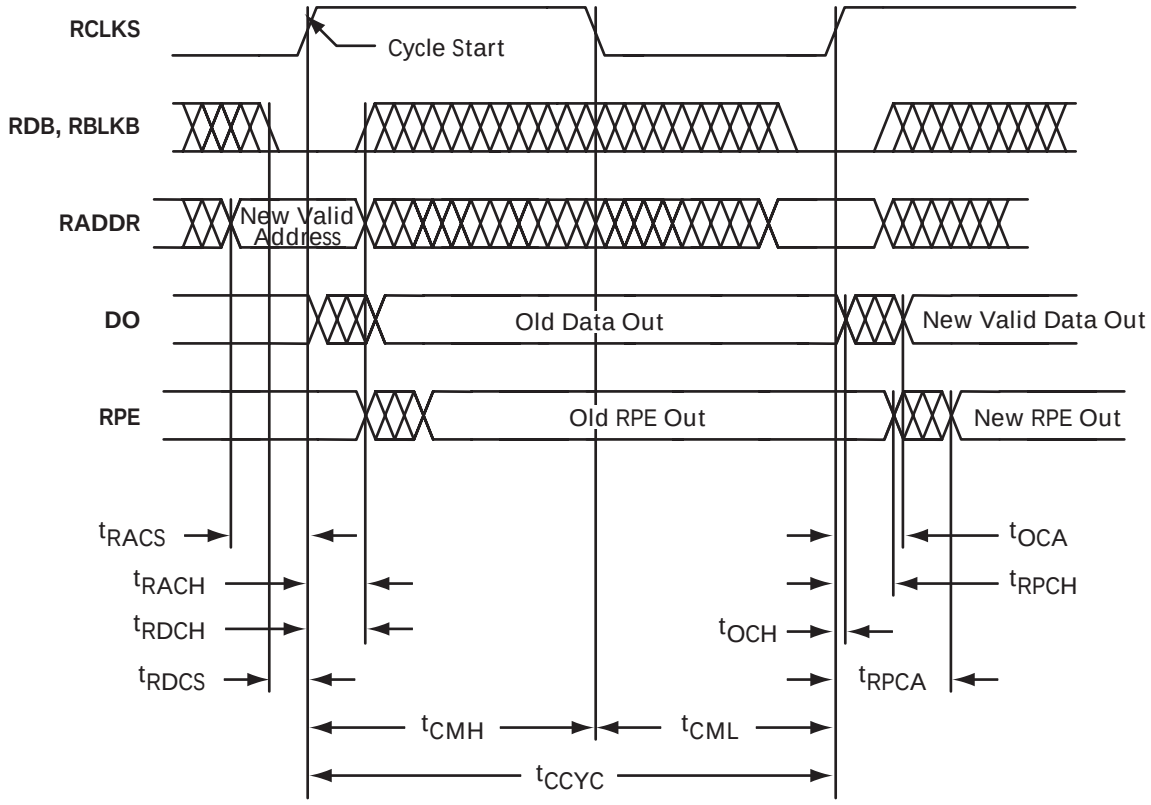
Figure 1-31 • **Synchronous SRAM Read, Access Timed Output Strobe (Synchronous Transparent)**

Table 1-33 • **T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V**

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
OCA	New DO access from RCLKS ↑	7.5		ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	
RACH	RADDR hold from RCLKS ↑	0.5		ns	
RACS	RADDR setup to RCLKS ↑	1.0		ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	9.5		ns	
RPCH	Old RPE valid from RCLKS ↑		3.0	ns	

Note: *–F speed grade devices are 20% slower than the standard numbers.*

Synchronous SRAM Read, Pipeline Mode Outputs (Synchronous Pipelined)



Note: *The plot shows the normal operation status.*

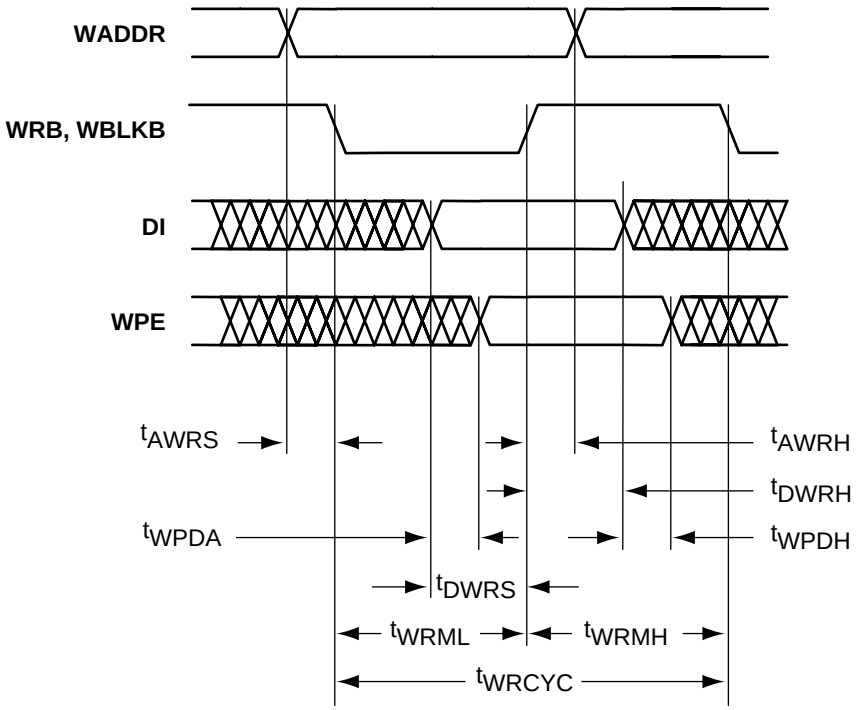
Figure 1-32 • **Synchronous SRAM Read, Pipeline Mode Outputs (Synchronous Pipelined)**

Table 1-34 • **T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V**

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
OCA	New DO access from RCLKS ↑	2.0		ns	
OCH	Old DO valid from RCLKS ↑		0.75	ns	
RACH	RADDR hold from RCLKS ↑	0.5		ns	
RACS	RADDR setup to RCLKS ↑	1.0		ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	4.0		ns	
RPCH	Old RPE valid from RCLKS ↑		1.0	ns	

Note: *–F speed grade devices are 20% slower than the standard numbers.*

Asynchronous SRAM Write



Note: *The plot shows the normal operation status.*

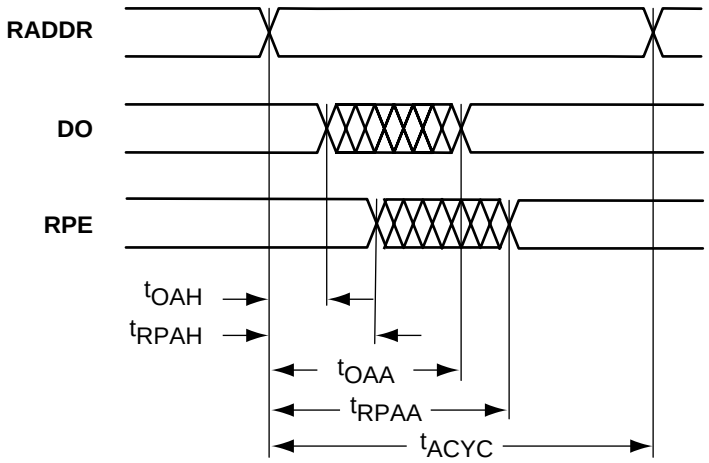
Figure 1-33 • **Asynchronous SRAM Write**

Table 1-35 • **T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V**

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
AWRH	WADDR hold from WB ↑	1.0		ns	
AWRS	WADDR setup to WB ↓	0.5		ns	
DWRH	DI hold from WB ↑	1.5		ns	
DWRS	DI setup to WB ↑	0.5		ns	PARGEN is inactive
DWRS	DI setup to WB ↑	2.5		ns	PARGEN is active
WPDA	WPE access from DI	3.0		ns	WPE is invalid while PARGEN is active
WPDH	WPE hold from DI		1.0	ns	
WRCYC	Cycle time	7.5		ns	
WRMH	WB high phase	3.0		ns	Inactive
WRML	WB low phase	3.0		ns	Active

Note: *–F speed grade devices are 20% slower than the standard numbers.*

Asynchronous SRAM Read, Address Controlled, RDB=0



Note: *The plot shows the normal operation status.*

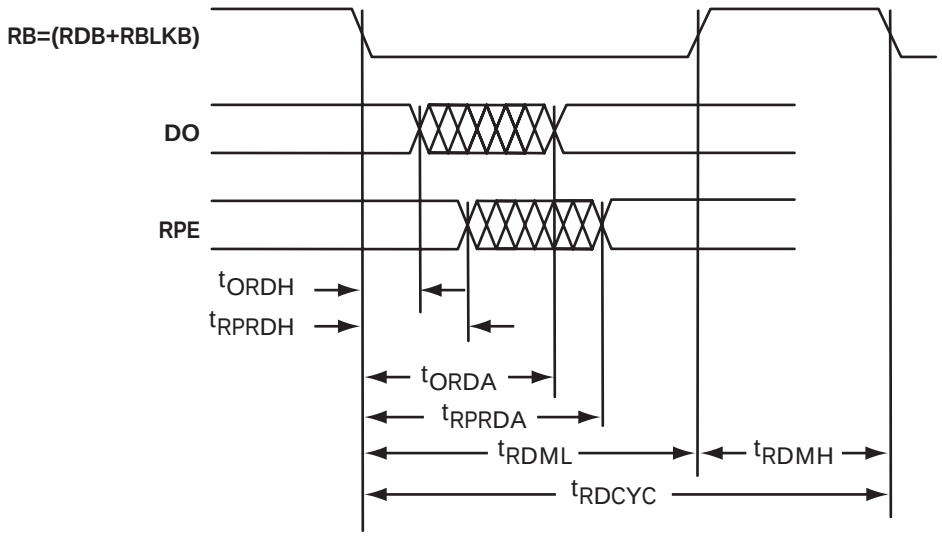
Figure 1-34 • **Asynchronous SRAM Read, Address Controlled, RDB=0**

Table 1-36 • **T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V**

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ACYC	Read cycle time	7.5		ns	
OAA	New DO access from RADDR stable	7.5		ns	
OAH	Old DO hold from RADDR stable		3.0	ns	
RPAA	New RPE access from RADDR stable	10.0		ns	
RPAH	Old RPE hold from RADDR stable		3.0	ns	

Note: *–F speed grade devices are 20% slower than the standard numbers.*

Asynchronous SRAM Read, RDB Controlled



Note: *The plot shows the normal operation status.*

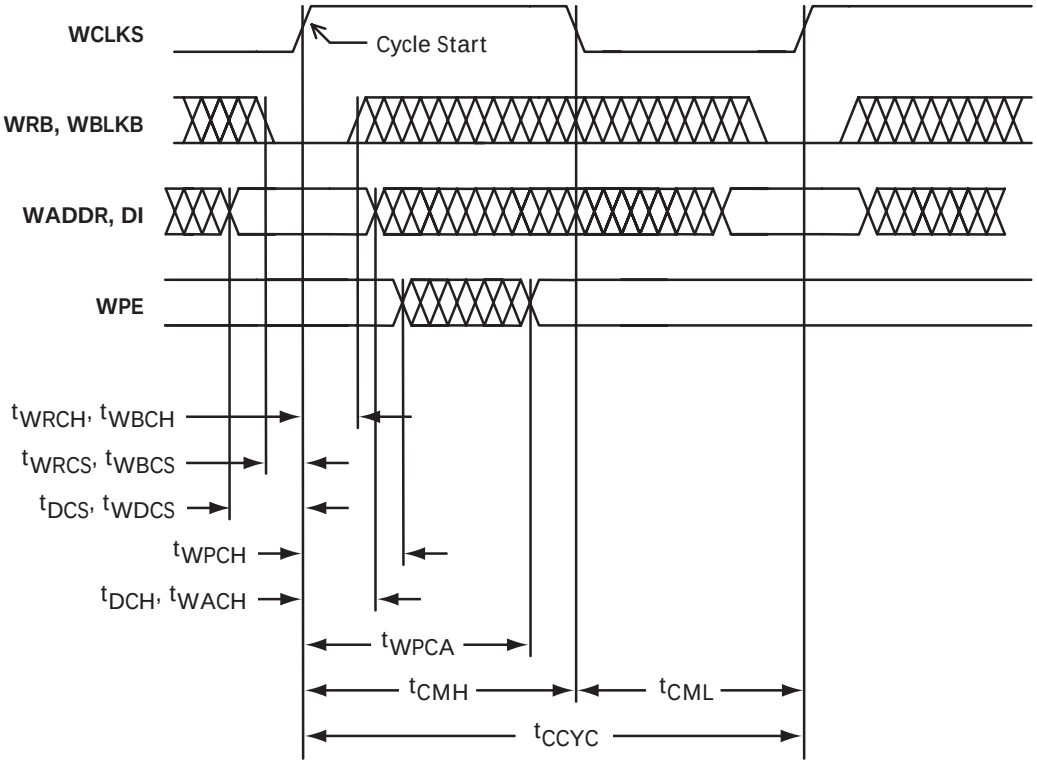
Figure 1-35 • **Asynchronous SRAM Read, RDB Controlled**

Table 1-37 • **T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V**

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDMH	RB high phase	3.0		ns	Inactive setup to new cycle
RDML	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		3.0	ns	

Note: *–F speed grade devices are 20% slower than the standard numbers.*

Synchronous SRAM Write



Note: *The plot shows the normal operation status.*

Figure 1-36 • **Synchronous SRAM Write**

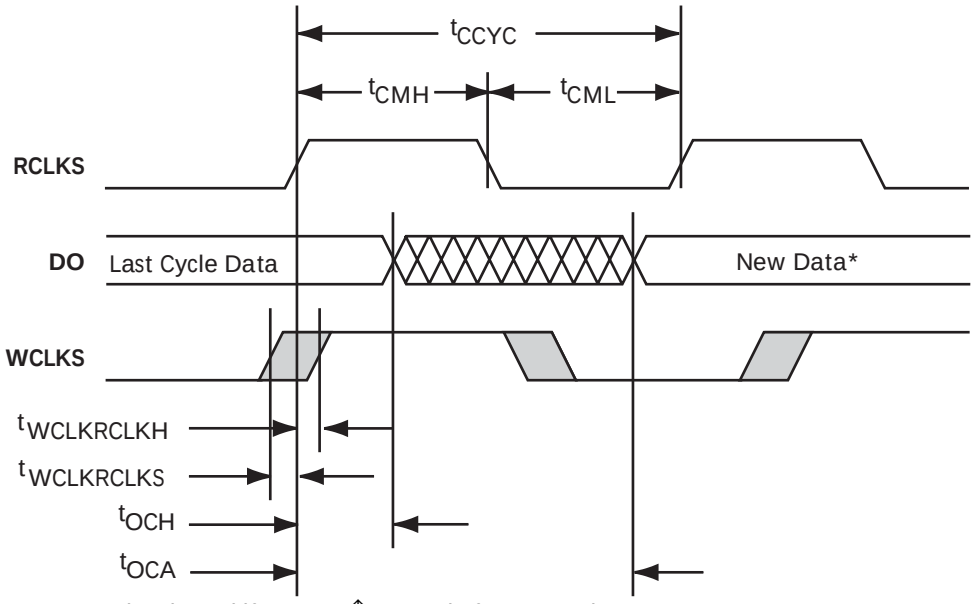
Table 1-38 • **T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V**

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	DI hold from WCLKS ↑	0.5		ns	
DCS	DI setup to WCLKS ↑	1.0		ns	
WACH	WADDR hold from WCLKS ↑	0.5		ns	
WDCS	WADDR setup to WCLKS ↑	1.0		ns	
WPCA	New WPE access from WCLKS ↑	3.0		ns	WPE is invalid while PARGEN is active
WPCH	Old WPE valid from WCLKS ↑		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from WCLKS ↑	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to WCLKS ↑	1.0		ns	

Notes:

1. On simultaneous read and write accesses to the same location DI is output to DO.
2. –F speed grade devices are 20% slower than the standard numbers.

Synchronous Write and Read to the Same Location



Note: *The plot shows the normal operation status.*

Figure 1-37 • **Synchronous Write and Read to the Same Location**

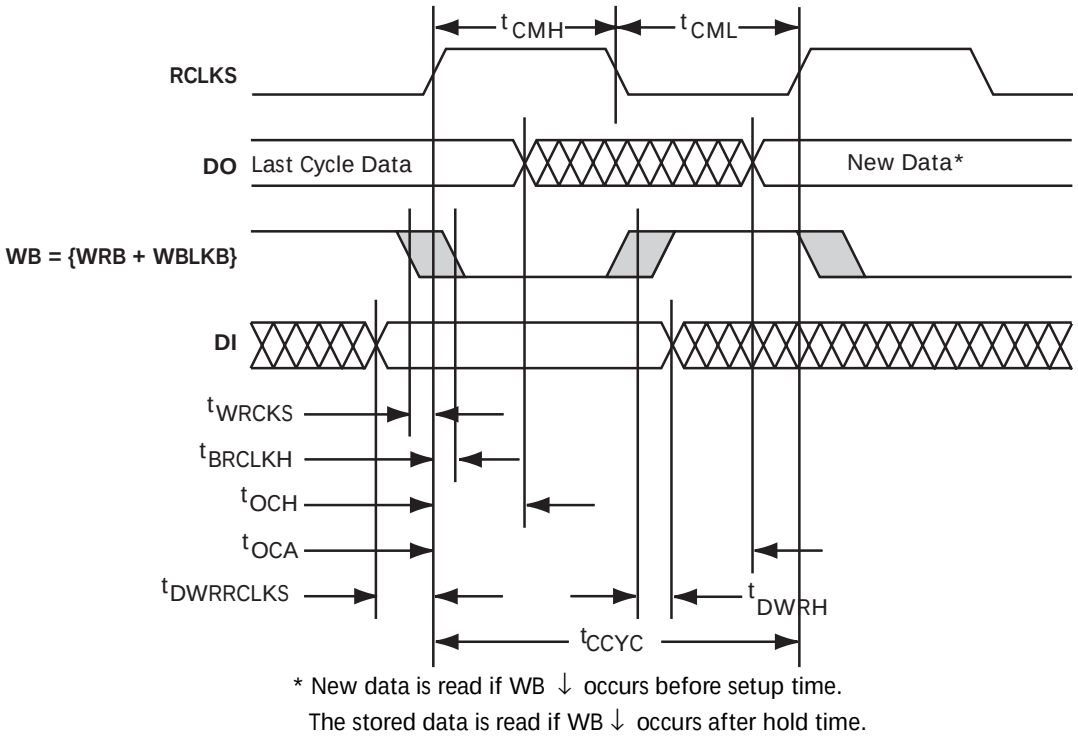
Table 1-39 • **T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V**

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
WCLKRCLKS	WCLKS ↑ to RCLKS ↑ setup time	– 0.1		ns	
WCLKRCLKH	WCLKS ↑ to RCLKS ↑ hold time		7.0	ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	OCA/OCH displayed for Access Timed Output
OCA	New DO valid from RCLKS ↑	7.5		ns	

Note:

1. This behavior is valid for Access Timed Output and Pipelined Mode Output. The table shows the timings of an Access Timed Output.
2. During synchronous write and synchronous read access to the same location, the new write data will be read out if the active write clock edge occurs before or at the same time as the active read clock edge. The negative setup time insures this behavior for WCLKS and RCLKS driven by the same design signal.
3. If WCLKS changes after the hold time, the data will be read.
4. A setup or hold time violation will result in unknown output data.
5. –F speed grade devices are 20% slower than the standard numbers.

Asynchronous Write and Synchronous Read to the Same Location



Note: *The plot shows the normal operation status.*

Figure 1-38 • **Asynchronous Write and Synchronous Read to the Same Location**

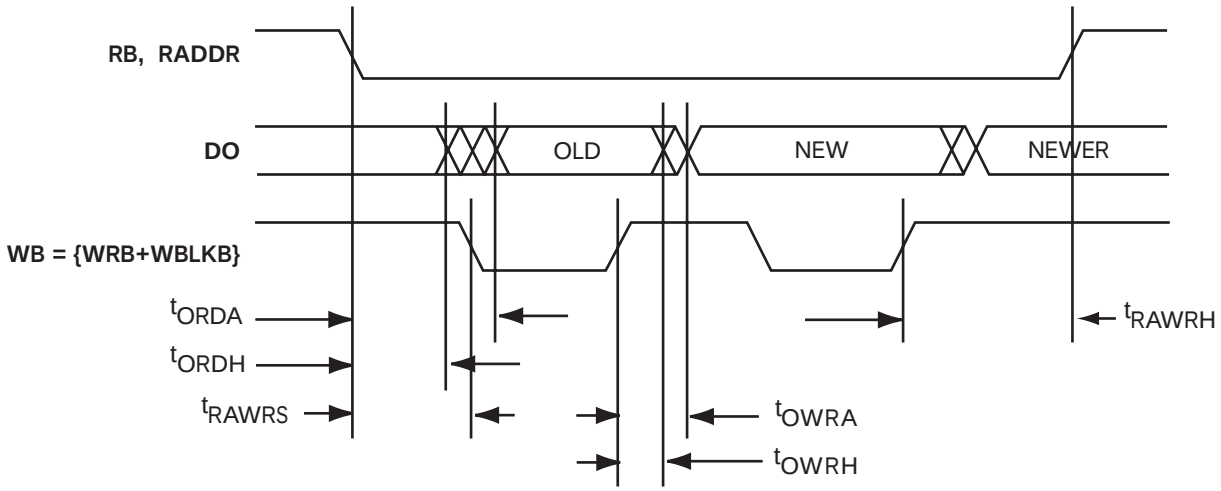
Table 1-40 • **T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V**

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
WBRCLKS	WB ↓ to RCLKS ↑ setup time	–0.1		ns	
WBRCLKH	WB ↓ to RCLKS ↑ hold time		7.0	ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	OCA/OCH displayed for Access Timed Output
OCA	New DO valid from RCLKS ↑	7.5		ns	
DWRRCLKS	DI to RCLKS ↑ setup time	0		ns	
DWRH	DI to WB ↑ hold time		1.5	ns	

Notes:

1. This behavior is valid for Access Timed Output and Pipelined Mode Output. The table shows the timings of an Access Timed Output.
2. In asynchronous write and synchronous read access to the same location, the new write data will be read out if the active write signal edge occurs before or at the same time as the active read clock edge. If WB changes to low after hold time, the data will be read.
3. A setup or hold time violation will result in unknown output data.
4. –F speed grade devices are 20% slower than the standard numbers.

Asynchronous Write and Read to the Same Location



Note: *The plot shows the normal operation status.*

Figure 1-39 • **Asynchronous Write and Read to the Same Location**

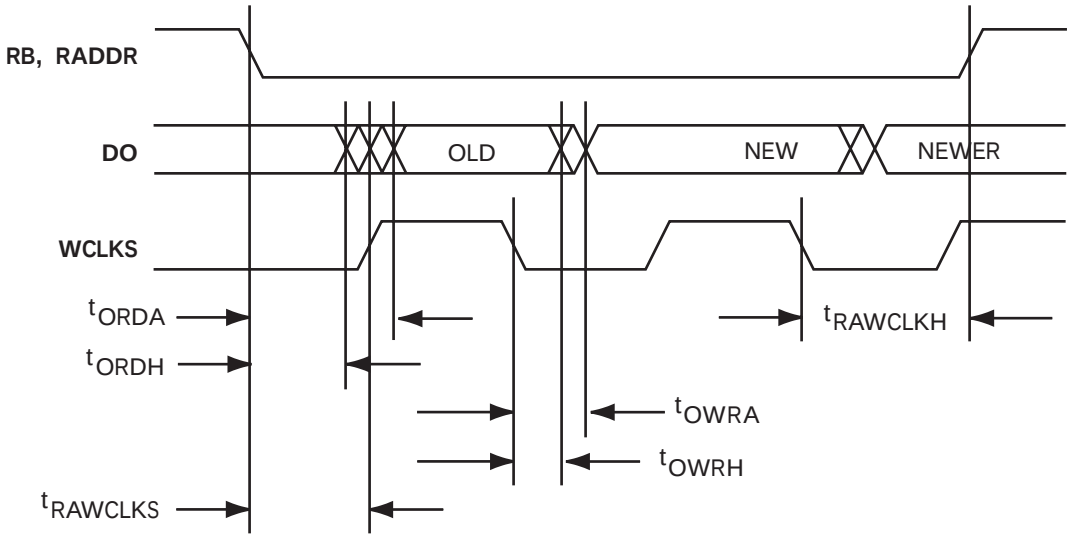
Table 1-41 • **T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V**

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
OWRA	New DO access from WB ↑	3.0		ns	
OWRH	Old DO valid from WB ↑		0.5	ns	
RAWRS	RB ↓ or RADDR from WB ↓	5.0		ns	
RAWRH	RB ↑ or RADDR from WB ↑	5.0		ns	

Notes:

1. During an asynchronous read cycle, each write operation (synchronous or asynchronous) to the same location will automatically trigger a read operation which updates the read data.
2. Violation or RAWRS will disturb access to the OLD data.
3. Violation of RAWRH will disturb access to the NEWER data.
4. –F speed grade devices are 20% slower than the standard numbers.

Synchronous Write and Asynchronous Read to the Same Location



Note: *The plot shows the normal operation status.*

Figure 1-40 • **Synchronous Write and Asynchronous Read to the Same Location**

Table 1-42 • **T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V**

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
OWRA	New DO access from WCLKS ↓	3.0		ns	
OWRH	Old DO valid from WCLKS ↓		0.5	ns	
RAWCLKS	RB ↓ or RADDR from WCLKS ↑	5.0		ns	
RAWCLKH	RB ↑ or RADDR from WCLKS ↓	5.0		ns	

Notes:

1. During an asynchronous read cycle, each write operation (synchronous or asynchronous) to the same location will automatically trigger a read operation which updates the read data.
2. Violation of RAWCLKS will disturb access to OLD data.
3. Violation of RAWCLKH will disturb access to NEWER data.
4. –F speed grade devices are 20% slower than the standard numbers.

Asynchronous FIFO Full and Empty Transitions

The asynchronous FIFO accepts writes and reads while not full or not empty. When the FIFO is full, all writes are inhibited. Conversely, when the FIFO is empty, all reads are inhibited. A problem is created if the FIFO is written during the transition out of full to not full or read during the transition out of empty to not empty. The exact time at which the write or read operation changes from inhibited to accepted after the read (write) signal which causes the transition from full or empty to not full or not empty is indeterminate. This indeterminate period starts 1 ns after the RB (WB) transition, which deactivates full or not empty and ends 3 ns after the RB (WB) transition for slow cycles. For fast cycles, the indeterminate period ends 3 ns (7.5 ns – RDL (WRL)) after the RB (WB) transition, whichever is later (Table 1-1 on page 1-6).

The timing diagram for write is shown in Figure 1-38 on page 1-51. The timing diagram for read is shown in Figure 1-39 on page 1-52. For basic SRAM configurations, see Table 1-11 on page 1-22.

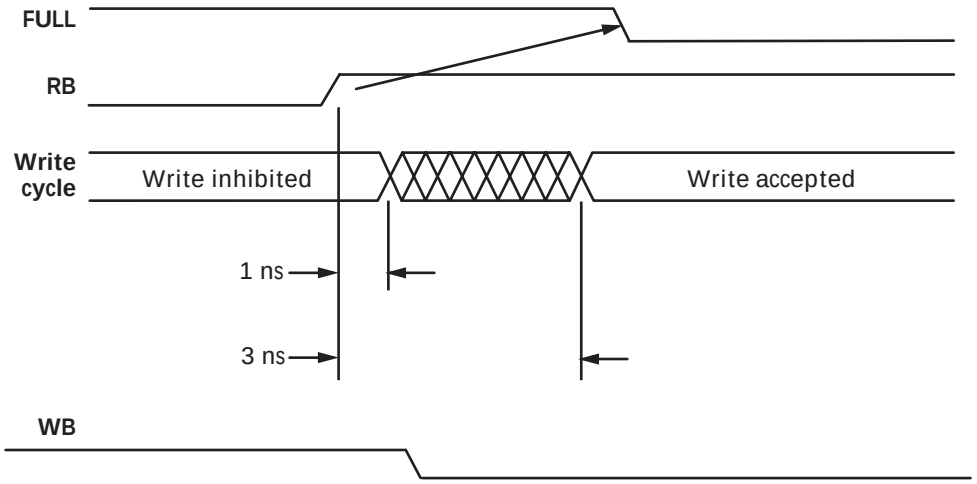
Enclosed Timing Diagrams – FIFO Mode:

- "Asynchronous FIFO Read"
- "Asynchronous FIFO Write"
- "Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)"
- "Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)"
- "Synchronous FIFO Write"
- "FIFO Reset"

Table 1-43 • **Memory Block FIFO Interface Signals**

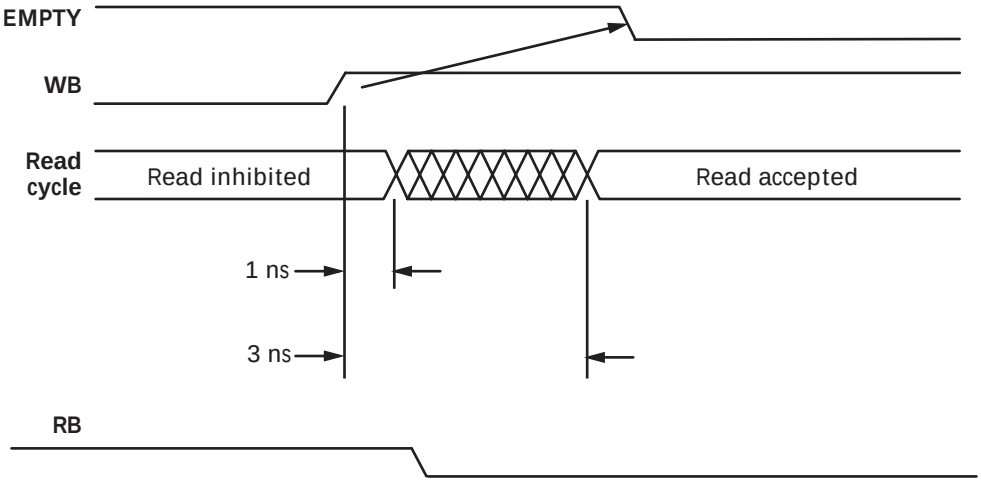
FIFO Signal	Bits	In/Out	Description
WCLKS	1	IN	Write clock used for synchronization on write side
RCLKS	1	IN	Read clock used for synchronization on read side
LEVEL <0:7>*	8	IN	Direct configuration implements static flag logic
RBLKB	1	IN	Read block select (active LOW)
RDB	1	IN	Read pulse (active LOW)
RESET	1	IN	Reset for FIFO pointers (active LOW)
WBLKB	1	IN	Write block select (active LOW)
DI<0:8>	9	IN	Input data bits <0:8>, <8> will be generated if PARGEN is true
WRB	1	IN	Write pulse (active LOW)
FULL, EMPTY	2	OUT	FIFO flags. FULL prevents write and EMPTY prevents read
EQTH, GEQTH*	2	OUT	EQTH is true when the FIFO holds the number of words specified by the LEVEL signal. GEQTH is true when the FIFO holds (LEVEL) words or more
DO<0:8>	9	OUT	Output data bits <0:8>
RPE	1	OUT	Read parity error (active HIGH)
WPE	1	OUT	Write parity error (active HIGH)
LGDEP <0:2>	3	IN	Configures DEPTH of the FIFO to $2^{(LGDEP+1)}$
PARODD	1	IN	Selects odd parity generation/detect when high, even when low

Note: **LEVEL is always eight bits (0000.0000, 0000.0001). That means for values of DEPTH greater than 256, not all values will be possible, e.g. for DEPTH=512, the LEVEL can only have the values 2, 4, . . ., 512. The LEVEL signal circuit will generate signals that indicate whether the FIFO is exactly filled to the value of LEVEL (EQTH) or filled equal or higher (GEQTH) than the specified LEVEL. Since counting starts at 0, EQTH will become true when the FIFO holds (LEVEL+1) words for 512-bit FIFOs.*



Note: *–F speed grade devices are 20% slower than the standard numbers.*

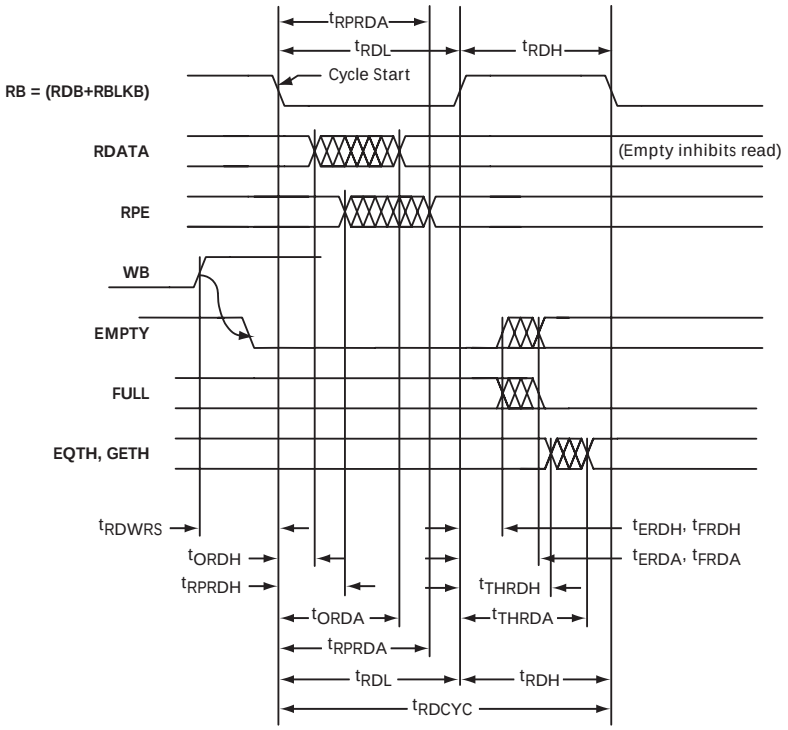
Figure 1-41 • **Write Timing Diagram**



Note: *–F speed grade devices are 20% slower than the standard numbers.*

Figure 1-42 • **Read Timing Diagram**

Asynchronous FIFO Read



Note: *The plot shows the normal operation status.*

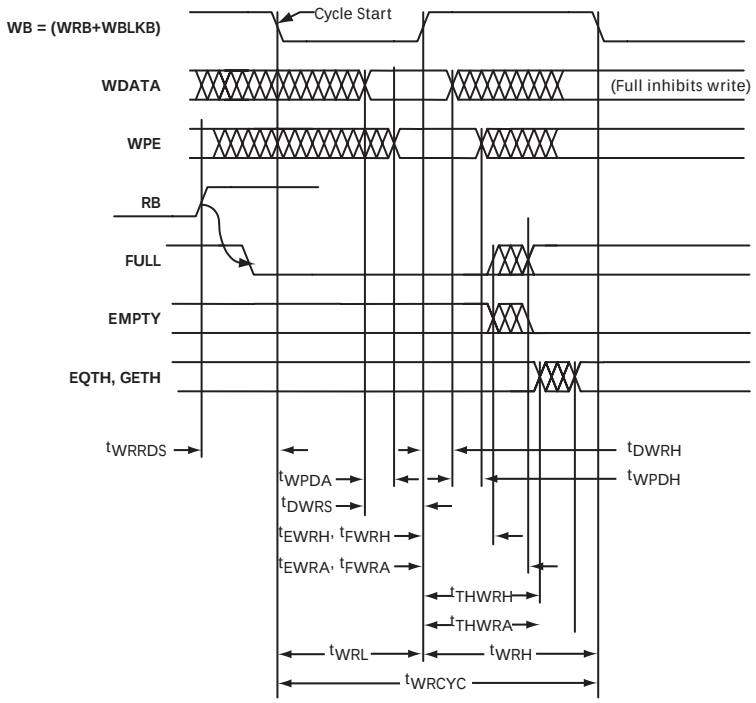
Figure 1-43 • **Asynchronous FIFO Read**

Table 1-44 • **T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V**

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ERDH, FRDH, THRDH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RB ↑		0.5	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
ERDA	New EMPTY access from RB ↑	3.0[1]		ns	
FRDA	FULL↓ access from RB ↑	3.0[1]		ns	
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDWRS	WB ↑, clearing EMPTY, setup to RB ↓	3.0[2]		ns	Enabling the read operation
			1.0	ns	Inhibiting the read operation
RDH	RB high phase	3.0		ns	Inactive
RDL	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		4.0	ns	
THRDA	EQTH or GETH access from RB↑	4.5		ns	

Notes:
1. At fast cycles, ERDA and FRDA = MAX (7.5 ns – RDL), 3.0 ns.
2. At fast cycles, RDWRS (for enabling read) = MAX (7.5 ns – WRL), 3.0 ns.
3. –F speed grade devices are 20% slower than the standard numbers.

Asynchronous FIFO Write



Note: *The plot shows the normal operation status.*

Figure 1-44 • **Asynchronous FIFO Write**

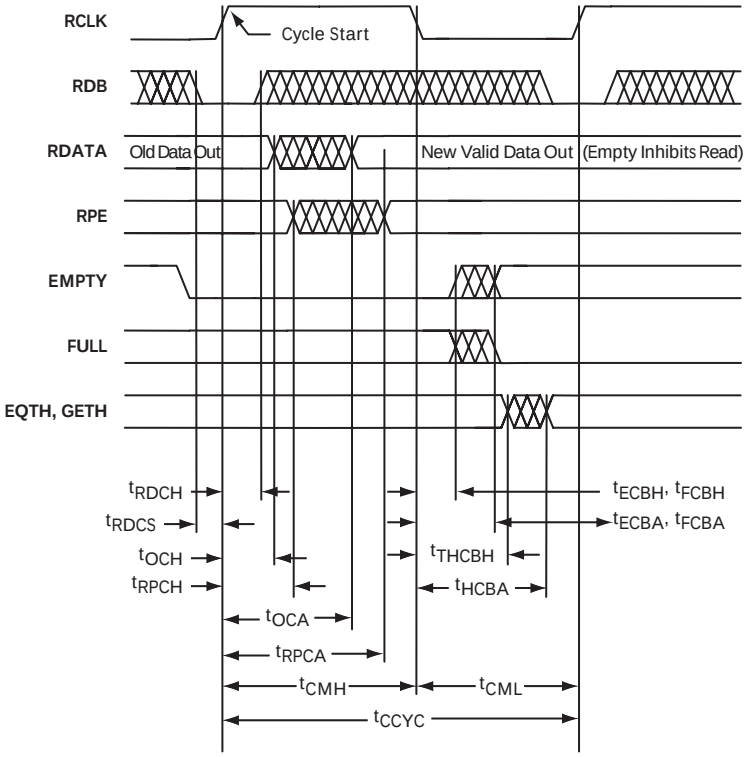
Table 1-45 • **T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V**

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
DWRH	DI hold from WB ↑	1.5		ns	
DWRS	DI setup to WB ↑	0.5		ns	PARGEN is inactive
DWRS	DI setup to WB ↑	2.5		ns	PARGEN is active
EWRH, FWRH, THWRH	Old EMPTY, FULL, EQTH, & GETH valid hold time after WB ↑		0.5	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
EWRA	EMPTY ↓ access from WB ↑	3.0[1]		ns	
FWRA	New FULL access from WB ↑	3.0[1]		ns	
THWRA	EQTH or GETH access from WB ↑	4.5		ns	
WPDA	WPE access from DI	3.0		ns	WPE is invalid while PARGEN is active
WPDH	WPE hold from DI		1.0	ns	
WRCYC	Cycle time	7.5		ns	
WRRDS	RB ↑, clearing FULL, setup to WB ↓	3.0[2]		ns	Enabling the write operation
			1.0		Inhibiting the write operation
WRH	WB high phase	3.0		ns	Inactive
WRL	WB low phase	3.0		ns	Active

Notes:

1. At fast cycles, EWRA, FWRA = MAX (7.5 ns – WRL), 3.0 ns.
2. At fast cycles, WRRDS (for enabling write) = MAX (7.5 ns – RDL), 3.0 ns.
3. –F speed grade devices are 20% slower than the standard numbers.

Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)



Note: *The plot shows the normal operation status.*

Figure 1-45 • **Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)**

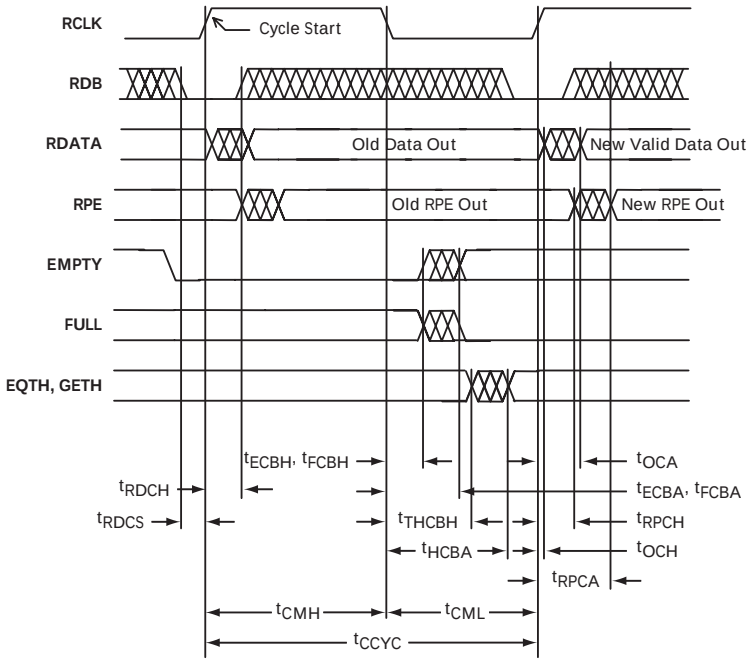
Table 1-46 • **T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V**

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from RCLKS ↓	3.0[1]		ns	
FCBA	FULL ↓ access from RCLKS ↓	3.0[1]		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
OCA	New DO access from RCLKS ↑	7.5		ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	9.5		ns	
RPCH	Old RPE valid from RCLKS ↑		3.0	ns	
HCBA	EQTH or GETH access from RCLKS ↓	4.5		ns	

Notes:

1. At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMH), 3.0 ns.
2. –F speed grade devices are 20% slower than the standard numbers.

Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)



Note: *The plot shows the normal operation status.*

Figure 1-46 • **Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)**

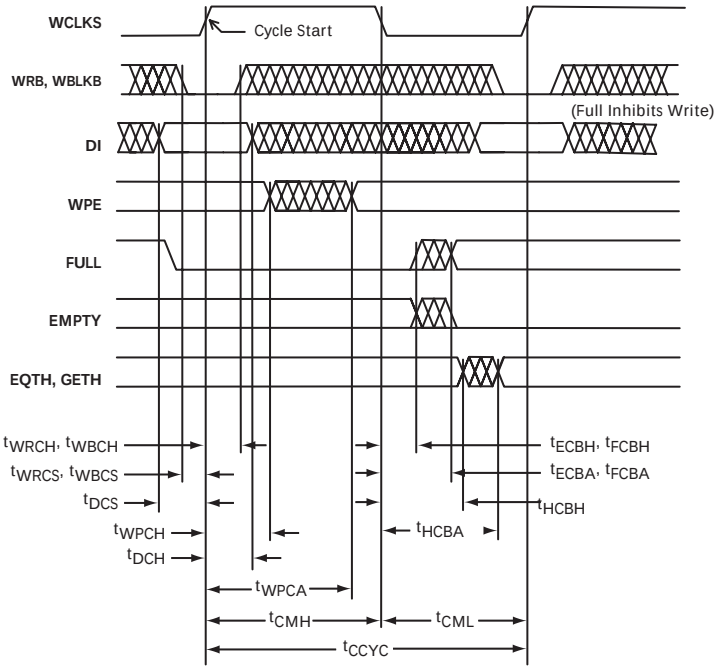
Table 1-47 • **T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V**

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from RCLKS ↓	3.0[1]		ns	
FCBA	FULL ↓ access from RCLKS ↓	3.0[1]		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
OCA	New DO access from RCLKS ↑	2.0		ns	
OCH	Old DO valid from RCLKS ↑		0.75	ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	4.0		ns	
RPCH	Old RPE valid from RCLKS ↑		1.0	ns	
HCBA	EQTH or GETH access from RCLKS ↓	4.5		ns	

Notes:

1. At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMS), 3.0 ns.
2. –F speed grade devices are 20% slower than the standard numbers.

Synchronous FIFO Write



Note: *The plot shows the normal operation status.*

Figure 1-47 • **Synchronous FIFO Write**

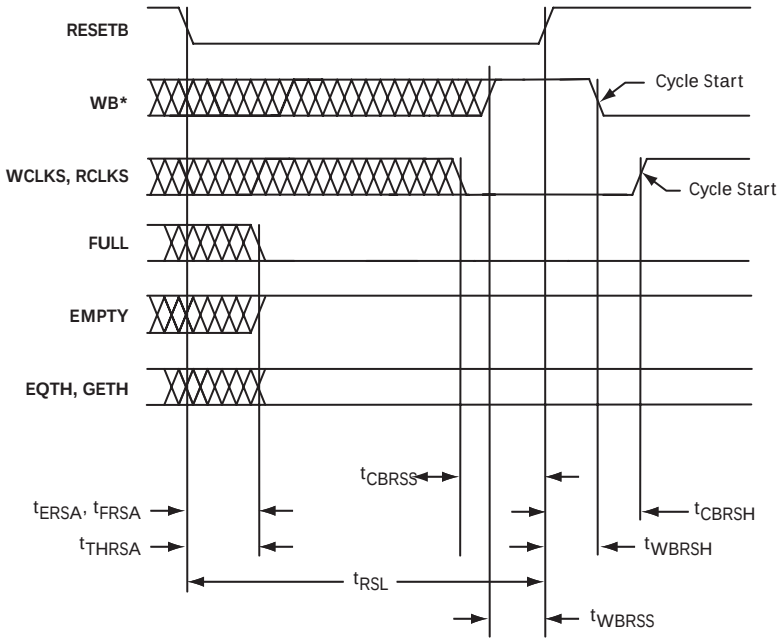
Table 1-48 • **T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V**

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	DI hold from WCLKS ↑	0.5		ns	
DCS	DI setup to WCLKS ↑	1.0		ns	
FCBA	New FULL access from WCLKS ↓	3.0[1]		ns	
ECBA	EMPTY↓ access from WCLKS ↓	3.0[1]		ns	
ECBH, FCBH, HCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from WCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
HCBA	EQTH or GETH access from WCLKS ↓	4.5		ns	
WPCA	New WPE access from WCLKS ↑	3.0		ns	WPE is invalid while PARGEN is active
WPCH	Old WPE valid from WCLKS ↑		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from WCLKS ↑	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to WCLKS ↑	1.0		ns	

Notes:

1. At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMH), 3.0 ns.
2. –F speed grade devices are 20% slower than the standard numbers.

FIFO Reset



Note: **The plot shows the normal operation status.*

Figure 1-48 • **FIFO Reset**

Table 1-49 • **T_J = 0°C to 110°C; V_{DD} = 2.3V to 2.7V**

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CBRSH	WCLKS or RCLKS ↑ hold from RESETB ↑	1.5		ns	Synchronous mode only
CBRSS	WCLKS or RCLKS ↓ setup to RESETB ↑	1.5		ns	Synchronous mode only
ERSA	New EMPTY ↑ access from RESETB ↓	3.0		ns	
FRSA	FULL ↓ access from RESETB ↓	3.0		ns	
RSL	RESETB low phase	7.5		ns	
THRSA	EQTH or GETH access from RESETB ↓	4.5		ns	
WBRSH	WB ↓ hold from RESETB ↑	1.5		ns	Asynchronous mode only
WBRSS	WB ↑ setup to RESETB ↑	1.5		ns	Asynchronous mode only

Note: *–F speed grade devices are 20% slower than the standard numbers.*

Asynchronous FIFO Full and Empty Transitions

The asynchronous FIFO accepts writes and reads while not full or not empty. When the FIFO is full, all writes are inhibited. Conversely, when the FIFO is empty, all reads are inhibited. A problem is created if the FIFO is written during the transition out of full to not full or read during the transition out of empty to not empty. The exact time at which the write or read operation changes from inhibited to accepted after the read (write) signal which causes the transition from full or empty to not full or not empty is indeterminate. This indeterminate period starts 1 ns after the RB (WB) transition, which deactivates full or not empty and ends 3 ns after the RB (WB) transition for slow cycles. For fast cycles, the indeterminate period ends 3 ns (7.5 ns – RDL (WRL)) after the RB (WB) transition, whichever is later (Table 1-43 on page 1-54).

The timing diagram for write is shown in Figure 1-41 on page 1-55. The timing diagram for read is shown in Figure 1-42 on page 1-55. For basic SRAM configurations, see Table 1-11 on page 1-22.

Enclosed Timing Diagrams – FIFO Mode:

- Asynchronous FIFO Read
- Asynchronous FIFO Write
- Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)
- Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)
- Synchronous FIFO Write
- FIFO Reset

Pin Description

User Pins

I/O **User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with standard LVTTL and LVCMOS specifications. Unused I/O pins are configured as inputs with pull-up resistors.

NC **No Connect**

To maintain compatibility with other Actel ProASICPLUS products, it is recommended that this pin not be connected to the circuitry on the board.

GL **Global Pin**

Low skew input pin for clock or other global signals. This pin can be configured with an internal pull-up resistor. When it is not connected to the global network or the clock conditioning circuit, it can be configured and used as a normal I/O.

GLMX **Global Multiplexing Pin**

Low skew input pin for clock or other global signals. This pin can be used in one of two special ways: (Please see Actel's *ProASIC^PLUS Clock Conditioning Circuits* application note for details).

1. When the external feedback option is selected for the PLL block, this pin is routed as the external feedback source to the clock conditioning circuit.
2. In applications where two different signals access the same global net (but at different times) through the use of GLMXx and GLMXLx macros, this pin will be fixed as one of the source pins.

This pin can be configured with an internal pull-up resistor. When it is not connected to the global network or the clock conditioning circuit, it can be configured and used as any normal I/O. If not used, a global will be configured as an input with pull-up.

Dedicated Pins

GND **Ground**

Common ground supply voltage.

V_{DD} **Logic Array Power Supply Pin**

2.5V supply voltage.

V_{DDP} **I/O Pad Power Supply Pin**

2.5V or 3.3V supply voltage.

TMS **Test Mode Select**

The TMS pin controls the use of boundary-scan circuitry. This pin has an internal pull-up resistor.

TCK **Test Clock**

Clock input pin for boundary scan (maximum 10 MHz). Actel recommends adding a nominal 20kΩ pull-up resistor to this pin.

TDI **Test Data In**

Serial input for boundary scan. A dedicated pull-up resistor is included to pull this pin high when not being driven.

TDO **Test Data Out**

Serial output for boundary scan. Actel recommends adding a nominal 20kΩ pull-up resistor to this pin.

TRST **Test Reset Input**

Asynchronous, active low input pin for resetting boundary-scan circuitry. This pin has an internal pull-up resistor.

Special Function Pins

RCK **Running Clock**

A free running clock is needed during programming if the programmer cannot guarantee that TCK will be uninterrupted. If not used, this pin has an internal pull-up and can be left floating.

NPECL **User Negative Input**

Provides high speed clock or data signals to the PLL block. If unused, leave the pin unconnected.

PPECL **User Positive Input**

Provides high speed clock or data signals to the PLL block. If unused, leave the pin unconnected.

AVDD **PLL Power Supply**

Analog V_{DD} should be V_{DD} (core voltage) 2.5V (nominal) and be decoupled from GND with suitable decoupling capacitors to reduce noise. For more information, refer to Actel's *Using ProASIC^PLUS Clock Conditioning Circuits* application note. If the PLLs or clock conditioning circuitry are not used in a design, AVDD should be tied high (2.5V normal).

AGND **PLL Power Ground**

Analog GND should be 0V and be decoupled from GND with suitable decoupling capacitors to reduce noise. For more information, refer to Actel's *ProASIC^PLUS Clock Conditioning Circuits* application note. If the PLLs or clock conditioning circuitry are not used in a design, AGND should be tied to GND.

V_{PP} Programming Supply Pin

This pin may be connected to any voltage between GND and 16.5V during normal operation, or it can be left unconnected.[1] For information on using this pin during programming, see the *Performing Internal In-System Programming Using Actel's ProASIC^PLUS Devices* application note. Actel recommends floating the pin or connecting it to V_{DDP}.

V_{PN} Programming Supply Pin

This pin may be connected to any voltage between GND and –13.8V during normal operation, or it can be left unconnected.[2] For information on using this pin during programming, see the *Performing Internal In-System Programming Using Actel's ProASIC^PLUS Devices* application note. Actel recommends floating the pin or connecting it to GND.

Recommended Design Practice for V_{PN}/V_{PP}

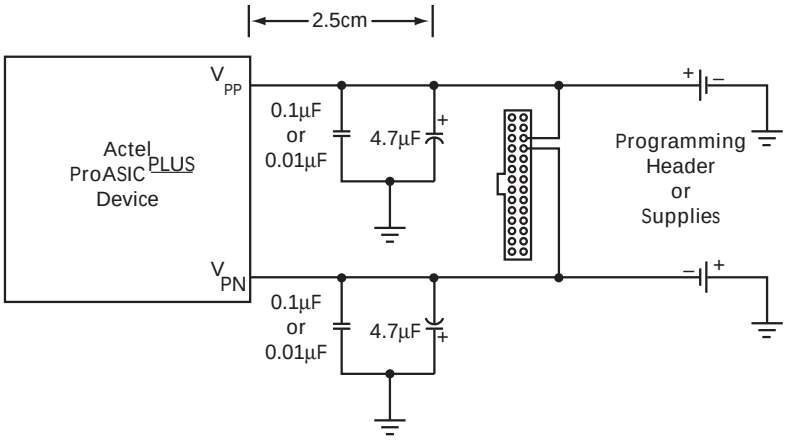
ProASIC^PLUS Devices – APA450, APA600, APA750, APA1000

Bypass capacitors are required from V_{PP} to GND and V_{PN} to GND for all ProASIC^PLUS devices during programming. During the erase cycle, ProASIC^PLUS devices may have current surges on the V_{PP} and V_{PN} power supplies. The only way to maintain the integrity of the power distribution to the ProASIC^PLUS device during these current surges is to counteract the inductance of the finite length conductors that distribute the power to the device. This can be accomplished by providing sufficient bypass capacitance between the V_{PP} and V_{PN} pins and GND (using the shortest paths possible). Without sufficient bypass capacitance to counteract the inductance, the V_{PP} and V_{PN} pins may incur a voltage spike beyond the voltage that the device can withstand. This issue applies to all programming configurations.

The power supply voltage limits are defined in the "Supply Voltages" on page 1-30. The solution prevents spikes from damaging the ProASIC^PLUS devices. Bypass capacitors are required for the V_{PP} and V_{PN} pads. Use a 0.01 µF to 0.1 µF ceramic capacitor with a 25V or greater rating. To filter low-frequency noise (decoupling), use a 4.7 µF (low ESR, <1 <Ω, tantalum, 25V or greater rating) capacitor. The capacitors should be located as close to the device pins as possible (within 2.5cm is desirable). The smaller, high-frequency capacitor should be placed closer to the device pins than the larger low-frequency capacitor. The same dual capacitor circuit should be used on both the V_{PP} and V_{PN} pins (Figure 1-49 on page 1-64).

ProASIC^PLUS Devices – APA075, APA150, APA300

These devices do not require bypass capacitors on the V_{PP} and V_{PN} pins as long as the total combined distance of the programming cable and the trace length on the board is less than or equal to 30 inches. Note: For trace lengths greater than 30 inches, use the bypass capacitor recommendations in the previous section.



(See the "Recommended Design Practice for VPN/VPP" on page 1-64)

Figure 1-49 • **ProASIC^PLUS V_{PP} and V_{PN} Capacitor Requirements**

1. *There is a nominal 40kΩ pull-up resistor on V_{PP}*
2. *There is a nominal 40kΩ pull-down resistor on V_{PN}.*