# HM5164165F Series
# HM5165165F Series

64M EDO DRAM (4-Mword × 16-bit)
8k refresh/4k refresh

HITACHI

ADE-203-1058B(Z)
Rev. 2.0
Nov. 30, 1999

## Description

The Hitachi HM5164165F Series, HM5165165F Series are 64M-bit dynamic RAMs organized as 4,194,304-word × 16-bit. They have realized high performance and low power by employing CMOS process technology. HM5164165F Series, HM5165165F Series offer Extended Data Out (EDO) Page Mode as a high speed access mode. They have the package variations of standard 50-pin plastic SOJ and standerd 50-pin plastic TSOPII

## Features

- Single 3.3 V supply: 3.3 V ± 0.3 V
- Access time: 50 ns/60 ns (max)
- Power dissipation
  - Active: 432 mW/396 mW (max) (HM5164165F Series)
    : 504 mW/432 mW (max) (HM5165165F Series)
  - Standby : 1.8 mW (max) (CMOS interface)
    : 1.1 mW (max) (L-version)
- EDO page mode capability
- Refresh cycles
  - $\overline{\text{RAS}}$-only refresh
    8192 cycles/64 ms (HM5164165F, HM5164165FL)
    4096 cycles/64 ms (HM5165165F, HM5165165FL)
  - CBR/Hidden refresh
    4096 cycles/64 ms (HM5164165F, HM5164165FL, HM5165165F, HM5165165FL)

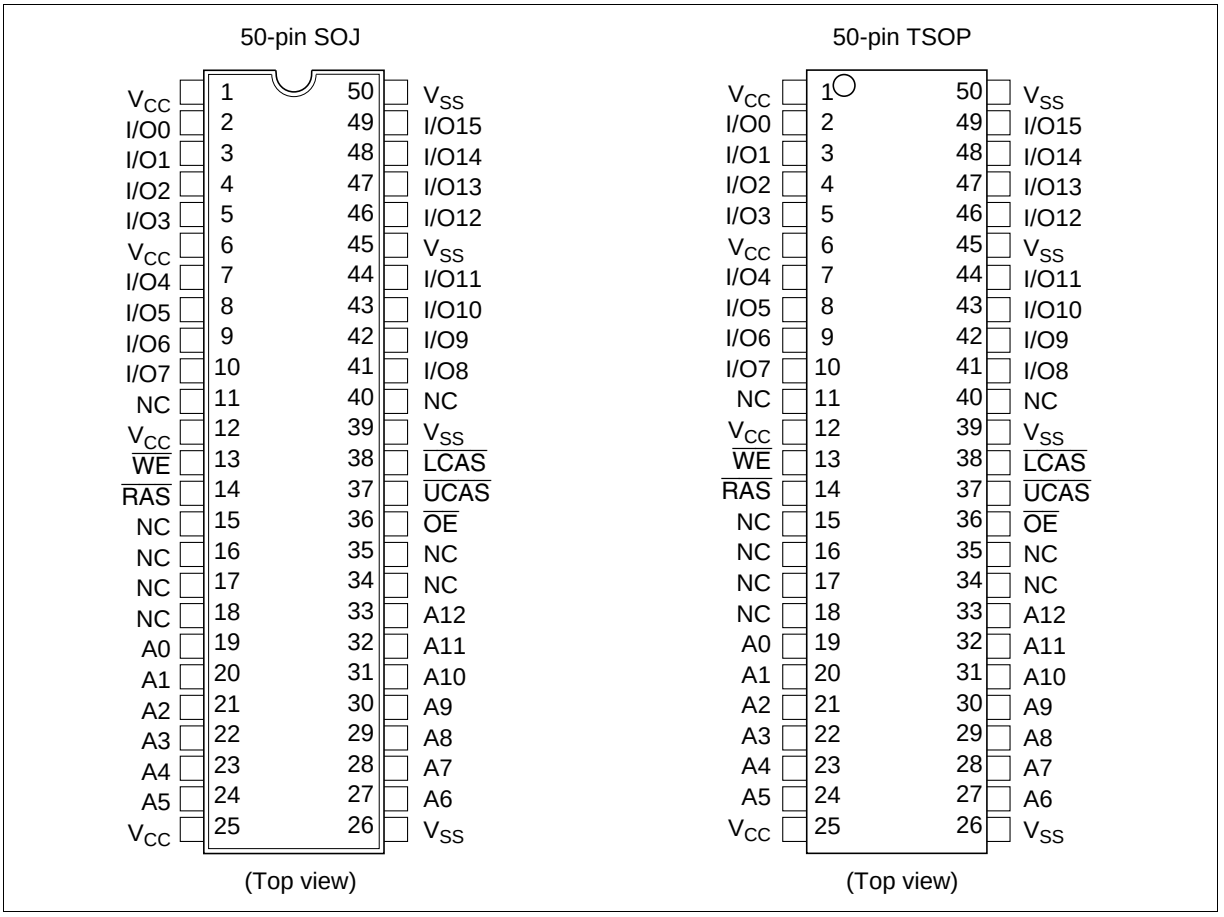
Hitachi semiconductor

- 4 variations of refresh
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
  - — Self refresh (L-version)
- 2$\overline{\text{CAS}}$-byte control
- Battery backup operation (L-version)

## Ordering Information

| Type No. | Access time | Package |
|---|---|---|
| HM5164165FJ-5 | 50 ns | 400-mil 50-pin plastic SOJ (CP-50DA) |
| HM5164165FJ-6 | 60 ns | |
| HM5164165FLJ-5 | 50 ns | |
| HM5164165FLJ-6 | 60 ns | |
| HM5165165FJ-5 | 50 ns | |
| HM5165165FJ-6 | 60 ns | |
| HM5165165FLJ-5 | 50 ns | |
| HM5165165FLJ-6 | 60 ns | |
| HM5164165FTT-5 | 50 ns | 400-mil 50-pin plastic TSOP II (TTP-50DB) |
| HM5164165FTT-6 | 60 ns | |
| HM5164165FLTT-5 | 50 ns | |
| HM5164165FLTT-6 | 60 ns | |
| HM5165165FTT-5 | 50 ns | |
| HM5165165FTT-6 | 60 ns | |
| HM5165165FLTT-5 | 50 ns | |
| HM5165165FLTT-6 | 60 ns | |

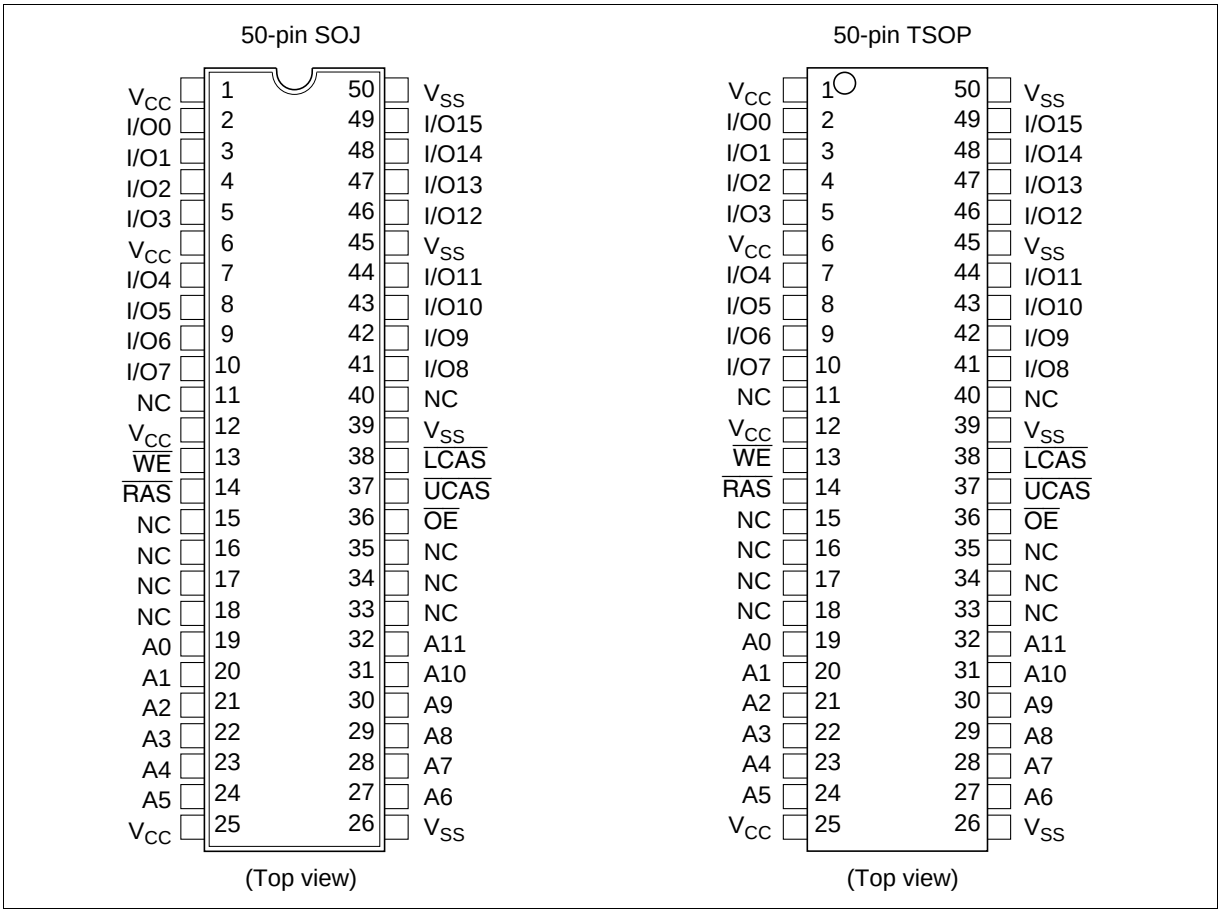
## Pin Arrangement (HM5164165F Series)




## Pin Description

| Pin name | Function |
|---|---|
| A0 to A12 | Address input<br>— Row/Refresh address A0 to A12<br>— Column address A0 to A8 |
| I/O0 to I/O15 | Data input/output |
| $\overline{RAS}$ | Row address strobe |
| $\overline{UCAS}$, $\overline{LCAS}$ | Column address strobe |
| $\overline{WE}$ | Write enable |
| $\overline{OE}$ | Output enable |
| $V_{CC}$ | Power supply |
| $V_{SS}$ | Ground |
| NC | No connection |

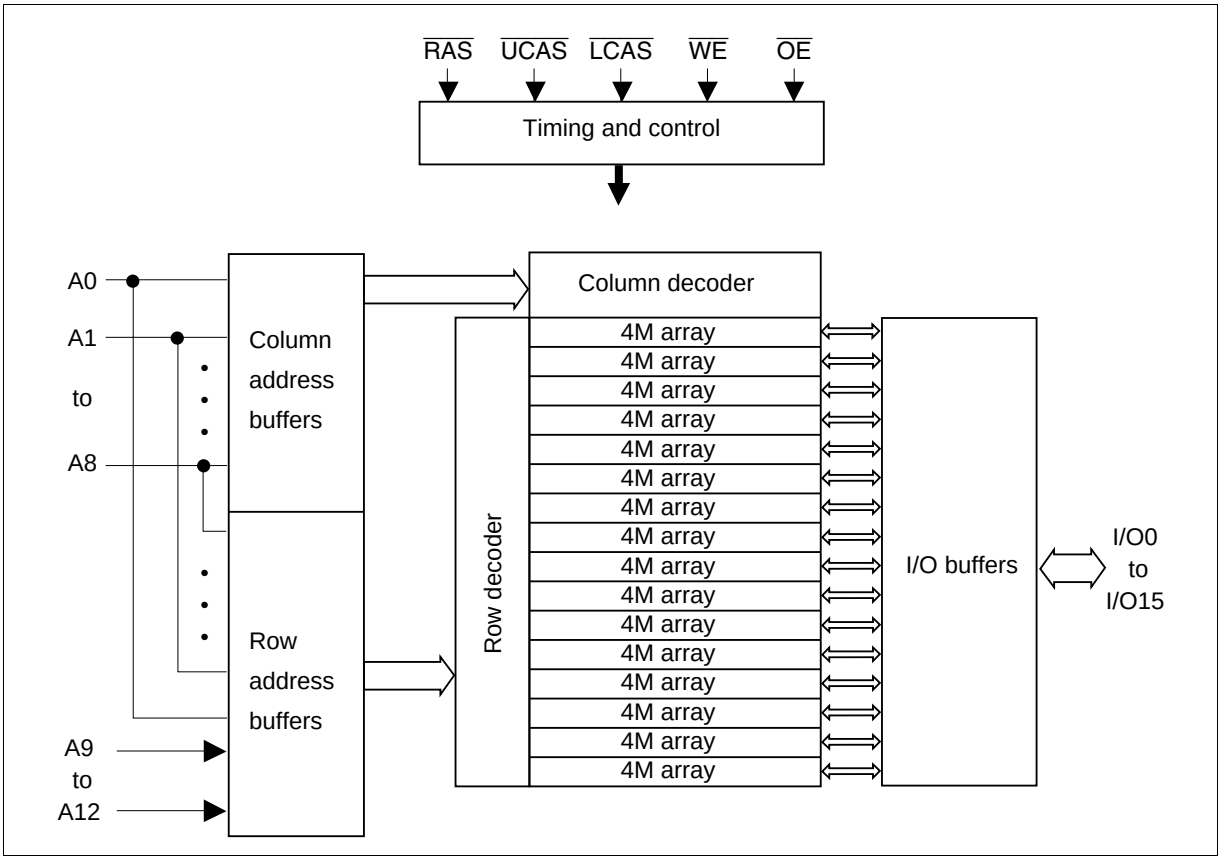
## Pin Arrangement (HM5165165F Series)



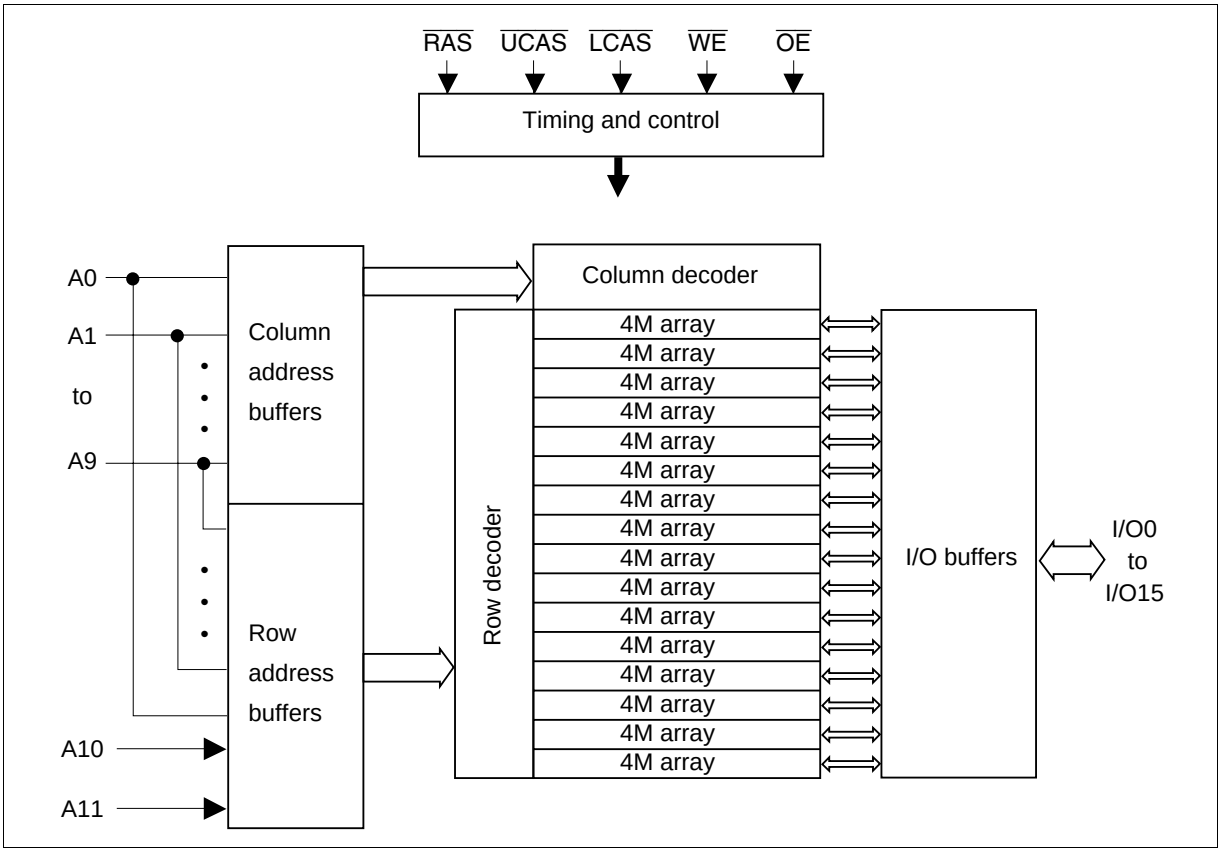

## Pin Description

| Pin name | Function |
|---|---|
| A0 to A11 | Address input<br>— Row/Refresh address A0 to A11<br>— Column address A0 to A9 |
| I/O0 to I/O15 | Data input/output |
| $\overline{RAS}$ | Row address strobe |
| $\overline{UCAS}$, $\overline{LCAS}$ | Column address strobe |
| $\overline{WE}$ | Write enable |
| $\overline{OE}$ | Output enable |
| $V_{CC}$ | Power supply |
| $V_{SS}$ | Ground |
| NC | No connection |

**Block Diagram** (HM5164165F Series)



**Block Diagram** (HM5165165F Series)



## Operation Table

| $\overline{RAS}$ | $\overline{LCAS}$ | $\overline{UCAS}$ | $\overline{WE}$ | $\overline{OE}$ | I/O 0 to I/O 7 | I/O 8 to I/O 15 | Operation |
|---|---|---|---|---|---|---|---|
| H | × | × | × | × | High-Z | High-Z | Standby |
| L | L | H | H | L | Dout | High-Z | Read cycle |
| L | H | L | H | L | High-Z | Dout | |
| L | L | L | H | L | Dout | Dout | |
| L | L | H | L*[2] | × | Din | × | Early write cycle |
| L | H | L | L*[2] | × | × | Din | |
| L | L | L | L*[2] | × | Din | Din | |
| L | L | H | L*[2] | H | Din | × | Delayed write cycle |
| L | H | L | L*[2] | H | × | Din | |
| L | L | L | L*[2] | H | Din | Din | |
| L | L | H | H to L | L to H | Dout/Din | High-Z | Read-modify-write cycle |
| L | H | L | H to L | L to H | High-Z | Dout/Din | |
| L | L | L | H to L | L to H | Dout/Din | Dout/Din | |
| L | H | H | × | × | High-Z | High-Z | $\overline{RAS}$-only refresh cycle |
| H to L | H | L | H | × | High-Z | High-Z | $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle or |
| H to L | L | H | H | × | High-Z | High-Z | Self refresh cycle (L-version) |
| H to L | L | L | H | × | High-Z | High-Z | |
| L | L | L | H | H | High-Z | High-Z | Read cycle (Output disabled) |

Notes: 1. H: $V_{IH}$ (inactive) L: $V_{IL}$ (active) ×: $V_{IH}$ or $V_{IL}$

2. $t_{WCS} \geq 0$ ns: Early write cycle
   $t_{WCS} < 0$ ns: Delayed write cycle

3. Mode is determined by the OR function of the $\overline{UCAS}$ and $\overline{LCAS}$. (Mode is set by the earliest of $\overline{UCAS}$ and $\overline{LCAS}$ active edge and reset by the latest of $\overline{UCAS}$ and $\overline{LCAS}$ inactive edge.) However write operation and output High-Z control are done independently by each $\overline{UCAS}$, $\overline{LCAS}$.
   ex. if $\overline{RAS}$ = H to L, $\overline{LCAS}$ = L, $\overline{UCAS}$ = H, then $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle is selected.

## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Terminal voltage on any pin relative to $V_{SS}$ | $V_T$ | –0.5 to $V_{CC}$ + 0.5 (≤ 4.6 V (max)) | V |
| Power supply voltage relative to $V_{SS}$ | $V_{CC}$ | –0.5 to +4.6 | V |
| Short circuit output current | Iout | 50 | mA |
| Power dissipation | $P_T$ | 1.0 | W |
| Storage temperature | Tstg | –55 to +125 | °C |

## DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V | 1, 2 |
| | $V_{SS}$ | 0 | 0 | 0 | V | 2 |
| Input high voltage | $V_{IH}$ | 2.0 | — | $V_{CC}$ + 0.3 | V | 1 |
| Input low voltage | $V_{IL}$ | –0.3 | — | 0.8 | V | 1 |
| Ambient temperature range | Ta | 0 | — | 70 | ˚C | |

Notes: 1. All voltage referred to $V_{SS}$.
2. The supply voltage with all $V_{CC}$ pins must be on the same level. The supply voltage with all $V_{SS}$ pins must be on the same level.

## DC Characteristics (HM5164165F Series)

| | | HM5164165F | | | | | |
|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Test conditions** |
| Operating current*1, *2 | $I_{CC1}$ | — | 120 | — | 110 | mA | $t_{RC}$ = min |
| Standby current | $I_{CC2}$ | — | 2 | — | 2 | mA | TTL interface<br>$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ = $V_{IH}$<br>Dout = High-Z |
| | | — | 0.5 | — | 0.5 | mA | CMOS interface<br>$\overline{RAS}$, $\overline{UCAS}$,<br>$\overline{LCAS}$ ≥ $V_{CC}$ – 0.2 V<br>Dout = High-Z |
| Standby current (L-version) | $I_{CC2}$ | — | 300 | — | 300 | µA | CMOS interface<br>$\overline{RAS}$, $\overline{UCAS}$,<br>$\overline{LCAS}$ ≥ $V_{CC}$ – 0.2 V<br>Dout = High-Z |
| $\overline{RAS}$-only refresh current*2 | $I_{CC3}$ | — | 120 | — | 110 | mA | $t_{RC}$ = min |
| Standby current*1 | $I_{CC5}$ | — | 5 | — | 5 | mA | $\overline{RAS}$ = $V_{IH}$<br>$\overline{UCAS}$, $\overline{LCAS}$ = $V_{IL}$<br>Dout = enable |
| $\overline{CAS}$-before-$\overline{RAS}$ refresh current | $I_{CC6}$ | — | 120 | — | 110 | mA | $t_{RC}$ = min |
| EDO page mode current*1, *3 | $I_{CC7}$ | — | 120 | — | 110 | mA | $\overline{RAS}$ = $V_{IL}$ , $\overline{CAS}$ cycle,<br>$t_{HPC}$ = $t_{HPC}$ min |
| Battery backup current*4 (Standby with CBR refresh) (L-version) | $I_{CC10}$ | — | 1.2 | — | 1.2 | mA | CMOS interface<br>Dout = High-Z<br>CBR refresh: $t_{RC}$ = 15.6 µs<br>$t_{RAS}$ ≤ 0.3 µs |
| Self refresh mode current (L-version) | $I_{CC11}$ | — | 500 | — | 500 | µA | CMOS interface<br>$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≤ 0.2 V<br>Dout = High-Z |
| Input leakage current | $I_{LI}$ | –5 | 5 | –5 | 5 | µA | 0 V ≤ Vin ≤ $V_{CC}$ + 0.3 V |
| Output leakage current | $I_{LO}$ | –5 | 5 | –5 | 5 | µA | 0 V ≤ Vout ≤ $V_{CC}$<br>Dout = disable |
| Output high voltage | $V_{OH}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | High Iout = –2 mA |
| Output low voltage | $V_{OL}$ | 0 | 0.4 | 0 | 0.4 | V | Low Iout = 2 mA |

Notes: 1. $I_{CC}$ depends on output load condition when the device is selected. $I_{CC}$ max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = $V_{IL}$.
3. Measured with one sequential address change per EDO cycle, $t_{HPC}$.
4. $V_{IH}$ ≥ $V_{CC}$ – 0.2 V, 0 V ≤ $V_{IL}$ ≤ 0.2 V.

## DC Characteristics (HM5165165F Series)

| | | HM5165165F | | | | | |
|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Test conditions** |
| Operating current*1, *2 | $I_{CC1}$ | — | 140 | — | 120 | mA | $t_{RC}$ = min |
| Standby current | $I_{CC2}$ | — | 2 | — | 2 | mA | TTL interface<br>$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ = $V_{IH}$<br>Dout = High-Z |
| | | — | 0.5 | — | 0.5 | mA | CMOS interface<br>$\overline{RAS}$, $\overline{UCAS}$,<br>$\overline{LCAS}$ ≥ $V_{CC}$ – 0.2 V<br>Dout = High-Z |
| Standby current (L-version) | $I_{CC2}$ | — | 300 | — | 300 | µA | CMOS interface<br>$\overline{RAS}$, $\overline{UCAS}$,<br>$\overline{LCAS}$ ≥ $V_{CC}$ – 0.2 V<br>Dout = High-Z |
| $\overline{RAS}$-only refresh current*2 | $I_{CC3}$ | — | 140 | — | 120 | mA | $t_{RC}$ = min |
| Standby current*1 | $I_{CC5}$ | — | 5 | — | 5 | mA | $\overline{RAS}$ = $V_{IH}$<br>$\overline{UCAS}$, $\overline{LCAS}$ = $V_{IL}$<br>Dout = enable |
| $\overline{CAS}$-before-$\overline{RAS}$ refresh current | $I_{CC6}$ | — | 140 | — | 120 | mA | $t_{RC}$ = min |
| EDO page mode current*1, *3 | $I_{CC7}$ | — | 120 | — | 110 | mA | $\overline{RAS}$ = $V_{IL}$ , $\overline{CAS}$ cycle,<br>$t_{HPC}$ = $t_{HPC}$ min |
| Battery backup current*4 (Standby with CBR refresh) (L-version) | $I_{CC10}$ | — | 1.2 | — | 1.2 | mA | CMOS interface<br>Dout = High-Z<br>CBR refresh: $t_{RC}$ = 15.6 µs<br>$t_{RAS}$ ≤ 0.3 µs |
| Self refresh mode current (L-version) | $I_{CC11}$ | — | 500 | — | 500 | µA | CMOS interface<br>$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≤ 0.2 V<br>Dout = High-Z |
| Input leakage current | $I_{LI}$ | –5 | 5 | –5 | 5 | µA | 0 V ≤ Vin ≤ $V_{CC}$ + 0.3 V |
| Output leakage current | $I_{LO}$ | –5 | 5 | –5 | 5 | µA | 0 V ≤ Vout ≤ $V_{CC}$<br>Dout = disable |
| Output high voltage | $V_{OH}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | High Iout = –2 mA |
| Output low voltage | $V_{OL}$ | 0 | 0.4 | 0 | 0.4 | V | Low Iout = 2 mA |

Notes: 1. $I_{CC}$ depends on output load condition when the device is selected. $I_{CC}$ max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = $V_{IL}$.
3. Measured with one sequential address change per EDO cycle, $t_{HPC}$.
4. $V_{IH}$ ≥ $V_{CC}$ – 0.2 V, 0 V ≤ $V_{IL}$ ≤ 0.2 V.

**Capacitance** (Ta = 25°C, $V_{CC}$ = 3.3 V ± 0.3 V)

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Input capacitance (Address) | $C_{I1}$ | — | — | 5 | pF | 1 |
| Input capacitance (Clocks) | $C_{I2}$ | — | — | 7 | pF | 1 |
| Output capacitance (Data-in, Data-out) | $C_{I/O}$ | — | — | 7 | pF | 1, 2 |

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{RAS}$, $\overline{UCAS}$ and $\overline{LCAS}$ = $V_{IH}$ to disable Dout.

## AC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0 V)*[1, *2, *19, *26]

### Test Conditions

- Input rise and fall time: 2 ns
- Input pulse levels: $V_{IL}$ = 0 V, $V_{IH}$ = 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + $C_L$ (100 pF) (Including scope and jig)

### Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

| | | HM5164165F/HM5165165F | | | | | |
|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Unit | Notes |
| Random read or write cycle time | $t_{RC}$ | 84 | — | 104 | — | ns | |
| $\overline{RAS}$ precharge time | $t_{RP}$ | 30 | — | 40 | — | ns | |
| $\overline{CAS}$ precharge time | $t_{CP}$ | 8 | — | 10 | — | ns | 30 |
| $\overline{RAS}$ pulse width | $t_{RAS}$ | 50 | 10000 | 60 | 10000 | ns | |
| $\overline{CAS}$ pulse width | $t_{CAS}$ | 8 | 10000 | 10 | 10000 | ns | |
| Row address setup time | $t_{ASR}$ | 0 | — | 0 | — | ns | |
| Row address hold time | $t_{RAH}$ | 8 | — | 10 | — | ns | |
| Column address setup time | $t_{ASC}$ | 0 | — | 0 | — | ns | 27 |
| Column address hold time | $t_{CAH}$ | 8 | — | 10 | — | ns | 27 |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | $t_{RCD}$ | 12 | 37 | 14 | 45 | ns | 3 |
| $\overline{RAS}$ to column address delay time | $t_{RAD}$ | 10 | 25 | 12 | 30 | ns | 4 |
| $\overline{RAS}$ hold time | $t_{RSH}$ | 13 | — | 15 | — | ns | |
| $\overline{CAS}$ hold time | $t_{CSH}$ | 35 | — | 40 | — | ns | |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | $t_{CRP}$ | 5 | — | 5 | — | ns | 28 |
| $\overline{OE}$ to Din delay time | $t_{OED}$ | 13 | — | 15 | — | ns | 5 |
| $\overline{OE}$ delay time from Din | $t_{DZO}$ | 0 | — | 0 | — | ns | 6 |
| $\overline{CAS}$ delay time from Din | $t_{DZC}$ | 0 | — | 0 | — | ns | 6 |
| Transition time (rise and fall) | $t_T$ | 2 | 50 | 2 | 50 | ns | 7 |

**Read Cycle**

| | | HM5164165F/HM5165165F | | | | | |
|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Access time from $\overline{RAS}$ | $t_{RAC}$ | — | 50 | — | 60 | ns | 8, 9 |
| Access time from $\overline{CAS}$ | $t_{CAC}$ | — | 13 | — | 15 | ns | 9, 10, 17 |
| Access time from address | $t_{AA}$ | — | 25 | — | 30 | ns | 9, 11, 17 |
| Access time from $\overline{OE}$ | $t_{OEA}$ | — | 13 | — | 15 | ns | 9 |
| Read command setup time | $t_{RCS}$ | 0 | — | 0 | — | ns | 27 |
| Read command hold time to $\overline{CAS}$ | $t_{RCH}$ | 0 | — | 0 | — | ns | 12, 28 |
| Read command hold time from $\overline{RAS}$ | $t_{RCHR}$ | 50 | — | 60 | — | ns | |
| Read command hold time to $\overline{RAS}$ | $t_{RRH}$ | 0 | — | 0 | — | ns | 12 |
| Column address to $\overline{RAS}$ lead time | $t_{RAL}$ | 25 | — | 30 | — | ns | |
| Column address to $\overline{CAS}$ lead time | $t_{CAL}$ | 15 | — | 18 | — | ns | |
| $\overline{CAS}$ to output in low-Z | $t_{CLZ}$ | 0 | — | 0 | — | ns | |
| Output data hold time | $t_{OH}$ | 3 | — | 3 | — | ns | 21 |
| Output data hold time from $\overline{OE}$ | $t_{OHO}$ | 3 | — | 3 | — | ns | |
| Output buffer turn-off time | $t_{OFF}$ | — | 13 | — | 15 | ns | 13, 21 |
| Output buffer turn-off to $\overline{OE}$ | $t_{OEZ}$ | — | 13 | — | 15 | ns | 13 |
| $\overline{CAS}$ to Din delay time | $t_{CDD}$ | 13 | — | 15 | — | ns | 5 |
| Output data hold time from $\overline{RAS}$ | $t_{OHR}$ | 3 | — | 3 | — | ns | 21 |
| Output buffer turn-off to $\overline{RAS}$ | $t_{OFR}$ | — | 13 | — | 15 | ns | 13, 21 |
| Output buffer turn-off to $\overline{WE}$ | $t_{WEZ}$ | — | 13 | — | 15 | ns | 13 |
| $\overline{WE}$ to Din delay time | $t_{WED}$ | 13 | — | 15 | — | ns | |
| $\overline{RAS}$ to Din delay time | $t_{RDD}$ | 13 | — | 15 | — | ns | |

### Write Cycle

| | | HM5164165F/HM5165165F | | | | | |
|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Write command setup time | $t_{WCS}$ | 0 | — | 0 | — | ns | 14, 27 |
| Write command hold time | $t_{WCH}$ | 8 | — | 10 | — | ns | 27 |
| Write command pulse width | $t_{WP}$ | 8 | — | 10 | — | ns | |
| Write command to $\overline{RAS}$ lead time | $t_{RWL}$ | 13 | — | 15 | — | ns | |
| Write command to $\overline{CAS}$ lead time | $t_{CWL}$ | 8 | — | 10 | — | ns | 29 |
| Data-in setup time | $t_{DS}$ | 0 | — | 0 | — | ns | 15, 29 |
| Data-in hold time | $t_{DH}$ | 8 | — | 10 | — | ns | 15, 29 |

### Read-Modify-Write Cycle

| | | HM5164165F/HM5165165F | | | | | |
|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Read-modify-write cycle time | $t_{RWC}$ | 116 | — | 140 | — | ns | |
| $\overline{RAS}$ to $\overline{WE}$ delay time | $t_{RWD}$ | 67 | — | 79 | — | ns | 14 |
| $\overline{CAS}$ to $\overline{WE}$ delay time | $t_{CWD}$ | 30 | — | 34 | — | ns | 14 |
| Column address to $\overline{WE}$ delay time | $t_{AWD}$ | 42 | — | 49 | — | ns | 14 |
| $\overline{OE}$ hold time from $\overline{WE}$ | $t_{OEH}$ | 13 | — | 15 | — | ns | |

### Refresh Cycle

| | | HM5164165F/HM5165165F | | | | | |
|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| $\overline{CAS}$ setup time (CBR refresh cycle) | $t_{CSR}$ | 5 | — | 5 | — | ns | 27 |
| $\overline{CAS}$ hold time (CBR refresh cycle) | $t_{CHR}$ | 8 | — | 10 | — | ns | 28 |
| $\overline{WE}$ setup time (CBR refresh cycle) | $t_{WRP}$ | 0 | — | 0 | — | ns | |
| $\overline{WE}$ hold time (CBR refresh cycle) | $t_{WRH}$ | 8 | — | 10 | — | ns | |
| $\overline{RAS}$ precharge to $\overline{CAS}$ hold time | $t_{RPC}$ | 5 | — | 5 | — | ns | 27 |

### EDO Page Mode Cycle

| | | HM5164165F/HM5165165F | | | | | |
|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| EDO page mode cycle time | $t_{HPC}$ | 20 | — | 25 | — | ns | 20 |
| EDO page mode $\overline{RAS}$ pulse width | $t_{RASP}$ | — | 100000 | — | 100000 | ns | 16 |
| Access time from $\overline{CAS}$ precharge | $t_{CPA}$ | — | 28 | — | 35 | ns | 9, 17, 28 |
| $\overline{RAS}$ hold time from $\overline{CAS}$ precharge | $t_{CPRH}$ | 28 | — | 35 | — | ns | |
| Output data hold time from $\overline{CAS}$ low | $t_{DOH}$ | 3 | — | 3 | — | ns | 9, 22 |
| $\overline{CAS}$ hold time referred $\overline{OE}$ | $t_{COL}$ | 8 | — | 10 | — | ns | |
| $\overline{CAS}$ to $\overline{OE}$ setup time | $t_{COP}$ | 5 | — | 5 | — | ns | |
| Read command hold time from $\overline{CAS}$ precharge | $t_{RCHC}$ | 28 | — | 35 | — | ns | |
| Write pulse width during $\overline{CAS}$ precharge | $t_{WPE}$ | 8 | — | 10 | — | ns | |
| $\overline{OE}$ precharge time | $t_{OEP}$ | 8 | — | 10 | — | ns | |

### EDO Page Mode Read-Modify-Write Cycle

| | | HM5164165F/HM5165165F | | | | | |
|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| EDO page mode read-modify-write cycle time | $t_{HPRWC}$ | 57 | — | 68 | — | ns | |
| $\overline{WE}$ delay time from $\overline{CAS}$ precharge | $t_{CPW}$ | 45 | — | 54 | — | ns | 14, 28 |

### Refresh (HM5164165F Series)

| **Parameter** | **Symbol** | **Max** | **Unit** | **Note** |
|---|---|---|---|---|
| Refresh period | $t_{REF}$ | 64 | ms | 8192 cycles |

**Refresh** (HM5165165F Series)

| Parameter | Symbol | Max | Unit | Note |
|---|---|---|---|---|
| Refresh period | $t_{REF}$ | 64 | ms | 4096 cycles |

**Self Refresh Mode** (L-version)

| | | HM5164165FL/HM5165165FL | | | | | |
|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Unit | Notes |
| $\overline{RAS}$ pulse width (self refresh) | $t_{RASS}$ | 100 | — | 100 | — | µs | 25 |
| $\overline{RAS}$ precharge time (self refresh) | $t_{RPS}$ | 90 | — | 110 | — | ns | 25 |
| $\overline{CAS}$ hold time (self refresh) | $t_{CHS}$ | –50 | — | –50 | — | ns | 29 |

Notes:
1. AC measurements assume $t_T$ = 2 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh).
3. Operation with the $t_{RCD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RCD}$ (max) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, than the access time is controlled exclusively by $t_{CAC}$.
4. Operation with the $t_{RAD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RAD}$ (max) is specified as a reference point only; if $t_{RAD}$ is greater than the specified $t_{RAD}$ (max) limit, then access time is controlled exclusively by $t_{AA}$.
5. Either $t_{OED}$ or $t_{CDD}$ must be satisfied.
6. Either $t_{DZO}$ or $t_{DZC}$ must be satisfied.
7. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$ (min) and $V_{IL}$ (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If $t_{RCD}$ or $t_{RAD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycles.
13. $t_{OFF}$ (max), $t_{OEZ}$ (max), $t_{WEZ}$ (max) and $t_{OFR}$ (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{AWD}$ and $t_{CPW}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. $t_{DS}$ and $t_{DH}$ are referred to $\overline{UCAS}$ and $\overline{LCAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

16. $t_{RASP}$ defines $\overline{RAS}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among $t_{AA}$, $t_{CAC}$ and $t_{CPA}$.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
19. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large $V_{CC}/V_{SS}$ line noise, which causes to degrade $V_{IH}$ min/$V_{IL}$ max level.
20. $t_{HPC}$ (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2\ t_T$) becomes greater than the specified $t_{HPC}$ (min) value.The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between $t_{OHR}$ and $t_{OH}$, and between $t_{OFR}$ and $t_{OFF}$.
22. $t_{DOH}$ defines the time at which the output level go cross. $V_{OL}$ = 0.8 V, $V_{OH}$ = 2.0 V of output timing reference level.
23. Before and after self refresh mode, execute CBR refresh to all refresh addresses in or within 64 ms period on the condition a and b below.
    a. Enter self refresh mode within 15.6 µs after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
    b. Start burst refresh or distributed refresh at equal interval to all refresh addresses within 15.6µs after exiting from self refresh mode.
24. In case of entering from $\overline{RAS}$-only-refresh, it is necessary to execute CBR refresh before and after self refresh mode according as note 23.
25 At $t_{RASS}$ > 100 µs, self refresh mode is activated, and not activated at $t_{RASS}$ < 10 µs. It is undefined within the range of 10 µs ≤ $t_{RASS}$ ≤ 100 µs. For $t_{RASS}$ ≥ 10 µs, it is necessary to satisfy $t_{RPS}$.
26. When both $\overline{UCAS}$ and $\overline{LCAS}$ go low at the same time, all 16-bit data are written into the device. $\overline{UCAS}$ and $\overline{LCAS}$ cannot be staggered within the same write/read cycles.
27. $t_{ASC}$, $t_{CAH}$, $t_{RCS}$, $t_{WCS}$, $t_{WCH}$, $t_{CSR}$ and $t_{RPC}$ are determined by the earlier falling edge of $\overline{UCAS}$ or $\overline{LCAS}$.
28. $t_{CRP}$, $t_{CHR}$, $t_{RCH}$, $t_{CPA}$ and $t_{CPW}$ are determined by the later rising edge of $\overline{UCAS}$ or $\overline{LCAS}$.
29. $t_{CWL}$, $t_{DH}$, $t_{DS}$ and $t_{CHS}$ should be satisfied by both $\overline{UCAS}$ and $\overline{LCAS}$.
30. $t_{CP}$ is determined by the time that both $\overline{UCAS}$ and $\overline{LCAS}$ are high.
31. XXX: H or L (H: $V_{IH}$ (min) ≤ $V_{IN}$ ≤ $V_{IH}$ (max), L: $V_{IL}$ (min) ≤ $V_{IN}$ ≤ $V_{IL}$ (max))

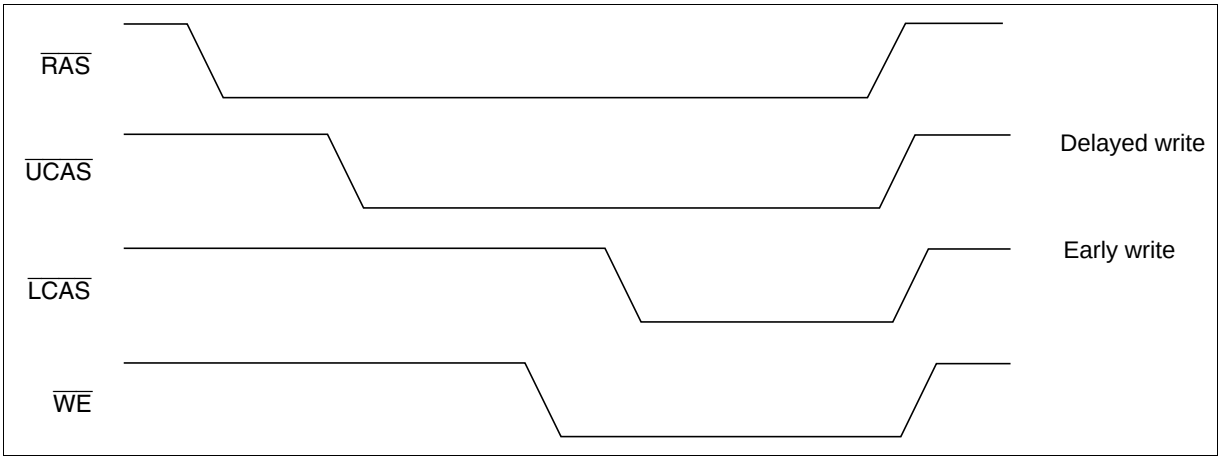
    ///////: Invalid Dout

    When the address, clock and input pins are not described on timing waveforms, their pins must be applied $V_{IH}$ or $V_{IL}$.

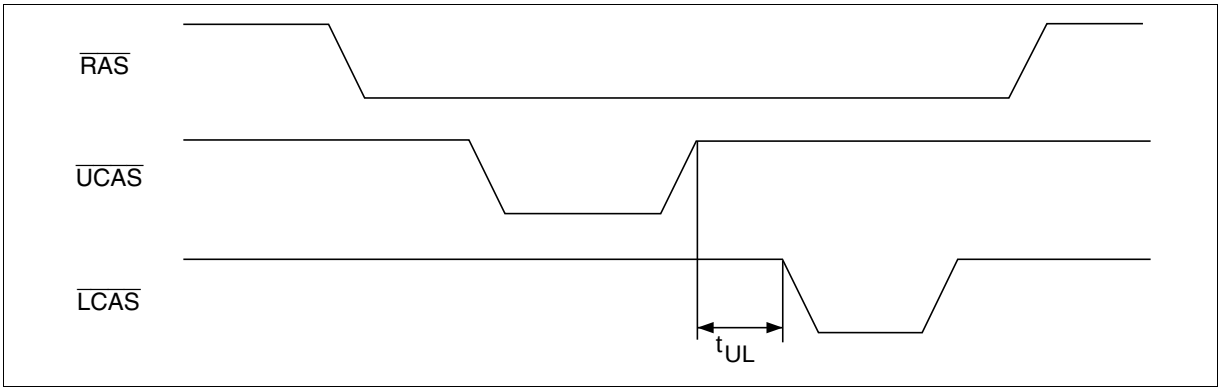
## Notes concerning 2$\overline{CAS}$ control

Please do not separate the $\overline{UCAS}$/$\overline{LCAS}$ operation timing intentionally. However skew between $\overline{UCAS}$/$\overline{LCAS}$ are allowed under the following conditions.

1. Each of the $\overline{UCAS}$/$\overline{LCAS}$ should satisfy the timing specifications individually.
2. Different operation mode for upper/lower byte is not allowed; such as following.



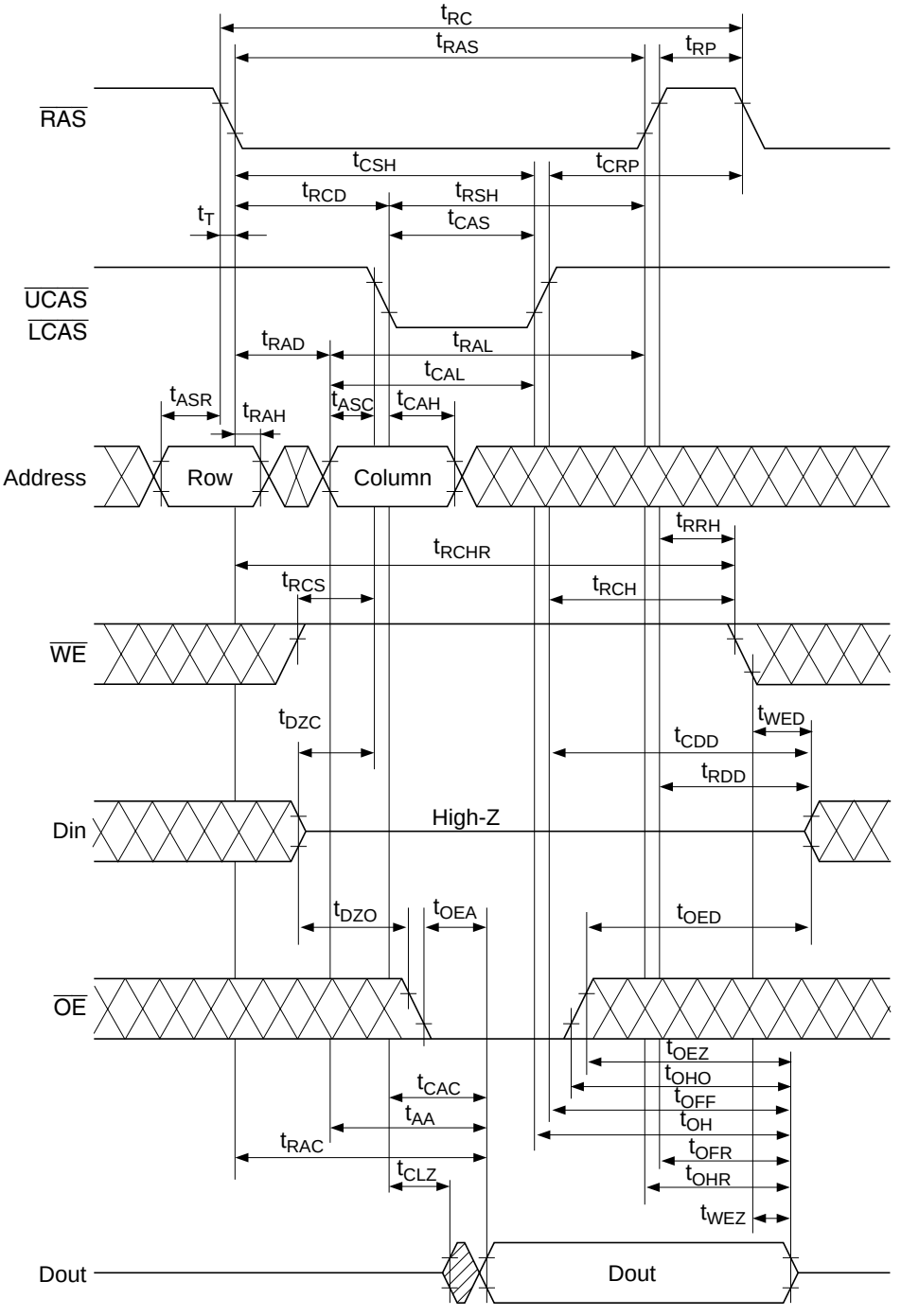

3. Closely separated upper/lower byte control is not allowed. However when the condition ($t_{CP} \leq t_{UL}$) is satisfied, EDO page mode can be performed.



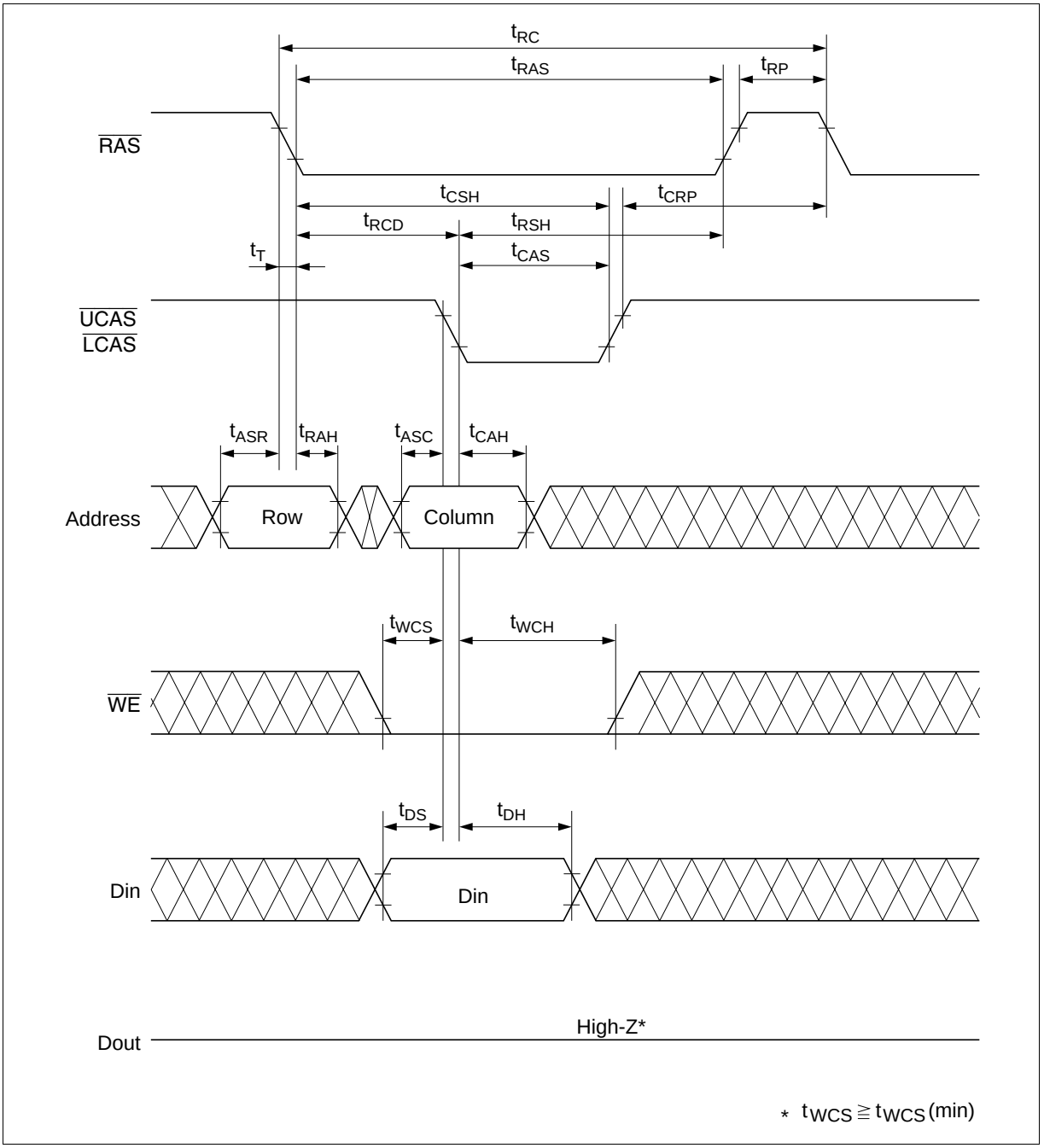

4. Byte control operation by remaining $\overline{UCAS}$ or $\overline{LCAS}$ high is guaranteed.

## Timing Waveforms*[31]

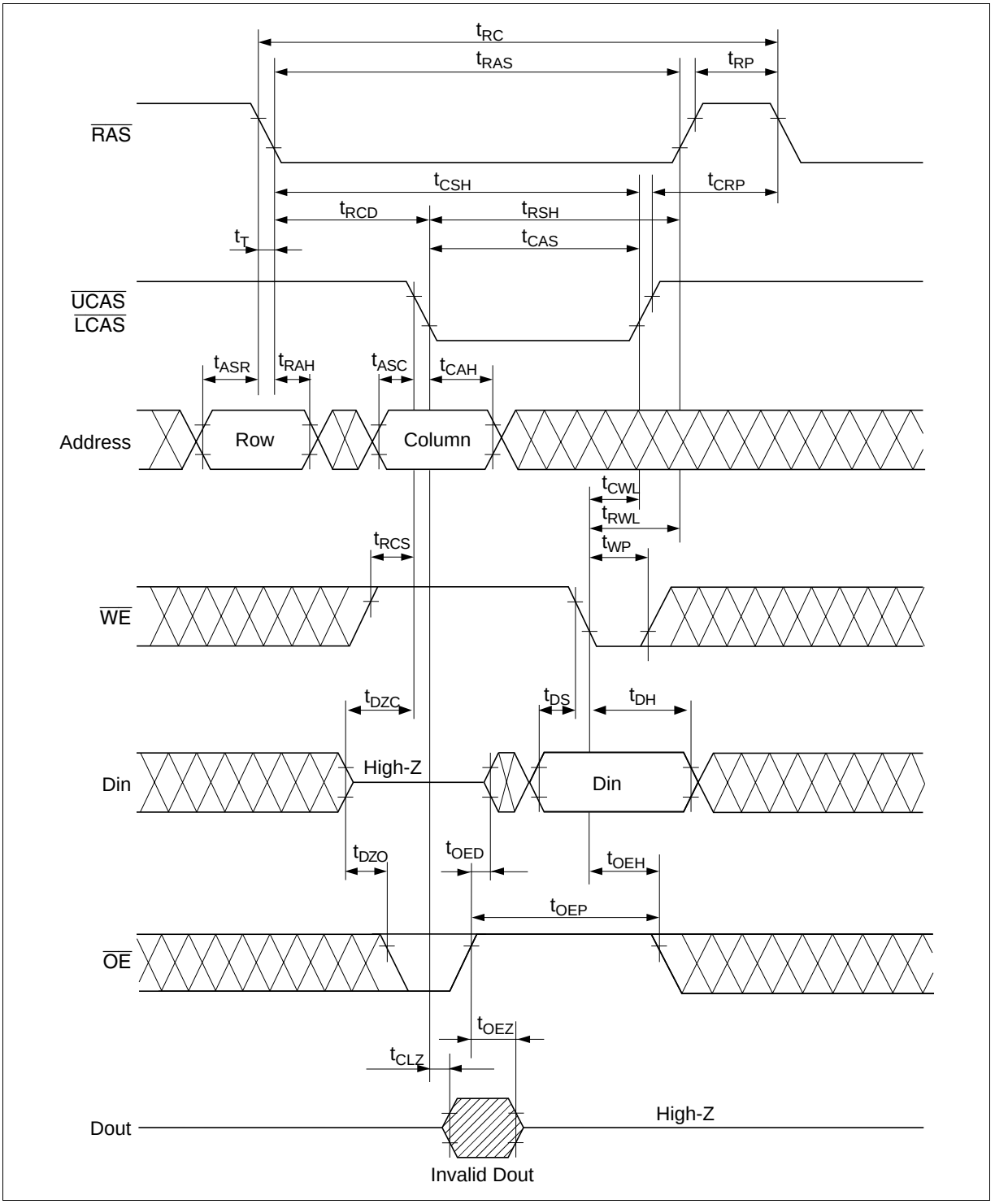
### Read Cycle



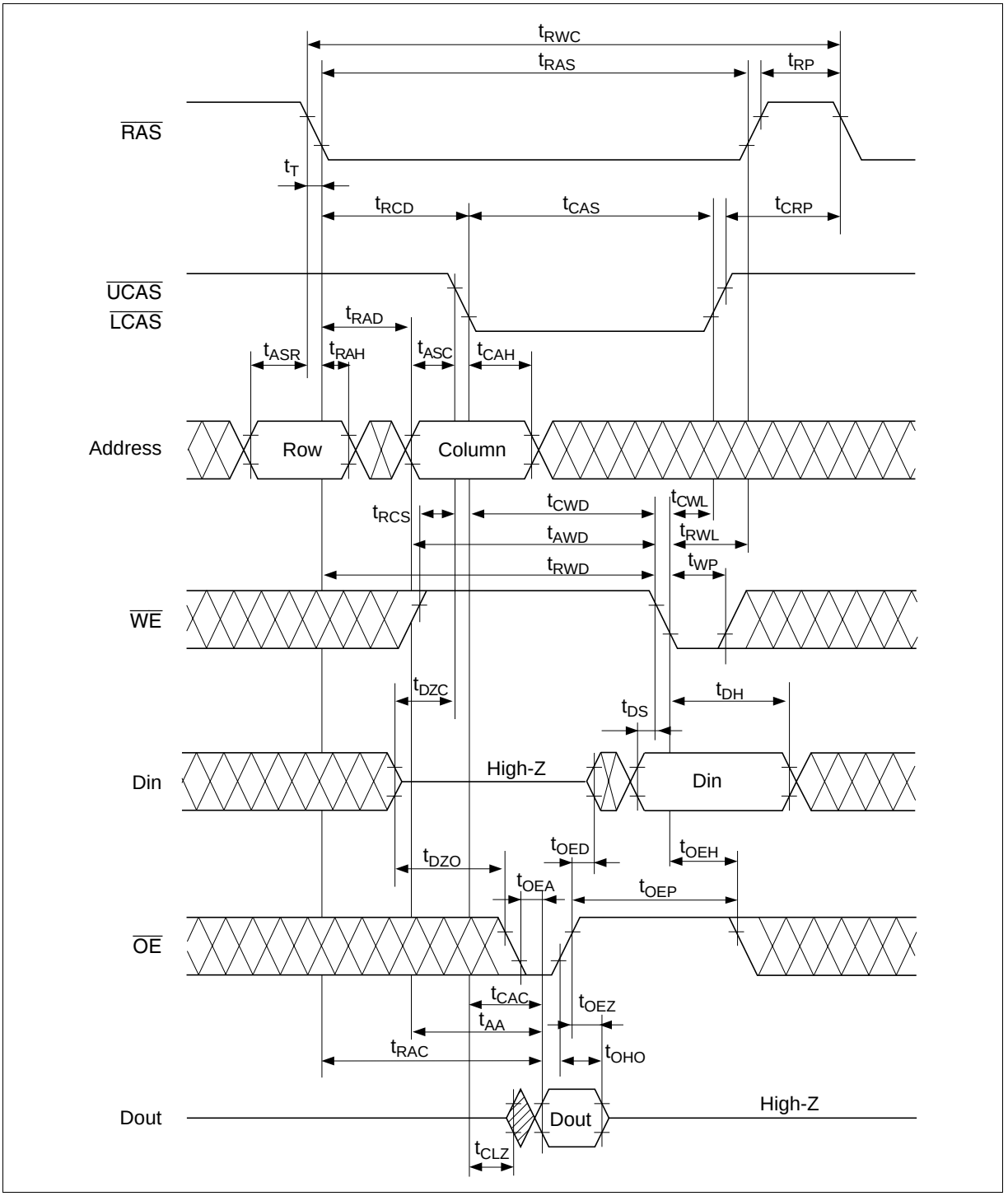
**Early Write Cycle**



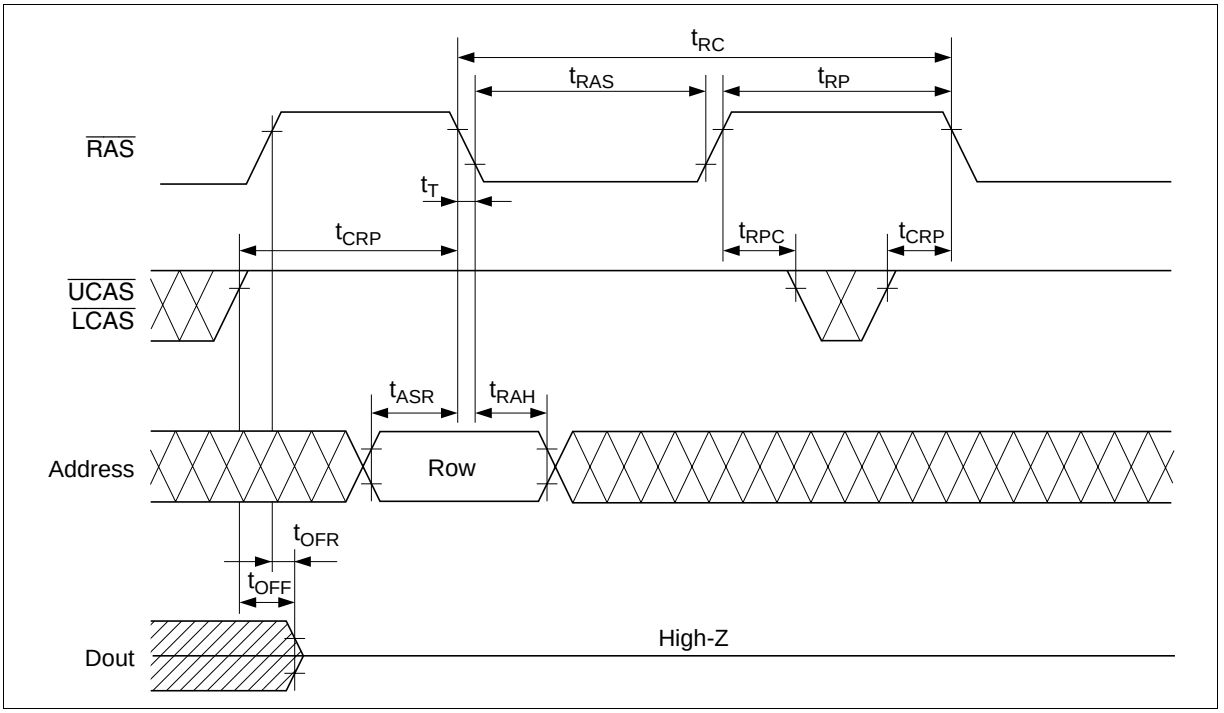
**Delayed Write Cycle***[18]



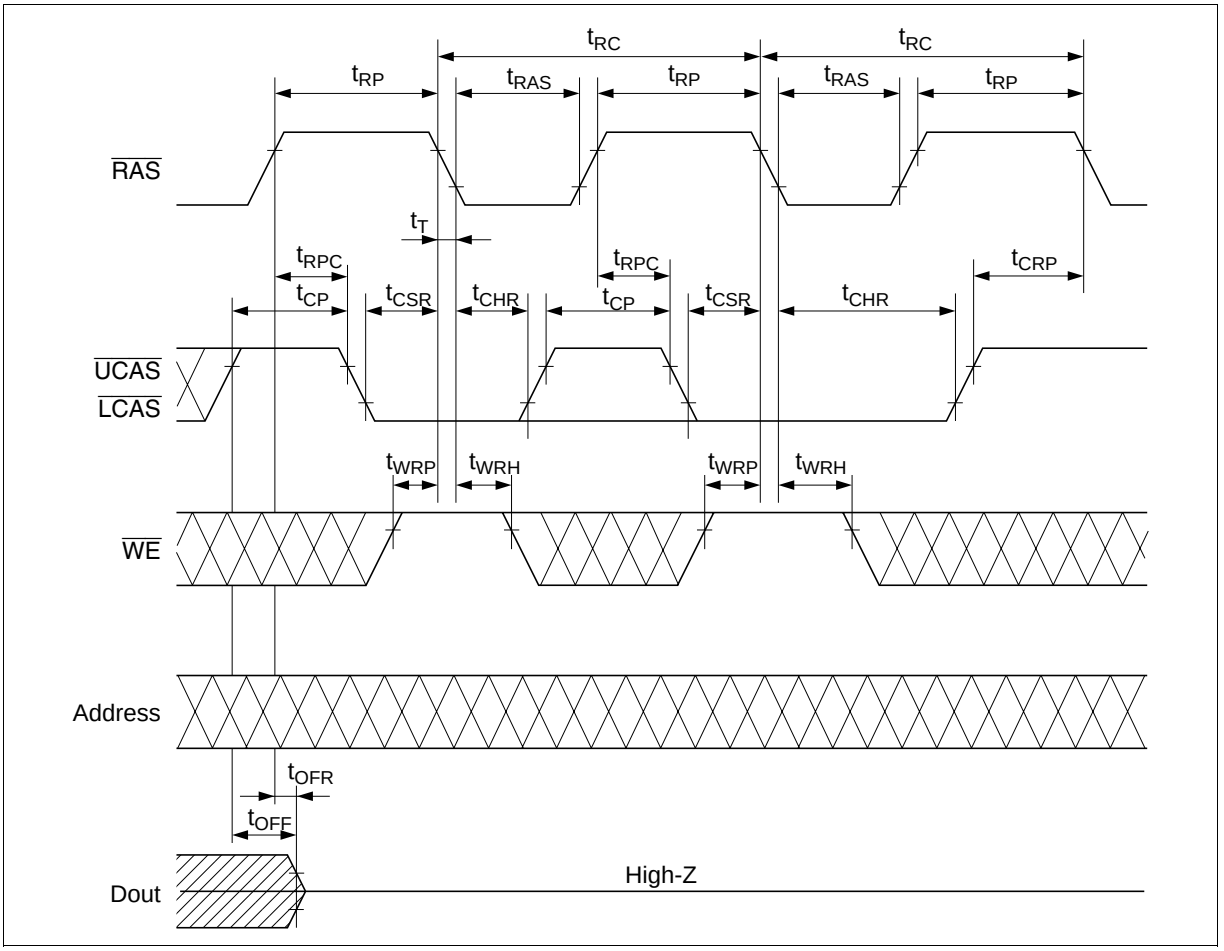
**Read-Modify-Write Cycle***[18]



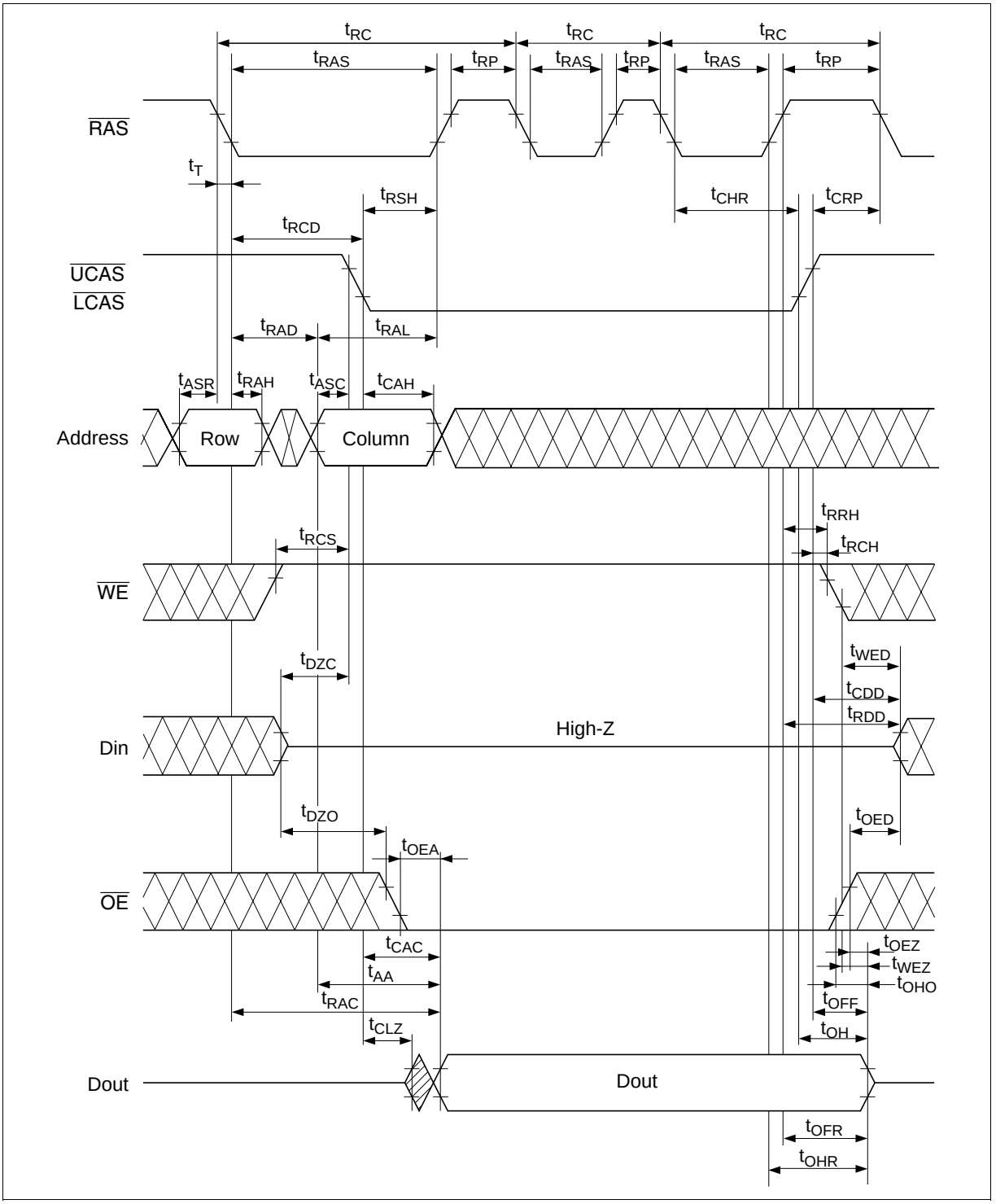
**$\overline{\text{RAS}}$-Only Refresh Cycle**



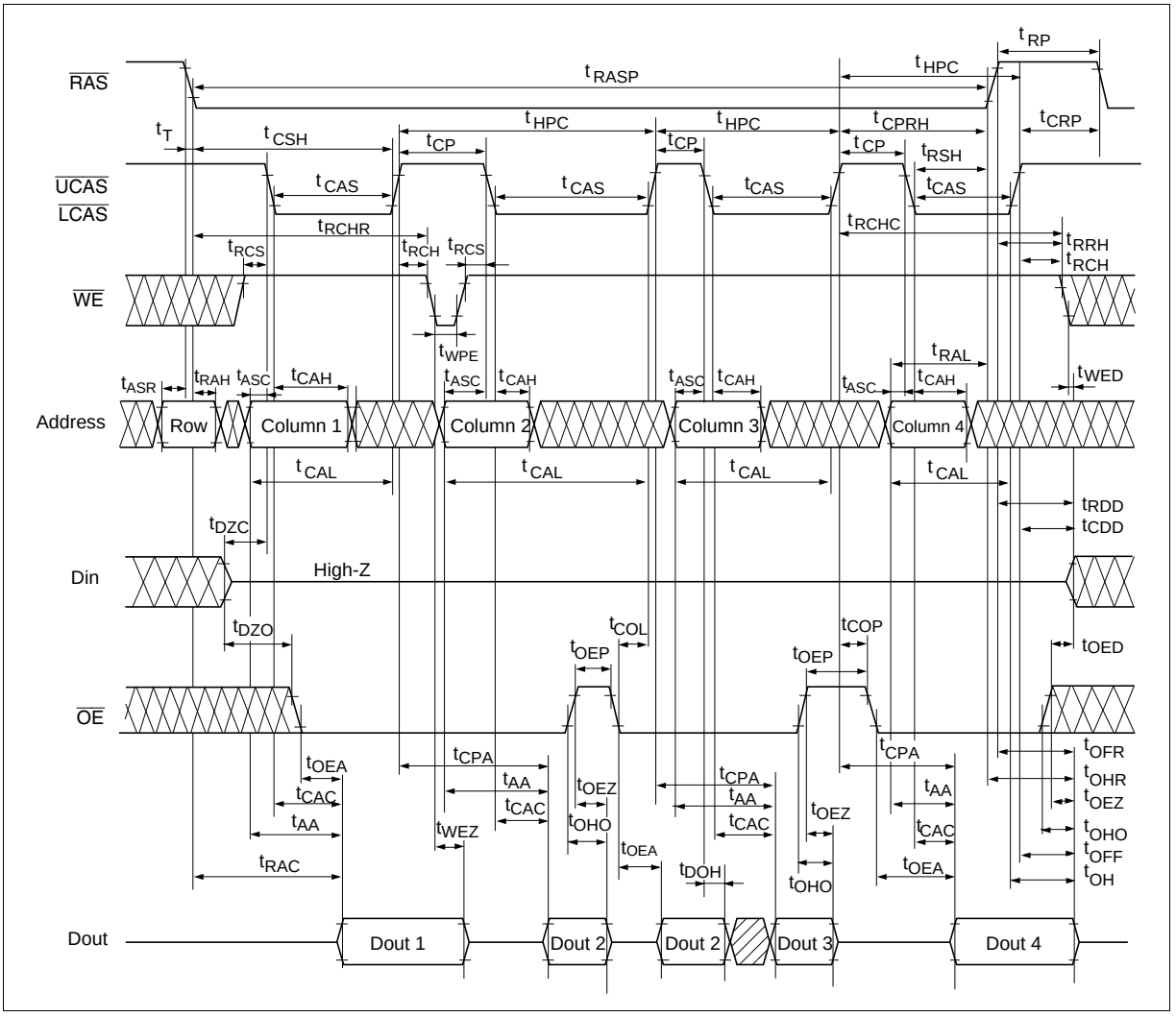
**$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle**



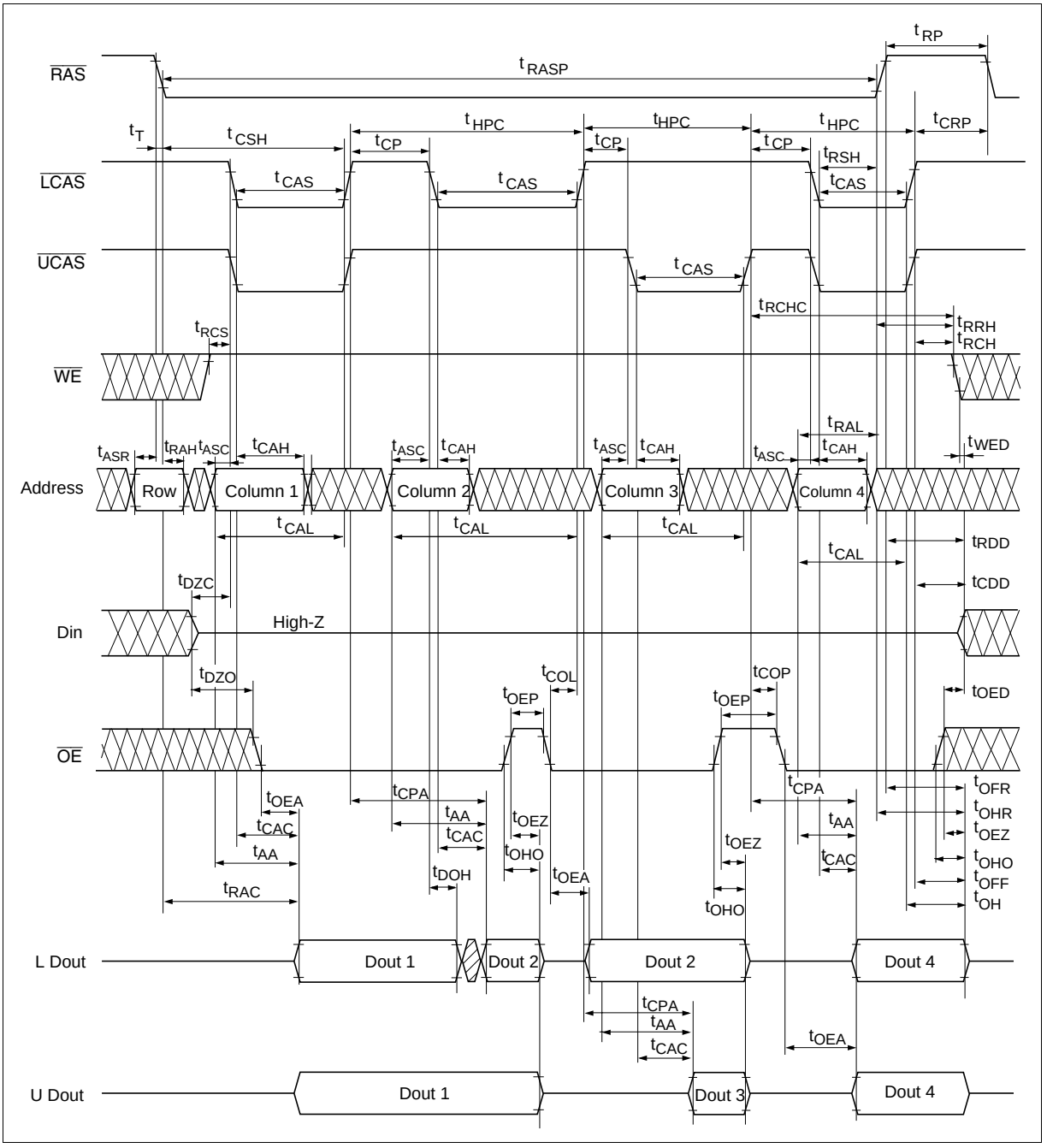
**Hidden Refresh Cycle**



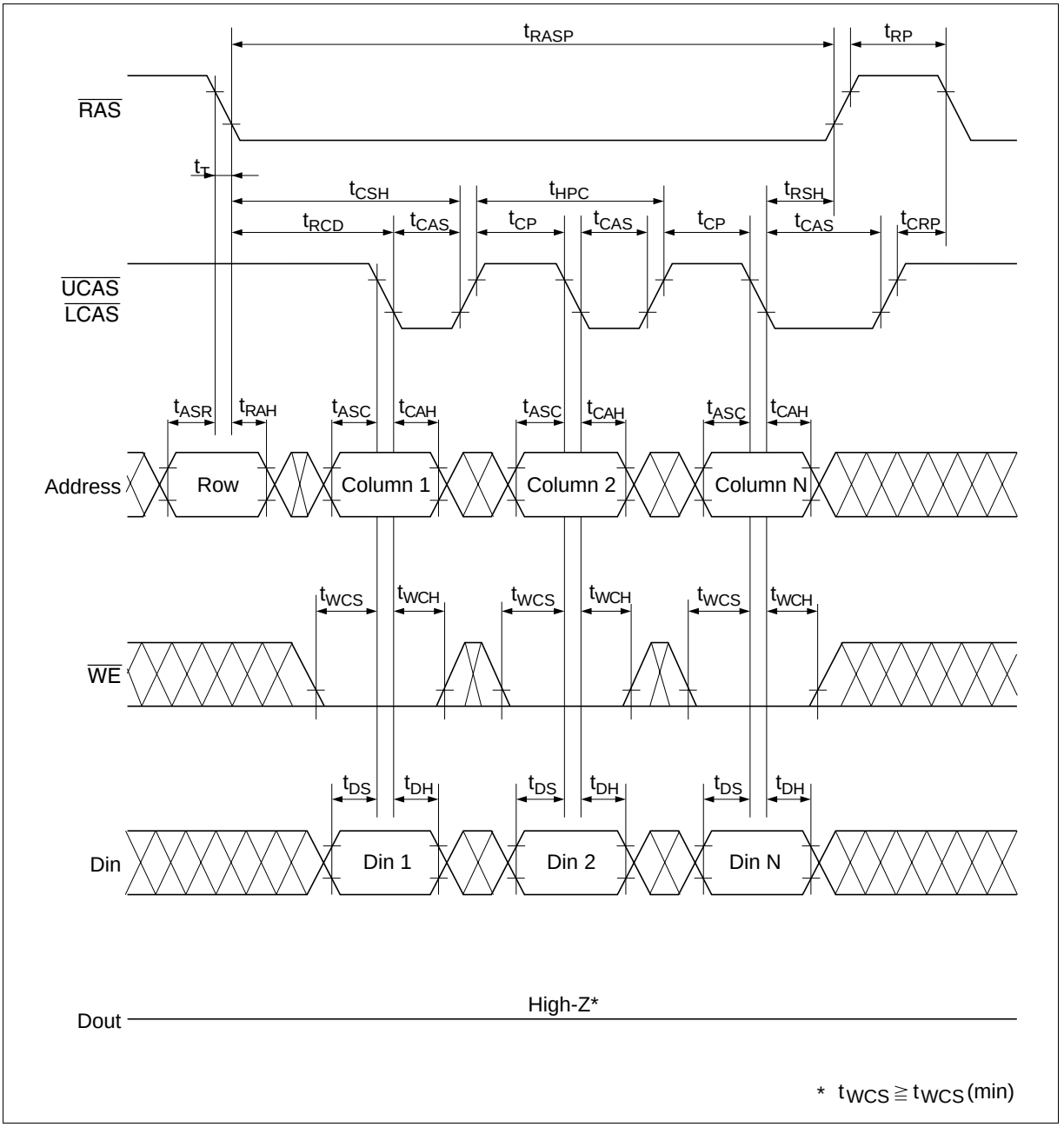
**EDO Page Mode Read Cycle**



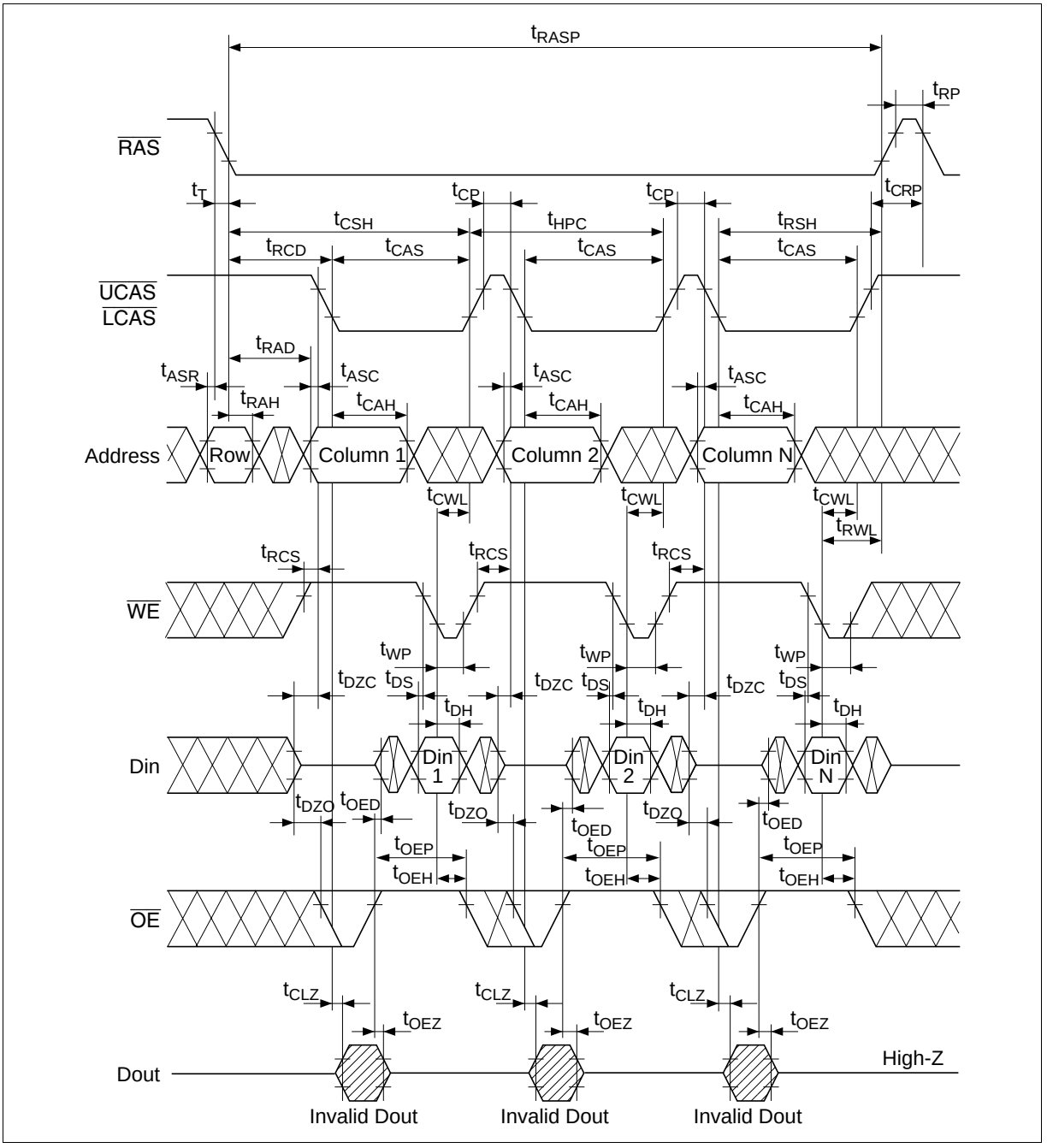
**EDO Page Mode Read Cycle** (2$\overline{\text{CAS}}$ control)



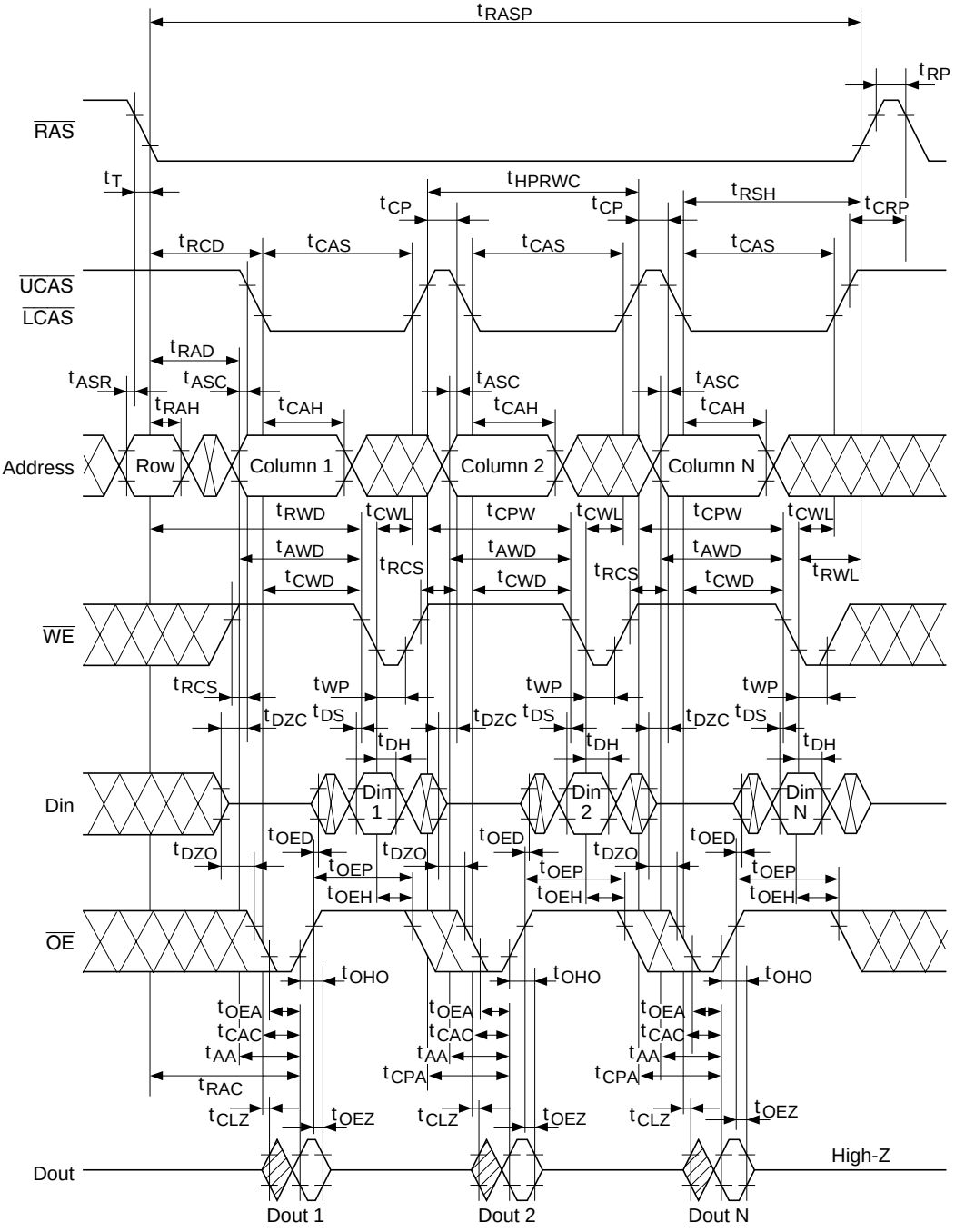
**EDO Page Mode Early Write Cycle**



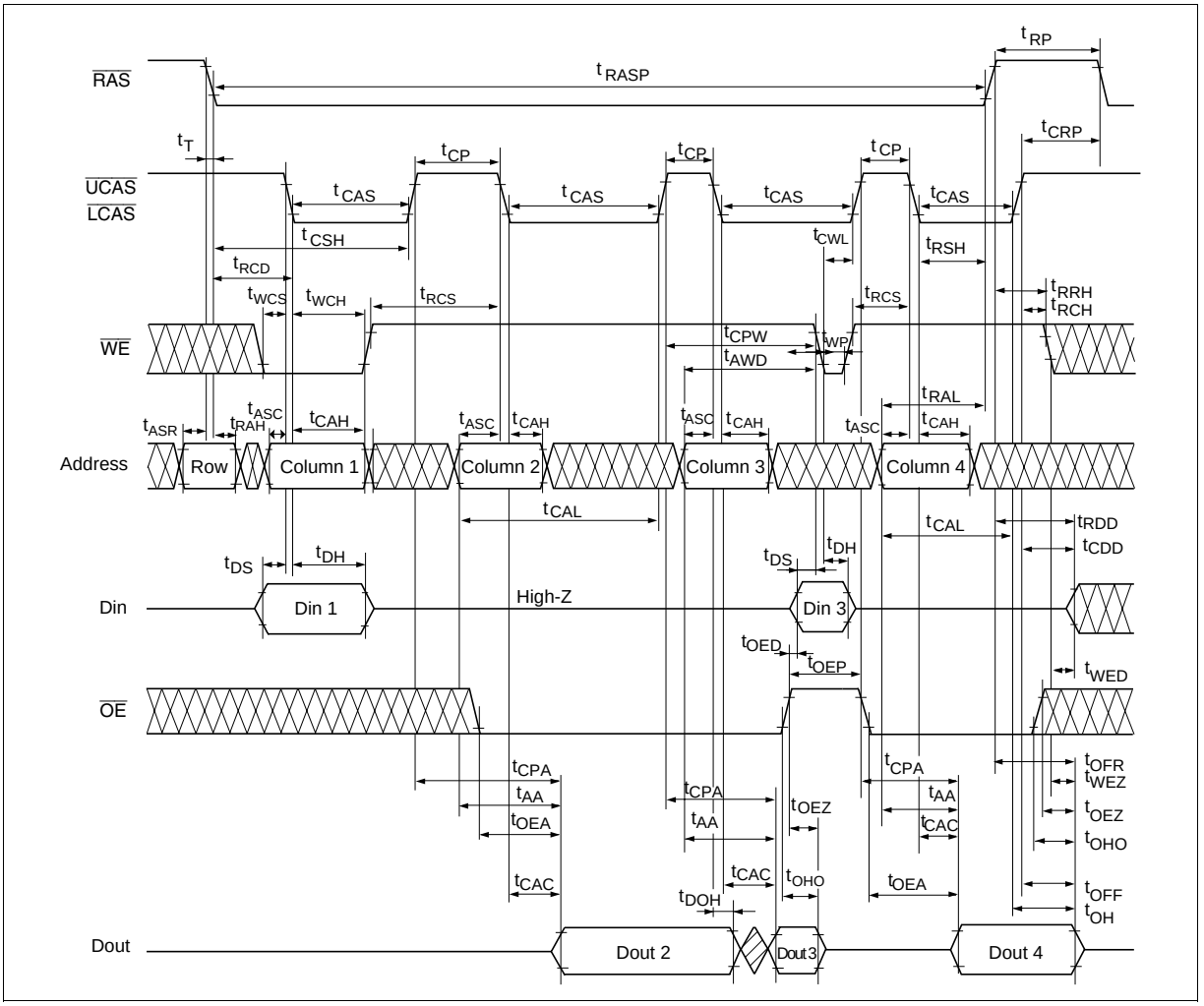
**EDO Page Mode Delayed Write Cycle***[18]



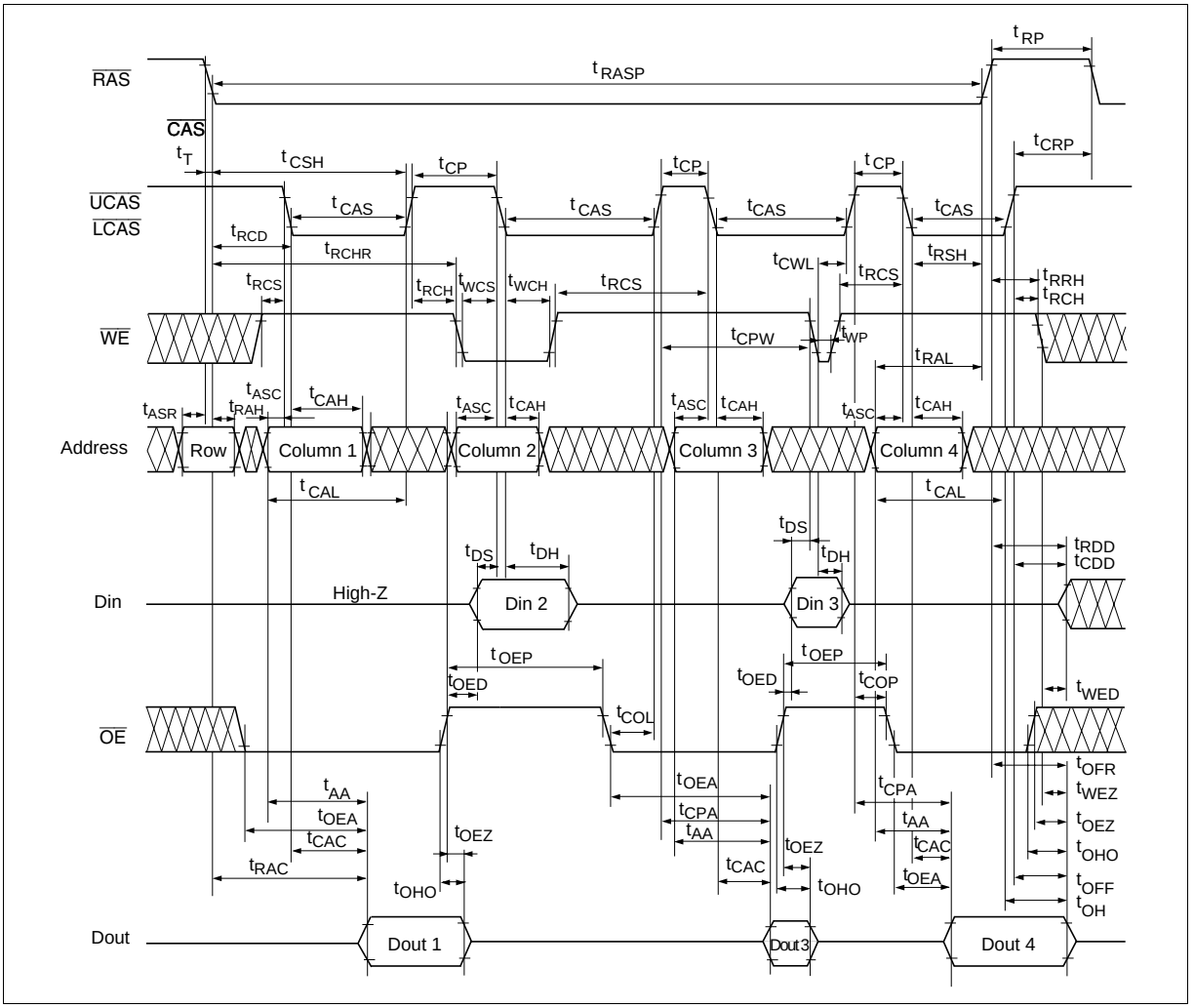
**EDO Page Mode Read-Modify-Write Cycle***[18]



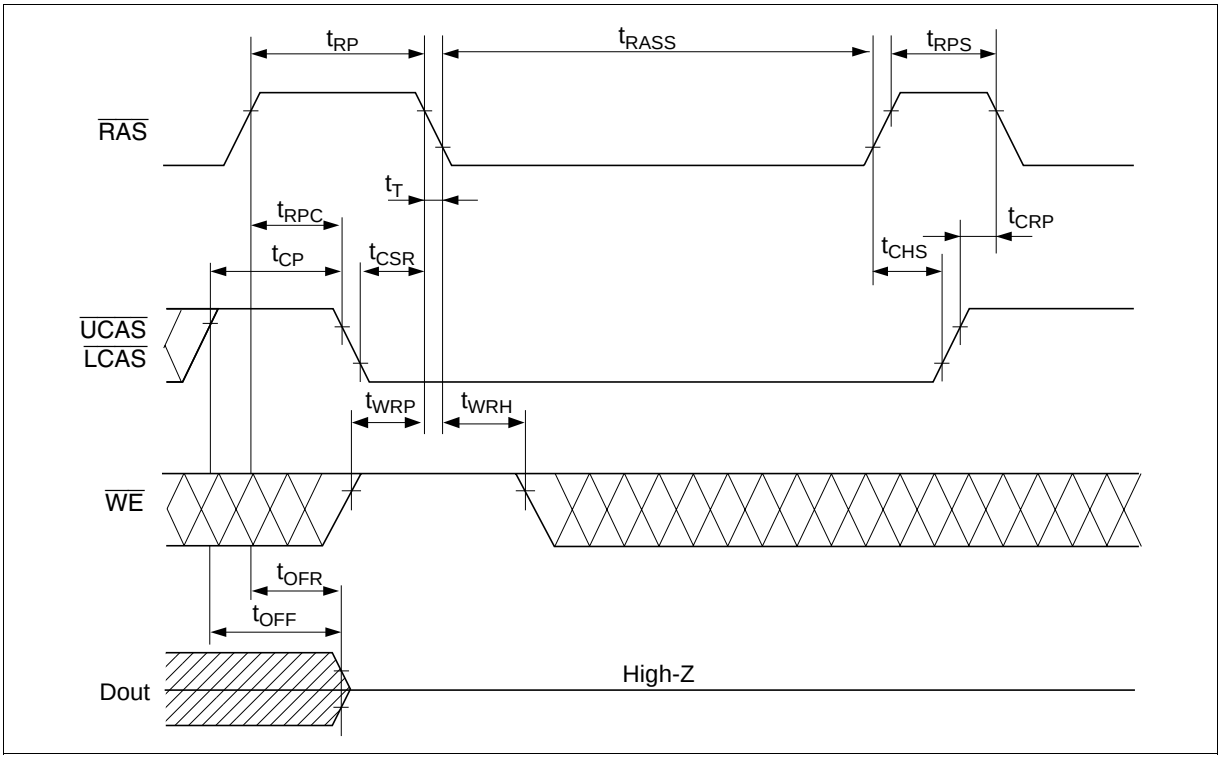
**EDO Page Mode Mix Cycle (1) *[20]**



**EDO Page Mode Mix Cycle (2)***[20]



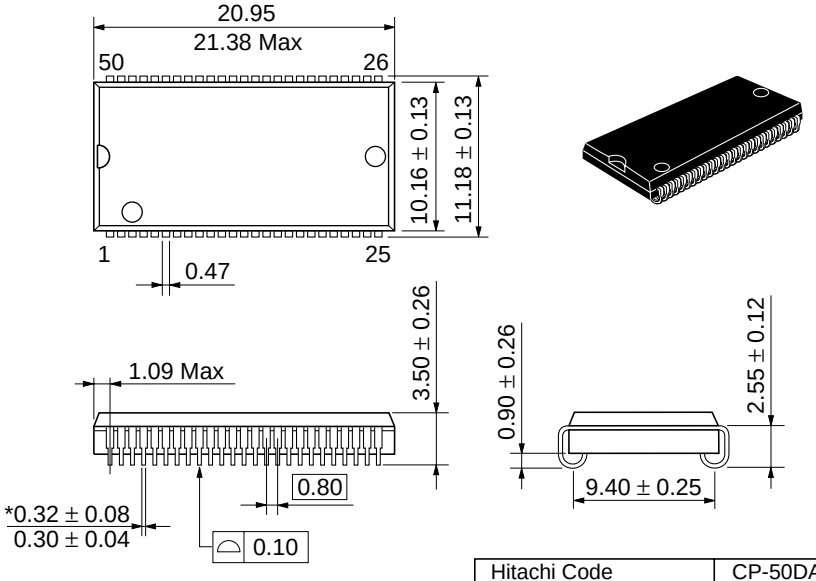
**Self Refresh Cycle** (L-version)*[23, 24, 25]



## Package Dimensions

**HM5164165FJ/FLJ Series**
**HM5165165FJ/FLJ Series** (CP-50DA)

Unit: mm



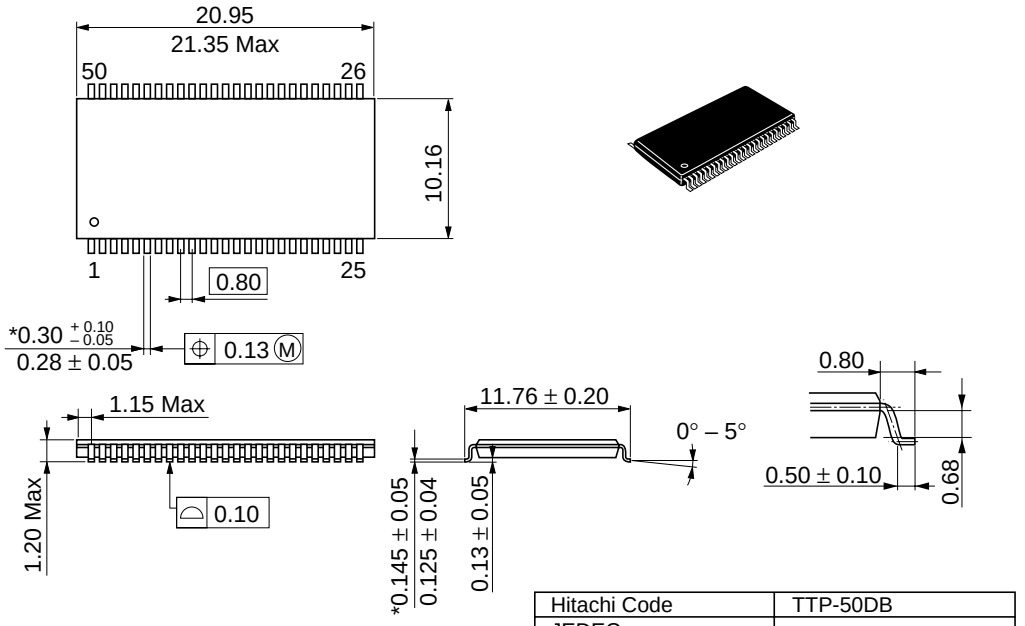

| | |
|---|---|
| Hitachi Code | CP-50DA |
| JEDEC | Conforms |
| EIAJ | — |
| Weight (reference value) | 1.2 g |

*Dimension including the plating thickness
Base material dimension

**HM5164165FTT/FLTT Series**

**HM5165165FTT/FLTT Series** (TTP-50DB)

Unit: mm




*Dimension including the plating thickness
Base material dimension

| | |
|---|---|
| Hitachi Code | TTP-50DB |
| JEDEC | — |
| EIAJ | — |
| Weight (reference value) | 0.51 g |

## Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

**Hitachi, Ltd.**
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
NorthAmerica : http:semiconductor.hitachi.com/
Europe : http://www.hitachi-eu.com/hel/ecg
Asia (Singapore) : http://www.has.hitachi.com.sg/grp3/sicd/index.htm
Asia (Taiwan) : http://www.hitachi.com.tw/E/Product/SICD_Frame.htm
Asia (HongKong) : http://www.hitachi.com.hk/eng/bo/grp3/index.htm
Japan : http://www.hitachi.co.jp/Sicd/indx.htm

**For further information write to:**

Hitachi Semiconductor (America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

## Revision Record

| Rev. | Date | Contents of Modification | Drawn by | Approved by |
|---|---|---|---|---|
| 0.0 | May. 25, 1999 | Initial issue | M. Kawamura | M. Mishima |
| 1.0 | Oct. 5, 1999 | Features: Change of Power dissipation<br>Standby (L-version) max: TBD to 1.1 mW<br>DC Characteristics<br>$I_{CC2}$ (L-version) max: TBD/TBD to 300/300 µA<br>$I_{CC10}$ (L-version) max: TBD/TBD to 1/1 mA<br>$I_{CC11}$ (L-version) max: TBD/TBD to 500/500 µA | M. Kawamura | Y. Kasama |
| 2.0 | Nov. 30, 1999 | DC Characteristics<br>$I_{CC10}$ (L-version) max: 1/1 mA to 1.2/1.2 mA | | |