ZiLOG, Inc.

2H - Year 2002

Quality

And

Reliability

Report

Chapter Title and Subsection

TABLE OF CONTENTS

Chapter Title and Subsection

Chapter Title and Subsection

Chapter 4 - **Quality Monitor Systems**

Chapter Title and Subsection

Chapter Title and Subsection

CHAPTER 1

ZiLOG's Quality Culture

RELIABILITY AND QUALITY ASSURANCE POLICY STATEMENT

ZiLOG's philosophy towards quality has been consistently aimed at continuous product improvement and optimization of processes associated with the design, manufacture, test and delivery of products that conform to all established requirements for total customer satisfaction.

It has been a ZiLOG tradition that the customer is the main driving force in a company-wide goal to achieve the highest quality possible. Through excellent management of its personnel, equipment, materials, and environmental resources, ZiLOG is well positioned for success.

ZiLOG QUALITY POLICY MISSION STATEMENT

"ZiLOG designs, builds, tests, and delivers quality through constant product and process improvements for total customer satisfaction."

- ZiLOG designs quality solutions by matching our designs to established process parameters. Hence, product design will always be guardbanded relative to process capabilities.
- ZiLOG builds quality so that the different contributing factors work harmoniously to achieve and maintain the required level of product quality and reliability.
- ZiLOG rigorously tests our products and processes so customers receive the highest quality and reliability.
- ZiLOG delivers quality so customers receive solutions that meet their expectations and contract requirements.

At ZiLOG, we subscribe to the philosophy that quality is everyone's responsibility.

The employees of ZiLOG believe that there can be no compromise in the Reliability and Quality of its products. The information provided in this report reflects their determination to provide the finest possible products.

ZiLOG is proud of its Reliability and Quality programs and is pleased to share this data with its customers. For further information, contact ZiLOG's Director of Reliability and Quality Assurance.

Mike Burgdorf
Director
Reliability and Quality Assurance

ZiLOG'S QUALITY AND RELIABILITY PROGRAM

ZiLOG, Inc. has an excellent reputation for the quality and reliability of its products.

ZiLOG's Quality and Reliability Program is based on careful study of the principles laid down by such pioneers as W. E. Deming and J. M. Juran. Even more importantly, we have benefited from the observation and practical implementation of those principles as practiced in Japanese, European and American manufacturing facilities.

The ZiLOG program begins with employee involvement. Whether the judgment of our performance is based on perfection with incoming inspection, trouble free service in the field, or timely and accurate customer service, we recognize that our employees ultimately control these factors. Hence, our quality program is broadly shared throughout the organization.

Harmony Between Design and Process

High product quality and reliability in VLSI products is possible only if there is structural harmony between product design and manufacturing. Great care is taken to ensure that the statistical process control limits observed within the manufacturing plants properly guardband the design technology used to configure the circuit and layout in ZiLOG's automated design methodology.

Through use of a technique which we call Process Templating, the technology file in the automated design system is periodically updated to ensure that product design parameters fall within the statistical control limits with which the process is actually operated. In simple terms, the Process Template is the profile displayed by the process evaluation parameters which are automatically recorded from the test patterns on wafers as they proceed through the production line. These parameters are translated into the design technology file attributes so every product design bears a lock and key relationship to the process.

Training

The integrity of our product design and manufacturing process depends on the skills of our employees. ZiLOG training emphasizes the fundamentals involved in product design and processing for quality and reliability.

Customer Service, an important aspect of ZiLOG's quality performance as a vendor, also depends upon our people clearly understanding their jobs and our obligations to our customers. This aspect of training is also a part of the overall curriculum administered by ZiLOG.

Order Acknowledgment Policy

One definition of vendor quality performance is that the vendor “does what he promises or acknowledges.” Acceptable reliability and quality is achieved only if ZiLOG and the customer are in agreement on product and delivery specifications.

Test Guardbanding

No physical attribute is absolute. Customers’ test methods may differ from ZiLOG’s due to variations in test equipment, temperature or specification interpretation. To ensure that every ZiLOG product performs to full customer expectations, ZiLOG uses a “waterfall” methodology in its testing. The first electrical tests made on the circuit for both AC and DC parameters, at the wafer probe operation, are guardbanded to the final test specifications. The final test specifications for both AC and DC parameters, in turn, are guardbanded to the quality control outgoing sample. The quality control outgoing sample is guardbanded to data sheet specifications. This technique of “waterfall” guardbanding eliminates circuits which may be marginal to the customer’s expectations long before they get to the shipping container.

Probe at Temperature

Semiconductor devices tend to exhibit their most limited performance at the highest operating temperature. Therefore, it is ZiLOG’s policy that all chips are tested at high temperature the very first time they are electrically screened at the wafer probe station. The circuits are tested again at their upper operating temperature limit in the 100% final test operation.

Process Characterization

Before release to production, every process is thoroughly characterized by an exhaustive series of pilot production runs and tests which identify the statistical, electrical, and mechanical limits of that particular process. This documentation is maintained as the historical record or “footprint” for that particular regime.

Process recharacterization is done any time there is a major process or manufacturing site change, and the resulting documentation is then added to the characterization history. Once the process is fully characterized, test site evaluation and process template data is gathered frequently to make sure that the process remains in specification.

Product Characterization

Every ZiLOG product design is evaluated over extremes of operating temperature, supply voltage, and clock frequency prior to production release. This information permits the proper guardbanding of the test program waterfall and identification of any marginal “corners” in design tolerances.

A product characterization summary, which details the more important tolerances identified in the process of this exhaustive product design evaluation, is available to ZiLOG’s customers.

Process Qualification

ZiLOG also qualifies every process prior to production by an exhaustive stress sequence performed on test chips and on representative products. Once a process regime is qualified, a process re-qualification is performed any time there is a major process change, or whenever the process template statistical quality limits are significantly exceeded or adjusted.

Product Qualification

In addition to characterization, every new ZiLOG product design is fully qualified by a comprehensive series of life, electrical, and environmental tests before release to production. Whenever possible, both industry standard environmental and life tests are employed. Again, a qualification summary is available to our customers which details certain key life and environmental data taken in the course of these evaluations. Please see Chapter Four (Qualification Requirements) for an example of the ZiLOG Package Qualification Summary and Device Qualification Summary.

PPM Measurement, Direct and Indirect

It is frequently said that if you want to improve something, you need to put a measure on it. Therefore, ZiLOG measures its outgoing quality “parts per million” by the maintenance of careful records on the statistical sampling of production lots prepared for shipment. This information is then translated by our statisticians to a statement of our parts per million outgoing quality performance.

Of course, it is one thing for ZiLOG to think it is doing a good job in outgoing product quality and it is another for a customer to agree. Therefore, we ask certain key customers to provide us with their incoming inspection data that helps us calibrate our outgoing performance in terms of the actual results in the field. The fact that ZiLOG has been awarded “ship to stock” status by many customers testifies to our success in this area.

FIT Measurement Direct and Indirect

Just as ZiLOG records its outgoing quality in terms of parts per million, it also measures its outgoing product reliability in terms of "FITS" or Failures per billion device hours. This calculation is done by using the results of weekly operating life test measurements on the circuits performed in accordance with standard specifications.

Field Quality Engineers

ZiLOG maintains a force of skilled Field Application Engineers, who are also trained as Field Quality Engineers. These engineers are available on immediate call to consult our customers on any problems they may be experiencing with ZiLOG product performance.

Product Analysis

Product Analysis facilities, staffed by experienced professionals, exist at each ZiLOG site to provide rapid evaluation of in-process and in-field rejects. ZiLOG is pleased to share product analysis reports on specific products with the customer upon request.

Oxide Charge to Breakdown (Qbd)

Gate oxide quality for ZiLOG's major fabrication processes is monitored weekly through extraction of wafer level Qbd data from the parametric test database. ZiLOG's Qbd test is based on the J-ramp test specified in JEDEC Standard JESD35- "Procedure for the Wafer-Level Testing of Thin Dielectrics."

Statistical Process Control

ZiLOG employs Statistical Process Control at all critical process steps. Deviations from norms must be evaluated by a Q/R review board.

Total Quality Program

ZiLOG employees actively participate in meetings where methods are proposed, reviewed, and adopted. These meetings enable a department to do its job in a more precise and accurate manner.

ZiLOG Vendor of the Year Award

ZiLOG is proud of the many quality and performance awards it has received from its customers. In turn, ZiLOG makes an annual award to the vendor who has done the best overall job for ZiLOG.

Environmental Protection Recycling

ZiLOG is committed to an environmental protection-recycling project that is becoming an international requirement. ZiLOG prefers that materials used to package its finished products be recyclable and/or manufactured from recycled material. The “Recyclable” symbol can already be found on shipping boxes, tubes and reels, and on shipping trays for QFP/VQFP products.

ZiLOG ENVIRONMENTAL, HEALTH AND SAFETY POLICY

ZiLOG's mission is to create superior value for our stakeholders. The health and safety of our employees, and the proper care of our environment, are of paramount importance. ZiLOG's concern for them is not only good corporate citizenship, it's also good business.

ZiLOG is committed to a continuously improving Environmental, Health and Safety Management System. Strict compliance with applicable EHS regulations is considered a minimum standard – neither production goals nor financial objectives shall excuse noncompliance.

The core values of ZiLOG's EHS Management System are to:

- Create, maintain and promote a safe and healthful workplace for all employees.
- Comply with the intent as well as the letter of all relevant EHS regulations at the Federal, State and Local levels.
- Set EHS goals and objectives and measure progress toward them.
- Promote a respect for the environment among employees.
- Conserve resources and minimize waste by reducing, reusing, and recycling.
- Integrate EHS considerations into business planning, decision making, and daily activities.
- Provide the resources and training to carry out this policy.
- Prevent accidents and minimize environmental impacts.
- Communicate our EHS performance.
- Respond to the concerns of the communities in which we do business.
- Support EHS public policy development.
- Encourage our contractors and suppliers to adopt EHS standards similar to our own.
- Exchange EHS knowledge and technology.

These core values build on our tradition of quality, innovation, and continuous improvement. Each employee is personally responsible for making these value a part of everyday worklife at ZiLOG.

Jim Thorburn
Chief Executive Officer
ZiLOG, Inc.

ISO CERTIFICATION

ZiLOG is extremely proud to have received the following ISO 9000 certification awards, which reflect the stringent quality standards to which all ZiLOG products are manufactured.

FACILITY/LOCATION	*CERTIFICATION RECEIVED*
ZiLOG Electronics Philippines, Inc. (ZEPI) Manila, The Philippines - Final Test and Shipment of Semiconductors	ISO 9002 – Re-certified 7/98 By SGS Yarsley International Certification Services Camberley, Surrey, UK ISO 14001 – Certified 11/99 by SGS International Certification Services Zurich, Switzerland
ZiLOG Nampa Nampa, Idaho - Wafer Fabrication	ISO 9001 Re-certified 9/98 by the National Standards Authority of Ireland. ISO 14001 – Certified 3/99 by the National Standards Authority of Ireland.

(*ISO - International Standards Organization)

ISO 9000 CERTIFICATION FOUNDRIES/SUBCONTRACTORS

FACILITY	*LOCATION*	*PROGRAM*
Wafer Foundries:		
UMC	Taiwan	ISO 9002
TSMC	Taiwan	ISO 9002
Assembly Subcontractors:	**Taiwan**	
AIT	Batam, Indoneasia	ISO 9002
Amkor	Manila, PI	ISO 9002
ASE	Manila, PI and Taiwan	ISO 9002
Carsem	Ipoh, Malaysia	ISO 9002

QUALITY AND RELIABILITY TREND CHARTS

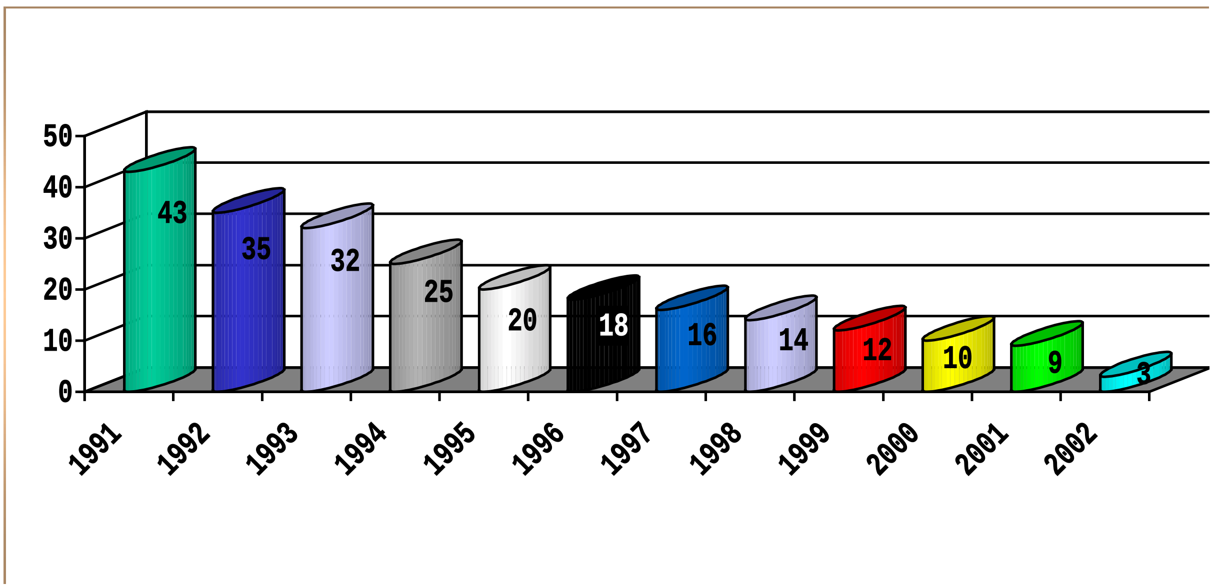


Figure 2-1.– FIT Rate (FIT = Failure in Time: Failures per Billion Hours)

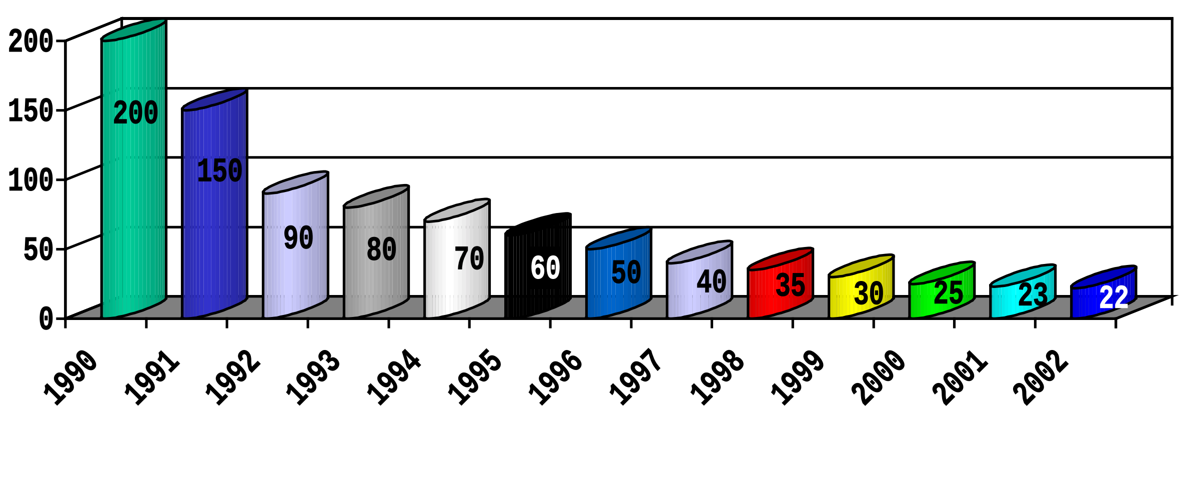
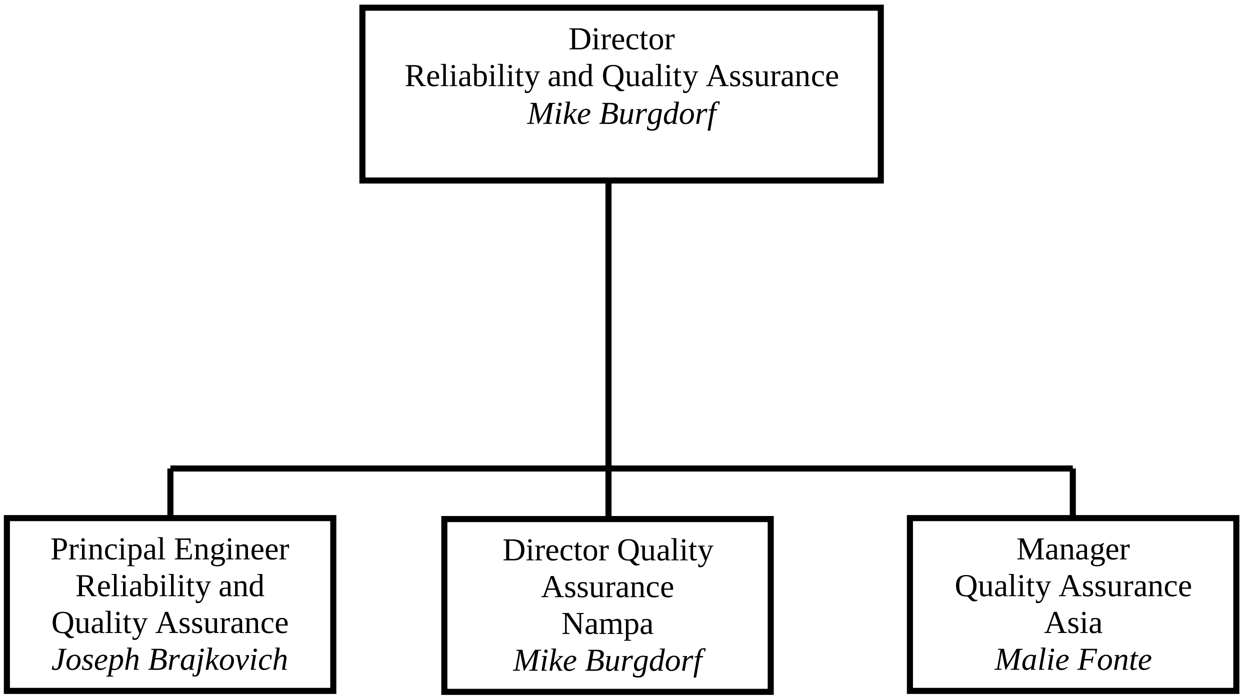


Figure 2-2. PPM Electrical

Figure 2-3. R/QA Organizational Chart



CHAPTER 2

Customer Quality Support

CUSTOMER FAILURE ANALYSIS/CORRELATION PROCEDURE

ZiLOG has a complete Customer Failure Analysis (CFA) system. Using this system, a customer may return units for failure analysis or test correlation. The sequence of events for the CFA procedure is as follows:

1. Customer suspects a failure.
2. The Customer and ZiLOG's Field Applications Engineer (FAE) generate a CFA request. See Figure 3-1.
3. A CFA request is assigned a number for tracking.
4. ZiLOG's FAE sends the unit(s) to the factory.
5. Product/Test Engineering performs a go/no-go electrical test.
6. The unit(s) and test results are given to the Failure Analysis Engineer.
7. If the unit(s) fail the test, the Failure Analysis Engineer performs electrical and physical analysis, and generates a CFA report. See Figure 3-2.
8. If the unit(s) pass the test, the Failure Analysis Engineer generates a CFA report and returns the unit(s) to the customer.
9. Our goal is to provide a complete CFA report within 10 working days from the time the unit(s) are received.

ZiLOG and the customer will work together to reduce all types of failures to zero. The CFA procedure is one of several communication tools that can be used to achieve this goal, proving its overall effectiveness since its inception in 1985.

Figure 3-1. ZiLOG Guideline Information Needed By The Factory With CFA's

Purpose: To eliminate time spent researching a failed component/part history in order to concentrate on finding the root cause of failure or complaint by the customer

OP184

FAILURE ANALYSIS QUESTIONNAIRE

GENERAL INFORMATION:

Initiated By: ____________ Date: ____________ B.U.: ____________

Customer Name: ____________

Customer Address: ____________

Phone No: ____________ Customer priority level: ____________

PART INDENTITY:

Device: ____________ Date/bb Code: ____________ Total # devices in lot: ____________

Qty. devices tested/inspected: ______ Qty. being returned: ______ Qty. of failed devices: ______

Customer Application: ____________

FAILURE DESCRIPTION:

Incoming: ______ Assembly: ______ Final Test: ______ Field Return: ______

Low Noise Option? ☐ Yes ☐ No How long in service before failure occurred? ____________

Was part removed with any other parts? ☐ Yes ☐ No ____________

Did failure follow part? ☐ Yes ☐ No ____________

Additional processing temperatures which part had seen before failure occurred: ____________

Is this a new application for this device? ☐ Yes ☐ No ____________

Is this a new failure mode? ☐ Yes ☐ No ____________

Is there a Customer board or test program available for use at ZiLOG? ☐ Yes ☐ No

Are there failing and passing samples available for correlation work? ☐ Yes ☐ No

Process steps part had seen up to time of failure: ____________

ADDITIONAL DETAILS:

____

____

____

____

____

____

Figure 3-2. ZiLOG Failure Analysis Report

PSI:	CUSTOMER FAILURE ANALYSIS		Page 1 of 1
Quantity:	***REPORT***		Date:
Customer:	*ZiLOG Confidential*		CFA#:
Analyst:	Date:	Approved:	Date:
Problem as reported by customer:			
Device Date Code(s):			
Analysis: External Visual: Bench Test: Electrical Test, Final Test at 100C, QA test at 25C, Sentry Tester:			
Conclusion:			
Recommended Action:			

Table 3-1. Summary of QC Test Equipment

Equipment At ZEPI	***Brand***	***Usage***
Wetting Balance Tester	Multicore Must II	Solderability Test
ISOMET Low Speed Saw	Buehler	Cross-Section Analysis
Curve Tracer	Tektronix 577	Bench Check
ESD Tester	IMCS 700	VZAP Testing
ESD Tester	Oryx 11000	VZAP Testing
HAST	Express Test	Reliability Test
Polimet Polisher	Buehler	Cross-Section Analysis
High Power Scope	Olympus	External/Internal Visual Inspection
Low Power Scope	Bausch & Lomb	External/Internal Visual Inspection
Jet Etch	Novus Technologies	Decapping of Plastic Devices
Hot Plates	3D Ready-Heat	Solderability-Steam Aging
Pressure Cooker	Electric Steroclave	Reliability Test
Plasmod Plasma Etcher	March Inst Inc	Topside Etch
SEM & EDX	Leica S420	Visual & Elemental Analysis
Digital Multimeter	Fluke	Latchup Test
Power Supply	HP	Latchup Test
Timer	Gralab	Timed Operations
Acoustic Microscope	Sonoscan C-SAM 3100	Delamination Inspection
Profile Projector	Mitutoyo	Dimensional Inspection
Temperature/Humidity Test Chamber	ESPEC	Temperature/Humidity Test
Temperature/Humidity Test Chamber	Sexton ESPEC	Moisture Resistance Test
Salt Atmospheric Chamber	Associated	Salt Atmosphere Test
Mechanical Shock Tester	Lansmont	Mechanical Shock Test

Table 3-1. Summary of QC Test Equipment

Equipment At ZEPI	***Brand***	***Usage***
VVF Test	Unholtz-Dickie	VVF Test
Thermal Shock	Tabai	Thermal Shock Test
Temperature Cycle	Ransco	Temp Cycle Test
Toolmaker Scope	Unitron	Dimensional Check
Hardness Tester	Ames Precision	Leadframe IQC
Plating Thickness Measuring Equipment	Fischerscope	For Plating Thickness
Wirepull Tester	Unitek	In-Process Wirepull Testing
Wirepull Tester	Westbond	In-Process Wirepull Testing
Beam Balance	None	Weight Measurement
Shear Tester	B&G	Die Shear Test
Particle Counter	Atcor	Airborne Particle Measurement
Flow Thru Cooler	Neslab	Viscosity Check
Digital Linear Gauge	---	Wafer Thickness Check
Incubator	Millipore	Bacteria Monitor
Ball Shear Tester	KTC	Wirebond Check
High Power Scope	Olympus	Inspection
1 Set PH Meter VWR	VWR	PH Check
3 PCS Chatillion Gauge	Chatillon	Die Push Test
Coplanarity Tester	RVSI	Coplanarity Check
MP-4 Land Camera With Stage And Floodlights	Polaroid	Photo Duplicating, Macrophotography 8X10
High Power Microscope w/Video Camera	Leitz, RCA	Wafer Level Inspection

Table 3-1. Summary of QC Test Equipment

Equipment At <u>Nampa</u>	***Brand***	***Usage***
Zoom Stereoscope 5-50X	Nikon	X-Section Mounting, Low-Power Inspection
High Power Microscope w/Camera, 50-1000X Long-Working Distance Objectives	Nikon	Package Die Visual Microphotography
X-Ray System	Faxitron	Film Radiography
Gold Coater	Denton Vacuum	SEM Sample Prep (Backup)
Low-Speed Diamond Saw	Buehler	Package Cross
Bench Top Furnace	Lindberg	High Temp Analysis to 1100C
High Temperature Ovens:		
175C	Blue M	Bake Recovering
150C	Blue M	Bake Recovering
125C	Blue M	SEM Sample Storage
Exhaust Hood	Kewaunee	Chemical Use Safety
Wet Sink w/Exhaust	JST Plastics	Chemical Use Safety
3-Wheel Polisher	Buehler	Cross-Section and Lap
Hot Plate PC100	Corning	Wafer Reliability Analysis
Hot Plate PC100	Corning	Hot Chemical Etch
Hot Plate	Lindberg	Wafer Pressure Pot Test
Hot Plate	Corning	Chip Unzip
Hot Plate	Arthur H. Thomas Type 2000	Chemical Heating
Ultrasonic Cleaner (2)	Bransonic	Sample Cleaning
Ultrasonic Cleaner	Branson 3510	Sample Cleaning
Plasma Etcher	Tegal	Topside Etch and Descum
Jet Etch & Jet Rinse	B&G Enterprises	Part Decapsulation
Cerdip Opener	B&G Enterprises	Part Decapsulation
Timmers (2)	Gralab	Timed Operations
Dial-O-Gram (2)	Ohaus	Chemical Measurement
UV Light	Blak-Ray	Dye Penetrant Test
UV Light EA	Loglcal Devices, Inc.	EPROM Erasing
Curve Tracer 576	Tektronix	Bench Check
Curve Tracer 577	Tektronix	Bench Check
CRT Camera	Tektronix	Waveform Photo
Temperature Forcing Unit	Temptronic	Bench Temperature Testing
Microprobe Station	Wentworth	Microprobing (Not Complete - no mcroscope)
Laser Cutter	New Wave EZ LAZE	Trace Cutting
Microprobe Device Socket Cards:		

Table 3-1. Summary of QC Test Equipment

Equipment At Nampa	***Brand***	***Usage***
44 LCC/PLCC	ZiLOG Designed	
48 Lead DIP	Micromanipulator	Bench Microprobe Work
64 Lead Narrow Pitch DIP	ZiLOG Designed	
High Power Microscope 50x - 400x	Nikon	Die Visual Microscope
High Power Microscope 50x - 1000x	Nikon	Die Visual Chip Unzip Inspection
S440 SEM	Leica	High Power Imaging
FIB With SIMS (SIMS not working)	FEI	Micro Cross Sectioning, Device Modification and Elemental Analysis and Imaging
Reactive ION Etcher (REI), 8-Inch	Trion	Device Deprocessing
Polycon, BF, DF, DIC, Confocal, Fluorescence,	Leica-Reichert	Product Visual Examination
W/8x8” Stage	Semprex	Feature Size Measurement
W/Micron Stage Readout	Optronics	Video Camera
W/Sony Color VP Video	Sony	3x4 Inch Color Video Print
Oscilloscopes	HP, Tektronics 7704	Signal and Waveform Monitor
4145A (2)	HP	Parametric Tester
w/LCR Meter	HP	Capacitance and CV Measure
Visionary 2000	Hypervision	Emission Microscope,
W/MP2000 8” Probe	Carl Suss	Device Microprobe, CV
Package Device Thermal	Temptronics	Emission Microscope,
Socket Cards:		Microprobe and Liquid
20 Lead PLCC	Temptronics	Crystal (Room and Hot)
44 Lead PLCC	Temptronics	
68 Lead PLCC	Temptronics	
84 Lead PLCC	Temptronics	
44 Lead PQFP	Temptronics	
100 Lead QFP	Temptronics	
100 Lead VQFP	Temptronics	
124 Lead PGA	Temptronics	
64 Lead DIP	Temptronics	
28 Lead DIP (300 Mil)	Temptronics	
Blazer 125 Tester	IMS	Bitmapping, Device Test
W/8” Probe Station	Wentworth	Microprobe
4156B Precision Semiconductor Parameter Analyzer	HP	Parametric Tester
35665A Dynamic Signal Analyzer	HP	Tester
4275A Multi-Frequency LCR Meter	HP	Tester (Inductance, capacitance, resistance instrument)

Table 3-1. Summary of QC Test Equipment

Equipment At Nampa	Brand	Usage
4274A Multi-Frequency LCR Meter	HP	Tester (Inductance, capacitance, resistance instrument)
Microminipulator Test Station (2)	Micromanipulator	Probe Test
4155B Semiconductor Parameter Analyzer	Agilent	Parameter Tester
208 PQFP	Schlumberger	Socket Adapters
44 QFP	Schlumberger	Socket Adapters
48 DIP	Schlumberger	Socket Adapters
64 DIP	Schlumberger	Socket Adapters
17x17 PGA	Schlumberger	Socket Adapters
84 PLCC	Schlumberger	Socket Adapters
24 DIP	Schlumberger	Socket Adapters
48 DIP	Schlumberger	Socket Adapters
28 DIP	Schlumberger	Socket Adapters
24 DIP	Schlumberger	Socket Adapters
44 PLCC	Schlumberger	Socket Adapters
124 PGA	Schlumberger	Socket Adapters
HP Display 1340A	HP	Signal Display
Philips XL30	Philips	Ultra High Resolution
SFEG SEM		SEI, BSE (Solid State)
Multiprep	Allied High Tech	Parallel Polishing
Techprep		
50x - 4500x High Power Optical Microscope	Nikon Eclipse L200	Bright field, Dark field, Numarsky, Confocal inspection, Digital Camera1280 x 1944
High Temperature Oven 20 C - 550 C	Grieve	Hammer Testing, Ink Dot Curing
Photographic Printer	Codonics	High Quality Photographic Printer
Printer (color)	Tektronics	Photographic Printer
MP4 Camera	Polaroid	Polaroid Photographs
Chip Unzip	Hypevision	Backside Analysis

Table 3-1. Summary of QC Test Equipment

Equipment At Campbell	***Brand***	***Usage***
Spectrum Analyzer	HP-8591A	Near Field EMI Testing
Pre-Amplifier	HP8447D	Near Field EMI Testing
Plotter	HP-7550A	Near Field EMI Testing
Biconical Antenna	#CEAB-100	Near Field EMI Testing
Log Periodic Antenna	#CEAL-100	Near Field EMI Testing

USE OF OUTSIDE FMA LABS

RIGA Analytical Lab, Inc.
3375 Scott Blvd., Suite 132
Santa Clara, CA 95051

Charles Evans & Assoc.
301 Chesapeake Drive
Redwood City, CA 94063

BridgePoint Tech. Mfg.
4007 Commercial Drive
Austin, TX 78744

CUSTOMER NOTIFICATION SYSTEM

Corporate R/QA notifies the customer with a formal change notification letter on major process and design changes if the customer requests notification of such.

The following is a list of criteria for which certain customers need to be notified:

1. Process: die size, passivation, metallization, mask changes.
2. Materials and finishes: either internally or externally, including symbolization.
3. Internal Connection Methods: including lead bonding and die attach.
4. Packaging: sealing and encapsulation techniques, including lead bonding and die attach.
5. Test Parameters: which may affect correlation.
6. Anti-Static Handling: procedures or packaging.

Shown on the following pages is an example of a change notification letter that gives the customer a schedule of the conversion, stating that:

- The customer will be given 30 days to respond to ZiLOG requesting samples for qualification by the customer.
- New product will be shipped within 60 days from the date of the letter, unless ZiLOG receives written notice from the customer to continue shipping their current qualified product.

June 30, 2000

Subject: Customer Change Notification -
Z80S183 / Z80L183 Die Revision Change From “B” to “C”

Dear Customer:

Please be advised that ZiLOG is in the process of changing the current Z80S183/Z80L183 die revision "B" for the Mixed Signal 180. The new Z80S183/Z80L183 die revision “C” is fully compatible with the existing Z80S183/Z80L183 with the exception of the following improvements.

1. Improved Sleep Mode current of less than 1.7 mA @ 5V less than 700µA @ 3V.
2. All modes of the Watch Dog Timer are functional.
3. The CPU ID Register at location 3Dh is changed from 00h to 02h to reflect the new die.

All Z80S183/Z80L183 have a date code in the lower left corner of the package and follow the yyww convention, where yy is the year and ww is the week. The improved die will be stamped date code later than 0025. If you wish to receive qualification samples of the new product, contact the ZiLOG field sales office serving your area.

Sincerely,

Mike Burgdorf
Director
Reliability and Quality Assurance

ZAC00-0045

CHAPTER 3

Qualification Requirements

PRODUCT/PROCESS QUALIFICATION REQUIREMENTS

Per Procedures SOP0940, SOP0903 and SOP0909, ZiLOG performs initial qualification on new processes, products and packages. Re-qualification is required when material changes occur.

Table 4-1. Product/Process Qualification Requirements

Test	*Sample Size*	*Acceptance Criteria*	*MIL-STD 883C/Procedure*	*Test Conditions*
ESD	10	HBM	3015.7	2 KV Min.
CMOS Latchup	6	200 mA Min	QR - QCC-1425 EIA/JESD78	3 PTIC, 3 NTIC
Operating Life	77	1/77	1005	150°C, 5V 184 Hour/Full Qual
Temp Cycle	45	0/45	1010, Condition C	–65°C to 150°C 500 Cycles/Qual 1000 Cycles/Test
Pressure Pot	45	0/45	QCC-1403	336 Hours 121°C at 2 ATM
HAST	45	0/45	PM 25-13	96 Hours 140° C, 85% RH, 2 ATM
Package Integrity	10	0/10		240°C, 10 Sec

Note: Process Qual requires three (3) lots, Product Qual requires one (1) lot.

ZiLOG Product Qualification Summary

PRODUCT QUALIFICATION SUMMARY

ZiLOG Authorized Distribution

Document Control Nbr.: QR-9392 Rev.: 02

Page 1 of 1

		DATE:	12-4-01
PRODUCT:	Z86L88	**PROCESS:**	UMC 0.35 um
WRITTEN BY:	Joseph Brajkovich	**APPROVED:**	M. Burgdorf

- **INTRODUCTION**

This report summarizes the qualification results of the Z86L88 16K IR Microcontroller.

- **INFORMATION SUMMARY**

All qualification tests were performed to MIL-STD-883 and/or internal ZiLOG procedures.

PRODUCT QUALIFICATION

Test Description	Test Method	Condition	Test Result
ESD	MIL-STD-883/3015	Condition D	PASS
Latch-up	QCC1425	Per Test	PASS
Burn-in	MIL-STD-883/1005	Condition B, 150° C	0/77 184 hours
Temperature cycle	MIL-STD-883/1010	Condition C	0/50 1000 cycles
Pressure pot	120° C, 15 PSI	Per Test	0/50 336 hours
HAST	140° C, 85% RH	Per Test	0/50 96 hours
Package integrity	240° C, 10 seconds	Per Test	0/15

QUALIFICATION	TYPE	DOC. NO.
Process	UMC 0.35 um	QR-0656
Device	Z86L88/G	QR-1098

Package Qualification Requirements

Test	*Sample Size*	*Acceptance Criteria*	*MIL-STD 883C/Procedure*	*Test Conditions*
Solderability	4	0/15	2003	LTPD 15/Leads
Physical Dimensions	15	0/15	2016	Per Mil-STD
Lead Fatigue	15	0/15	2004	Per Mil-STD
External Visual	4	0/4	1004	Per Mil-STD
Internal Visual	4	0/4	1004	Per Mil-STD
Die Shear	3	0/3	QCC-0105	8 Lbs Min
Bond Strength	4	0/15	2011, Condition D	4 gms Min.
Bond Shear	3	0/3	QCC-0184	
Operating Life	77	1/77	1005	150°C, 5V 184 Hour/Full Qual
Temp Cycle	45	0/45	1010, Condition C	–65°C to 150°C 500 Cycles/Qual 1000 Cycles/Test
Pressure Pot	45	0/45	QCC-1403	336 Hours 121°C at 2 ATM
HAST	45	0/45	PM 25-13	96 Hours 140°C, 85% RH, 2 ATM
Package Integrity	5	0/15		240°C, 10 Sec
X-Ray	32	0/32	2012	Per Mil-STD
Solder Dunk	5	0/5		Per Test Method

ZiLOG Package Qualification Summary

PACKAGE QUALIFICATION SUMMARY

Document Control Nbr.: QR-3002 Rev.: 01

Page 1 of 1 OP25

PACKAGE TYPE: 44L QFP **DATE:** 1-27-99

WRITTEN BY: Joseph Brajkovich **APPROVED:** Alice Baluni

- **INTRODUCTION**

This report summarizes the qualification results of the 44L QFP package.

- **INFORMATION SUMMARY**

All qualification tests were performed to MIL-STD-883 B, C and/or internal ZiLOG procedures.

PACKAGE QUALIFICATION

Test Description	Test Method	Condition	Test Result
Bond Strength	MIL-STD-883/2011	Condition D	6.8/8.2/7.5 min/max/ave
Ball Shear	QCM-0184	Per Spec	0/3
Die Shear	QCM-0105	Per Spec	0/3
Physical Dimensions	MIL-STD-883/2016	Per Test Method	0/15
Resistance to Solvents	MIL-STD-883/2015	Per Test Method	0/15
Lead Fatigue	MIL-STD-883/2004	Per Test Method	0/1
Solderability	MIL-STD-883/2003	Per Test Method	0/6
Pressure Pot	QCC1403	Per Spec	0/45 336 hrs
Temperature Cycle	MIL-STD-883/1010	Condition C	0/45 1000 cycles
Burn-In	MIL-STD-883/1005	125ºC	0/77 1000 hrs
Package Integrity	240ºC, 10 seconds 3X	Per Test Method	0/15
Solder Dunk	240ºC, 10 seconds 3X	After 1000 Temp Cycle	0/5

QUALIFICATION	TYPE	DOC. NO.
Package	44L QFP	QR-0308

CHAPTER 4

Quality Monitor Systems

FAILURE RATE PREDICTION CALCULATIONS

ZiLOG estimates the operating life of our products through statistical methods. It is not possible to guarantee the lifetime of an individual part because the tests to determine this are destructive. Therefore, we can only use statistics to predict the typical behavior of groups of parts. These predictions, and the methods they are based on, are documented in FIT reports. The FIT report is based on process specific data and is derated to reflect individual device characteristics. FIT reports are available for all of ZiLOG's products.

Other factors that affect device lifetime include actual operating hours, ambient temperature, stability of the power supply, board assembly and other handling practices. All of these factors are outside of the control of ZiLOG and may dramatically shorten the lifetime of a device.

The failure rate for each product and process is a function of time, temperature and applied power. The primary temperature is, of course, the product junction temperature. This is externally influenced by the ambient temperature and internally influenced by the power dissipated in the die. The power dissipation, in turn, is a function of the duty cycle and applied VCC. In the case of CMOS, product power dissipation is also a function of the operating frequency. ZiLOG product failure rates were derived from accelerated life test results accumulated on an ongoing basis as part of the ZiLOG reliability monitor. The accelerated life test reliability data includes both infant mortality (early life results 0-160 hours) and long term life results (168-1000 hours). Various interim time points and sample sizes are used. Lifetest may be performed at either 125°C for 1000 hours or the Mil-Std-883 equivalent or 150°C for 184 hours.

The acceleration obtained when using high temperature life stressing, may be calculated for various stress and application temperatures using the widely accepted Arrhenius equation as follows:

$$A = \exp(-Ea(T1 - T2)/k(T1)(T2))$$

Where

A:	Acceleration factor
Ea:	Activation energy (eV)
T1:	Application junction temperature (°K)
T2:	Stress junction temperature (°K)
k:	Boltzmann Constant 8.62 x 10^{-5} (eV/°K)

Z85230VSC FIT Rate Calculation

The acceleration obtained when using high temperature life stressing may be calculated for various stress and application temperatures using the widely accepted Arrhenius equation as follows:

$$A = \exp(-Ea\ (T1 - T2) / (k\ (T1)\ (T2)))$$

Where

A:	Acceleration factor
Ea:	Activation energy (eV)
T1:	Application junction temperature (˚K)
T2:	Stress junction temperature (˚K)
k:	Boltzmann Constant 8.62 x 10-5 (eV / ˚K)

Assume Ea = .7, Ta application = 55C, Ta stress = 125˚C and k = 8.62 x 10^5. Consider now a typical CMOS product Z85230 operating with a 100% duty cycle at 16 MHz in a 44 pin PLCC package. Then with a VCC of 5V and an Icc of 7 ma this would give T1 = 330˚K and T2 = 400˚K.

$$A = \exp(-.7(330 - 400) / 8.62 \times 10^5\ (330)\ (400)\ ) = 75$$

So 1000 hours of life stress at 125˚C is equivalent to 75,000 hours of system application operation at 55˚C.

FIT and Failure Rate Estimation:

Given High Temperature Operating Life stress results:

	168 Hours	500 Hours	1000 Hours
Z85230	0/76	0/76	0/76
Rel Monitor 1994	0/837	0/760	0/606
Rel Monitor 1995	0/10,759		
Rel Monitor 1996	1/6,152		
Rel Monitor 1997	0/7,520		
Rel Monitor 1998	0/22,470		
Rel Monitor 1999	0/38,258	077	0/77
Rel Monitor 2000	0/61,646	0/231	0/231
Rel Monitor 2001	0/12,992	0/200	0/200
Rel Monitor 1H-2002	0/8,394		

Failure Rate Estimations are made assuming a Poisson distribution using the Chi^2 density function to assign confidence values as an estimate for the general population as follows:

60% Confidence # Fails = 1 then Chi^2 = 4.05

Given 1 reject from 29,527,680 device hours at 125˚C. Then using Chi^2 this gives a median failure rate of 4.05/2 rejects per 29,527,680 device hours or 0.0686 rejects per 10^6 device hours.

Failure rate = 0.0686 rej / 10^6 dev. hrs.
= 68.6 rej / 10^9 dev. hrs.
= 68.6 FIT at 125 C

Failure Rate = 68.6/75 = 1 FIT at 55˚C (A = 75 as above)
MTBF = 10^9/1 = 124,471 years

ESD TESTING METHODOLOGY

ZiLOG has an unqualified commitment to quality and reliability and, as part of this commitment, ZiLOG strives to provide the best possible ESD protection for each of our products.

Since 1983, ZiLOG has had an ongoing electrostatic discharge development program to monitor and improve its ESD protection circuitry. During an ESD event, the ESD protection circuitry must absorb the power of the ESD pulse while allowing little or no damage to occur to the internal circuitry of the chip. A 3000 volt ESD pulse can induce transient currents approaching one amp, and it is the management of these transient currents that is the key to good ESD protection. At ZiLOG, ESD protection circuits have been developed to optimize the handling of ESD pulse currents, by paying close attention to current flow patterns, and minimizing current density and crowding problems that cause damage to the circuitry. This circuitry has resulted in typical ESD failure voltages above 2000 volts for NMOS products and above 4000 volts for CMOS products, with concomitant improvement in product quality and reliability.

All of ZiLOG's products are tested for their ESD immunity as part of routine internal qualification procedures. The ESD test hardware is in compliance with MIL-STD-883 and Method 3015.7.

LATCHUP TESTING METHODOLOGY

ZiLOG has an unqualified commitment to quality and reliability and, as part of this commitment, also strives to provide each of its products with the best possible latchup protection.

ZiLOG has an ongoing program to monitor and improve its latchup protection circuitry. Latchup may occur as a result of either current injection (positive or negative) or supply pin overvoltage. The latchup action is that of a parasitic SCR, converting from a high-impedance state, to a low impedance, regenerative, state. The resulting current flow may exceed the design capabilities of the device. Damage may occur to interconnections (bond wires and die metallization) as a result of thermal heating effects and excessive current flow.

During conditions, which may lead to latchup, the device must be able to shunt the triggering event (the positive or negative injection current) without damage to the device. ZiLOG has targeted a 200 mA minimum latchup requirement for all new designs to minimize the risk of latchup. In addition, ZiLOG recommends that the customer do a careful analysis of system transients to ensure that our maximum undershoot and overshoot applied potentials are not violated. Absolute maximum ratings are: voltage on Vcc with respect to V_{SS} – 0.3V to +7.0V and voltages on all inputs with respect to V_{SS} – 0.3 to V_{CC} + 0.3V.

All of ZiLOG's products are tested for their latchup immunity as part of routine internal qualification procedures. The latchup test hardware is in compliance with EIA JEDEC Standard 78, and the detailed test procedure is per ZiLOG specification QCC1425, which is available upon request.

ZiLOG'S RELIABILITY SUMMARY

ZiLOG's reliability program is unique, in that the reliability testing takes place on standard production material at the point of assembly. Reliability testing has been integrated into the manufacturing process. This flow creates a "Quick Reaction" reliability monitor, and allows ZiLOG to ensure the integrity of material prior to shipment, gather trend analysis data for internal corrective actions, and maintain a meaningful database for customer review.

The tests currently employed under ZiLOG's quick reaction reliability monitor, include early life (burn-in), steam pressure pot, and temperature cycle. Testing conditions are included with the attached test results.

In addition to early life testing, a long-term life test is performed on selected lots to gather FIT data. Test conditions and FIT calculations are included with the attached data. Following are brief descriptions of various reliability tests included in this program:

EARLY LIFE

Early Life testing, also called burn-in, is typically performed at 125°C for 168 hours. A dynamic or static bias is employed, depending on the device that is being tested. Early Life test results expose process or assembly defects. These results are a valuable measure of a given fabrication or assembly process.

LONG TERM LIFE

Long Term Life testing is generally performed at 150°C for 184 hours. Either dynamic or static bias is used to stress the device appropriately. These test results are used to estimate field operation lifetime for a device. This data can be applied to all products manufactured using the same fabrication process.

PRESSURE POT

Pressure pot testing is performed at 121°C, 15 PSIG, and 100% relative humidity. This test evaluates the ability of a plastic device to withstand the long-term effects of a humid environment.

TEMPERATURE CYCLE

Temperature Cycle testing is performed at a –65°C to 150°C temperature. This test uses an air-to-air environment. The 215°C cold to hot temperature difference determines if proper thermal expansion matching exists between all materials used in device manufacture. The temperature cycle simulates the thermal stresses a device undergoes during power-up and power-down events.

HIGHLY ACCELERATED STRESS TEST

The Highly Accelerated Stress Test (HAST) is performed at a 141°C temperature and 85% Relative Humidity (RH) at 2 ATM of pressure with alternate pin bias. This test replaces the traditional 85/85 test and greatly reduces the time taken to evaluate the ability of a plastic encapsulated device to withstand the long-term effects of a biased humid environment.

PACKAGE INTEGRITY TEST

Package Integrity testing ensures the integrity of surface mount devices in terms of package cracking, bonding craters, and marked deterioration as a result of heat application during the soldering operation. This includes testing of 5 units on each 3 legs as follows:

CONTROL	-	10-SECOND SOLDER DUNK AT 240°C
TEST 1	-	10-HOUR *PPT
		10-SECOND SOLDER DUNK AT 240°C
TEST 2	-	10-HOUR *PPT
		3-HOUR OVEN BAKE AT 150°C
		10-SECOND SOLDER DUNK AT 240°C

(*PPT = Pressure Pot Testing at 121°C, 100% RH, 2 ATM)

End-points are room temperature electrical test, visual inspection, mark permanency and crater test.

Table 5-1. ZiLOG's Reliability Monitor Testing Requirements

Test Conditions	***Product to be Tested***	***Frequency***	***SS***	***Allowable Rejects***	***Test***
Temp cycle	Each pkg type	Monthly	45	0	–65° to 150°C 100, 500, 1000 cycles
Pressure Pot	Package/Fab Process	Monthly	45	0	96, 168, and 336 hrs 121°C, 100% RH, 2 ATM
Burn-in	Per assembly and process flow	Weekly	77	0	168 hrs, 125°C
Life test	Per assembly and process flow	Every 2 Months	77	1	184 hrs cum, 150°C
Package Integrity	PLCC or QFP package	Weekly	15	0	10-hr Pressure Pot, 10 second solder dunk
ESD	Each new die revision or device	N/A	10	N/A	Mil Std 883
Latch-up CMOS	Each new die revision or device	N/A	10 or as needed	N/A	Per ZiLOG spec
HAST	1 pkg/fab process	Monthly	45	0	NMOS - 48 hours CMOS - 96 hours at 140°C, 85% RH 2 ATM
Solderability	Each package type	Monthly	3	0	Mil Std 883
Solder thickness monitor	Any package type with solder	Weekly	3	0	MAB 1042
Lead fatigue test	Each package type	Weekly	1	0	Per ZiLOG spec

Table 5-2. ZiLOG Reliability Monitor Early Life Test Conditions: 168 HRS, 125°C Burn-in CMOS Plastic Package 2002

Device Type	Lot No.	Rej	S/S	Fail Notes
1H – 2002				
Z8018008FSC	Y132AB0Q	0	77	
Z88C0020VED1700TR	EYH42CC0PBB	0	1134	
Z84C9008VED1380TR	EY130NR0PBG	0	206	
Z84C9008VED1380TR	EY130NR0OBG	0	397	
Z86E0208PSC1925	AYI43HH0BP	0	77	
Z84C9008VED1380TR	EY130NR0PAB	0	110	
Z84C9008VED1380TR	E123AJ0C	0	139	
Z8018233FSC	AY144LY0P	0	77	
Z84C9008VED1380TR	E125BN0QAA	0	528	
Z84C9008VED1380TR	E125BN0QABA	0	795	
Z84C9008VED1380TR	E125BN0QABB	0	462	
Z84C9008VED1380TR	E125BN0QBA	0	795	
Z8018008VSC	BX145AS0	0	77	
Z84C9008VED1380TR	E125BN0QBBA	0	795	
Z8622812PSC	E143GX0T	0	77	
Z88C0020VED1700TR	BY151BH0A	0	1801	
Z86C3316PSCR4124	AYH1120AR	0	77	
Z9023406PSCR51X3	EYH1314BG	0	77	
Z86C4312PSCR5122	BYH0988D	0	100	
Z86C9012PSC	EYH1373B	0	100	
Z86L8708PSCR51R3	EYHBJ28.01	0	77	
Z86L8708PSCR51R3	EHBJ27.0F	0	77	
Z86C0208PSCR517J	EZ209HU0E	0	77	

Table 5-2. ZiLOG Reliability Monitor Early Life Test Conditions: 168 HRS, 125°C Burn-in CMOS Plastic Package 2002

Device Type	*Lot No.*	*Rej*	S/S	*Fail Notes*
Z86C0412PECR4537	EZ208DS0B	0	77	
Z86L8808PSCR51JW	NXHCE27.0CT	0	77	
Z85C3008VSC	B038GN0QB	0	77	
Z85C3008VSC	B038GN0QA	0	77	
Z84C0008PEC1983	A036FY0X1P	0	77	
Z84C0008PEC1983	A038GG0PQ	0	77	
Z86C0712PSCR2568	B135PT0RBB	0	100	
Z84C9010VSC	EY20SLU0Q	0	77	
Z84C0008FEC	BY206BJ0B	0	77	
Z8S18033VSC	EY145BN8A	0	77	
Z8S18033VSC	BY204FH0AR	0	77	
Z86C3312PECR50RX	BX208DL0P	0	77	
Z9023406PSCR522X	BYHCE29	0	77	
Z86C9533ASC2041	A125CF8B	0	77	
Z86L8808PSCR51JW	NXHCE27.0CT	0	77	
Z9023406PSCR522X	BYHCE29	0	77	
Z9025506PSCR523H	BYN22H6895.00P	0	77	
Z9025506PSCR51AP	BYH1601B	0	77	
Z85C3008VSC	S042AE0R	0	77	
Z85C3008PSC	K041HJ0S	0	77	
Z86C0208PSCR4502	K207PY0AR	0	77	
Z903561212PSCR50LM	BH1666AC	0	77	
Z8L18020FSC	A214GL0AAP	0	77	
Z8S18020VSC	K207XX0AR	0	77	
Z85C3008PSC	K041HJ0S	0	77	

Table 5-2. ZiLOG Reliability Monitor Early Life Test Conditions: 168 HRS, 125°C Burn-in CMOS Plastic Package 2002

Device Type	*Lot No.*	*Rej*	S/S	*Fail Notes*
Z84C9010VSC	K207HR0AP	0	77	
Z8S18020VSC	K207XX0AR	0	77	
Z9023406PSCR5140	BYH1786D	0	77	
Z84C9010VSC	EY205LU0Q	0	77	
Z9025506PSCR51AP	BYH1490FD	0	100	
Z8702414SSCR51XK	BHBT78.04B	0	72	
Z8702414SSCR51XK	CHBT77	0	75	
Z8S18033VSC	BY204FH0AR	0	77	
2H - 2002				
Z8S18020VSC	A222FN0AQ	0	77	
Z86L4308FSCR50AF	BZ222HS0B	0	77	
Z86E3312SSC	AZ222JK0AAQ	0	77	
Z86E0208PSC1925	AZ221TU0PA	0	77	
Z84C0006PEC	KZ219KN0P	0	100	
Z9023406PSCR51J1	BHCWF8.020A	0	100	
Z8S18010VSC	A222FN0AQ	0	100	
Z86K1505PSCR4530	AZ233FP0PB	0	100	
Z9023406PSCR50M5	BYH1509RB	0	100	
Z84C0010PEC	AZ219KP0QR	0	100	
Z86L4308FSCR50AF	BZ222HS0B	0	100	
Z86E0208PSC1925	AZ222JJ0AAB	0	100	
Z86E0208PSC1925	AZ223FZ0PA	0	100	
Z86E0812SSC1866	NZ224KR0PB	0	100	
Z86E3312SSC	AZ222JK0AAQ	0	100	
Z86E0412PSC1866	AZ223HW0APB	0	100	

Table 5-2. ZiLOG Reliability Monitor Early Life Test Conditions: 168 HRS, 125°C Burn-in CMOS Plastic Package 2002

Device Type	*Lot No.*	*Rej*	S/S	*Fail Notes*
Z86E0208PSC1925	AZ221TU0PA	0	100	
Z86E0208PSC1925	AZ221TU0PC	0	100	
Z84C2006VEC	B219SV0S	0	100	
Z86E2112PSC	A048LW0X	0	100	
Z86E3312PSC	B225HN0APB	0	100	
Z86E3312PSC	BZ25HN0APB	0	77	
Z86C0812PSCR2422	AZ227CG0AP	0	77	
Z86C3312PSCR2130	B220CDDAAA	0	77	
Z8F6403FZ030SC	AR60986.1P	0	77	
Z864170813SCR3212	BYH16655B	0	77	
Z8674312FSC	BZ228AL0AQ	0	77	
Z84C0008FEC	AZ221JN0PQA	0	100	
Z86C6116PSCR3360	AZ227LN0AQ	0	100	
Z85C3008VSC	BZ228SY0	0	100	
Z8S18020VSC1960	B001LN0P	0	100	
Z8702414SSCR52CH	AZHF11.132A	0	77	
EZ80F92AZ020SC	KR61001.AZ	0	76	
Z86C0812PSCR50PX	AZ234HJ0PA	0	100	
Z86E0212PSC1866	AZ233AY0PPA	0	100	
Z86L8808PSCR51JW	BZHF03S.00E	0	100	
Z84C00010PEC	AZ231JP0RR	0	100	
Z9023306PSCR51J9	BHF1W2.03C	0	100	
Z8018008VSC	BZ233BF0	0	100	
Z9025106PSCR52NN	B230EJ0A	0	77	
Z86C3312PECR517F	NY214GN0P	0	77	
Z8019520FSC	K232CN0A	0	77	
Z86C6516PSCR3332	NZ235DG0B	0	77	
Z86C6116PSCR2224	AZ230PU0KQA	0	77	
Z84C00008PEC	A222KS0ATQ	0	77	
Z86K1505PSCR4230	AZ239KY0BPA	0	77	
Z8F6403FZ030SC	AR61105.A1	0	83	

Table 5-3. ZiLOG Reliability Monitor Early Life Test Conditions: 168 HRS, 125°C Burn-in NMOS Plastic Package 2002

Device Type	*Lot No.*	*Rej*	S/S	*Fail Notes*
1H - 2002				
Z0843004DSA0563	B0315W0RRA	0	381	
Z0843004DEA0539	B031SW0RQ	0	178	
Z0843004DSA0563	B031SW0RRBA	0	1146	
Z0843004DSA0563	B031SW0RRBB	0	501	
Z0844004DSA0541	B607BDOACAB	0	1669	
Z0840004DEA0540	B709GJ0AAPB	0	275	
Z0843004DSA0563	B031SW0RRBC	0	60	
Z0840004DEA0540	B709GJ0AAPC	0	284	
Z0853606DEA	B031RZ0BA	0	188	
Z0840004DEA0540	B709GJ0AAPE	0	285	
Z0803008DEA	B840KZ0AQA	0	198	
Z0853606DEA	B031RZ0BB	0	106	
Z0840004DEA0540	B709GJ0AAPG	0	285	
Z0840004DEA0540	B709GJ0AAPH	0	285	
Z0840004DEA0540	B709GJ0AAPI	0	285	
Z0840004DEA0540	B709GJ0AAPJ	0	253	
Z0840004DEA0560	B709GJ0AAPG	0	285	
Z0847004PSC	E1451Z0P	0	100	
Z0803606PSC	E144NT0P	0	180	
Z084004DSA0560	B709GJ0AARA	0	285	
Z084004DSA0560	B709GJ0AARB	0	285	
Z084004DSA0560	B709GJ0AARC	0	285	
Z084004DSA0560	B709GJ0AARD	0	285	
Z084004DSA0560	B709GJ0AARE	0	285	
Z084004DSA0560	B709GJ0AAQH	0	200	
Z084004DSA0560	B709GJAAQF	0	73	
Z0803606PSC	E204FF0AP	0	77	
Z0840004PSC	EY205AN0AP	0	77	
Z0847006PSC	EY149EX0AR	0	77	

Table 5-3. ZiLOG Reliability Monitor Early Life Test Conditions: 168 HRS, 125°C Burn-in NMOS Plastic Package 2002

Device Type	*Lot No.*	*Rej*	S/S	*Fail Notes*
2H - 2002				
Z0847006PSC	A212LN0AZP	0	100	
Z0853006PSC	A221CG0QP	0	100	
Z0853006VSC	A217JR0RR	0	77	
Z0844006PSC	B145WZ0	0	77	
Z0853606VSC	BZ203AE0AP	0	100	
Z0853006PSC	A237LZ0AAPA	0	77	
Z0853006PSC	A237LZ0AAQP	0	77	

Table 5-4. ZiLOG Reliability Monitor Long-Term Life Test Conditions: 150°C, 5V,184 HRS Burn-in CMOS 2002

Device Type	*Lot No.*	Rej	*S/S*	*Fail Notes*
1H - 2002				
Z86L990PZ008SCR51ML	BYHBHAE	0	77	
Z86L990PZ008SCR51J5	BH0517A	0	77	
Z86C0612PSCR51RX	E146EW8R	0	77	
Z8932320FSCR51M7	AYH2TX8R	0	77	
Z86C3316PSCR51F7	AY148BS8	0	77	
Z9023406PSCR51X3	EYH1B032	0	77	
EZ80L92AZ020SC	MB54G	0	76	
Z9023406PSCR503W	EYH134BG	0	76	
Z9023406PSCR51X3	EYHBQ33	0	77	
Z86L8708PSCR51R3	EYHBS28.01	0	77	
Z86L8708PSCR51R3	EHBJ27.0F	0	77	
Z0221524VSCRJ0A5	KY209KT0A	0	77	
Z9023406PSCR522X	BYHCE29	0	77	
Z8702414SCR51XK	BHBT78.04B	0	72	
Z8702414SCR51XK	CHBT77	0	75	
Z86L990PZ008SCR51ML	EYHCF08	0	77	
Z0221524VSCR50A5	BY203BJ84	0	77	
2H - 2002				
Z1GS02BA	EY204EE8HSC	0	77	
Z1GS03BA	EY215BX8	0	77	
Z9023406PSCR51J1	BCWF8.02DA	0	77	
Z8702414SSCR52CH	KR61001.A2	0	77	
EZ80F92AZ020SC2047	AZHF11.132A	0	77	
Z86L34PZ008SCR525N	N2AHF565.01	0	77	
Z0221524VSCR51JA	KA227EU8AB	0	77	

Table 5-5. ZiLOG Reliability Monitor Long-Term Life Test
Conditions: 125°C 1000 HRS Burn-in CMOS 2002

Device Type	Lot No.	Rej	S/S	Fail Notes
1H - 2002				
Z85C3008PSC	K041HJ0S	0	77	
Z8S18020VSC	K207XX0AR	0	77	
2H - 2002				
Z86C3312PSCR2130	B220CD0AAA	0	77	
Z84C0006PEC	KZ219KN0P	0	77	

Table 5-6. Reliability Test Summary Early Life Test Summary 2002

Technology	*Package Type*	*Samples Tested*	*Rejects*	*FITS (55°C,60%,0.7eV)*
1H - 2002				
NMOS	Plastic	8,873	0	8
CMOS	Plastic	10,172	0	7
TOTAL 1H - 2002:		**19,045**	**0**	**4**
2H - 2002				
NMOS	Plastic	608	0	121
CMOS	Plastic	4,245	0	17
TOTAL 2H - 2002:		**4,853**	**0**	**15**
TOTAL - 2002		**23,898**	**0**	**3**

Table 5-7. Reliability Test Summary Long-Term Life Test Summary 2002

Technology	**Device Hrs @ 125°C**	*Rejects*	*FITS (55°C,60%,0.7eV)*
1H - 2002			
CMOS	1,454,000	0	9
2H - 2002			
NMOS	154,000	0	80
CMOS	539,000	0	23
TOTAL 2H – 2002	**693,000**	**0**	**18**
TOTAL – 2002	**2,147,000**	**0**	**6**

Table 5-8. ZiLOG Reliability Monitor Pressure Pot Test Conditions: 121°C, 2 ATM. CMOS Plastic Packages 2002

Device Type	Lot No.	96 Hrs Rej	96 Hrs S/S	168 Hrs Rej	168 Hrs S/S	336 Hrs Rej	336 Hrs S/S	Fail Notes
1H - 2002								
Z86L87088PSCR51R3	EYHBJ270F	-	-	0	45	0	45	
Z86L990PZ008SCR51ML	BYHBHAE	-	-	0	45	0	45	
Z86L990PZ008SCR51J5	BH0517A	-	-	0	45	0	45	
Z8018008VSC	BX145ASO	-	-	-	-	0	45	
Z9023406PSCR51X3	EYHB032	-	-	0	45	0	45	
Z84C0008PEC1983	A036FY0X1P	-	-	-	-	0	45	
Z8018008FSC	Y132AB0Q	-	-	-	-	0	45	
Z8937320ASC	B810WW8Q2	-	-	-	-	0	45	
Z86L87SZ008SCRXXX	G1473AFB	-	-	-	-	0	45	
Z86C3316PSCR4124	AYH1120AR	-	-	0	45	0	45	
Z86C0408PECR2981	A204EK0RPPA	-	-	-	-	0	45	
Z86L8808SSCR51PX	BXH1505APB	-	-	0	45	0	45	
Z84C0008FEC	BY206BJ0B	-	-	-	-	0	45	
Z9023406PSCR5140	BYH1786D	-	-	-	-	0	45	
Z8673312PSC	0EY204JW0B	-	-	-	-	0	32	
Z84C9010VSC	EY205LU0Q	-	-	-	-	0	45	
Z86L8808SSCR51XF	EYHBHTH.0CP	-	-	-	-	0	45	
Z86E136SZ016SC	NYH1736AAT	-	-	-	-	0	45	
Z86E136SZ016SC	NYH1736AATA	-	-	-	-	0	45	
Z85C3008VSC	B038NG0QA	-	-	0	45	0	45	
Z85C3008VSC	B038GN0QB	-	-	0	45	0	45	
Z0843006PSC	K037JX0T	0	45	-	-	0	45	
Z8937320ASC	K813TY8	0	45	-	-	0	45	
Z16C0110PSC	B9S0JY0	-	-	-	-	0	45	

Table 5-8. ZiLOG Reliability Monitor Pressure Pot Test Conditions: 121°C, 2 ATM. CMOS Plastic Packages 2002

Device Type	Lot No.	96 Hrs Rej	96 Hrs S/S	168 Hrs Rej	168 Hrs S/S	336 Hrs Rej	336 Hrs S/S	Fail Notes
Z8702414SSCR51XK	BHBT78.04B	-	-	0	45	0	45	
Z8702414SSCR51XK	CHBT77	-	-	0	45	0	45	
Z8623316VSCR4591	KE2080Q	-	-	-	-	0	45	
Z84C9010VSC	K207HR0AP	-	-	-	-	0	45	
Z85C3008PSC	K041HJ0S	-	-	-	-	0	45	
Z16C0110PSC	K930FX0	-	-	-	-	0	45	
Z86C0208PSCR4502	K207PY0AR	-	-	0	45	0	45	
2H - 2002								
Z8F6403FZ020SC	AR60986	-	-	-	-	0	45	
Z86E136SZ016SC	AG0797EX	-	-	0	45	0	45	
Z80180008VSC00TR	BZ221XX0B	-	-	-	-	0	45	
Z8S18020VSC	K207XX0AR	-	-	0	45	0	45	
Z8612912SSC	A224DL0AP	-	-	0	45	0	45	
Z9023406PSCR51J1	BHCWF8.02DA	-	-	0	45	0	45	
Z8PE003HZ010SC	B219FP0	-	-	0	45	0	45	
Z86C6516PSCR3332	NY211NS0B	-	-	0	45	0	45	
Z84C0006PEC	KZ219KN0P	-	-	0	45	0	45	
EZ80F92AZ020SC2047	KR61001.02	-	-	0	45	0	45	
Z86D991SZ008SC2046	SY206HH0BAP	-	-	1	45	0	44	B8F -EOS
Z8S18010VSC	A222FN0AQ	-	-	0	45	0	45	
Z8F6403FT020SC	R61105.A1	-	-	0	45	0	45	
Z8702414SSCR52CH	AZH11.132A	-	-	0	45	0	45	
Z86C3312PSCR3130	B220CD0AAA	-	-	0	45	0	32	
Z8641708BSCR3212	BYH1665B	-	-	-	-	0	45	
Z86L98HZ008SCR526R	SHCNQ5.02RA	-	-	0	45	0	45	
Z8018233ASC1932	AH0657SB	-	-	-	-	0	45	
Z8019520FSC	K232CN0A	-	-	-	-	0	45	
Z86C3312PECR5177	NY214GN0P	-	-	-	-	0	45	

Table 5-9. ZiLOG Reliability Monitor Pressure Pot Test Conditions: 121°C, 2 ATM. NMOS Plastic Packages 2002

Device Type	Lot No.	96 Hrs Rej	96 Hrs S/S	168 Hrs Rej	168 Hrs S/S	336 Hrs Rej	336 Hrs S/S	Fail Notes
1H - 2002								
No Samples Available								
2H - 2002								
Z0853606VSC	B205APOA	-	-	0	45	0	45	

Table 5-10. ZiLOG Reliability Monitor For Temperature Cycling Test Conditions: Condition C, -65°C To 150°C CMOS 2002

Device Type	Lot No.	100X Rej	100X S/S	500X Rej	500X S/S	1000X Rej	1000X S/S	Fail Notes
1H - 2002								
Z86L8708PSCR51N7	EYHBHMA	-	-	0	45	0	45	
Z86L88708PSCR51R3	EYHBJ270F	-	-	0	45	0	45	
Z86L990H2008SCR50XC	H0757	-	-	0	45	0	45	
Z8623312PSCR4409	EY149EP0RA	0	45	-	-	-	-	
Z8623312PSCR4409	EY149EP0RB	0	45	-	-	-	-	
Z856L8808PSCR51JW	EY10004AJ	0	45	-	-	-	-	
Z86E136PZ016SC	EYH0765AA	0	45	-	-	-	-	
Z84C3008PEC	EY144SW0V	0	45	-	-	-	-	
Z84C3008PEC	EY145DE0Q	0	45	-	-	-	-	
Z84C3008PEC	EY145DE0R	0	45	-	-	-	-	
Z8937320ASC	B810WW8Q2	-	-	0	45	0	45	
Z9023406PSCR51X3	EYHBQ33	-	-	0	45	0	45	
Z86C0208PSCR517J	EZ209HU0E	0	45	-	-	-	-	
Z86C0412PECR4537	EZ208DS0B	0	45	-	-	-	-	
Z8673312PSC	OEY204JW0B	-	-	0	45	0	45	
Z86L8808SCCR51XF	EYHBHTH.0CP	-	-	-	-	0	45	
Z84C9010VSC	EY205LU0Q	-	-	-	-	0	45	
Z8523008VSC	AY142YY0BBP			0	45	0	45	
Z8611608SSCR3407	AY142RY0RX1	-	-	0	45	0	45	
Z8611608SSCR3407	AY142RY0RX2	-	-	0	45	0	45	
Z86C3316PSCR4124	AYH1120AR	-	-	0	45	0	45	
Z84C0008PEC1983	A036FY0X1P	-	-	0	45	0	45	
EZ80L92AZ020SC	AMB54GC	0	45	0	45	0	45	
Z9035612PSCR3720	BYH1722A	-	-	0	45	0	45	

Table 5-10. ZiLOG Reliability Monitor For Temperature Cycling Test Conditions: Condition C, -65°C To 150°C CMOS 2002

		100X		500X		1000X		
Device Type	***Lot No.***	***Rej***	***S/S***	***Rej***	***S/S***	***Rej***	***S/S***	***Fail Notes***
Z8018008VSC	BX145AS0	-	-	0	45	0	45	
Z86L8808SSCR51XP	BXH1505APB	-	-	0	45	0	45	
Z8937320ASC	B810WW8Q2	-	-	0	45	0	45	
Z84C008FEC	BY206BJ0B	-	-	-	-	0	45	
Z9023406PSCR5140	BYH1786D	-	-	-	-	0	45	
Z86C0408PECR2981	A204EK0RPPA	-	-	-	-	0	45	
Z853008VSC	B038GN0QA	-	-	0	45	0	45	
Z853008VSC	B038GN0QB	-	-	0	45	0	45	
Z8018008VSC	BX145AS0	-	-	0	45	0	45	
Z8018008FSC	Y132AB0Q	-	-	0	45	-	-	
Z86L827SZ008SCRXXX	G1473AFB	-	-	0	45	0	45	
Z86E136SZ016SC	AYH1736AASP	-	-	0	45	0	45	
Z86E0208PSC1925	AYB9BN0BBP	-	-	0	45	0	45	
Z86E0208PSC1925	AY143HH0BP	-	-	0	45	0	45	
Z86E126PZ016EC	AG0797EX	-	-	0	45	0	45	
Z8702414SCR51XK	CHBT77	-	-	0	45	0	45	
Z8702414SCR51XK	BHBT78.04B	-	-	0	45	0	45	
Z16C0110PSC	B9S0JY0	-	-	0	45	0	45	
Z8018008FSC	Y132AB0Q	-	-	0	45	0	45	
Z8523008VSC	S042AE0R	-	-	0	45	0	45	
Z86E136SZ016SC	NYH1736AAT	-	-	0	45	0	45	
Z86E136SZ016SC	NYH1736AATA	-	-	0	45	0	45	
Z84C9010VSC	K207HR0AP	-	-	0	45	0	45	
Z85C3008PSC	K041HJ0S	-	-	0	45	0	45	
Z16C0110PSC	K930FX0	-	-	0	45	0	45	

Table 5-10. ZiLOG Reliability Monitor For Temperature Cycling Test Conditions: Condition C, -65°C To 150°C CMOS 2002

Device Type	Lot No.	100X Rej	100X S/S	500X Rej	500X S/S	1000X Rej	1000X S/S	Fail Notes
Z86C0208PSCR4502	K207PY0AR	-	-	0	45	0	45	
2H - 2002								
EZ80L92AZ020SC	AMB54GC	0	45	0	45	0	45	
Z8018008VSC00TR	BZ221X0B	-	-	0	45	0	45	
Z8623316VSC4591	KE2080Q	-	-	0	45	0	45	
Z8S18020VSC	K207XX0AR	-	-	0	45	0	45	
Z8937320ASC	K813TX8	-	-	0	45	0	45	
Z8623312PSCR51XW	K151UY0RA	0	45	0	45	-	-	
Z86L8808PSCR51JW	KZHCP26.0MJ	-	-	0	45	-	-	
Z86L8808PSCR521A	KZHCNYS.0KA	-	-	0	45	-	-	
Z86L8808PSCR2607	KZH1772BE	-	-	0	45	-	-	
Z86L8808PSCR51JW	KZHCNL2.0B	-	-	0	45	-	-	
Z86L8808PSCR51JW	KZHCNSY.0G	-	-	0	45	-	-	
Z86L8808PSCR51JW	KZHCNSY.00E	-	-	0	45	-	-	
Z8PE003HZ010SC	B219FP0	-	-	0	45	0	45	
Z9023406PSCR522F	KHCRIT.0CRC	0	45	0	45	0	45	
Z86L8808PSCR51JW	OEY204JW0B	0	45	0	45	0	45	
Z9023406PSCR522F	KHCYGG.00PI	0	45	0	45	0	45	
Z86L8808PSCR4455	NZHCPJN.0QS	0	45	0	45	0	45	
Z8612912SSC	A224DL0AP			0	45	0	45	
Z86E2112PSC	A048LW0X	1	45	0	44	0	44	B3F Leakage
Z86L8808PSCR4455	BZHCW79.02E	-	-	0	45	0	45	
Z9023406PSCR51J1	AYH1120AR	-	-	0	45	0	45	
Z86L8808PSCR51J1	KZHCNL0.00C	0	45	0	45	0	45	
Z86E136PZ016SC	KH1577AD	0	45	0	45	0	45	
Z86E136PZ016SC	KH1577AG	0	45	0	45	0	45	
Z86C6516PSCR3322	NY211NS0B	-	-	0	45	0	45	
Z84C0006PEC	KZ219KN0P	-	-	0	45	0	45	
EZ80F92AZ020SC2047	KR61001.A2	-	-	0	45	0	45	

Table 5-10. ZiLOG Reliability Monitor For Temperature Cycling Test Conditions: Condition C, -65°C To 150°C CMOS 2002

		100X		500X		1000X		
Device Type	**Lot No.**	**Rej**	**S/S**	**Rej**	**S/S**	**Rej**	**S/S**	**Fail Notes**
Z86D991SZ008SC2046	SY206HH0BAP	-	-	0	45	0	45	
Z8018233ASC1932	AH0657SB	-	-	0	45	0	45	
Z8F6403FT020SC	R61105.A1	-	-	0	45	0	45	
Z8018233ASC1932	AH0657SB	-	-	0	45	0	45	
Z86C3312PSCR2130	B220CD0AAA	-	-	0	45	0	45	
Z8641708BSCR3212	BYH1665B	-	-	-	-	0	45	
Z8019520FSC	Y132AB0Q	-	-	0	45	0	45	
Z86C3312PECR517F	NY214GN0P	-	-	0	45	0	45	
Z86L98HZ008SCR526R	SHCNQ5.01RA	-	-	0	45	0	45	

Table 5-11. ZiLOG Reliability Monitor For Temperature Cycling Test Conditions: Condition C, -65°C To 150°C NMOS 2002

		100X		500X		1000X		
Device Type	**Lot No.**	**Rej**	**S/S**	**Rej**	**S/S**	**Rej**	**S/S**	**Fail Notes**
1H - 2002								
Z0844004DSA0541	B607BD0ACAA	-	-	0	45	0	45	
2H - 2002								
Z0843006PSC	K037JX0T	-	-	0	45	0	45	
Z0853606VSC	B205AP0A	-	-	0	45	0	45	

Table 5-14. ZiLOG Reliability Monitor Highly Accelerated Stress Test (HAST) Test Conditions: 140°C @ 85% Humidity At 2 ATM Of Pressure CMOS Plastic 2002

Device Type	Lot No.	Rej	S/S	48 Hrs Rej	96 Hrs S/S	Fail Notes
1H - 2002						
Z9023406PSCR51X3	EYHB032			0	45	
Z86L990PZ008SCR51ML	BYHBHAE			0	45	
Z86L990PZ00R51J5	BH0517A			0	45	
EZ80L92AZ020SC	MB546			0	45	
Z86L990PZ008SCR51ML	BYHBHAE			0	45	
Z86L990PZ008SCR51J5	BH0517A			0	45	
Z8702414SCR51XK	BHBT78.04B			0	45	
2H - 2002						
Z8702414SSCR52CH	AZHF11.132A			0	45	
EZ80F92AZ020SC2047	KR61001.A2			0	45	
Z8S18020VEC	B222FR0AP			0	40	
Z0221524VSCR51JA	KA227EU8AB			0	30	

Table 5-13. ZiLOG Reliability Monitor ZiLOG Package Integrity Test Results CMOS 2002

Device Type	Lot No.	Rej	S/S	Fail Notes
1H - 2002				
Z86E0208PSC1925	AY139BN0BBP	0	15	
Z86E3108SSCR50W0	AY147RS0BPP	0	15	
Z8018233FSC	AY144LY0P	0	15	
Z9035612PSCR3720	BYH1722A	0	15	
Z8018008VSC	BX145AS0	0	15	
Z86L8808SSCR51PX	BXH1505APB	0	15	
Z8624312FECR51R4	BY147KK0R	0	15	
Z8673312VEC	EY147KP0RB	0	15	
Z86L8708PSCR51R3	EYHBJ70F	0	15	
Z8018008FSC	Y132AB0Q	0	15	
Z86L827SZ008SCRXXX	G1473AFB	0	15	
Z84C0008PEC1983	A036FY0X1P	0	15	
Z8019520FSC	AY147NP0RAP	0	15	
Z86E3116PSC	BY150HR0AAD	0	15	
Z8673312VSCR3845	BY149GU0AAB	0	15	
Z86C8316SSCR4564	BY141JS0R	0	15	
Z86E0208HSC1925	BY135K0B	0	15	
Z86E0412PSC1866	EZ150NP0P	0	15	
Z8673312VSCR3845	EKY149GUOB	0	15	
Z80L183AZ030SCR4567	KG1164	0	15	
Z86E0812SSC1866	NZ150NP0A	0	15	
Z86C3316PSCR4124	AYH1120AR	0	15	
Z86E0208SECR516F	AZ203BP0APP	0	15	
Z86L430-8FSCR50AF	AX201CW0RPX	0	15	
Z15M1720ASC1868	A048TY0X10	0	15	
Z8624312PECR40945	BY202HS0RAD	0	15	
Z86733VSCR3845	BY201EZ0AAQ	0	15	
Z8623312SECR4472TR	B202HR0RA	0	15	
Z8617216FSCR5053	BY1506Y0RP	0	15	
Z86E0208HSC1925	BY135KZ0B	0	15	
Z8623312PSCR4409	EX201DL0R	0	15	
Z8S18033VSC	EY145BN8A	0	15	
Z86L8808SSCR51XF	EYHBHTH.0CP	0	15	
Z86L0808SSCR5009	NZ203SU0R	0	15	
Z86C0408PECR2981	A204EK0RPPA	0	15	
Z8673312VSCR3845	AY209AG0P	0	15	
Z8S18010FSC	AY204FN0AP	0	15	

Device Type	Lot No.	Rej	S/S	Fail Notes
Z86E136SZ016SC	AYH1736AASP	0	15	
Z9023406PSCR5140	BYH1786D	0	15	
Z8932320VECR519W	BY206BR0RBA	0	15	
Z86L8808SSCR4590TR	BXHCA91.0QC	0	15	
Z84C0008FEC	BY206BJ0B	0	15	
Z8673312PSC	OEY204JW0B	0	15	
Z84C9010VSC	EY205LU0Q	0	15	
Z86E136SZ016SC	NYH1736AAT	0	15	
Z86L8808PSCR51JW	NXHCE27.0CT	0	15	
Z86C8316PSCR264	AZ212CZ0PX	0	15	
Z8S18033VSC	1206FJ8ARP	0	15	
Z2209SZ000XC	ABS8859.1XA	0	15	
Z8673312PSC	BY210GN0AAP	0	15	
Z8S18033VSC	B207XX0AS	0	15	
Z8702414SCR51XK	BHBT78.04B	0	15	
Z9023306FSCR51J8	BYH1303Q	0	15	
Z86E0812SSC1866	EZ209LY0C	0	15	
Z8673312VSCR3845	E203BT0ABBA	0	15	
Z8PE002PZ010SCR523K	EZ209AR0AB	0	15	
Z86C0208PSCR4502	K207PY0AR	0	15	
Z8937320ASC	K813TY8	0	15	
Z8S18020VSC	K207XX0AR	0	15	
Z86E126PZ016EC	AG0797EX	0	15	
Z8612912SSC	A217JX0PNP	0	15	
Z8F6403FZ020SC	AR60986	0	15	
Z16C0110PSC	B9S0JY0	0	15	
Z8702414SCR51XK	BHBT78.04B	0	15	
Z853008PSC	K041HJ0S	0	15	
Z86L9533ASC	KH006A	0	15	
Z8623316VSCR4591	KE2080Q	0	15	
Z0221520ASCR50A5	BY150JP0A	0	15	
2H - 2002				
Z86K1505PSCR4530	AT221RU0AAC	0	15	
Z8S18033VSC00TR	A222FP0AQ	0	15	
Z8018110FEC	AY143GZ0AU	0	15	
Z86E132SZ016SC	AH1575AABAP	0	15	
Z9023406PSCR503W	BHCT27.00C	0	15	
Z8932320VECR50XPTR	BY206BS0A	0	15	
Z86D8608SSCR524	B224SY0AA	0	15	
Z86L4308FSCR50AF	BX208DK0B	0	15	
Z8E0010HEC	B20BL0S	0	15	

Device Type	***Lot No.***	***Rej***	**S/S**	***Fail Notes***
Z86E13016PEC	NZ221SU0	0	15	
Z86E0812SSC1866	NZ224KR0PAA	0	15	
Z86L8808PSCR51JW	KZHCP26.0N	0	15	
Z8L18220ASC	KY219GU0P	0	15	
Z86E0412PSC2004	AZ224C00APB	0	15	
Z8S18010VSC	A222FN0AQ	0	15	
Z8L18020FSC	A227PX0APPA	0	15	
Z8612912SSC	A224DL0AP	0	15	
Z9023406PSCR51J1	BHCWF8.020A	0	15	
Z86C4316VSCR4065	B226GT0P	0	15	
Z86D8608SSCR52L1	B224SY0AA	0	15	
Z86L4308FSCR50AF	BZ220HS0B	0	15	
Z8PE003HZ010SC	B219FP0	0	15	
Z86C6516PSCR3332	NY211NS0B	0	15	
Z86C0208SSCR3358	NZ224UZ0PB	0	15	
Z84C0006PEC	KZ219KN0P	0	15	
Z8937320ASC	K816FN0	0	15	
Z86L8808SCR50HWTR	SZHCPSN.5QB	0	15	
Z86E0812PSC1866	AZ227CW0RA	0	15	
Z86C8316SECR52JATR	BY1506Y0RP	0	15	
Z8018233ASC1932	AH0657SB	0	15	
Z86L8808PSCR4455	BZHWY3.1PC	0	15	
Z86L4308FSCR50AF	BZ220HS0B	0	15	
Z8641708BSCR3212	BYH1665B	0	15	
Z8PE003HZ010SC	BZ220BP0AA	0	15	
Z86E0208SSC1925	NZ224UZ0PB	0	15	
Z8937320ASC	K816FN0	0	15	
Z86D991SZ008SC2046	SY206HH0BAP	0	15	
Z86E0812PSC1866	AZ229EW0BPA	0	15	
Z86E3412SSC	AZ231PS0APA	0	15	
Z8018233ASC1932	AH0657SB	0	15	
Z8702414SSCR52CH	AZHF11.132A	0	15	
Z8673312PSC	BZ230AJ0	0	15	
Z8932320VECR50XP	B226DT0BA	0	15	
Z8674312FSC	BZ230AN0	0	15	
Z8641708BSCR3212	BYH1665B	0	15	
Z86D990HZ0082046	C0142BT0ABA	0	15	
Z86C3312PECR517F	NY214GN0P	0	15	
Z86C0812SSCR2433	NZ233WZ0BB	0	15	
EZ80F92AZ020SC2047	KR61001.A2	0	15	
Z8019520FSC	K232CN0A	0	15	
Z86E0412PSC1866	AZ237PT0PB	0	15	
Z8623312SECR4472TR	AZ235CY0PA	0	15	
Z8F6403FT020SC	AR6110.5A	0	15	
Z84C3008PEC	B228AB0AQ	0	15	
Z86E3412VSC	BZ228FW0A	0	15	
Z86L4308FSCR50AF	BZ237FG0AB	0	15	
Z86C6516PSCR3752	NE0903D	0	15	

Device Type	Lot No.	Rej	S/S	Fail Notes
Z86E0812SSCR5017TR	NZ235FN0P	0	15	
Z16M1720ASC1868	KA049B00X1	0	15	
Z86K1505PSCR5016	AH1656APB	0	15	
Z86C36SSCR5189TR	AZ24CJP0PA	0	15	
Z86L4308FSCR50AF	AZ243CU0PB	0	15	
Z09036512PSCR51MR	BH1670AQB	0	15	
Z86E7216FSC	B242PR0A	0	15	
Z86C3316PSCR2913	NZ243EH0BP	0	15	
Z86C0812SECR5129TR	NZ241EH0AA	0	15	

Table 5-14. ZiLOG Reliability Monitor ZiLOG Package Integrity Test Results NMOS 2002

Device Type	Lot No.	Rej	S/S	Fail Notes
1H - 2002				
Z0843006PSC	K037JX0T	0	15	
Z0853008VSC00TR	A217JR0SP	0	15	
Z0853008VSC	B217JR0	0	15	
2H - 2002				
Z0853606VSC	B224CY0AAP	0	15	
Z0853606VSC	B205AP0A	0	15	

Table 5-15. C-Mode Scanning Acoustic Microscope Monitor 2002
CMOS

Device Type	Lot No.	Sample Selection	Results
1H - 2002			
Z9035612PSC	BE2468	500X TC	0/5
Z8673312PSC	BY146GP0AB	FRESH SAMPLES	0/5
Z8673312PSC	BY143ET0B	FRESH SAMPLES	0/5
Z9035612PSCR3720	BYH1722	FRESH SAMPLES	0/5
Z8673312PSC	BY145CP0	FRESH SAMPLES	0/5
Z85C3008VSC00TR	B036DJ0FB	FRESH SAMPLES	0/5
Z9037116PSC	BY146GP0AA	FRESH SAMPLES	0/5
Z8673312PSC	BY145CP0B	FRESH SAMPLES	0/5
Z86C8316SSCR4564	BY145JS0R	FRESH SAMPLES	0/5
Z86L990PZ008SCR51J5	BH0517A	1000X TC	0/5
Z86L990PZ008SCR51ML	BYHBHAE	1000XTC	0/5
Z9035612PSCR3720	BY1722A	500X	0/5
Z8018008VSC	BX145AS0	500X	0/5
Z8611608SSCR3407	AY142RY0R1GB	500X	0/5
Z8611608SSCR3407	AYK12RY0RIHA	500X	0/5
Z86C0812SECR50AHTR	AZ150JZ0RAA	FRESH SAMPLES	0/5
Z86C8316SSCR4564	AY141JS0R1X	FRESH SAMPLES	0/5
Z86E0812SSC1866	AX144LT0QA	FRESH SAMPLES	0/5
Z86E0208SSCR2433	AZ147PZ0RP	FRESH SAMPLES	0/5
Z86C0812SSCR2433	AZ146ET0RPA	FRESH SAMPLES	0/5
Z8702114SSCR4216TR	AZ15V0RAP	FRESH SAMPLES	0/5
Z8611608SSCR3407	AY129FH0R	1000X TC	0/5
Z86E0208PSC1925	AY143HH0BP	500X	0/5
Z86E0208PSC1925	AY139BN0BBY	500X	0/5
Z86L8708PSCR51N7	EYHBHMA	1000X TC	0/5
Z86L0808SSCR5009	E151W0RQ	FRESH SAMPLES	0/5
Z86L8708PSCR51R3	EYHBJ270F	1000X TC	0/5
Z86L827SZ008SCRXXX	G1473AFB	FRESH SAMPLES	0/5
Z8018008FSC	Y132AB0Q	FRESH SAMPLES	0/5
Z86C0208SSCR50JH	N140CT0RAA	FRESH SAMPLES	0/5
Z86E0412SSC1866	NZ150NP0AP	FRESH SAMPLES	0/5
Z86C0812SECR5129TR	NZ150LY0RA	FRESH SAMPLES	0/5
Z86C0812SECR5129TR	NZ146EX0RB	FRESH SAMPLES	0/5
Z86E0412SSC1866	NZ145BH0AP	FRESH SAMPLES	0/5
Z86CE0812SEC	N145BH0AQ	FRESH SAMPLES	0/5
Z86E0208SECR516PTR	N149FR0AA	FRESH SAMPLES	0/5
Z86L8808SSCR51PX	BXH1505APB	500X TC	0/5
Z8937320ASC	B810WW8Q2	FRESH SAMPLES	0/5
Z9037116PSC	BYH101PS	FRESH SAMPLES	0/5
Z9037116PSC	MB546	500X TC	0/5
Z8702114SSCR4216TR	AZ201DG0RAC	FRESH SAMPLES	0/5
Z8702114SSCR4216TR	AZ151PU0RBP	FRESH SAMPLES	0/5
Z86E0812SSC1866	NZ150NP0A	FRESH SAMPLES	0/5
Z86C0812SSCR2433	AZ151RS0RPB	FRESH SAMPLES	0/5
Z86L0808SSCR5009	A151AR0RAPC	FRESH SAMPLES	0/5
Z86C3316PSCR4124	AYH1120AR	500X TC	0/5
Z84C0008PEC1983	A036FY0X1P	500X TC	0/5

Table 5-15. C-Mode Scanning Acoustic Microscope Monitor 2002
CMOS

Device Type	Lot No.	Sample Selection	Results
Z8018008FSC	Y132AB0Q	500X TC	0/5
Z86E0812SSC1866	NZ150NP0A	FRESH SAMPLES	0/5
Z9037116PSC	BYH1101PWE	FRESH SAMPLES	0/5
Z9037116PSC	BYH1101B	FRESH SAMPLES	0/5
Z9037116PSC	BYH149BPB	FRESH SAMPLES	0/5
Z8937320ASC	B810WW8Q2	FRESH SAMPLES	0/5
Z16C3010ASC	B124AT0P	FRESH SAMPLES	0/5
Z8937320ASC	B810WW8Q2	500X TC	0/5
Z9037116PSC	BYH1498QA	FRESH SAMPLES	0/5
Z9037116PSC	BYH1498QB	FRESH SAMPLES	0/5
Z86L990PZ008SCR51ML	BYHBHP1A	FRESH SAMPLES	0/5
Z9023406PSCR5140	BYH1786D	FRESH SAMPLES	0/5
Z8937320ASC	B810WW8Q2	1000X TC	0/5
Z86C3316PSCR4124	AYH1120AR	500X TC	0/5
Z86C0408PEC	A204EK0RRPPA	FRESH SAMPLES	0/5
Z86E136SZ016SC	AYH1736AASP	FRESH SAMPLES	0/5
Z84C9010VSC	EY205LU0Q	FRESH SAMPLES	0/5
Z86L8808SSCR51XF	EYHBHTH.0CP	FRESH SAMPLES	0/5
Z867331PSC	EY204JW0	FRESH SAMPLES	0/5
Z86L8808PSCR5101	EH0092A	FRESH SAMPLES	0/5
Z86L8108PSCR5101	EH0092B	FRESH SAMPLES	0/5
Z86E136SZ016SC	NYH1736AATA	FRESH SAMPLES	0/5
Z86E136SZ016SC	NYH1736AAT	FRESH SAMPLES	0/5
Z8937320ASC	K810WW8QA	FRESH SAMPLES	0/5
Z8937320ASC	K810WW8Q1	FRESH SAMPLES	0/5
Z8937320ASC	K810WW8Q1	500X TC	0/5
Z8E00110HSCR508F	B1091S0S	FRESH SAMPLES	0/5
Z85C3008VSC	B038GN0QA	FRESH SAMPLES	0/5
Z85C3008VSC	B038GN0QB	FRESH SAMPLES	0/5
Z84C0008FEC	BY206BJ0B	FRESH SAMPLES	0/5
Z85C3008VSC	B038GN0QA	500X TC	0/5
Z85C3008VSC	B038GN0QB	500X TC	0/5
Z9037116PSC	BYH1498SA	FRESH SAMPLES	0/5
Z9023406PSCR5140	BYH1786D	FRESH SAMPLES	0/5
Z86C0408PECR2981	A204EK0RRPPA	1000X TC	0/5
Z86E136SZ016SC	AYH1736AASP	500X TC	0/5
Z84C0008PEC1983	A036FY0Y1P	500X TC	0/5
Z86C3316PSCR4124	AYH1120AR	1000X TC	0/5
Z84C9010VSC	EY205LU0Q	1000X TC	0/5
Z86L8808SSCR51XF	EYHBHTH.0CP	1000X TC	0/5
Z86E136SZ016SC	NYH1736AAT	500X TC	0/5
Z86E136SZ016SC	NYH1736AATA	500X TC	0/5
Z8937320ASC	KY916JZ0A	FRESH SAMPLES	0/5
Z8937320ASC	KY916JZ0C	FRESH SAMPLES	0/5
Z9037116PSC	BYH1498TG	FRESH SAMPLES	0/5
Z9037116PSC	BYH1498UA	FRESH SAMPLES	0/5
Z16C0110PSC	B9S0JY0	FRESH SAMPLES	0/5
Z85C3008VSC	B0386N00Q	FRESH SAMPLES	0/5

Table 5-15. C-Mode Scanning Acoustic Microscope Monitor 2002
CMOS

Device Type	*Lot No.*	*Sample Selection*	*Results*
Z9023406PSCR5140	BYH1786	1000X TC	0/5
Z84C0008FEC	BY206BJ0B	1000X TC	0/5
Z9037116PSC	BYH1498S0	FRESH SAMPLES	0/5
Z9037116PSC	BYH1498SN	FRESH SAMPLES	0/5
Z9035612PSCR3720	BYH1722A	1000X TC	0/5
Z85C3008VSC	B0386N0QA	1000X TC	0/5
Z85C3008VSC	B0386N0QB	1000X TC	0/5
Z16C3010VSC00TR	B217S0A	FRESH SAMPLES	0/5
Z16C3010VSC00TR	B219TU0	FRESH SAMPLES	0/5
Z86L8808PSCR521A	BZHCNSW.00U	FRESH SAMPLES	0/5
Z9023406PSCR51X3	EYHB032	500X TC	0/5
Z9023406PSCR51X3	EYHB032	1000X TC	0/5
Z8673312PSC	0EY204JW03	1000X TC	0/5
Z8937320ASC	KY916JZ0C	3X REFLOW	0/5
Z16C0110PSC	K930FX0	FRESH SAMPLES	0/5
Z84C9010VSC	K207HR0AP	FRESH SAMPLES	0/5
Z8937320ASC	K813TY8	500X TC	0/5
Z8S18020VSC	K207XX0A	400X TC	0/5
Z85C3008PSC	K041HJ0S	FRESH SAMPLES	0/5
Z9037116PSC	BYH1498AH	FRESH SAMPLES	0/5
Z9037116PSC	BYH1498PD	FRESH SAMPLES	0/5
Z9037116PSC	BYH1498AC	FRESH SAMPLES	0/5
Z16C0110PSC	B9S0JY0	500X TC	0/5
Z8702414SSCR51XK	BHBT78.04B	1000X TC	0/5
Z8702414SSCR51XK	CHBT77	1000X TC	0/5
Z16C3010VSC00TR	B219TU0	FRESH SAMPLES	0/5
Z16C3010VSC00TR	B217S0A	FRESH SAMPLES	0/5
Z86L8808PSCR2607	BYHB625.EHA	FRESH SAMPLES	0/5
Z86L8808PSCR5121	BZHCNTA.04T	FRESH SAMPLES	0/5
Z86E126PZ016EC	AG0797EX	FRESH SAMPLES	0/5
Z16C0110PSC	K930FX0	500X TC	0/5
Z85C3008PSC	K041HJ0S	500X TC	0/5
Z84C9010VSC	K207HR0AP	500X TC	0/5
Z86C0208PSCR4502	K207HR0AP	1000X TC	0/5
EZ80L92AZ020SC	KYMB54GC	300X TC	0/5
Z86C3316VSCR4591	KE2080Q	FRESH SAMPLES	0/5
Z84C3006PEC	K210GW0CA	FRESH SAMPLES	0/5
Z86L8808PSCR521A	KZHCNYS.00G	FRESH SAMPLES	0/5
Z86L8808PSCR51JW	KZHCNTM.0ZE	FRESH SAMPLES	0/5
Z86L8808PSCR51JW	KZHCP26.0ML	FRESH SAMPLES	0/5
Z86L8808PSCR51JW	KZHCP26.0ME	FRESH SAMPLES	0/5
Z86L8808PSCR51JW	KZHCP26.00P	FRESH SAMPLES	0/5
Z86C9533ASC	KYH1769AB	FRESH SAMPLES	0/5
Z86L8808PSCR521A	KZHCNYS.0KB	FRESH SAMPLES	0/5
Z86E136PZ016SC	KH1747AABPAC	FRESH SAMPLES	0/5
Z84C3010PEC	K213AY0AP	FRESH SAMPLES	0/5
Z86L1608PSCR2565	K136BB0A	FRESH SAMPLES	0/5
Z86E0612PSC	K117DJ0S	FRESH SAMPLES	0/5

Table 5-15. C-Mode Scanning Acoustic Microscope Monitor 2002
CMOS

Device Type	Lot No.	Sample Selection	Results
Z86L8808PSCR521A	KZHCNYS.00T	FRESH SAMPLES	0/5
Z86L8808PSCR521A	KZHCNYS.00B	FRESH SAMPLES	0/5
Z8937320ASC	K816FP0	FRESH SAMPLES	0/5
Z86C3312PECR2035	K210BX0	FRESH SAMPLES	0/5
Z86E136PZ016SC	KH1736AATA	FRESH SAMPLES	0/5
Z86L8808PSCR2607	KZH1772BC	FRESH SAMPLES	0/5
Z86L8808PSCR2607	KZH1772BA	FRESH SAMPLES	0/5
Z86E3016PSC	KZ210GS0AAB	FRESH SAMPLES	0/5
Z86C6516PSCR50CH	NG0060A	FRESH SAMPLES	0/5
Z86L8808PSCR51JW	NZHCNST.0PB	FRESH SAMPLES	0/5
Z86L0808SSCR5009	NZ215ABAAA	FRESH SAMPLES	0/5
Z86L0808SSCR5009	NZ215ABBAAB	FRESH SAMPLES	0/5
Z86L0808SSCR5009	NZ215AB0AB	FRESH SAMPLES	0/5
Z86L8808PSCR51JW	NZHCNST	FRESH SAMPLES	0/5
Z85C3008VSC	S042AE0R	FRESH SAMPLES	0/5
Z86L8808PSCR521A	KZHCNSY.00X	FRESH SAMPLES	2/15 DIE/MOLD INT

2H - 2002			
Z16C0110PSC	B9S0TY0	1000X TC	0/5
Z8018008VSC00TR	BZ221XX0B	300X TC	0/5
Z8E0010HSCR508F	B019LS0S	1000X TC	0/5
Z86K1505PSC4530	A220EZ0PAA	FRESH	0/15
Z86K1505PSC4530	A220EZ0PC	FRESH	0/15
Z9010204PSCR3855	A219GG0PB	FRESH	0/15
Z86C6516PSCR3918	A2170G0PA	FRESH	0/15
Z86E126PZ016EC	AG0797EX	500X TC	0/5
Z86E3016VSC	AZ219JP0AP	FRESH	0/15
Z8523016VSC00TR	AZ215EK0AQ	FRESH	0/15
Z86E126PZ016EC	AG079EX	1000X TC	0/15
Z86L8808PSCR51JW	KXHCP2K.02A	FRESH	0/15
Z86C3312PECR529J	K219JU0A	FRESH	0/15
Z86C3312PECR529J	K219JU0B	FRESH	0/15
Z86C0208PSCR4448	KZ218PR0PAA	FRESH	0/15
Z98622812PSC	K220GT0AAB	FRESH	0/15
Z98622812PSC	K220GT0AAA	FRESH	0/15
Z84C3006PEC	K219SZ0PB	FRESH	0/15
Z84C3006PEC	K219SZ0PA	FRESH	0/15
Z86C0412PSCR51M6	KZ219HP0A	FRESH	0/15
Z86L0208PSCR4241	K219KY0D	FRESH	0/15
Z86C0408PECR2981	KZ219HL0D	FRESH	0/15
Z86C0408PECR2981	KZ219HL0C	FRESH	0/15
Z8623312PEC2035	K220CF0A	FRESH	0/15
Z86E136PZ016SC	KH1721AAR	FRESH	0/15
EZ80L92AZ020SC	KYMB54GC	100X TC	0/5
Z8623312PECR52F5	KZ220AY0AA3	FRESH	0/15
Z8623312PECR52F5	KZ220AY0AAA	FRESH	0/15

Table 5-15. C-Mode Scanning Acoustic Microscope Monitor 2002
CMOS

Device Type	*Lot No.*	*Sample Selection*	*Results*
Z86K1505PSCR4243	KZ28FF0A	FRESH	0/15
Z8623312PECR52F5	KZ220AY0AB	FRESH	0/15
Z86C3312PECR2035	K220CF0AB	FRESH	0/15
Z86C3312PECR2035	K220CF0AC	FRESH	0/15
Z86C3312PSCR2130	K220C00AP	FRESH	0/15
Z86C3312PSCR2035	K220CF0AA	FRESH	0/15
Z86C3316VSCR4591	KE2080Q	500X TC	0/5
Z86C3012PECR3495	KZ214BZ0BB	FRESH	0/15
Z16C0110PSC	K930FX0	1000X TC	0/5
Z84C9010VSC	K207HP0AP	1000X TC	0/5
EZ80L92AZ020SC	KYMB54GC	500X TC	0/5
Z8623312VSCR4591	KE2080Q	1000X TC	0/5
Z86E3116PSC	KZ210GT0AAQ	FRESH	0/15
Z86C6516PSCR507F	N219EU0AA	FRESH	0/15
Z86C6516PSCR3918	N212CT0	FRESH	0/15
Z86C6516PSCR3918	NY211LP0A	FRESH	0/15
Z86L8808PSCR51JW	NZHCPK0.00P	FRESH	0/5
Z86C6516PSCR3918	N214DH0	FRESH	0/15
Z86C6516PSCR3918	N211LR0A	FRESH	0/15
Z86L8808PSCR51JW	NZHCPK0.00A	FRESH	0/15
Z86L8808PSCR4455	NZHCPJS.00E	FRESH	0/15
Z86L8808PSCR4455	NZHCPJS.00Q	FRESH	0/15
Z86L8808PSCR4455	NZHCPJS.00L	FRESH	0/15
Z86L8808PSCR4455	NZHCPJS.00N	FRESH	0/15
Z86L8808PSCR4455	NZHCPJS.00G	FRESH	0/15
Z86L8808PSCR4455	NZHCPJS.00R	FRESH	0/15
Z16C3010VSC	B223BB0P	FRESH	0/15
Z16C3010VEC00TR	B136CU0P	FRESH S	0/15
Z8018008VSC00TR	BZ221XX0B	1000X TC	0/5
Z16C3010VSC00TR	B223BB0	FRESH	0/15
Z9023106PSC	B213AW0Q	FRESH	0/15
Z9023106PSC	B213AT0B	FRESH	0/15
Z9023106PSC	B213AX0C	FRESH	0/15
Z9023106PSC	B213106PSC	FRESH	0/15
Z9023106PSC	B213AT0A	FRESH	0/15
Z9023406PSCR51J1	BHF0F3.05D	FRESH	0/15
Z9023406PSCR522F	BHF0F3.00PB	FRESH	0/15
Z86L8808PSCR4455	BZHCW79.2BC	FRESH	0/15
Z86L8808PSCR4455	BZHCW79.28B	FRESH	0/15
Z86L8808PSCR4455	BZHCW79.02C	FRESH	0/15
Z86L8808PSCR4455	BZHCW79.2BA	FRESH	0/15
Z16C3010VEC00TR	A224CX0Q	FRESH	0/15
Z84C1510AEC	AZ220FT0P	FRESH	0/5
Z8F6403FZ020SC	AR60986	100X TC	0/5
Z16C3010VSC	A224CZ0PX	FRESH	0/15

Table 5-15. C-Mode Scanning Acoustic Microscope Monitor 2002
CMOS

Device Type	*Lot No.*	*Sample Selection*	*Results*
Z16C3010VSC	A224CY0X	FRESH	0/15
Z8523016VSC00TR	A219TT0PAP	FRESH	0/15
EZ80L92AZ020SC	KYMB54GC	1000X TC	0/5
Z8623312PECR503X	KZ222ET0	FRESH	0/15
Z8623312PECR503X	KZ222EP0	FRESH	0/15
Z88C0020PSC	K220EH0A	FRESH	0/15
Z86E136PZ016SC	KH1577AE	FRESH	0/15
Z86C3312PECR2035	K224NZ0A	FRESH	0/15
Z86E136PZ016SC	KH1577AB	FRESH	0/15
Z84C3006PEC	K223EK0	FRESH	0/15
Z86E136PZ016SC	KH1577AF	FRESH	0/15
Z84C3006FEC	K208EF0BA	FRESH	0/15
Z84C3006FEC	K22ACT0AP	FRESH	0/15
Z86C3108PECR3519	KZ224WY0AP	FRESH	0/15
Z86E136PZ016SC	KH1577AC	FRESH	0/15
Z86E3016PSC	KZ221CZ0B	FRESH	0/15
Z84C0006PEC1527	KZ222TT0U	FRESH	0/15
Z86L8808PSCR51JW	KZHCNL0.0AA	FRESH	0/15
Z86C6516PSCR50CH	NG0060A	500X TC	0/15
Z86L98HZ008SCR526R	SHCNQ5.01RA	FRESH	0/15
Z86L98HZ008SCR526R	SHCNQ5.01RA	PKG INT	0/15
Z86L8808SSCR50HWTR	SZHCQ47.00B	FRESH	0/15
Z86L8808PSCR51JW	BZHCWY7.02E	FRESH	0/15
Z86L8808PSCR521A	BZHCW7C.1PD	FRESH	0/15
Z9023306PSCR5159	BHF0F3.063	FRESH	0/15
Z9023406PSCR51J1	BHF0F3.05D	FRESH	0/15
Z9023406PSCR522F	BHF0F3.00PB	FRESH	0/15
Z86L8808PSCR4455	BZHCW79.2BC	FRESH	0/15
Z86L8808PSCR4455	BZHCW79.28B	FRESH	0/15
Z8621912SSC	A224DL0AP	500X TC	0/15
Z86L8808SSCR4590	AR60986.1	FRESH	0/5
Z8702414SSCR52CH	AZHF11.132A	100X TC	0/5
Z16C3010VSC	A224CZ0PX	FRESH	0/15
Z16C3010VSC	A224CY0X	FRESH	0/15
Z8523016VSC00TR	A219TT0PAP	FRESH	0/15
Z8018233ASC1932	AH0657SB	FRESH	0/15
Z8621912SSC	A224DL0AP	1000X TC	0/15
EZ80F92AZ020SC	KR61001.A2	500X TC	0/5
Z86C6516PSCR50CH	NG0060A	500X TC	0/15
Z86L98HZ008SCR526R	SHCNQ5.01RA	500X TC	0/15
Z86D991SZ008SC2046	SY206HH0BAP	500X TC	0/15
Z9023406PSCR51KC	BHF2P0.00AA	FRESH	0/15
Z86L8808PSCR51JW	BZHF03W.05B	FRESH	0/15
Z86L8808PSCR51JW	BZHF03W.05A	FRESH	0/15
Z86L8808PSCR51JW	BHCY0Q.00AA	FRESH	0/15

Table 5-15. C-Mode Scanning Acoustic Microscope Monitor 2002
CMOS

Device Type	Lot No.	Sample Selection	Results
Z86L8808PSCR51JW	BZHF03W.05E	FRESH	0/15
Z86L8808PSCR51JW	BZHF035.0PA	FRESH	0/15
Z8641708BSCR3212	BYH1665B	FRESH	0/15
Z86L8808PSCR51JW	BZHF035.0PF	FRESH	0/15
Z86L8808PSCR51JW	BZHF035.0QE	FRESH	0/15
Z86L8808PSCR51JW	BZHF035.0PB	FRESH	0/15
Z9025106PSC	B230EK0A	FRESH	0/15
Z16C3010VSC00TR	BZ233FT0	FRESH	0/15
Z16C3010VSC00TR	BZ233FS0A	FRESH	0/15
Z16C3010VSC00TR	BZ233FS0AP	FRESH	0/15
Z16C3010VSC00TR	BZ233HK0	FRESH	0/15
Z16C3010VSC00TR	BZ234AJ0AP	FRESH	0/15
Z9023406PSC	BHF343.00F	FRESH	0/15
Z86L8808PSCR51JW	BZHF035.00D	FRESH	0/15
Z86L8808PSCR51JW	BZHF035.00C	FRESH	0/15
Z86L8808PSCR51JW	BZHF035.00F	FRESH	0/15
Z86L8808PSCR51JW	BZHF035.0PL	FRESH	0/15
Z86L8808PSCR51JW	BZHF035.0QJ	FRESH	0/15
Z86L8808PSCR51JW	BZHF035.0PJ	FRESH	0/15
Z86L8808PSCR51JW	BZHF035.00E	FRESH	0/15
Z9023406PSCR51KC	BHF343.00B	FRESH	0/15
Z86L8808PSCR51JW	BZHF03R.00B	FRESH	0/15
Z8PE003HZ010SC	B219FP0	1000X TC	0/15
Z86L8808SSCR4590	AZHCY3W.00B	FRESH	0/15
Z8F6403FZ020SC	AR60986.1	FRESH	0/15
Z86L8808SSCR52M8	AZHCY3Y.7PB	FRESH	0/15
Z86L8808SSCR4590	AZHCY3W.00D	FRESH	0/15
Z86L8808SSCRR5086TR	AZHF03W.2PB	FRESH	0/15
Z8018233ASC1932	AH0657SB	FRESH	0/15
Z86L8808SSCR52C7	AZHCY2Y.9PA	FRESH	0/15
Z8621912SSC	A224DL0AP	500X TC	0/15
Z86L8808SSCR50HWTR	AZHCY0N.0PI	FRESH	0/15
Z8702414SSCR52CH	AZHF11.132A	500X TC	0/15
Z96L8808SSCR52FN	AZHF096.008	FRESH	0/15
Z8621912SSC	A224DL0AP	1000X TC	0/15
Z90255066PSCR51K9	BHF42J00PA	FRESH	0/15
Z90255066PSCR51K9	BH42J00PG	FRESH	0/15
Z90255066PSCR51K9	BHW55.00B	FRESH	0/15
Z90255066PSCR51K9	BH42J.00PB	FRESH	0/15
Z90255066PSCR51K9	BH42J.00PI	FRESH	0/15
Z90255066PSCR51K9	BH42J.00PD	FRESH	0/15
Z9023406PSCR51J1	BHCWF8.02DA	1000X TC	0/15
Z90255066PSCR51K9	BHF42J.00PC	FRESH	0/15
Z9023406PSCR522F	BHFM15.00E	FRESH	0/15
Z9023406PSCR522F	BHFM15.00E	FRESH	0/15

Table 5-15. C-Mode Scanning Acoustic Microscope Monitor 2002
CMOS

Device Type	Lot No.	Sample Selection	Results
Z86L8808PSCR51JW	BZHF29N.01E	FRESH	0/15
Z86L8808PSCR51JW	BZHF29N.01D	FRESH	0/15
Z9025506PSCR5288	BH0Q3Q.02AB	FRESH	0/15
Z9025506PSCR5288	BHCQ3Q.02A	FRESH	0/15
Z8641708BSCR3212	BYH1665B	500X TC	0/15
Z86C3312PSCR2130	B220CD0AAA	FRESH	0/15
Z86L8808PSCR51JW	BZHF26W.0P1	FRESH	0/15
Z86L8808PSCR51JW	BZHF26W.0QG	FRESH	0/15
Z86L8808PSCR51JW	BZHF26W.0PH	FRESH	0/15
Z9025506PSCR52LX	BHF3G2.00DB	FRESH	0/15
Z9023406PSCR51KC	BHF3QP.02PA	FRESH	0/15
Z9023406PSCR51KC	BHF3QP.02PC	FRESH	0/15
Z9023406PSCR51KC	BHF343.00AC	FRESH	0/15
Z9023406PSCR51KC	BHF3G2.00DC	FRESH	0/15
Z86L8808PSCR51JW	BZHF26.0PA	FRESH	0/15
Z8621912SSC	A224DL0AP	100X TC	0/15
Z86L8808SSCR50HWTR	AZHCY0N.0PH	FRESH	0/15
Z86L8808SSCR50HWTR	AZHCY0N.00C	FRESH	0/15
Z86L8808SSCR50HWTR	AZHCY0N.PEB	FRESH	0/15
Z86L8808SSCR50HWTR	AZHCY0N.00B	FRESH	0/15
Z86L8808SSCR50HWTR	AZHCY0N.00D	FRESH	0/15
Z86L8808SSCR52MC	AZHF29S.01A	FRESH	0/15
Z8018233ASC1932	AH0G57SB	FRESH	0/15
Z8S18010VSC	A222FN0AQ	FRESH	0/15
Z8018233ASC1932	AH0G57SB	500X TC	0/15
Z8S18010VSC	A222FN0AQ	500X TC	0/15
Z86L8808SSCR50HWTR	NZHF03T.0BC	FRESH	0/15
Z86L8808SSCR50HWTR	NZHF2CF.0AC	FRESH	0/15
Z86L8808SSCR50HWTR	NZHF2CF.0AK	FRESH	0/15
Z86L8808SSCR50HWTR	NZHF2CF.08K	FRESH	0/15
Z86L8808SSCR50HWTR	NZHF2CF.0AL	FRESH	0/15
Z86L8808SSCR50HWTR	NZHF2CF.0BI	FRESH	0/15
Z86L8808SSCR50HWTR	NZHF2CF.0AM	FRESH	0/15
Z86L8808SSCR50HWTR	NZHF2CF.0BH	FRESH	0/15
Z86L8808SSCR519P	NZHF295.4PA	FRESH	0/15
Z86L8808SSCR50HWTR	NZHF03T.0BE	FRESH	0/15
Z86C3312PECR517F	NY214GN0P	500X TC	0/15
Z86L8808SSCR50HWTR	NZHF29S.06P	FRESH	0/15
Z86L8808SSCR4470TR	NZHF29S.06P	FRESH	0/15
Z86L8808SSCR4470TR	NZHF29Q.02	FRESH	0/15
Z86L8808SSCR4590	NZHF29Q.1PE	FRESH	0/15
Z86L8808SSCR4590	NZHF29Q.1PG	FRESH	0/15
Z86L8808SSCR52FN	NZHF29S.05	FRESH	0/15
Z86D991SZ008SC2046	SY206HH0BAP	1000X TC	0/15
Z86L8808SSCR4590	SZHF29N.02P	FRESH	0/15

Table 5-15. C-Mode Scanning Acoustic Microscope Monitor 2002 CMOS

Device Type	Lot No.	Sample Selection	Results
Z86L8808PSCR51JW	KZHCNL0.00C	1000X TC	0/15
Z84C0006PEC	KZ219KN0P	500X TC	0/15
EZ80F92AZ020SC2047	KR61001.A2	1000X TC	0/15
Z8019520FSC	K232CN0A	500X TC	0/15
Z86L8808PSCR51JW	KZHF29N.01P	FRESH	0/15
Z9023306PSCR51J9	BH343.06PC	FRESH	0/15
Z8S18020VEC	B222RR0AP	FRESH	0/15
Z8S18020VEC	B222FR0BA	FRESH	0/15
Z86L8808PSCR51JW	BZHFR26W.00D	FRESH	0/15
Z86L8808PSCR521A	BZHF2CH.1PB	FRESH	0/15
Z86L8108SSCR52HTR	BZHCN3A.05B	FRESH	0/15
Z8641708BSCR3212	BYH1665B	1000X TC	0/15
Z86L8108PSCR5101	BZHCN0D.1PB	FRESH	0/15
Z8018233ASC1932	AH06575B	1000X TC	0/15
Z86L8808SSCR52FN	AZHF29R.0PF	FRESH	0/15
Z86L8108SSCR528HTR	AZHCN3A.05A	FRESH	0/15
Z86L8108PSCR5101	AZHCN00.01P	FRESH	0/15
Z86L8808SSCR50HWTR	NZHF2CG.01D	FRESH	0/15
Z84C0006PEC	KZ219KN0P	1000X TC	0/15
Z8019520FSC	K232CN0A	500X TC	0/15
Z86L8808PSCR521A	KZHF2CH.01C	FRESH	0/15
Z86L8808PSCR521A	KZHF2CH.01B	FRESH	0/15
Z0221524VSCR51JA	KA227EU8AB	500X TC	0/15
Z8019520FSC	K232CN0A	1000X TC	0/15

Table 5-16. C-Mode Scanning Acoustic Microscope Monitor 2002 NMOS

Device Type	Lot No.	Sample Selection	Results
1H - 2002			
Z0843006PSC	K037JX0T	FRESH SAMPLES	0/5
Z0220112VSCR4078TR	K139AX0R	1000X TC	0/5
Z0843004PSC	K037JX0T	500X TC	0/5
2H - 2002			
Z0853606VSC	B205AP0A	1000X TC	0/15
Z0853606VSC	B205AP0A	500X TC	0/15
Z084C3006PSC	K037JX0T	1000X TC	0/5

CHAPTER 5

Assembly and Test

Package types:

8 / 18 / 20 / 22 / 28 / 40 / 48	Plastic Dual In-line Package (PDIP)
42 / 52 / 64	Shrink Dual In-line Package (SDIP)
28 / 44 / 68 / 84	Plastic-Leaded Chip Carrier (PLCC)
44 / 80 / 100 / 132/ 144 / 208	Quad Flat Pack (QFP)
44 / 64 / 100 / 144 / 160	Very Small Quad Flat Pack (VQFP)
64	Thin Quad Flat Pack (TQFP)
18 / 20 / 28	Small Outline Integrated Circuit (SOIC)
20 / 28 / 48	Shrink Small Outline Package (SSOP)

Technology Data:

Die attach (method/composition)	Oven cure/silver filled epoxy
Wirebond (type/material)	Ball bond, thermosonic/gold to aluminum Crescent bond, thermosonic/gold to silver plated frame
Bonding wires (material/diameter)	Gold 1.0 / 1.3 mil
Package seal	Transfer epoxy molding
Lead and lead finish	Solder plate
Leadframe material/plating	Copper (A151) / Ag spot plate for PLCC Copper (A194)/Ag spot plate for PDIP, SDIP, SOIC and SSOP Copper (A7025)/Ag spot plate for QFP and VQFP
Leadframe plating thickness	Ag spot is 150-400 microinches
Moisture Sensitivity Level for Surface Mount Devices	PLCC, QFP, LQFP & TQFP: MSL = 3, Floor Life = 168 hrs. @ 30°C/60% RH

Pre/Post Packaging Device Test Procedures:

Wafer probe at 70ºC; final test at 70ºC;   Wafer probe tests guardband final test

Number/Type of Testers	**Sentry 15/20/21, Megatest, ITS9000, SZ**
Provision for Testing at Speed	Yes
Provision of high temp testing	Environmental handlers
Provisions for tape and reel shipment of SMT devices	Yes
Provisions for tray shipment of QFP devices	Yes

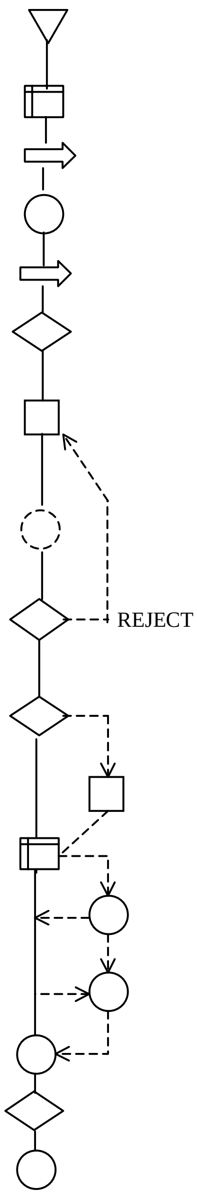
ATTACHMENT 1

Legend:

- Material — Bank
- Transport — QC acceptance
- Process — Inspection/Test

PLASTICS PROCESS FLOW

Flow



Process/Item	***Document***
Wafer	
Die Bank	SOM-040
Pack/transport to Subcon	SOM-005
Subcon Assembly	
Pack/transport ZEPI	SOM-005
Incoming Inspection of Subcontract ZilOG Products	QCM-235
Electrical Test	TSM-021
<For Stress Test D Flow only> Burn-In (48hrs or as specified on PSI)/ 100% Electrical Test at Room	TSM-012/ TSM-021
Electrical Test Gate	QCM-108
QC Outgoing & Shipping Gate (see note 1)	QCM-126
Final Visual Inspection (For visual reject)	MAM-235
Finished Goods	SOM-171
Bake Out (for VQFP/QFP/TQFP)	MAM-212
Tape & Reel (as required per PSI)	MAM-236
Pack	MAM-067
Shipping Audit	QCM-301
Ship	QCM-301

ATTACHMENT 2

PLASTIC-STANDARD ASSEMBLY/TEST PROCESS

PLASTIC – STANDARD (C FLOW)
• DIE BANK
• WAFER SAW
• EPOXY DIE ATTACH
• WIREBOND
• MOLD
• STRIPMARK
• SOLDER PLATE
• BAKEOUT (FOR PLCC)
• TRIM/FORM
• 100% ELECTRICAL TEST – HOT AND QC SAMPLE ELECTRICAL AT 25ºC
• QC PRESHIP INSPECTION
• BAKEOUT FOR QFP/VQFP INT RAY
• TAPE AND REEL (OPTIONAL FOR SOIC, QFP AND PLCC)
• PACK

PLASTIC – STRESSED (D FLOW)
• DIE BANK
• WAFER SAW
• EPOXY DIE ATTACH
• WIREBOND
• MOLD
• STRIPMARK
• SOLDER PLATE
• BAKEOUT (FOR PLCC)
• TRIM/FORM
• 100% ELECTRICAL TEST – HOT
• BURN-IN 48 HOURS AT 125ºC
• 100% ELECTRICAL TEST AT ROOM
• QC PRESHIP INSPECTION
• BAKEOUT FOR QFP/VQFP IN TRAY
• TAPE AND REEL (OPTIONAL FOR PLCC, QFP, SOIC)
• PACK

ATTACHMENT 3
GENERAL MATERIAL SPECIFICATION

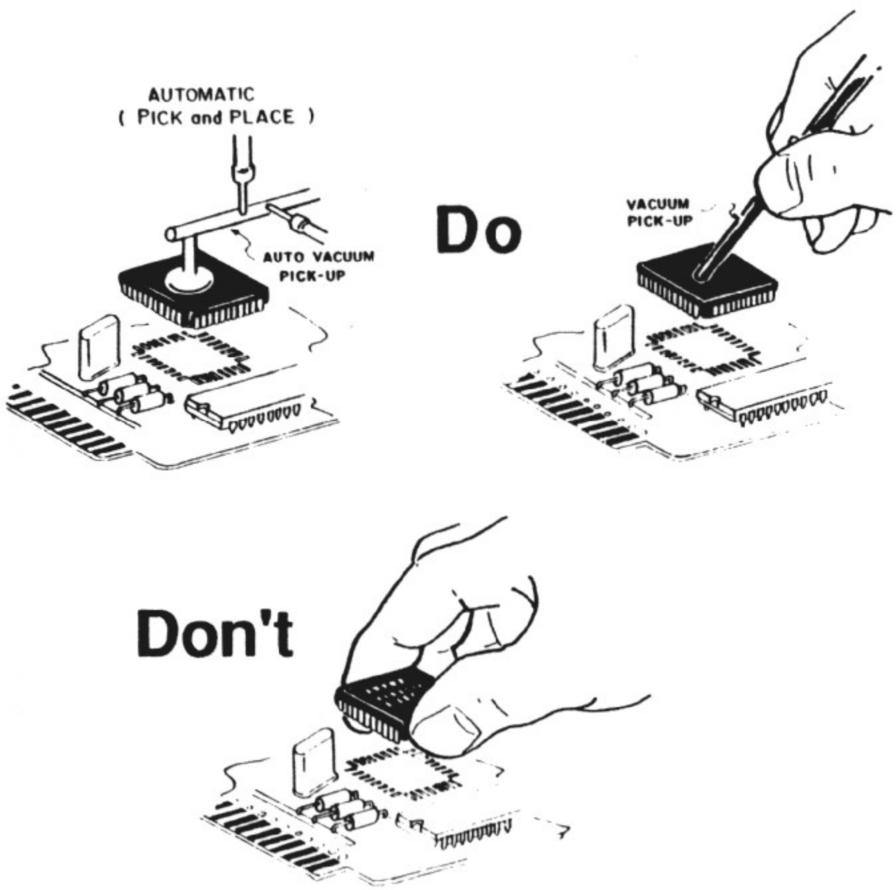
MATERIAL	*DIE ATTACH EPOXY*	*WIRE SIZE*	*MOLD COMPOUND*	*MARKING*	*PLATING*
PDIP	Silver Filled Epoxy	1.0 - 1.3 mil Au	EME6300H / HJ / RQ	Laser / Padmark	85/15 Tin Lead
	EN4065D		EME6600CS		
	84-1 LMIS		EME6600		
	84-1 LMISR4		CEL4630 SXT / SX		
	CRM 1033B		CEL 4600P8/P8T		
	8390A				
SDIP - REGULAR	Silver Filled Epoxy	1.0 - 1.3 mil Au	EME6300H /HJ /RQ	Laser / Padmark	85/15 Tin Lead
	EN4065D		CEL4660 SXT		
	84-1 LMIS		CEL4630 SXT / SX		
	84-1 LMISR4		EME6600CS		
	CRM1033B		CEL4600P8/P8T		
SDIP - MCM	Silver Filled Epoxy	1.2 mil Au	DONG JIN 200NF	Laser / Padmark	85/15 Tin Lead
	8390A				
PLCC	Silver Filled Epoxy	1.0 - 1.3 mil Au	EME6300H	Laser / Padmark	85/15 Tin Lead
	EN4065D		EME6600		
	84-1 LMISR4		EME6600CS		
	CRM 1033B		CEL 4630SX / SXT		
SOIC	Silver Filled Epoxy	1.0 - 1.3 mil Au	MP AN 8000 AN	Laser / Padmark	85/15 Tin Lead
	84-1 LMISR4		EME6300H		
	CRM1033D		EME6600CS		
	CRM1033B		EME6600		
			CEL4630SX / SXT		
SSOP	Silver Filled Epoxy	1.0 - 1.2 mil Au	MP AN 8000 AN	Laser/ Padmark	85/15 Tin Lead
	84-1 LMISR4				
EPTSSOP	Silver Filled Epoxy	1.2 mil Au	7050B	Laser / Padmark	85/15 Tin Lead
	8290				
QFP	Silver Filled Epoxy	1.0 - 1.3 mil Au	EME6300H / HJ	Laser / Padmark	85/15 Tin Lead
	84-1 LMISR4		EME6600CS		
	EN4065D		EME6600H		
	CRM 1033B		EME7320CR		
			CEL4630SXT		
TQFP/VQFP	Silver Filled Epoxy	1.0 - 1.3 mil Au	EME7320CR	Laser / Padmark	85/15 Tin Lead
	84-1 LMISR4				
	8360				
	CRM 1033B				

CHAPTER 6

The Handling and Storage of Surface Mount Devices

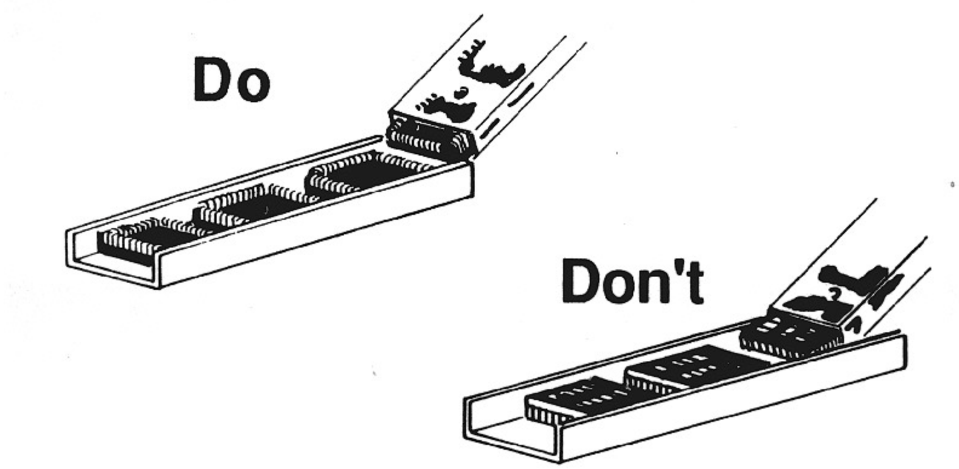
1. Handling

Components should be handled with vacuum pick to ensure that coplanarity of leads is maintained.



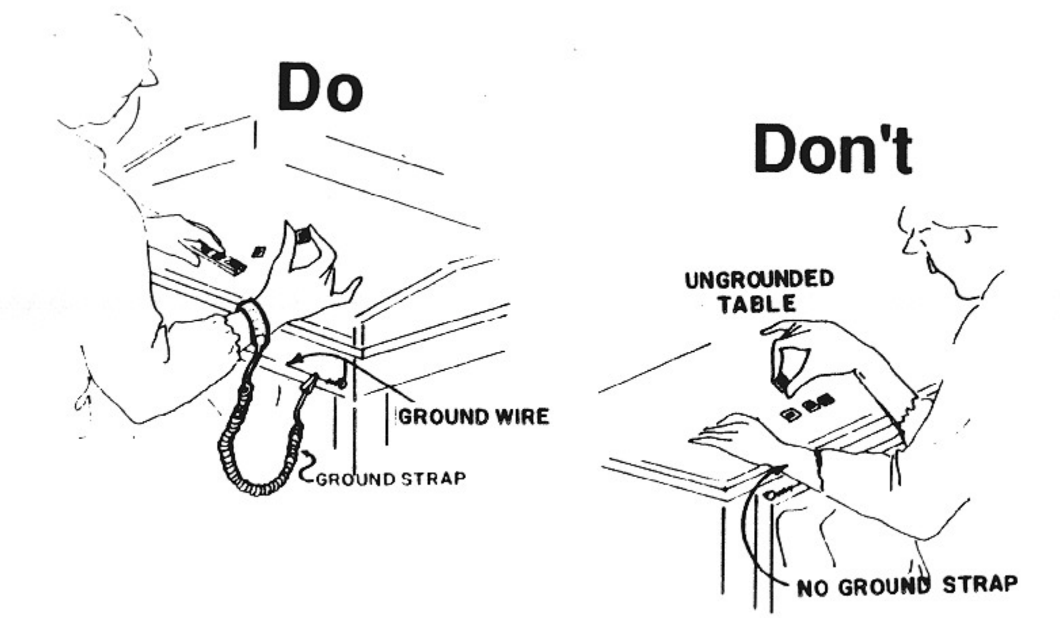
2. Lead Protection

Avoid sliding of units with leads in contact. The solder coating is prone to contamination/scraping. If sliding cannot be avoided, the contact surface should be clean and smooth.



3. ESD Protection

Observe ESD protection at all times. *These are static sensitive devices.*



4. Storage/Unpacking Caution

The plastic body of a surface mount product may be subjected to high temperatures during the printed circuit board assembly operation. Any moisture that may be present in the plastic may expand and damage the unit. Therefore, it is very important that the surface mount IC be dry before the printed circuit board operation begins.

ZiLOG assures that the unit is thoroughly dry before final packing for shipment. The units are shipped in a "dry pack" envelope designed to keep moisture away from the IC's. The user should carefully observe the following practices to assure that the units remain moisture free at the time of the printed circuit board soldering operation:

- Do not open the dry pack until you are ready to solder. Product may be exposed to ambient conditions of 30C/60%RH (or less) for no more than 168 hours. ***This corresponds to a moisture sensitivity level of 3.***
- Unopened dry packs may be stored at <40^{o}C/90% RH.
- When the dry pack must be opened for a short period of time (such as for incoming inspection) it should be resealed as soon as possible, ensuring that the desiccant remains inside the dry pack. Resealing should be done with heat seal for best closure of the bag.
- If the units have been exposed to more than 168 hours at ambient conditions of 30C/60%RH(or less) or if the humidity indicator card in the bag shows humidity above 20%, devices should be baked for 8 hours at 125^{o}C, before board soldering.

5. Soldering

Recommended surface mount profile is as follows:

- ☛ Maximum 3^{o}C/sec. ramp up.
- ☛ Maximum 220^{o}C peak temp.
- ☛ Minimum 1 min. cool down from peak temp. to 50^{o}C.

6. Desoldering

Parts removed due to board assembly problems or suspected failure.

If boxed-in type desoldering fixture is used, the following are recommended operating parameters:

- ☛ Package Temp: 220^{o}C max.
- ☛ Dwell Time: 1 min. max.

It is important that the above precautions are followed to ensure integrity of the packages.

CHAPTER 7

Quality Systems

QUALITY SYSTEMS

- Organization: Quality control departments are located at all plants

- Equipment: Nampa and Manila can conduct failed material analysis including decapsulation, SEM, microprobe, Emission microscope, X-Ray, EDX, cross-section and Sonoscan acoustic microscope. See Table 3-1 for a complete list of QC test equipment.

SUBCONTRACTING: 100% of assembly is subcontracted.

LOT TRACEABILITY: There is complete lot traceability by product date code back through the assembly process and wafer manufacturing process to the starting material.

AVAILABILITY OF DOCUMENTATION ON MONITORING: Documents are available in either hard copy or electronic form (SOP0937).

QUALITY DATA:

- Data availability: Outgoing quality is measured by the quality control acceptance/rejection data and on each production lot which is reported on a PPM basis. In addition, ZiLOG cooperates with certain customers who provide their incoming inspection data on a PPM basis for correlation, per Procedures SOP0903 and SOP0927.

- Mechanism of transfer: Hard copy/electronic

- Details/attributes provided: PPM

- Method of calculation: See Procedure SOP0927

- Current levels (by family/technology/package) per attribute: 30 PPM on mature products (mature products defined as those which have transited the initial startup experience curve). PPM detail is provided to the customer in ZiLOG's semi-annual quality and reliability report.

- Goals for next three to five years: ZiLOG desires to have all mature products at better than 20 PPM during this period.

TESTING (QA/Operating)

- Test program release procedure: ZiLOG has a formal test program review/release procedure, per Procedures SOP1239.

- Does QA sample test? Yes. Lots are sampled by QA using a statistically valid sampling plan. If the QA sample fails, the entire lot is re-tested and a second QA sample is drawn.

- Is datasheet tested or guaranteed? ZiLOG provides its product specifications to the customer in a document called a data sheet (SOP0302). The product specification describes the attributes that ZiLOG warrants.

- Is the product tested at full temperature range? Yes

- Is the product 100% electrically tested prior to QA? Yes

- Does QA pull samples for both AC and DC Testing? Yes

- How is propagation delay tested (e.g., simultaneous switching effect): Simultaneous

- Fault coverage (Operating vs. QA): As close to 100% as practical

- Coplanarity requirement on SMD: 4 mils maximum; reference the seating plane

- Define failure: Does not meet specifications

TEST TAPE SUPPORT: Test tapes, load boards and documentation are available

WHAT HAPPENS WHEN FAILURES OCCUR?

- Is sample truncated? No

- Corrective action plan: Plant sample failure analysis overviewed by HQ R/QA

- How is product segregated (i.e., is there protection from mixing)? Automatic binning during electrical test is used to segregate product. Product traceability to the customer order is maintained by a unique part numbering system (SOP0937 and SOP0902).

WHEN MANUFACTURING IS PERFORMED OFFSHORE, WHAT ARE THE CONTROLS?:
Same as onshore; the Manila plant is monitored through the Inventory Activity Yield (IAY) data collection system by the Director of Quality Assurance and Reliability on a contemporaneous basis, as is the Nampa plant. Reporting is continuous. Periodic audits are performed on all offshore facilities by ZiLOG personnel.

AVAILABILITY OF PROGRAMMING FACILITIES:
ZiLOG develops its own test programs with facilities located in Manila, Campbell and Nampa.

DOCUMENTATION CONTROL: (Include procedure for changes and updates.)
See Procedures SOP0922, SOP0901, and SOP0937. R/QA operates Document Control.

QA AUDIT:

- Availability of audit reports: Serialized run sheets and audit checklists are maintained by the Quality Control organization.

MATERIALS CONTROL: See Procedures SOP0811,SPOL025.

VENDOR OF THE YEAR AWARD:

ZiLOG has an aggressive commitment to the continuous improvement of the quality and reliability of our products. This concern affects not only material produced, but all materials and/or services procured by ZiLOG. Toward this end, ZiLOG has embarked on a program of ongoing vendor reviews at each site. These reviews culminate in a Vendor of the Year Award(s) from each site.

VENDOR OF THE YEAR

Year	***Winner***
2002	**Nampa, Idaho Site**
	Category 1 Silicon - LG Siltron
	Category 1 Raw Materials - Arch Chemicals
	Category 2 Raw Materials - Honeywell
	Freight Carriers - Air Van North American
	Contracted Services - Tri-State Electric

Year	***Winner***
2001	**Nampa, Idaho Site**
	Category 1 Silicon - LG Siltron
	Category 1 Raw Materials - Tosoh SMD
	Category 2 Raw Materials - Microsil
	Freight Carriers - Air Van North American
	Contracted Services - Tri-State Electric

Year	***Winner***
2000	**Nampa, Idaho Site**
	Category 1 Silicon - LG Siltron
	Category 2 Raw Materials - Microsil
	Logistics - Air Van North American

VENDOR OF THE YEAR
(Continued)

Year	*Winner*
	Nampa, Idaho Site
1998/1999	L.G. Electronics
1997	Photronic Labs, Inc.
1996	Astra Microtronics (AMT)
1995	Mitsubishi Silicon America
1994	Thesys GmbH
1993	Kawasaki Steel Corporation
1992	Schlumberger Technologies ATE Division
1991	OCG/Olin Hunt
1990	Sumitomo
1989	Photronic Labs, Inc.

CHAPTER 8

Statistical Process Control

STATISTICAL PROCESS CONTROL

SCOPE:

All major manufacturing processes are under SPC control Process stability and capability analyses are reported monthly.

A corporate-wide specification defines the scope of the program and provides detailed instructions for implementing SPC at an operation. It also defines the frequency of evaluation of control limits, training requirements, and responsibilities (SOP0918)

CONTROL CHARTS:

ZiLOG (Nampa) uses the 8-Point Zone Control Chart. The Zone Control Chart is easily adapted to nonstandard distributions. All Technicians are certified on the use of the Zone Control Chart. Control limits and out-of-control action plans are written into the process specifications. Control limits are changed as process improvements are implemented.

DESIGN OF EXPERIMENTS:

New processes require rigorous qualification through one or more Statistical Design of Experiments (SDE). Research is ongoing to improve the traditional SDE methodology.

CHAPTER 9

Document Control

DOCUMENT CONTROL SYSTEM

ZiLOG's Document Control Department promotes reliability and quality through efficient, global document management and revision control systems. The Document Control Department maintains an electronic document management system that is accessible by ZiLOG employees worldwide 24 hours a day. Manufacturing documents are available electronically for all wafer foundry and assembly subcontractors. The system automatically manages revision control; ensuring users have the most up-to-date version every time.

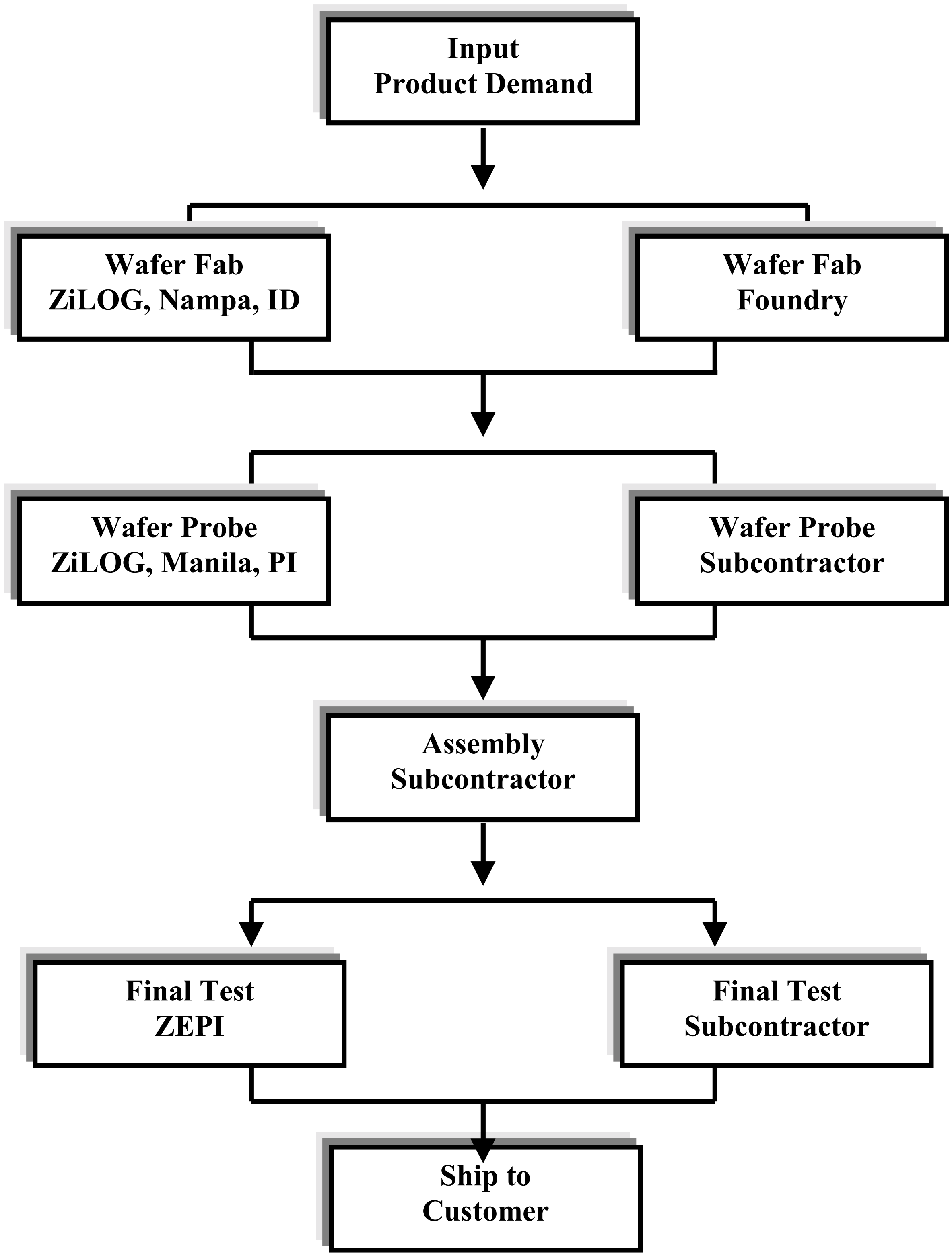
Corporate Document Control in Campbell, California, oversees the worldwide document management processes for revision controlled documents. They are also responsible for managing design, engineering and marketing documents and records as well as company-wide policies and procedures. Document Control departments in Nampa, Idaho, and Manila, Philippines, manage the manufacturing, assembly and test procedures and specifications.

Additional details regarding any of the sections contained in this document may be found in ZiLOG policies, procedures or specifications. General categories are listed below. Please contact the ZiLOG Director of Quality and Reliability with specific questions.

- Corporate-Wide Policies
- Standard Operating Procedures for Business Units, Corporate Communications, Finance, Human Resources, Information Technology, Legal, Operations, Reliability and QA, Sales, Strategy, Technology, Design & Test
- Core Process Documents for all Phases of the Product Life Cycle
- Product and Process Specific Manufacturing, Assembly and Test Procedures and Specifications

Document #	***Document Title***
POL025	Procurement Organization Roles And Responsibilities
POL003	Zilog Testing Policy
POL013	Tooling Revision Customer Qualification Policy
POL031	Manufacturing Management Fundamentals
QCC1425	CMOS D.C. Latch-Up Test Procedure
QCC1478	Electrostatic Discharge Procedure (Mil-Std)
SOP0302	Procedure For Administering A Technical Specification (CPS and/or DS)
SOP0811	Procedure For The Return of Purchased Material
SOP0817	Die and Wafer Procedure
SOP0901	Procedure For Submitting A Change Notice Form
SOP0902	Product Number Identity System
SOP0903	Quality And Reliability Program
SOP0906	EMC Testing Standards Procedure
SOP0908	Ship-To-Stock Procedure
SOP0913	Customer Notification Procedure
SOP0916	Fits Program Procedure
SOP0918	Statistical Process Control Procedure
SOP0922	Procedure For Creating Or Revising Policies Or Cross-Functional Procedures
SOP0923	Hast Testing Procedure
SOP0925	Military Group C And D Qualifications
SOP0927	PPM Measurement Program
SOP0932	Customer Order Reschedule And Cancellation Procedure
SOP0936	Product/Process Characterization Testing
SOP0937	Master Specification System Procedure
SOP1233	Procedure For Naming And Controlling Product Mask Step And Layer Revisions

ATTACHMENT 6



ATTACHMENT 7

SPC Fabrication
Typical Process

	Thickness	*Particulate*	*Thickness/ Uniformity*	*Critical Dimension*	*Concentration*	*Etch Rate*
Barrier Oxidation	X	-	-	-	-	-
Silicon Nitride Deposition	X	-	-	-	-	-
N-Well Mask	-	X	X	-	-	-
SDG Mask	-	X	X	X	-	-
P Field Implant	X	X	X	-	-	-
Poly Mask	-	X	X	X	-	-
S/D Implant Mask	-	X	X	-	-	-
Source Drain Reoxidation	X	-	X	-	X	-
Contact Mask	-	X	X	-	-	X
Metal-I Mask	-	X	X	X	-	-
Spin on Glass	-	-	-	-	-	X
Final Inspect	X	-	-	-	-	-
Via Mask	-	X	X	X	-	X
Metal II Mask	-	X	X	X	-	-
Pad Mask	-	-	X	-	-	-
Pad Mask Pix	-	-	X	-	-	-

CHAPTER 10

Thermal Properties

THERMAL CHARACTERISTICS

Calculation of Device Junction Temperature

Failure rates and Failures in Time (FITS) obtained from life test data are based on ambient temperatures (TA), and are not corrected to junction temperature (TJ). However, when a significant difference between TA and TJ exists, TJ can be incorporated into the Arrhenius Equation for accelerated failure rates by using the following equations:

Junction Temp. (T_J): $T_J = (\theta_{JA})\ (P_D) + T_A$

where: θ_{JA} is the thermal resistance of junction with respect to ambient (C/W). P_D is the maximum power dissipation at T_A in watts

and: T_A is the ambient temperature °C.

Case Temperature (T_C): $T_C = T_J - (\theta_{JC})\ (P_D)$

where: θ_{JC} is the thermal resistance of junction with respect to case.

Illustration: In order to calculate junction temperature (T_J) and case temperature (T_C) for static airflow for the Z86C04 in an 18L PDIP, we do the following:

1. At 25°C, maximum power dissipation for this device is 0.08 watts.

2. For our example, ambient temperature is denoted by T_A and is assumed to be 25°C.

For the Z86C04 in plastic (copper); θ_{JA} and θ_{JC} are 75 and 18°C/watt respectively.

Therefore, $T_J = 75 \times (0.08) + 25 = 31.2°C$, and

$T_C = 31.2 - (18 \times 0.08) = 29.8°C$

Table 11-1. Device θ_{JA}, θ_{JC} Table Summary Of Thermal Characteristics For ZiLOG Plastic Packages

Package Type	*Package Code*	θ_{JA}	θ_{JC}	*Lead Frame*
PDIP	**P**			
18L		75	18	Cu
20L		75	18	Cu
28L		60	12	Cu
40L		43	12	Cu
42L		42	11	Cu
48L		40	8	Cu
52L		38	8	Cu
64L		42	14	Cu
PLCC	**V**			
44L		46	13	Cu
68L		43	14	Cu
84L		42	12	Cu
QFP	**F**			
44L		45	10	Cu
80L		43	16	Cu
100L		38	17	Cu
VQFP	**A**			
64L		70	19	Cu
100L		100	25	Cu
SOIC	**S**			
8L		110	N/A	
18L		70	N/A	Cu
20L		75	N/A	Cu
28L		60	N/A	Cu
SSOP	**HZ**			
20L		75	18	Cu
28L		60	12	Cu
48L		45	12	Cu
EPT SSOP	**HT**			
28		36	10	Cu
LCC	**L**			
44L		53	7	
52L		48	10	
68L		40	6	

Table 11-2. Device θ_{JA}, θ_{JC} Table Summary Of Thermal Resistance For Hermetic Packages

PBGA	**B**			
256L		25	N/A	2 Layer
256L		21	N/A	4 Layer
CERDIP	**D**			
28		52	14	
40		41	11	
48		32	5	
Ceramic Side Braze	**C**			
18		81	21	
28		49	11	
40		48	11	
48		36	4	
Ceramic Window	**K**			
44L		32	3	
Pin Grid Array	**G**			
68L		36	6	

Notes:

P=Plastic DIP

C=Ceramic DIP

D=Cerdip

L=LCC-Ceramic Leadless Chip Carrier

V=PLCC-Plastic Leaded Chip Carrier

F=QFP-Plastic Quad Flat Pack

A=VQFP-Very Small Quad Flat Pack

G=Ceramic Pin Grid Array

S=SOIC-Small Outline Integrated Circuit

B=PBGA-Plastic Ball Grid Array

HZ=SSOP-Shrink Small Outline Package

HT=EPT SSOP-Exposed Pad Thin SSOP

CHAPTER 11

Glossary

TERM	DEFINITION
Å:	Symbol for Angstrom, which equals 10^{-10} meters (one ten-billionth of a meter).
Accelerated Life Test:	A life test, in which the applied stress level exceeds that needed in actual use in order to shorten the time required to observe failure. A good accelerated test should not alter the basic modes and/or mechanisms of failure.
Acceleration Factor:	The ratio of the times needed to obtain the same failure rates under two different sets of stress conditions involving the same failure modes or mechanisms.
Activation Energy (Ae):	The energy level needed to activate a specific failure mechanism.
AES:	Auger Electron Spectroscopy typically used for interlayer dielectrics and passivation films.
Align:	The operation of exposing a resist covered wafer in a projection printer.
APCVD:	Atmospheric Pressure Chemical Vapor Deposition. One method for deposition of glass used for interlayer or passivation dielectric.
ASSP:	Application Specific Standard Product.
AQL:	Acceptable Quality Level. Generally, 95 percent confidence that material of the stated AQL will pass sample inspection.
Bonding:	The act of connecting package leads to specified locations on the chip via fine wire.
Bond Pads:	Exposed aluminum pads on a chip to which wires from the package lead frame are bonded during assembly.
Burn-In:	The operation of a device prior to its application, at elevated temperature and/or voltage for a specific period of time. The purpose is to stabilize the device characteristics, identify early failures, and eliminate devices subject to infant mortality or excessive parametric drift.

TERM	DEFINITION
BPSG:	Boron doped Phosphosilicate Glass.
CD:	Critical Dimension.
CFA:	Customer Failure Analysis/Correlation Request.
C of C:	Certificate of Conformance.
CMOS:	Complementary MOS technology combining n and p transistors in the same product. Advantages include low power dissipation.
Confidence:	A specialized statistical term which refers to the probability of a statement being true.
Check:	A visual check done at the conclusion of a (dry or wet) masking step.
Chip:	One square on a wafer containing a single integrated circuit. The substrate on which all active and passive components of a circuit are fabricated; also called a die.
Clean Room:	The room in a chip fabrication plant in which wafers are processed. This area features a controlled environment with filtered air that eliminates essentially all dust and dirt.
Contact:	A connection between two conductive layers, e.g., metal-to-silicon contact.
Control limit:	A statistically defined limit which determines whether or not a process has changed significantly as compared to past history. A measure of statistical process control.
C-SAM:	C-Mode Scanning Acoustic Microscope which examines packaged units and produces high resolution, ultrasonic images.
CVD:	Chemical Vapor Deposition of thin films. Gaseous reactants are brought together over the silicon wafer, depositing required layers typically used for interlayer dielectrics and passivation films.
DC:	Document Control.
DESC:	Defense Electronic Supply Center.
DI:	Deionized water.
DIP:	Dual-in-Line Package.
DRC:	Design Rule Check.
DUT:	Device Under Test.
Depletion transistor:	A MOSFET with a permanently “on” channel; requires a negative applied gate voltage to turn off (see “enhancement transistor”).

TERM	DEFINITION
Develop:	A chemical process that solidifies photoresist where it has been exposed and removes it elsewhere (for negative resist) or vice versa (for positive resist).
Develop inspect:	A visual check following dry masking to verify proper resist patterning before etch, e.g., alignment and thickness are checked.
Die:	A single integrated circuit separated from the wafer on which it was made; also called a chip.
Diffusion:	The process of doping silicon by diffusing impurities from the surface into the wafer at high temperature. Any region in the silicon substrate doped by diffusion or by ion implant (e.g., source and drain diffusions).
Dopant:	Any impurity intentionally introduced into silicon to control its electronic behavior (e.g., Boron, Arsenic, and Phosphorus).
Dose:	In ion implant, a measure of the amount of dopant implanted; usually expressed in ions per square centimeter.
Drain:	A highly doped region adjacent to a transistor currently carrying channel. It carries electrons out of the transistor to the next circuit element or conductor.
Dry Masking:	A process segment where a photoresist is spun onto the wafer, soft baked, exposed, and developed to obtain a desired pattern ready for etch or implant (see "wet masking”).
EDX:	Energy Dispersive X-ray analysis. Normally uses electron beam excitation in the scanning electron microscope.
EOS:	Electrical overstress, common application failure mechanism.
ESD:	Electrostatic discharge, common handling failure mechanism.
Enhancement transistor:	A MOSFET with a normally “off” channel; requires a positive applied gate voltage to turn on (see “depletion transistor”).
Etch rate:	The rate at which a given layer is etched off in a given standard acid solution, expressed in Å/sec.
Evaporation:	Deposition technique for Aluminum, Gold, and Chromium thin films.
Expose:	Expose a photoresist-coated wafer to light through a mask.
FAE:	Field Application Engineer.
Final Test:	Measurement of assembled device performance. Products are categorized by speed/power/performance criteria.

TERM	DEFINITION
FIT:	"Failure units" or "Failure in Time," a measure of failure rate defined as one failure in 10^9, or one billion device hours.
FPO:	Finish Process Order. A lot traveler, which accompanies each lot through the finish (Mark and Pack and FQA) areas.
FQE:	Field Quality Engineer.
Gate:	The gate of a transistor.
Gate oxide:	Dielectric oxide between the gate and the channel region of a transistor.
Generic:	Devices similar in process or function. ZiLOG uses a generic approach in its Reliability Program. Devices built in the same wafer fab process and having similar complexity or function are grouped into a "generic" product family. Data on any device within a family is considered indicative of the performance of all other devices in that group and process line.
Gettering:	Trapping of contamination atoms (especially alkali ions) to prevent their drift into device regions where they may affect electrical performance.
Glass:	The amorphous form of SiO_2, used in various insulating layers on the wafer.
Hard Bake:	A step following dry masking, where the resist is heated to prepare it for wet etch.
HAST:	Highly Accelerated Stress Test.
HTOL:	High Temperature Operating Life.
IC:	Integrated Circuit.
Infant Mortality:	Initial failure rate in life studies. It is followed by early failure period and then final wear out portion of failure "bathtub" curve.
IQC:	Incoming Quality Control.
K:	Kilo, thousand, 10^3.
Layout:	A magnified, physical representation of an electronic circuit at the transistor level.
LCC:	Leadless Chip Carrier.
Lead:	The external connection to a packaged integrated circuit.
Life Test:	A test for the purpose of estimating some characteristic(s) of a device's useful lifetime.
LSI:	Large Scale Integration

TERM	DEFINITION
LPCVD:	Low Pressure Chemical Vapor Deposition. Typical method for deposition of glass used for interlayer or passivation dielectric.
LTO glass:	Low Temperature Oxide glass used for interlayer or passivation dielectric. Typically deposited at the same temperature as APCVD deposited glasses used for passivation, but at low pressure.
LTPD:	Lot Tolerance Percent Defective. A sample plan that will reject 90 percent of the lots equal to or worse than the stated LTPD value.
Mask:	A pattern usually “printed” on glass, used to define areas of the chip on the wafer for production purposes.
Masking:	The lithography portion of the process or physical area where lithography occurs.
MeV:	Million electron Volts.
meV:	Milli electron Volts.
MFG:	Manufacturing.
Mil:	0.001 inch.
MIL:	Military.
Mod:	Nampa Fabrication Module.
MOS:	Metal Oxide Semiconductor integrated circuit technology.
MRB:	Material Review Board.
MTBF:	Mean Time Between Failures.
MTTF:	Mean Time to Fail. Time to 50 percent Cumulative Fail.
Nano:	10^{-9}.
Negative photoresist:	A resist material in which unexposed areas are developed away.
NIST:	National Institute of Standards and Technology.
Nitride:	Silicon Nitride, Si_3N_4.
NMOS:	N channel MOS technology.
Nm:	Nanometer (1nm = 10A = 10^{-9} meters).
Ns:	Nanoseconds (10^{-9} seconds).
OEM:	Original Equipment Manufacturer.
OTP:	One Time Programmable Product sold in plastic packaging. No window is provided for UV erasure.
“Oxi”:	A process whereby thick oxide islands are grown between active device regions for better isolation and performance.

TERM	DEFINITION
Oxynitride:	A plasma deposited passivation or interlayer dielectric film consisting of silicon, oxygen, and nitrogen.
P:	Phosphorous.
PDIP:	Plastic Dual In-Line Package.
PE:	Product Engineer.
PECVD:	Plasma Enhanced Chemical Vapor Deposition.
PGA:	Pin Grid Array (package).
PLCC:	Plastic Leaded Chip Carriers.
PM:	Procedural Manual that contains ZiLOG's policies and procedures.
POA:	Point of Acceptance.
PPM:	PPM Quality Data, Parts per Million defective; 1000 PPM = 0.1 percent defective.
PPOT:	Pressure Pot.
PROM:	Programmable Read Only Memory.
PSG:	Phosphosilicate Glass. A glass containing phosphorus (in the form of P_20_5). LTO, Pyrox and Pyroglass are all types of PSG.
Package:	The container used to hold an active semiconductor device.
Photolithography:	The portion of the process involving the use of light sensitive photoresist material for layer definition.
Photomask:	(1) A patterned chrome on glass photographic plate used to transfer a pattern to photo-resist in dry masking. (2) A process segment involving the patterning of a given layer by use of a photomask.
Photoresist:	A light sensitive polymer material which is used as a mask for etching and ion implant steps. See also Negative and Positive Photoresist.
Plasma ash:	A process using a gas transformed by an RF field into a reactive plasma.
Plasma deposition:	Deposition of thin films using gaseous reactants in the presence of a plasma for lower temperatures.
Plasma etch:	An etching process using a gas transformed by an RF field into a reactive plasma.
Poly:	Polycrystalline silicon made up of many tiny crystals (as opposed to single crystal silicon.

TERM	DEFINITION
Poly Re-ox:	Oxidation of the poly after it has been defined. The re-ox provides the interpoly di-electric in a double (two layer) poly process.
Positive photoresist:	A photosensitive organic polymer material in which exposed areas are developed away.
Prebake:	First step of dry masking, in which the wafers are dried in an oven prior to resist application.
Probe:	The first electrical test of processed wafers.
Process Templating:	The profile displayed by the process evaluation parameters, which are automatically recorded from the test patterns on wafers as they proceed through the production line.
Projection Aligner:	A machine which projects the photomask onto the resist-coated wafer. The mask is the same size as the wafer and imaged 1:1 on the wafer.
Pyrox:	A type of phosphosilicate glass containing approximately 4.5 wt Phosphorous.
QA:	Quality Assurance.
QE:	Quality Engineer.
QR-XXXX:	Product or Process Qualification Report (XXXX = report number).
RBS:	Rutherford Back Scattering. A method for non-destructive depth profile analysis of thin films by back scattering of high-energy helium ions.
RE:	Reliability Engineer.
RGA:	Residual Gas Analysis.
QFP:	Quad Flat Package.
QIP:	Quality Improvement Process.
Q&R:	Quality and Reliability.
RH:	Relative Humidity.
RIE:	Reactive Ion Etch.
RMA:	Return Material Authorization.
ROM:	Read Only Memory.
Refractive Index:	A basic physical property which determines the extent of light bending (refraction) upon entering the surface. Used in thin film process control as an indirect measure of chemistry.
Resist:	See Photoresist.

TERM	DEFINITION
SDE:	Statistical Design of Experiments.
SEM:	Scanning Electron Microscope. A microscope which makes use of a scanning beam of electrons to image detail less than 100A in size (surface only).
SIMS:	Secondary Ion Mass Spectroscopy.
SL-Lot:	Special Lot. ZiLOG identification used to identify products designed to unique customer requirements.
SPC:	Statistical Process Control.
STS:	Ship-to-Stock. Eliminates need for customer IQC.
Silicon:	Metallic element which forms the substrate in most semiconductor devices.
Soft bake:	A step preparing freshly spun photoresist for exposure by baking it in an oven (to remove excess solvent).
SOIC:	Small Outline Integrated Circuit package.
Source:	Equivalent to the drain of a transistor with the exception that electrons leave the source into the channel of the active device.
Spec. Limit:	Absolute acceptable limit for a process parameter.
Spin:	A process step which coats a spinning wafer with liquid photoresist by dispensing the liquid onto its center.
Sputtering:	Deposition of a metal layer by bombarding a metal target with heavy ions from a gaseous (e.g., argon) plasma. Metal atoms are removed from the target and deposited onto the wafer during this process.
TD:	Technology Development.
TDDB:	Time Dependent Dielectric Breakdown.
TEM:	Transmission Electron Microscope. A microscope used to obtain high-resolution images with a transmitted electron beam by electron lens imaging rather than scanning.
THB:	Temperature Humidity Bias (85°C/85% RH).
TSOP:	Thin small outline package.
Test patterns:	Special electrical test structures included on production device wafers for monitoring critical parameters.
Thermal oxide:	A high quality Si_{O2} layer grown by oxidizing the silicon in a furnace (as opposed to externally deposited glass).
UL:	Underwriters Laboratory.

TERM	DEFINITION
UV:	Ultra Violet.
V/I:	A monitor measuring voltage and current between probes applied to a semiconductor layer. Measures layer resistivity.
Visual:	A check of process quality by examination of wafers under a light microscope.
VLSI:	Very Large Scale Integration.
VQFP:	Very small Quad Flat Pack package.
Vt:	Transistor threshold voltage. Voltage at which the transistor turns on.
Wafer:	A thin piece of silicon sliced from a cylinder shaped crystal. It is polished so that the surface is like a mirror. It is most commonly found in 4, 5, and 6-inch diameters. The wafer is the base material for most of the world's integrated circuits.
Wafer flat:	A flat area ground onto the original silicon ingot from which the wafers are sliced. Gives crystallographic orientation.
Waterfall Guardbanding:	The technique of testing a circuit at different levels of the manufacturing process, to insure above marginal product performance and compliance.
Wet masking:	Process segment following "dry masking" in which the wafer, covered with the resist pattern, is etched to transfer the resist pattern to the wafer. The resist is then removed (includes wet and/or plasma etching).
Wet etch:	Etching in a liquid acid or solution.
Wire bonding:	The process of connecting thin wires from the chip's bond pads to the package lead. (This is done at assembly.)
ZD:	Zero Defects.
ZEPI:	ZiLOG Electronics Philippines, Inc.
ZUS:	ZiLOG Corporate Headquarters, San Jose, California.